LONGTECH

OPTICS

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Jimei North Area Xiamen China.

SPECIFICATIONS OF LCD MODULE

MODULE NO : LGC12865A-FSW-GBW

DOC.REVISION: 00

	SIGNATURE	DATE
PREPARED BY (RD ENGINEER)	QIU	2009-6-5
CHECKED BY	Chen	2009-6-5
APPROVED BY	yfe	2009-6-5

DOCUMENT REVISION HISTORY

VERSINO	DATE	DESCRIPTION	CHANGED BY
00	Jun-5-2009	First issue	

CONTENTS

1. Features

1. 128*65 dots
2. 68 or 80 MPU interfaces
3. Built-in controller (SPLC501C)
4. Display Mode & Backlight Variations
5. ROHS Compliant

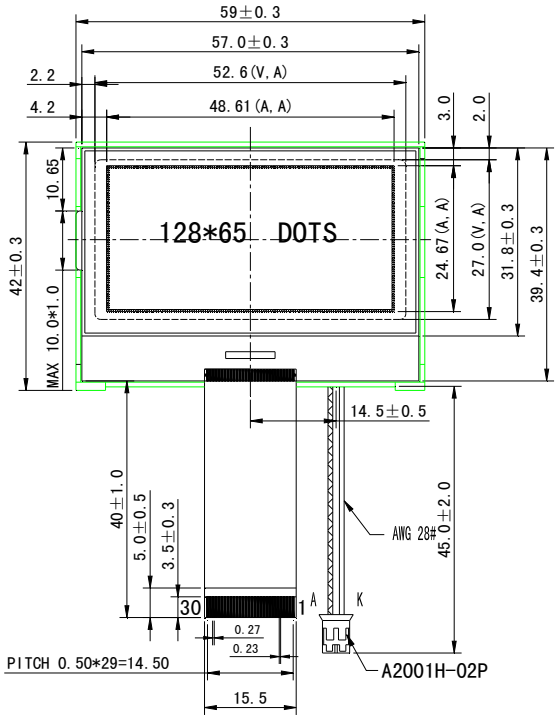
LCD type	☐TN			
	☐FSTN	☐FSTN Negative		
	☐STN Yellow Green	☑STN Gray	☐STN Blue Negative	
View direction	☑6 O'clock	☐12 O'clock		
Rear Polarizer	☐Reflective	☑Transflective	☐Transmissive	
Backlight Type	☑LED	☐EL	☐Internal Power	☑3.0V Input
		☐CCFL	☑External Power	☐5.0V Input
Backlight Color	☑White	☐ Blue	☐ Amber	☐Yellow-Green
Temperature Range	☐Normal	☑Wide	☐Super Wide	
DC to DC circuit	☑Build-in	☐Not Build-in		
Touch screen	☐With	☑Without		
Font type	☐English-Japanese	☐English-European	☐English-Russian	☑other

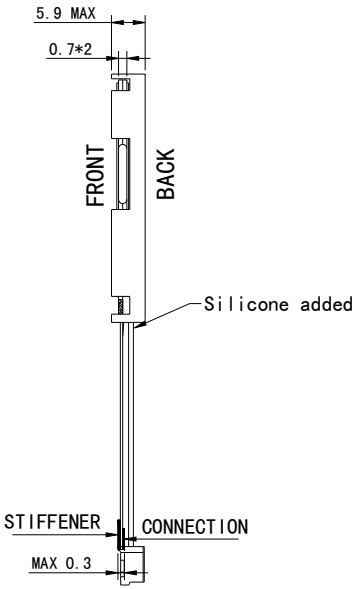
2. MECHANICAL SPECIFICATIONS

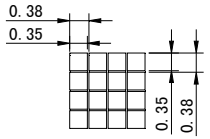
Module size	59.0mm(L)*39.4mm(W)*5.9mm(H)
Viewing area	52.6mm(L)*27.0mm(W)
Dots size	0.35mm(L)*0.35mm(W)
Dots pitch	0.38mm(L)*0.38mm(W)
Weight	Approx.

3. Outline dimension

REV	DESCRIPTION:	DATE
1.0	First connector wire spec	2008.07.09



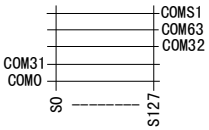




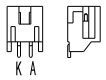
PIXEL DETAILS

PIN CONNECTIONS:

PIN	SIGNAL	PIN	SIGNAL
1	/CS1	16	VOUT
2	/RES	17	CAP3N
3	A0	18	CAP1P
4	/RW	19	CAP1N
5	E(RD)	20	CAP2N
6	DB0	21	CAP2P
7	DB1	22	V1
8	DB2	23	V2
9	DB3	24	V3
10	DB4	25	V4
11	DB5	26	V5
12	DB6	27	VR
13	DB7	28	C86
14	VDD	29	PS
15	VSS	30	IRS

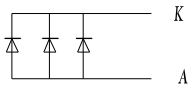


LCD LAYOUT



A2001WR-S-02PD01

LED CIRCUIT



Specification:

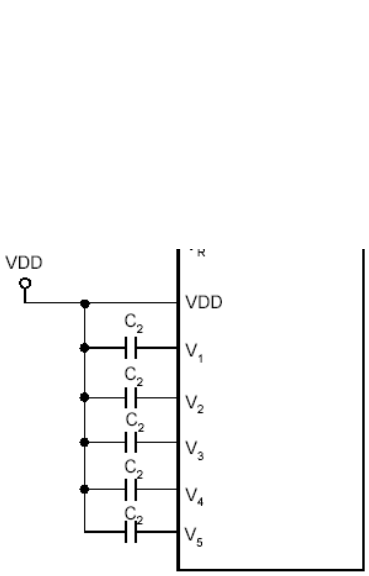
1). Driving: Duty:1/65, 1/9 Bais, Vlcd: 9.5V
2). Viewing Direction: 6 O'clock
3). Display mode: STN(Gray)/positive/transflective
4). Ledbacklight: White Color, 3~3.3V, Curent: 45~60mA
5). Operating temp.: -20°c~+70°C
    Storage temp.: -30°c~+80°C
6). Driver : SPLC501C VDD:3.3V
7). Unmarked Tolerances: ±0.2mm
8). RoHS Compliant

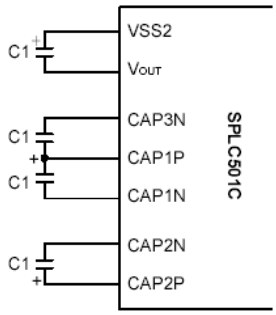
Model Name: LGC12865A-FSW-GBW		LONGTECH OPTICS CO,. LTD.
GENERAL TOL: ± 0.2		
APPROVALS	DATE	DRAWN NO. / SCALE: 1:1
DWN: Qipei Qiu		
CHK:		SIZE: A4 / UNIT: mm / Page: 1-1
APP: Guoxiang Ye		

4. Absolute maximum ratings

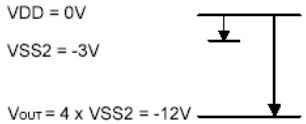
Item	Symbol	Standard			Unit
Power voltage	V_{DD}-V_{SS}	0	-	6.0	V
Input voltage	V_{IN}	VSS	-	VDD	
Operating temperature range	V_{OP}	-20	-	+70	℃
Storage temperature range	V_{ST}	-30	-	+80	

5. Block diagram





4 x step-up voltage circuit



4 x step-up voltage relationships

Capacitance: C1=1uF~2.2uF, C=0.47uF~2.2uF

6. Interface pin description

Pin no.	Symbol	External connection	Function
1	/CS	MPU	Used to enter chip select signal
2	/RESET	MPU	Controller reset (module reset)
3	A0	MPU	Register select signal
4	R/W	MPU	Read/write select signal
5	E	MPU	Operation (data read/write) enable signal
6~10	DB0~DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
11~13	DB4~DB7	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
14	V_{DD}	Power supply	Power supply for logic (+5V) for LCM
15	V_{SS}		Signal ground for LCM (GND)
16	VOUT		DC/DC voltage converter.
17	CAP3-		
18	CAP1+		
19	CAP1-		
20	CAP2-		
21	CAP+		
22~26	V1~V5	Power for LCD	A multi-level power supply for the liquid crystal drive.
27	VR		Output voltage regulator terminal.
28	C86	MPU	This is the MPU interface switch terminal.
29	PS	MPU	This is the parallel input/serial data input switch terminal.
30	/IRS	MPU	This terminal selects the resistors for the V5 voltage level adjustment.

7. Display data RAM

5.5. Display Data RAM

5.5.1. Display data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (8 page x 8 bit +1) x 132-bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the DB7 - 0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple SPLC501C chips are used. Therefore, display structures can be created easily and with a high degree of freedom.

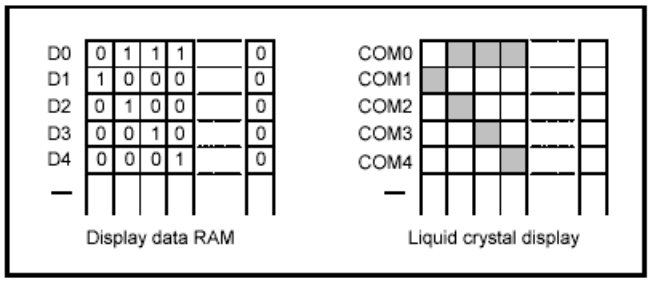


Figure 3

Moreover, reading from and writing to the display RAM in the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

5.5.2. The page address circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address 8 (DB3, DB2, DB1, DB0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data DB0 is used.

5.5.3. The column addresses

As is shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the increment of column addresses stops with 83H. Because the column address depends on the page address, it is necessary to re-specify both the page address and the column address when moving, for example, from page 0 column 83H to page 1 column 00H. Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0	SEG131
ADC '0'	0 (H) →	Column Address → 83(H)
(DB0) '1'	83(H) ←	Column Address ← 0(H)

5.5.4. The line address circuit

The line address circuit, as shown in Figure 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, which is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal and the COM63 output for SPLC501C when the common output mode is reversed. The display area is a 65-line area for the SPLC501C from the display start line address. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, …etc. can be performed.

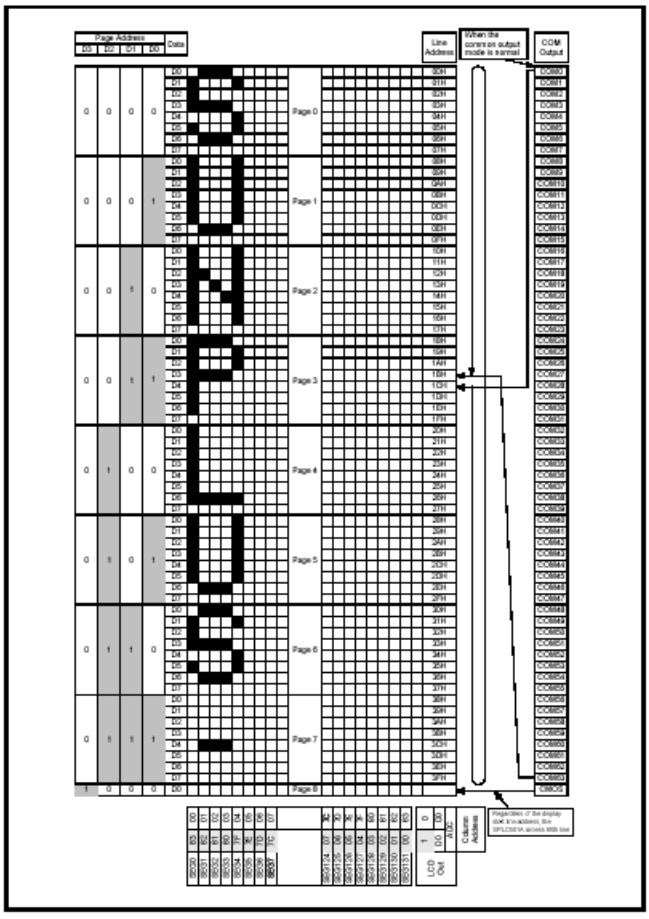


Figure 4

5.6. The Display Data Latch Circuit

The display data latch circuit temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

5.7. The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when MS = 'H' and CLS = 'H'. When CLS = 'L', the oscillation stops, and the display clock is input through the CL terminal.

5.8. The Common Output Status Select

In the SPLC501C chips, the COM output scan direction can be selected by the common output status select command (See Table 5.). Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 5

Status	COM Scan Direction
	SPLC501C
Normal	COM0→COM63
Reverse	COM63→COM0

5.9. Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display. Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive-wave form using a 2-frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

8. Contrast adjust

5.11.2. The voltage regulator circuit

The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V_5 through the voltage regulator circuit. Because the SPLC501C chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. Moreover, in the SPLC501C, two types of thermal gradients have been prepared as V_{REG} options: (1) approximately -0.05%/℃ and (2) external input (supplied to the VRS terminal).

5.11.2.1. When the V_5 voltage regulator internal resistors are used

Through the use of the V_5 voltage regulator internal resistors and the electronic volume function, the liquid crystal power supply voltage, V_5, can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V_5 voltage can be calculated using equation A-1 over the range where $|V_5| < |V_{OUT}|$.

$$V_5 = \left\{1+\frac{Rb}{Ra}\right\} \bullet V_{EN}$$

$$= \left\{1+\frac{Rb}{Ra}\right\} \bullet \left\{1-\frac{\alpha}{162}\right\} \bullet V_{REG}$$

$$\left[\because V_{EN} = (1-\alpha/162) \bullet V_{REG}\right] \qquad \text{Equation A-1}$$

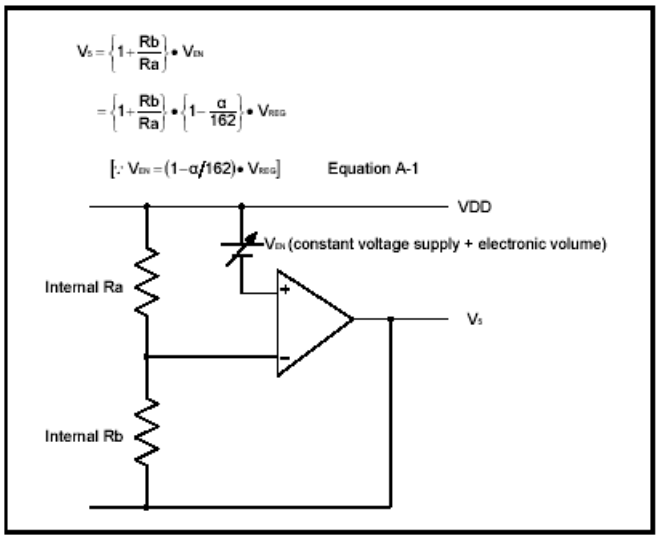


Figure 8

V_{REG} is the IC-internal fixed voltage supply, and its voltage at T_A = 25℃ is as shown in Table 9.

Table 9

Equipment Type	Thermal Gradient	Units	VREG	Units
(1) Internal Power Supply	-0.05	[%/℃]	-2.1	[V]
(2) External Input	-	-	VRS	[V]

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for depending on the electronic volume register settings.

Table 10

DB5	DB4	DB3	DB2	DB1	DB0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
:	:	:	:	:	:	:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra is the V_5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V_5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V_5 voltage regulator internal resistor ratio register.

V_5 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			SPLC501C	
			Equipment Type by Thermal Gradient [Units: %/℃]	
DB2	DB1	DB0	(1) -0.05	(2) VREG External Input
0	0	0	3.0	1.5
0	0	1	3.5	2.0
0	1	0	4.0	2.5
0	1	1	4.5	3.0
1	0	0	5.0	3.5
1	0	1	5.5	4.0
1	1	0	6.0	4.5
1	1	1	6.4	5.0

5.11.2.2. When an external resistance is used (i.e., The V_5 Voltage Regulator Internal Resistors are not used) (1)

The liquid crystal power supply voltage V_5 can also be set without using the V_5 voltage regulator internal resistors (IRS terminal = 'L') by adding resistors Ra' and Rb' between VDD and VR, and between VR and V_5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V5 through commands. In the range where $|V_5| < |V_{OUT}|$, the V_5 voltage can be calculated using equation B-1 based on the external resistance, Ra' and Rb'.

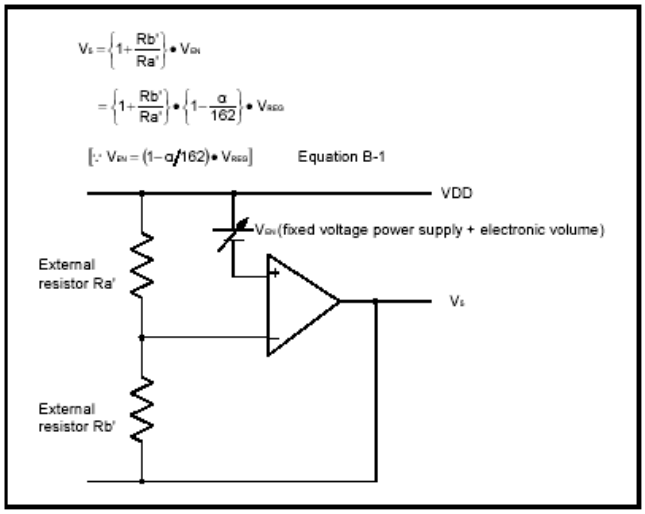


Figure 9

Setup example: When selecting T_A = 25℃ and V_5 = -7.0V for an SPLC501C model where the temperature gradient = -0.05%/℃. When the central value of the electron volume register is (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0, 0), then α = 31 and V_{REG} = -2.1V. According to equation B-1:

$$V_5 = \left\{1+\frac{Rb'}{Ra'}\right\} \bullet V_{EN}$$

$$-7.0V = \left\{1+\frac{Rb'}{Ra'}\right\} \bullet \left\{1-\frac{\alpha}{162}\right\} \bullet (-2.1) \qquad \text{Equation B-2}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5μA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{Equation B-3}$$

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$

$$Ra' = 340k\Omega$$

$$Rb' = 1060k\Omega$$

At this time, the V_5 voltage variable range and notch width, based on the electron volume function, is as given in Table 12.

Table 12

V_5	Min.	Typ.	Max.	Units
Variable Range	-8.6 (63 levels)	-7.0 (central value)	-5.3 (0 level)	[V]
Notch width	-	52	-	[mV]

5.11.2.3. When external resistors are used (i.e. The V_5 Voltage Regulator Internal Resistors Are Not Used). (2)

When the external resistor described above are used, adding a variable resistor makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V_5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V_5 by commands to adjust the liquid crystal display brightness. In the range where $|V_5| < |V_{OUT}|$ the V_5 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistor) and R3 settings, where R2 can be subjected to fine adjustments (△R2).

$$V_5 = \left\{1+\frac{R_3+R_2-\Delta R_2}{R_1+\Delta R_2}\right\} \bullet V_{EN}$$

$$= \left\{1+\frac{R_3+R_2+\Delta R_2}{R_1+\Delta R_2}\right\} \bullet \left\{1-\frac{\alpha}{162}\right\} \bullet (V_{REG})$$

$$\left[\because V_{EN} = (1-\alpha/162) \bullet V_{REG}\right] \qquad \text{Equation C-1}$$

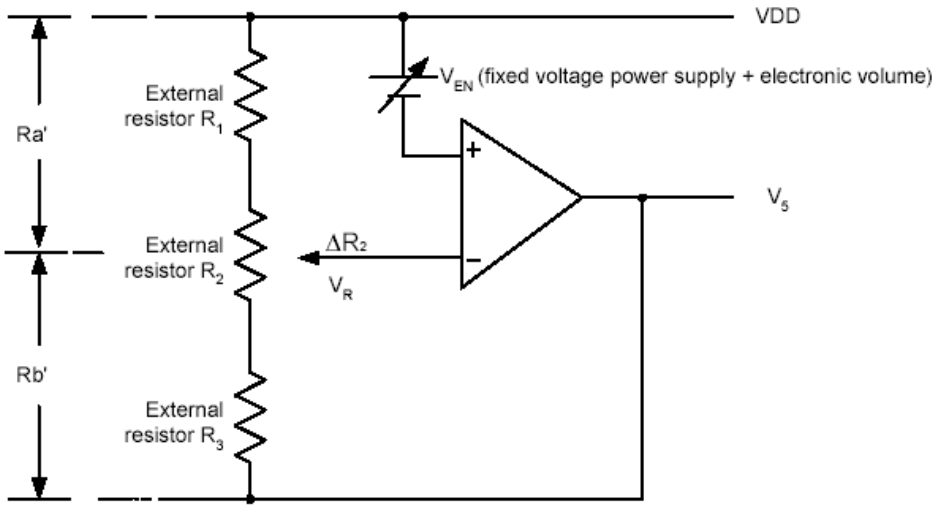


Figure 10

Setup example: When selecting T_A = 25℃ and V_5 = -5.0V to -9.0V (using R2) for an SPLC501C model where the temperature gradient = -0.05%/℃.

When the central value for the electronic volume register is set at (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0, 0),

α = 31
V_{REG} = -2.1V

so, according to equation C-1, when △R2 = 0Ω , in order to make V_5 = -9.0V,

$$-9.0V = \left\{1+\frac{R_3+R_2}{R_1}\right\} \bullet \left\{1-\frac{31}{162}\right\} \bullet (-2.1) \qquad \text{Equation C-2}$$

When △R2 = R2, in order to make V = -5.0V,

$$-5.0V = \left\{1+\frac{R_3}{R_1+R2}\right\} \bullet \left\{1-\frac{31}{162}\right\} \bullet (-2.1) \qquad \text{Equation C-3}$$

Moreover, when the current flowing VDD and Vs is set to 5μA,

R1 + R2 + R3 = 1.4MΩ Equation C-4

With this, according to equation C-2, C-3 and C-4,

R1 = 264kΩ
R2 = 211kΩ
R3 = 925kΩ

At this time, the Vs voltage variable range and notch width based on the electron volume function is as shown in Table 13.

Table 13

V_5	Min.	Typ.	Max.	Units
Variable Range	-8.6 (63 levels)	-7.0 (central value)	-5.3 (0 level)	[V]
Notch width	-	53	-	[mV]

Note1: When the V_5 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.

Note2: The VR terminal is enabled only when the V_5 voltage regulator internal resistors are not used (i.e. the IRS terminal = 'L'). When the V_5 voltage regulator internal resistors are used (i.e. when the IRS terminal = 'H'), the VR terminal is left open.

Note3: Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

5.11.3. The liquid crystal voltage generator circuit

The V_5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for SPLC501C can be selected.

5.12. High Power Mode

The power supply circuit equipped in the SPLC501C chips has very low power consumption (normal mode: $\overline{HPM}$ = 'H'). However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the $\overline{HPM}$ terminal to 'L' (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode. Moreover, if the improvement to the display is inadequate even after high power mode has been set, it is necessary to add a liquid crystal drive power supply externally.

5.13. The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 11 is recommended for shutting down the internal power supply. First place the power supply in power saver mode and then turn the power supply OFF.

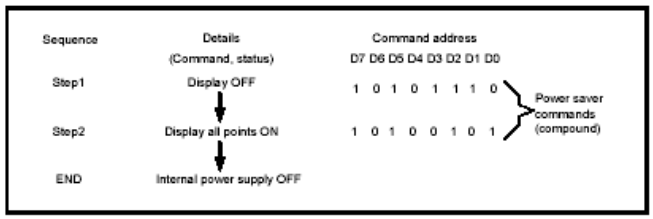


Figure 11

9. Optical characteristics

STN type display module (Ta=25℃, VDD=3.3V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_r \geqslant 4$	-25	-	-	deg
	Φ		-30	-	30	
Contrast ratio	C_r		-	2	-	-
Response time (rise)	T_r	-	-	120	150	ms
Response time (fall)	T_r	-	-	120	150	

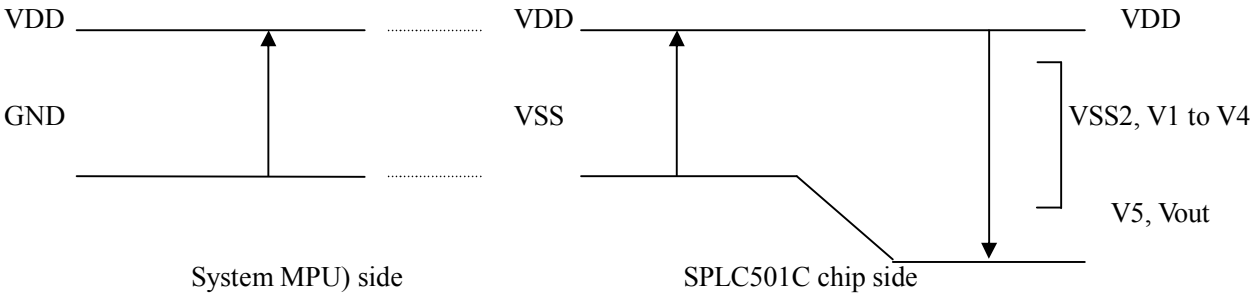
FSTN type display module (Ta=25℃, VDD=3.3V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_r \geqslant 2$	-60	-	35	deg
	Φ		-40	-	40	
Contrast ratio	C_r		-	6	-	-
Response time (rise)	T_r	-	-	150	250	ms
Response time (fall)	T_r	-	-	150	250	

10. Electrical characteristics

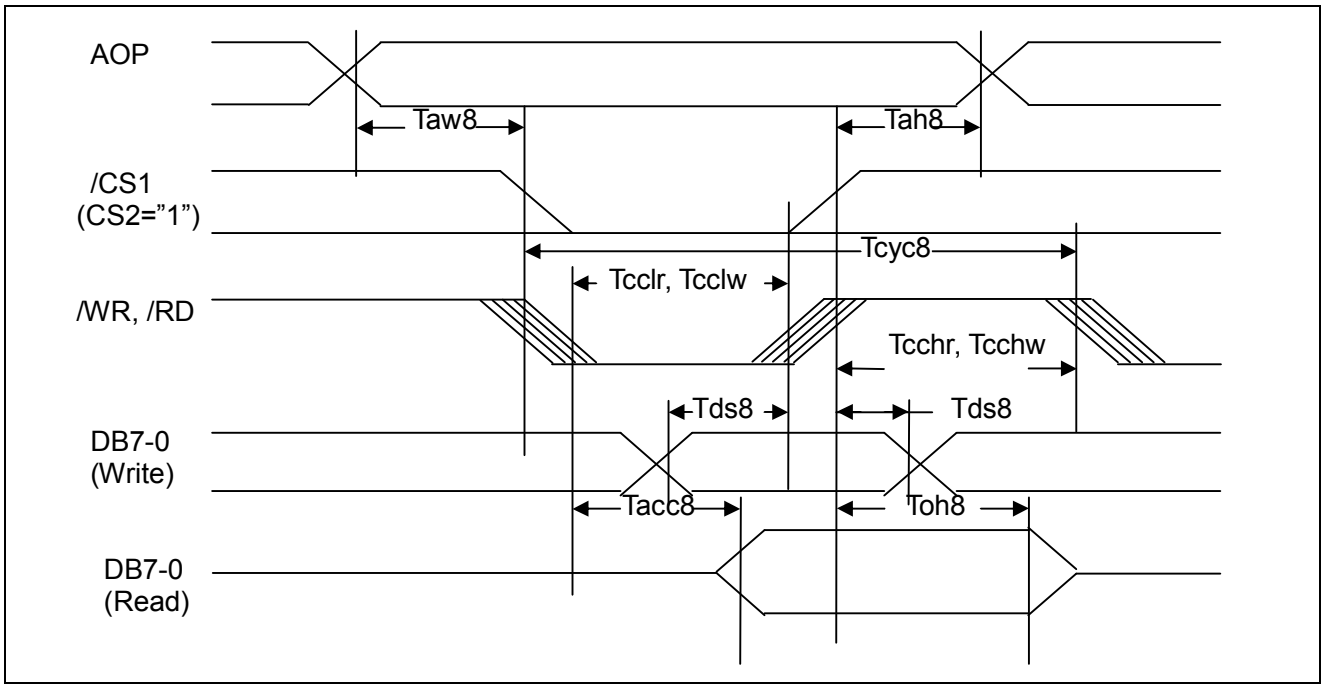
DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	V_{DD}-V_0	Ta =25℃	-	8.8	-	V
Input voltage	V_{DD}		3.0	3.3	3.5	
Supply current	I_{DD}	Ta=25℃, V_{DD}=3.3V	-	0.25	0.45	mA
Input leakage current	I_{LKG}		-	-	1.0	uA
“H” level input voltage	V_{IH}		2.2	-	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	-	0.6	
“H” level output voltage	V_{OH}	LOH=-0.25mA	2.4	-	-	
“L” level output voltage	V_{OL}	LOH=1.6mA	-	-	0.4	
Backlight supply voltage	V_F		-	3.0	-	
Backlight supply current	I_{LED}	V_F=3.0V	-	45	-	mA



11. Timing Characteristics

System bus read/write characteristics 1 (for the 8080 series MPU)



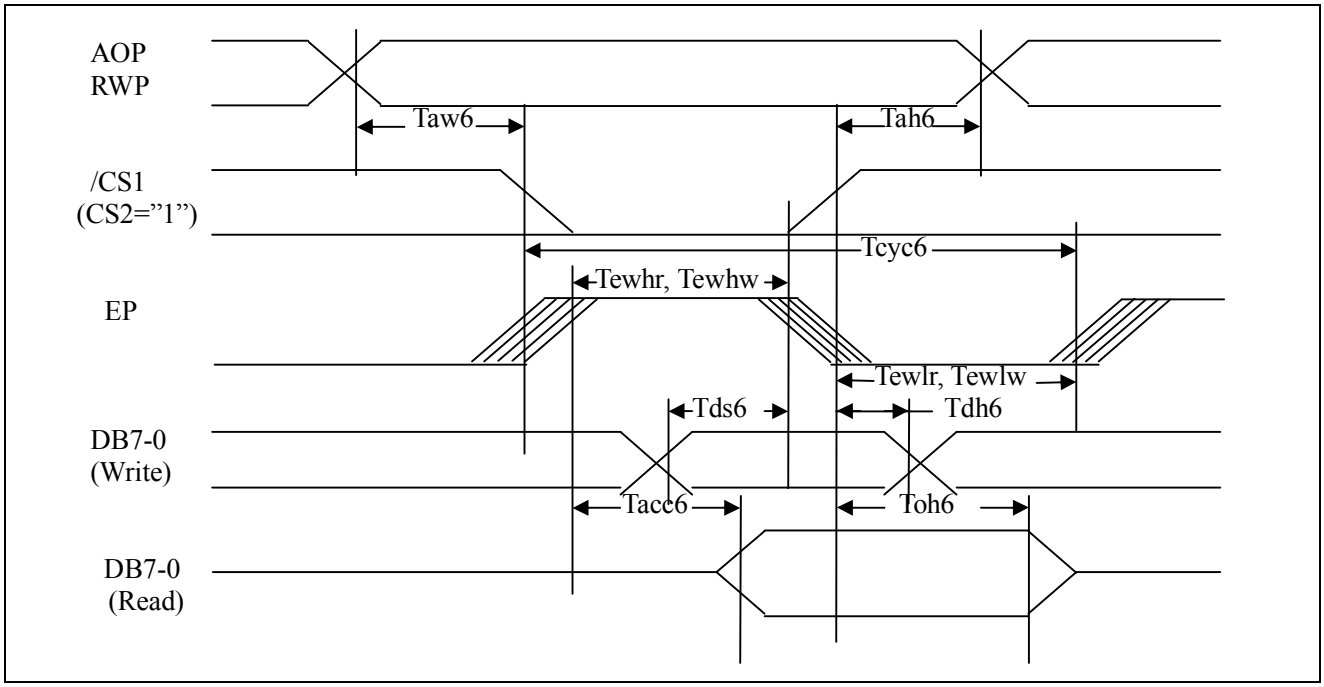
12. (VDD=4.5V to 5.5V, Ta=25C)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	AOP	Tah8		0	-	ns
Address setup time		Taw8		0	-	ns
System cycle time	AOP	Tcyc8		166	-	ns
Control L pulse with (/WR)	/WR	Tcclw		30	-	ns
Control L pulse with (/RD)	/RD	Tcclr		70	-	ns
Control H pulse with (/WR)	/WR	Tcchw		30	-	ns
Control H pulse with (/RD)	/RD	Tcchr		30	-	ns
Data setup time	DB7-0	Tds8		30	-	ns
Address hold time		Tdh8		10	-	ns
/RD access time		Tacc8	Cl=100pF	-	70	ns
Output disable time		Toh8		5.0	50	ns

13. (VDD=2.7V to 4.5V, Ta=25C)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	AOP	Tah8		0	-	ns
Address setup time		Taw8		0	-	ns
System cycle time	AOP	Tcyc8		300	-	ns
Control L pulse with (/WR)	/WR	Tcclw		60	-	ns
Control L pulse with (/RD)	/RD	Tcclr		120	-	ns
Control H pulse with (/WR)	/WR	Tcchw		60	-	ns
Control H pulse with (/RD)	/RD	Tcchr		60	-	ns
Data setup time	DB7-0	Tds8		40	-	ns
Address hold time		Tdh8		15	-	ns
/RD access time		Tacc8	Cl=100pF	-	140	ns
Output disable time		Toh8		10	100	ns

System bus read/write characteristics 1 (for the 6800 series MPU)



14. (VDD=4.5V to 5.5V, Ta=25C)

Item		Signal	Symbol	Condition	Rating		Unit
					Min.	Max.	
Address hold time		AOP	Tah6		0	-	ns
Address setup time			Taw6		0	-	ns
System cycle time		AOP	Tcyc6		166	-	ns
Data setup time		DB7-0	Tds6	Cl=100pF	30	-	ns
Data hold time			Tdh6		10	-	ns
Access time			Tacc6		-	70	ns
Output disable time			Toh6		10	50	ns
Enable H pulse time	Read	EP	Tewhr		70	-	ns
	Write		Tewhw		30	-	ns
Enable L pulse time	Read	EP	Tewlr		30	-	ns
	Write		Tewlw		30	-	ns

15. (VDD=2.7V to 4.5V, Ta=25C)

Item		Signal	Symbol	Condition	Rating		Unit
					Min.	Max.	
Address hold time		AOP	Tah6		0	-	ns
Address setup time			Taw6		0	-	ns
System cycle time		AOP	Tcyc6		300	-	ns
Data setup time		DB7-0	Tds6	Cl=100pF	40	-	ns
Data hold time			Tdh6		15	-	ns
Access time			Tacc6		-	140	ns
Output disable time			Toh6		10	100	ns
Enable H pulse time	Read	EP	Tewhr		120	-	ns
	Write		Tewhw		60	-	ns
Enable L pulse time	Read	EP	Tewlr		60	-	ns
	Write		Tewlw		60	-	ns

12. Table of LCM commands

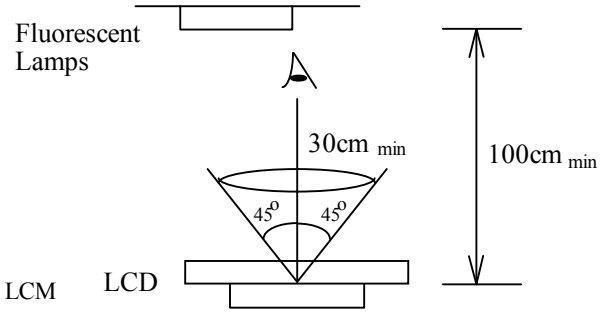
Command	Command Code											Function
	AOP /WR		/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1 DB0		
1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
2) Display start line set	0	1	0	0	1	Display start address						Set the display RAM display start line address
3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address
Column address set Lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address
5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
6) Display data write	1	1	0	Write data								Writes the status RAM
7) Display data read	1	0	1	Read data								Reads from the display RAM
8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/reverse 0: normal, 1: reverse
10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD driver voltage bias ratio SPLC501C…..0: 1/9, 1: 1/7
12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
17) V5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V5 output voltage electronic volume register
Electronic volume register set	0	1	0	*	*	Electronic volume value						
19) Static indicator ON/OFF				1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
Static indicator Register set				*	*	*	*	*	*	Mode		Set the flashing mode
20) Page Blink	0	1	0	1	1	0	1	0	1	0	1	P7-0: 1 – blinking page 0 – no blinking, normal display
Page selection	0	1	0	P7	P6	P5	P4	P3	P2	P1	P0	
21) Driving Mode set	0	1	0	1	1	0	1	0	0	1	0	Set the driving mode register Driving capability (D1, D0): (1,1)>(0,0)>(0,1)>(1,0)
Mode selection	0	1	0	D1	D0	0	0	0	0	0	0	
22) Power saver												Display OFF and display all points ON compound command

13. QUALITY SPECIFICATIONS

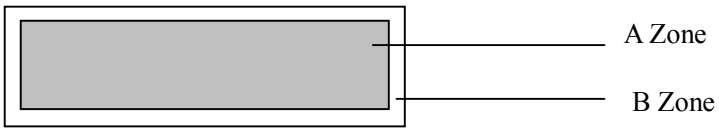
13.1 Standard of the product appearance test

Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps. Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 30 cm or more.

Viewing direction for inspection is 45° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).
B Zone: Non-active display area (outside viewing area).

13.2 Specification of quality assurance

AQL inspection standard

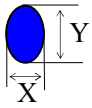
Sampling method: MIL-STD-105E, Level II, single sampling

Defect classification **(Note: * is not including)**

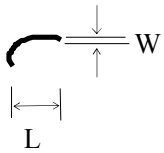
Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction		
		Contrast defect (dim, ghost)	2	
		Back-light	1,8	
	Non-display	Flat cable or pin reverse	10	
		Wrong or missing component	11	
Minor	Display state	Background color deviation	2	1.0
		Black spot and dust	3	
		Line defect, Scratch	4	
		Rainbow	5	
		Chip	6	
		Pin hole	7	
	Polarizer	Protruded	12	
		Bubble and foreign material	3	
	Soldering	Poor connection	9	
	Wire	Poor connection	10	
	TAB	Position, Bonding strength	13	

Note on defect classification

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td rowspan="6">1</td><td>Short or open circuit</td><td rowspan="6">Not allow</td></tr>
<tr><td>LC leakage</td></tr>
<tr><td>Flickering</td></tr>
<tr><td>No display</td></tr>
<tr><td>Wrong viewing direction</td></tr>
<tr><td>Wrong Back-light</td></tr>
<tr><td rowspan="2">2</td><td>Contrast defect</td><td rowspan="2">Refer to approval sample</td></tr>
<tr><td>Background color deviation</td></tr>
<tr><td>3</td><td>Point defect,
Black spot, dust
(including Polarizer)

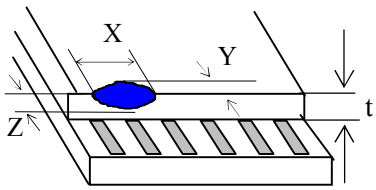
ϕ = (X+Y)/2</td><td> 

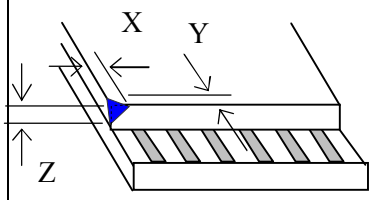
<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>ϕ≤0.10</td><td>Disregard</td></tr>
<tr><td>0.10<ϕ≤0.20</td><td>3</td></tr>
<tr><td>0.20<ϕ≤0.25</td><td>2</td></tr>
<tr><td>0.25<ϕ≤0.30</td><td>1</td></tr>
<tr><td>ϕ>0.30</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>4</td><td>Line defect,

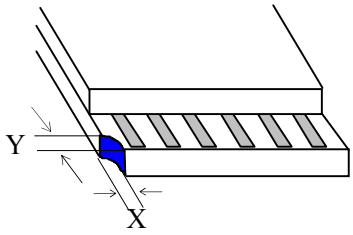
Scratch</td><td> 

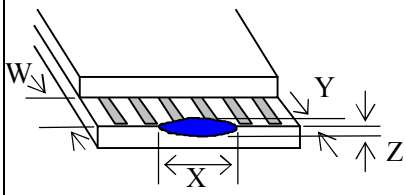
<table>
<tr><th colspan="2">Line</th><th>Acceptable Qty.</th></tr>
<tr><td>L</td><td>W</td><td></td></tr>
<tr><td>---</td><td>0.015≥W</td><td>Disregard</td></tr>
<tr><td>3.0≥L</td><td>0.03≥W</td><td rowspan="2">2</td></tr>
<tr><td>2.0≥L</td><td>0.05≥W</td></tr>
<tr><td>1.0≥L</td><td>0.1>W</td><td>1</td></tr>
<tr><td>---</td><td>0.05<W</td><td>Applied as point defect</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two color changes across the viewing area.</td></tr>
</table>

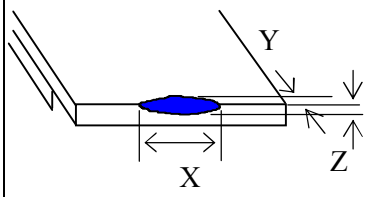
<table>
<tr><th>No</th><th>Item</th><th>Criterion</th></tr>
<tr><td>6</td><td>Chip

Remark:
X: Length direction
Y: Short direction
Z: Thickness direction
t: Glass thickness
W: Terminal Width</td><td>


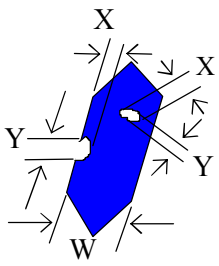
Acceptable criterion
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤2</td><td>0.5mm</td><td>≤t/2</td></tr>
</table>


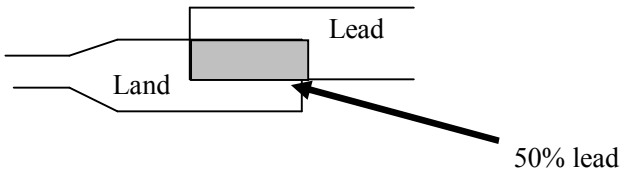
Acceptable criterion
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤2</td><td>0.5mm</td><td>≤t</td></tr>
</table>


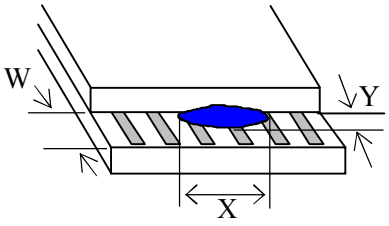
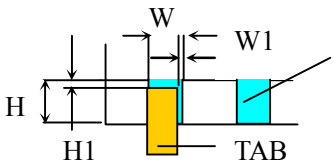
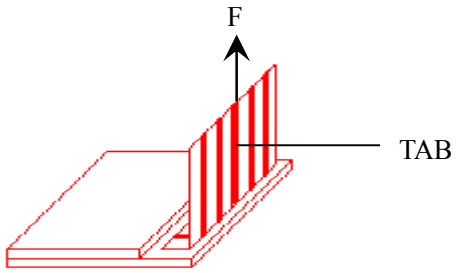
Acceptable criterion
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3</td><td>≤2</td><td>≤t</td></tr>
<tr><td colspan="2">shall not reach to ITO</td><td></td></tr>
</table>


Acceptable criterion
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>Disregard</td><td>≤0.2</td><td>≤t</td></tr>
</table>


Acceptable criterion
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤5</td><td>≤2</td><td>≤t/3</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>7</td><td>Segment
pattern
W = Segment width
ϕ = (X+Y)/2</td><td>(1) Pin hole
ϕ < 0.10mm is acceptable.
 

<table>
<tr><th>Point Size</th><th>Acceptable Qty</th></tr>
<tr><td>ϕ≤1/4W</td><td>Disregard</td></tr>
<tr><td>1/4W< ϕ≤1/2W</td><td>1</td></tr>
<tr><td>ϕ>1/2W</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>8</td><td>Back-light</td><td>(1) The color of backlight should correspond its specification.
(2) Not allow flickering</td></tr>
<tr><td>9</td><td>Soldering</td><td>(1) Not allow heavy dirty and solder ball on PCB.
(The size of dirty refer to point and dust defect)
(2) Over 50% of lead should be soldered on Land.
 
</td></tr>
<tr><td>10</td><td>Wire</td><td>(1) Copper wire should not be rusted
(2) Not allow crack on copper wire connection.
(3) Not allow reversing the position of the flat cable.
(4) Not allow exposed copper wire inside the flat cable.</td></tr>
<tr><td>11*</td><td>PCB</td><td>(1) Not allow screw rust or damage.
(2) Not allow missing or wrong putting of component.</td></tr>
</table>

No	Item	Criterion
12	Protruded W: Terminal Width	 Acceptable criteria: Y ≤ 0.4
13	TAB	1. Position  W1≤1/3W H1≤1/3H 2 TAB bonding strength test  P (=F/TAB bonding width) ≥650gf/cm ,(speed rate: 1mm/min) 5pcs per SOA (shipment)
14	Total no. of acceptable Defect	A. Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.

13.3 Reliability of LCM

Reliability test condition:

Item	Condition	Time (hrs)	Assessment
High temp. Storage	80°C	48	No abnormalities in functions and appearance
High temp. Operating	70°C	48	
Low temp. Storage	-30°C	48	
Low temp. Operating	-20°C	48	
Humidity	40°C/ 90%RH	48	
Temp. Cycle	0°C ← 25°C →50°C (30 min ← 5 min → 30min)	10cycles	

Recovery time should be 24 hours minimum. Moreover, functions, performance and appearance shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (20±8°C), normal humidity (below 65% RH), and in the area not exposed to direct sun light.

13.4 Precaution for using LCD/LCM

LCD/LCM is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification. The followings should be noted.

General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isoproply alcohol, ethyl alcohol or trichlorotriflorothane, do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting LONGTECH
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.
4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

Soldering Precautions:

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature: 280°C±10°C
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

Operation Precautions:

1. The viewing angle can be adjusted by varying the LCD driving voltage Vo.
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage over 40 C is required, the relative humidity should be kept below 60%,and avoid direct sunlight.

Limited Warranty

LONGTECH LCDs and modules are not consumer products, but may be incorporated by LONGTECH's customers into consumer products or components thereof, LONGTECH does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of LONGTECH is limited to repair or replacement on the terms set forth below. LONGTECH will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between LONGTECH and the customer, LONGTECH will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with LONGTECH general LCD inspection standard. (Copies available on request)
2. No warranty can be granted if any of the precautions state in handling liquid crystal display above has been disregarded. Broken glass, scratches on polarizer mechanical damages as well as defects that are caused accelerated environment tests are excluded from warranty.
3. In returning the LCD/LCM, they must be properly packaged; there should be detailed description of the failures or defect.