HIGH-VOLTAGE MIXED-SIGNAL IC

UC1681s

68 x 98RGB C-STN LCD Controller-Driver
w/ 32-Shade Modulation Engine, 13-bit per RGB
(Dither to 60,543 Colors with 16-bit 5R-6G-5B input)

MP Specifications
Revision 1.3

August 29, 2006

ULTRACHIP

The Coolest LCD Driver, Ever!!

TABLE OF CONTENT

UC1681s

Single-Chip, Ultra-Low Power
68COM x 294SEG Matrix
Passive Color LCD Controller-Driver

INTRODUCTION

UC1681s is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images, with well balanced gray shades and vivid colors.

In addition to low power COM and SEG drivers, UC1681s contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 68x98 matrix C-STN LCD with comprehensive support for input format and color depth:
  12-bit RGB: 4K-color
  16-bit RGB: 60.5K-color (dither)
- Support video rate CSTN applications.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Two ID pins plus two programmable ID flags, totally 4 software-readable ID bits, to support configurable vender identification.
- Support both row ordered and column ordered display buffer RAM access.
- Support industry standard 3-wire, 4-wire serial bus (S9, S8, S8uc) and 8-bit/4-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Ultra-low power consumption under all display patterns.
- No power consumption or image quality penalty when used with video rate CSTN
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Software programmable four temperature compensation coefficients.
- Self-configuring 8x charge pump with on-chip pumping capacitors
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (10 pins with S9) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range: 1.8V ~ 3.3V
  V_{DD} (analog) range: 2.5V ~ 3.3V
  LCD V_{OP} range: 4.8V ~ 11.8V
- MTP V_{LCD} trimming circuit to support precise LCD contrast matching
- Available in gold bump dies:
  Bump pitch: 38 μM
  Bump gap: 15 μM
  Bump surface: > 2369 μM^2

ORDERING INFORMATION

GOLD BUMPED DIE

Part Number	MTP	Description
UC1681sGBB	Yes	Gold bumped die with MTP function

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT & ESD SENSITIVITY

The MTP memory cell is sensitive to photon excitation and ESD. Under extended exposure to strong ambient light, or when TST4 pin is exposed to ESD strikes, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light & ESD shields to realize full MTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

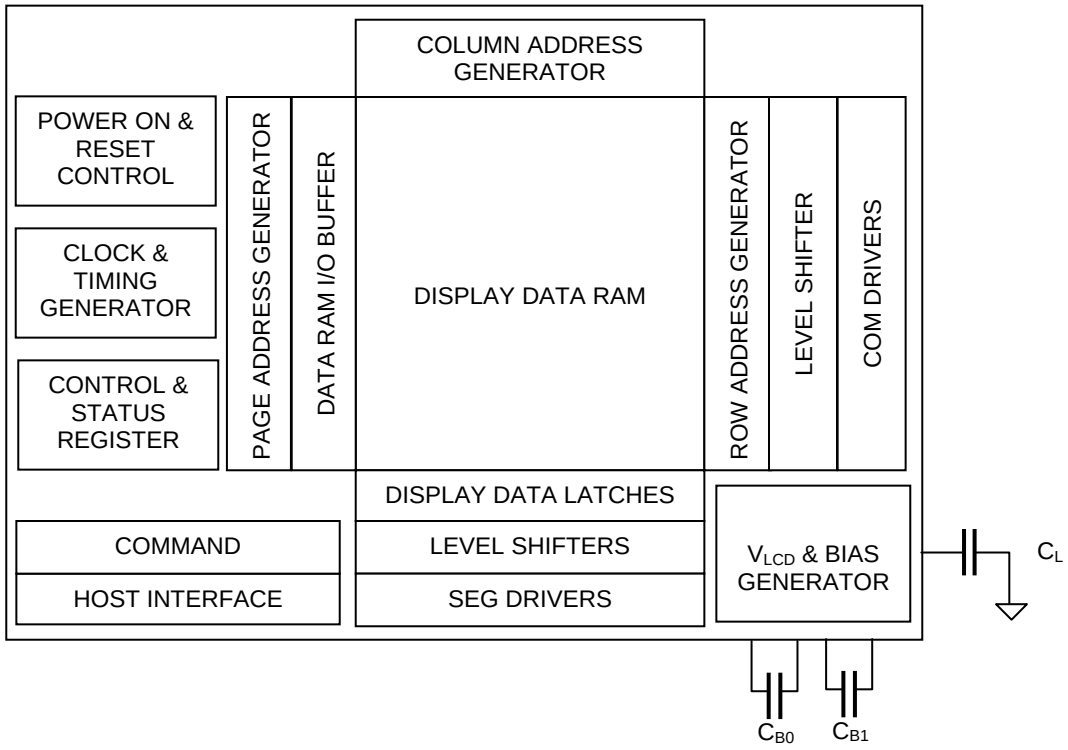
CONTENT DISCLAIMER

UltraChip believes the information contained in this document to be accurate and reliable. However, it is subject to change without notice. The information and data provided herein is for reference only. No responsibility is assumed by UltraChip for the use of information contained in this datasheet. Always contact UltraChip for commit to mass production for the latest product information and operation parameters.

CONTACT INFORMATION

UltraChip Inc. (Headquarter)
2F, No. 70, Chowtze Street,
Nei Hu District, Taipei 114,
Taiwan, R. O. C.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	# Pads	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	6 6 2	V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$. Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	9 9	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for these two nodes.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+} V_{B1-} V_{B0+} V_{B0-}	PWR	7 7 7 7	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR	2 2	High voltage LCD Power Supply. Connect these pins together. Capacitor C_L should be connected between V_{LCD} and V_{SS}. In COG applications, keep the ITO trace resistance between 50~80 Ω.

NOTE

- Recommended capacitor values:
  C_B: 300 x LCD load capacitance or 2.2μF (5V), whichever is higher.
  C_L: 15nF~50nF (16V) is appropriate for most applications.

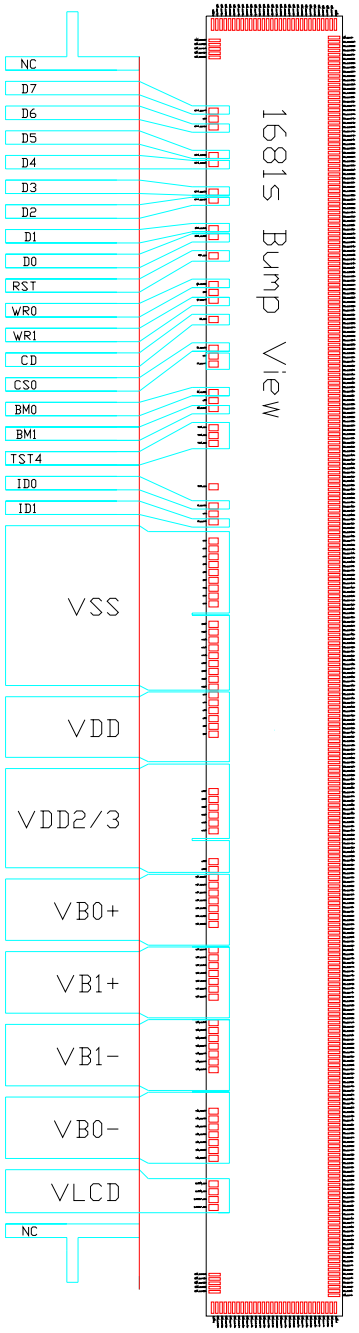
<table>
<tr><th>Name</th><th>Type</th><th># Pads</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>2</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>D[7:6]</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/8-bit</td></tr>
<tr><td>01</td><td>00</td><td>6800/4-bit</td></tr>
<tr><td>00</td><td>00</td><td>8080/4-bit</td></tr>
<tr><td>01</td><td>10</td><td>3-wire SPI w/ 9-bit token
(S9: conventional)</td></tr>
<tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr>
<tr><td>00</td><td>11</td><td>3/4-wire SPI w/ 8-bit token
(S8uc: Ultra-Compact)</td></tr>
</table></td></tr>
<tr><td>CS0
CS1</td><td>I</td><td>2</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1681s has built-in Power-ON Reset and Software Reset command, so RST pin is not be required for most systems. However, if the V_{DD} On-Off behavior is not “clean”, it is possible for UC1681s’s Power-ON reset to become confused.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation. In S9 mode, CD pin is not used. Connect CD to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID0
ID1</td><td>I</td><td>2</td><td>ID pin is for production control.
The connection will affect the content of PID[1:0] when using Get Status command. Connect to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>2</td><td>WR[1:0] controls the read/write operation of the host interface. See Section HOST INTERFACE for more detail.
In parallel mode, the meaning of WR[1:0] depends on whether the interface is in 6800 mode or 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA,
<table>
<tr><th></th><th>BM=1x
(Parallel)</th><th>BM=0x
(Parallel)</th><th>BM=01
(S9)</th><th>BM=00
(S8/S8uc)</th></tr>
<tr><td>D0</td><td>D0</td><td>D0/D4</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>D1/D5</td><td>–</td><td>–</td></tr>
<tr><td>D2</td><td>D2</td><td>D2/D6</td><td>–</td><td>–</td></tr>
<tr><td>D3</td><td>D3</td><td>D3/D7</td><td>SDA</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D5</td><td>D5</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D6</td><td>D6</td><td>–</td><td>0</td><td>S8/S8uc</td></tr>
<tr><td>D7</td><td>D7</td><td>0</td><td>1</td><td>1</td></tr>
</table>
Connect unused pins to V_{DD} or V_{SS}.</td></tr>
</table>

Name	Type	# Pads	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG294	HV	294	SEG (column) driver outputs. Support up to 98 x RGB pixels. Leave unused drivers open-circuit.
COM1 ~ COM68	HV	68	COM (row) driver outputs. Support up to 68 rows. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 68, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 68] open-circuit.
MISC. PINS			
V_{DDX}	O	5	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus on chip. They are provided to facilitate chip configurations in COG application. These pins should not be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
TST4	I/HV	3	TST4 controls test mode and is also used to supply one of the high voltage required for MTP Program operation. Leave TST4 open during normal LCD operation. In COG applications keep TST4 trace resistance between 50 ~ 100 Ω.
TST2	I/O	1	Test I/O pins. Leave these pins open during normal LCD operation.

Note:

- Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value ranges for those index registers will be 0~67 for COM and 0~293 for SEG.

REFERENCE COG LAYOUT



Notes for V_{DD} with COG:

The V_{DD}=1.8V, typical operation condition of UC1681s, must be met under all operation conditions. To give UC1681s capability of supporting video, the peak of I_{DD} during high speed SRAM write can be 25~28mA, (depends on the bus speed and V_{DD}). Special care of V_{DD} and $V_{DD2/3}$ ITO trances are recommended for COG applications where V_{DD} and $V_{DD2/3}$ are separated. High resistance on V_{DD} trace can cause actual on-chip V_{DD} to drop below 1.65V during high speed data write condition and cause the IC to malfunction. Therefore, V_{DD} and $V_{DD2/3}$ ITO traces need to be very carefully designed for COG modules where V_{DD} and $V_{DD2/3}$ use separate power supplies.

CONTROL REGISTERS

UC1681s contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and default values. The commands supported by UC1681s will be described in the next two sections, starting with a summary table, followed by detailed descriptions.

Name: The Symbolic reference of the register.
Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (67– 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively divided into three segments: one scrollable segment double-covered by two non-scrollable ones. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three segments: 2xFLT non-scrollable rows on one side, 2XFLB non-scrollable rows on the other side, and scrollable DST~DEN in the middle.
CR	7	0H	Return Column Address. Useful for cursor implementation.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	7	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 5 01b: 7 10b: 8 **11b: 9**
TC	2	0H	Temperature Compensation (per ^{o}C) **00b: -0.05%** 01b: -0.10% 10b: -0.15% 11b: -0.20%
PM	8	67H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	7	00H	PM offset. PMO[6]=1: The effective PM value, PMV = PM - PMO[5:0] PMO[6]=0: The effective PM value, PMV = PM + PMO[5:0]
PC	4	EH	Power Control. PC[1:0]: Panel Loading 00b: LCD: ⩽ 5nF 01b: LCD: 5~7nF **10b: LCD: 7~9.5nF** 11b: LCD: 9.5~12nF PC[3:2]: Pump Control 00b: External V_{LCD} **11b: Internal V_{LCD}** (Standard)

Name	Bits	Default	Description
AC	5	01H	Address Control: AC[0]: WA: Automatic column/row Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0: Column (CA) first** 1: Row (RA) first AC[2]: RID: RA (row address) auto increment direction (**0:+1** 1:-1) AC[3]: CUM: Cursor update mode, (Default **0: OFF**) when CUM=1, CA increment on write only, wrap around suspended AC[4] : Window Program Enable **0: Disable** 1: Enable
DC	5	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display On-Off (Default **0: OFF**) DC[4:3]: Gray-shade Modulation mode & Dither Function. 00b : On-Off mode without dither function 01b : 32-shade mode without dither function 10b : 8-shade mode without dither function **11b : 32-shade mode with dither function**
LC	10	090H	LCD Control: LC[0]: Enable the first FLx2 lines in partial display mode (Default **OFF**). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 13.5 Klps 01b: 15.5 Klps **10b: 17.7 Klps** 11b: 20.2 Klps Line Rate (for On/Off mode): 00b: 5.7 Klps 01b: 6.5 Klps **10b: 7.4 Klps** 11b: 8.5 Klps (Frame-Rate = Line-Rate / Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) **0 : BGR-BGR** 1 : RGB-RGB LC[7:6] : Color and input mode Dither enabled 01b : 4K color mode. 4R-4G-4B (12-bit/RGB) **10b : 60.5K color mode**. 5R-6G-5B (16-bit/RGB) Dither disabled 01b : 4K color mode. 4R-5G-3B (12-bit/RGB) 10b : 8K color mode. 4R-5G-4B (16-bit/RGB) For data over 4R-5G-4B, the redundant LSB of each color will be truncated. (Example below: R0, G0, and B0 will be truncated.) R4 R3 R2 R1 R0 - G5 G4 G3 G2 G1 G0 - B4 B3 B2 B1 B0. LC[9:8] : Partial Display Control **0xb: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 10b: Enabled Mux-Rate = CEN+1 11b: Enabled Mux-Rate = DEN-DST+1+LC[0]x(FLT+FLB)x2
CEN DST DEN	7 7 7	43H 00H 43H	COM scanning end (last COM with full line cycle, 0 based index) Partial display start (first COM with active scan pulse, 0 based index) Partial display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9

Name	Bits	Default	Description
MSK	3	0H	R/G/B Write Data mask bits MSK[2:0] = {MR, MG, MB} (Default: **000b**) 0: Write 1: Block
WPC0	7	00H	Window program starting column address. Value range: 0 ~ 97.
WPP0	7	00H	Window program starting row address. Value range: 0 ~ 67.
WPC1	7	61H	Window program ending column address. Value range: 0 ~ 97.
WPP1	7	43H	Window program ending row address. Value range: 0 ~ 67.
MTPC	6	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : Idle 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip debugging use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Use/ignore MTP value. 0: Ignore **1: Use** MTPC[5] : For testing only. Set to 0 for normal operation.
MTP	7	–	Multiple-time Programming. For V_{LCD} fine tune.
MTPID	2	–	Multiple-time Programming. For LCM manufacturers' configuration.
MTPM	7	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
MTPM1	2	0H	MTP Write Mask. Bit =1: program, Bit=0: no action
APC0 APC1	8 8	– –	Advanced Program Control. For UltraChip only. Please do *NOT* use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag 0: without MTP 1: with MTP
MS	1	–	MTP programming in-progress
WS	1	–	MTP Command Succeeded
ID	2	PIN	Access the connected status of ID pin.

COMMAND TABLE

The following is a list of host commands supported by UC1681s

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
#: Useful Data bits –: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	DR	MX	MY	WA	DE	WS	MD	MS	Get Status	N/A
				Rev.	PMO [6:0]								
				Product Code				PID[1:0]		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	-	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0, 1, or 2	N/A
		0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0
10	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	-	#	#	#	Set RA[6:4]	0
11	Set V_{BIAS} Potentiometer (double-byte command)	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set PM[7:0]	67H
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	0: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0 0	0 0	1 #	0 #	0 #	1 #	0 #	0 #	0 #	0 #	Set {FLT, FLB}	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
18	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
19	Set Color Mask	0	0	1	0	1	1	0	#	#	#	Set MSK[2:0]	0
20	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
21	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
22	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do NOT use.	N/A
		0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 9
27	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
28	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
29	Set COM End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	0 #	1 #	Set CEN[6:0]	67
30	Set Partial Display Start	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	0 #	Set DST[6:0]	0
31	Set Partial Display End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	1 #	Set DEN[6:0]	67
32	Set Window Program Starting Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Set WPC0[6:0]	0
33	Set Window Programming Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #	Set WPP0[6:0]	0
34	Set Window Programming Ending Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	0 #	Set WPC1[6:0]	97
35	Set Window Programming Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #	Set WPP1[6:0]	67
36	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]	0: Disable

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
37	Set MTP Operation control	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	0 #	Set MTPC[5:0]	0
38	Set MTP Write Mask	0 0 0	0 0 0	1 - -	0 # -	1 # -	1 # -	1 # -	0 # -	0 # #	1 # #	Set MTPM[7:0]	0
39	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Programming commands	N/A
40	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		
41	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		
42	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		

Notes:

- All bit patterns other than commands listed above may result in undefined behavior.
- The interpretation of commands (38)~(42) depends on register MTPC[3].
- Commands (39)~(42) are shared with commands (32)~(35), and have exactly the same code.
  When MTPC[3]=0, commands (39)~(42) are interpreted as *Window Programming* commands.
  When MTPC[3]=1, they are *MTP Control* commands.
- MTPM and PM are actually the same register. Only one of the commands (38 or 11) is valid at any time, and it is determined by MTPC[3].
- After MTP-ERASE or MTP-PROGRAM operation, please always perform the following steps,
  a) Disconnect TST4 power source.
  b) Do a full V_{DD} ON-OFF cycle (make sure V_{DD} drops below 50mV).
  before resuming normal operation.

COMMAND DESCRIPTION

(1) Write Data To Display Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

UC1681s will convert input RAM data to 13-bits of RGB data. Please refer to command `Set Color Mode` for detail of data-write sequence.

(2) Read Data From Display Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Each RGB triplet is stored as 13-bit in the display RAM. Each 13-bits RGB data takes 2 RAM read cycles. The data read will start with the high byte D[12:5] and then low byte {D[4:0], 4'b000}. The read out RGB data is *after-dither* for 60.5K color

R3	R2	R1	R0	G4	G3	G2	G1	G0	B3	B2	B1	B0	0	0	0
1st Read								2nd Read							

Write/Read Data Byte (command 1/2) operation uses internal Row Address register (RA) and Column Address register (CA). RA and CA can be programmed by issuing the `Set Row Address` and the `Set Column Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the CA boundary, and system programmers need to set the values of RA and CA manually. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (RID, AC[2]).

When RA reaches the boundary of RAM (i.e. RA = 0 or 67), RA will be wrapped around to the other end of RAM and continue.

(3) Get Status & PM

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	DR	MX	MY	WA	DE	WS	MD	MS
	0	1	Rev	PMO[6:0]						
	0	1	Product Code				PID[1:0]		MID[1:0]	

Status 1 definitions:

DR: 1: Dither Enabled 0: Dither Disabled
MX: Status of register LC[1], mirror X.
MY: Status of register LC[2], mirror Y.
WA: Status of register AC[0]. Automatic column/row wrap around.
DE: Display enable flag. DE=1 when display is enabled
WS: MTP Command Succeeded
MD: MTP Option (Yes/No)
MS: MTP action status

Status 2 definitions:

Rev : Version Code. 0 or 1 *PMO[6:0] :* PM offset value

Status 3 definitions:

Product Code : 0001b(1h)
PID[1:0] : Provide access to ID pins connection status
MID[1:0] : LCM manufacturers' configuration

If multiple *Get Status* commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[6:4]	0	0	**0**	**0**	**0**	**1**	-	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: **0~97**

(5) Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	**TC1**	**TC0**

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
00b = -0.05%/°C 01b = -0.10%/°C 10b = -0.15%/°C 11b = -0.20%/°C

(6) Set Panel Loading

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: 00b : ⩽ 5nF 01b = 5~7nF **10b = 7~9.5nF** 11b = 9.5~12nF

(7) Set Pump Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:
00b = External V_{LCD} **11b = Internal V_{LCD}**

(8) Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control APC[0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**R**	R
(Double-byte command)	0	0	APC register parameter							

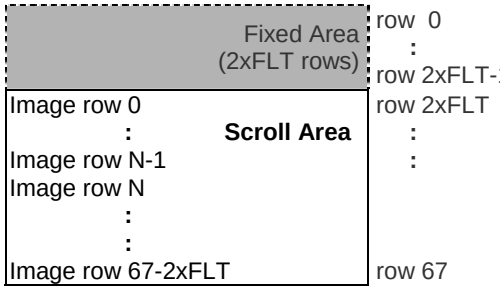
For UltraChip only. Please do NOT use.

(9) Set Scroll Line

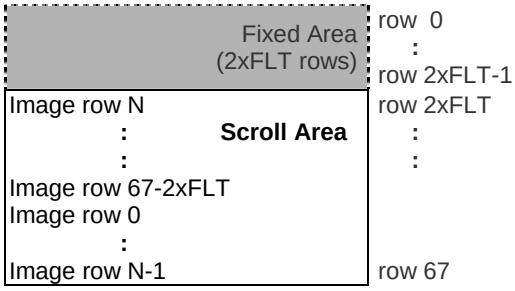
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	-	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 67-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by the `Set Fixed Lines` command.



SL=0



SL=N

(10) Set Row Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address MSB RA [6:4]	0	0	**0**	**1**	**1**	**1**	-	RA6	RA5	RA4

Set SRAM row address for read/write access.

Possible value = **0~67**

(11) Set V_{BIAS} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0]	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section *LCD VOLTAGE SETTING* for more detail.

Effective range: **0 ~ 255**

(12) Set Partial Display Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [9:8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC9	LC8

This command is used to enable partial display function.

LC[9:8] : **0X**b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)
10b: Enable Partial Display, Mux-Rate = CEN+1
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+ LC[0] x (FLT+FLB)x2

(13) Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order
0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).
1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

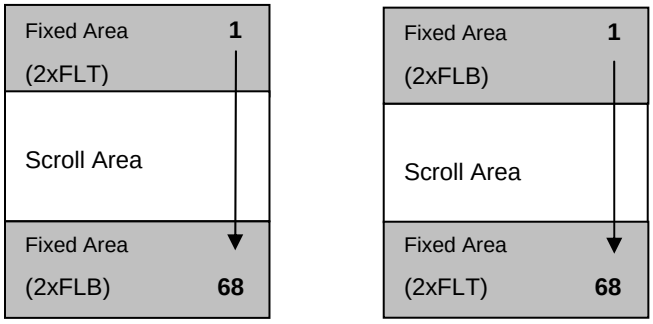
AC[2]: RID, row address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. When Window Program is enabled (AC[4]=ON), see Section COMMAND DESCRIPTION (32) ~ (36) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[4] is.

(14) Set Fixed Lines

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB}	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into Scroll and Fixed areas. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0 MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure

MY=0 DST ⩾ FLTx2
DEN ⩽ (CEN-FLBx2).

MY=1 DST ⩾ FLBx2
DEN ⩽ (CEN-FLTx2)

(15) Set Line Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 1/2 and 1/3 at Mux-Rate = 28 and 16.

The following are line rates at Mux Rate = 29 ~ 68.

00b: 13.5 Klps 01b: 15.5 Klps **10b: 17.7 Klps** 11b: 20.2 Klps
(Klps: Kilo-Line-per-second)

While the followings are Line Rates in On/Off mode:
00b: 5.7 Klps 01b: 6.5 Klps **10b: 7.4 Klps** 11b: 8.5 Klps

(16) Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(17) Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

(18) Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

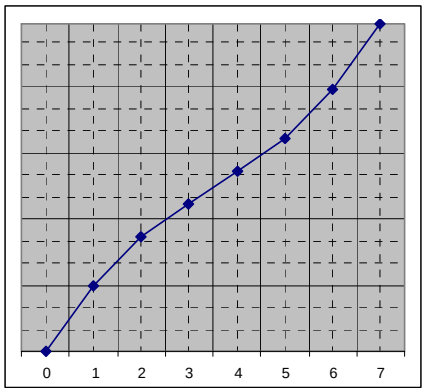
This command is for programming register DC[4:2].

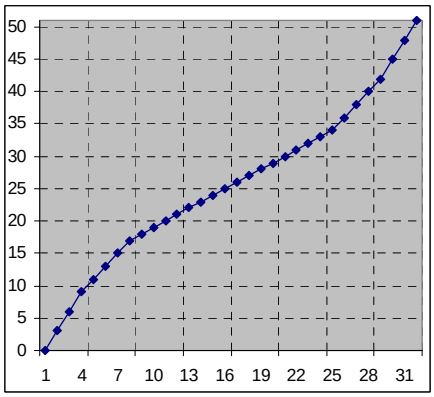
When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1681s will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[4:3]: Gray-shade Modulation mode & Dither Function.

00b : On-Off mode without dither function 01b : 32-shade mode without dither function
10b : 8-shade mode without dither function **11b : 32-shade mode with dither function**

For 8-shade mode and 32-shade mode, modulation curves are shown below:





In On-Off mode, the SEG output is either ON or OFF, decided by MSB (i.e. R/G/B bit) of input data.

(19) Set Color Mask

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mask MSK [2:0]	0	0	**1**	**0**	**1**	**1**	**0**	MSK[2:0]		

This command is used for program MSK[2:0] which will control whether the input RGB data will be blocked from updating RGB data in the RAM. (1: Block, 0: Normal. MSK[2:0] = {MSK_R, MSK_G, MSK_B})

Example: Let color mode = 256 color, MSK[2:0] = 100b (MSK_R = 1, MSK_G = 0, MSK_B = 0). There is one pixel to be updated, and the original data for the pixel are 11100110b (RRR-GGG-BB). Suppose the new input RGB data are 00000000b, since R is masked, the data for the pixel would be updated as 11100000b.

(20) Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for program LC[2:0] for COM (row) mirror (MY) and SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 97-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC[0] controls whether the two soft icon sections (2xFLT on the top and 2xFLB on the bottom) are displayed during partial display mode.

(21) Set Color Pattern

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	LC5

UC1681s supports on-chip swapping of R⇔B data mapping to the SEG drivers.

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	SEG292	SEG293	SEG294
0	B	G	R	B	G	R	…	B	G	R
1	R	G	B	R	G	B	…	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in `Set Color Mode` below.

(22) Set Input Color Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Dither Enabled (DC[4:3]=11):

LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K color)

1-bit extension for G. 12 bits of input data is stored to 13 RAM bits.
3 bytes of input data will be merged into 2 sets of RGB data. No dither is performed.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R3	R2	R1	R0	G3	G2	G1	G0
2nd Byte Write Data	B3	B2	B1	B0	R3	R2	R1	R0
3rd Byte Write Data	G3	G2	G1	G0	B3	B2	B1	B0

LC[7:6] = **10b** (RRRRR-GGGGGG-BBBBB, 60.5K color)

1-bit dither for R/G/B each. 16 bits input data dithered to 13 RAM bits.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R4	R3	R2	R1	R0	G5	G4	G3
2nd Byte Write Data	G2	G1	G0	B4	B3	B2	B1	B0

Data Read Sequence

for LC[7:6] = 01b

Data Read Sequence	***D[7:0]***							
1st Byte Read Data	R3	R2	R1	R0	G3	G2	G1	G0
2nd Byte Read Data	G_{M3}	B3	B2	B1	B0	0	0	0

R/G/B: the input Red/Green/Blue data.

R/G_{MN}: the Red/Green bits mapped from RGB input data.

for LC[7:6] = 10b

Data Read Sequence	***D[7:0]***							
1st Byte Read Data	R_{D3}	R_{D2}	R_{D1}	R_{D0}	G_{D4}	G_{D3}	G_{D2}	G_{D1}
2nd Byte Read Data	G_{D0}	B_{D3}	B_{D2}	B_{D1}	B_{D0}	0	0	0

$R/G/B_{DN}$: the N-th bit of after-dither Red/Green/Blue input data.

Dither Disabled (DC[4:3]=10, 01, 00):

LC[7:6] = 01b (RRRR-GGGGG-BBB, 4K-color)

12 bits of input data is stored to 13 RAM bits. 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R3	R2	R1	R0	G4	G3	G2	G1
2nd Byte Write Data	G0	B2	B1	B0	R3	R2	R1	R0
3rd Byte Write Data	G4	G3	G2	G1	G0	B2	B1	B0

LC[7:6] = **10b** (RRRRX-GGGGGX-BBBBX, 8K-color)

1-bit truncation each for R/G/B. 16 bits input data truncated to 13 RAM bits.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R4	R3	R2	R1	--	G5	G4	G3
2nd Byte Write Data	G2	G1	--	B4	B3	B2	B1	--

Data Read Sequence

For LC[7:6] = 0, read data sequence is same as Dither Enabled mode.

LC[7:6] = 01b

Data Read Sequence	***D[7:0]***							
1st Byte Read Data	R3	R2	R1	R0	G4	G3	G2	G1
2nd Byte Read Data	G0	B2	B1	B0	B_{M2}	0	0	0

R/G/B: the input Red/Green/Blue data.

R/G_{MN}: the Red/Green bits mapped from RGB input data.

LC[7:6] = 10b

Data Read Sequence	***D[7:0]***							
1st Byte Read Data	R_{T3}	R_{T2}	R_{T1}	R_{T0}	G_{T4}	G_{T3}	G_{T2}	G_{T1}
2nd Byte Read Data	G_{T0}	B_{T3}	B_{T2}	B_{T1}	B_{T0}	0	0	0

$R/G/B_{TN}$: the N-th bit of after-truncated Red/Green/Blue input data.

(23) System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(25) Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do NOT use.

(26) Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b = 5 01b = 7 10b = 8 **11b = 9**

(27) Reset Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=0, CA=CR	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This command is used to reset cursor update mode function.

(28) Set Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1, CR=CA	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**

This command is used for setting cursor update mode function. When cursor update mode is set, UC1681s will update register CR with the value of register CA. The column address CA will increment with write RAM data operation but the address wraps around will be suspended no matter what WA setting is. However, the column address will not increment in read RAM data operation.

The set cursor update mode can be used to implement “write after read RAM” function. The column address (CA) will be restored to the value, which is before the set cursor update mode command, when resetting cursor update mode.

The purpose of this pair of commands and their features is to support “write after read” function for cursor implementation.

(29) Set COM End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	-	*CEN* register parameter						

This command programs the ending COM electrode. CEN defines the number of COM electrodes used, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 68 pixel rows, the LCM designer should set CEN to *N-1* (where *N* is the number of pixel rows) and use COM1 through COM-*N* as COM driver electrodes.

(30) Set Partial Display Start

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(Double-byte command)	0	0	-	*DST* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

(31) Set Partial Display End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double-byte command)	0	0	-	*DEN* register parameter						

This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

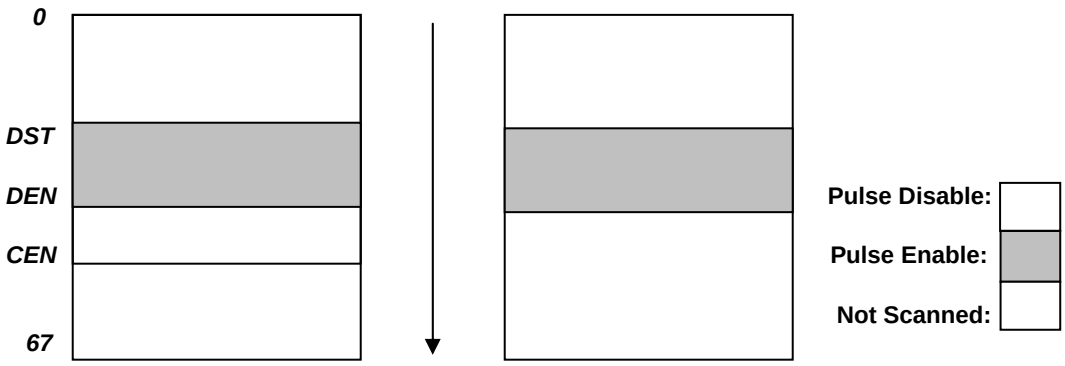
When LC[9]=1, two partial display modes are possible with UC1681s:
LC[8]=1: On-Off only, ultra-low-power mode (if Mux-Rate ⩽ 30, set BR=5).
LC[8]=0: Full gray shade low power mode (BR and PM stays the same)

When LC[9:8]=10b, the Mux-Rate is still CEN+1. This is achieved by suppressing only the scanning pulses, but not the scanning time slots for COM electrodes that are outside of DST~DEN. Under this mode, the gray-scale quality of the display is preserved, while the power is reduced significantly.

When LC[9:8]=11b, the Mux-Rate is narrowed down to DST-DEN + LC[0]x(FLT+FLB)x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also requires BR and V_{LCD} to be readjusted. When Mux-Rate is under 30, it is recommend to set BR=5.

For minimum power consumption, set LC[9:8]=11b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use On-Off mode, set PC[1:0]=00b, and use lowest BR and lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(32) Set Window Program Starting Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	-	*WPC0[6:0]* register parameter						

This command is to program the starting column address of RAM program window.

(33) Set Window Program Starting Row Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	-	*WPP0[6:0]* register parameter						

This command is to program the starting row address of RAM program window.

(34) Set Window Program Ending Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	-	*WPC1[6:0]* register parameter						

This command is to program the ending column address of RAM program window.

(35) Set Window Program Ending Row Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	-	*WPP1[6:0]* register parameter						

This command is to program the ending row address of RAM program window.

(36) Set Window Program Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[4]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC4

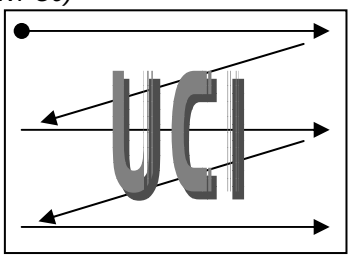
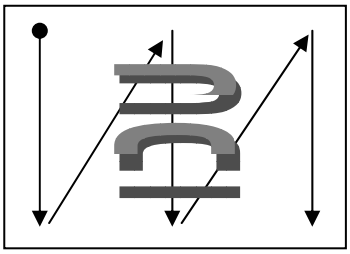
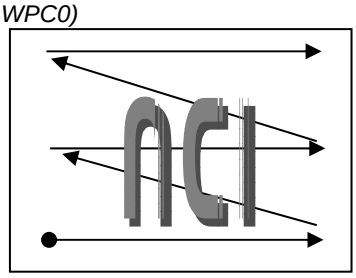
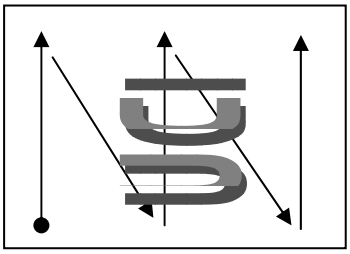
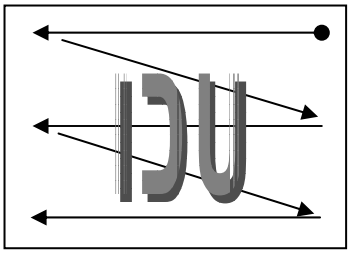
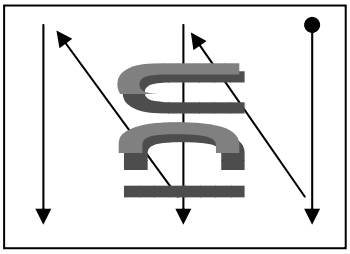
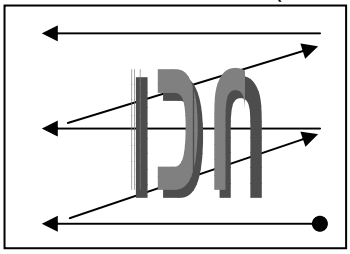
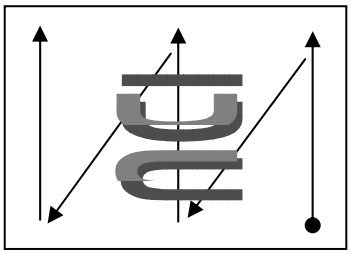
This command is to enable the Window Program Function. Window Program Enable should always be set right before starting the new boundary program and be reset when changing the window program boundary.

Window Program Function can be used to refresh the RAM data in a specified window of SRAM address. When window programming is enabled, the CA and RA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next row/column after reaching the specified window column / row boundary. RID controls the RAM address incrementing from WPP0 toward WPP1 (RID=0) or reverse the direction (RID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM column address incrementing from 97-WPC0 to 97-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

By different combination of RID, AC[1], MX, and by setting CA, RA at proper corners of the “window”, effects such as mirrors and rotations can be easily achieved.

Setting or resetting AC[4] does not affect the value of CA and RA. After Window Program is enabled, remember to reposition CA, RA to a pixel inside the “window”. If CA, RA points to a pixel outside the “window”, the subsequent data write can produce undefined results.

Auto-increment order = 0 MX=0 RID = 0	Auto-increment order = 1 MX=0 RID = 0
(WPP0,WPC0)  *(WPP1,WPC1)*	*(WPP0,WPC0)*  *(WPP1,WPC1)*
Auto-increment order = 0 MX=0 RID = 1	**Auto-increment order = 1 MX=0 RID = 1**
(WPP0,WPC0)  *(WPP1,WPC1)*	*(WPP0,WPC0)*  *(WPP1,WPC1)*
Auto-increment order = 0 MX=1 RID = 0	**Auto-increment order = 1 MX=1 RID = 0**
(WPP0,97-WPC0)  *(WPP1,97-WPC1)*	*(WPP0,97-WPC0)*  *(WPP1,97-WPC1)*
Auto-increment order = 0 MX=1 RID = 1	**Auto-increment order = 1 MX=1 RID = 1**
(WPP0,97-WPC0)  *(WPP1,97-WPC1)*	*(WPP0,97-WPC0)*  *(WPP1,97-WPC1)*

(37) Set MTP Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC (Double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	-	-	*MTPC* register parameter					

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Idle
001 : MTP Read
010 : MTP Erase
011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)
MTPC[5] : For testing only. Set to 0 for normal operation

The following commands (38)~(42) are only valid when MTPC[3]=1.

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

(38) Set MTP Write Mask

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM (Triple-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	**-**	*MTPM[6:0]* register parameter						
	0	0	**-**	**-**	-	-	-	-	MTPM1 [1:0]	

This command is enable write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to “1”. MTPM[x]=0 means no write action for x-th bit. And the content of this bit will not change.

The amount of “programming current” increases with the number of 1’s in MTPM. If the “programming current” appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1’s evenly into these cycles.

MTPM[6:0]: Set PMO value
MTPM1[1:0]: Set MID value

This command is only valid when MTPC[3]=1.

(39) Set VMTP1 Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	Shared register parameter							

This command is for fine tuning V_{OPT1} setting (use with BR=00) and is valid only when MTPC[3]=1.

(40) Set VMTP2 Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} PM setting (use with BR=11) and is valid only when MTPC[3]=1.

(41) Set MTP Write Timer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	Shared register parameter							

This command is valid only when MTPC[3]=1.

(42) Set MTP Read Timer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP5 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	Shared register parameter							

This command is valid only when MTPC[3]=1.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1681s via registers CEN, DST, DEN, FLT, FLB, and partial display control flags LC[9:8] and LC[0].

Combined with low power partial display mode and a low bias ratio of 5, UC1681s can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=68), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally can not maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1681s supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	7	8	9

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	**0**	**1**	**2**	**3**
% per ^{o}C	-0.05	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2]. For good product reliability, it is recommended to keep V_{LCD} under 11.8V over the entire operating range.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

Color STN LCD is sensitive to even a 0.5% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

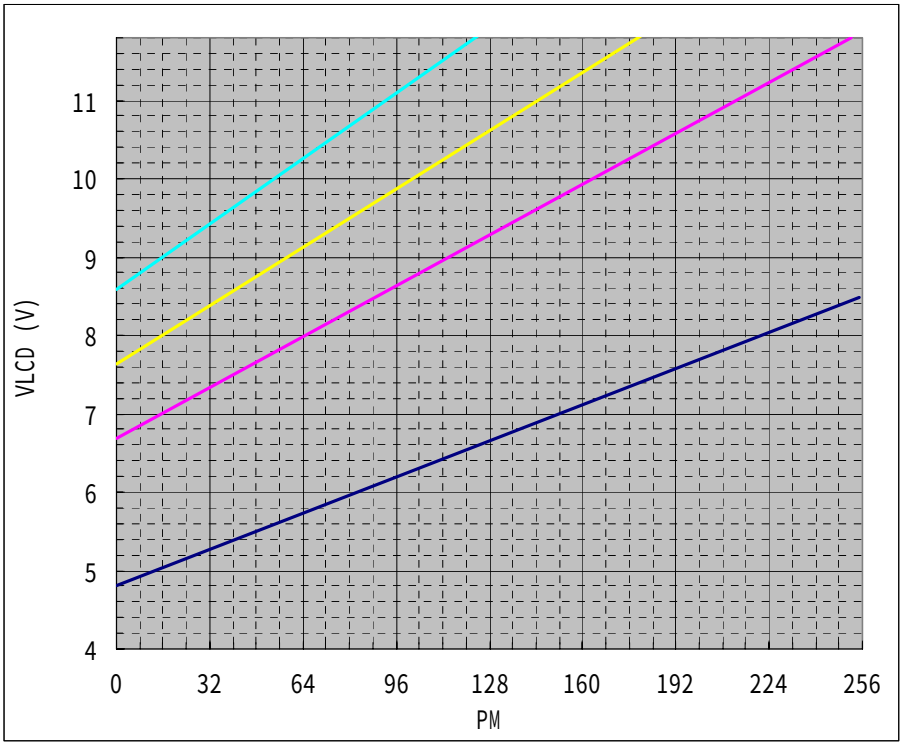
For the best results, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1681s is designed to handle LCD panels with loading up to ~12nF using 10-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.65V$. For larger LCD panels use lower resistance ITO glass packaging.

Due to crosstalk consideration, ~12nF is also the recommended maximum LCD panel size for COG applications, unless 7-Ω/Sq or lower resistance ITO glass is used.

V_{LCD} QUICK REFERENCE



V_{LCD}-PM relationship for different BR setting at 25°C.

BR	C_{V0} (V)	C_{PM} (mV)	PM_reg	V_{LCD} (V)
5	4.806	14.47	0	4.81
			255	8.50
7	6.695	20.26	0	6.70
			252	11.80
8	7.642	23.16	0	7.64
			180	11.81
9	8.584	26.05	0	8.58
			124	11.81

Note:

1. For good product reliability, keep $V_{LCD\ (max)}$ under **11.8V** under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

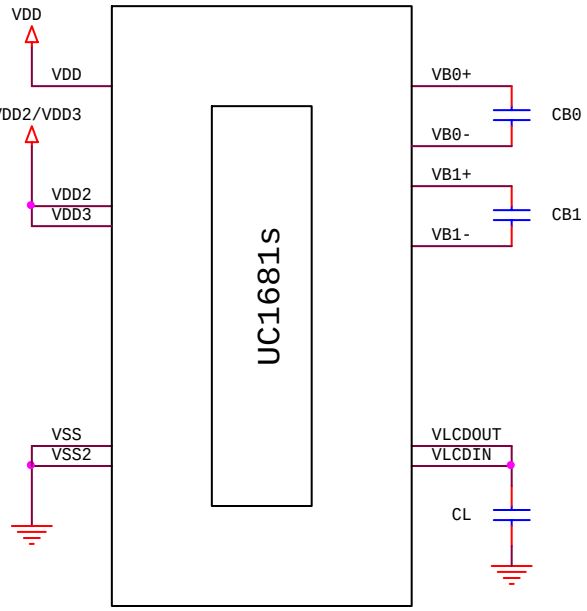


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note:
Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

C_B: 300x LCD load capacitance or 2.2μF (5V), whichever is higher.
C_L: 15nF~50nF (16V) is appropriate for most applications.
R_L: 3.3~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1681s contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 28, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 58, line rate will be scaled down by 2 times automatically reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Frame rate 220Hz or higher is recommended for 32-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When switching from 32-shade modulation to 8-shade modulation, line rate will be scaled down automatically by ~30%.

Under most situations, flicker behavior is similar between these two different modulation schemes. However, it is recommended to test each mode to make sure the result is as expected.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in Idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x=1~68, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1681s will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1681s will first exit from Sleep mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FLT and FLB specify two regions of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. FLT and FLB registers can be used to implement fixed regions when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1681s provides flexible control of Mux Rate and active display area. Please refer to command *Set COM End, Set Partial Display Start*, and *Set Partial Display End* for more detail.

GRAY-SHADE MODULATION MODE

UC1681s has three gray-shade modulation modes: 32-shade, 8-shade, and On-Off modes.

The 8-shade mode will consume roughly 25~30% less power than the 32-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth among On-Off mode, 8-shade mode and 32-shade mode.

INPUT COLOR FORMATS

UC1681s supports the following four different input color formats.

4KC (12-bit/RGB): In this color mode, G will be extended while B will be dithered, and the input data will be converted into 4R-5G-4B format before they are stored to display RAM.

60.5KC (16-bit/RGB): On-chip dither engine will convert the input data into internal 13-bit-per-RGB pixel format and store it to on-chip display RAM. This is the default mode.

Changing color mode does not affect the content already stored in the display buffer RAM. Users can use several color modes together in real time.

For example, the menu portion can be painted in 4K-color mode for fast update speed, and then switch to 60.5K-color mode, together with window programming option, and take advantage of built-in dither engine to produce smooth graphics images.

ITO LAYOUT AND LC SELECTION

Since the COM scanning pulse of UC1681s can be as short as 32μS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM ITO TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk. Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below:

$$(R_{ROW} / 2.7 + R_{COM} + R_{OUT}) \times C_{ROW} < 2.3\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please also make sure

$$| RC_{MAX} – RC_{MIN} | < 0.5\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worse case parameters for the above calculations.)

SEG ITO TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} /2.7 + R_{SEG}) \times C_{COL} < 0.4\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / #_of_column, C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worse case parameters for the above calculations.)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too large, contrast will drop, color saturation will deteriorate, and images will look murky and dull. When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast becomes too strong, visibility of shades will suffer, and crosstalk will increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where

V_{90}, V_{10} is the LC characteristics, and V_{ON}, V_{OFF} is the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/68	1/9	12.61%	10.09%	9.91%
1/68	1/8	12.40%	9.08%	8.92%

FAST CSTN & COG

UC1681s can support very fast CSTN for video rate applications. For LCM with t_r+t_f = 80mS or smaller, it is recommended to set the line rate higher such that the frame rate is 220Hz of higher. For such applications, special attentions are necessary for COG design to minimize crosstalk and ensure sufficient power is available to UC1681s to drive the LCM at such high speed.

- At this fast scan rate, the SEG/COM trace RC decay minimization will be very critical in minimizing crosstalk.
- MPU will perform frequent high speed update to the on-chip video RAM for video applications. Make sure the ITO does not cause on-chip V_{DD} -V_{SS} to fall below 1.65V, and V_{SS} bounce is under 6% x V_{DD}.

For video CSTN applications, it is recommended to use low resistance ITO glass to help reduce SEG signal RC decay, minimize V_{DD}, V_{SS} noise, and ensure sufficient V_{DD2}, V_{SS2} supply for the on-chip DC-DC converter.

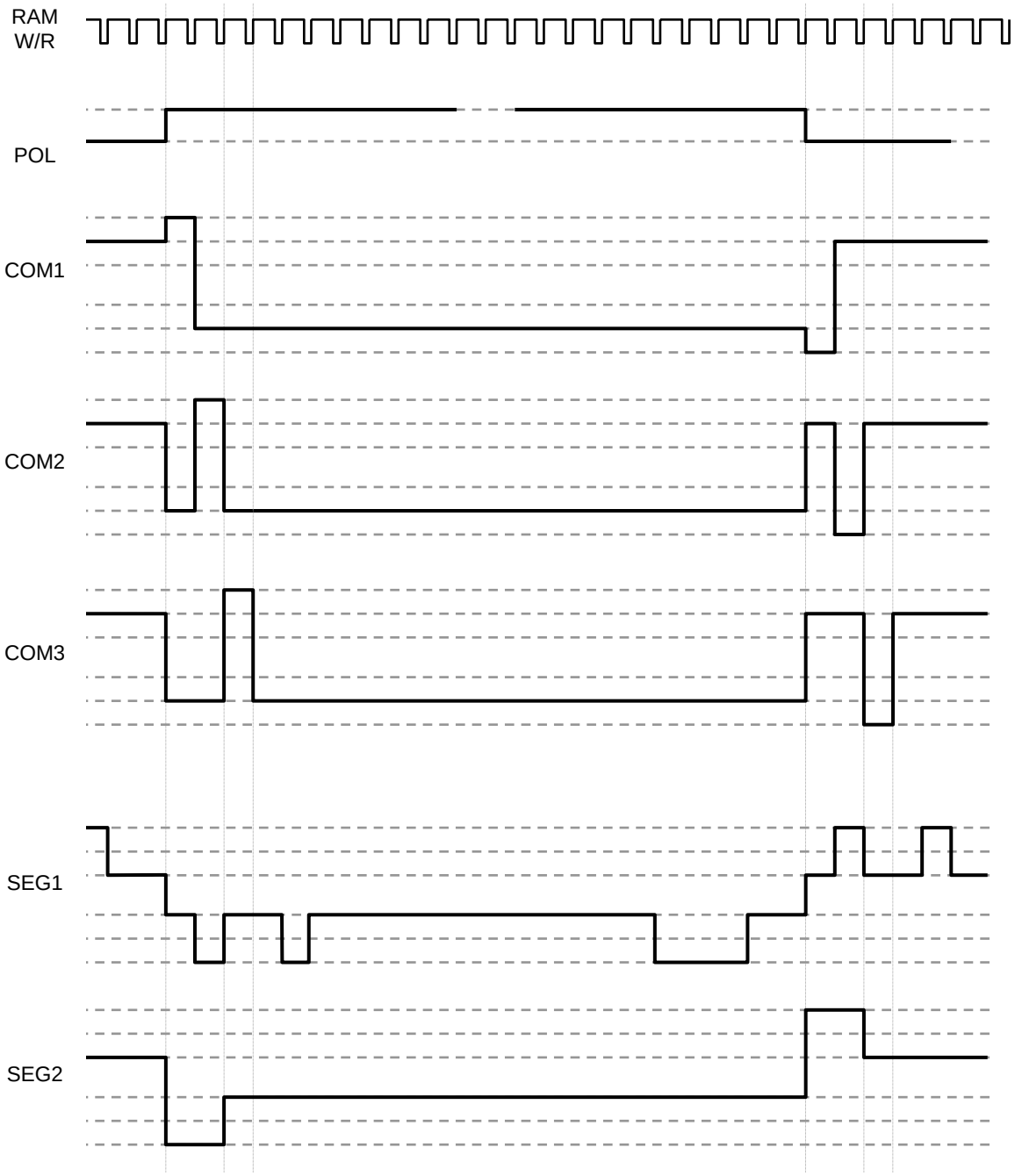


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1681s supports two parallel bus protocols, in either 8-bit or 4-bit bus width, and three serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

Bus Type		8080		6800		S8 (4wr)	S8uc (3wr)	S9 (3wr)
Width		8-bit	4-bit	8-bit	4-bit	Serial		
Access		Read/Write				Write Only		
Control & Data Pins	BM[1:0]	10	00	11	01	00	00	01
	D[7:6]	Data	0X	Data	0X	10	11	10
	CS[1:0]	Chip Select						
	CD	Control/Data						0
	WR0	$\overline{WR}$		R/$\overline{W}$		0		
	WR1	$\overline{RD}$		EN		0		
	D[5:4]	Data	–	Data	–	–		
	D[3:0]	Data	Data	Data	Data	D0=SCK, D3=SDA		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}.

	CS Disable Interface	CS Init bus state	CD 1⇔0 Init bus state	CD 1⇨0 init color mapping	RESET Init bus state	RESET init color mapping
8-bit	✓	–	–	✓	✓	✓
4-bit	✓	–	✓	✓	✓	✓
S8 or S9	✓	✓	–	✓	✓	✓
S8uc	✓	–	✓	✓	✓	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CD refers to CD transitions within valid CS window. CD = 0 means write command or read status.
- CS / CD Sync / RESET can be used to initialize bus state machine (like 4 bits / S8 / S9).
- RESET can be pin reset / soft reset / power on reset.
- CD can be used to initialize the multi-byte input RGB format to/from on-chip SRAM mapping.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1681s internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 4-bit mode, by either *Set CA,* or *Set RA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT & 4-BIT BUS OPERATION

UC1681s supports both 8-bit and 4-bit bus width. The bus width is determined by pin BM[1].

4-bit bus operation exactly doubles the clock cycles of 8-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 4-bit mode is reset each time CD pin changes state (when CS is active).

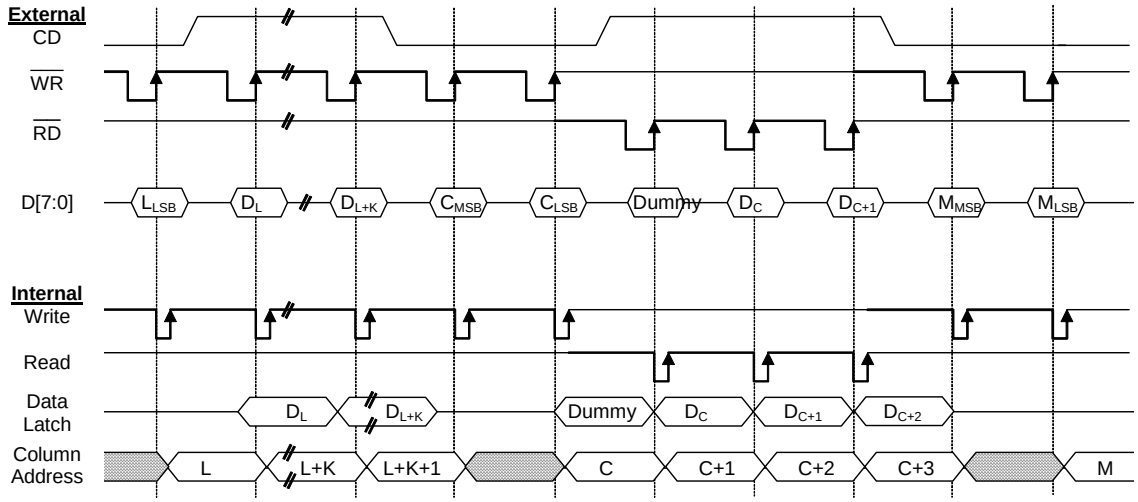


FIGURE 3: 8 bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1681s supports three serial modes, one 4-wire SPI mode (S8), one compact 3/4-wire mode (S8uc) and one 3-wire SPI mode (S9). Bus interface mode is determined by the wiring of the BM[1:0] and D[7:6]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

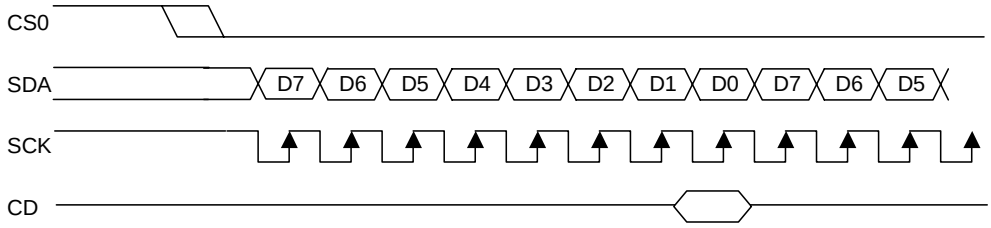


FIGURE 4: 4-wire Serial Interface (S8)

S8UC (3/4-WIRE) INTERFACE

Only write operations are supported in this 3/4-wire serial mode. The data format is identical to S8. The CD pin transitions will reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

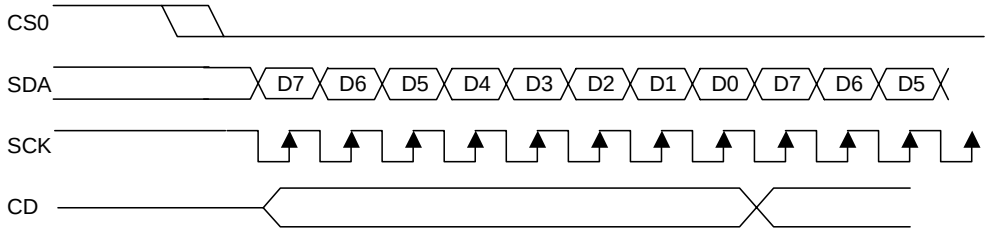


FIGURE 5: 3/4-wire Serial Interface (S8uc)

S9 (3-WIRE) INTERFACE

Only write operations are supported in this 3-wire serial mode. Pins CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

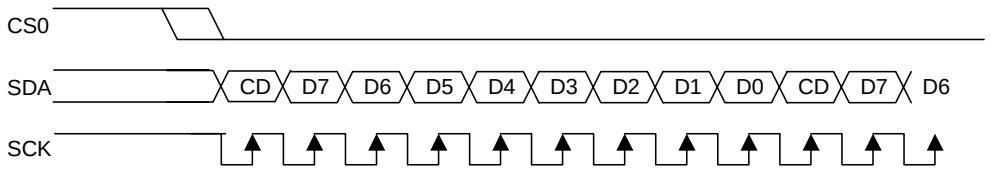


FIGURE 6: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

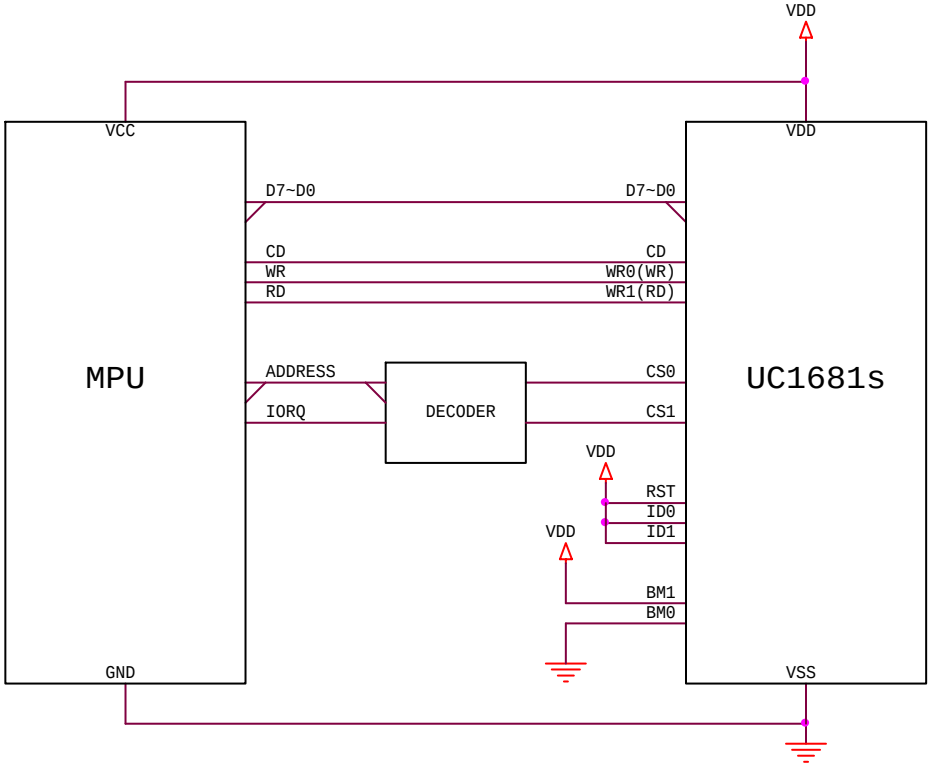


FIGURE 7: 8080/8bit parallel mode reference circuit

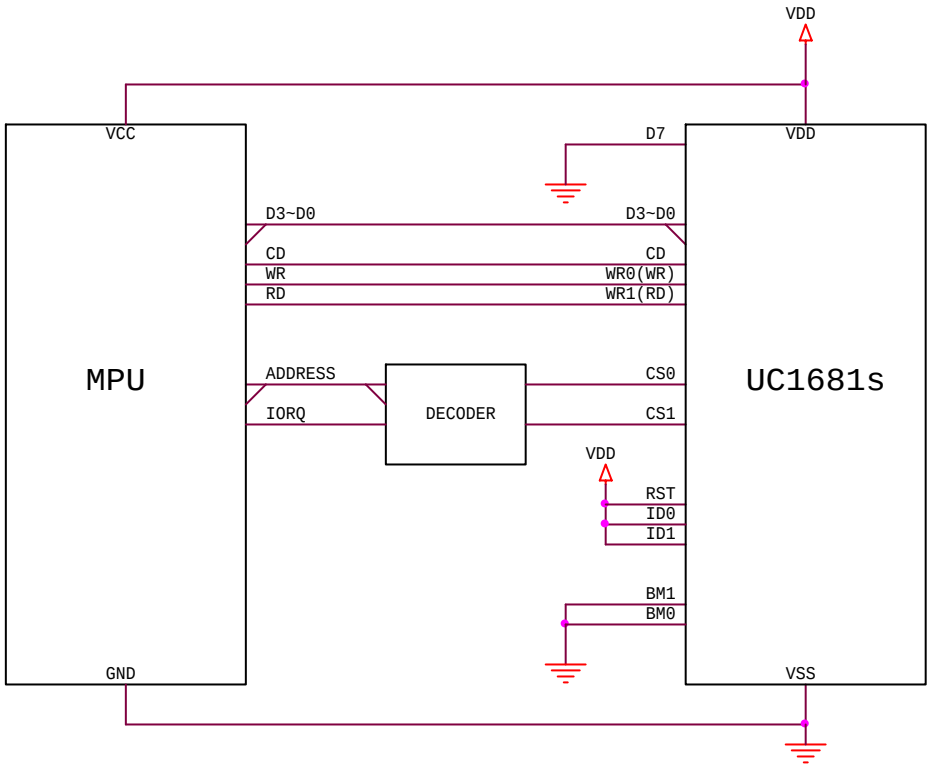


FIGURE 8: 8080/4bit parallel mode reference circuit

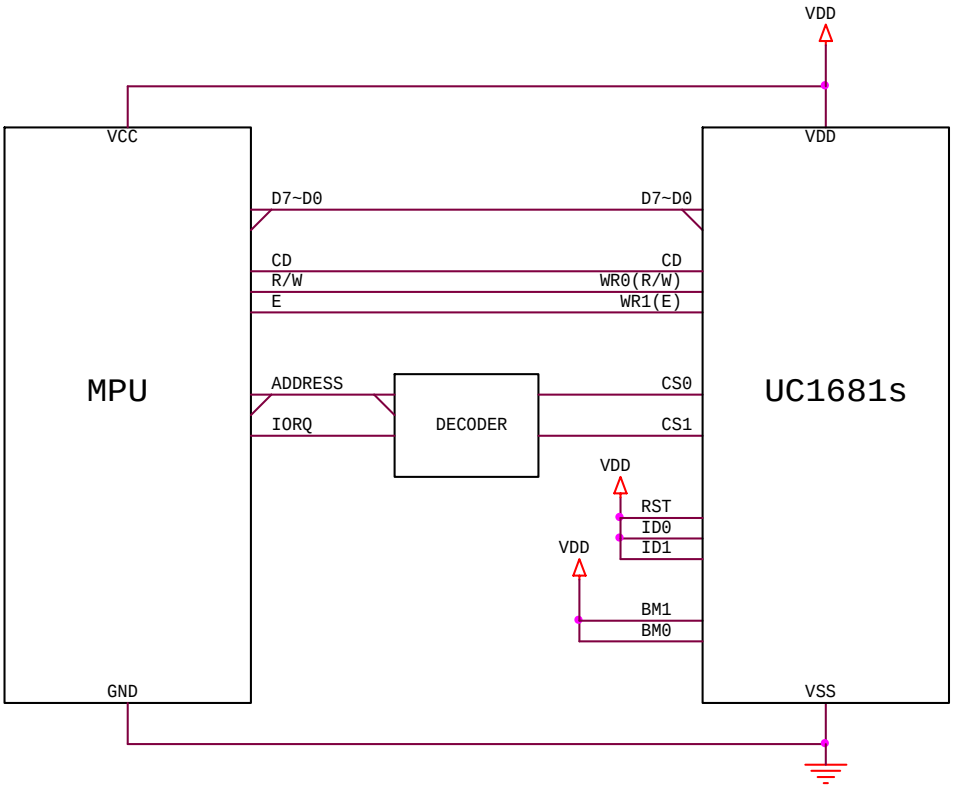


FIGURE 9: 6800/8bit parallel mode reference circuit

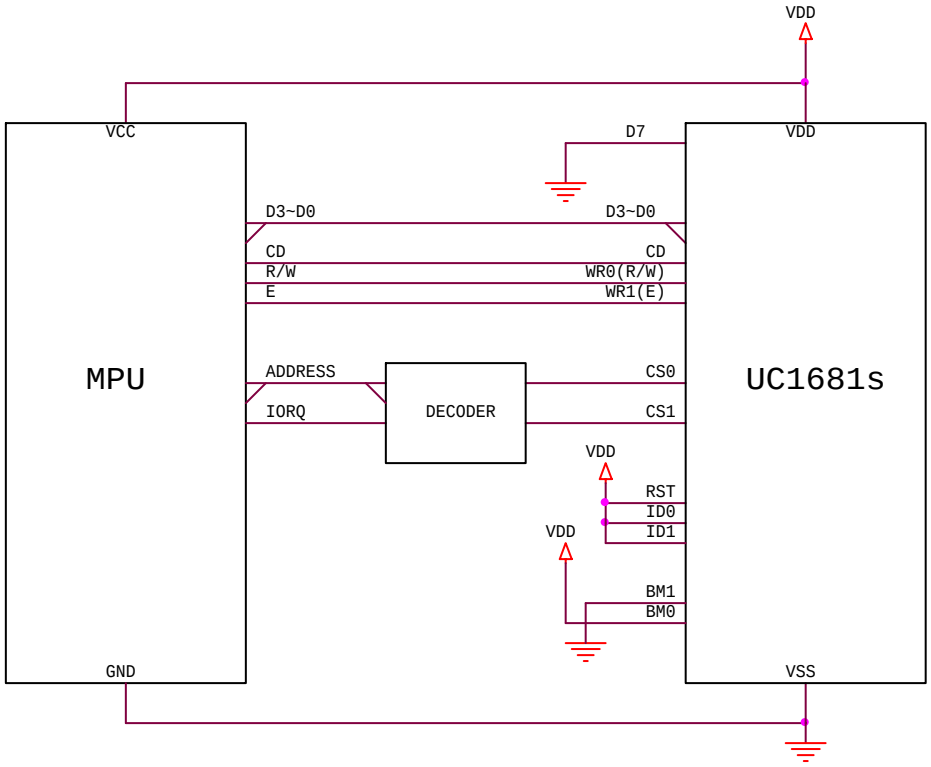


FIGURE 10: 6800/4bit parallel mode reference circuit

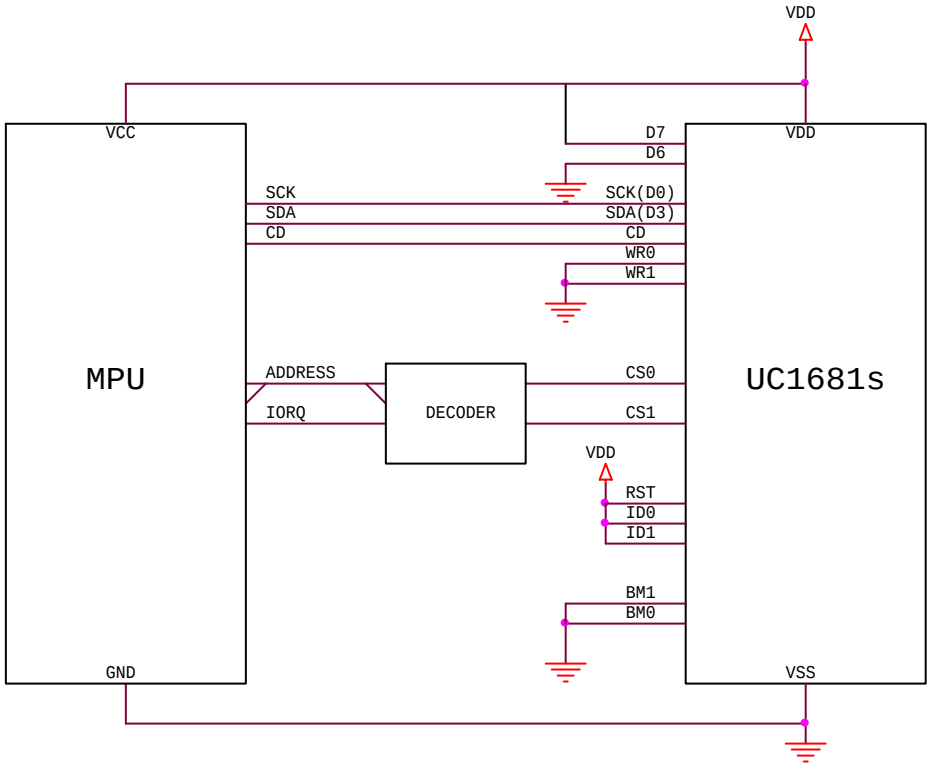


FIGURE 11: 4-Wires SPI (S8) serial mode reference circuit

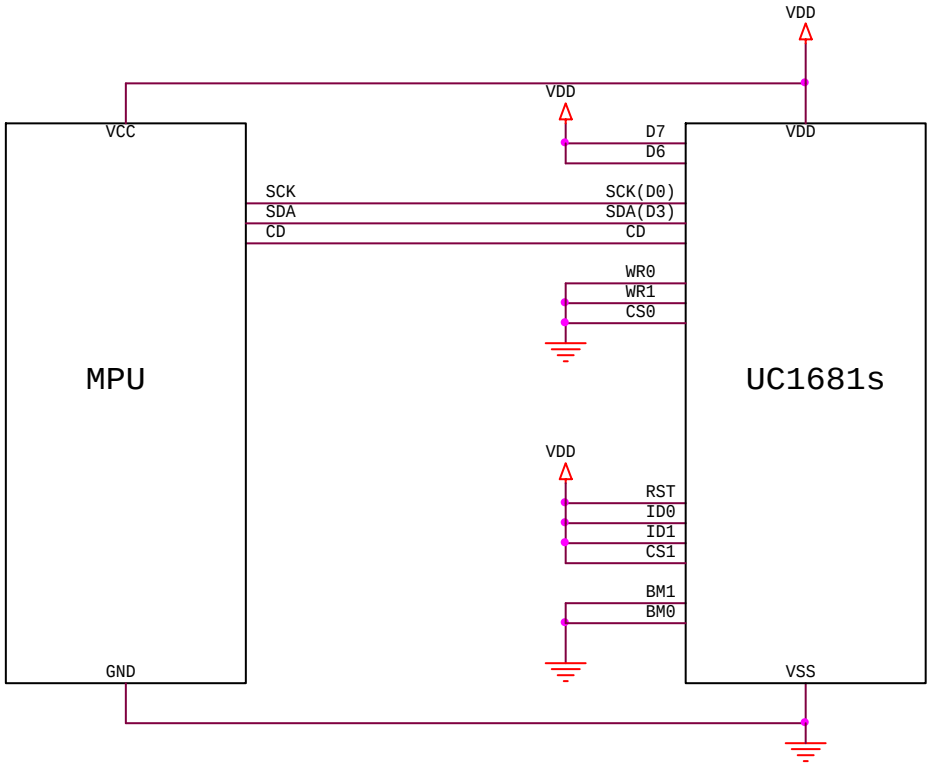


FIGURE 12: 3/4-Wires SPI (S8uc) serial mode reference circuit

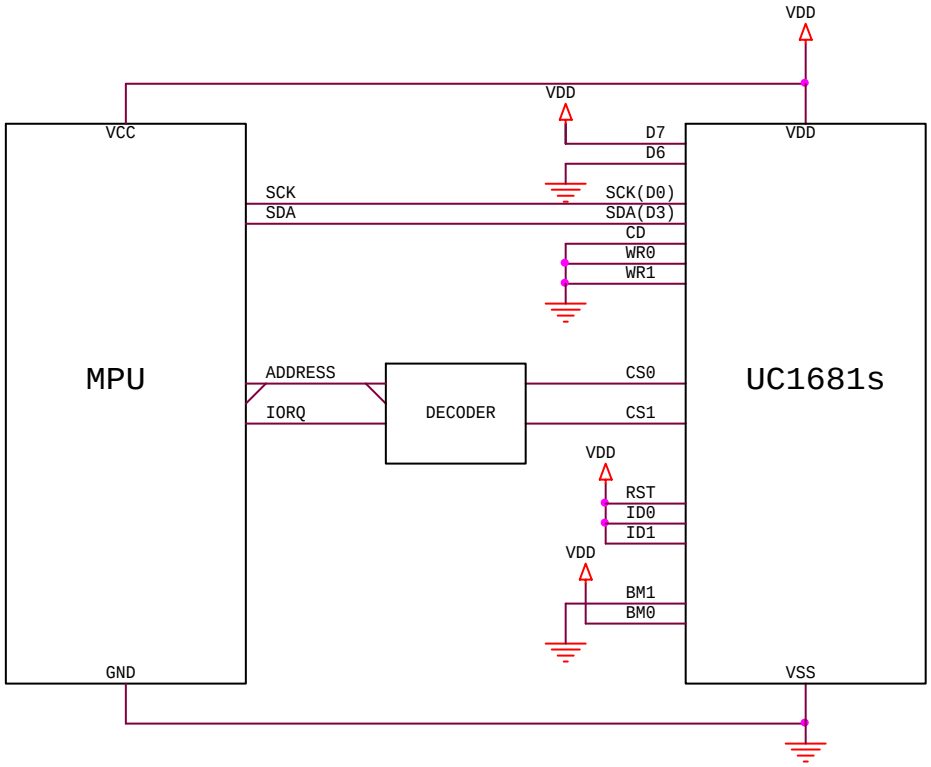


FIGURE 13: 3-Wires SPI (S9) serial mode reference circuit

Note

- ID pin is for production control. The connection will affect the content of D[7] when using *Get Status* command. Connect to V_{DD} for "H" or V_{SS} for "L".
- RST pin is optional. When RST pin is not used, connect the pin to V_{DD}.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 68x98x13.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (97), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 67), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (97–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT,FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

Line = *SL*

Otherwise

Line = Mod(*Line*+1, 68)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *68*. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

Line = Mod(*SL* + *MUX-1*, *68*)
where MUX = CEN + 1

Otherwise

Line = Mod(*Line-1* , *68*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

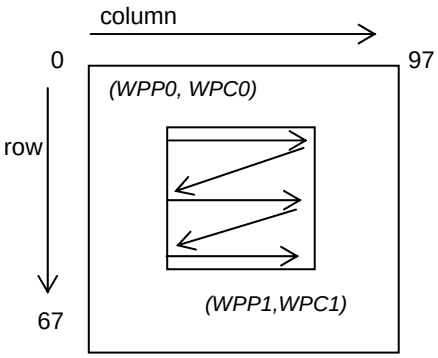
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and then enable AC[4]. After AC[4] sets, data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). AC[4] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

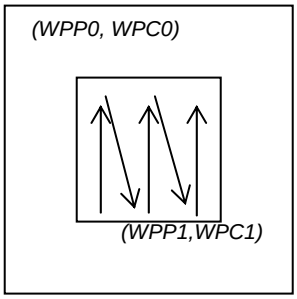
Example1:

AC[2:0] = 001 MX=0



Example 2:

AC[2:0] = 111 MX = 0



Row Adderss	RAM												MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H													COM1	COM53	COM68	COM16
01H													COM2	COM54	COM67	COM15
02H													COM3	COM55	COM66	COM14
03H													COM4	COM56	COM65	COM13
04H													COM5	COM57	COM64	COM12
05H													COM6	COM58	COM63	COM11
06H													COM7	COM59	COM62	COM10
07H													COM8	COM60	COM61	COM9
08H													COM9	COM61	COM60	COM8
09H													COM10	COM62		COM7
0AH													COM11	COM63		COM6
0BH													COM12	COM64		COM5
0CH													COM13	COM65		COM4
0DH													COM14	COM66		COM3
0EH													COM15	COM67		COM2
0FH													COM16	COM68		COM1
10H													COM17	COM1		COM68
11H													COM18	COM2		COM67
12H													COM19	COM3		COM66
13H													COM20	COM4		COM65
14H													COM21	COM5		COM64
15H													COM22	COM6		COM63
16H													COM23	COM7		COM62
17H													COM24	COM8		COM61
18H													COM25	COM9		COM60
19H													COM26	COM10		COM59
1AH													COM27	COM11		COM58
1BH													COM28	COM12		COM57
1CH													COM29	COM13		COM56
2CH																COM40
2DH																COM39
2EH																COM38
2FH																COM37
30H																COM36
31H																COM35
32H																COM34
33H																COM33
34H																COM32
35H																COM31
36H																COM30
37H																COM29
38H																COM28
39H																COM27
3AH																COM26
3BH																COM25
3CH																COM24
3DH																COM23
3EH																COM22
3FH													COM64	COM48	COM5	COM21
40H													COM65	COM49	COM4	COM20
41H													COM66	COM50	COM3	COM19
42H													COM67	COM51	COM2	COM18
43H													COM68	COM52	COM1	COM17

MX	SEG1	SEG2	SEG3	SEG4	SEG5			SEG290	SEG291	SEG292	SEG293	SEG294
0	SEG1	SEG2	SEG3	SEG4	SEG5			SEG290	SEG291	SEG292	SEG293	SEG294
1	SEG292	SEG293	SEG294	SEG289	SEG290			SEG5	SEG6	SEG1	SEG2	SEG3

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 60.5K color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

⇒ 1st Byte write data: 11111111b

⇒ 2nd Byte write data: 11111111b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1681s has two different types of Reset:
Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 5~10mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1681s enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1681s has three operating modes (OM):
Reset, Sleep, Normal.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0}, C_{B1}, and C_L. To drain these capacitors, use Reset command to activate the on-chip draining circuit.

Action	Mode	OM
Reset command or RST_ pin pulled "L" Power ON Reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Even though UC1681s consumes very little energy in Sleep mode (typically 5uA or less); however, since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1681s contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1681s internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1681s power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait ~150 mS before the CPU starting to issue commands to UC1681s. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on V_{DD}, $V_{DD2/3}$ should be started not later than V_{DD}.

Delay allowance between V_{DD} and $V_{DD2/3}$ is illustrated as Figure 16.

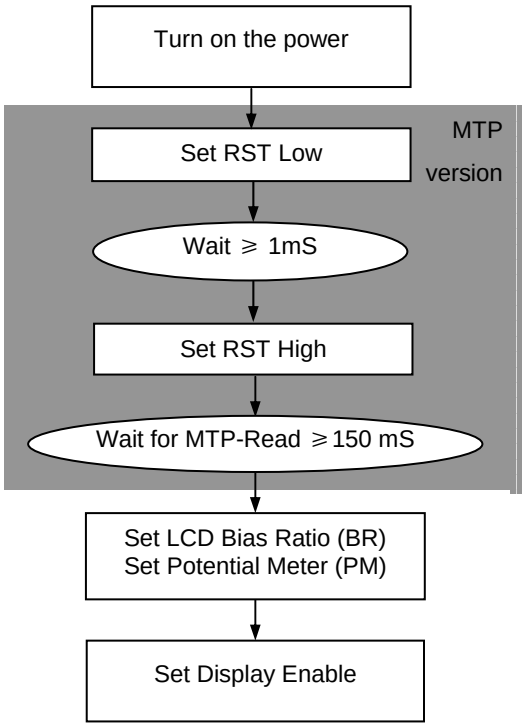


Figure 14: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+}, C_{BX-}, and C_L from damaging the LCD, when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_{B+}. For example, if C_L is 15nF, then the draining time required for V_{LCD} is 0.5~1mS.

When external V_{LCD} is used, UC1681s will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

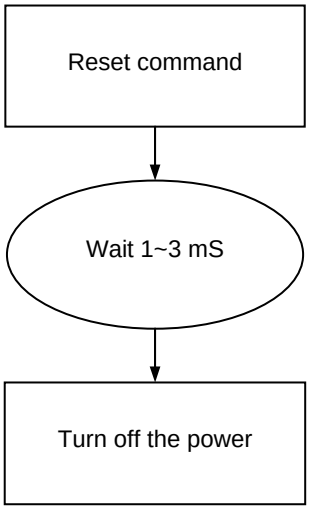


Figure 15: Reference Power-Down Sequence

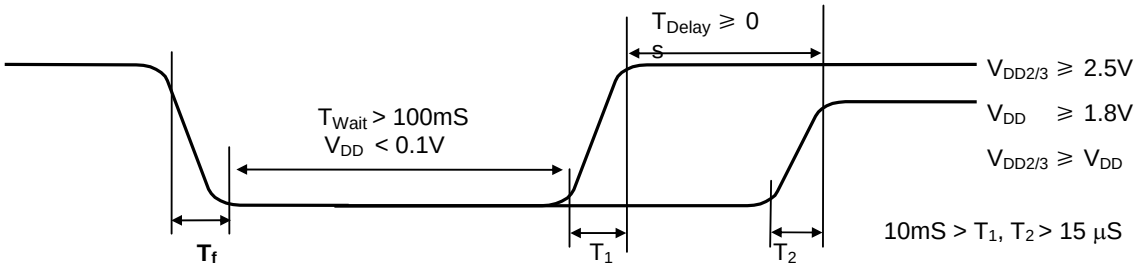


Figure 16: Delay allowance and Power Off-On Sequence

MULTI-TIME PROGRAM NV MEMORY

OVERVIEW

MTP feature is available for UC1681s such that LCM maker can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1681s:
MTP-Erase, MTP-Program, MTP-Read.

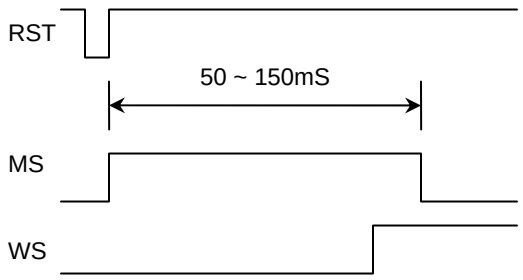
MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1681s, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1681s, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the *Read Status* commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use *Read Status* command in a polling loop to make sure {MS,WS}={0,1} before proceeding with the `Set Display Enable` command, however, it may be simpler to just issue the `Set Display Enable` command every 0.2~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above “Periodical re-initializing” approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command. This enables the ICs to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software *RESET* for normal operation control purpose and hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operation, TST4 should be open, or connected to V_{DD3}.

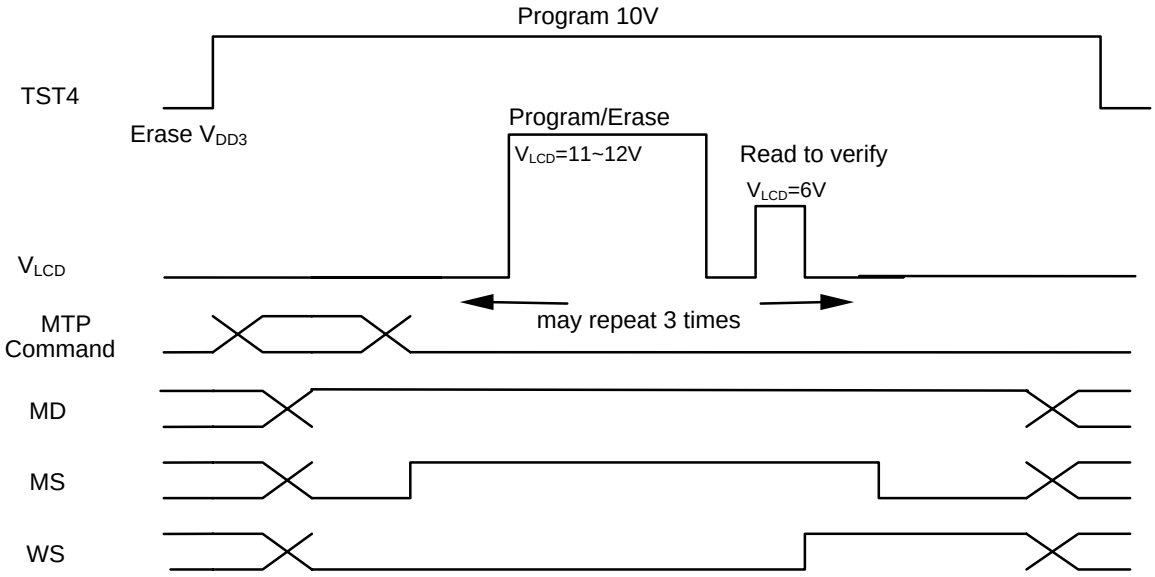
Operation	**V_{LCD}**	**TST4 (external input)**
Program	MTP3 : 86h (12V)	10V (1mA per bit)
Erase	MTP3 : 86h (12V)	Floating or V_{DD3}
Read	MTP2 : 57h (6V)	Floating or V_{DD3}

Note:

1. Do Erase before Program. Program one bit at a time.
2. When doing MTP Program or Erase, it's required to use $V_{DD2/3} \geqq 3.0V$.

2. Read MTP status bits

With normal Get Status method (CD=0,W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

MTP CELL VALUE USAGE

There are 9 MTP cell bits. They are divided into two groups for different trimming purpose.

(1) MTP[6:0] : V_{LCD} Trim

When PMO[6]=1: PM with trim = PM - PMO[5:0]
When PMO[6]=0: PM with trim = PM + PMO[5:0]

(2) MTPID[1:0] : For LCM manufacturer's configuration.

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	1	0	1	0	1	1	1		MTP2: 57h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	1	0	0	0	0	1	1	0		MTP3: 86h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	0	0	0		MTP4:20h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	0	1	0		MTP5:02h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	1 0	MTPM MTP1	Ex: To program PMO[6:0]=0000001b MID[1:0],= 00b set MTPM to 00000001b * set MTP1 to 00000000b
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	ws	-	MS	Get Status & PM	Check MTP Status until MS=0 and WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	1	0	1	0	1	1	1		MTP2: 57h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	1	0	0	0	0	1	1	0		MTP3: 86h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	0	0	0		MTP4:20h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	0	1	0		MTP5:02h(10ms)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0 0	1 0	1 0	1 0	1 0	1 0	1 1	1 1	MTPM MTP1	Ex: To erase PMO[6:0]MID[1:0] set MTPM to 01111111b set MTP1 to 00000011b*
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	ws	-	MS	Get Status & PM	Check MTP Status
												until MS=0 WS=1
R											V_{DD}=0V	Power OFF

* It is recommended that users clear all the bits to be programmed.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display On-Off operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~150mS after V_{DD} is ON
R	0 0	0 0	0 0	0 0	1 0	1 1	0 0	0 0	1 0	0 0	Set APC Command	Turn off SRAM power saving
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	Set Color Mode	
C	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Driving voltage (-25^{O}C ~ +75^{O}C)	-0.3	+11.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} is based on V_{SS} = 0V.
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.3	V
$V_{DD2/3}$	Supply for bias & pump	$1.3 \geqslant V_{DD2/3} - V_{DD} \geqslant 0$	2.5		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ = 2.8V, 25^{O}C		11.2	11.8	V
V_D	LCD data voltage	$V_{DD2/3}$ = 2.8V, 25^{O}C	0.95		1.64	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3}$ = 3.3V, Temp = 85^{o}C			50	μA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 10V		1.15	2.0	KΩ
$R_{ON(COM-vcms)}$	COM output impedance	V_{LCD} = 10V		1.5	2.5	KΩ
$R_{ON(COM-vcn)}$	COM output impedance	V_{LCD} = 10V		3.5	4.5	KΩ
f_{LINE}	Average Line rate	LC[4:3] = 10b	-10%	17.7	+10%	Klps

POWER CONSUMPTION

(Data with COB:)

V_{DD} = 2.70V,
V_{LCD} = 11.32,
Mux Rate = 68,
C_B = 2.2 μF,
Color Mode = 60.5K mode,
Bias Ratio = 9,
Line Rate = 17.7 Klps,
Bus mode = 6800,
Temperature = 25^{o}C,
All HV outputs are open circuit.
PM = 108,
Panel Loading (PC[1:0]) = 9~12 nF,
C_L = 47 nF,
MTP = 00H,

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-Pixel-OFF	Data Bus = idle, SEG/COM open	405.70	608.2
2-pixel checker	Data Bus = idle, SEG/COM open	540.26	810.39
None	Reset (stand-by current)	--	5

AC CHARACTERISTICS

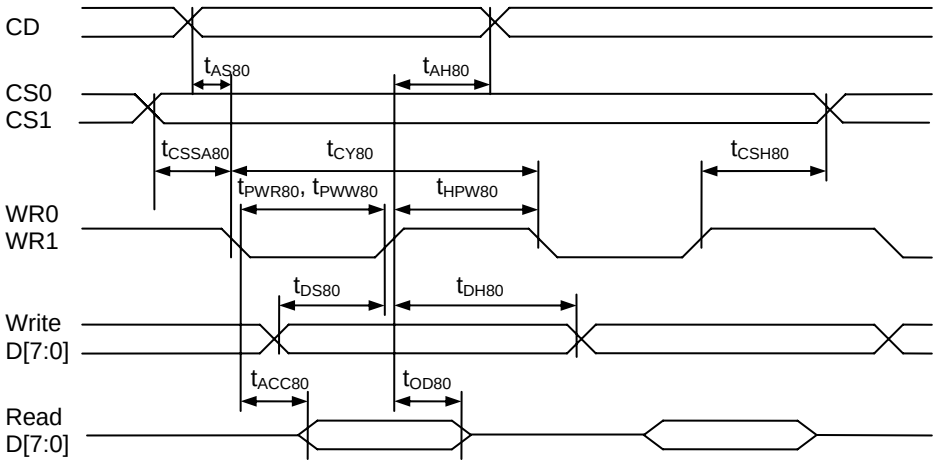


FIGURE 17: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		10 15	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 25	80 25	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		15 30	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 280 160 280 160	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits (read)		140 140	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits (write)		80 80	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		60 30	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	- 50	160 50	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10		nS

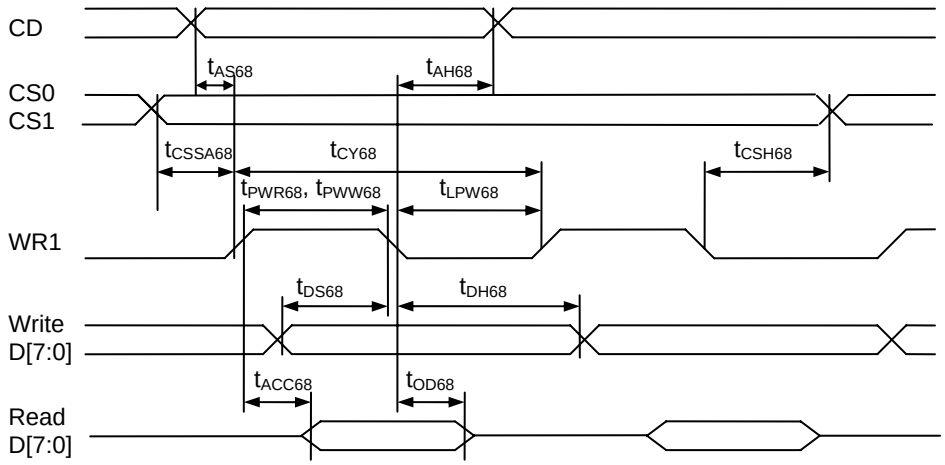


FIGURE 18: Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ⩽ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		10 20	–	nS
t_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 90	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 25	80 25	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		15 40	–	nS
t_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 280 160 280 160	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		140 140	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		80 80	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 30	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	- 50	160 50	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10		nS

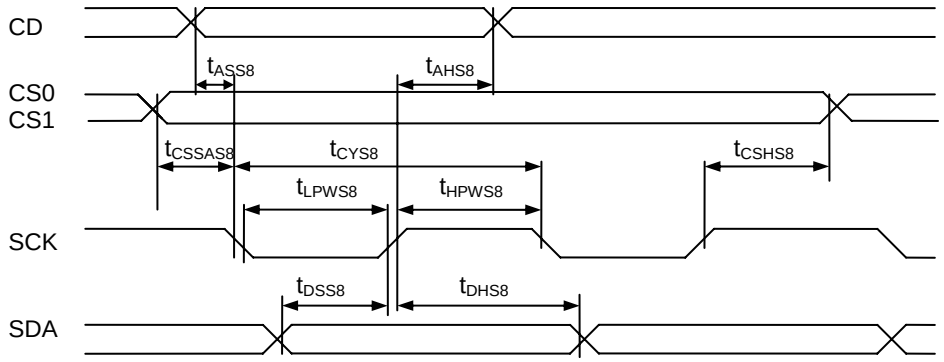


FIGURE 19: Serial Bus Timing Characteristics (for S8)

(2.5V ⩽ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		15	–	nS
t_{CYS8}	SCK	System cycle time		90	–	nS
t_{LPWS8}		Low pulse width		35	–	nS
t_{HPWS8}		High pulse width		35	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 5		nS

(1.65V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		30	–	nS
t_{CYS8}	SCK	System cycle time		180	–	nS
t_{LPWS8}		Low pulse width		70	–	nS
t_{HPWS8}		High pulse width		70	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		60 40	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10		nS

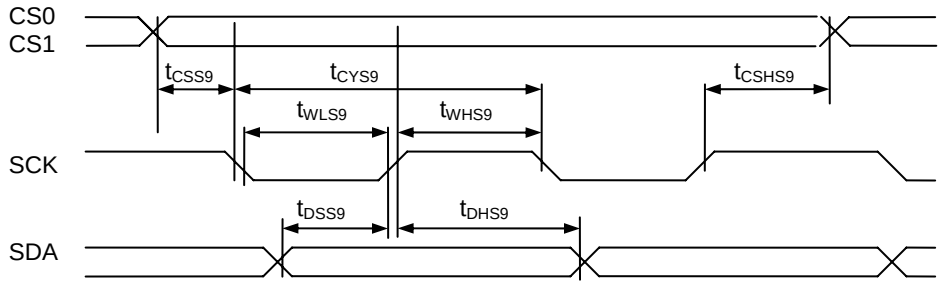


FIGURE 20: Serial Bus Timing Characteristics (for S9)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		90	–	nS
t_{LPWS9}		Low pulse width		35	–	nS
t_{HPWS9}		High pulse width		35	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		180	–	nS
t_{LPWS9}		Low pulse width		70	–	nS
t_{HPWS9}		High pulse width		70	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		60 40	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10		nS

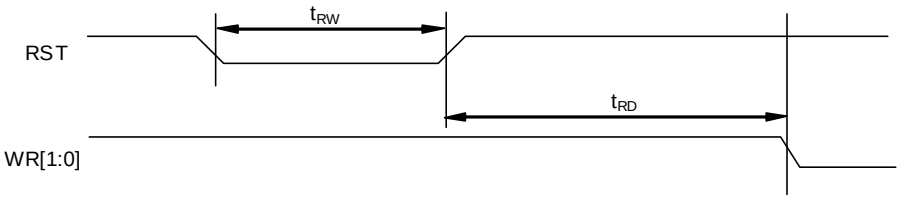


FIGURE 21: Reset Characteristics

(1.65V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	µS
t_{RD}	RST, WR	Reset to WR pulse delay		10		mS

PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE:
11627 x 1263 μM^2

DIE THICKNESS:
0.5 mm

BUMP HEIGHT:
15 μM
H_{MAX} - H_{MIN} (within die) < 2 μM

BUMP SIZE:
SEG/COM: 23x103 μM^2

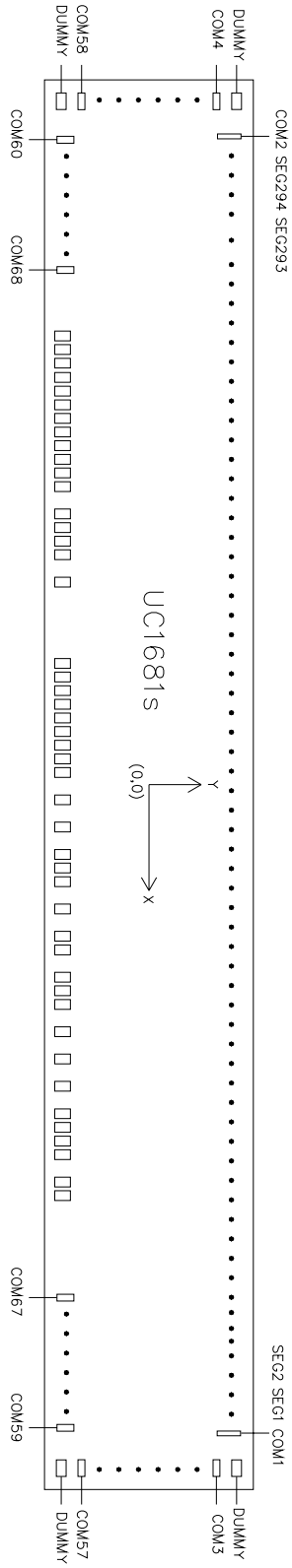
BUMP PITCH:
SEG: 38 μM (Typ.)
COM: 38 μM (Typ.)

BUMP GAP:
SEG/COM: 15 μM (Typ.)

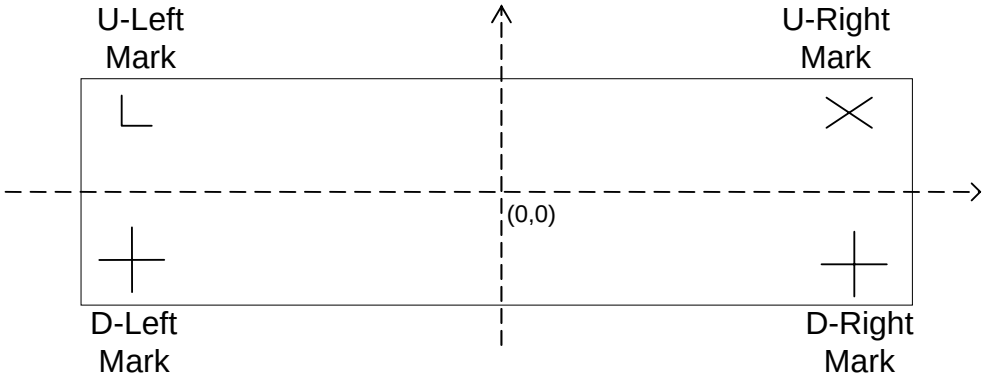
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

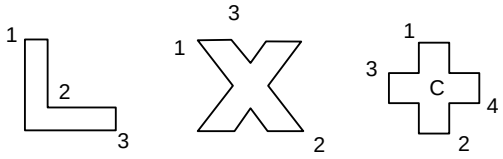
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

The “x” and “+” marks are symmetric both horizontally and vertically.

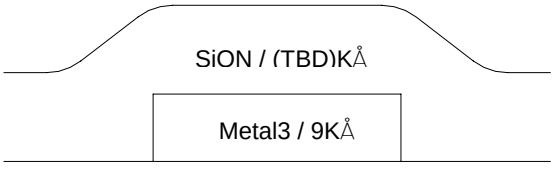
COORDINATES:

	U-Left Mark		U-Right Mark	
	X	Y	X	Y
1	-5627.1	268.5	5598.5	268.5
2	-5615.3	251.6	5627.0	240.0
3	-5598.6	240.0	5606.0	268.5

	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-5637.2	-497.3	5626.2	-497.3
2	-5626.2	-535.3	5637.2	-535.3
3	-5643.7	-510.8	5619.7	-510.8
4	-5619.7	-521.8	5643.7	-521.8
C	-5631.7	-516.3	5631.7	-516.3

Note: The values of the x-coordinate and the y-coordinate in the table are after-rounded.

TOP METAL AND PASS



FOR MTP PROCESS CROSS-SECTION

PAD COORDINATES

#	PAD	X	Y	W	H
1	DUMMY	-5718.3	548.5	103	23
2	COM4	-5718.3	510.5	103	23
3	COM6	-5718.3	472.5	103	23
4	COM8	-5718.3	434.5	103	23
5	COM10	-5718.3	396.5	103	23
6	COM12	-5718.3	358.5	103	23
7	COM14	-5718.3	320.5	103	23
8	COM16	-5718.3	282.5	103	23
9	COM18	-5718.3	244.5	103	23
10	COM20	-5718.3	206.5	103	23
11	COM22	-5718.3	168.5	103	23
12	COM24	-5718.3	130.5	103	23
13	COM26	-5718.3	92.5	103	23
14	COM28	-5718.3	54.5	103	23
15	COM30	-5718.3	16.5	103	23
16	COM32	-5718.3	-21.5	103	23
17	COM34	-5718.3	-59.5	103	23
18	COM36	-5718.3	-97.5	103	23
19	COM38	-5718.3	-135.5	103	23
20	COM40	-5718.3	-173.5	103	23
21	COM42	-5718.3	-211.5	103	23
22	COM44	-5718.3	-249.5	103	23
23	COM46	-5718.3	-287.5	103	23
24	COM48	-5718.3	-325.5	103	23
25	COM50	-5718.3	-363.5	103	23
26	COM52	-5718.3	-401.5	103	23
27	COM54	-5718.3	-439.5	103	23
28	COM56	-5718.3	-477.5	103	23
29	COM58	-5718.3	-515.5	103	23
30	DUMMY	-5718.3	-553.5	103	23
31	COM60	-5576.8	-536.3	23	103
32	COM62	-5538.8	-536.3	23	103
33	COM64	-5500.8	-536.3	23	103
34	COM66	-5462.8	-536.3	23	103
35	COM68	-5424.8	-536.3	23	103
36	DATA7	-4946.4	-545.8	54	84
37	VDDX	-4875.7	-545.8	54	84
38	DATA6	-4805.4	-545.8	54	84
39	DATA5	-4550.4	-545.8	54	84
40	DATA4	-4479.4	-545.8	54	84
41	DATA3	-4224.4	-545.8	54	84
42	DATA2	-4153.4	-545.8	54	84
43	DATA1	-3898.4	-545.8	54	84
44	DATA0	-3827.4	-545.8	54	84
45	RST	-3656.4	-545.8	54	84
46	WR0	-3401.4	-545.8	54	84
47	VDDX	-3330.4	-545.8	54	84
48	WR1	-3259.8	-545.8	54	84
49	CD	-3088.8	-545.8	54	84
50	CS0	-2833.8	-545.8	54	84
51	VDDX	-2762.8	-545.8	54	84
52	CS1	-2692.2	-545.8	54	84
53	BM0	-2437.2	-545.8	54	84

#	PAD	X	Y	W	H
54	VDDX	-2366.2	-545.8	54	84
55	BM1	-2295.6	-545.8	54	84
56	TST4	-2124.6	-545.8	54	84
57	TST4	-2054.6	-545.8	54	84
58	TST4	-1984.6	-545.8	54	84
59	TST2	-1598	-545.8	54	84
60	ID0	-1427	-545.8	54	84
61	VDDX	-1356.1	-545.8	54	84
62	ID1	-1285.4	-545.8	54	84
63	VSS	-1114.4	-545.8	54	84
64	VSS	-1044.4	-545.8	54	84
65	VSS	-974.4	-545.8	54	84
66	VSS	-904.4	-545.8	54	84
67	VSS	-834.4	-545.8	54	84
68	VSS	-764.4	-545.8	54	84
69	VSS	-694.4	-545.8	54	84
70	VSS	-624.4	-545.8	54	84
71	VSS	-554.4	-545.8	54	84
72	VSS2	-372.4	-545.8	54	84
73	VSS2	-302.4	-545.8	54	84
74	VSS2	-232.4	-545.8	54	84
75	VSS2	-162.4	-545.8	54	84
76	VSS2	-92.4	-545.8	54	84
77	VSS2	-22.4	-545.8	54	84
78	VSS2	47.6	-545.8	54	84
79	VSS2	117.6	-545.8	54	84
80	VSS2	187.6	-545.8	54	84
81	VDD	257.6	-545.8	54	84
82	VDD	327.6	-545.8	54	84
83	VDD	397.6	-545.8	54	84
84	VDD	467.6	-545.8	54	84
85	VDD	537.6	-545.8	54	84
86	VDD	607.6	-545.8	54	84
87	VDD2	1118.4	-545.8	54	84
88	VDD2	1188.6	-545.8	54	84
89	VDD2	1258.6	-545.8	54	84
90	VDD2	1328.6	-545.8	54	84
91	VDD2	1398.6	-545.8	54	84
92	VDD2	1468.6	-545.8	54	84
93	VDD3	1742.5	-545.8	54	84
94	VDD3	1812.7	-545.8	54	84
95	VB0+	1882.7	-545.8	54	84
96	VB0+	1952.7	-545.8	54	84
97	VB0+	2022.7	-545.8	54	84
98	VB0+	2092.7	-545.8	54	84
99	VB0+	2162.7	-545.8	54	84
100	VB0+	2232.7	-545.8	54	84
101	VB0+	2302.7	-545.8	54	84
102	VB1+	2530.5	-545.8	54	84
103	VB1+	2600.5	-545.8	54	84
104	VB1+	2670.5	-545.8	54	84
105	VB1+	2740.5	-545.8	54	84
106	VB1+	2810.5	-545.8	54	84

#	PAD	X	Y	W	H
107	VB1+	2880.5	-545.8	54	84
108	VB1+	2950.5	-545.8	54	84
109	VB1-	3178.3	-545.8	54	84
110	VB1-	3248.3	-545.8	54	84
111	VB1-	3318.3	-545.8	54	84
112	VB1-	3388.3	-545.8	54	84
113	VB1-	3458.3	-545.8	54	84
114	VB1-	3528.3	-545.8	54	84
115	VB1-	3598.3	-545.8	54	84
116	VB0-	3967.3	-545.8	54	84
117	VB0-	4037.3	-545.8	54	84
118	VB0-	4107.3	-545.8	54	84
119	VB0-	4177.3	-545.8	54	84
120	VB0-	4247.3	-545.8	54	84
121	VB0-	4317.3	-545.8	54	84
122	VB0-	4387.3	-545.8	54	84
123	VLCDIN	4615.1	-545.8	54	84
124	VLCDIN	4685.4	-545.8	54	84
125	VLCDOUT	4755.4	-545.8	54	84
126	VLCDOUT	4825.4	-545.8	54	84
127	COM67	5424.8	-536.3	23	103
128	COM65	5462.8	-536.3	23	103
129	COM63	5500.8	-536.3	23	103
130	COM61	5538.8	-536.3	23	103
131	COM59	5576.8	-536.3	23	103
132	DUMMY	5718.3	-553.5	103	23
133	COM57	5718.3	-515.5	103	23
134	COM55	5718.3	-477.5	103	23
135	COM53	5718.3	-439.5	103	23
136	COM51	5718.3	-401.5	103	23
137	COM49	5718.3	-363.5	103	23
138	COM47	5718.3	-325.5	103	23
139	COM45	5718.3	-287.5	103	23
140	COM43	5718.3	-249.5	103	23
141	COM41	5718.3	-211.5	103	23
142	COM39	5718.3	-173.5	103	23
143	COM37	5718.3	-135.5	103	23
144	COM35	5718.3	-97.5	103	23
145	COM33	5718.3	-59.5	103	23
146	COM31	5718.3	-21.5	103	23
147	COM29	5718.3	16.5	103	23
148	COM27	5718.3	54.5	103	23
149	COM25	5718.3	92.5	103	23
150	COM23	5718.3	130.5	103	23
151	COM21	5718.3	168.5	103	23
152	COM19	5718.3	206.5	103	23
153	COM17	5718.3	244.5	103	23
154	COM15	5718.3	282.5	103	23
155	COM13	5718.3	320.5	103	23
156	COM11	5718.3	358.5	103	23
157	COM9	5718.3	396.5	103	23
158	COM7	5718.3	434.5	103	23
159	COM5	5718.3	472.5	103	23
160	COM3	5718.3	510.5	103	23
161	DUMMY	5718.3	548.5	103	23

#	PAD	X	Y	W	H
162	COM1	5608.3	536.3	23	103
163	SEG1	5570.3	536.3	23	103
164	SEG2	5532.3	536.3	23	103
165	SEG3	5494.3	536.3	23	103
166	SEG4	5456.3	536.3	23	103
167	SEG5	5418.3	536.3	23	103
168	SEG6	5380.3	536.3	23	103
169	SEG7	5342.3	536.3	23	103
170	SEG8	5304.3	536.3	23	103
171	SEG9	5266.3	536.3	23	103
172	SEG10	5228.3	536.3	23	103
173	SEG11	5190.3	536.3	23	103
174	SEG12	5152.3	536.3	23	103
175	SEG13	5114.3	536.3	23	103
176	SEG14	5076.3	536.3	23	103
177	SEG15	5038.3	536.3	23	103
178	SEG16	5000.3	536.3	23	103
179	SEG17	4962.3	536.3	23	103
180	SEG18	4924.3	536.3	23	103
181	SEG19	4886.3	536.3	23	103
182	SEG20	4848.3	536.3	23	103
183	SEG21	4810.3	536.3	23	103
184	SEG22	4772.3	536.3	23	103
185	SEG23	4734.3	536.3	23	103
186	SEG24	4696.3	536.3	23	103
187	SEG25	4658.3	536.3	23	103
188	SEG26	4620.3	536.3	23	103
189	SEG27	4582.3	536.3	23	103
190	SEG28	4544.3	536.3	23	103
191	SEG29	4506.3	536.3	23	103
192	SEG30	4468.3	536.3	23	103
193	SEG31	4430.3	536.3	23	103
194	SEG32	4392.3	536.3	23	103
195	SEG33	4354.3	536.3	23	103
196	SEG34	4316.3	536.3	23	103
197	SEG35	4278.3	536.3	23	103
198	SEG36	4240.3	536.3	23	103
199	SEG37	4202.3	536.3	23	103
200	SEG38	4164.3	536.3	23	103
201	SEG39	4126.3	536.3	23	103
202	SEG40	4088.3	536.3	23	103
203	SEG41	4050.3	536.3	23	103
204	SEG42	4012.3	536.3	23	103
205	SEG43	3974.3	536.3	23	103
206	SEG44	3936.3	536.3	23	103
207	SEG45	3898.3	536.3	23	103
208	SEG46	3860.3	536.3	23	103
209	SEG47	3822.3	536.3	23	103
210	SEG48	3784.3	536.3	23	103
211	SEG49	3746.3	536.3	23	103
212	SEG50	3708.3	536.3	23	103
213	SEG51	3670.3	536.3	23	103
214	SEG52	3632.3	536.3	23	103
215	SEG53	3594.3	536.3	23	103
216	SEG54	3556.3	536.3	23	103

#	PAD	X	Y	W	H
217	SEG55	3518.3	536.3	23	103
218	SEG56	3480.3	536.3	23	103
219	SEG57	3442.3	536.3	23	103
220	SEG58	3404.3	536.3	23	103
221	SEG59	3366.3	536.3	23	103
222	SEG60	3328.3	536.3	23	103
223	SEG61	3290.3	536.3	23	103
224	SEG62	3252.3	536.3	23	103
225	SEG63	3214.3	536.3	23	103
226	SEG64	3176.3	536.3	23	103
227	SEG65	3138.3	536.3	23	103
228	SEG66	3100.3	536.3	23	103
229	SEG67	3062.3	536.3	23	103
230	SEG68	3024.3	536.3	23	103
231	SEG69	2986.3	536.3	23	103
232	SEG70	2948.3	536.3	23	103
233	SEG71	2910.3	536.3	23	103
234	SEG72	2872.3	536.3	23	103
235	SEG73	2834.3	536.3	23	103
236	SEG74	2796.3	536.3	23	103
237	SEG75	2758.3	536.3	23	103
238	SEG76	2720.3	536.3	23	103
239	SEG77	2682.3	536.3	23	103
240	SEG78	2644.3	536.3	23	103
241	SEG79	2606.3	536.3	23	103
242	SEG80	2568.3	536.3	23	103
243	SEG81	2530.3	536.3	23	103
244	SEG82	2492.3	536.3	23	103
245	SEG83	2454.3	536.3	23	103
246	SEG84	2416.3	536.3	23	103
247	SEG85	2378.3	536.3	23	103
248	SEG86	2340.3	536.3	23	103
249	SEG87	2302.3	536.3	23	103
250	SEG88	2264.3	536.3	23	103
251	SEG89	2226.3	536.3	23	103
252	SEG90	2188.3	536.3	23	103
253	SEG91	2150.3	536.3	23	103
254	SEG92	2112.3	536.3	23	103
255	SEG93	2074.3	536.3	23	103
256	SEG94	2036.3	536.3	23	103
257	SEG95	1998.3	536.3	23	103
258	SEG96	1960.3	536.3	23	103
259	SEG97	1922.3	536.3	23	103
260	SEG98	1884.3	536.3	23	103
261	SEG99	1846.3	536.3	23	103
262	SEG100	1808.3	536.3	23	103
263	SEG101	1770.3	536.3	23	103
264	SEG102	1732.3	536.3	23	103
265	SEG103	1694.3	536.3	23	103
266	SEG104	1656.3	536.3	23	103
267	SEG105	1618.3	536.3	23	103
268	SEG106	1580.3	536.3	23	103
269	SEG107	1542.3	536.3	23	103
270	SEG108	1504.3	536.3	23	103
271	SEG109	1466.3	536.3	23	103

#	PAD	X	Y	W	H
272	SEG110	1428.3	536.3	23	103
273	SEG111	1390.3	536.3	23	103
274	SEG112	1352.3	536.3	23	103
275	SEG113	1314.3	536.3	23	103
276	SEG114	1276.3	536.3	23	103
277	SEG115	1238.3	536.3	23	103
278	SEG116	1200.3	536.3	23	103
279	SEG117	1162.3	536.3	23	103
280	SEG118	1124.3	536.3	23	103
281	SEG119	1086.3	536.3	23	103
282	SEG120	1048.3	536.3	23	103
283	SEG121	1010.3	536.3	23	103
284	SEG122	972.3	536.3	23	103
285	SEG123	934.3	536.3	23	103
286	SEG124	896.3	536.3	23	103
287	SEG125	858.3	536.3	23	103
288	SEG126	820.3	536.3	23	103
289	SEG127	782.3	536.3	23	103
290	SEG128	744.3	536.3	23	103
291	SEG129	706.3	536.3	23	103
292	SEG130	668.3	536.3	23	103
293	SEG131	630.3	536.3	23	103
294	SEG132	592.3	536.3	23	103
295	SEG133	554.3	536.3	23	103
296	SEG134	516.3	536.3	23	103
297	SEG135	478.3	536.3	23	103
298	SEG136	440.3	536.3	23	103
299	SEG137	402.3	536.3	23	103
300	SEG138	364.3	536.3	23	103
301	SEG139	326.3	536.3	23	103
302	SEG140	288.3	536.3	23	103
303	SEG141	250.3	536.3	23	103
304	SEG142	212.3	536.3	23	103
305	SEG143	174.3	536.3	23	103
306	SEG144	136.3	536.3	23	103
307	SEG145	98.3	536.3	23	103
308	SEG146	60.3	536.3	23	103
309	SEG147	22.3	536.3	23	103
310	SEG148	-15.7	536.3	23	103
311	SEG149	-53.7	536.3	23	103
312	SEG150	-91.7	536.3	23	103
313	SEG151	-129.7	536.3	23	103
314	SEG152	-167.7	536.3	23	103
315	SEG153	-205.7	536.3	23	103
316	SEG154	-243.7	536.3	23	103
317	SEG155	-281.7	536.3	23	103
318	SEG156	-319.7	536.3	23	103
319	SEG157	-357.7	536.3	23	103
320	SEG158	-395.7	536.3	23	103
321	SEG159	-433.7	536.3	23	103
322	SEG160	-471.7	536.3	23	103
323	SEG161	-509.7	536.3	23	103
324	SEG162	-547.7	536.3	23	103
325	SEG163	-585.7	536.3	23	103
326	SEG164	-623.7	536.3	23	103

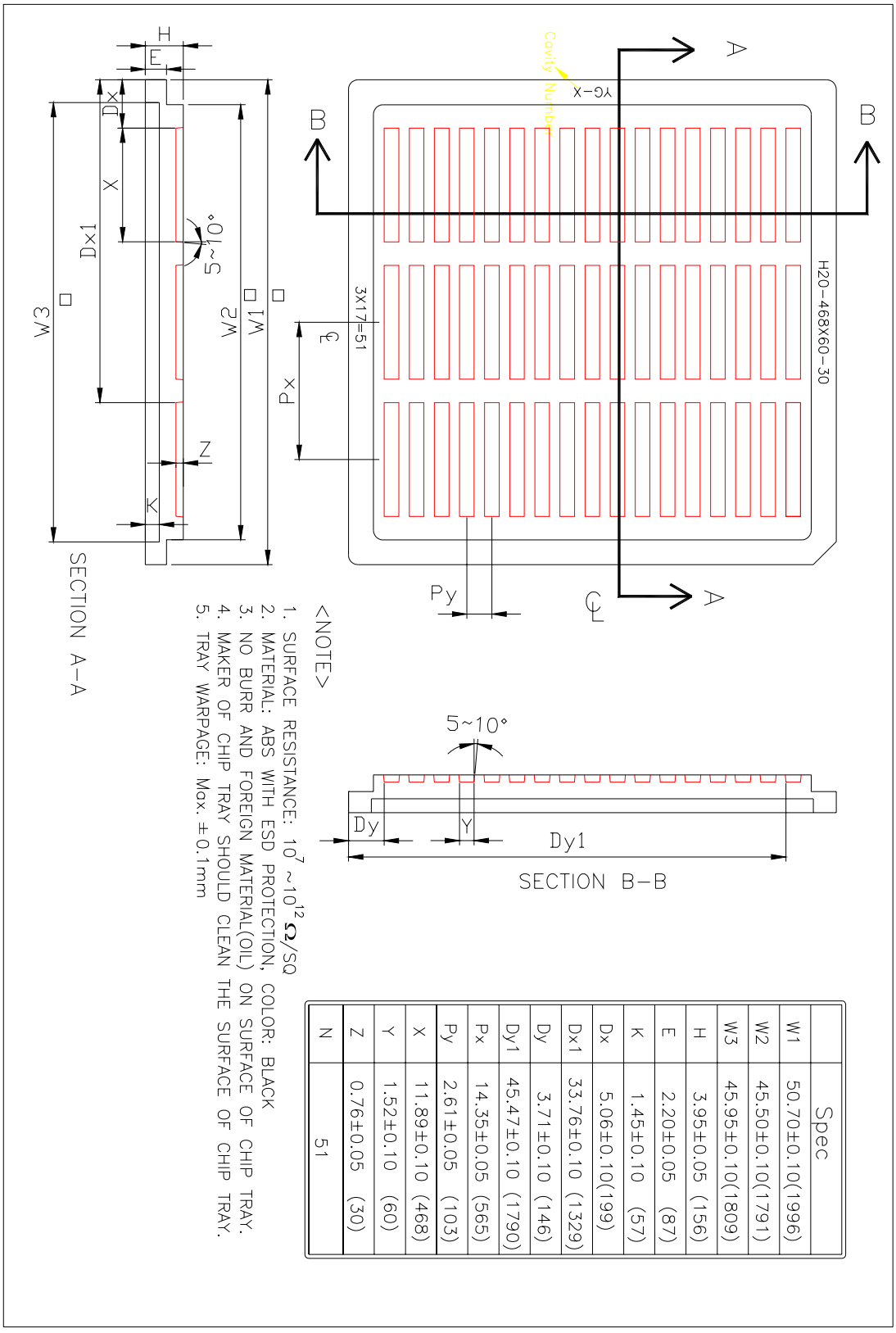
#	PAD	X	Y	W	H
327	SEG165	-661.7	536.3	23	103
328	SEG166	-699.7	536.3	23	103
329	SEG167	-737.7	536.3	23	103
330	SEG168	-775.7	536.3	23	103
331	SEG169	-813.7	536.3	23	103
332	SEG170	-851.7	536.3	23	103
333	SEG171	-889.7	536.3	23	103
334	SEG172	-927.7	536.3	23	103
335	SEG173	-965.7	536.3	23	103
336	SEG174	-1003.7	536.3	23	103
337	SEG175	-1041.7	536.3	23	103
338	SEG176	-1079.7	536.3	23	103
339	SEG177	-1117.7	536.3	23	103
340	SEG178	-1155.7	536.3	23	103
341	SEG179	-1193.7	536.3	23	103
342	SEG180	-1231.7	536.3	23	103
343	SEG181	-1269.7	536.3	23	103
344	SEG182	-1307.7	536.3	23	103
345	SEG183	-1345.7	536.3	23	103
346	SEG184	-1383.7	536.3	23	103
347	SEG185	-1421.7	536.3	23	103
348	SEG186	-1459.7	536.3	23	103
349	SEG187	-1497.7	536.3	23	103
350	SEG188	-1535.7	536.3	23	103
351	SEG189	-1573.7	536.3	23	103
352	SEG190	-1611.7	536.3	23	103
353	SEG191	-1649.7	536.3	23	103
354	SEG192	-1687.7	536.3	23	103
355	SEG193	-1725.7	536.3	23	103
356	SEG194	-1763.7	536.3	23	103
357	SEG195	-1801.7	536.3	23	103
358	SEG196	-1839.7	536.3	23	103
359	SEG197	-1877.7	536.3	23	103
360	SEG198	-1915.7	536.3	23	103
361	SEG199	-1953.7	536.3	23	103
362	SEG200	-1991.7	536.3	23	103
363	SEG201	-2029.7	536.3	23	103
364	SEG202	-2067.7	536.3	23	103
365	SEG203	-2105.7	536.3	23	103
366	SEG204	-2143.7	536.3	23	103
367	SEG205	-2181.7	536.3	23	103
368	SEG206	-2219.7	536.3	23	103
369	SEG207	-2257.7	536.3	23	103
370	SEG208	-2295.7	536.3	23	103
371	SEG209	-2333.7	536.3	23	103
372	SEG210	-2371.7	536.3	23	103
373	SEG211	-2409.7	536.3	23	103
374	SEG212	-2447.7	536.3	23	103
375	SEG213	-2485.7	536.3	23	103
376	SEG214	-2523.7	536.3	23	103
377	SEG215	-2561.7	536.3	23	103
378	SEG216	-2599.7	536.3	23	103
379	SEG217	-2637.7	536.3	23	103
380	SEG218	-2675.7	536.3	23	103
381	SEG219	-2713.7	536.3	23	103

#	PAD	X	Y	W	H
382	SEG220	-2751.7	536.3	23	103
383	SEG221	-2789.7	536.3	23	103
384	SEG222	-2827.7	536.3	23	103
385	SEG223	-2865.7	536.3	23	103
386	SEG224	-2903.7	536.3	23	103
387	SEG225	-2941.7	536.3	23	103
388	SEG226	-2979.7	536.3	23	103
389	SEG227	-3017.7	536.3	23	103
390	SEG228	-3055.7	536.3	23	103
391	SEG229	-3093.7	536.3	23	103
392	SEG230	-3131.7	536.3	23	103
393	SEG231	-3169.7	536.3	23	103
394	SEG232	-3207.7	536.3	23	103
395	SEG233	-3245.7	536.3	23	103
396	SEG234	-3283.7	536.3	23	103
397	SEG235	-3321.7	536.3	23	103
398	SEG236	-3359.7	536.3	23	103
399	SEG237	-3397.7	536.3	23	103
400	SEG238	-3435.7	536.3	23	103
401	SEG239	-3473.7	536.3	23	103
402	SEG240	-3511.7	536.3	23	103
403	SEG241	-3549.7	536.3	23	103
404	SEG242	-3587.7	536.3	23	103
405	SEG243	-3625.7	536.3	23	103
406	SEG244	-3663.7	536.3	23	103
407	SEG245	-3701.7	536.3	23	103
408	SEG246	-3739.7	536.3	23	103
409	SEG247	-3777.7	536.3	23	103
410	SEG248	-3815.7	536.3	23	103
411	SEG249	-3853.7	536.3	23	103
412	SEG250	-3891.7	536.3	23	103
413	SEG251	-3929.7	536.3	23	103
414	SEG252	-3967.7	536.3	23	103
415	SEG253	-4005.7	536.3	23	103
416	SEG254	-4043.7	536.3	23	103
417	SEG255	-4081.7	536.3	23	103
418	SEG256	-4119.7	536.3	23	103
419	SEG257	-4157.7	536.3	23	103
420	SEG258	-4195.7	536.3	23	103
421	SEG259	-4233.7	536.3	23	103
422	SEG260	-4271.7	536.3	23	103
423	SEG261	-4309.7	536.3	23	103
424	SEG262	-4347.7	536.3	23	103
425	SEG263	-4385.7	536.3	23	103
426	SEG264	-4423.7	536.3	23	103
427	SEG265	-4461.7	536.3	23	103
428	SEG266	-4499.7	536.3	23	103
429	SEG267	-4537.7	536.3	23	103
430	SEG268	-4575.7	536.3	23	103
431	SEG269	-4613.7	536.3	23	103
432	SEG270	-4651.7	536.3	23	103
433	SEG271	-4689.7	536.3	23	103
434	SEG272	-4727.7	536.3	23	103
435	SEG273	-4765.7	536.3	23	103
436	SEG274	-4803.7	536.3	23	103

#	PAD	X	Y	W	H
437	SEG275	-4841.7	536.3	23	103
438	SEG276	-4879.7	536.3	23	103
439	SEG277	-4917.7	536.3	23	103
440	SEG278	-4955.7	536.3	23	103
441	SEG279	-4993.7	536.3	23	103
442	SEG280	-5031.7	536.3	23	103
443	SEG281	-5069.7	536.3	23	103
444	SEG282	-5107.7	536.3	23	103
445	SEG283	-5145.7	536.3	23	103
446	SEG284	-5183.7	536.3	23	103
447	SEG285	-5221.7	536.3	23	103
448	SEG286	-5259.7	536.3	23	103
449	SEG287	-5297.7	536.3	23	103
450	SEG288	-5335.7	536.3	23	103
451	SEG289	-5373.7	536.3	23	103
452	SEG290	-5411.7	536.3	23	103
453	SEG291	-5449.7	536.3	23	103
454	SEG292	-5487.7	536.3	23	103
455	SEG293	-5525.7	536.3	23	103
456	SEG294	-5563.7	536.3	23	103
457	COM2	-5601.7	536.3	23	103

(The values of the x-coordinate and the
y-coordinate in the table are after rounded.)

TRAY INFORMATION



	Spec
W1	50.70±0.10(1996)
W2	45.50±0.10(1791)
W3	45.95±0.10(1809)
H	3.95±0.05 (156)
E	2.20±0.05 (87)
K	1.45±0.10 (57)
Dx	5.06±0.10(199)
Dx1	33.76±0.10 (1329)
Dy	3.71±0.10 (146)
Dy1	45.47±0.10 (1790)
Px	14.35±0.05 (565)
Py	2.61±0.05 (103)
X	11.89±0.10 (468)
Y	1.52±0.10 (60)
Z	0.76±0.05 (30)
N	51

REVISION HISTORY

Revision	Contents	Date of Rev.
0.6	(First Released)	Jul. 22, 2005
0.7	(1) The Note description of "V_{DD} to drop below…" is adjusted: 1.7V → 1.65V (Section "Reference COG Layout", page 7)	Jul. 29, 2005
	(2) The RS entry is removed. (Section "Control Registers", page 8)	
	(3) The RS and BZ-related content is removed. (Section "Reset & Power Management" – Reset Status, page 44)	
	(4) The minimum value of V_{DD} is adjusted: 1.8V → 1.65V (Section "Specifications" - DC Characteristics, page 53)	
	(5) The trial condition range is adjusted: 1.8V → 1.65V (Section "AC Characteristics", Pp 54~60)	
0.8	(1) Line Rates are corrected: 14.0, 15.9, 18.7, 20.1 → 13.5, 15.5, 17.7, 20.2 (2) One more set of line rates is added to On-Off mode: 5.7, 6.5, 7.4, 8.5 (Section "Control Register" – LC[4:3], page 9; "Command Description", page 17)	Sep. 29, 2005
	(3) The number of bits used are corrected: [7:0] → [6:0] (Section "Command Table" – (29) ~ (35), page 11; "Command Description" – (29) ~ (35), Pp 22 ~ 23)	
	(4) The V_{LCD} formula is updated. (Section "V_{LCD} Quick Reference", page 28)	
	(5) The typical voltage for MTP is adjusted : 7.8V → 8.5V The voltage range for MTP is also adjusted: 7~8V → 7~9V "MTP allows to program at least 10 times" is added. (Section "MTP NV Memory" - Overview, page 46; "MTP Operation for LCM Makers", Pp 47 ~ 48; "MTP Command Sequence Sample Codes", page 49)	
	(6) The command line is corrected in Program and Erase sample code tables. (Section "MTP Command Sequence Sample Codes", Pp 49 ~ 50)	
	(7) The characteristics of f_{LINE} are adjusted: Conditions: LC[4:3]=11b → 10b Typical: 20.2 → 17.7 Maximum: "—" (score) → +10% (Section "Specifications" – DC Characteristics, page 53)	
	(8) Some AC timings are adjusted. (Section "AC Characteristics", Pp 54~57)	
1.0	(1) The COG drawing is updated due to a typo. (Section "COG Layout", page 7)	Oct. 19, 2005
	(2) The V_{LCD} chart presentation is slightly adjusted. (Section "V_{LCD} Quick Reference, page 28)	
	(3) A remark is added to indicate that the experiment is done with COB. (Section "Specifications" – Power Consumption, page 53)	
	(4) Some AC timings are adjusted. (Section "AC Characteristics", Pp 54-59)	

Revision	Contents	Date of Rev.
1.1	(1) COF is removed from available packing. (Section “Feature Highlights”, page 1; “Pin Description” - V_{DDX}, page 6; “LCD Voltage Setting” – Load Driving Strength, page 27)	Feb. 20, 2006
	(2) One more command line is inserted. (Section “MTP Operation for LCM Makers” – Sample Power Management Command Sequences, page 52)	
1.2	(1) External input, TST4, for Program : 8.5V → 8.8V (2) A note on $V_{DD2/3}$ is added. (Section “MTP Operation for LCM Makers”, Pp 48~50)	Aug. 9, 2006
1.3	(1) The recommended C_B is adjusted: 2.2μF/2V → 2.2μF/5V (Section “Pin Description”, page 4; “Hi-V Generator Reference Circuit”, page 29)	Aug. 29, 2006
	(2) A paragraph on MTP-READ is removed. (Section “Multi-Time Program NV Memory”, page 46)	
	(3) External input for Program, TST4, is adjusted : 8.5V → 10V (Section “MTP Operation for LCM Makers”, Pp 47~49)	
	(4) One more entry, I_{SB}, is added for standby current. (Section “Specifications” – DC Characteristics, page 53)	