TW8819

Ultra Low Cost LCD Controller

The TW8819 is an ultra low cost highly integrated LCD controller. It combines a high quality 2D comb NTSC/PAL/SECAM video decoder, high quality scaler, Font based OSD engine, and image enhancement functions. It also supports panoramic scaling for conversion to wide screen display. The TW8819 supports analog composite video inputs and the output supports a wide variety of digital LCD panel types.

Features

Analog Video Decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM with automatic format detection
- 10-bit ADC and analog clamping circuit
- Fully programmable static gain or automatic gain control for the Y or CVBS channel
- Programmable white peak control for the Y or CVBS channel
- High quality adaptive 2D comb filter for both NTSC and PAL inputs
- PAL delay line for color phase error correction
- Image enhancement with 2D dynamic peaking and CTI
- Digital sub-carrier PLL for accurate color decoding
- Digital horizontal PLL and advanced synchronization processing for VCR playback and weak signal performance
- Programmable hue, brightness, saturation, contrast and sharpness

TFT Panel Support

- Built-in programmable timing controller
- Supports 3, 4, 6 or 8 bits per pixel up to 16.8 million colors with built-in dithering engine
- Supports digital panels up to WXGA+ (1366x768) resolution
- Supports serial (8-bit) RGB panels

Timing Controller (TCON)

- Supports programmable timing interface signals for control
- Column (source) driver/row (gate) driver

On Screen Display

- 256 Font RAM and 512 Display RAM
- Four windows font OSD with bordering/shadowing
- 1/2/3/4 bits/pixel
- Supports variable width (12/16), height (2~32)

Image Processing

- High quality scaler with both up/down and nonlinear scaling support
- Panorama/water-glass scaling
- Built-in 2D de-interlacing function
- Programmable hue, brightness, saturation, contrast and sharpness
- Programmable cropping of input video and graphics
- Independent RGB gain and offset controls
- Programmable 8-bit Gamma correction for each color
- Operates in Frame Sync mode
- Black/White Stretch

Clock Generation

- Spread spectrum clock
- Selectable
- modulation frequency and spread width

Power Management

- Supports functional based independent power down
- 1.8/3.3V operation

Miscellaneous

- Short to Battery Detection Test
- Short to Ground Detection Test
- Supports 2-wire serial bus interface
- Single 27MHz crystal
- 48 pin WFQFN package (Wettable Flank QFN available)

Applications

- Rear camera display
- Video door phone

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1. Overview

1.1 Block Diagram

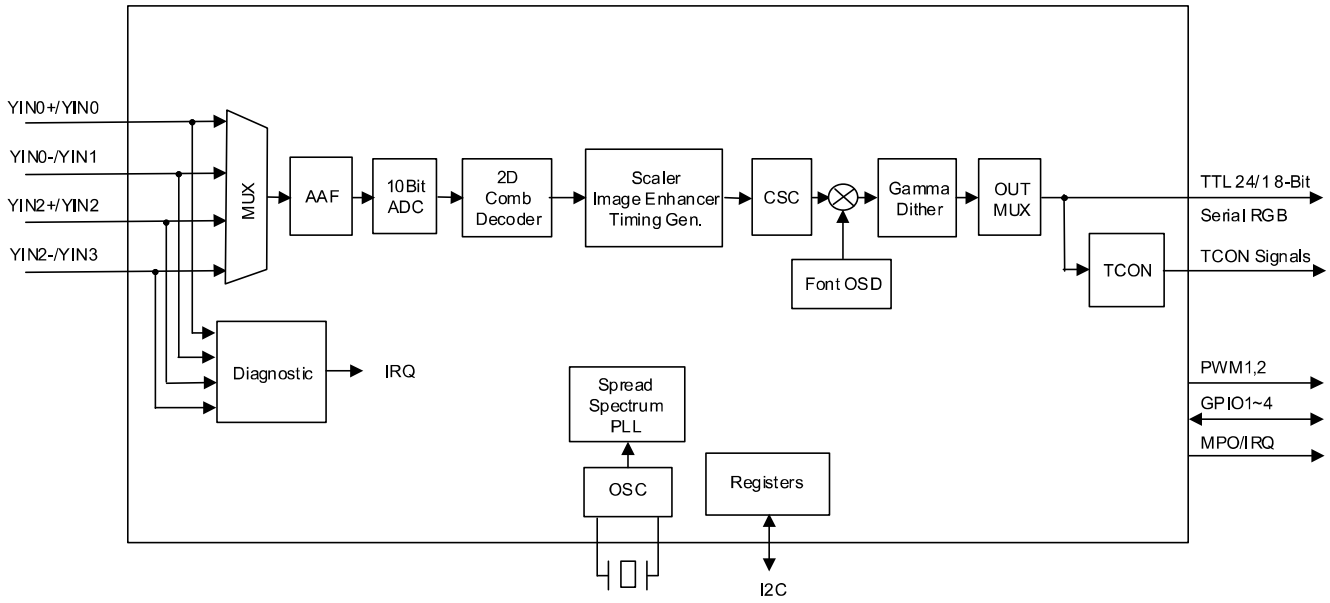
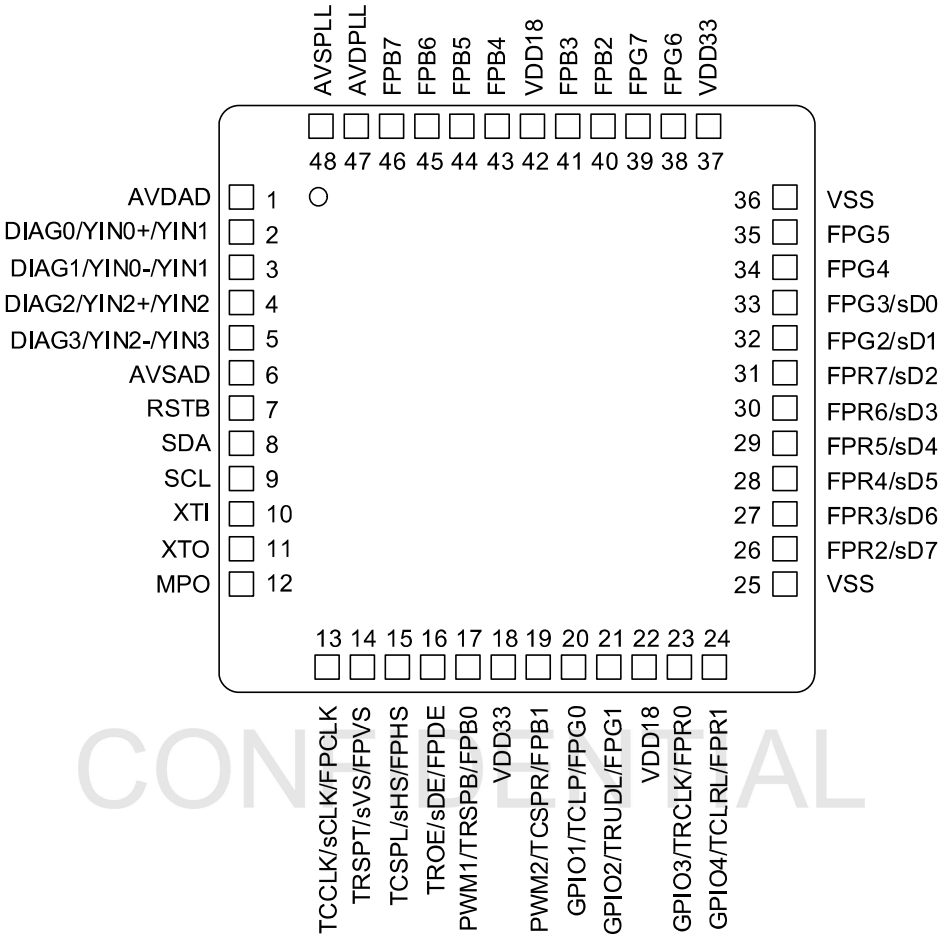


Figure 1. Functional Block Diagram

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2. Pin Information

2.1 Pin Assignments



Top View

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2.2 Pin Descriptions

PIN#	I/O	Pin Name	Description	Internal Connection	Recommended Connection of Unused Pin[1][2][3]	Status at HW Reset
Analog I/F signals and Power						
1	P	AVDAD	Analog A/D Power +1.8V	-	-	Pwr
2	AI	YIN0	Single Ended Analog CVBS input 0	-	Connect to Ground	Hi-Z
		YIN0+	Differential CVBS Positive input 0			
		DIAG0	Short Detection input 0			
3	AI	YIN1	Single Ended Analog CVBS input 1			
		YIN0 –	Differential CVBS Negative input 0			
		DIAG1	Short Detection input 1			
4	AI	YIN2	Single Ended Analog CVBS input 2			
		YIN2+	Differential CVBS Positive input 2			
		DIAG2	Short Detection input 2			
5	AI	YIN3	Single Ended Analog CVBS input 3			
		YIN2 –	Differential CVBS Negative input 2			
		DIAG3	Short Detection input 3			
6	P	AVSAD	Analog A/D Ground	-	-	Pwr
47	P	AVDPLL	PLL (Internal Analog) Power +1.8V	-	-	Pwr
48	P	AVSPLL	PLL (Internal Analog) Ground	-	-	Pwr
DIGITAL I/F signals						
7	I	RSTB	Reset Pin	-	-	-
8	I/O	SDA	I2C Data	-	Connect through pull up resistor	Hi-Z
9	I	SCL	I2C Clock	-	Connect through pull up resistor	Hi-Z
10	I	XTI	Crystal terminal or Oscillator input	-	-	-
11	O	XTO	Crystal terminal	-	Open/Unconnected	-
12	O	MPO	Multi-Purpose output	-	Open/Unconnected	Hi-Z
13	O	FPCLK	Flat Panel Clock	-	Open/Unconnected	Hi-Z
		sCLK	Serial RGB Clock			
		TCCLK	TCON Column Driver Clock			
14	O	FPVS	Flat Panel VSYNC	-	Open/Unconnected	Hi-Z
		sVS	Serial RGB VSYNC			
		TRSPT	TCON Row Driver Start Pulse (Top)			
15	O	FPHS	Flat Panel HSYNC	-	Open/Unconnected	Hi-Z
		sHS	Serial RGB HSYNC			
		TCSPL	TCON Column Driver Start Pulse (Left)			

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PIN#	I/O	Pin Name	Description	Internal Connection	Recommended Connection of Unused Pin[1][2][3]	Status at HW Reset
16	O	FPDE	Flat Panel Data Enable	-	Open/Unconnected	Hi-Z
		sDE	Serial RGB Data Enable			
		TROE	TCON Row Driver Output Enable			
17	O	FPB0	Flat Panel Output Blue Bit[0]	-	Open/Unconnected	Hi-Z
		TRSPB	TCON Row Driver Start Pulse (Bottom)			
		PWM1	PWM Control 1			
19	O	FPB1	Flat Panel Output Blue Bit[1]	-	Open/Unconnected	Hi-Z
		TCSPR	TCON Column Driver Start Pulse (Right)			
		PWM2	PWM Control 2			
20	I/O	FPG0	Flat Panel Output Green Bit[0]	-	Open/Unconnected	Hi-Z
		TCLP	TCON Column Driver Latch Pulse			
		GPIO1	General Purpose I/O			
21	I/O	FPG1	Flat Panel Output Green Bit[1]	-	Open/Unconnected	Hi-Z
		TRUDL	TCON Row Driver Up/Down Control			
		GPIO2	General Purpose I/O			
23	I/O	FPR0	Flat Panel Output Red Bit[0]	-	Open/Unconnected	Hi-Z
		TRCLK	TCON Row Driver Clock			
		GPIO3	General Purpose I/O			
24	I/O	FPR1	Flat Panel Output Red Bit[1]	-	Open/Unconnected	Hi-Z
		TCLRL	TCON Column Driver L/R Control			
		GPIO4	General Purpose I/O			
26	O	FPR2	Flat Panel Output Red Bit[2]	-	Open/Unconnected	Hi-Z
		sD7	Serial RGB Output Data 7			
27	O	FPR3	Flat Panel Output Red Bit[3]	-	Open/Unconnected	Hi-Z
		sD6	Serial RGB Output Data 6			
28	O	FPR4	Flat Panel Output Red Bit[4]	-	Open/Unconnected	Hi-Z
		sD5	Serial RGB Output Data 5			
29	O	FPR5	Flat Panel Output Red Bit[5]	-	Open/Unconnected	Hi-Z
		sD4	Serial RGB Output Data 4			
30	O	FPR6	Flat Panel Output Red Bit[6]	-	Open/Unconnected	Hi-Z
		sD3	Serial RGB Output Data 3			
31	O	FPR7	Flat Panel Output Red Bit[7]	-	Open/Unconnected	Hi-Z
		sD2	Serial RGB Output Data 2			
32	O	FPG2	Flat Panel Output Green Bit[2]	-	Open/Unconnected	Hi-Z
		sD1	Serial RGB Output Data 1			

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PIN#	I/O	Pin Name	Description	Internal Connection	Recommended Connection of Unused Pin[1][2][3]	Status at HW Reset
33	O	FPG3	Flat Panel Output Green Bit[3]	-	Open/Unconnected	Hi-Z
		sD0	Serial RGB Output Data 0			
34	O	FPG4	Flat Panel Output Green Bit[4]	-	Open/Unconnected	Hi-Z
35	O	FPG5	Flat Panel Output Green Bit[5]	-	Open/Unconnected	Hi-Z
38	O	FPG6	Flat Panel Output Green Bit[6]	-	Open/Unconnected	Hi-Z
39	O	FPG7	Flat Panel Output Green Bit[7]	-	Open/Unconnected	Hi-Z
40	O	FPB2	Flat Panel Output Blue Bit[2]	-	Open/Unconnected	Hi-Z
41	O	FPB3	Flat Panel Output Blue Bit[3]	-	Open/Unconnected	Hi-Z
43	O	FPB4	Flat Panel Output Blue Bit[4]	-	Open/Unconnected	Hi-Z
44	O	FPB5	Flat Panel Output Blue Bit[5]	-	Open/Unconnected	Hi-Z
45	O	FPB6	Flat Panel Output Blue Bit[6]	-	Open/Unconnected	Hi-Z
46	O	FPB7	Flat Panel Output Blue Bit[7]	-	Open/Unconnected	Hi-Z
Digital Power						
18,37	P	VDD33	Digital I/O Power +3.3V	-	-	Pwr
22,42	P	VDD18	Digital Core Power +1.8V	-	-	Pwr
25,36	P	VSS	Digital Ground	-	-	Pwr

1. Pull-up Resistor 38kΩ(min), 54kΩ(typ), 83kΩ(max)
2. Pull-down Resistor 35kΩ(min), 57kΩ(typ), 107kΩ(max)
3. - means N/A

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3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Min	Typ	Max	Units
V_{DDA18} (Measured to V_{SSA18}) 1.8V[1]	VDDAM	-0.5	-	2.3	V
V_{DD18} (Measured to V_{SS}) 1.8V[1]	VDD18M	-0.5	-	2.3	V
V_{DD33} (Measured to V_{SS}) 3.3V	VDD33M	-0.5	-	4.2	V
Voltage on any Digital Signal Pin[2]	-	V_{SS} –0.5	-	5.5	V
Analog Input Voltage (Supplied by 1.8V)	-	V_{SSA18} – 0.5	-	2.3	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Reflow Soldering	Tpeak	255 +5/-0 (10~30 seconds)			°C

1. V_{DDA18}: AVDAD, AVDPLL
   V_{SSA18}: AVSAD, AVSPLL
   V_{DD33}: VDD33
   V_{DD18}: VDD18
   V_{SS}: VSS
2. This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in can induce destructive latch-up.

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3.2 Characteristics

Parameter	Symbol	Min[1]	Typ	Max[1]	Unit
Supply					
Power Supply — IO 3.3V	V_{DD33}	3.00	3.3	3.6	V
Power Supply — Digital Core 1.8V	V_{DD18}	1.62	1.8	1.98	V
Power Supply — Analog 1.8V	V_{DDA18}	1.62	1.8	1.98	V
Ambient Operating Temperature (TW8819AT)	T_A	-40	-	+105	°C
Ambient Operating Temperature (TW8819)	T_A	-40	-	+85	°C
Analog Supply Current 1.8V (CVBS)	Iaa18	-	19	-	mA
Digital I/O Supply Current 3.3V[2]	Idd33	-	16	-	mA
Digital Core Supply Current[2]	Idd18	-	66	-	mA
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DD33} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} = V_{DD})	I_{IH}	-	-	10	µA
Input Low Current (V_{IN} = V_{SS})	I_{IL}	-	-	–10	µA

Parameter	Symbol	Min[1]	Typ	Max[1]	Unit
Input Capacitance (f = 1MHz, V_{IN} = 2.4V)	C_{IN}	-	5	-	pF
Digital Outputs					
Output High Voltage (I_{OH} = –4mA)	V_{OH}	2.4	-	VDD33	V
Output Low Voltage (I_{OL} = 4mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	μA
Output Capacitance	C_O	-	5	-	pF
Analog Input					
Analog Pin Input Voltage	Vi	-	1	-	V_{P-P}
YIN0~YIN3 Input Range (AC Coupling Required)		0.5	1.0	2.0	V_{P-P}
Analog Pin Input Capacitance	C_A	-	7	-	pF
Horizontal PLL					
Line Frequency (50Hz)	f_{LN}	-	15.625	-	kHz
Line Frequency (60Hz)	f_{LN}	-	15.734	-	kHz
Static Deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
Subcarrier Frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
Subcarrier Frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
Lock In Range	Δf_H	±450	-	-	Hz
Crystal Spec[3]					
Nominal Frequency (Fundamental)		-	27	-	MHz
Deviation		-	-	±50	ppm
Load Capacitance	CL	-	20	-	pF
Series Resistor	RS	-	80	-	Ω

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1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Digital I/O and core power supply current measurement is based on WVGA input (40MHz clock rate) with SMPTE pattern.
3. 2.Crystal Deviation crossover normal operation temperature range.

3.3 Output Timing

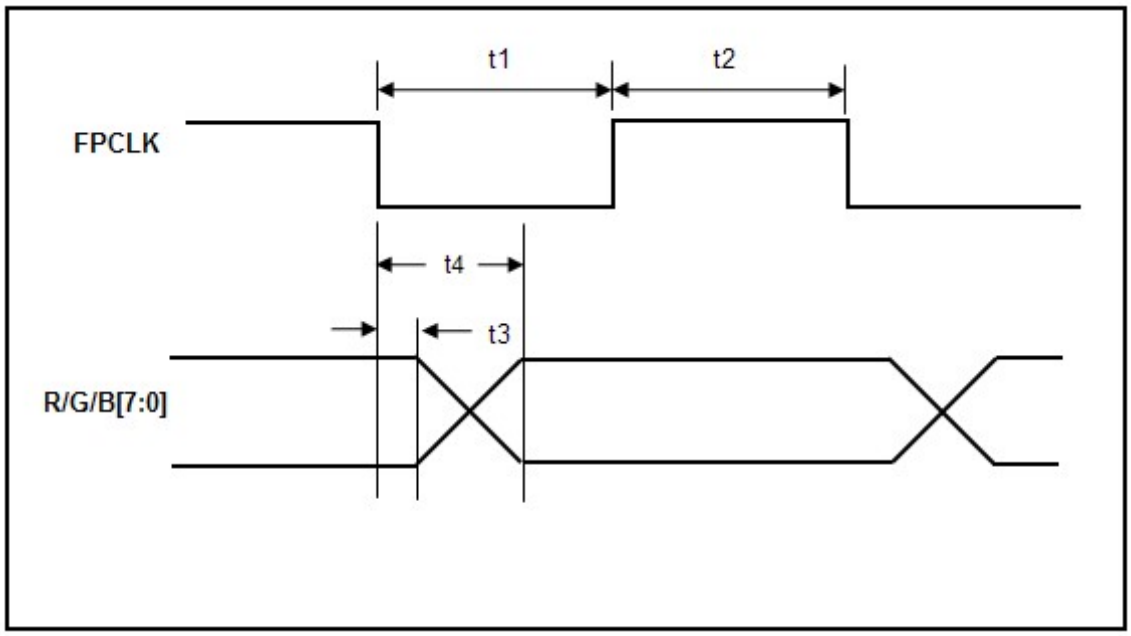


Figure 2. Output Timing

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Duty Cycle FPCLK		FPCLK DIV = 0	40	50	60	%
FPCLK Low Time	t1	FPCLK = 9~80MHz	6.7		66.7	ns
FPCLK High Time	t2	FPCLK = 9~80MHz	6.7		66.7	ns
Output Hold Time	t3	FPCLK Div = 0, Pol = low	6.0			ns
		FPCLK Div = 1, Pol = low	9.0			
		FPCLK Div = 2, Pol = high	21.0			
		FPCLK Div = 3, Pol = low	34.5			
Output Delay Time	t4	FPCLK Div = 0, Pol = low		10.5	14.5	ns
		FPCLK Div = 1, Pol = low		13.5	17.5	
		FPCLK Div = 2, Pol = high		25.5	29.5	
		FPCLK Div = 3, Pol = low		39.5	43.5	

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

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4. Filter Curves

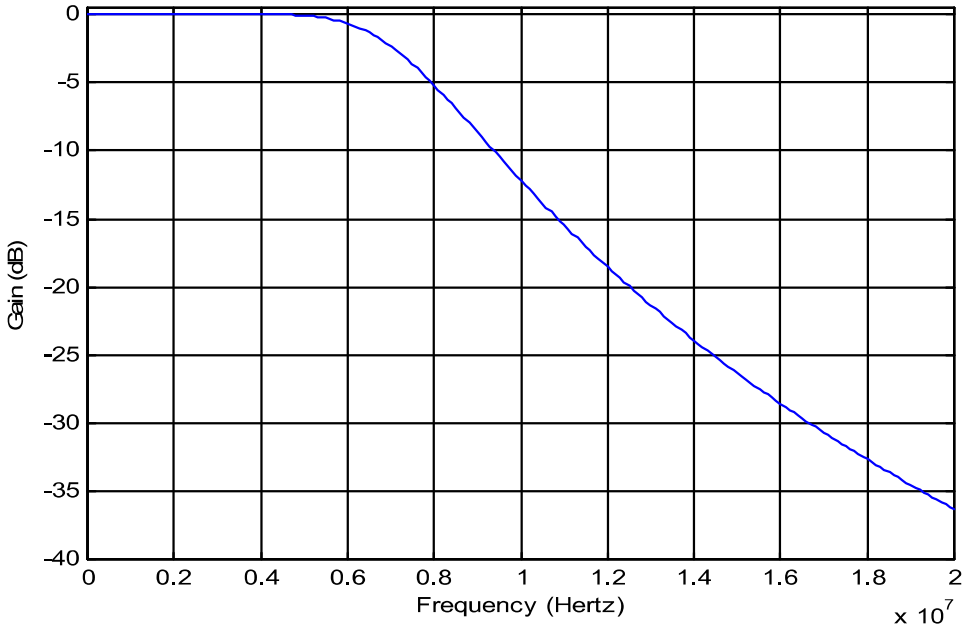


Figure 3. Anti-Alias Filter

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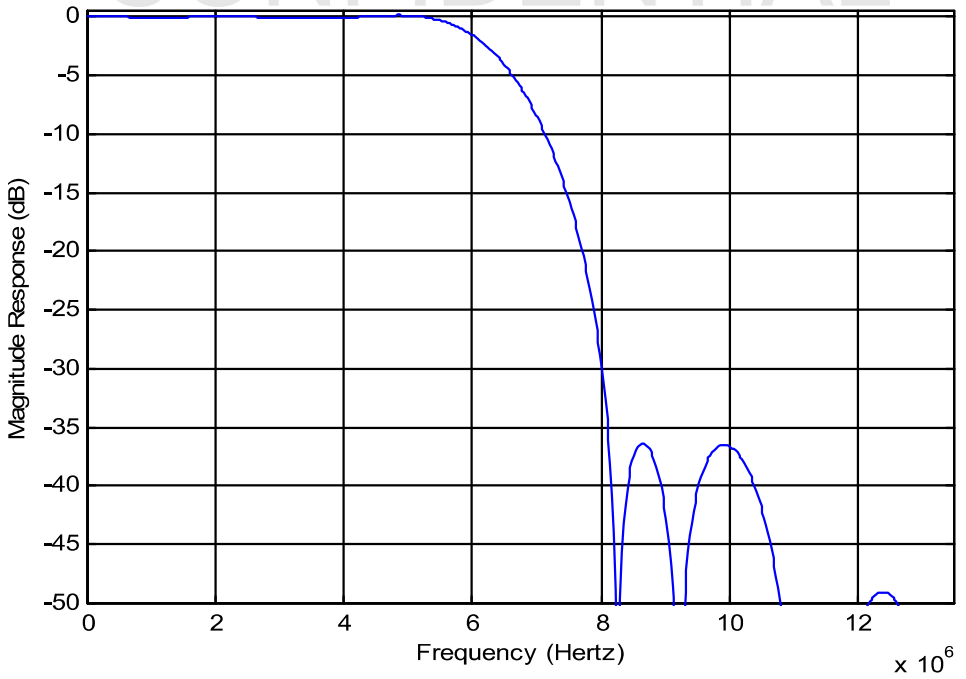


Figure 4. Decimation Filter

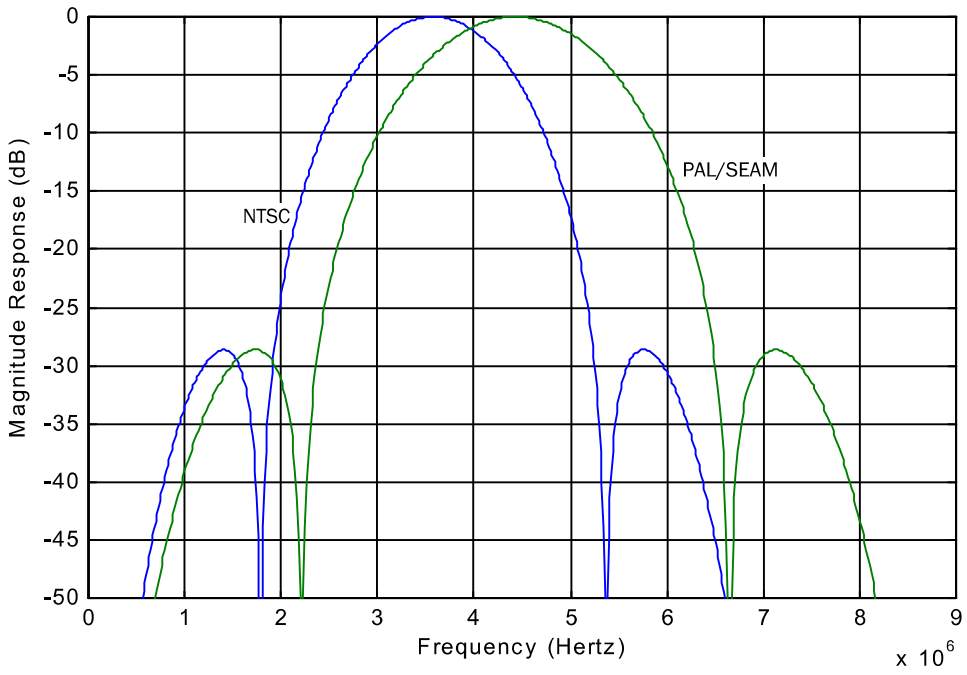
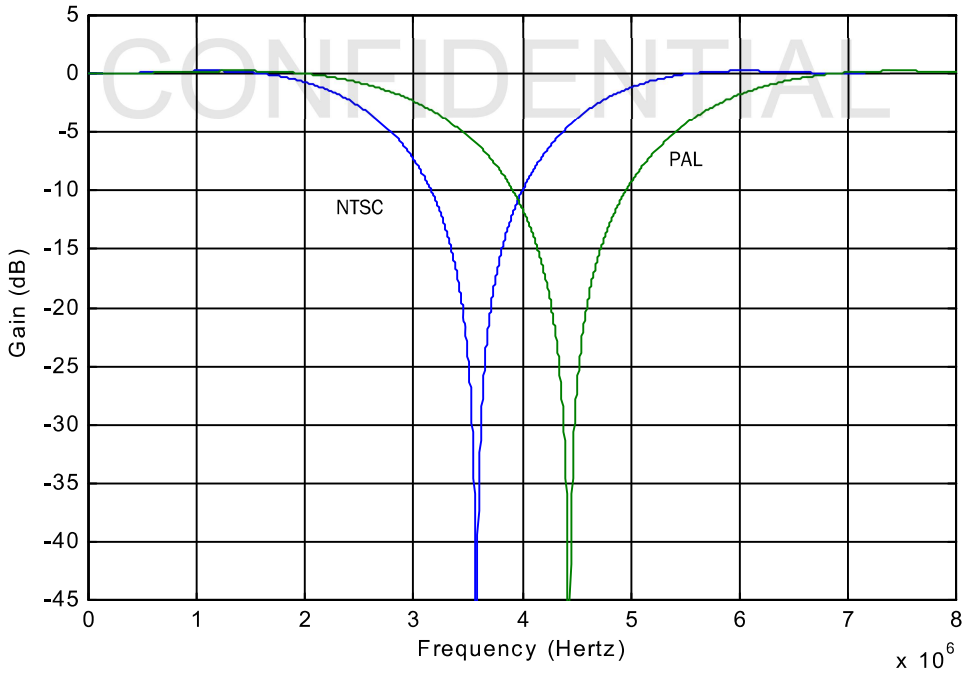


Figure 5. Chroma Band Pass Filter Curves



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Figure 6. Luma Notch Filter Curve for NTSC and PAL

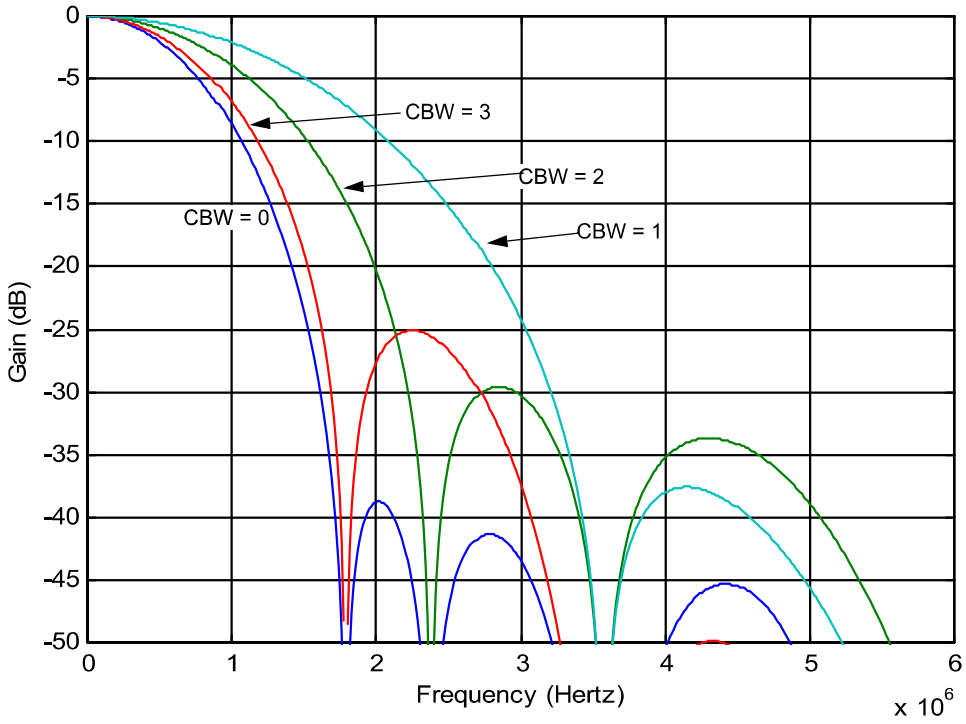


Figure 7. Chrominance Low-Pass Filter Curve

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5. Functional Description

5.1 Overview

Renesas' TW8819 LCD controller is a highly integrated TFT panel controller. It integrates a high quality NTSC/PAL/SECAM 2D comb video decoder, scalers, de-interlacer, a timing controller, and a flexible font based multi-window OSD engine. This unique level of mixed signal integration turns a TFT panel into a flexible display system. It incorporates easy-to-operate features in a single package for automotive rear camera displays and video door phone LCD display systems.

TW8819 contains all the logic required to convert composite analog video signal formats to the signal formats that are necessary to drive various kinds of digital TFT panels. It supports a variety of different panel resolutions based on the scaler and panel clock settings, and has a built-in Timing Controller (TCON) for directly connecting to low cost TCON-less panels.

The integrated analog front-end contains ADCs with clamping circuits and an Automatic Gain Control (AGC) circuit as well as anti-aliasing filters to minimize the need for external components. The built-in video decoder employs Renesas' proprietary 2D Comb filter Y/C separation technologies to produce exceptionally high quality images.

The chip's internal logic synchronizes the panel frame rate to the input source frame rate, and, along with a high quality image-scaling engine that is used to convert the different input resolutions to the appropriate output panel resolution, the TW8819 has a built-in de-interlacer which allows interlaced video to be displayed.

Additional features include a font based, multi-window On Screen Display (OSD) engine, Short to Battery (STB) / Short to Ground (STG) detection function, and a panel bias voltage generator to further simplify the system design. The host control interface is a standard 2-wire serial bus

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5.2 Analog Front-end

The analog front-end converts analog video signals to the required digital format. Each channel contains an automatic clamping circuit, AGC circuit, anti-aliasing filter and high performance ADCs to minimize the number of external components needed. The clamping circuit restores the signal DC level so it can be properly digitized. The analog input source selections are software programmable. Different input sources have different signal conditioning logic to properly convert the signal into correct format for further processing.

5.3 Video Decoder

5.3.1 Sync processor

The decoder sync processor of the video input detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-Video input. The processor contains a digital phase-locked-loop (PLL) and decision logic to achieve reliable sync detection in both stable signals as well as in unstable signals, such as those from VCR fast forward or rewind.

5.3.2 Horizontal Sync Processing

Horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide a jitter free output image. From there, the PLL also provides orthogonal sampling raster for the down-stream processor. It has a very wide lock-in range for tracking any non-standard video signal.

5.3.3 Vertical Sync Processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. A detection window controls the sync determination to provide a more reliable synchronization and simulates the functionality

of a PLL without the complexity of a PLL. The field status is determined at the vertical synchronization time based on the vertical and horizontal sync relationship.

5.3.4 Color Decoding

5.3.4.1 Y/C Separation

The color-decoding block contains the luma / chroma separation engine for composite video signals and multi-standard color demodulation. For NTSC and PAL standard signals, the luma / chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter can be found in the filter curve section.

In the case of comb filter, the decoder separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary adaptive comb filter algorithm. It leads to good Y/C separation with minimal cross luma and cross color at both horizontal and vertical edges. Due to the nature of the line buffer used in the comb filter, there is always a two line processing delay in the output images regardless of what standard or filter option is chosen.

5.3.4.2 Color Demodulation

The color demodulation for NTSC and PAL standards are done by quadrature mixing of the chroma signal to the base band and extracting the chroma components with the low-pass filter. The low-pass filter characteristics can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The SECAM color demodulation process consists of bell filtering, FM demodulation, and de-emphasis filtering. The chroma carrier frequency is identified in the process and used to control the SECAM color demodulation.

The sub-carrier signal used in the color demodulator is generated by a direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard NTSC or PAL signal to be demodulated easily.

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5.3.4.3 Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by transmission loss in the video signal. In the NTSC/PAL standards, the color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals amplitude is then compensated accordingly. The range of ACC control is –6db to +24db.

5.3.4.4 Low Color Detection and Removal

For low color amplitude signals, black and white video, or very noisy signals, the color will be “killed”. The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer operation. This function can be disabled by programming a low threshold value.

5.3.4.5 Automatic Standard Detection

The video decoder has automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency, and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Any of these standards can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

5.3.5 Video Format Support

The integrated video decoder supports all common video formats as shown in Table 1. This needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported

Format	Lines	Fields	f_{SC}	Country
NTSC-M	525	60	3.58MHz	U.S., many others
NTSC-Japan[1]	525	60	3.58MHz	Japan
PAL-B, G, N	625	50	4.43MHz	Many
PAL-D	625	50	4.43MHz	China
PAL-H	625	50	4.43MHz	Belgium
PAL-I	625	50	4.43MHz	Great Britain, others
PAL-M	525	60	3.58MHz	Brazil
PAL-CN	625	50	3.58MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.43MHz	China
NTSC (4.43)	525	60	4.43MHz	Transcoding

1. NTSC-Japan has 0 IRE setup.

5.3.6 Component Processing

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5.3.6.1 Luminance Processing

The video decoder adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The decoder also provides a sharpness control function through a control register. The center frequency of the peaking filter is selectable, and a coring function is provided along with the sharpness control to reduce enhancement to the noise.

5.3.6.2 The Hue and Saturation

When decoding NTSC signals, the decoder can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

5.4 Short Detection

TW8819 provides a Short-to-Battery (STB) and Short-to-Ground (STG) detection capability. The Short Diagnostics module has 2 channels: A & B. Each channel is completely independent and may be assigned to any of the 4 analog input pin, therefore, any of the 4 analog video input pins can be configured to act as a Short Detection input instead of as a video input. Both STB and STG support a 4 step programmable threshold level (2 bits per threshold). The Short to Ground thresholds range from 5/16, 3/16, 2/16, and 1/16 of the 3.3V power supply. The Short to Battery thresholds range from 7/8, 5/8, 3/8, and 1/8 of the 3.3V power supply. A Short event can be detected by either polling registers or by using the interrupt pin.

5.5 Input Image Control

The input cropping control provides a way to program the active display window region for the selected input video or graphics. In normal operation, the first active line starts with the VSYNC signal. This and the vertical active length register setting are used to determine the active vertical window. The active pixel starts HSYNC. This and the horizontal active width register are used to determine the active horizontal window. The vertical window is programmed in line increments. The horizontal window is programmed in single pixel increments for single pixel input mode or two pixel increments for double pixel input mode. If the data qualifier is used, then only qualified pixels will be counted in the window size.

5.6 Image Scaling

The internal high quality image-scaling engine can scale the input image up or down to fit the output panel resolution. The scaler operates in frame-sync mode such that both the input and the output frame rates are always the same. The vertical and horizontal scaling ratio can be adjusted independently in fine granularity. The panel clock frequency selection needs to be coordinated with the scaling ratio as well as the input frequency to avoid internal buffer overrun. The scaler also acts as a de-interlacer to properly de-interlace the input video based on its field nature. The scaler can also be programmed to perform panoramic or water glass mode scaling for flexibility in the display output. In addition, image mirroring can be supported through the scaler by register control.

5.7 Image Enhancement Processing

5.7.1 Black/White Stretch

This feature is used to expand the static range of the input image, which creates a more vivid image impression.

5.8 TFT Panel Support

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TW8819 supports a variety of active matrix TFT panel types and resolutions.

5.8.1 Dithering

The dithering circuit is used to reduce the output dynamic range to fit the panel type. This allows LCD panels with 4, 6 or 8 bits per color per pixel to display up to 16.8 million colors and LCD panels with 3 bits per color per pixel to can display up to 2.1 million colors. This device employs both spatial and frame modulation dithering. When dithering with the least significant 4-bits of input data it uses spatial modulation with 4x4 blocks of pixels. When dithering with the least significant 1 to 3 bits of input data, it uses either spatial modulation with 2x2 pixel blocks, or frame modulation.

5.8.2 Gamma Table

TW8819 has an integrated gamma table for each color output and it is fully programmable through the host bus.

5.8.3 TCON

The integrated Timing controller provides flexible column/row driver control signals to interface with TCON-less panels directly.

5.9 Font On Screen Display

The TW8819 has a built-in OSD controller with programmable RAM font. The OSD display is independent of the input active window setting and the scaling ratio.

The on-chip OSD controller is a character-based controller. The pre-defined character or graphic bit map is stored in the font RAM. TW8819 can store up to 256 single color fonts when character is 12 pixels wide by 18 pixels high. The characters can be displayed on the screen in four user defined window locations of any size from 1 to 512 characters. The spaces between characters are also programmable. There is a limit of 512 characters that may be displayed on screen at one time in all windows combined. The attributes of each window can also be set to

give it a shadow effect or 3-D effect. In addition, the characters can be expanded by a factor of 2, 3, or 4 in vertical or horizontal directions and can have a blinking effect and a border/shadow effect on a character by character basis.

5.9.1 On chip OSD functions

- Font SRAM: Max 256 User Programmable Single Color Font (6912x8 SRAM)
- Character Register SRAM: 512 Location (8-bit Font Address + 10-bit Character Attribute, 512x18 SRAM)
- Characters
  - Character Color: 16 colors
  - Character Background Color: 16 colors
  - Character Blinking: Enable/Disable, 1 Hz Blinking frequency
  - Character Border/Shadow Effect: Enable/Disable
    - (Multi OSD Window Display Case: Chip has a limitation)
  - Character Space: Both H and V programmable by number of pixels
  - Quick Character Change in Window: Programmable Start Address and Buffer Size
  - Programmable OSD Color Palette Support
  - Re-designed OSD Font Supporting Standard Alpha-Numerical Character Set
- Windows
  - Number of Windows: 4 Independent Windows
  - Window Color: 16 colors
  - Window Zoom: 2, 3, 4 times zoom by dot number, H/V separate zooming control
  - Window Position: Programmable
    - H Direction: 1-pixel per step, V Direction: 1-Line per step
  - Window Size: Both H and V programmable by number of characters
  - Window Bordering/Shadowing Effect: 4 Independent Windows Enable/Disable Control
  - Window Alpha Blending Control: 4 Independent Windows Control
  - → 16 Different Color for Alpha Blending support(4-bit control)
  - Window 3-D Effect: 4 Independent Windows Enable/Disable Control
  - Window Border Color: 16 Colors
  - Window Border Width: programmable

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5.9.2 Basic Register Setting Flow Example for Built-in OSD Controller

1. OSD_FONT_SIZE_CONFIGURATION
   a. Select FONT Width to be 12 or 16- 0x300 (Bit[4])
   b. Set FONT Height- 0x350 (Bit[4-0])
   c. Set Sub-Font Total Count- 0x351 (Bit[6-0])
2. OSD_WINDOW_CONFIGURATION setting for **Window#1** (0x310~0x31F)
   Note: **Window#2** (0x320~0x32F), **Window#3** (0x330~0x33F), **Window#4** (0x340~0x34F)

1. OSD Window Disable	0x310, Bit[7]
2. OSD Window Zoom multiplier	0x310, Bit[1-0]: V, Bit[3-2]:H
3. OSD Window H/V border Color	0x31E, Bit[7-4]

4. OSD Window 3-D Effect Top/Bottom Mode Select	0x31B, Bit[6]
5. OSD Window 3-D Effect Level Select	0x31B, Bit[5]
6. OSD Window 3-D Effect Enable/Disable	0x31B, Bit[7]
7. OSD Window H-Start Location (see details in next page)	0x313, Bit[7-0] 0x312, Bit[6-4]
8. OSD Window V-Start Location (see details in next page)	0x314, Bit[7-0] 0x312, Bit[1-0]
9. OSD Window Width	0x316, Bit[5-0]
10. OSD Window Height	0x315, Bit[5-0]
11. OSD Window Border_Line Width	0x318, Bit[4-0]
12. OSD Window Border Color	0x317, Bit[3-0]
13. OSD Window Border_Line Enable	0x318, Bit[7]
14. OSD Window Shadow Width	0x31C, Bit[4-0]
15. OSD Window Shadow Color	0x31B, Bit[3-0]
16. OSD Window Shadow Enable	0x31C, Bit[7]
17. OSD Window H-Space Width (Between Border_line and Characters)	0x319, Bit[6-0]
18. OSD Window V-Space Width (Between Border_line and Characters)	0x31A, Bit[6-0]
19. Character H-Space Width (Between Character and Character)	0x31D, Bit[7-4] 0x31C, Bit[6]
20. Character V-Space Width (Between Character and Character)	0x31D, Bit[3-0] 0x31C, Bit[5]
21. OSD Window Alpha Blending Color Select	0x352, Bit[4-0]
22. OSD Window Alpha Blending Value Control	0x311, Bit[3-0]
23. Window content start address	0x306, Bit[7-0]
24. Repeat 1 – 23	

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3. OSD_COLOR_ATTRIBUTE / FONT setting (OSD RAM)
   a. Enable OSD RAM Access
      i. 0x304 (Bit[0] = 0)
   b. Set Multi-Color Start Address
      i. 0x30B (Bit[7-0]), 0x353 (Bit[7-0]), 0x354 (Bit[7-0])
   c. OSD RAM Address
      i. 0x306 (Bit[7-0])
      ii. The first address is Step_1_32 Window content start address.
   d. OSD RAM Data Port High (Font Address)
      i. 0x307 Data is written to above address automatically.
   e. OSD RAM Data Port Bit17 (Border Effect) and Bit16 (Blinking Effect)
      i. 0x304 Bit[4] and Bit[7] Data are written to above address automatically.
   f. OSD RAM Data Port Low (Color Attribute)
      i. 0x308 Data is written to above address automatically.
   g. Repeat c), d), e), and f)
      i. The address should be increased by one each.
4. COLOR LOOK-UP TABLE setting
   a. Select Color Look-Up Table Write Address
      i. 0x30C (Bit[5:0])
      ii. Bit[5:0]: These 6 bits specify one of the 64 entries in the look-up table. Each entry is a 16-bit RGB color by its content.
      iii. There are 65536 colors available. For single color font, only sixteen of them are accessible by OSD controller at a given time.
   b. Color Look-Up Table control bits setting
      i. 0x30D (High Byte), 0x30E (Low Byte)
      ii. The data of the Look-Up Table is accessed through 0x30D and 0x30E.
   c. Repeat a) and b) to program each entry of the Look-Up Table.
5. FONT_RAM_DATA setting (FONT RAM)
   a. Enable FONT RAM Access
      i. 0x304 (Bit[0] = 1)
   b. FONT RAM Address Setting - 8 bits(h00 – hFF)
      i. 0x309
      ii. h00~hFF: Single Font RAM(256 Programmable Characters)
   c. FONT RAM Data Port
      i. - 0x30A Data is written to above address automatically.
   d. Repeat (4) at 27 times for one FONT RAM Data
      i. The internal address automatically increases by one each.
   e. New FONT RAM Address Setting – 8 bits
      i. 6. Repeat c), d), e)
      ii. The FONT RAM Address should be increased by one each.
      Note: As for the FONT RAM configuration and font bit mapping, see the detailed description

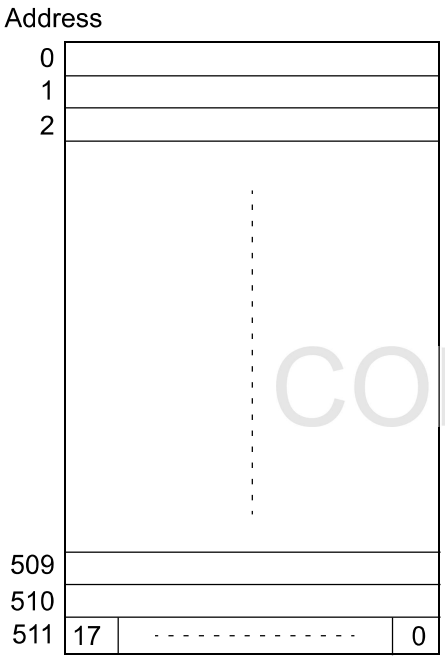
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6. End of OSD setting and Enable OSD
   a. OSD On/Off Enable Control 0: ON, 1: OFF
      i. 0x30C (Bit[6] = 0)
   b. OSD Window Enable
      i. 0x310 (Bit[7] = 1) Window1 Enable

5.9.3 OSD Window Start Location: Built-in OSD controller

- Internal generated OSD DE Position delayed from H-SYNC: 0x303[7:0].
- OSD window H_start location from start of internal OSD DE: 0x312[6:4], 0x313[7:0] increment by 1 pixel at a time.
- OSD window V_start location from start of VACT: 0x312[1:0], 0x314[7:0] increment by 1 line at a time.

5.9.4 OSD_RAM Configuration



The characters can be displayed on the screen in four user defined window locations of any size from 1 to 512 characters. There is a limit of 512 characters that may be displayed on screen at one time in all windows combined.

Example:

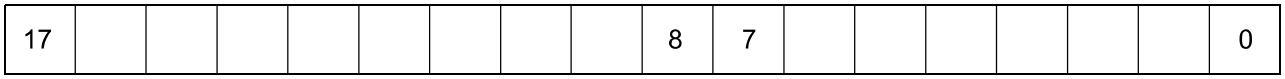
Window #1: Address 0 – 2 (3 characters)

Window #2: Address 3 – 100 (98 characters)

Window #3: Address 201– 354 (154 characters)

Window #4: Address 511 (1 character)

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FONT_ADDRESS (10-bits)

Bit [17]: Border/Shadow

Bit [16]: Blinking

Bits [15 - 8]: FONT Address

FONT_ATTRIBUTE (8-bits)

Bits [7-4]: Character's background color

Bits [3-0]: Character's foreground color

5.9.5 Alpha Blending for OSD Window

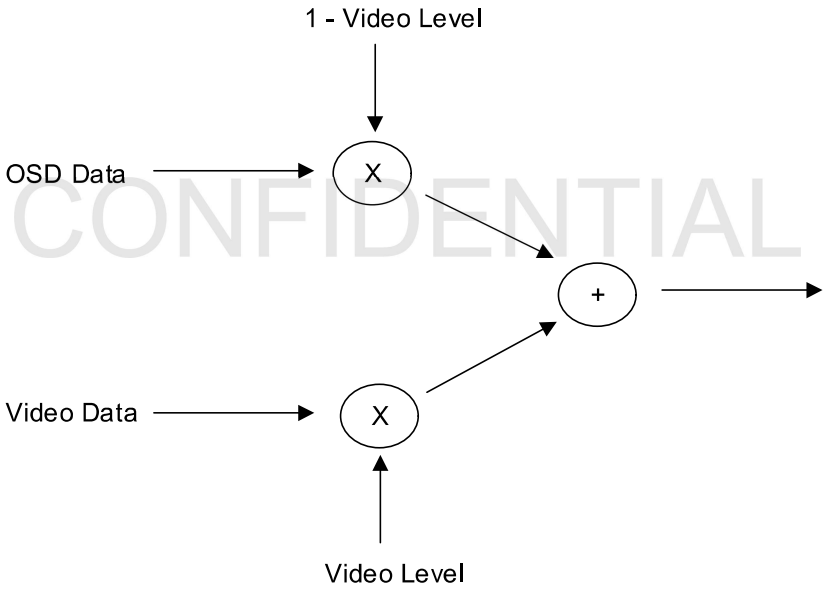
The TW8819 uses Alpha Blending in the OSD's 4 separation windows & 64 separation colors. The upper 32 separation colors are forced to 0. Alpha blending mixes (adds) the video signal and OSD signal at the following specified levels. In other words, alpha blending determines the transparency of each color in the OSD window in relation to video signal. When alpha blending is disabled, only OSD data is displayed in the OSD window.

The alpha blending level selection is 4-bit assigned, and can support 8 different level controls.

The alpha blending level bits are in register 0x311[3:0] for window#1, 0x321[3:0] for window#2, 0x331[3:0] for window#3, 0x341[3:0] for window#4 and alpha blending color selection bits are in register 0x352[4:0] for 32 separation colors.

alpha[3:0]	Video Level
0000	0.00%
0001	12.5
0010	25.0
0011	37.5
0100	50.0
0101	62.5
0110	75.0
0111	87.5
1000	100

5.9.6 Alpha Blending Concept



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5.10 Microcontroller Interface

The host interface is accessed using a 2-wire serial bus interface. It always operates as a slave device.

5.10.0.1 2-Wire Serial Bus Interface

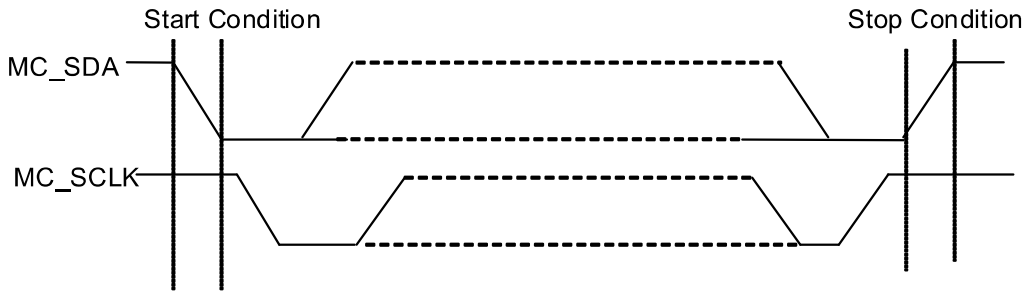


Figure 8. Definition of the Serial Bus Interface Bus Start and Stop

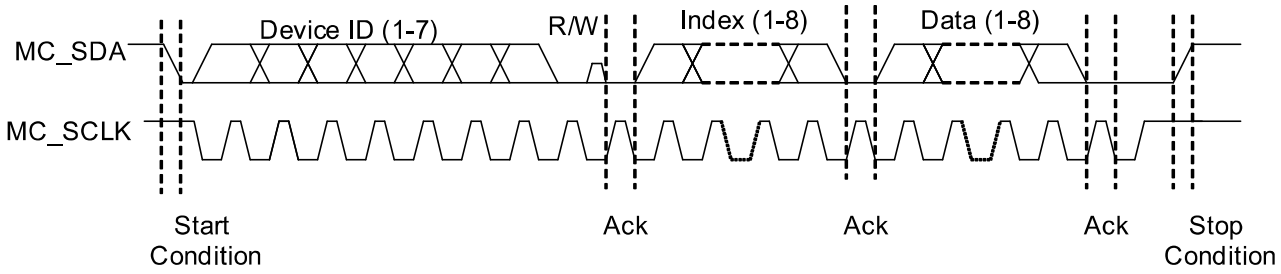


Figure 9. One Complete Register Write Sequence using the Serial Bus Interface

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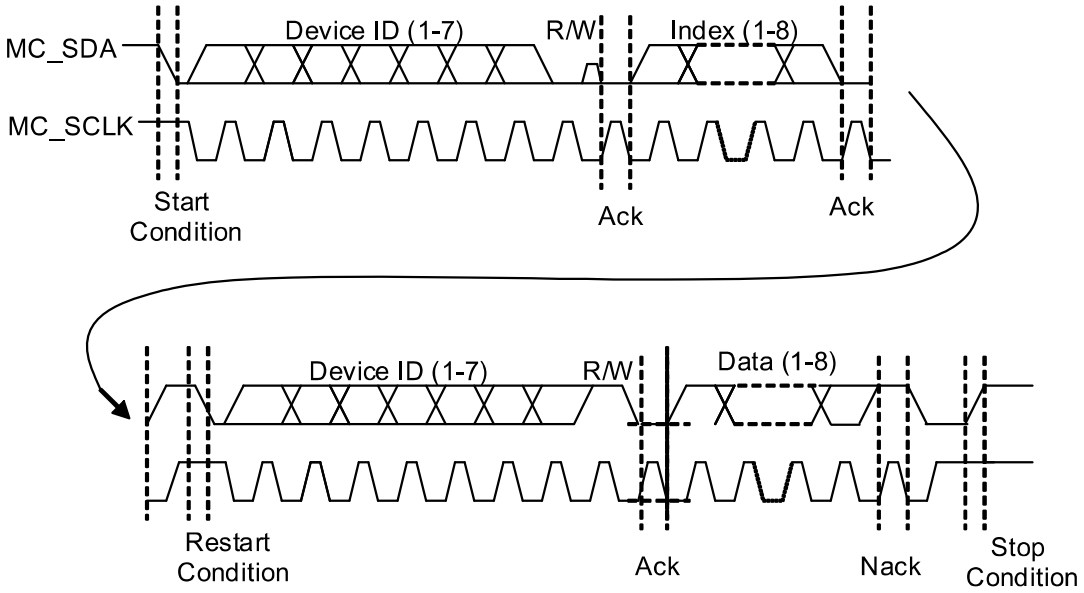


Figure 10. One Complete Register Read Sequence using the Serial Bus Interface

The 2-wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the internal registers. MC_SCLK is the serial clock and MC_SDA is the data line. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling MC_SCLK and MC_SDA low through open drain outputs. In normal operation the master generates all clock pulses, but control of

the MC_SDA line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever MC_SCLK is high.

The device is operated as a bus slave device. The 7-bit device address field is fixed and concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be a read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives MC_SDA from high to low, while MC_SCLK is high, this is defined to be a start condition (see Figure 8). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 9. (The next byte is normally the index to the internal registers and is a write to the device therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the MC_SDA line while holding MC_SCLK low, and wait for an acknowledgment from the slave. If the address matches the device address of a slave, the slave will respond by driving the MC_SDA line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register, the master sends another 8-bits of data, it loads this to the register pointed by the internal index register. The device will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes if they are in ascending sequential order. After each 8-bit transfer the device will acknowledge the receipt of the 8-bits with an acknowledgment pulse. To end all transfers, the host has to issue a stop condition.

Table 2. Serial Bus Interface 7-Bit Slave Address and Read/Write Bit

Serial Bus Interface 7-bit Slave Address							Read/Write Bit
1	0	0	0	1	0	1	1 = Read 0 = Write

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The device read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register (see Figure 10). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the MC_SDA line and acknowledge the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (MC_SDA is left high during a clock pulse) and issue a stop condition.

Table 3. Serial Bus Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time Between STOP and START	t_{BF}	740	-	-	ns
MC_SDA Setup Time	t_{sSDAT}	74	-	-	ns
MC_SDA Hold Time	t_{hSDAT}	50	-	900	ns
Setup Time for START Condition	t_{sSTA}	370	-	-	ns
Setup Time for STOP Condition	t_{sSTOP}	370	-	-	ns
Hold Time for START Condition	t_{hSTA}	74	-	-	ns
Rise Time for MC_SCLK and MC_SDA	t_R	-	-	300	ns

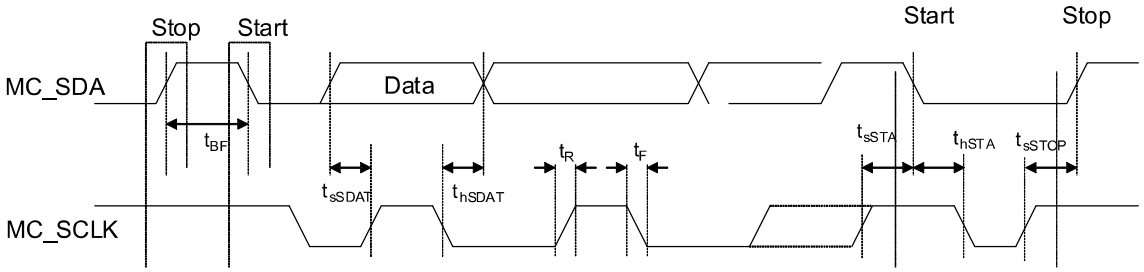


Figure 11. Serial Bus Interface Timing

6. Register Summary

For Register a - means Reserved and for Reset Value a - means unknown.

6.1 General

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
000	ID								19h
001	REV1				REV2				00h
XFF	-				PAGE				00h

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Index (HEX)	7	6	5	4	3	2	1	0	Reset value
002	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0	CAh
003	IMASK								FFh
004	-			STG_STS	STB_STS	VSCHG	HSCHG	VDLOS	00h
006	SRST	-	AINC	TCKDIV	TRUDL	TCLRL	TB	LR	00h
007	SWPPRT	SWPBIT	SHFT2		-	TCONSEL			00h
008	TCKDRV		TRI_FPD	TRI_EN	GPO_SEL				30h
01F	TEST_DEBUG								00h

6.2 GPIO

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
080	-				GPIO_EN				00h
088	-				GPIO_OE				00h
090	-				GPIO_OD				00h
098	-				GPIO_ID				-

6.3 PWM Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0D6	-	TCCLK_O_SEL			-		PWM_EN		00h
0DB	-				FPWM2[9-8]		FPWM1[9-8]		55h
0DC	FPWM1[7-0]								00h
0DD	DPWM1								80h
0DE	FPWM2[7-0]								00h
0DF	DPWM2								80h

6.4 SSPLL

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0F6	-				PCLK_DIV				00
0F7	-	EDGE_SEL_P	CP_X4_SSPLL_P		LP_X4_SSPLL_P		LP_X8_SSPLL_P		16h
0F8	-				FPLL[19:16]				01h
0F9	FPLL[15:8]								20h
0FA	FPLL[7:0]								00h
0FB	FSS[7:0]								40h
0FC	PD_SSPLL	SSD			SSG				B0h
0FD	POST		VCO		-	IPMP			11h

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6.5 Decoder

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
101	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	-	MONO	DET50	-
102	-	FC27	IFSEL		YSEL		-		40h
104	-	CKHY		-					00h
105	-		SAVE	-	FBPY	-	-	DEC_SEL	00h
106	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	-		00h
107	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		12h
108	VDELAY_LO								12h
109	VACTIVE_LO								20h
10A	HDELAY_LO								0Ah
10B	HACTIVE_LO								D0h

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
10C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CCh
110	BRIGHTNESS								00h
111	CONTRAST								5Ch
112	SCURVE	VSF	CTI		SHARPNESS				11h
113	SAT_U								80h
114	SAT_V								80h
115	HUE								00h
117	SHCOR				-	VSHP			80h
118	CTCOR		CCOR		VCOR		CIF		44h
11C	DTSTUS	STDNOW			ATREG	STANDARD			27h
11D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSCM	7Fh
120	CLPEND				CLPST				50h
121	NMGAIN				WPGAIN			AGCGAIN 8	22h
122	AGCGAIN								F0h
123	PEAKWT								D8h
124	CLMPLD	CLMPL							BCh
125	SYNCTD	SYNCT							B8h
126	MISSCNT				HSWIN				44h
127	PCLAMP								38h
128	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00h
129	BSHT			VSHT					00h
12A	CKILLMAX		CKILLMIN						78h
12B	FCOMB	HTL			VTL1	VTL			44h
12C	CKLM	YDLY			HFLT				30h
12D	-	EVCNT	-	SDET	TBC_EN	BYPASS	SYOUT	-	14h
12E	HPM		ACCT		SPM		CBW		A5h
12F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0h
130	SID_FAIL	PID_FAIL	FSC_FAIL	SLOCK_FAIL	CSBAD	MVCSN	CSTRIPE	CTYPE	-
131	VCR	WKAIR	WKAIR1	VSTD	NINTL	-			-
132	HFREF/GVAL/PHERRDO/CGAINO/BAMPO/MINAVG/SYTHRD/SYAMP								-
133	FRM		YNR		CLMD		PSP		05h
134	INDEX		NSEN/SSEN/PSEN/WKTH						1Ah
135	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	00h
136	-				CL_MARGIN	TOGGLE_MODE	CM_CLAMP_MODE		00h

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Index (HEX)	7	6	5	4	3	2	1	0	Reset value
137	-	CM_REJECT	CM_REJECT_CTL		HSPGA_EN	SINGLEENDEDMODE	AAFLPF		06h
138	VCMIN_SEL		ICLAMP_SEL		IB_ADC		IBINBUF_SEL		D9h
139	CM_SLEEP	CM_LO_GM	CM_CURRENT_MODE	CM_INTERNAL_REF	-		SH_SEL_IN		31h
13A	SH_EN_GND	SH_THRESH_GND			SH_EN_BAT	SH_THRESH_BAT			30h
13B	CM_IN_PRECON	CM_MAX_HEAD	CM_BIAS_TRACKS	AN_TEST_EN	-		AN_TEST_SEL		00h

6.6 SCALER / TCON

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
201	MIRROR	PWEN	PXDBL	LNDBL	LNEXT	LNFIX	VALOCK	SMODE	00h
202	-		FOFFSET						20h
203	XSCALE[7-0]								00h
204	XSCALE[15-8]								20h
205	YSCALE[7-0]								00h
206	YSCALE[15:8]								20h
207	PXSCALE[11-4]								80h
208	PXINC[7-0]								10h
209	HDSCALE[7-0]								00h
20A	-	VANOM	-	HFT	HDSCALE[11-8]				04h
20B	HDELAY2								30h
20C	HACTIVE[7-0]								D0h
20D	HACTIVE2[9-8]		CKOSEL	CKP	VSP	HSP	CKDIV		80h
20E	-		LNTT[9-8]		HPADJ[11-8]				00h
20F	HPADJ[7-0]								00h
210	HAPOS								10h
211	HALEN[7-0]								00h
212	PXSCALE[3-0]				HALEN[11-8]				03h
213	HSPOS								10h
214	PXINC[11-8]				HSLEN				20h
215	VAPOS								20h
216	VALEN[7-0]								00h
217	PXINC[11-8]				VALEN{11-8]				03h
218	VSLEN		VSPOS						00h
219	LNTT[7-0]								00h

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Index (HEX)	7	6	5	4	3	2	1	0	Reset value
21A	DM_TOP								00h
21B	DM_BOT								00h
21C	HTOTAL_HI				DEP	PRUN	PLOSS	HTFIX	40h
21D	HTOTAL_LO								00h
21E	-						ABK	FBK	00h
21F	VA_EXT								00h
220	-		VA_POS_HI		VS_POS_HI				00h
221	-		HA_POS_HI		-		HS_POS_HI		00h
240	CSP_WID				CSP_POS				10h
241	CLP_POS								00h
242	CLP_WID								01h
243	-	RCK_POS[10-8]			-	RCK_WID[10-8]			00h
244	RCK_POS[7-0]								00h
245	RCK_WID[7-0]								01h
246	ROE_EXT		ROE_POS[10-8]		-	ROE_WID[10-8]			00h
247	ROE_POS[7-0]								00h
248	ROE_WID[7-0]								01h
249	-		RSP_WID		-	RSP_POS[10-8]			10h
24A	RSP_POS[7-0]								00h
24B	-	CPL_POS[10-8]			CLP_EXT				00h
24C	CPL_POS[7-0]								10h
24D	ROE_MOD		CPL_POL	RSP_POL	ROE_POL	RCK_POL	CLP_POL	CSP_POL	80h
24E	CPL_REF	CPL_SWP	CPL_TGM		ROE_DE	CLP_REF	CLP_DE	CSP_DE	00h

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6.7 Image Adjustment

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
280	-		HUE						20h
281	CONTRAST_R								80h
282	CONTRAST_G								80h
283	CONTRAST_B								80h
284	CONTRAST_Y								80h
285	CONTRAST_Cb								80h
286	CONTRAST_Cr								80h
287	BRIGHTNESS_R								80h
288	BRIGHTNESS_G								80h

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
289	BRIGHTNESS_B								80h
28A	BRIGHTNESS_Y								80h
28B	H_SHARP_COR				H_SHARPNESS				30h
28C	SH_FREQ	-							00h
2B0	-		PEDLVL	WHTLVL	-			BW_EN	10h
2B1	BW_FMIN								40h
2B2	BW_FMAX								40h
2B6	BW_BLACK_TILT								67h
2B7	BW_WHITE_TILT								94h
2BF	TPG_EN	SWAP			PAT_SEL				00h

6.8 Gamma & Dither

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
2E0	GAMAE_R	GAMAE_G	GAMAE_B	-	AUTO_INC		GAMMA_RGB_INDX		00h
2E1	GAMMA_RAM_STARTING_ADDR								00h
2E2	-						GAMMA_RAM_DATA[9:8]		00h
2E3	GAMMA_RAM_DATA[7:0]								00h
2E4	-	DITHER_OPTION			-	DITHER_FORMAT			00h
2F0	RDPOS_X[7:0]								00h
2F1	RDPOS_Y[7:0]								00h
2F2	-	RDPOS_Y[10:8]			RDPOS_X[11:8]				00h
2F3	RDVALUE_R								-
2F4	RDVALUE_G								-
2F5	RDVALUE_B								-
2F8	-	RGB_ORDR	AVRG_EN	AVRG_POL	COL_ODD		COL_EVEN		00h
2F9	DELTA_TYPE	-					DMMY_EN	DMMY_POS	80h

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6.9 FOSD

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
300	-			W16EN	-	MIREN	FONT_SWITCH	OSD_SWITCH	00h
301	-							STATUS	-
302	-		DBGWIN		DBG				06h

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
303	OSD DE Delay								06h
304	BLINK	-	UP256	BSEN	AUTO		CLEAR	FR_RAC_SEL	00h
305	-		FBITEXT	RD_SEL	-				00h
306	I2COSDRAD								00h
307	FDATA								00h
308	FATTRIBUTE								00h
309	I2CFONTRAD								00h
30A	I2CFONTDAT								00h
30B	MADD2								31h
30C	-	OSDON	TABLE_WSEL						00h
30D	TABLE_CON_H								00h
30E	TABLE_CON_L								00h
310	WIN1EN	WIN1MCOLOR	WIN1CVEXT	-	XWIN1ZOOM		YWIN1ZOOM		00h
311	-				WIN1ALPHA				00h
312	-	WIN1HSTR			-		WIN1VSTR		00h
313	WIN1HSTR								00h
314	WIN1VSTR								00h
315	-				WIN1HEIGHT				00h
316	-				WIN1WIDTH				00h
317	-			WIN1REGSTA	WIN1BC				00h
318	WIN1BCEN	-		WIN1BCWID					00h
319	-	WIN1HBWID							00h
31A	-	WIN1VBWID							00h
31B	WIN1BEN	WIN1TEN	WIN1EFF	WIN1BSEL	WIN1SC				00h
31C	WIN1SCEN	WIN1CHSPC	WIN1CVSPC	WIN1SCWID					00h
31D	WIN1CHSPC				WIN1CVSPC				00h
31E	WIN1BGC				WIN1BSC				00h
31F	WIN1REGSTA								00h
320	WIN2EN	WIN2MCOLOR	WIN2CVEXT	-	XWIN2ZOOM		YWIN2ZOOM		00h
321	-				WIN2ALPHA				00h
322	-	WIN2HSTR			-		WIN2VSTR		00h
323	WIN2HSTR								00h
324	WIN2VSTR								00h

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Index (HEX)	7	6	5	4	3	2	1	0	Reset value
325	-		WIN2HEIGHT						00h
326	-		WIN2WIDTH						00h
327	-			WIN2REGSTA	WIN2BC				00h
328	WIN2BCEN	-		WIN2BCWID					00h
329	-	WIN2HBWID							00h
32A	-	WIN2VBWID							00h
32B	WIN2BEN	WIN2TEN	WIN2EFF	WIN2BSEL	WIN2SC				00h
32C	WIN2SCEN	WIN2CHSPC	WIN2CVSPC	WIN2SCWID					00h
32D	WIN2CHSPC				WIN2CVSPC				00h
32E	WIN2BGC				WIN2BSC				00h
32F	WIN2REGSTA								00h
330	WIN3EN	WIN3MCOLOR	WIN3CVEXT	-	XWIN3ZOOM		YWIN3ZOOM		00h
331	-				WIN3ALPHA				00h
332	-	WIN3HSTR			-		WIN3VSTR		00h
333	WIN3HSTR								00h
334	WIN3VSTR								00h
335	-		WIN3HEIGHT						00h
336	-		WIN3WIDTH						00h
337	-			WIN3REGSTA	WIN3BC				00h
338	WIN3BCEN	-		WIN3BCWID					00h
339	-	WIN3HBWID							00h
33A	-	WIN3VBWID							00h
33B	WIN3BEN	WIN3TEN	WIN3EFF	WIN3BSEL	WIN3SC				00h
33C	WIN3SCEN	WIN3CHSPC	WIN3CVSPC	WIN3SCWID					00h
33D	WIN3CHSPC				WIN3CVSPC				00h
33E	WIN3BGC				WIN3BSC				00h
33F	WIN3REGSTA								00h
340	WIN4EN	WIN4MCOLOR	WIN4CVEXT	-	XWIN4ZOOM		YWIN4ZOOM		00h
341	-				WIN4ALPHA				00h
342	-	WIN4HSTR			-		WIN4VSTR		00h
343	WIN4HSTR								00h

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Index (HEX)	7	6	5	4	3	2	1	0	Reset value
344	WIN4VSTR								00h
345	-		WIN4HEIGHT						00h
346	-		WIN4WIDTH						00h
347	-			WIN4REGSTA	WIN4BC				00h
348	WIN4BCEN	-		WIN4BCWID					00h
349	-	WIN4HBWID							00h
34A	-	WIN4VBWID							00h
34B	WIN4BEN	WIN4TEN	WIN4EFF	WIN4BSEL	WIN4SC				00h
34C	WIN4SCEN	WIN4CHSPC	WIN4CVSPC	WIN4SCWID					00h
34D	WIN4CHSPC				WIN4CVSPC				00h
34E	WIN4BGC				WIN4BSC				00h
34F	WIN4REGSTA								00h
350	-			CHEIGHT					12h
351	-	MUL_CON							1Bh
352	-			ALPHA_SEL					00h
353	MADD3								71h
354	MADD4								B1h

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7. TW8819 Register Descriptions

7.1 General

7.1.1 0x000 – Product ID Code Register (ID)

Bit	Function	R/W	Description	Reset
7-0	ID	R	The TW8819 Product ID code	19

7.1.2 0x001 – Product Revision Code Register (ID)

Bit	Function	R/W	Description	Reset
7-0	REV	R	Revision number	00

7.1.3 0x002 – IRQ

Bit	Function	R/W	Description	Reset
7	INT7	R/W	Short-To-Ground interrupt	0
6	INT6	R/W	Vertical display end	0
5	INT5	R/W	Measure status ready	0
4	INT4	R/W	Short-To-Battery interrupt	0
3	INT3	R/W	VSYNC leading edge	0
2	INT2	R/W	Sync Changed	0
1	INT1	R/W	V Loss or H Loss Changed	0
0	INT0	R/W	Reserved	0

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7.1.4 0x003 – IMASK

Bit	Function	R/W	Description	Reset
7-0	IMASK	R/W	Interrupt mask for IRQ status register. An “1” for any bit masks the interrupt for that specific bit.	FF

7.1.5 0x004 – Status

Bit	Function	R/W	Description	Reset
7-5		-	Reserved	-
4	STG_STS	R	Short-To-Ground status	-
3	STB_STS	R	Short-To-Battery status	-
2	VSCHG	R	VYSNC changed	-

Bit	Function	R/W	Description	Reset
1	HSCHG	R	HSYNC changed	-
0	VDLOS	R	Video Loss.	-

7.1.6 0x006 – SRST

Bit	Function	R/W	Description	Reset
7	SRST	W	Chip soft reset by writing “1” to this bit. No register will be affected by this action. It is a self-resetting bit.	0
6	Reserved	R/W	Reserved	0
5	AINC	R/W	2-wire host interface auto index increment control 1 = disable, 0 = enable	0
4	TCKDIV	R/W	TCCLK divider control 1 = ½, 0 = 1	0
3	TRUD	R/W	TRSP output direction. 1 = TRSPT, 0 = TRSPB	0
2	TCLR	R/W	TCSP output direction. 1 = TCSPL, 0 = TCSPR	0
1	TB	R/W	TRUDL pin control. 1 = high, 0 = low	0
0	LR	R/W	TCLRL pin control.1 = high, 0 = low	0

7.1.7 0x007 – Output CTRL I

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Bit	Function	R/W	Description	Reset
7	SWPPRT	R/W	FP data port FPR and FPB swapping control.1 = Swapped, 0 = Normal	0
6	SWPBIT	R/W	MSB and LSB swapped within each individual FP data port. 1 = Swapped, 0 = Normal	0
5-4	SHFT2	R/W	FP data port bit shifting 0 = Normal, 1 = Shift down 2-bit 2 = Shift up 2-bit	0
3	Reserved	R/W	Reserved	0
2-0	TCONSEL	R/W	TCON pin output mode control 0 = TCON 1 = Serial RGB 2 = FP LSB data 3 = Y-ADC data 4 = C-ADC data 5 = V-ADC data 6 = Test	0

7.1.8 0x008 – Output CTRL II

Bit	Function	R/W	Description	Reset
7-6	TCKDRV	R/W	TCCLK drive strength 0 = disable, 1 = 4mA, 2 = 8mA, 3 = 12mA	0
5	TRI_FPD	R/W	1 = Tristate all FP data pins.	1

Bit	Function	R/W	Description	Reset
4	TRI_EN	R/W	1 = Tristate all output pins	1
3-0	GPOSEL	R/W	GPO pin output control 0 = Negative IRQ controlled by IRQ and IMASK registers 1 = Positive IRQ controlled by IRQ and IMASK registers 2 = OSD Debug Signal 3 = N/A 4 = N/A 5 = vact2 6 = TCPOLP 7 = FIELD 8 = N/A 9 = FPDE A = PWM2 output B = 0 C = 1 D = N/A E = N/A F = N/A	0

7.1.9 0x01F – TEST

Bit	Function	R/W	Description	Reset
7-0	TEST	R/W	4 = dtest1 6 = dactest1 7 = dactest2 9 = cctest B = Clamp test	00

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7.2 GPIO

7.2.1 0x080 – GPIO_EN

Bit	Function	R/W	Description	Reset
7-0	GPIO_EN	R/W	GPIO enable (active high)	00

7.2.2 0x088 – GPIO_OE

Bit	Function	R/W	Description	Reset
7-0	GPIO_OE	R/W	GPIO output enable (active high)	00

7.2.3 0x090 – GPIO_OD

Bit	Function	R/W	Description	Reset
7-0	GPIO_OD	R/W	GPIO output data	00

7.2.4 0x098 – GPIO_ID

Bit	Function	R/W	Description	Reset
7-0	GPIO_ID	R	GPIO input data	-

7.3 PWM Control

7.3.1 0x0D6 – TCLK AND PWM CNTL

Bit	Function	R/W	Description	Reset
6-4	TCCLK_O_SEL	R/W	TCCLK output delay control	0
3-2	Reserved	R/W	Reserved	0
1-0	PWM_EN	R/W	PWM Enable.	0

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7.3.2 0x0DB – FPWM_HI

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-2	FPWM2[9-8]	R/W	PWM2 frequency control MSB. A 10-bit register.	1
1-0	FPWM1[9-8]	R/W	PWM1 frequency control MSB. A 10-bit register.	1

7.3.3 0x0DC – FPWM1_LO

Bit	Function	R/W	Description	Reset
7-0	FPWM1[7-0]	R/W	PWM1 frequency control LSB. A 10-bit register. Freq = 27MHz / 256 / FPWM1	80

7.3.4 0x0DD – DPWM1

Bit	Function	R/W	Description	Reset
7-0	DPWM1	R/W	PWM1 Duty cycle control. Duty = (DPWM1 / 256)%	00

7.3.5 0x0DE – FPWM2_LO

Bit	Function	R/W	Description	Reset
7-0	FPWM2[7-0]	R/W	PWM2 frequency control LSB. A 10-bit register. Freq = 27MHz / 256 / FPWM2	80

7.3.6 0x0DF – DPWM2

Bit	Function	R/W	Description	Reset
7-0	DPWM2	R/W	PWM2 Duty cycle control. Duty = (DPWM2 / 256) %	00

7.4 SSPLL

7.4.1 0x0F6 – CLOCK_DIV

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	Reserved	R/W	Reserved	-
3-2	Reserved	R/W	Reserved	-
1-0	PCLK_DIV	R/W	These bits control the PCLK divider as follow 0 = 1, 1 = ½, 2 = 1/4, 3 = 1/8	0

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7.4.2 0x0F7 – SSPLL

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	EDGE_SEL_P	R/W	Edge selection for SSPLL. Factory use only	0
5-4	SSPLL_CP_X4	R/W	SSPLL_X4 CP selection. Factory use only. 1μA / 5μA / 10μA / 15μA	1
3-2	SSPLL_LP_X4	R/W	SSPLL_X4 LP selection among 80K to 20K. Factory use only.	1
1-0	SSPLL_LP_X8	R/W	SSPLL_X8 LP selection among 18K to 0.8K. Factory use only.	2

7.4.3 0x0F8 – SSPLL Control Registers

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	FPLL[19-16]	R/W	Part of a 20-bit register that control the PLL center frequency as below. PLL Oscillation frequency = 108MHz × FPLL / 2 ^ 17 / 2^ POST	1

7.4.4 0x0F9 – SSPLL Frequency Control Registers

Bit	Function	R/W	Description	Reset
7-0	FPLL[15-8]	R/W	Part of a 20-bit register that control the PLL center frequency as below. PLL Oscillation frequency = 108MHz × FPLL / 2 ^ 17 / 2^ POST	20

7.4.5 0x0FA – SSPLL Frequency Control Registers

Bit	Function	R/W	Description	Reset
7-0	FPLL[7-0]	R/W	Part of a 20-bit register that control the PLL center frequency as below. PLL Oscillation frequency = 108MHz × FPLL / 2 ^ 17 / 2^ POST	00

7.4.6 0x0FB – SSPLL Modulation Frequency Control Registers

Bit	Function	R/W	Description	Reset
7-0	FSS[7-0]	R/W	Spread spectrum modulation frequency = 27MHz × FSS / 2^16	40

7.4.7 0x0FC – SSPLL

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Bit	Function	R/W	Description	Reset
7	PD_SSPLL	R/W	PD_SSPLL, PLL power down control 1 = Power Down	1
6-4	SSD	R/W	Spread spectrum gain divider. See SSG description.	3
3-0	SSG	R/W	Spread Spectrum gain control. The frequency deviation is controlled by a center spreading saw tooth waveform. The controlling frequency is determined by FSS and its associated equation. The percentage of peak-to-peak spread or deviation of the center frequency is determined by the following equation. DEVpp = SSG × 2^8 / (FPLL × 2^SSD) × 100%	0

7.4.8 0x0FD – SSPLL Analog Control Registers

Bit	Function	R/W	Description	Reset
7-6	POST	R/W	POST, PLL post divider 0 = 1, 1 = 1/2, 2 = 1/4, 3 = 1/8 Set PLL post divider larger than 1 is recommended	0
5-4	VCO	R/W	VCO Range control. 0 = 13.5 ~ 27MHz, 1 = 27 ~ 54 MHz, 2 = 54 ~ 108MHz, 3 = 108 ~ 216MHz	1

Bit	Function	R/W	Description	Reset
3	OSC_RST	R/W	Reserved	-
2-0	IPMP	R/W	Charge pump currents (μA) 0 = 1.5, 1 = 2.5, 2 = 5, 3 = 10, 4 = 20, 5 = 40, 6 = 80, 7 = 160	1

7.5 Decoder

7.5.1 0x101 – Chip Status Register (CSTATUS)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	-
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	-
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	-
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	-
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	-
2	Reserved	R	Reserved	-
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	-
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	-

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7.5.2 0x102 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	0 = Composite video decoding Others = N/A	0

Bit	Function	R/W	Description	Reset
3-2	YSEL	R/W	These two bits control the input video selection. It selects the composite video source. For single-ended input: 0 = YIN0 1 = YIN1 2 = YIN2 3 = YIN3 For differential input: 0,1 = YIN0±, 2,3 = YIN2±	0
1-0	Reserved	R/W	Reserved	-

7.5.3 0x104 – HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-5	CKHY	R/W	Color killer time constant 0 = Fastest, 3 = Slowest	0
4-0	Reserved	R/W	Reserved	-

7.5.4 0x105 – Reserved

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	0
3	FBPY	R/W	0 = Disable Y channel anti-aliasing filter (RGB mode) 1 = Enable Y channel anti-aliasing filter (decoder mode)	0
2-1	Reserved	R/W	Reserved	-
0	DEC_SEL	R/W	AFE control selection 0 = Reserved, 1 = Decoder input mode	0

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7.5.5 0x106 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	0
5	VREF	R/W	0 = Internal voltage reference. 1 = Internal voltage reference shut down.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = 27MHz clock in power down mode.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1-0	Reserved	R/W	Reserved	-

7.5.6 0x107 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	Bit[9:8] of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	Bit[9:8] of the 10-bit VACTIVE register. Refer to description on Reg0x109 for its shadow register.	1
3-2	HDELAY_HI	R/W	Bit[9:8] of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	Bit[9:8] of the 10-bit HACTIVE register.	2

7.5.7 0x108 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	Bit[7:0] of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

7.5.8 0x109 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	Bit[7:0] of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x11C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

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7.5.9 0x10A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	Bit[7:0] of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0A

7.5.10 0x10B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	Bit[7:0] of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

7.5.11 0x10C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	Combined with VTL[3], there are four different chroma bandwidth can be selected. 1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Color killer sensitivity 1 = Low, 0 = High	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC/PAL 0 = Notch filter	1
2	HCOMP	R/W	1 = Operation mode 1. (recommended) 0 = Operation mode 0.	1
1	YCOMB	R/W	This bit controls the comb operation when there is no color burst. 1 = No comb, 0 = Comb.	0
0	PDLY	R/W	PAL delay line 1 = Disable, 0 = Enable	0

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7.5.12 0x110 – Brightness Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

7.5.13 0x111 – Contrast Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CONTRAST	R/W	These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 100 (64h) yields a gain of 100%. The gain ranges from 0 to 255%	5C

7.5.14 0x112 – Sharpness Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = Low 1 = Center	0
6	VSF	R/W	This bit is for internal used.	0

Bit	Function	R/W	Description	Reset
5-4	CTI	R/W	Color transient improvement level control. There are 4 enhancement levels with 0 being the lowest and 3 being the highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image and 15 being the strongest.	1

7.5.15 0x113 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

7.5.16 0x114 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

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7.5.17 0x115 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue. It is in 2's complement form with 0 being the center value. Positive value results in red hue and negative value gives green hue.	00

7.5.18 0x117 – Vertical Peaking Control I

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	3
3	Reserved	R/W	Reserved	-
2-0	VSHP	R/W	Vertical peaking gain control	0

7.5.19 0x118 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring function for the CTI. It has internal step size of 2.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of the vertical peaking logic. It has an internal step size of 2.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5 dB 2 = 3 dB 3 = 6 dB	0

7.5.20 0x11C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle1 = detection in progress	-
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = N/A	-
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STANDARD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

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7.5.21 0x11D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = Enable recognition of PAL60. 0 = Disable recognition.	1
5	PALN_EN	R/W	1 = Enable recognition of PAL (CN). 0 = Disable recognition.	1
4	PALM_EN	R/W	1 = Enable recognition of PAL (M). 0 = Disable recognition.	1
3	NT44_EN	R/W	1 = Enable recognition of NTSC 4.43. 0 = Disable recognition.	1
2	SEC_EN	R/W	1 = Enable recognition of SECAM. 0 = Disable recognition.	1
1	PALB_EN	R/W	1 = Enable recognition of PAL (B,D,G,H,I). 0 = Disable recognition.	1
0	NTSC_EN	R/W	1 = Enable recognition of NTSC (M). 0 = Disable recognition.	1

7.5.22 0x120 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

7.5.23 0x121 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	4
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN8	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

7.5.24 0x122 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0

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7.5.25 0x123 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold.	D8

7.5.26 0x124– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

7.5.27 0x125– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

7.5.28 0x126 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits set the size for the horizontal sync detection window.	4

7.5.29 0x127 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	38

7.5.30 0x128 – Vertical Control I

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = Fastest 3 = Slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = Fastest 3 = Slowest.	0
3	VMODE	R/W	Vertical detection window. 0 = Vertical count down mode 1 = Search mode	0
2	DETV	R/W	0 = Normal VSYNC logic 1 = recommended for special application only	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 0 = Short 1 = Normal	0

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7.5.31 0x129 – Vertical Control II

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control.	0
4-0	VSHT	R/W	VSYNC output delay control in the increment of half line length	00

7.5.32 0x12A – Color Killer Level Control

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38

7.5.33 0x12B – Comb Filter Control

Bit	Function	R/W	Description	Reset
7	FCOMB	R/W	1 = Non-adaptive comb 0 = Adaptive comb.	0
6-4	HTL	R/W	Adaptive Comb filter control (factory use only).	4
3	VTL1	R/W	Comb filter bandwidth control	0
2-0	VTL	R/W	Adaptive Comb filter threshold control (factory use only)	4

7.5.34 0x12C – Luma Delay and H-Filter Control

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = Normal 1 = Fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HFLT	R/W	Peaking control 2. The peaking curve is controlled by SCURVE bit.	0

7.5.35 0x12D – Miscellaneous Control Register I (MISC1)

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Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	EVCNT	R/W	0 = Normal operation, 1 = Even field counter in special mode	0
5	Reserved	R/W	Reserved	-
4	SDET	R/W	ID detection sensitivity. 1 is recommended.	1
3	TBC_EN	R/W	0 = TBC off, 1 = Internal TBC enabled. (test purpose only)	0
2	BYPASS	R/W	It controls the standard detection and should be set to 1 in normal use.	1
1	SYOUT	R/W	0 = HSYNC is always generated 1 = HSYNC is disabled when video loss is detected	0
0	Reserved	R/W	Reserved	-

7.5.36 0x12E – Miscellaneous Control Register II (MISC2)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 0 = Slow, 1 = Medium, 2 = Auto, 3 = Fast	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC, 1 = Slow, 2 = Medium, 3 = Fast	2

Bit	Function	R/W	Description	Reset
3-2	SPM	R/W	Burst PLL control. 0 = Slowest, 1 = Slow, 2 = Fast, 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. 0 = Low, 1 = Medium, 2 = High, 3 = NA	1

7.5.37 0x12F – Miscellaneous Control III (MISC3)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disable	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disable	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disable	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disable	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disable	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color 0 = Black	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disable	0

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7.5.38 0x131 – Chip Status II (CSTATUS2)

Bit	Function	R/W	Description	Reset
7	VCR	R	VCR signal indicator	-
6	WKAIR	R	Weak signal indicator 2	-
5	WKAIR1	R	Weak signal indicator1	-
4	VSTD	R	Standard line per field indicator	-
3	NINTL	R	Non-interlaced signal indicator	-
2-0	Reserved	-	Reserved	-

7.5.39 0x132 – H Monitor (HFREF)

Bit	Function	R/W	Description	Reset
7-0	HFREF, etc.	R	Horizontal line frequency indicator HREF[9:2] / GVAL[8:1] / PHERRDO / CGAINO / BAMPO / MINAVG / SYTHRD / SYAMP	-

7.5.40 0x133 – Clamp Mode (CLMD)

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode. 0 = Auto mode, 1 = Auto mode, 2 = 60 Hz, 3 = 50 Hz	0
5-4	YNR	R/W	Y HF Noise Reduction. 0 = None, 1 = Smallest, 2 = Small, 3 = Medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = NA	1
1-0	PSP	R/W	Slice level. 0 = Low 1 = Medium 2 = High 3 = NA	1

7.5.41 0x134 – ID Detection Control (NSEN/SSEN/PSEN/WKTH)

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Bit	Function	R/W	Description	Reset
7-6	INDEX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A/ 20/ 1C/ 2A

7.5.42 0x135 – Clamp Control (CLCNTL)

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debug use.	0
6	YCLEN	R/W	0 = Enable Y channel clamp, 1 = Disable	0
5	CCLEN	R/W	0 = Enable C channel clamp, 1 = Disable	0
4	VCLEN	R/W	0 = Enable V channel clamp, 1 = Disable	0
3	GTEST	R/W	0 = Normal operation, 1 = Test	0
2	VLPF	R/W	Sync filter bandwidth control	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

7.5.43 0x136 – Differential Clamping Control 1

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3	CL_MARGIN	R/W	Adjusts the timing spacing between the two non-overlapping clocks that operate in the toggle-mode. 0 = 3-27MHz clock periods 1 = 6-27MHz clock periods	0
2	TOGGLE_MODE	R/W	Enables the toggle-mode which eliminates systematic offsets between the two output phases of the Common-Mode Restore Amp by swapping them from line to line. 0 = Disable toggle mode 1 = Enable	0
1-0	CM_CLAMP_MODE	R/W	Selects between 4 modes of operation for the Common-Mode-Restore: table needed derived from verilog module 00 = Clamp counter 01 = Blanking period 10 = Burst period 11 = Back-porch counter	0

7.5.44 0x137 – Differential Clamping Control 2

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	CM_REJECT	R/W	Enable common-mode restore inside the AFE 0 = Disable 1 = Enable	0
5-4	CM_REJECT_CTL	R/W	Common-mode reject control	0
3	HSPGA_EN	R/W	PGA control 0 = Low-speed operation 1 = High-speed operation	0
2	SINGLEENDEDMODE	R/W	1 = Input muxes are in single-end mode and common-mode restore amp is disabled. 0 = Input muxes operate in differential mode and common-mode restore amp is allowed to enable.	1
1-0	AAFLPF	R/W	Anti-aliasing filter control 00 = 0dB at 9MHz 01 = -3.4dB at 10MHz 10 = 0dB at 7MHz 11 = -3.4dB at 8MHz	2

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7.5.45 0x138 – Differential Clamping Control 3

Bit	Function	R/W	Description	Reset
7-6	VCMIN_SEL	R/W	Input common mode voltage control from 400mV to 1.02V in 20mV increment 00 = 700mV (RGB default) 01 = 800mV 10 = 900mV (Decoder default) 11 = 1000mV	3
5-4	ICLAMP_SEL	R/W	Clamp current control from 5μA to 80μA in 5μA increment 00 = 10μA 01 = 20μA (default for RGB, and decoder) 10 = 30μA 11 = 40μA	1
3-2	IB_ADC	R/W	ADC bias current selection 00 = 10μA (Decoder default) 01 = 15μA 10 = 20μA (RGB default) 11 = 25μA	2
1-0	IBINBUF_SEL	R/W	Bias current control for AFE input buffers, and the high speed 9-bit PGA 00 = 20uA (Decoder default) 01 = 40μA 10 = 60μA (RGB default) 11 = 80μA	1

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7.5.46 0x139 – Differential Clamping Control 4

Bit	Function	R/W	Description	Reset
7	CM_SLEEP	R/W	The common mode restore amp 0 = Disable 1 = Enable	0
6	CM_LO_GM	R/W	Reduces the strength of the common-mode restore clamp	0
5	CM_CURRENT_MODE	R/W	Selects between current mode (active amplifier) and voltage mode (passive resistor network) for the common-mode-restore function 0 = passive resistor network for the common-mode-restore function 1 = active amplifier for common mode restore	1
4	CM_INTERNAL_REF	R/W	Select common mode reference 0 = it uses the existing ground based programmable reference to set common mode 1 = adjusts the common mode using a mid-supply based reverence internal to the common-mode-amp	1
3-2	Reserved	R/W	Reserved	-
1-0	SH_SEL_IN	R/W	Selects which one of four input pins becomes attached to the short diagnostic comparators	0

7.5.47 0x13A – Short Detection Control

Bit	Function	R/W	Description	Reset
7	SH_EN_GND	R/W	Enables Short-to-Ground Detection 0 = Disable 1 = Enable	0
6-4	SH_THRESH_GND	R/W	Selects threshold for Short-to-Ground Detection. 0 = AVDAD×(1/16) 1 = AVDAD×(2/16) 2 = AVDAD×(3/16) 3 = AVDAD×(4/16) 4 = AVDAD×(5/16) 5 = AVDAD×(6/16) 6 = AVDAD×(7/16) 7 = AVDAD×(8/16)	3
3	SH_EN_BAT	R/W	Enables Short-to-Battery Detection (Battery or High-Side Supply) 0 = Disable 1 = Enable	0
2-0	SH_THRESH_BAT	R/W	Selects threshold for Short-to-Battery Detection. 0 = AVDAD×(1/16) 1 = AVDAD×(3/16) 2 = AVDAD×(5/16) 3 = AVDAD×(7/16) 4 = AVDAD×(9/16) 5 = AVDAD×(11/16) 6 = AVDAD×(13/16) 7 = AVDAD×(15/16)	0

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7.5.48 0x13B – Differential Clamping Control 5

Bit	Function	R/W	Description	Reset
7	CM_IN_PRECON	R/W	Enables Common-Mode Input Preconditioning. Forces unused (unselected) inputs to ½ supply 0 = Disable 1 = Enable	0
6	CM_MAX_HEAD	R/W	Common-Mode Maximum Headroom Mode 0 = Disable 1 = Enable	0
5	CM_BIAS_TRACKS	R/W	Common-Mode Restore Amp-Bias Current tracks the Bias Current settings for the Differential-Digital/DC Restore	0
4	AN_TEST_EN	R/W	Enables the Analog Test Mode 0 = Disable 1 = Enable	0

Bit	Function	R/W	Description	Reset
2-3	Reserved	R/W	Reserved	-
1-0	AN_TEST_SEL	R/W	Select which analog differential signals from inside the AFE are presented to analog input pins 2 and 3 00 = Tests outputs of input buffers 01 = Tests analog diff output of PGA Programmable Gain Amp 10 = Tests the input multiplexer, but only for inputs 0,1 11 = Pin2 looks at VinCModeRef Pin3 looks at The CmIsClamping, common-mode activity signal	0

7.6 Scaler

7.6.1 0x201 – General Scaler Control

Bit	Function	R/W	Description	Reset
7	MIRROR	R/W	1 = Enable horizontal mirror output 0 = Normal output	0
6	PWEN	R/W	1 = Enable Panoramic / water glass display 0 = Normal display	0
5	PXDBL	R/W	1 = Enable pixel doubling function. 0 = Disabled	0
4	LNDBL	R/W	1 = Enable line doubling function 0 = Disabled	0
3	LNEXT	R/W	Reserved for factory use.	0
2	LNFIX	R/W	1 = Fix the scaler output line number defined by register LNTT. 0 = Output line number determined by scaling factor.	0
1	VALOCK	R/W	1 = Output active start position tracks the input active position 0 = Output active start position defined by VA_POS register.	0
0	SMODE	R/W	Scaler mode selection 1 = Scaling from the start of the field / frame 0 = Scaling from the start of the input active	0

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7.6.2 0x202– Scaling Offset Control

Bit	Function	R/W	Description	Reset
7-6	RDLY	R/W	Scaling buffer read out delay in lines	0
5-0	FOFFSET	R/W	Scaling initial offset control	20

7.6.3 0x203– XSCALE_LO

Bit	Function	R/W	Description	Reset
7-0	XSCALE_LO	R/W	Up scaling ratio control in X-direction. A 16-bit register. The scaling ratio is defined as 2000h / XSCALE.	00

7.6.4 0x204– XSCALE_HI

Bit	Function	R/W	Description	Reset
7-0	XSCALE_HI	R/W	Up scaling ratio control in X-direction. A 16-bit register. The scaling ratio is defined as 2000h / XSCALE	20

7.6.5 0x205– YSCALE_LO

Bit	Function	R/W	Description	Reset
7-0	YSCALE_LO	R/W	Up / down scaling ratio control in Y-direction. A 16-bit register. The scaling ratio is defined as 2000h / YSCALE.	00

7.6.6 0x206– YSCALE_HI

Bit	Function	R/W	Description	Reset
7-0	YSCALE_HI	R/W	Up / down scaling ratio control in Y-direction. A 16-bit register. The scaling ratio is defined as 2000h / YSCALE	20

7.6.7 0x207– PXSCALE

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Bit	Function	R/W	Description	Reset
7-0	PXSCALE	R/W	Initial Scaling value for the Panoramic / water glass display in increment of 4. MSB 8-bit of a 12-bit register.	80

7.6.8 0x208– PXINC

Bit	Function	R/W	Description	Reset
7-0	PXINC[7-0]	R/W	Increment step value for the Panoramic / water glass display. The step is in 2's complement format for both positive and negative increment.	10

7.6.9 0x209– HDSCALE_LO

Bit	Function	R/W	Description	Reset
7-0	HDSCALE_LO	R/W	Down scaling control in X-direction. A 12-bit register. The down scaling ratio is defined as 400h / HDSCALE	00

7.6.10 0x20A– HDSCALE_HI

Bit	Function	R/W	Description	Reset
7	VAEXT	R/W	Special VA extension function. 1 = Enable DE on line, 10 = Off	0
6	VANOM	R/W	VA control. Factory use only.	0
5	Reserved	R/W	Reserved	-
4	HFT	R/W	Down scaler filter control. 1 = On, 0 = Off	0
3-0	HDSCALE_HI	R/W	Down scaling control in X-direction. A 12-bit register. The down scaling ratio is defined as 400h / HDSCALE	4

7.6.11 0x20B– HDELAY2

Bit	Function	R/W	Description	Reset
7-0	HDELAY2	R/W	Scaler buffer data output delay in number of pixels in relation to the H sync.	30

7.6.12 0x20C– HACTIVE2_LO

Bit	Function	R/W	Description	Reset
7-0	HACTIVE2	R/W	Scaler data output length in number of pixels. A 11-bit register.	D0

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7.6.13 0x20D– LNTT_HI

Bit	Function	R/W	Description	Reset
7-6	LNTT_HI	R/W	It controls the scaler total output lines when LNFIX=1. It is used in special case. A 10-bit register.	0
5	CKOSEL	R/W	Pixel clock output selection. 0 = Divided clock specified by CKDIV, 1 = Undivided clock	0
4	CKP	R/W	Pixel clock polarity control. 0 = No inversion.	0
3	VSP	R/W	FPVS output polarity control. 0 = No inversion.	0
2	HSP	R/W	FPHS output polarity control. 0 = No inversion.	0
1-0	CKDIV	R/W	Pixel clock output frequency division control. 0 = 1, 1 = ½, 2 = 1/3, 3 = ¼	0

7.6.14 0x20E– HPADJ_HI

Bit	Function	R/W	Description	Reset
6-4	HACTIVE2_HI	R/W	Scaler data output length in number of pixels. A 11-bit register.	2
3-0	HPADJ_HI	R/W	Blanking H period adjustment. A 12-bit 2's complement register.	0

7.6.15 0x20F– HPADJ_LO

Bit	Function	R/W	Description	Reset
7-6	HPADJ_LO	R/W	Blanking H period adjustment. A 12-bit 2's complement register	00

7.6.16 0x210– HA_POS

Bit	Function	R/W	Description	Reset
7-0	HA_POS	R/W	Output DE position control relative to the internal reference in number of output clock	10

7.6.17 0x211– HA_LEN_LO

Bit	Function	R/W	Description	Reset
7-0	HALEN_LO	R/W	Output DE length control in number of the output clocks. A 12-bit register	00

7.6.18 0x212– HA_LEN_HI

Bit	Function	R/W	Description	Reset
7-4	PXSCALE	R/W	Initial X scaling factor. LSB 4-bit of a 12-bit register.	0
3-0	HALEN_HI	R/W	Output DE length control in number of the output clocks. A 12-bit register	3

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7.6.19 0x213– HS_POS

Bit	Function	R/W	Description	Reset
7-0	HS_POS	R/W	Output HSYNC position relative to internal reference in number of output clocks.	10

7.6.20 0x214– HS_LEN

Bit	Function	R/W	Description	Reset
7-0	HS_LEN	R/W	Output HSYNC length in number of output clocks.	20

7.6.21 0x215– VA_POS

Bit	Function	R/W	Description	Reset
7-0	VA_POS	R/W	Output DE position control relative to the internal reference in number of output lines	20

7.6.22 0x216– VA_LEN_LO

Bit	Function	R/W	Description	Reset
7-0	VALEN_LO	R/W	Output DE control in number of the output lines. A 12-bit register	00

7.6.23 0x217– VA_LEN_HI

Bit	Function	R/W	Description	Reset
7-4	PXINC[11-8]	R/W	MSB 4-bit of a 12-bit register that defines the scaling increment for both panorama and waterglass display. It works with PXSCALE.	0
3-0	VALEN_HI	R/W	Output DE control in number of the output lines. A 12-bit register	3

7.6.24 0x218– VS_LEN_POS

Bit	Function	R/W	Description	Reset
7-6	VS_LEN	R/W	Output V sync length in number of output lines.	0
5-0	VS_POS	R/W	Output V sync position relative to internal reference in number of output lines.	0

7.6.25 0x219– LNTT_LO

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Bit	Function	R/W	Description	Reset
7-0	LNTT_LO	R/W	It controls the scaler total output lines when LNFIX=1. It is used in special case. A 10-bit register.	00

7.6.26 0x21A– DM_TOP

Bit	Function	R/W	Description	Reset
7-0	DM_TOP	R/W	These bits control the number of data masked lines (black lines) from the top of DE	00

7.6.27 0x21B– DM_BOT

Bit	Function	R/W	Description	Reset
7-0	DM_BOT	R/W	These bits control the number of data masked lines from the end of DE.	00

7.6.28 0x21C– PANEL_FRUN

Bit	Function	R/W	Description	Reset
7-4	HTOTAL_HI	R/W	MSB of a 12-bit register. It controls the panel free run H length.	4
3	DEP	R/W	DE polarity control. 1 = Inversion, 0 = No inversion.	0
2	PRUN	R/W	Panel free run control. 1 = Free run with HTOTAL and LNTT, 0 = Disabled	0
1	PLOSS	R/W	Panel free run on the condition of input loss. 1 = Enabled, 0 = Disabled	0
0	HTFIX	R/W	Panel output line length control. 1 = Fixed by HTOTAL, 0 = Auto adjusted.	0

7.6.29 0x21D– HTOTAL_LO

Bit	Function	R/W	Description	Reset
7-0	HTOTAL_LO	R/W	LSB of a 12-bit register. It controls the panel free run H length.	00

7.6.30 0x21E– BLANK

Bit	Function	R/W	Description	Reset
7-2	Reserved	R/W	Reserved	-
1	ABK	R/W	1 = enable screen blanking when no input only 0 = off	0
0	FBK	R/W	1 = enable screen blanking 0 = off	0

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7.6.31 0x21F– VA_EXT

Bit	Function	R/W	Description	Reset
7-2	VA_EXT	R/W	Number of VA extension lines, when 0x20A[7] is set.	00

7.6.32 0x220– V_POS_HI

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	VA_POS_HI	R/W	MSB of a 10-bit register. Output DE position control relative to the internal reference in number of output lines	0
3-0	VS_POS_HI	R/W	MSB of a 9-bit register. Output V sync position relative to internal reference in number of output lines.	0

7.6.33 0x221– H_POS_HI

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	HA_POS_HI	R/W	MSB of a 10-bit register. Output DE position control relative to the internal reference in number of output clocks.	0
1-0	HS_POS_HI	R/W	MSB of a 10-bit register. Output H sync position relative to internal reference in number of output clocks.	0

7.7 TCON

7.7.1 0x240– CSP Control

Bit	Function	R/W	Description	Reset
7-4	CSPWID	R/W	Column Start pulse width control in number of output clocks.	1
3-0	CSPPOS	R/W	Column start pulse position control relative to the leading edge of the DE	0

7.7.2 0x241– CLP Position

Bit	Function	R/W	Description	Reset
7-0	CLPPOS	R/W	Column latch pulse position control relative to either the trailing edge of DE of the start of line reference depending on CLPREF	00

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7.7.3 0x242– CLP Width

Bit	Function	R/W	Description	Reset
7-0	CLPWID	R/W	Column latch pulse width control in number of output clocks.	01

7.7.4 0x243– RCK Control HI

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	RCKPOS_HI	R/W	RCK position control relative to the leading edge of DE in number of output clocks. A 11-bit register.	0
3	Reserved	R/W	Reserved	-
2-0	RCKWID_HI	R/W	RCK width control in number of output clocks. A 11-bit register.	0

7.7.5 0x244– RCK Position LO

Bit	Function	R/W	Description	Reset
7-0	RCKPOS_LO	R/W	RCK position control relative to the leading edge of DE in number of output clocks. A 11-bit register.	00

7.7.6 0x245– RCK Width LO

Bit	Function	R/W	Description	Reset
7-0	RCKWID_LO	R/W	RCK width control in number of output clocks. A 11-bit register.	01

7.7.7 0x246– ROE Control HI

Bit	Function	R/W	Description	Reset
7-6	ROE_EXT	R/W	Row driver enable pulse extension control.	0
5-4	ROEPOS_HI	R/W	ROE position control relative to the leading edge of DE in number of output clocks. A 10-bit register.	0
3	Reserved	R/W	Reserved	-
2-0	ROEWID_HI	R/W	ROE width control in number of output clocks. A 11-bit register.	0

7.7.8 0x247– ROE Position LO

Bit	Function	R/W	Description	Reset
7-0	ROEPOS_LO	R/W	ROE position control relative to the leading edge of DE in number of output clocks. A 10-bit register.	00

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7.7.9 0x248– ROE Width LO

Bit	Function	R/W	Description	Reset
7-0	ROEWID_LO	R/W	ROE width control in number of output clocks. A 11-bit register.	01

7.7.10 0x249– RSP Control

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	RSPWID	R/W	Row Start pulse width control in number of output lines.	1
3	Reserved	R/W	Reserved	-
2-0	RSPPOS_HI	R/W	Row start pulse position control relative to the first output DE line. An 11-bit register in 2's complement form.	0

7.7.11 0x24A– RSP Position Control

Bit	Function	R/W	Description	Reset
7-0	RSP_POS_LO	R/W	Row start pulse position control relative to the first output DE line. An 11-bit register in 2's complement format.	00

7.7.12 0x24B– CPL Position Control

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	CPLPOS_HI	R/W	Polarity pulse change position relative to the reference controlled by CPLREF in number of output clocks. This is a 11-bit register.	0
3-0	CPLEXT	R/W	Polarity pulse extension in number of lines. This is effective in polarity toggle mode 2 only.	0

7.7.13 0x24C– CPL Position Control LO

Bit	Function	R/W	Description	Reset
7-0	CPLPOS_LO	R/W	Polarity pulse change position relative to the reference controlled by CPLREF in number of output clocks. This is a 11-bit register.	10

7.7.14 0x24D– TCON Control I

Bit	Function	R/W	Description	Reset
7-6	ROEMOD	R/W	ROE output mode control. 0 = Always low 1 = Always high 2 = Toggle	2
5	CPLPOL	R/W	Polarity pulse polarity control. 0 = No inversion	0
4	RSPPOL	R/W	Row start pulse polarity control. 0 = High active	0
3	ROEPOL	R/W	Row output enable pulse polarity control. 0 = High active	0
2	RCKPOL	R/W	Rck output polarity control. 0 = High active	0
1	CLPPOL	R/W	Column driver latch pulse polarity control. 0 = High active	0
0	CSPPOL	R/W	Column driver start pulse polarity control. 0 = High active	0

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7.7.15 0x24E– TCON Control II

Bit	Function	R/W	Description	Reset
7	CPLREF	R/W	Polarity pulse change reference point control. It is to be used with CPLPOS register. 0 = Reference to internal line sync 1 = Reference to trailing edge of DE	0
6	CPLSWP	R/W	Positive and negative polarity pulse swap. 0 = no swap	0
5-4	CPLTGM	R/W	Polarity pulses toggle mode control. 0 = Frame inversion 1 = No frame inversion 2 = Frame inversion in blanking period only	0
3	ROEDE	R/W	Row driver output enable control 0 = Output in active line 1 = Output in every line	0

Bit	Function	R/W	Description	Reset
2	CLPREF	R/W	Column driver latch pulse position reference control. 0 = Leading edge of DE 1 = Trailing edge of DE	0
1	CLPDE	R/W	Column driver latch pulse control. 0 = Only output in active line 1 = Output in every line	0
0	CSPDE	R/W	Column driver start pulse control. 0 = Only output in active line 1 = Output in every line.	0

7.8 Image Adjustment

7.8.1 0x280 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	HUE	R/W	Hue Adjustment. These bits control the color hue. The range is +45 degrees to –45 degrees in 1.4 degree increments. 0 degrees is the default (xx10 0000)	20

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7.8.2 0x281 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_R	R/W	Red Contrast Adjustment 80h+ = Higher contrast contrast 80h = Neutral 80h- = Lower	80

7.8.3 0x282 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_G	R/W	Green Contrast Adjustment 80h+ = Higher contrast contrast 80h = Neutral 80h- = Lower	80

7.8.4 0x283 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_B	R/W	Blue Contrast Adjustment 80h+ = Higher contrast contrast 80h = Neutral 80h- = Lower	80

7.8.5 0x284 – Image Adjustment Register

Bit	Function	R/W	Description			Reset
7-0	CONTRAST_Y	R/W	Y Contrast Adjustment 80h+ = Higher contrast contrast	80h = Neutral	80h- = Lower	80

7.8.6 0x285 – Image Adjustment Register

Bit	Function	R/W	Description			Reset
7-0	CONTRAST_Cb	R/W	Cb Contrast Adjustment 80h+ = Higher contrast contrast	80h = Neutral	80h- = Lower	80

7.8.7 0x286 – Image Adjustment Register

Bit	Function	R/W	Description			Reset
7-0	CONTRAST_Cr	R/W	Cr Contrast Adjustment 80h+ = Higher contrast contrast	80h = Neutral	80h- = Lower	80

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7.8.8 0x287 – Image Adjustment Register

Bit	Function	R/W	Description			Reset
7-0	BRIGHTNESS_R	R/W	Red Brightness Adjustment 80h+ = Higher brightness brightness	80h = Neutral	80h- = Lower	80

7.8.9 0x288 – Image Adjustment Register

Bit	Function	R/W	Description			Reset
7-0	BRIGHTNESS_G	R/W	Green Brightness Adjustment 80h+ = Higher brightness brightness	80h = Neutral	80h- = Lower	80

7.8.10 0x289 – Image Adjustment Register

Bit	Function	R/W	Description			Reset
7-0	BRIGHTNESS_B	R/W	Blue Brightness Adjustment 80h+ = Higher brightness brightness	80h = Neutral	80h- = Lower	80

7.8.11 0x28A – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_Y	R/W	Y Brightness Adjustment 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

7.8.12 0x28B – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-4	H_SHARP_COR	R/W	Coring function for sharpness control	3
3-0	H_SHARPNESS	R/W	Sharpness Adjustment	0

7.8.13 0x28C – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	H_SHARP_FREQ	R/W	Sharpness frequency select 0 = Low freq 1 = High freq	0
6-0	Reserved	-	Reserved	-

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7.8.14 0x2B0 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	-
5	PEDLVL	R/W	Black level selection. 0 = 0 1 = 16d	0
4	WHTLVL	R/W	White level selection. 0 = 235d 1 = 255d	1
3-1	Reserved	-	Reserved	-
0	BW_EN	R/W	0 = BW stretch disable 1 = BW stretch enable	0

7.8.15 0x2B1 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_BSLOPE	R/W	Black side slope. 00h: x1, 40h: x2, 80h: x3, C0h: x4, Should not be more than D0h	40

7.8.16 0x2B2 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_WSLOPE	R/W	White side slope. 00h: x1, 40h: x2, 80h: x3, C0h: x4, Should not be more than D0h	40

7.8.17 0x2B6 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_BLACK_TILT	R/W	Tilt point for black stretch	67

7.8.18 0x2B7 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_WHITE_TILT	R/W	Tilt point for white stretch	94

7.8.19 0x2BE – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	-	Reserved	-
1	Y16	R/W	Y pedestal level selection of YUV to RGB conversion. 1: Decimal 16 level become black level, 0: No offset adjustment	0
0	BT7	R/W	Conversion matrix selection of YUV to RGB conversion. 1: Matrix for HDTV standard, 0: Matrix for SDTV standard.	0

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7.8.20 0x2BF – Test Pattern Generator Register

Bit	Function	R/W	Description	Reset
7	TPG_EN	R/W	1 = Internal Test Pattern Generator Enabled, 0 = Scaler output (Default)	0
6-4	SWAP	R/W	RGB/YcbCr byte swap for color change	0
3-0	PAT_SEL	R/W	Pattern selection. 0 = Hue map 1 = Hue map (fine) 2 = Gray horizontal 17 steps 3 = Gray vertical 17 steps 4 = Gray H/V 17x17 steps 5 = White rectangle 6 = Vertical 1-dot stripe 7 = Horizontal 1-dot stripe 8 = Black/White checker board 9 = RGB checker board A = Gray horizontal 17 steps + horizontal black stripes B = Mitsubishi WQVGA test pattern C = Flat 100% blue D = Ramp E, F = Flat 50% gray	0

7.9 Gamma and Dither

7.9.1 0x2E0 – LCDC Gamma Control Register

Bit	Function	R/W	Description	Reset
7	GAMAE_R	R/W	Enable Red gamma correction.	0
6	GAMAE_G	R/W	Enable Green gamma correction.	0
5	GAMAE_B	R/W	Enable Blue gamma correction.	0
4	Reserved	-	Reserved	-
3-2	AUTO_INC	R/W	Enable Gamma table address auto increment for reading/writing Gamma data port. 0 = Disable, 1 = Read Only, 2 = Write Only, 3 = Read/Write	0
1-0	GAMMA_RGB_INDX	R/W	Gamma tables access selection: Index address 0x2F1 to 0x2F2 are used for gamma table accesses. There are 3 sets of gamma table, one table for one color, sharing the same address port and data port. These 2 bits identifies which table is accessed. 0 = RGB Gamma table 1 = Red Gamma table 2 = Green Gamma table 3 = Blue Gamma table	0

7.9.2 0x2E1 – Gamma Table Address Port Register

Bit	Function	R/W	Description	Reset
7-0	GAMMA_RAM-STARTING_ADDR	R/W	Gamma table address port.	00

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7.9.3 0x2E3 – Gamma Table Data Port Register

Bit	Function	R/W	Description	Reset
7-0	GAMMA_RAM_DATA[7:0]	R/W	Gamma table data port (lower bits)	00

7.9.4 0x2E4 – Dither Option Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
7-0	DITHER_OPTION	R/W	Dither Option Code 010 is recommended for 6:6:6 output	0
3	Reserved	R/W	Reserved	-
2-0	DITHER_FORMAT	R/W	Dither Output Format Selection 001 is recommended for 6:6:6 output	0

7.9.5 Dither Output Selection and Calculations

Dither Output Format Selection	Flat Panel RGB Bit Format Output	Dither Option Code	Input LSBs Used in Dither Calculation	Dither Method
000	8:8:8	000	n/a	none
001	6:6:6	001	(3) (3) (3)	2x2
		010	(3,2) (3,2)(3,2)	2x2
		011	(3,2,1) (3,2,1)(3,2,1)	2x2
		100	(3,2,1,0) (3,2,1,0)(3,2,1,0)	4x4
010	5:6:5	001	(4) (3) (4)	2x2
		010	(4,3) (3,2) (4,3)	2x2
		011	(4,3,2) (3,2) (4,3,2)	2x2
		100	(4,3,2,1) (3,2,1) (4,3,2,1)	4x4
011	5:5:5	001	(4) (4) (4)	2x2
		010	(4,3) (4,3) (4,3)	2x2
		011	(4,3,2) (4,3,2) (4,3,2)	2x2
		100	(4,3,2,1) (4,3,2,1) (4,3,2,1)	4x4
100	4:4:4	001	(5) (5) (5)	2x2
		010	(5,4) (5,4) (5,4)	2x2
		011	(5,4,3) (5,4,3) (5,4,3)	2x2
		100	(5,4,3,2) (5,4,3,2) (5,4,3,2)	4x4
101	3:3:3	001	(6) (6) (6)	2x2
		010	(6,5) (6,5) (6,5)	2x2
		011	(6,5,4) (6,5,4) (6,5,4)	2x2
		100	(6,5,4,3) (6,5,4,3) (6,5,4,3)	4x4
110	3:3:2	001	(6) (6) (7)	2x2
		010	(6,5) (6,5) (7,6)	2x2
		011	(6,5,4) (6,5,4) (6,5,4)	2x2
		100	(6,5,4,3) (6,5,4,3) (7,6,5,4)	4x4

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7.9.6 0x2F0 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	RDKEYPOS_X	R/W	Color level readout position X [7:0] (LSB)	00

7.9.7 0x2F1 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	RDKEYPOS_Y	R/W	Color level readout position Y [7:0] (LSB)	00

7.9.8 0x2F2 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6-4	RDKEYPOS_Y[10:8]	R/W	Color level readout position Y [10:8] (MSB)	0
3-0	RDKEYPOS_X[11:8]	R/W	Color level readout position X [11:8] (MSB)	0

7.9.9 0x2F3 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	RED_LVL	R	Red level	-

7.9.10 0x2F4 – RGB Level Readout Register

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Bit	Function	R/W	Description	Reset
7-0	GRN_LVL	R	Green level	-

7.9.11 0x2F5 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	BLU_LVL	R	Blue level	-

7.9.12 0x2F8 – 8-bit Panel Interface Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6	RGB_ORDR	R/W	0 = R->G->B order, 1 = R->B->G order	0
5	AVRG_EN	R/W	1 = Averaging on every other line enable, 0 = No Averaging	0
4	AVRG_POL	R/W	1 = Averaging on even line, 0 = Averaging on odd line	0
3-2	COL_ODD	R/W	Start color for odd line,0 = R, 1 = B, 2 = G, 3 = X	0
1-0	COL_EVEN	R/W	Start color for even line, 0 = R, 1 = B, 2 = G, 3 = X	0

7.9.13 0x2F9 – 8-bit Panel Interface Register

Bit	Function	R/W	Description	Reset
7	DELTA_TYPE	R/W	Type selection of 8-bit interface for averaging, 1 = Serial RGB, 0 = Delta RGB	0
6	REV_EN	R/W	1 = REV output (toggles when more than 9 bits of RGB data have transition) activated	0
5-2	Reserved	R/W	Reserved	-
1	DMMY_EN	R/W	Serial RGB mode, 1 = S-RGB with Dummy, 0 = S-RGB without Dummy	0
0	DMMY_POS	R/W	Serial RGB Dummy byte position, 1 = Dummy comes first, 0 = Dummy comes last	0

7.10 FONT OSD

7.10.1 0x300 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	-
4	W16EN	R/W	1 = Char. Width = 16 pixels, 0 = Char. Width = 12 pixels	0
3	Reserved	R/W	Reserved	-
2	MIREN	R/W	1 = Enable FONT Mirror	0
1	FONT_SWITC	R/W	1 = Bypass FONT RAM FIFO	0
0	OSD_SWITCH	R/W	1 = Bypass OSD RAM FIFO	0

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7.10.2 0x301 – Test Register

Bit	Function	R/W	Description	Reset
7-1	Reserved	R	Reserved	-
0	STATUS	R	OSD Window Active Status	-

7.10.3 0x302 – Test Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	DBGWIN	R/W	OSD Debug Window Selection	0
3-0	DBG	R/W	OSD Debug Signal Selection	6

7.10.4 0x303 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7-0	OSD DE Delay	R/W	OSD DE Delay from H-SYNC	00

7.10.5 0x304 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7	BLINK	R/W	1 = Character Blinking effect enable	0
6	Reserved	R/W	Reserved	-
5	UP256	R/W	0 = Lower 256 char, 1 = Upper 256 char	0
4	BSEN	R/W	1 = Character Bordering/Shadowing effect enable.	0
3-2	AUTO	R/W	OSD RAM Auto Increase of Write Address Mode Selection. 00 = Normal mode, 01 = Font Data or Attribute Address auto mode 11 = Font Data auto mode (Previous Attribute data automatic write)	0
1	CLEAR	R/W	OSD RAM Auto Clear Mode	0
0	FR_RAC_SEL	R/W	Font/OSD RAM Serial Bus Access 0 = OSD RAM, 1 = Font RAM access	0

7.10.6 0x305 – Font OSD Control Register

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Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5	FBITEXT	R/W	1 = Enable character horizontal extension.	0
4	RD_SEL	R/W	Register 097h, 098h Read mode selection. 0 = Normal display, 1 = QVGA display	0
3-0	Reserved	R/W	Reserved	-

7.10.7 0x306 – OSD RAM Address Register

Bit	Function	R/W	Description	Reset
7-0	I2COSDRAD	R/W	OSD RAM Address Low 8-bit (word address for single byte access).	00

7.10.8 0x307 – OSD RAM Data Port Hi Register

Bit	Function	R/W	Description	Reset
7-0	FDATA	R/W	OSD RAM Data Port Hi (Font Data).	-

7.10.9 0x308 – OSD RAM Data Port Lo Register

Bit	Function	R/W	Description	Reset
7-0	FATTRIBUTE	R/W	OSD RAM Data Port Lo (Font Attribute).	-

7.10.10 0x309 – Font RAM Address Register

Bit	Function	R/W	Description	Reset
7-0	I2CFONTRAD	R/W	Serial Bus Font RAM Address.	00

7.10.11 0x30A – Font RAM Data Port

Bit	Function	R/W	Description	Reset
7-0	I2CFONTDAT	R/W	Serial Bus Font RAM Data Port.	-

7.10.12 0x30B – Multi-Color Font Start Position Register

Bit	Function	R/W	Description	Reset
7-0	MADD2	R/W	Programmable SRAM address start position for 2-bit Multi-Color fonts.	31

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7.10.13 0x30C – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6	OSDON	R/W	OSD ON/OFF Enable Control 0 = OSD ON, 1 = OSD OFF	0
5-0	TABLE_WSEL	R/W	Character color look up table write address select.	0

7.10.14 0x30D – Character Color Look-up table data port High Byte Register

Bit	Function	R/W	Description	Reset
7-0	TABLE_CON_H	R/W	Character color look up table data port high byte.	00

7.10.15 0x30E – Character Color Look-up table data port Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	TABLE_CON_L	R/W	Character color look up table data port low byte.	00

7.10.16 0x310 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	WIN1EN	R/W	OSD Window #n Enable	0
6	WIN1MCOLOR	R/W	1 = OSD Window #n multicolor font enable.	0
5	WIN1CVEXT	R/W	1 = Character vertical extension enable.	0
4	Reserved	R/W	Reserved.	-
3-2	XWIN1ZOOM	R/W	OSD Window #n Horizontal Zoom. 00 = no zoom, 01 = x2, 10 = x3, 11 = x4	0
1-0	YWIN1ZOOM	R/W	OSD Window #n Vertical Zoom. 00 = no zoom, 01 = x2, 10 = x3, 11 = x4	0

7.10.17 0x311 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved.	-
3-0	WIN1ALPHA	R/W	OSD Window #n alpha blending amount.	0

7.10.18 0x312 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-4	WIN1HSTR	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	0
3-2	Reserved	R/W	Reserved.	-
1-0	WIN1VSTR	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	0

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7.10.19 0x313 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN1HSTR	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	00

7.10.20 0x314 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN1VSTR	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	00

7.10.21 0x315 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN1HEIGHT	R/W	OSD Window #n V-Height (1 Character height per step).	00

7.10.22 0x316 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN1WIDTH	R/W	OSD Window #n H-Width (1 Character width per step).	00

7.10.23 0x317 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved.	-
4	WIN1REGSTA	R/W	OSD Display RAM starting address High 1-bit (total 9bits) of OSD Window #n	0
3-0	WIN1BC	R/W	OSD Window #n Border Color control.	0

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7.10.24 0x318 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	WIN1BCEN	R/W	OSD Window #n Border Color Enable.	0
6-5	Reserved	R/W	Reserved.	-
4-0	WIN1BCWID	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	00

7.10.25 0x319 – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN1HBWID	R/W	OSD Window #n H-Border Width (1 pixel per step).	00

7.10.26 0x31A – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN1VBWID	R/W	OSD Window #n V-Border Width (1 scan line per step).	00

7.10.27 0x31B – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	WIN1BEN	R/W	OSD Window #n 3-D effect enable.	0
6	WIN1TEN	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
5	WIN1EFF	R/W	OSD Window #n 3-D effect Level Control.	0
4	WIN1BSEL	R/W	Character Border/Shadow selection. 1 = Shadow, 0 = Border	0
3-0	WIN1SC	R/W	OSD Window #n shadow color control.	0

7.10.28 0x31C – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7	WIN1SCEN	R/W	OSD Window #n shadow enable.	0
6	WIN1CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
5	WIN1CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
4-0	WIN1SCWID	R/W	OSD Window #n shadow width.	0

7.10.29 0x31D – OSD Window1 Control Register

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Bit	Function	R/W	Description	Reset
7-4	WIN1CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step)	0
3-0	WIN1CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step).	0

7.10.30 0x31E – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN1BGC	R/W	OSD Window #n Background Color control	0
3-0	WIN1BSC	R/W	OSD Window #n character border/shadow color Control	0

7.10.31 0x31F – OSD Window1 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN1REGSTA	R/W	OSD Display RAM starting address Low 8-bit of OSD Window #n.	00

7.10.32 0x320 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	WIN2EN	R/W	OSD Window #n Enable	0
6	WIN2MCOLOR	R/W	1 = OSD Window #n multicolor font enable.	0
5	WIN2CVEXT	R/W	1 = Character vertical extension enable.	0
4	Reserved	R/W	Reserved.	-
3-2	XWIN2ZOOM	R/W	OSD Window #n Horizontal Zoom. 00 = no zoom, 01 = x2, 10 = x3, 11 = x4	0
1-0	YWIN2ZOOM	R/W	OSD Window #n Vertical Zoom. 00 = no zoom, 01 = x2, 10 = x3, 11 = x4	0

7.10.33 0x321 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved.	-
3-0	WIN2ALPHA	R/W	OSD Window #n alpha blending amount.	0

7.10.34 0x322 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-4	WIN2HSTR	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	0
3-2	Reserved	R/W	Reserved.	-
1-0	WIN2VSTR	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	0

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7.10.35 0x323 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN2HSTR	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	00

7.10.36 0x324 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN2VSTR	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	00

7.10.37 0x325 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN2HEIGHT	R/W	OSD Window #n V-Height (1 Character height per step).	00

7.10.38 0x326 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN2WIDTH	R/W	OSD Window #n H-Width (1 Character width per step).	00

7.10.39 0x327 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved.	-
4	WIN2REGSTA	R/W	OSD Display RAM starting address High 1-bit (total 9bits) of OSD Window #n	0
3-0	WIN2BC	R/W	OSD Window #n Border Color control.	0

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7.10.40 0x328 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	WIN2BCEN	R/W	OSD Window #n Border Color Enable.	0
6-5	Reserved	R/W	Reserved.	-
4-0	WIN2BCWID	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	00

7.10.41 0x329 – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN2HBWID	R/W	OSD Window #n H-Border Width (1 pixel per step).	00

7.10.42 0x32A – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN2VBWID	R/W	OSD Window #n V-Border Width (1 scan line per step).	00

7.10.43 0x32B – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	WIN2BEN	R/W	OSD Window #n 3-D effect enable.	0
6	WIN2TEN	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
5	WIN2EFF	R/W	OSD Window #n 3-D effect Level Control.	0
4	WIN2BSEL	R/W	Character Border/Shadow selection. 1 = Shadow, 0 = Border	0
3-0	WIN2SC	R/W	OSD Window #n shadow color control.	0

7.10.44 0x32C – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7	WIN2SCEN	R/W	OSD Window #n shadow enable.	0
6	WIN2CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
5	WIN2CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
4-0	WIN2SCWID	R/W	OSD Window #n shadow width.	0

7.10.45 0x32D – OSD Window2 Control Register

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Bit	Function	R/W	Description	Reset
7-4	WIN2CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step)	0
3-0	WIN2CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step).	0

7.10.46 0x32E – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN2BGC	R/W	OSD Window #n background color control	0
3-0	WIN2BSC	R/W	OSD Window #n character border/shadow color Control	0

7.10.47 0x32F – OSD Window2 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN2REGSTA	R/W	OSD Display RAM starting address Low 8-bit of OSD Window #n.	00

7.10.48 0x330 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	WIN3EN	R/W	OSD Window #n Enable	0
6	WIN3MCOLOR	R/W	1 = OSD Window #n multicolor font enable.	0
5	WIN3CVEXT	R/W	1 = Character vertical extension enable.	0
4	Reserved	R/W	Reserved.	-
3-2	XWIN3ZOOM	R/W	OSD Window #n Horizontal Zoom. 00 = no zoom, 01 = x2, 10 = x3, 11 = x4	0
1-0	YWIN3ZOOM	R/W	OSD Window #n Vertical Zoom. 00 = no zoom, 01 = x2, 10 = x3, 11 = x4	0

7.10.49 0x331 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved.	-
3-0	WIN3ALPHA	R/W	OSD Window #n alpha blending amount.	0

7.10.50 0x332 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-4	WIN3HSTR	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	0
3-2	Reserved	R/W	Reserved.	-
1-0	WIN3VSTR	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	0

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7.10.51 0x333 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN3HSTR	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	00

7.10.52 0x334 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN3VSTR	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	00

7.10.53 0x335 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN3HEIGHT	R/W	OSD Window #n V-Height (1 Character height per step).	00

7.10.54 0x336 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN3WIDTH	R/W	OSD Window #n H-Width (1 Character width per step).	00

7.10.55 0x337 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved.	-
4	WIN3REGSTA	R/W	OSD Display RAM starting address High 1-bit (total 9bits) of OSD Window #n	0
3-0	WIN3BC	R/W	OSD Window #n Border Color control.	0

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7.10.56 0x338 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	WIN3BCEN	R/W	OSD Window #n Border Color Enable.	0
6-5	Reserved	R/W	Reserved.	-
4-0	WIN3BCWID	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	00

7.10.57 0x339 – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN3HBWID	R/W	OSD Window #n H-Border Width (1 pixel per step).	00

7.10.58 0x33A – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN3VBWID	R/W	OSD Window #n V-Border Width (1 scan line per step).	00

7.10.59 0x33B – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	WIN3BEN	R/W	OSD Window #n 3-D effect enable.	0
6	WIN3TEN	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
5	WIN3EFF	R/W	OSD Window #n 3-D effect Level Control.	0
4	WIN3BSEL	R/W	Character Border/Shadow selection. 1 = Shadow, 0 = Border	0
3-0	WIN3SC	R/W	OSD Window #n shadow color control.	0

7.10.60 0x33C – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7	WIN3SCEN	R/W	OSD Window #n shadow enable.	0
6	WIN3CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
5	WIN3CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
4-0	WIN3SCWID	R/W	OSD Window #n shadow width.	0

7.10.61 0x33D – OSD Window3 Control Register

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Bit	Function	R/W	Description	Reset
7-4	WIN3CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step)	0
3-0	WIN3CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step).	0

7.10.62 0x33E – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN3BGC	R/W	OSD Window #n background color control	0
3-0	WIN3BSC	R/W	OSD Window #n character border/shadow color control	0

7.10.63 0x33F – OSD Window3 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN3REGSTA	R/W	OSD Display RAM starting address Low 8-bit of OSD Window #n.	00

7.10.64 0x340 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	WIN4EN	R/W	OSD Window #n Enable	0
6	WIN4MCOLOR	R/W	1 = OSD Window #n multicolor font enable.	0
5	WIN4CVEXT	R/W	1 = Character vertical extension enable.	0
4	Reserved	R/W	Reserved.	-
3-2	XWIN4ZOOM	R/W	OSD Window #n Horizontal Zoom 00 = No zoom, 01 = x2, 10 = x3, 11 = x4	0
1-0	YWIN4ZOOM	R/W	OSD Window #n Vertical Zoom. 00 = No zoom, 01 = x2, 10 = x3, 11 = x4	0

7.10.65 0x341 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved.	-
3-0	WIN4ALPHA	R/W	OSD Window #n alpha blending amount.	0

7.10.66 0x342 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-4	WIN4HSTR	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	0
3-2	Reserved	R/W	Reserved.	-
1-0	WIN4VSTR	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	0

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7.10.67 0x343 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN4HSTR	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	00

7.10.68 0x344 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN4VSTR	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	00

7.10.69 0x345 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN4HEIGHT	R/W	OSD Window #n V-Height (1 Character height per step).	00

7.10.70 0x346 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved.	-
5-0	WIN4WIDTH	R/W	OSD Window #n H-Width (1 Character width per step).	00

7.10.71 0x347 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved.	-
4	WIN4REGSTA	R/W	OSD Display RAM starting address High 1-bit (total 9bits) of OSD Window #n	0
3-0	WIN4BC	R/W	OSD Window #n Border Color control.	0

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7.10.72 0x348 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	WIN4BCEN	R/W	OSD Window #n Border Color Enable.	0
6-5	Reserved	R/W	Reserved.	-
4-0	WIN4BCWID	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	00

7.10.73 0x349 – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN4HBWID	R/W	OSD Window #n H-Border Width (1 pixel per step).	00

7.10.74 0x34A – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	WIN4VBWID	R/W	OSD Window #n V-Border Width (1 scan line per step).	00

7.10.75 0x34B – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	WIN4BEN	R/W	OSD Window #n 3-D effect enable.	0
6	WIN4TEN	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
5	WIN4EFF	R/W	OSD Window #n 3-D effect Level Control.	0
4	WIN4BSEL	R/W	Character Border/Shadow selection. 1 = Shadow, 0 = Border	0
3-0	WIN4SC	R/W	OSD Window #n shadow color control.	0

7.10.76 0x34C – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7	WIN4SCEN	R/W	OSD Window #n shadow enable.	0
6	WIN4CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
5	WIN4CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
4-0	WIN4SCWID	R/W	OSD Window #n shadow width.	0

7.10.77 0x34D – OSD Window4 Control Register

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Bit	Function	R/W	Description	Reset
7-4	WIN4CHSPC	R/W	Character H-Space inside Window #n (1 pixel per step)	0
3-0	WIN4CVSPC	R/W	Character V-Space inside Window #n (1 scan line per step).	0

7.10.78 0x34E – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-4	WIN4BGC	R/W	OSD Window #n background color control	0
3-0	WIN4BSC	R/W	OSD Window #n character border/shadow color control	0

7.10.79 0x34F – OSD Window4 Control Register

Bit	Function	R/W	Description	Reset
7-0	WIN4REGSTA	R/W	OSD Display RAM starting address Low 8-bit of OSD Window #n.	00

7.10.80 0x350 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved.	-
4-0	CHEIGHT	R/W	Font OSD Character Height	12

7.10.81 0x351 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved.	-
6-0	MUL_CON	R/W	Sub-Font Total Count	1B

7.10.82 0x352 – Font OSD Control Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved.	-
4-0	ALPHA_SEL	R/W	Window alpha blending color selection.	00

7.10.83 0x353 – Multi-Color Font Start Position Register

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Bit	Function	R/W	Description	Reset
7-0	MADD3	R/W	Programmable SRAM address start position for 3-bit Multi-Color fonts.	71

7.10.84 0x354 – Multi-Color Font Start Position Register

Bit	Function	R/W	Description	Reset
7-0	MADD4	R/W	Programmable SRAM address start position for 4-bit Multi-Color fonts.	B1

8. Life Support Policy

These products are not authorized for use as critical components in life support devices or systems.

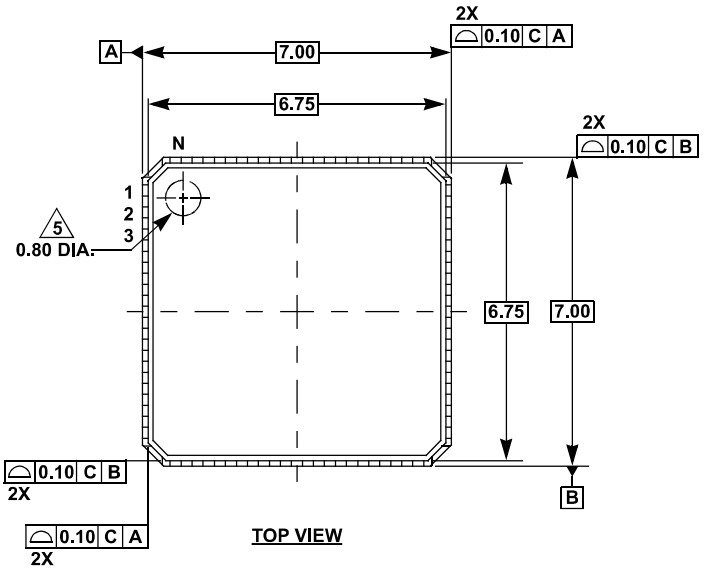
9. Package Outline Drawings

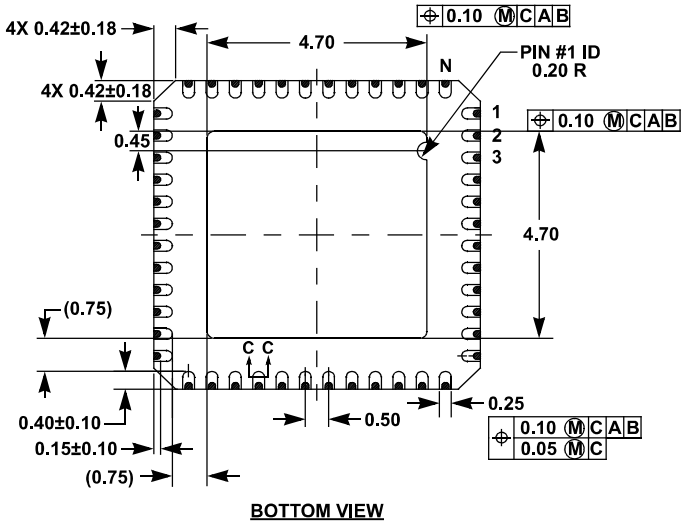
For the most recent package outline drawing, see L48.7x7V.

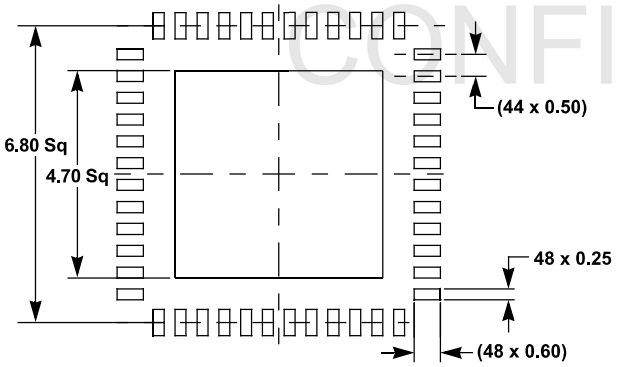
L48.7x7V

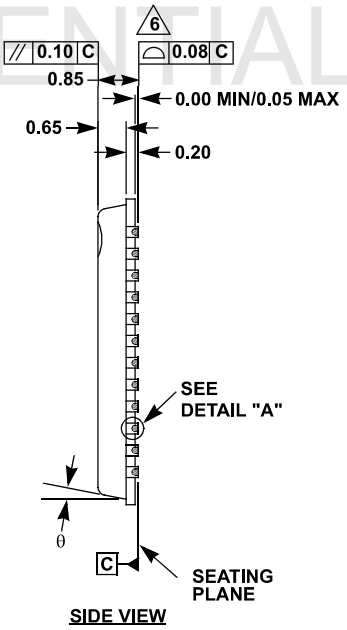
48 Lead Quad Flat No-Lead Plastic Package (Punch QFN with Wettable Flank)

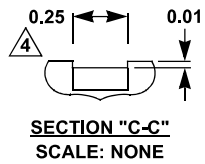
Rev 3, 12/15

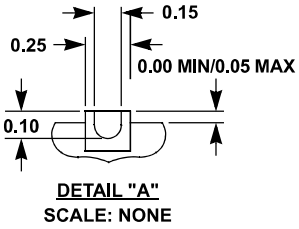












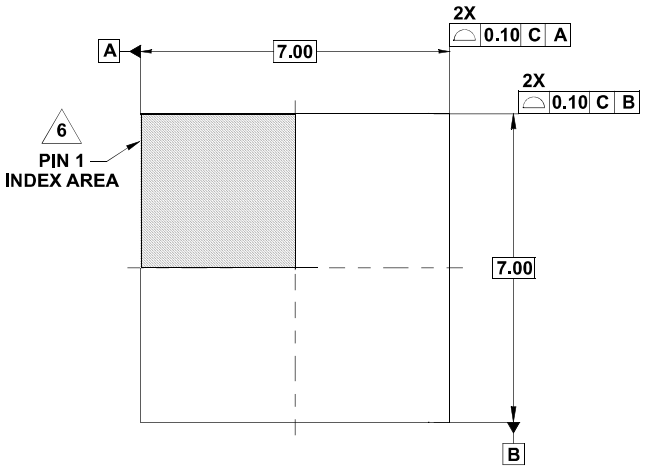
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NOTES:

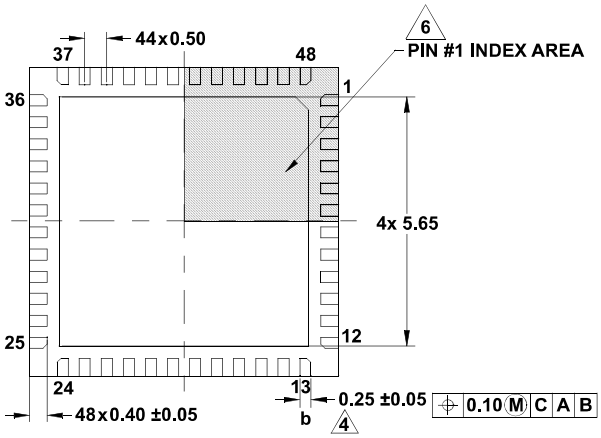
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.20mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

For the most recent package outline drawing, see L48.7x7W.

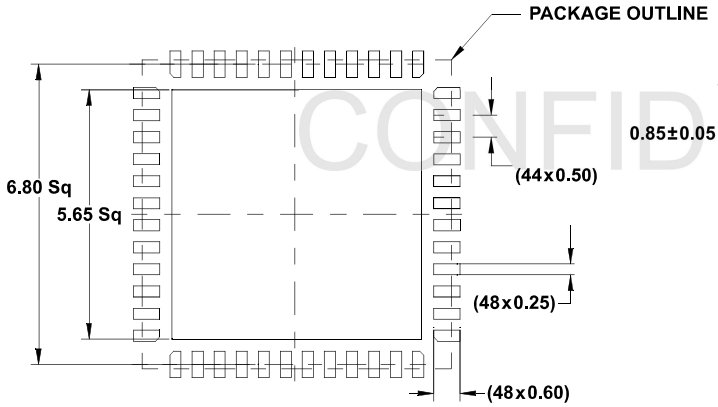
L48.7x7W
48 Lead Quad Flat No-Lead Plastic Package
Rev 0, 8/12



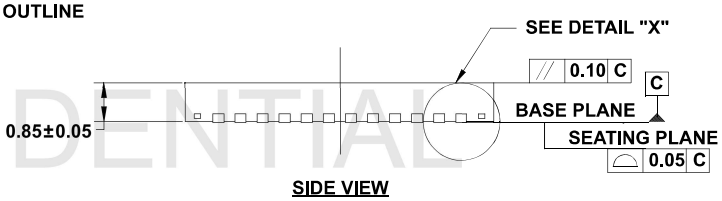
TOP VIEW



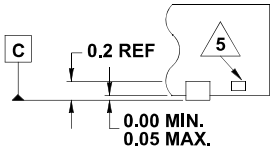
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

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NOTES:

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   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.20mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

10. Ordering Information

Part Number[1]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type[2]	Temp. Range
TW8819AT-NA2-GR[3]	TW8819AT NA2-GR	48L WFQFN (wettable flanks)	L48.7x7V	Tray	-40 to +105°C
TW8819AT-NA2-GRT[3]				Reel, 3k	
TW8819-NA2-CR[4]	TW8819 NA2-CR	48L QFN	L48.7x7W	Tray	-40 to +85°C
TW8819-NA2-CRT[4]				Reel, 3k	

1. For Moisture Sensitivity Level (MSL), see the TW8819 product page. For more information about MSL, see TB363.
2. See TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

11. Revision History

Revision	Date	Description
3.00	Dec 21, 2022	Applied latest template. Populated the TBDs in the Characteristics section. Corrected typo in the parameter name for YIN0~YIN3 Input Range. Removed the following registers because feature does not exist: ▪ 0x10D, 0x11A, 0x11B, 0x041, 0x140, 0x141, 0x142 Updated Register 0x131 changed Bit[2:0} to reserved. Updated Register 0x13A by adding more details. Updated Register 0x102 Bits[3:2] description. Updated Ordering Information table formatting/content. Updated Register 0x218 by correcting typo for the bit numbers in first row. Removed About Intersil section.
2.00	Dec 23, 2015	Page 29 - Replaced POD L48.7x7J with L48.7x7V.
1.00	May 8, 2014	Page 92 – 2nd line of the disclaimer changed from “Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality” to “Intersil products are manufactured, assembled and tested utilizing ISO9001 or TS16949 quality systems as applicable noted in the quality certifications found at http://www.intersil.com/en/support/qualandreliability.html” Page 1 – updated copyright information
0.00	Sep 24, 2013	Initial release.

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(Rev.5.0-1 October 2020)

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