STV8105

256 x 72 x 4-Bit OLED Passive Matrix Controller/Driver

PRELIMINARY DATA

(Bumped Die)
ORDER CODE: STV8105

Main Features

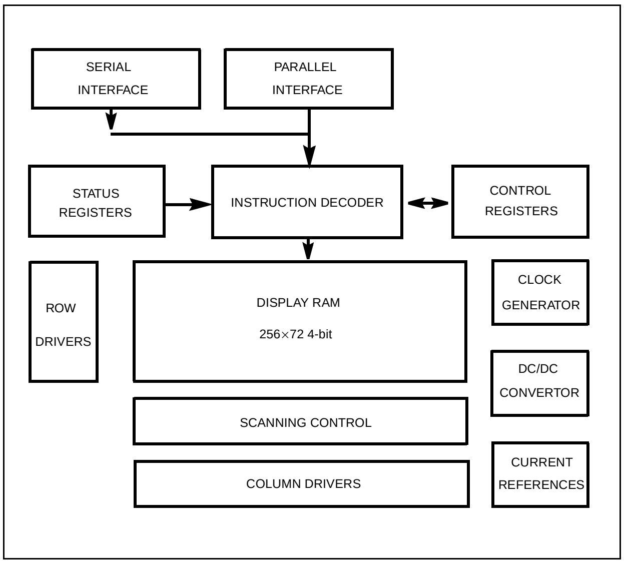
- **Supports Monochrome OLED Passive Matrices in different formats:**
  - 256×72 Black & White
  - 256×72×2-bits/4 levels of gray
  - 256×72×4-bits/16 levels of gray
  - 256×36×6-bits/64 levels of gray
  - 128×72×6-bits/64 levels of gray
- **On-chip DC/DC Step-up Converter**
- **Display Power Supply up to 25V**
- **Device Power Supply: 3.0 to 3.6V**
- **Low-power Consumption Suitable for Battery-operated Systems**
- **Column Source Current capability: 800µA, max.**
- **Row Sink Current capability: 110mA, max.**
- **On-chip Oscillator**
- **Programmable Gamma Correction**
- **Programmable Display Multiplexing**
- **Two Brightness Control registers of 128 steps each**
- **32 Step Dimmer Control**
- **One Time Programmable (OTP) fuse ROM for key configuration parameters**
- **Dual Scan, Master/Slave Capability**
- **Selectable 8-bit Parallel as well as Serial Peripheral Interfaces**

Description

The STV8105 is a low-power, controller/driver “combo” IC for OLED displays. The STV8105 supports 256 columns by 72 rows with 16 levels of gray for monochrome and 2 x 128 columns by 72 rows with 16 levels of gray for “two” color displays. It can control a display of 128 columns by 72 rows or 256 columns by 36 rows with 64 levels of gray in monochrome mode.

The STV8105 provides all necessary functions in a single chip, including on-chip supply control and bias current generators, resulting in a minimum of external components and in very low-power consumption.

The STV8105 communicates with the system via fully configurable interfaces (parallel or serial) to ease interfacing with the host microcontroller. The STV8105 has a set of command and control registers that can be addressed by these interfaces.



Contents

1 General Overview

The STV8105 is a monochrome, low-power controller/driver combo from STMicroelectronics' family of controllers for OLED displays. It has been developed to bring a flexible solution to applications and systems based on OLED passive matrices.

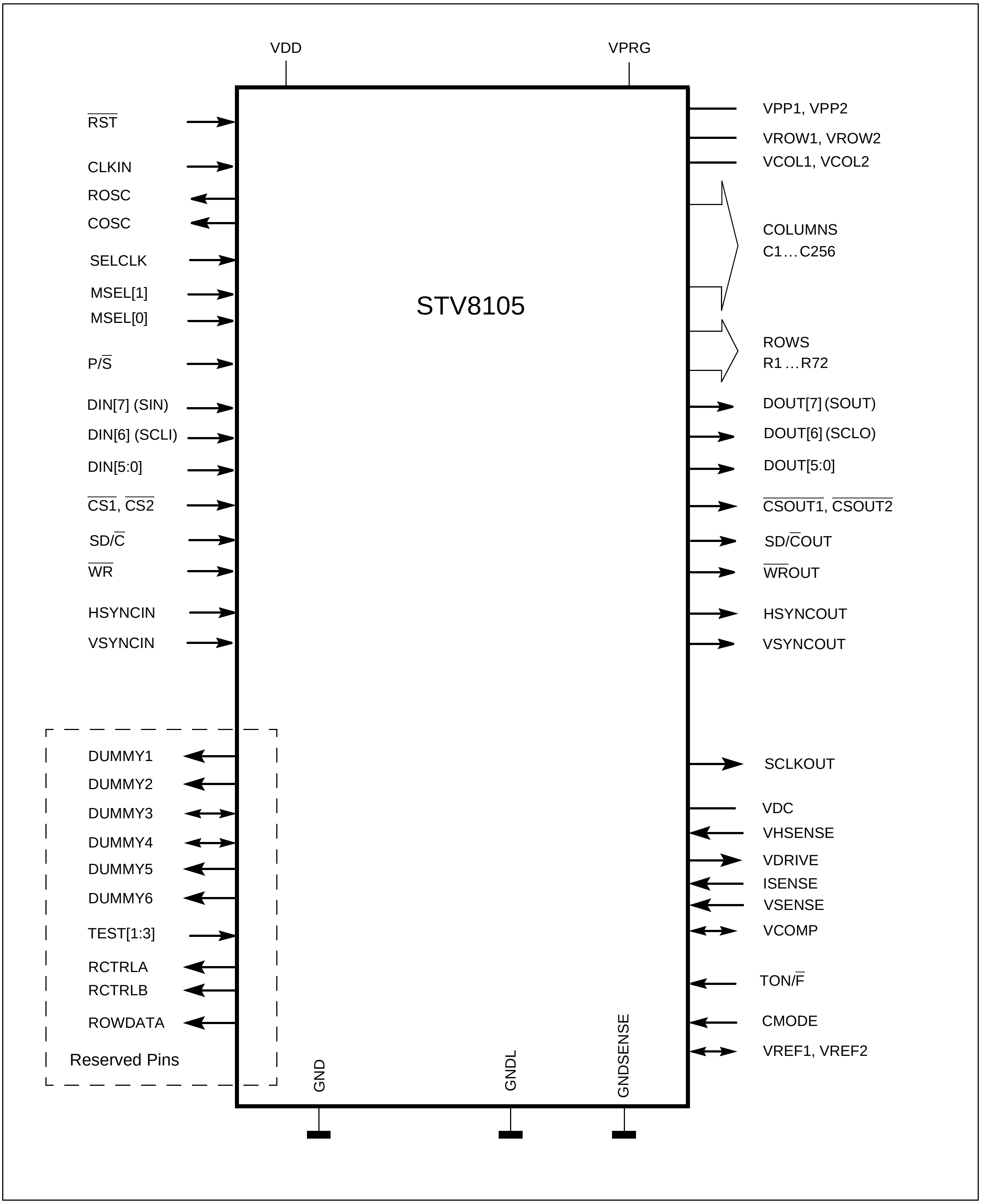
The STV8105 can be used with many different host micro-controllers. It supports a serial bus and a parallel interface covering most of the possible application architectures. This provides easy access to a set of command and control registers to properly program the STV8105.

The STV8105 includes a dual port Display RAM of 256 x 72 x 4-bits to support the full display capabilities of 256 column and 72 row drivers with several display functions.

The on-chip DC/DC step-up converter generates the necessary supply voltage (18V, typically) for all row and column drivers from the battery.

Processed in BCD technology, the STV8105 features a low-power digital core and output drivers that can source up to 800µA for columns and sink up to 110mA for rows with a display supply of up to 25V. Thanks to the high level of integration, the number of required external components is drastically reduced.

Figure 1: STV8105 Input/Output Diagram



1.1 Bumped Die Pad Description

Figure 2: Die Mechanical Data (Bump-side View)

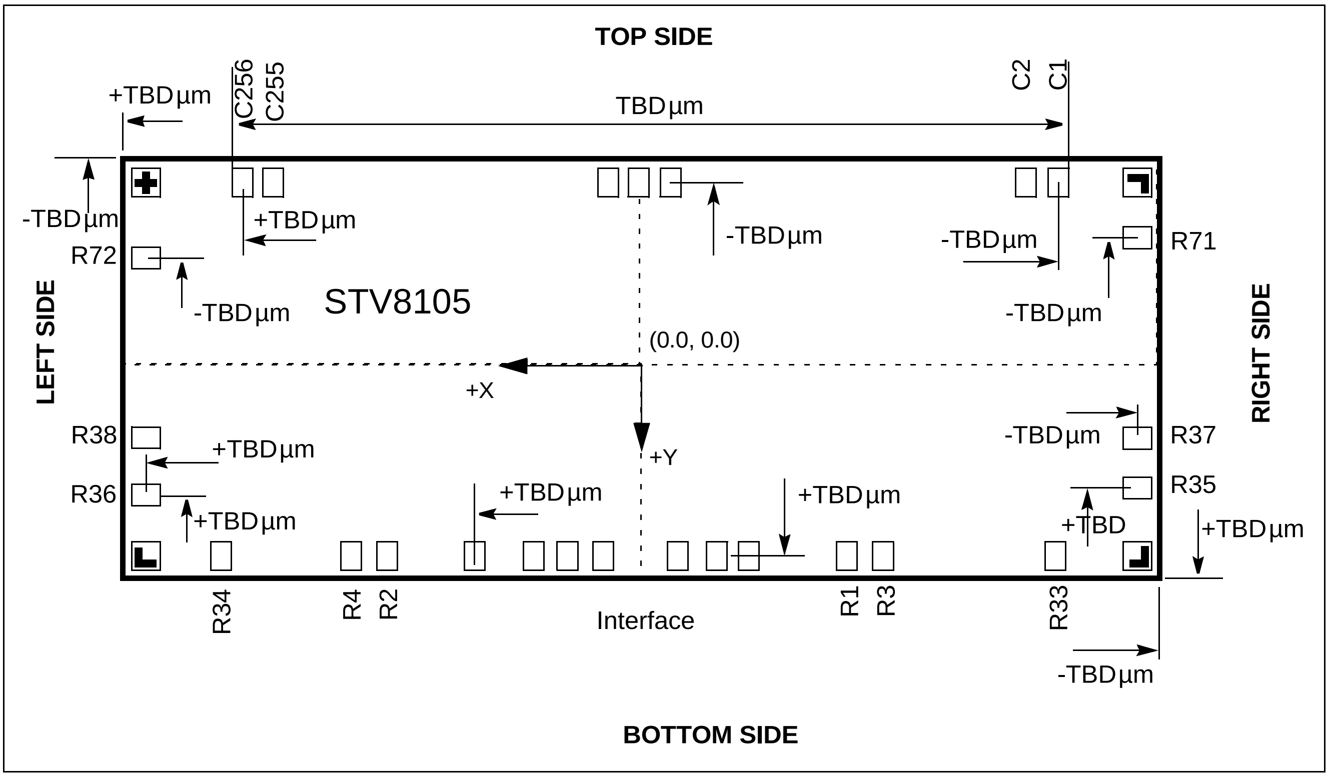


Figure 3: Alignment Mark Positions (Bump-side View)

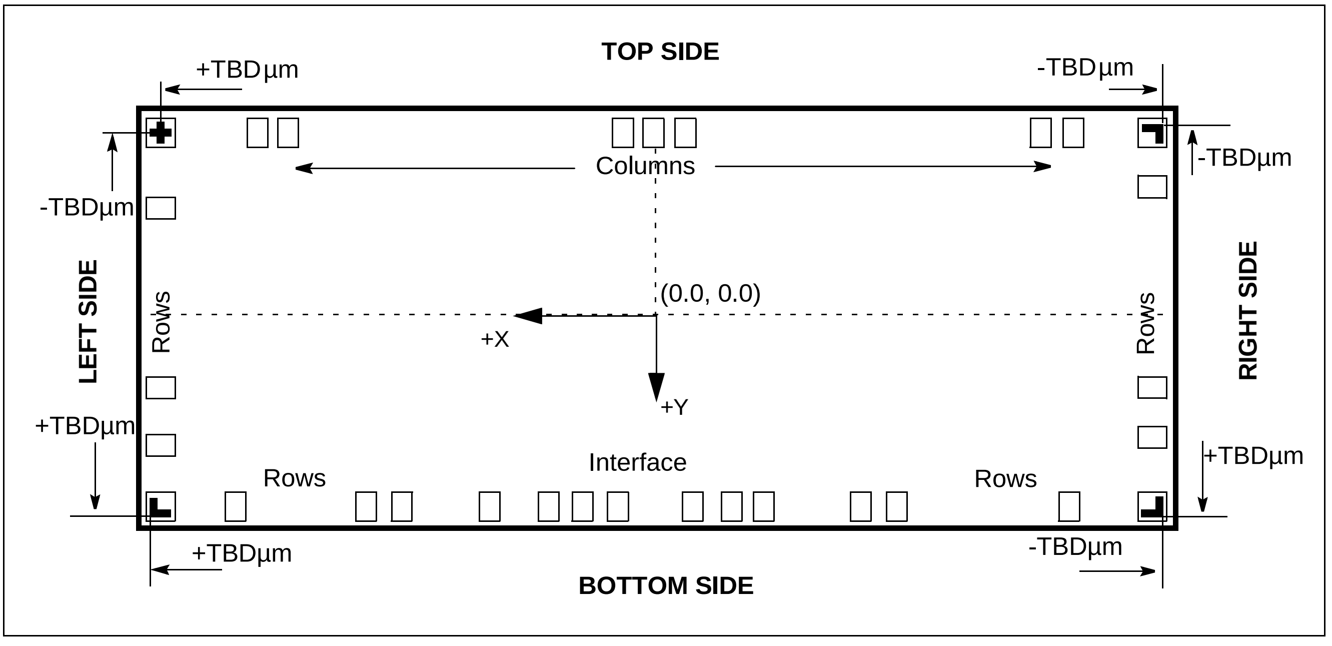


Figure 4: Alignment Mark Mechanical Data

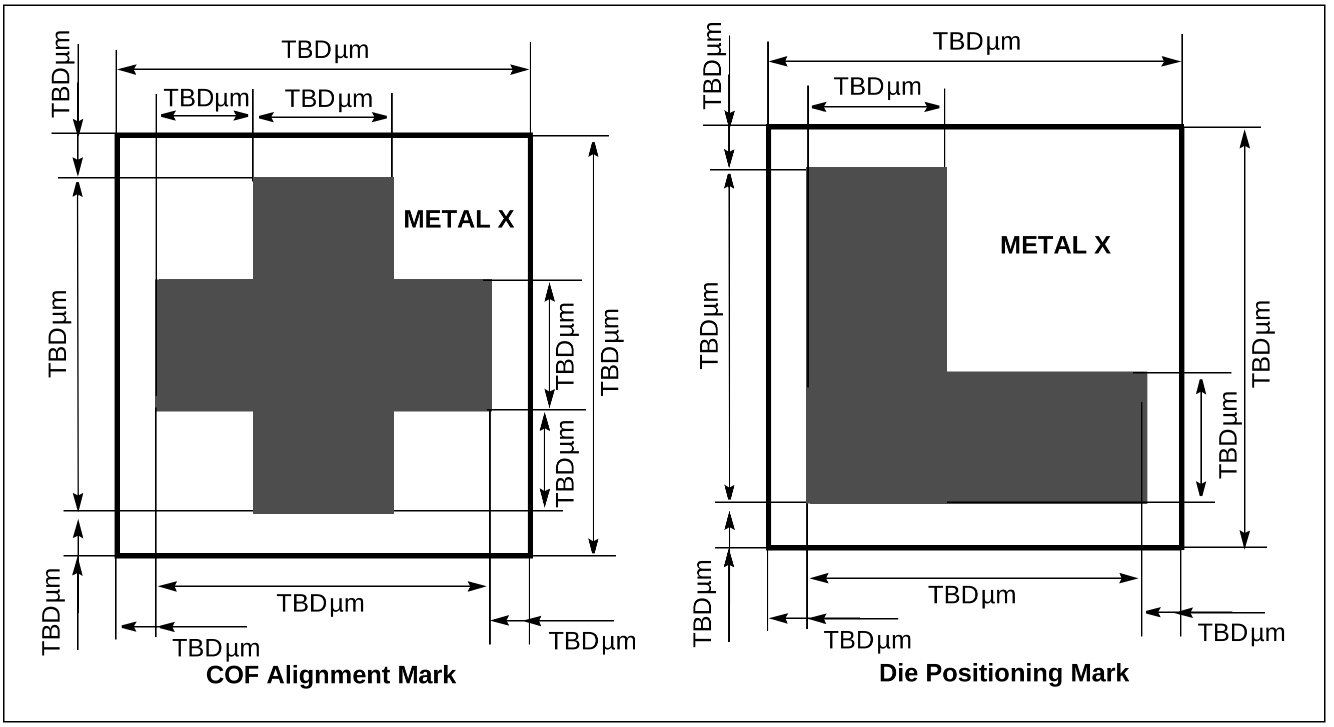
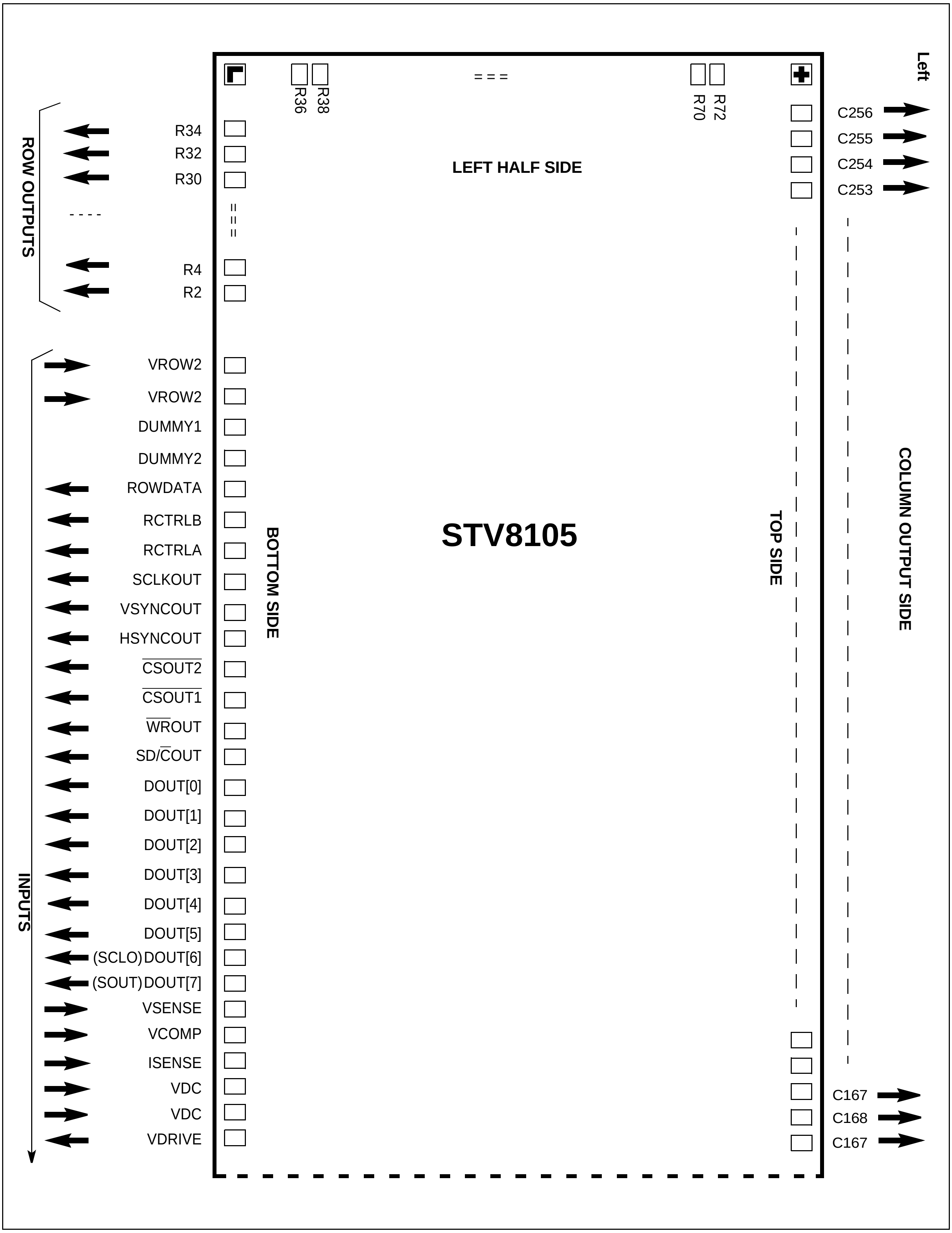
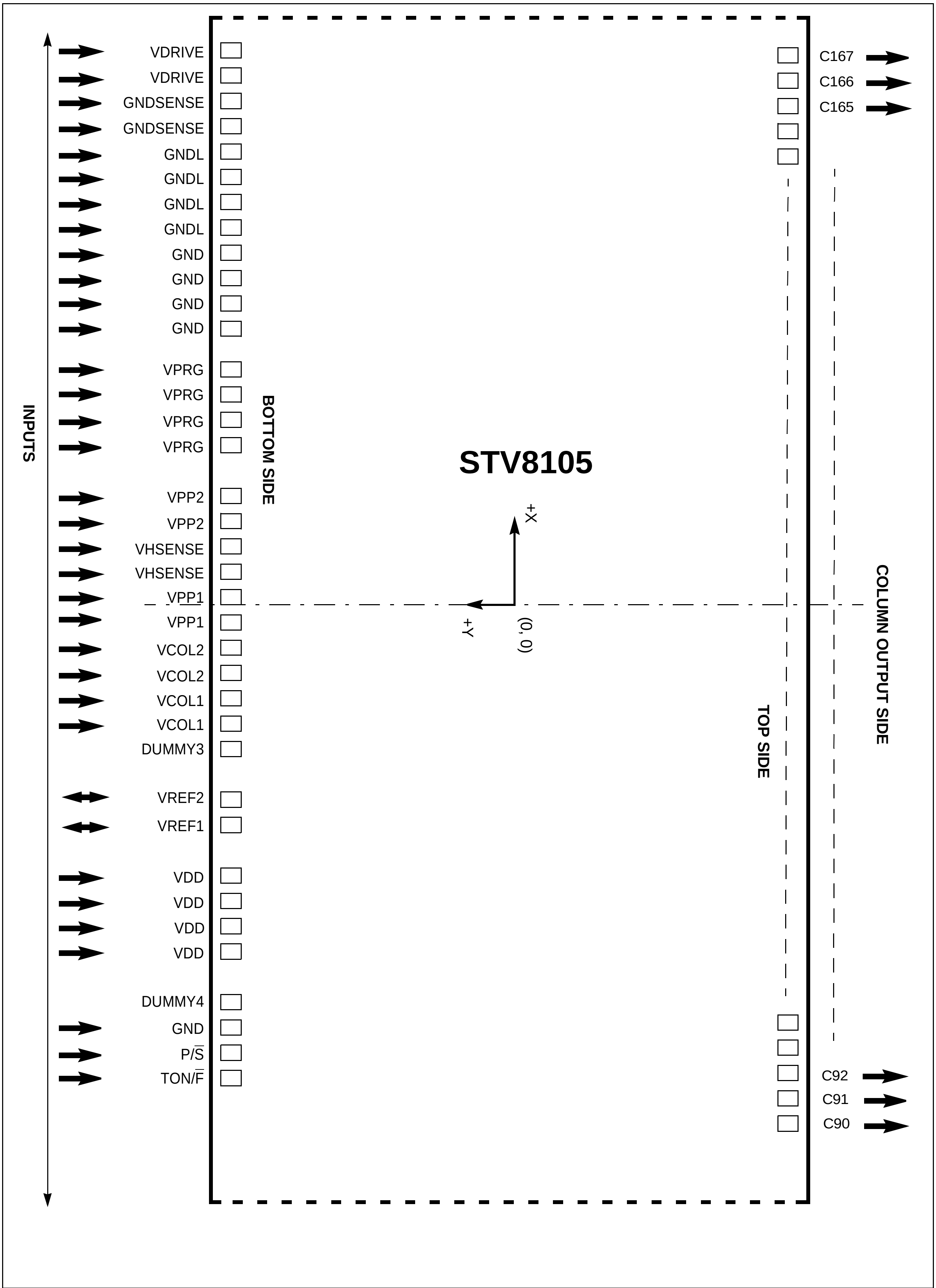
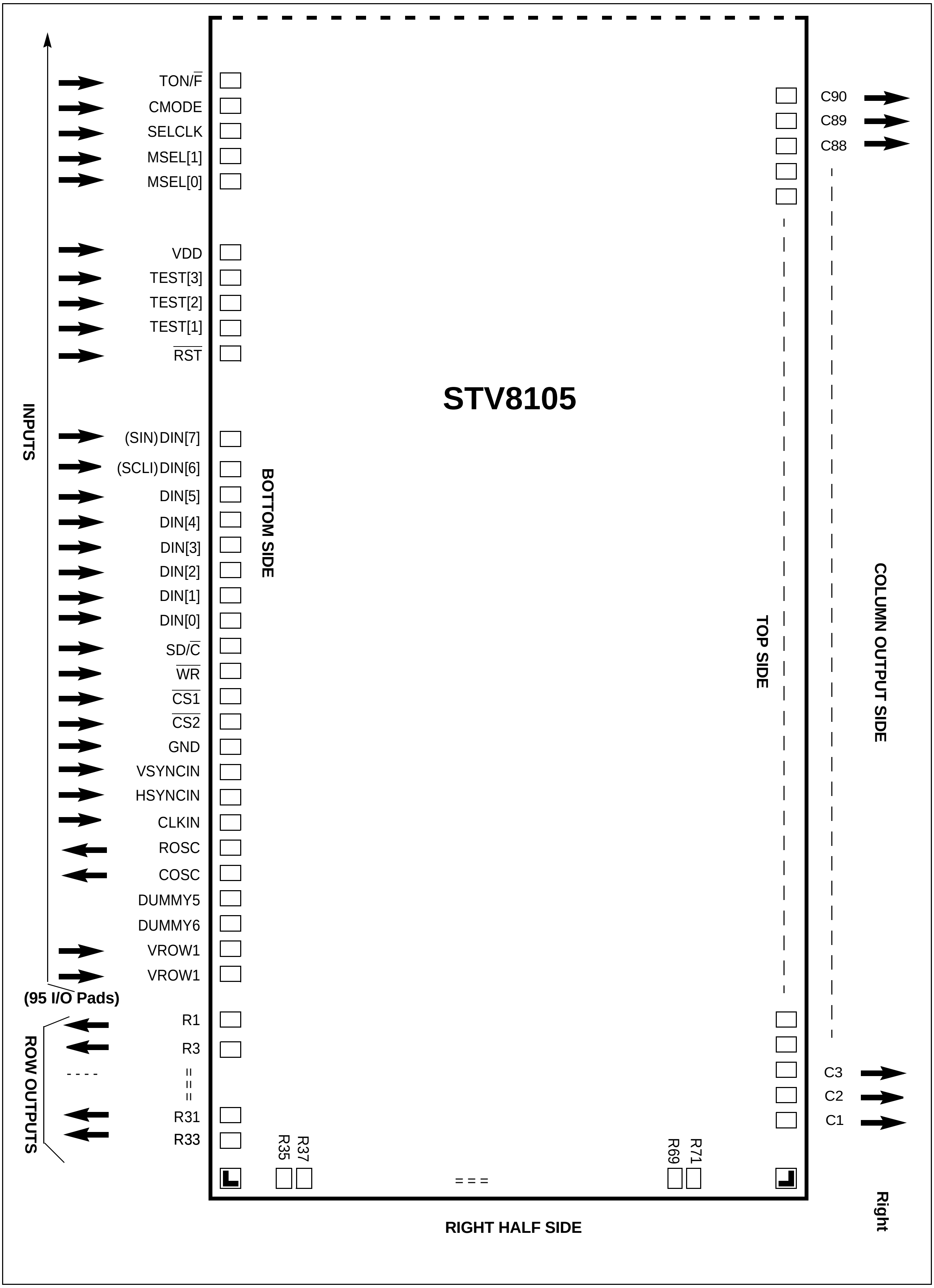


Figure 5: Pad Position (Bump-Side View)




INPUTS
VDRIVE
VDRIVE
GNDSENSE
GNDSENSE
GNDL
GNDL
GNDL
GNDL
GND
GND
GND
GND
VPRG
VPRG
VPRG
VPRG
VPP2
VPP2
VHSENSE
VHSENSE
VPP1
VPP1
VCOL2
VCOL2
VCOL1
VCOL1
DUMMY3
VREF2
VREF1
VDD
VDD
VDD
VDD
DUMMY4
GND
P/S
TON/F
BOTTOM SIDE
STV8105
+X
+Y
(0, 0)
TOP SIDE
C167
C166
C165
C92
C91
C90
COLUMN OUTPUT SIDE


INPUTS
TON/F
CMODE
SELCLK
MSEL[1]
MSEL[0]
VDD
TEST[3]
TEST[2]
TEST[1]
RST
(SIN)DIN[7]
(SCLI)DIN[6]
DIN[5]
DIN[4]
DIN[3]
DIN[2]
DIN[1]
DIN[0]
SD/C
WR
CS1
CS2
GND
VSYNCIN
HSYNCIN
CLKIN
ROSC
COSC
DUMMY5
DUMMY6
VROW1
VROW1
(95 I/O Pads)
ROW OUTPUTS
R1
R3
R31
R33
R35
R37
R69
R71
BOTTOM SIDE
STV8105
TOP SIDE
C90
C89
C88
C3
C2
C1
COLUMN OUTPUT SIDE
RIGHT HALF SIDE
Right

1.2 Pad Signal Description

Table 1: STV8105 Pad Description (Sheet 1 of 2)

Ball Name	Input/Output	Description
C1-C256	O	Column Driver Outputs
R1-R72	O	Row Driver Outputs
CLKIN	I	External RC/Crystal connection or Clock input
CMODE	I	Mode Select: “H”: Dual color mode “L”: Single color mode
COSC	O	External RC oscillator, capacitor connection
$\overline{CS1}$	I	Chip Select 1 Input (Master Device Chip Select)
$\overline{CS2}$	I	Chip Select 2 Input (Slave Device Chip Select)
$\overline{CSOUT1}$	O	Chip Select 1 Output
$\overline{CSOUT2}$	O	Chip Select 2 Output
DIN[5:0]	I	P/$\overline{S}$=”H”: Parallel Data Input P/$\overline{S}$=”L”: Not used. Fix to “H” or “L”
DIN[6] (SCLI)	I	P/$\overline{S}$=”H”: Parallel Data Input P/$\overline{S}$=”L”: Serial Clock Input
DIN[7] (SIN)	I	P/$\overline{S}$=”H”: Parallel Data Input P/$\overline{S}$=”L”: Serial Data Input
DOUT[5:0]	O	P/$\overline{S}$=”H”: Parallel Data Output P/$\overline{S}$=”L”: Non Connection
DOUT[6] (SCLO)	O	P/$\overline{S}$=”H”: Parallel Data Output P/$\overline{S}$=”L”: Serial Clock Output
DOUT[7] (SOUT)	O	P/$\overline{S}$=”H”: Parallel Data Output P/$\overline{S}$=”L”: Serial Data Output
GND	Supply	Analog and Digital ground
GNDL	Supply	Column and Row driver ground
GNDSENSE	Supply	Ground for DC/DC Converter
HSYNCIN	I	Horizontal SYNC Input
HSYNCOUT	O	Horizontal SYNC Output
ISENSE	I	Over current sense signal for external switching MOS transistor
MSEL[0]	I	Master /Slave Select: “H”: Master “L”: Slave
MSEL[1]	I	Primary /Secondary Select: “H”: Primary “L”: Secondary
P/$\overline{S}$	I	Parallel Interface or Serial Interface Select
RCTRLA	O	Reserved for Test
RCTRLB	O	Reserved for Test
ROSC	O	External RC oscillator, resistor connection or Crystal connection

Table 1: STV8105 Pad Description (Sheet 2 of 2)

Ball Name	Input/Output	Description
ROWDATA	O	Reserved for Test
$\overline{\text{RST}}$	I	System Reset Input
SCLKOUT	O	System Clock Output
SD/$\overline{\text{C}}$	I	Display Data or Command: SD/$\overline{\text{C}}$="H": Display Data SD/$\overline{\text{C}}$="L": Command
SD/$\overline{\text{C}}$OUT	O	SD/$\overline{\text{C}}$ Output
SELCLK	I	"H": An internal oscillator (if MSEL[0]="1") "L": External clock used
TEST[2:1]	I	Test Mode Select: "H": Test Mode OFF (internal pull-up) "L": Reserved modes
TEST[3]	I	Reserved (internal pull-up)
TON/$\overline{\text{F}}$	I	DC/DC Converter Mode Select "H": PFM constant t_{ON} mode "L": PWM constant switching frequency mode
VCOL1	Supply	Odd column supply
VCOL2	Supply	Even column supply
VCOMP	I/O	Compensation pad for DC/DC converter, constant frequency PWM mode
VDC	Supply	Supply for gate drive output buffer
VDD	Supply	Analog/Digital low-voltage controller supply
VDRIVE	O	Gate drive for external switching MOS transistor
VHSENSE	I	VH sense input
VPP1	Supply	Odd column driver power supply
VPP2	Supply	Even column driver power supply
VPRG	Supply	Non-volatile OTP memory program power supply
VREF1	I/O	Reference Voltage 1
VREF2	I/O	Reference Voltage 2
VROW1	Supply	Odd row driver supply
VROW2	Supply	Even row driver supply
VSENSE	I	Feedback signal
VSYNCIN	I	Vertical SYNC Input
VSYNCOUT	O	Vertical SYNC Output
$\overline{\text{WR}}$	I	Display Data and Command Write Pulse
$\overline{\text{WR}}$OUT	O	Write Pulse Output
DUMMY1,2,5,6	O	Reserved for Test
DUMMY3,4	I/O	Reserved for Test

1.3 Lead Pad Reference Chart

The reference for the following tables is the center of the die (X = 0.0, Y = 0.0)

Table 2: Top Side (from left to right)

Lead Pad Name	Pad Placements (center), µm		Pad Dimensions, µm	
	X	Y	X	Y
C256	TBD	TBD	TBD	TBD
-----	-------	-------	-------	-------
C2	TBD	TBD	TBD	TBD
C1	TBD	TBD	TBD	TBD

Table 3: Right Side (from top to bottom)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
R71	TBD	TBD	TBD	TBD
-------	-------	-------	-------	-------
R37	TBD	TBD	TBD	TBD
R35	TBD	TBD	TBD	TBD

Table 4: Bottom Side (from right to left)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
R33	TBD	TBD	TBD	TBD
-------	-------	-------	-------	-------
R1	-------	-------	-------	-------
VROW1	-------	-------	-------	-------
-------	-------	-------	-------	-------
-------	-------	-------	-------	-------
VROW2	-------	-------	-------	-------
R2	-------	-------	-------	-------
-------	-------	-------	-------	-------
R34	-------	-------	-------	-------

Table 5: Left Side (from bottom to top)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
R36	TBD	TBD	TBD	TBD
R38	TBD	TBD	TBD	TBD
-------	-------	-------	-------	-------
R72	TBD	TBD	TBD	TBD

1.4 Mechanical Dimensions

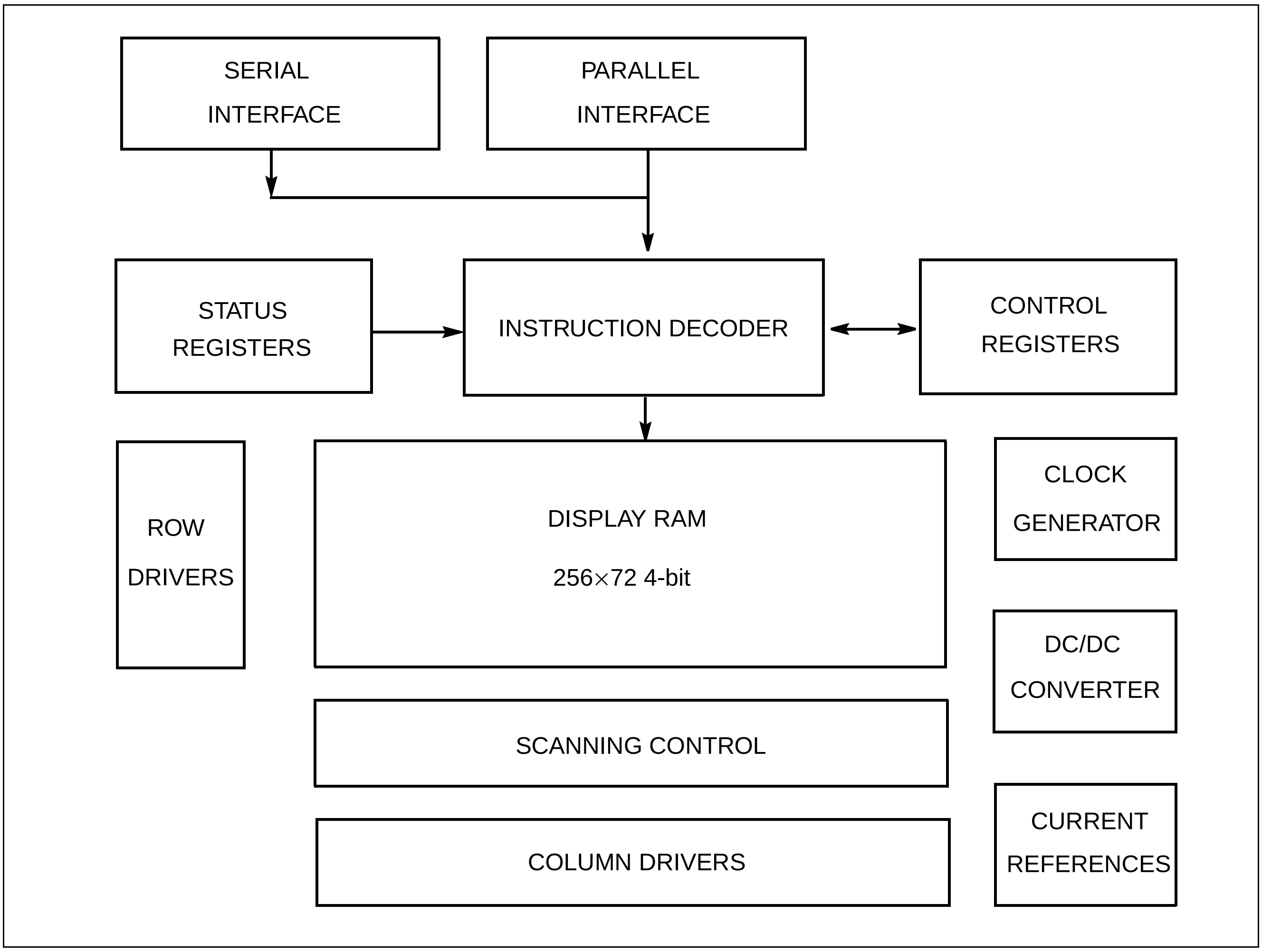
Table 6: Mechanical Dimensions

Description	Dimension
Die Size (mm x mm)	12.5 x 1.72
Pad Pitch (µm)	45 - 80
Pad Size (µm)	TBD
Pad Height (µm)	20
Wafer Thickness (µm)	450
Bump Size (µm)	46 x 66 and13 x 66
Bump Characteristics	gold, electrolytic
Bump Hardness	30-80Hv

1.5 Functional Description

The architecture of the STV8105 provides all of the functions required to drive OLED displays. The block diagram below gives an overview of the different on-chip components, embedded functions and their links.

Figure 6: STV8105 Block Diagram



The following rules are used in this datasheet to describe bit, bit-fields and registers:

- ROWDRVSEL is the name of a register,

- RDIR.ROWDRVSEL is the RDIR bit of register ROWDRVSEL,

- RMODE.ROWDRVSEL is the RMODE bit-field of register ROWDRVSEL.

Refer to Chapter 13: Command and Control Registers on page 64 for details of the various registers.

The various functions of the STV8105 are described in the following sections, starting with the bus interfaces.

2 Bus Interfaces

The parallel interface and serial interface are selected using a P/$\overline{S}$ pad.

The parallel interface is active when P/$\overline{S}$ ="H"; the serial interface when P/$\overline{S}$ ="L".

The serial input pads SIN and SCLI are shared with DIN7 and DIN6, respectively.

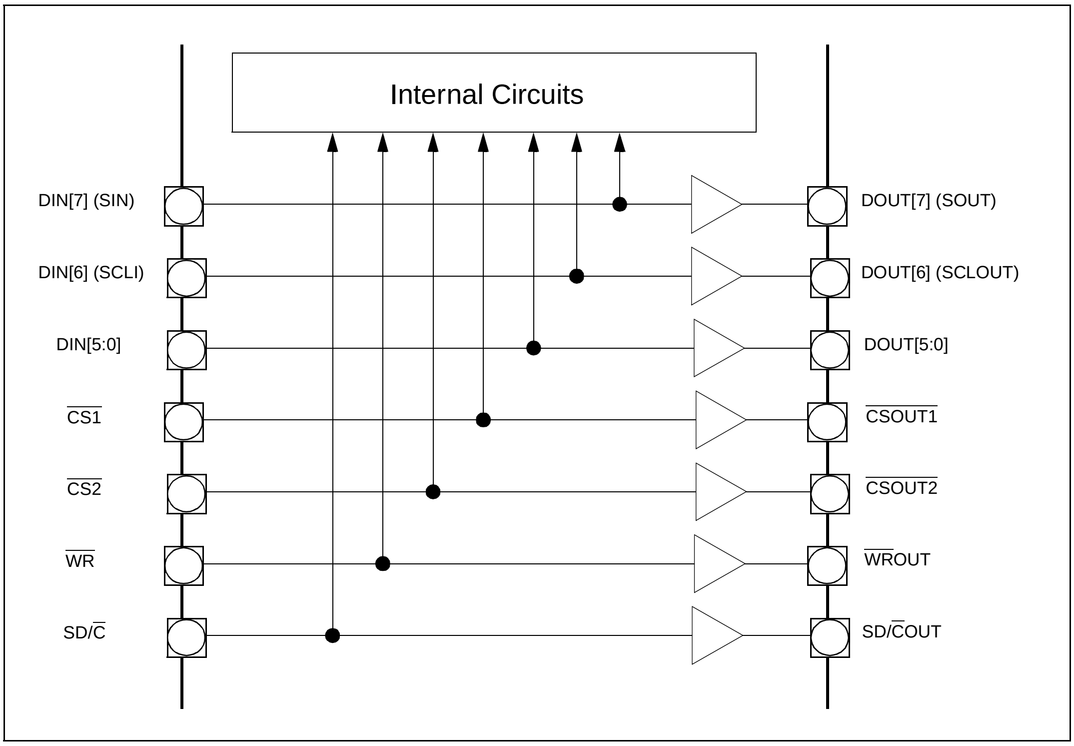
Buffered versions of the serial signals, for cascading purposes, are output on pads SOUT and SCLO and shared with DOUT7 and DOUT6, respectively.

The parallel interface pads DIN[7:0], $\overline{CS1}$, $\overline{CS2}$ and $\overline{WR}$ are buffered and sent out on DOUT[7:0], $\overline{CSOUT1}$, $\overline{CSOUT2}$, and $\overline{WROUT}$.

$\overline{CS1}$ and $\overline{CSOUT1}$ are chip select signals for the Primary-Master and Secondary-Master devices.

$\overline{CS2}$ and $\overline{CSOUT2}$ are chip select signals for the Primary-Slave and Secondary-Slave devices.

Figure 7: Buffering of Bus Interface Signals



2.1 Interface Sequence

After Reset or Power ON, an interface is in the state of waiting for a Command Address and Display RAM Data.

After receiving the Command Address, the interface is in the state of waiting for Command Data.

When Command Data is received while in the receive Command Data state, the interface returns to the receive Command Address state.

When Display RAM Data is received while in the receive Command Data state, the interface also returns to the receive Command Address state.

When the Serial Interface is selected, the output buffer for the interface signals is cleared when $\overline{CS1}$ and $\overline{CS2}$ are both "High".

2.2 Parallel Interface

The parallel interface is active when pad P/$\overline{S}$ is "High".

When writing parallel data, the $\overline{WR}$ pad is asserted while $\overline{CS1}$ and $\overline{CS2}$ are both "Low".

Data is interpreted as a command if SD/$\overline{C}$ is "Low"; it is interpreted as Display RAM data if SD/$\overline{C}$ is "High".

When transmitting a command, the command address is sent first followed by command data.

A command is decided by a 2-byte access: a command code followed by a data byte.

When there is a Display RAM access with SD/$\overline{C}$ set “High” but without respecting the “2-byte nature” of a command, the STV8105 enters the state where it is waiting for a Command Address.

Figure 8: Parallel Interface

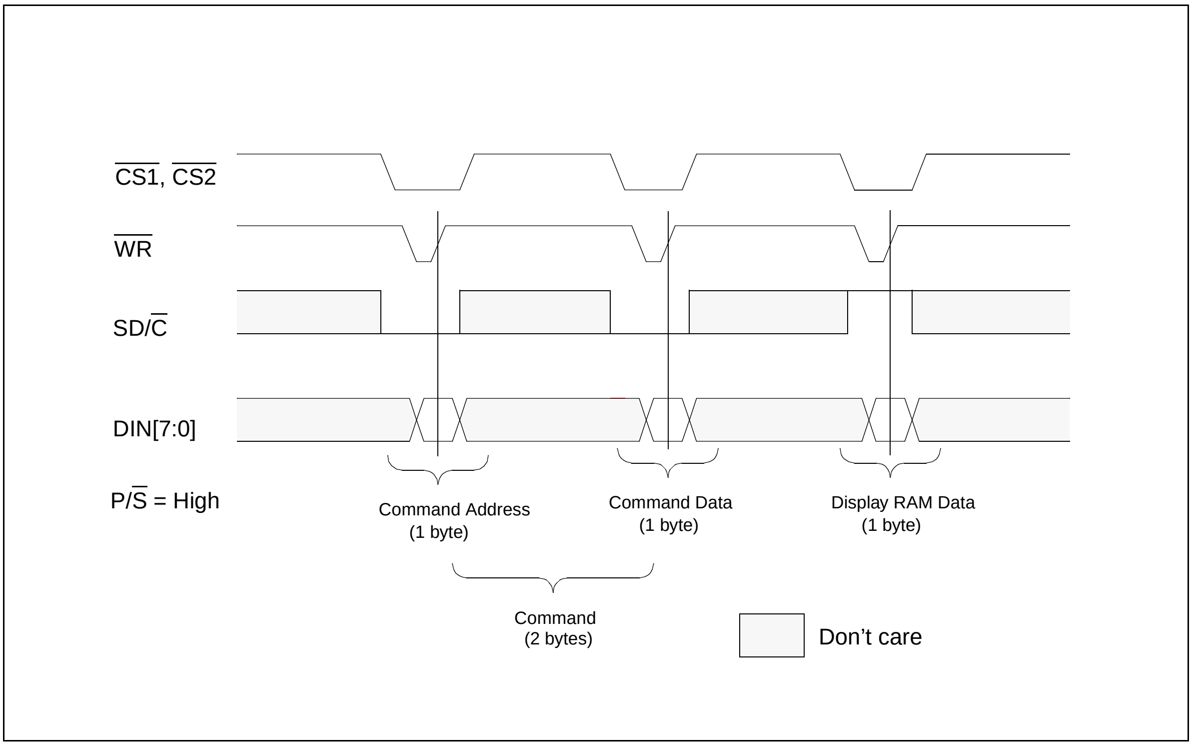


Figure 9: 8-bit Parallel Interface Timing Diagram

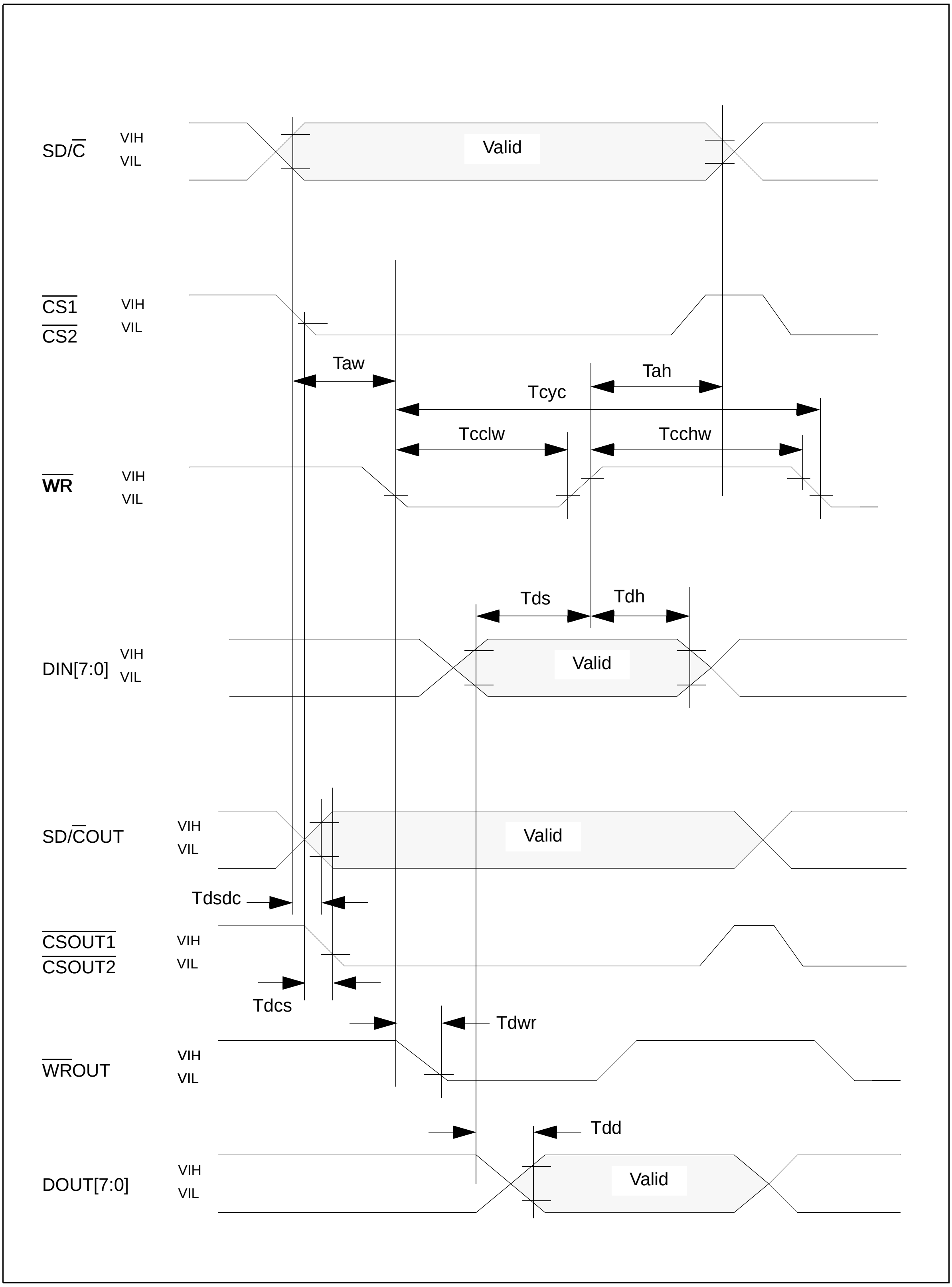


Table 7: 8-bit Parallel Interface Timing

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Tah	Address Hold Time	$\overline{\text{WR}}$	10			ns
Taw	Address Setup Time	$\overline{\text{WR}}$	0			ns
Tcyc	System Cycle Time	$\overline{\text{CS1}}$, $\overline{\text{CS2}}$	200			ns
Tcclw	Write Pulse Width	$\overline{\text{WR}}$	60			ns
Tds	Data Setup Time	DIN[7:0]	60			ns
Tdh	Data Hold Time	DIN7:0]	10			ns
Tdsdc	SD/C Output Delay	SD/$\overline{\text{C}}$OUT			30	ns
Tdcs	CS Output Delay	$\overline{\text{CSOUT1}}$, $\overline{\text{CSOUT2}}$			30	ns
Tdwr	WR Output Delay	$\overline{\text{WR}}$OUT			30	ns
Tdd	DATA Output	DOUT[7:0]			30	ns

2.3 Serial Interface

The serial interface is active when P/$\overline{\text{S}}$ is "Low".

Serial data is written in using DIN[7] (SIN) and DIN[6] (SCLI) while $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are both "Low".

Data is interpreted as a command if SD/$\overline{\text{C}}$ is "Low"; it is interpreted as Display RAM data if SD/$\overline{\text{C}}$ is "High".

DIN[5:0] are not used; they should be tied either “High” or “Low”.

Figure 10: Serial Interface

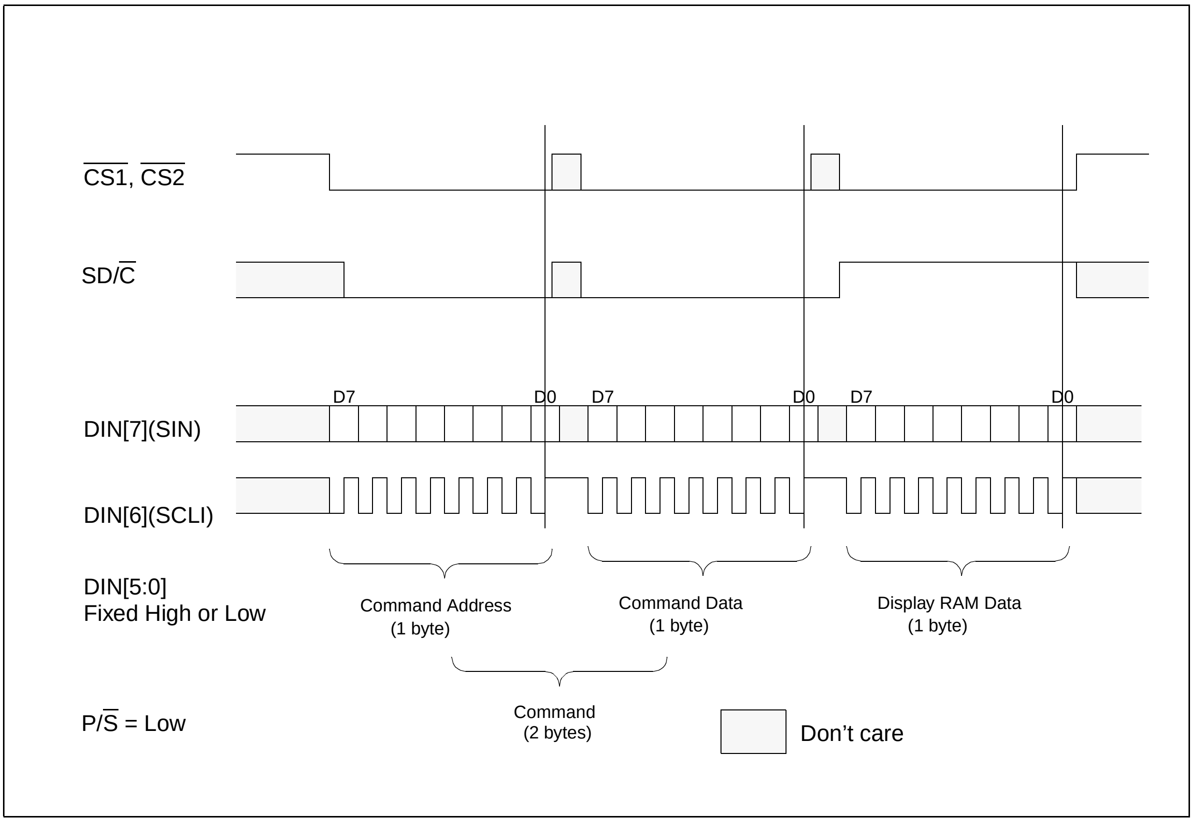


Figure 11: 4-wire Serial Interface Timing Diagram

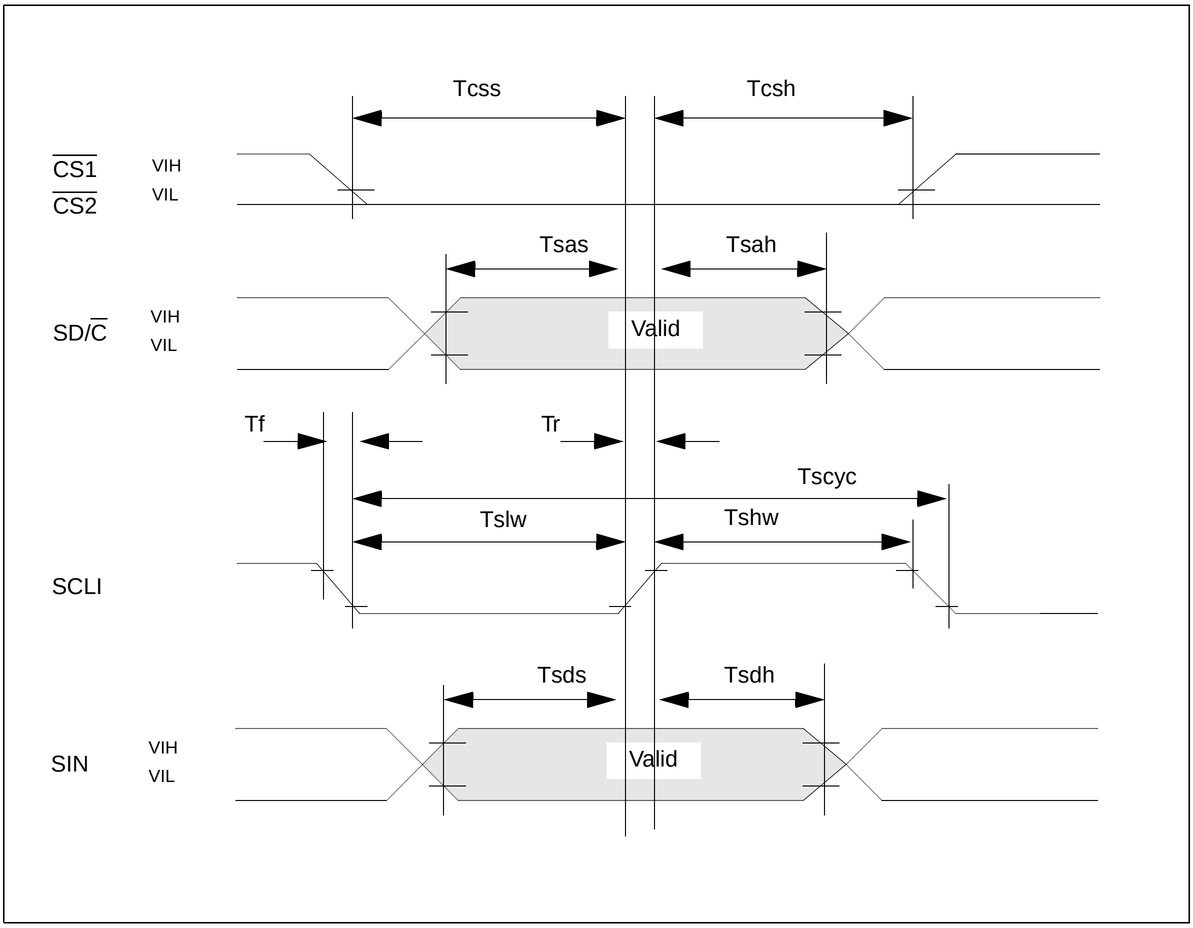


Table 8: 4-wire Serial Interface Timing

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Tscys	Serial Clock Cycle		200			ns
Tshw	Pulse Width (High)		90			ns
Tslw	Pulse Width (Low)		90			ns
Tsas	Address Setup Time		20			ns
Tsah	Address Hold Time		20			ns
Tsds	Data Setup Time		20			ns
Tsdh	Data Hold Time		20			ns
Tcss	CS-SCL Time		20			ns
Tcsh	CS-SCL Time		20			ns

2.4 Master/Slave Connection

Figure 12 below shows an example connection between two STV8105 ICs for Master/Slave mode.

Figure 12: Master/Slave Mode

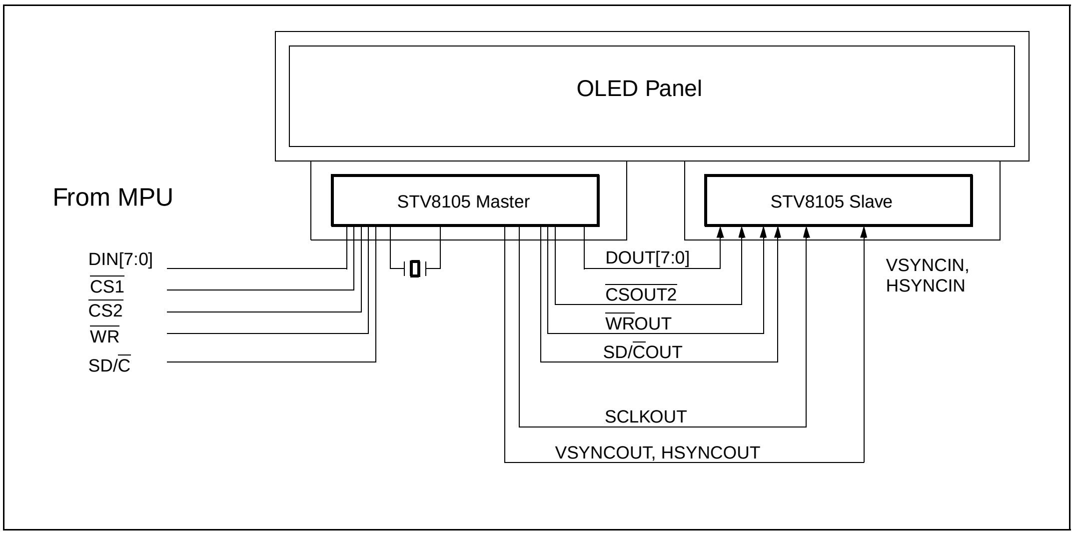


Figure 13: External IC Interface Timing Diagram

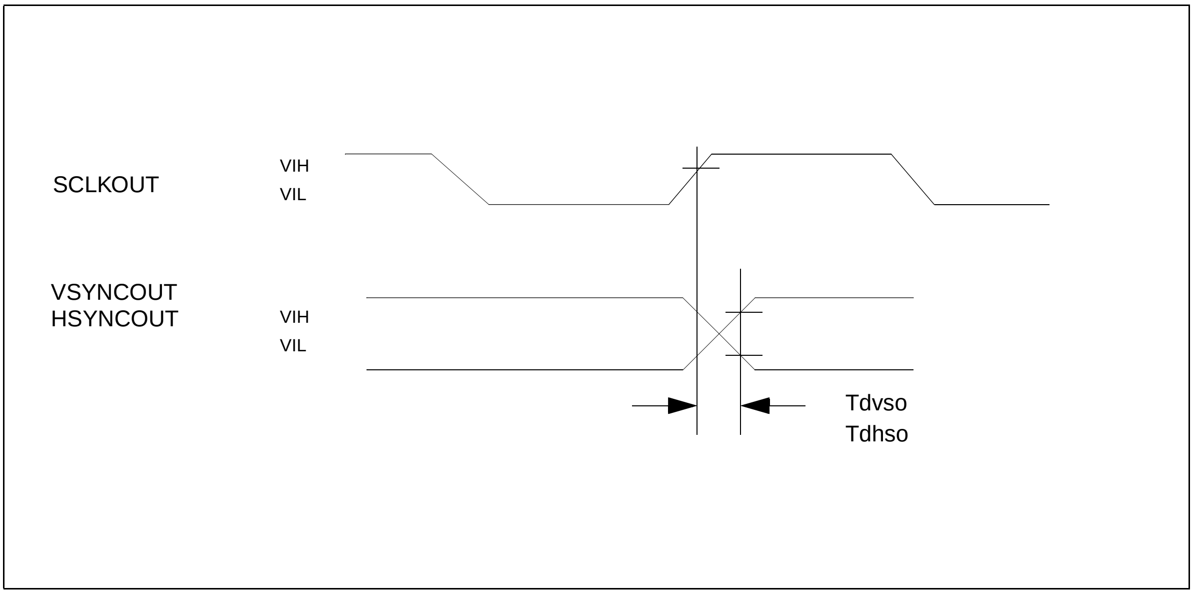


Table 9: External IC Interface Timing

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Tdvso	VSYNCOUT Delay				20	ns
Tdhso	HSYNCOUT Delay				20	ns

3 Display RAM

The STV8105 contains a Dual Port, 256 × 72 x 4-bit Display RAM. As shown in Figure 14 below, Port A is for write only; Port B, read only.

It is possible to access any location thanks to X and Y, programmable pointers with ranges corresponding to the selected display mode.

The X address is specified with the command RAMXSTART, the Y address with RAMYSTART.

The X and Y addresses can be automatically incremented with bits YINC and XINC of the GSADDINC command. The GSMODE bit-field of this command is also used to select the display mode and gray scale. See Section 13.2 for details.

Depending on the selected display mode, one, two or four pictures can be stored in the Display RAM, and one or two colors can be controlled:

16 level gray scale mode: 256 × 72 × 4 bits - 1 picture - one/two colors

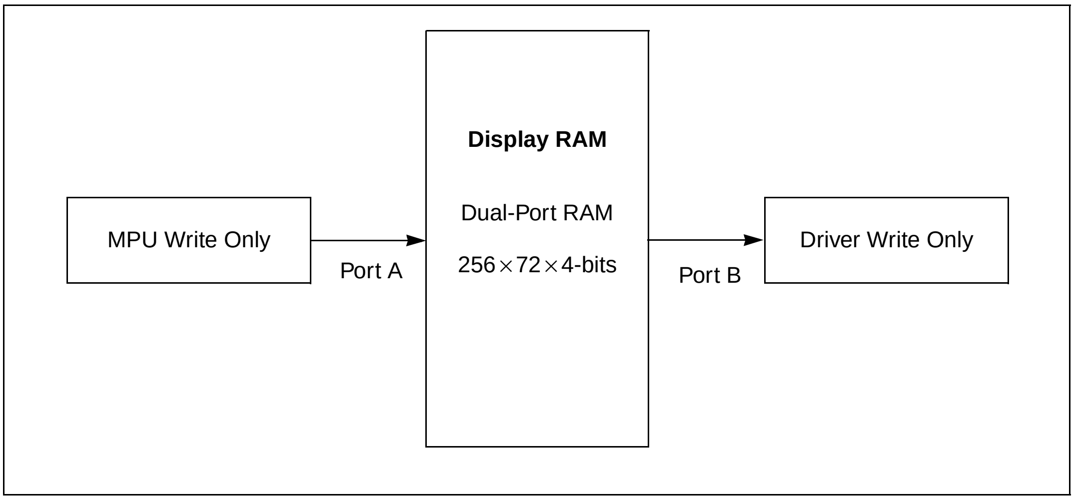
4 level gray scale mode: 256 × 72 × 2 bits - 2 pictures - one/two colors

64 level gray scale mode 1: 128 × 72 × 6 bits - 1 picture - one color

64 level gray scale mode 2: 256 × 36 × 6 bits - 1 picture - one color

Black and White, monochrome mode: 256 × 72 × 1 bit - 4 pictures - one/two colors

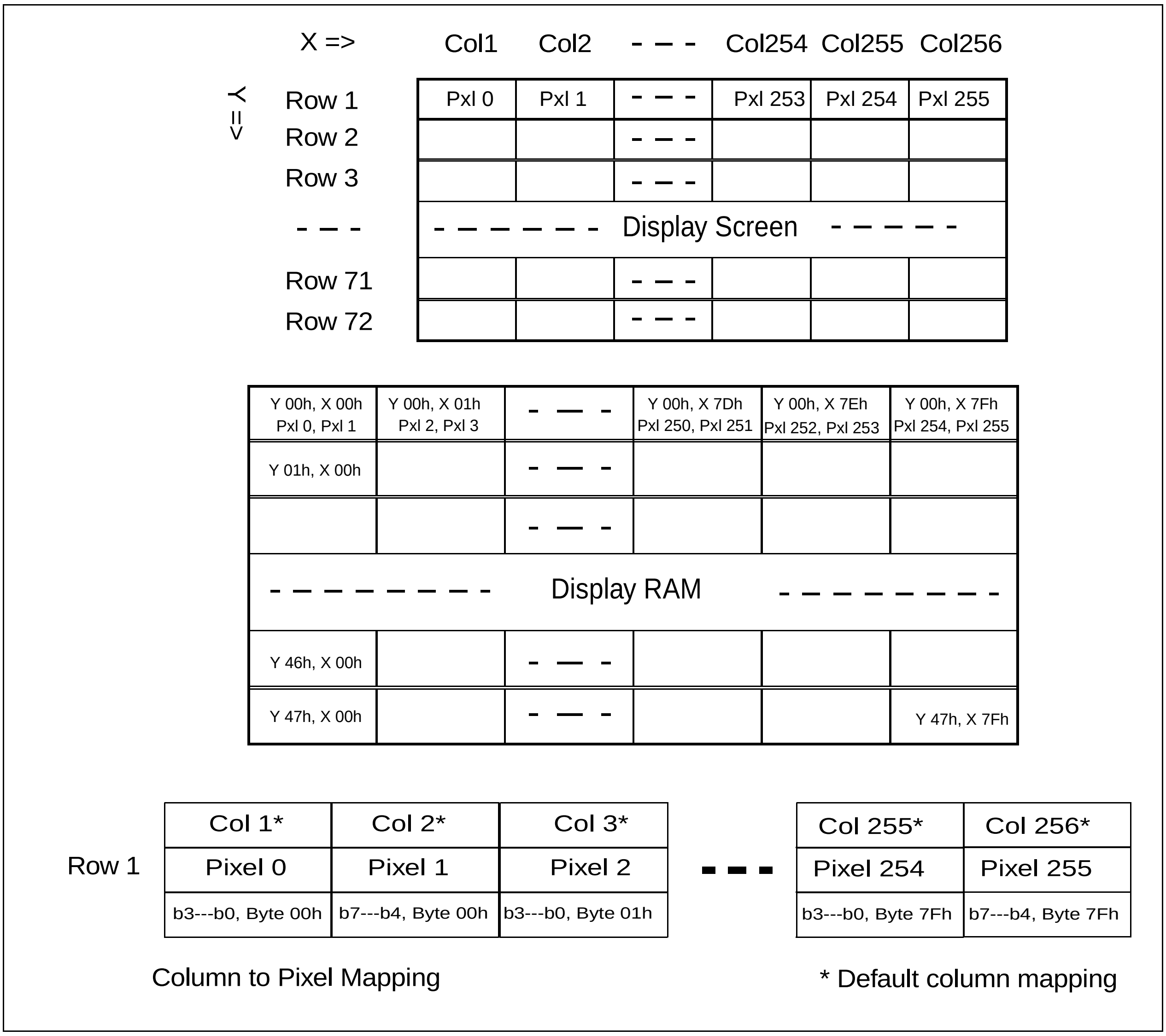
Figure 14: Dual Port Display RAM Composition



3.1 16 Level Gray Scale Mode Memory Map

In this mode, the picture has 256 x 72 pixels, and the gray scale of each pixel is defined by the corresponding 4-bit value stored in Display RAM. This mode is selected using field GSMODE of the GSADDINC command. Only one picture can be stored in the Display RAM. The range of the address pointers is 00h to 7Fh for X and 00h to 47h for Y. One byte loaded in Display RAM contains data for two pixels.See Section 13.2 for details. The “two” color mode can be used; see Section 9.1: Color Selection Modes for details.

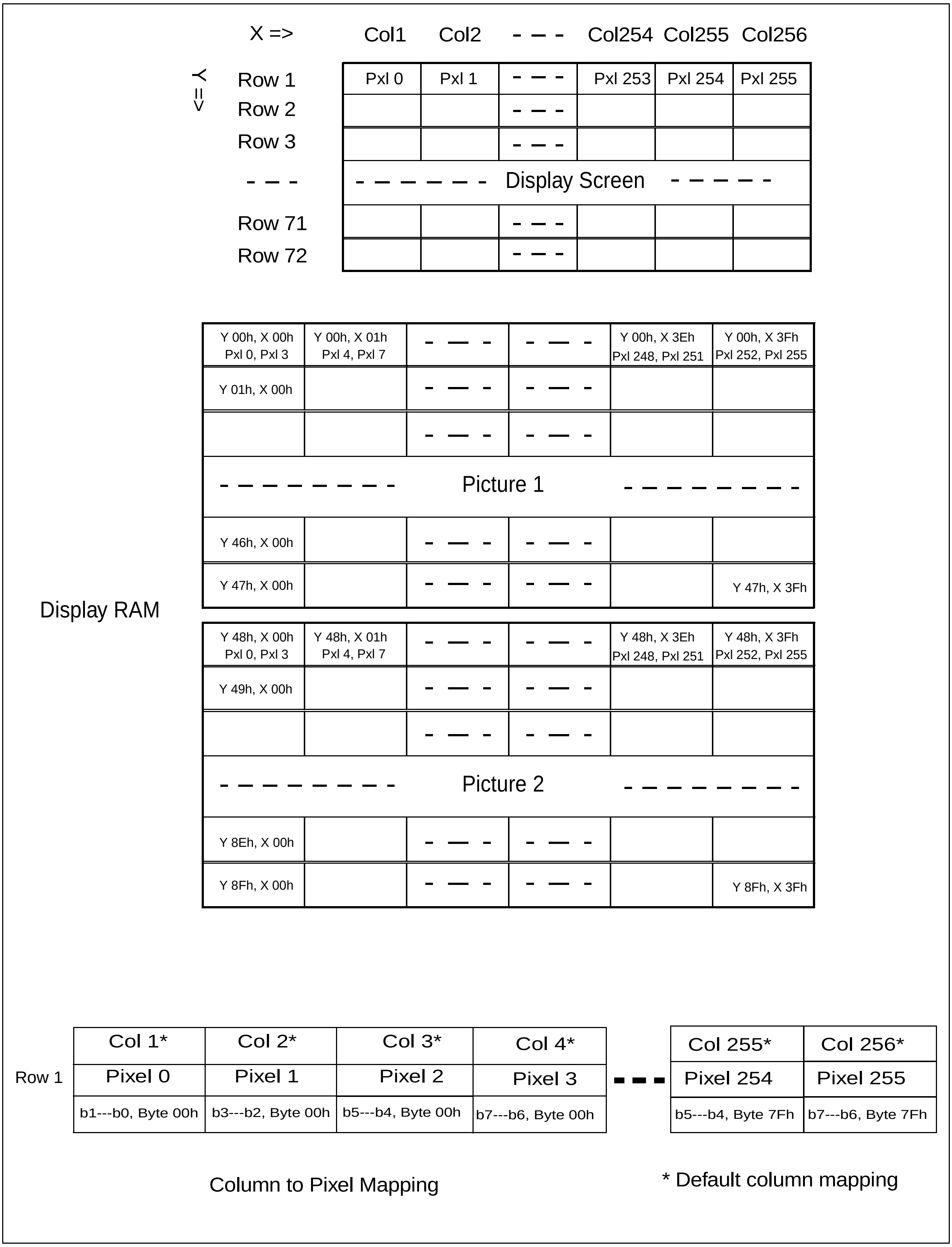
Figure 15: 16 Level Gray Scale Mode - Display RAM Organization



3.2 4 Level Gray Scale Mode Memory Map

In this mode, the picture has 256 x 72 pixels. The gray scale of each pixel is defined by the corresponding 2-bit value stored in Display RAM. This mode is selected using field GSMODE of the GSADDINC command. Two pictures can be stored in the Display RAM. The range of the address pointers is 00h to 3Fh for X and 00h to 8Fh for Y. One byte loaded in Display RAM contains data for 4 pixels. See Figure 16 for details. The “two” color mode can be used, see Section 9.1: Color Selection Modes for details.

Figure 16: 4 Level Gray Scale Mode - Display RAM Organization

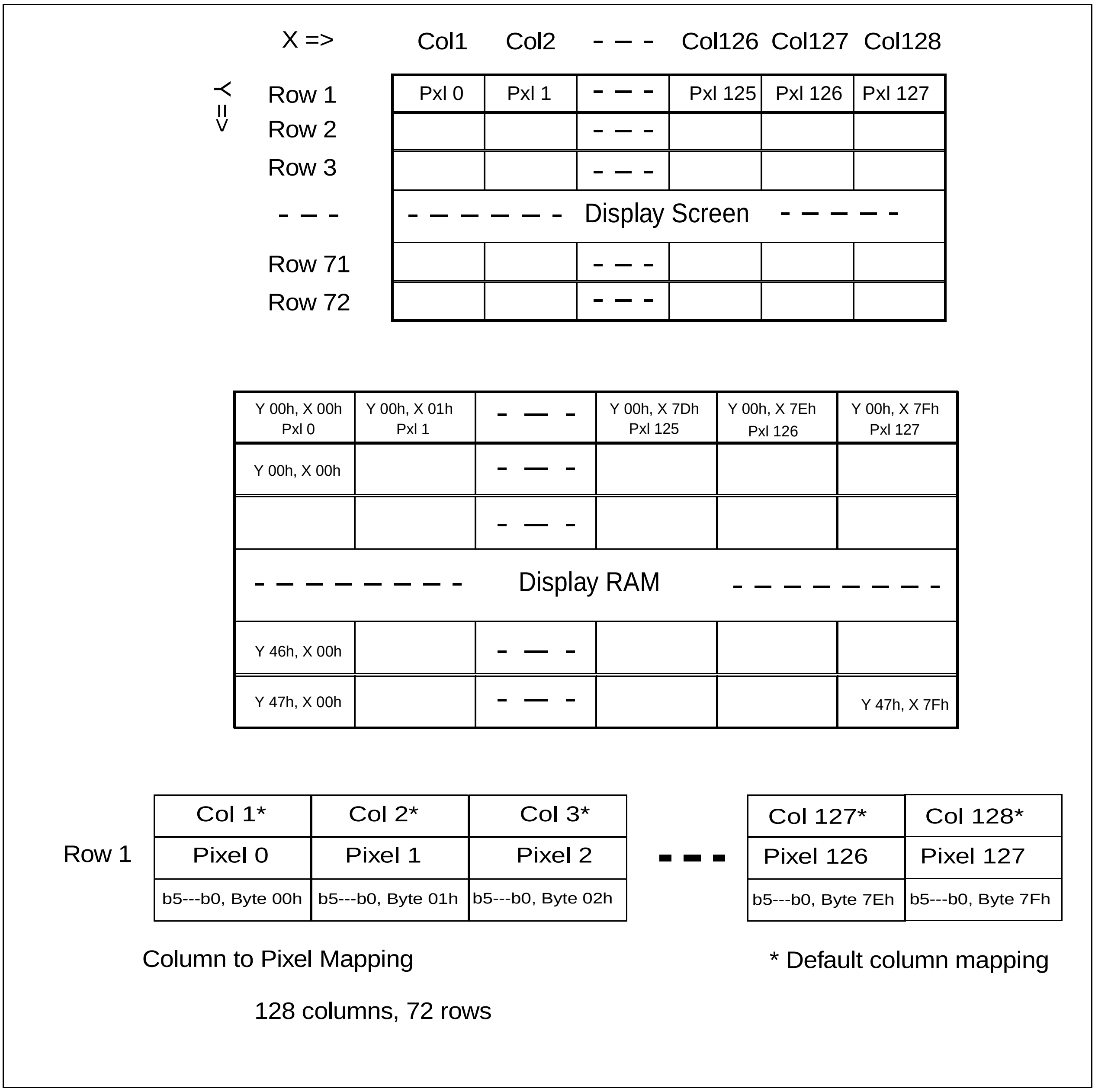


3.3 64 Level Gray Scale Mode 1 Memory Map

In this mode, the picture has 128 x 72 pixels. The gray scale of each pixel is defined by the corresponding 6-bit value stored in Display RAM. This mode is selected using field GSMODE of the GSADDINC command. Only one picture can be stored in the Display RAM. The range of the address pointers is 00h to 7Fh for X and 00h to 47h for Y. One byte loaded in the Display RAM contains data for one pixel.

In this mode, column outputs C_{n+1} and C_n, must be connected together. It is not possible to use the “two” color mode, see Section 9.1: Color Selection Modes for details. For more information on using this mode, refer to the description of command GSADDINC in Section 13.2.

Figure 17: 64 Level Gray Scale Mode 1 - Display RAM Organization

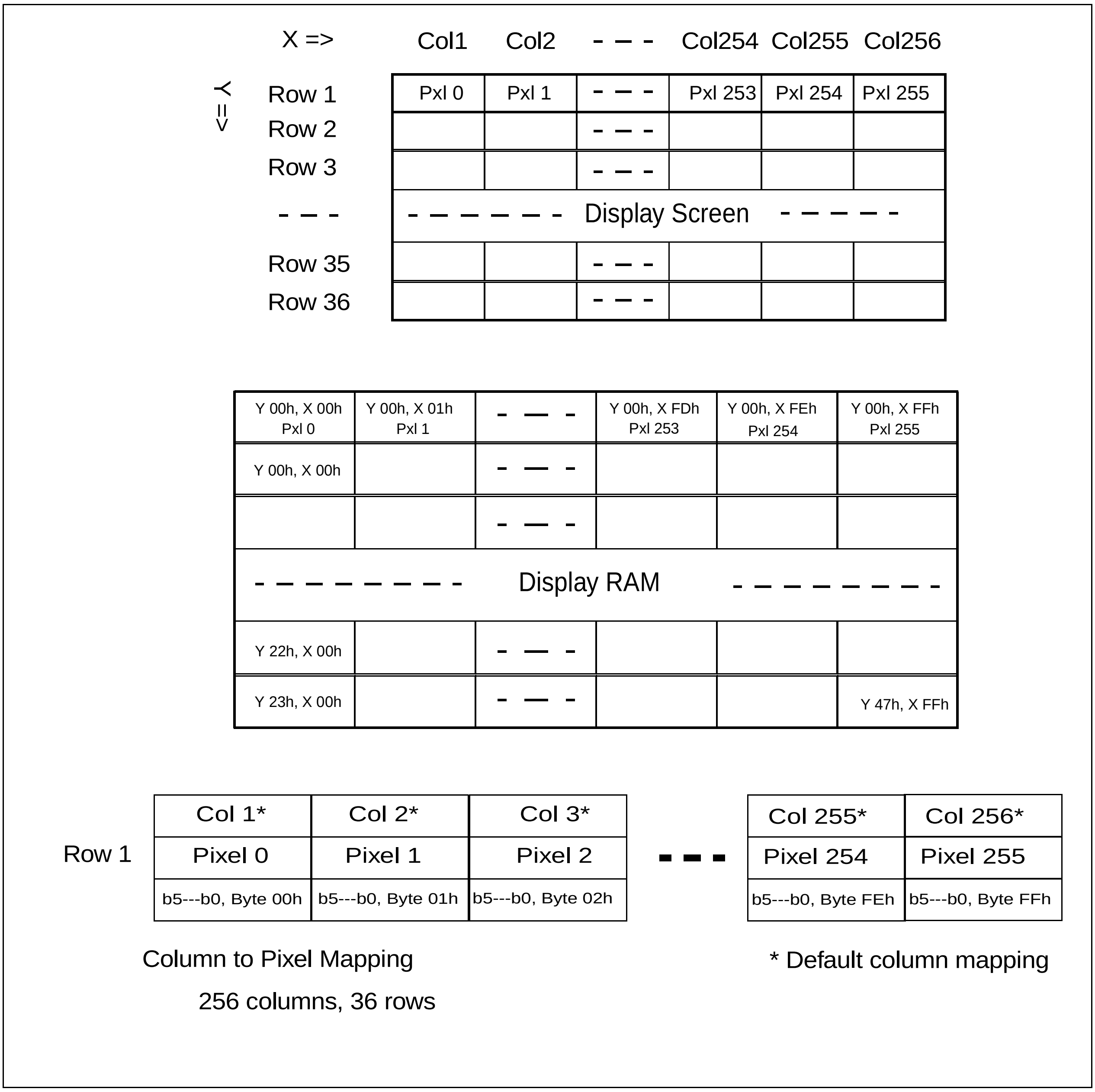


3.4 64 Level Gray Scale Mode 2 Memory Map

In this mode, the picture has 256 x 36pixels, the gray scale of each pixel is defined by the corresponding 6-bit value stored in Display RAM. This mode is selected using field GSMODE of the GSADDINC command. Only one picture can be stored in the Display RAM. The range of the address pointers is 00h to FFh for X, 00h to 23h for Y. One byte loaded in the Display RAM contains data for one pixel.

The “two” color mode cannot be used, see Section 9.1: Color Selection Modes for detail. For more information on using this mode, refer to the description of command GSADDINC in Section 13.2.

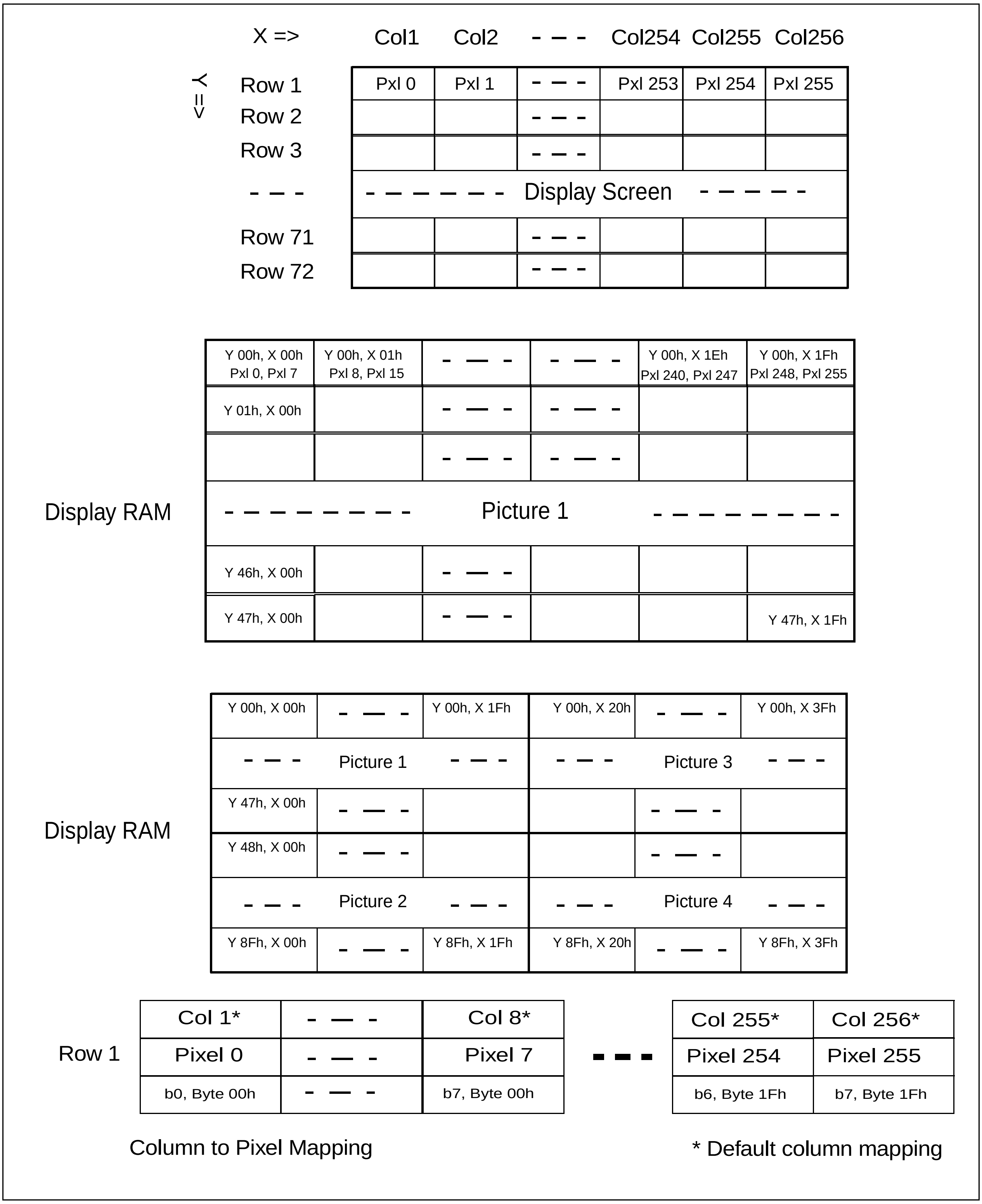
Figure 18: 64 Level Gray Scale Mode 2 - Display RAM Organization



3.5 Monochrome Mode Memory Map

In this mode, the picture has 256 x 72 pixels, and each pixel is black or white depending on the corresponding 1-bit value stored in Display RAM. This mode is selected using field GSMODE of the GSADDINC command. Four pictures can be stored in the Display RAM. The “two” color mode can be used, see Section 9.1: Color Selection Modes for details. The range of the address pointers is 00h to 3Fh for X, 00h to 8Fh for Y. One byte loaded in Display RAM contains data for eight pixels. See Section 13.2.

Figure 19: Monochrome Mode - Display RAM Organization

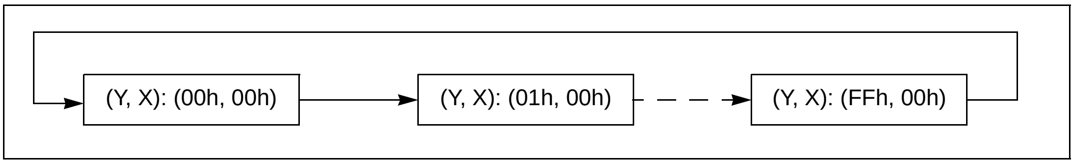


3.6 Display RAM Loading

Four increment modes can be selected using the XINC and YINC bit of the GSADDINC command as described below:

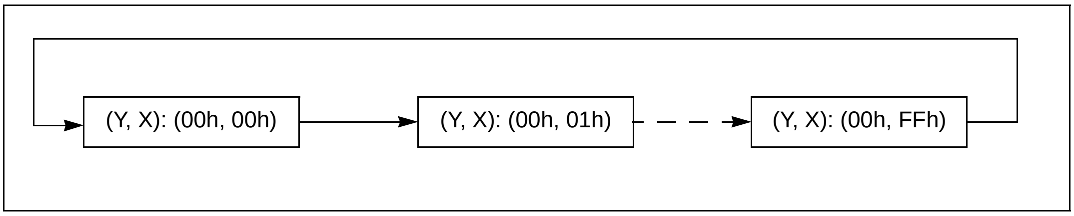
- If bits YINC and XINC of command GSADDINC are both “Low”, there is no increment of the X and Y Display RAM addresses.
- If YINC="High” and XINC="Low”, then only the Y address of the Display RAM is incremented as shown is Figure 20.

Figure 20: Automatic Increment of Display RAM Y Address



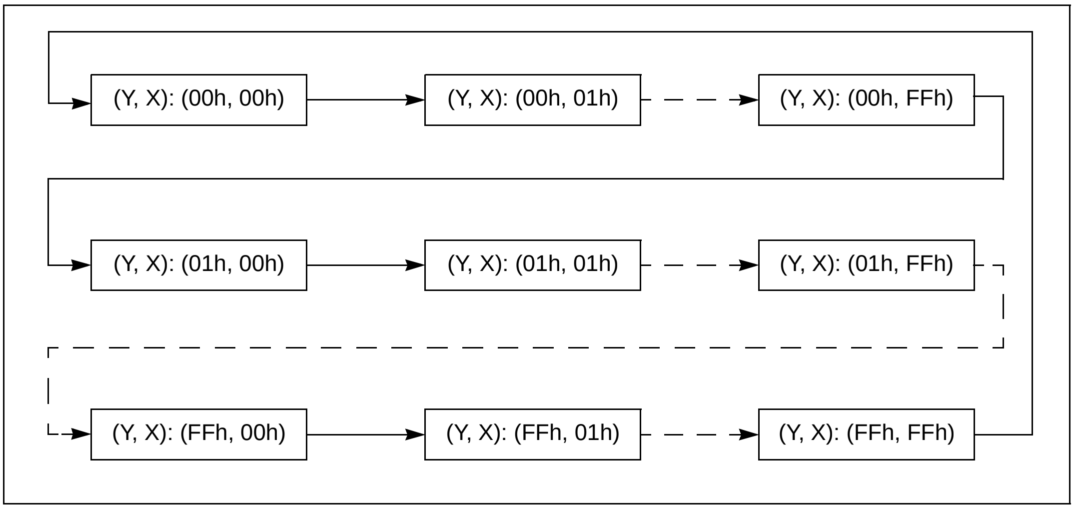
- Conversely, if YINC="Low” and XINC="High”, then only the X address of the Display RAM is incremented, Figure 21.

Figure 21: Automatic Increment of Display RAM X Address



- If YINC and XINC are both "High”, then both the X and Y addresses of the Display RAM are incremented. If the X address reaches its limit of FFh, then only Y address will be incremented, Figure 22.

Figure 22: Automatic Increment Both X and Y Display RAM Addresses



It is the software designer’s responsibility to keep the X and Y address pointers consistent with the selected display mode by mainly using automatic incrementation to avoid writing data in areas that are not read.

4 Dot-Matrix Display

The STV8105 can display pictures of different resolutions with different shades or levels of gray as described below:

16 level grayscale mode: 256 × 72 × 4 bits

4 level grayscale mode: 256 × 72 × 2 bits

64 level grayscale mode 1: 128 × 72 × 6 bits

64 levels grayscale mode 2: 256 × 36 × 6 bits

Black and White, monochrome mode: 256 × 72 × 1 bit

The selected picture in Display RAM can be displayed in four different ways thanks to bits VTUR and HTUR of the command DOTMTRXDIR (command code 11h):

- bit VTUR selects the vertical display direction versus Display RAM contents, Figure 23.
- bit HTUR selects the horizontal display direction versus Display RAM contents, Figure 24. Bit HTUR applies when writing data into the Display RAM. To get effective horizontal picture mirroring after changing the HTUR bit, the picture must be re-written into Display RAM.

The display is turned on when bit DISPON of command DCTRL (10h) is set; bit DISPON is cleared by default on reset or during power-on reset.

Figure 23: Invert Image - Vertical Direction

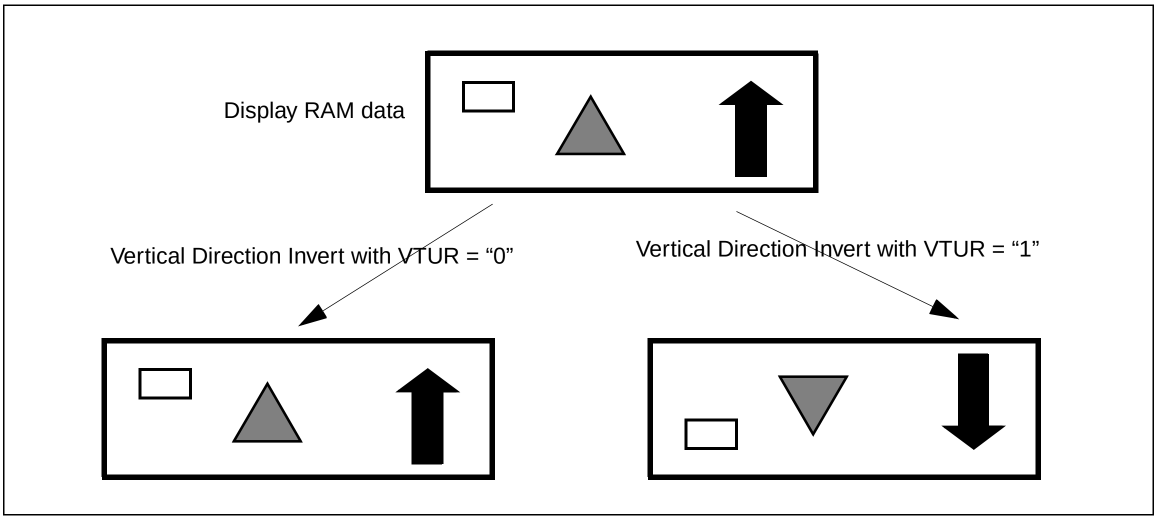
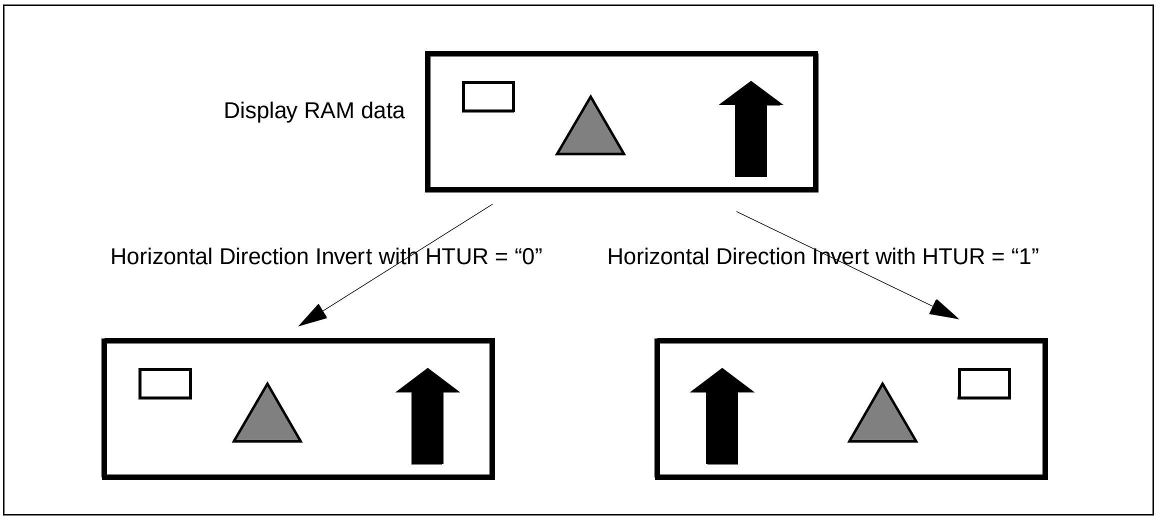


Figure 24: Invert Image - Horizontal Direction



The STV8105 can scan a reduced number of rows by programming the SCLN bit-field of command DOTMTRXSCAN (12h). See Section 13.2 for details regarding commands DCTRL, DOTMTRXDIR and DOTMTRXSCAN.

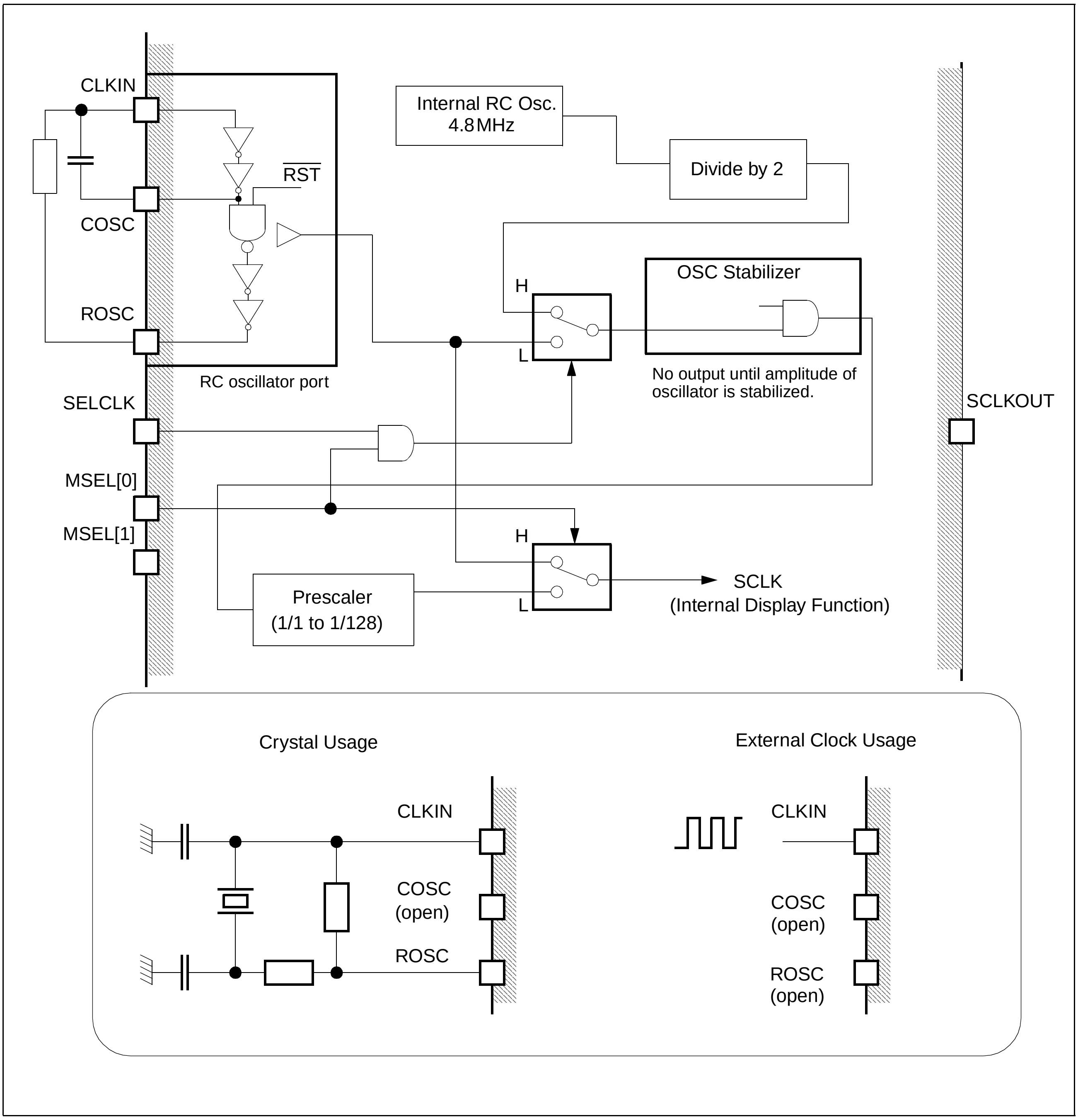
5 Clock Generation

The STV8105 has two on-chip oscillator circuits to generate the internal clock SCLK. One circuit is dedicated to an external crystal or RC network. It is also possible to source an external clock on pad CLKIN directly. A second RC oscillator is fully integrated. It does not require any external components and provides a reference clock of 4.8MHz, typ. The clock source is selected using input pads SELCLK and MSEL[0].

The internal clock SCLK is buffered and sent to output pad SCLKOUT for slave devices.

The oscillator frequency can be divided by a factor of 2^N, where integer N can range from 0 to 7, by programming the SDIV bit-field of command SCLKDIV. This sets up a “prescaler” ratio of from 1/1 to 1/128; see Figure 25. For details regarding the SCLKDIV command, see Section 13.2: Command Details Ordered by Command Code.

Figure 25: Clock Generation



6 Master/Slave and Primary/Secondary Operation

Master/Slave operation of two STV8105s allows driving a panel of 512 columns by 72 rows with 16 levels of gray.

Master/Slave plus Primary/Secondary operation of four STV8105s (two along the top of the panel and two along the bottom, see Figure 26), allows driving 512 columns by 144 rows with 16 levels of gray.

The STV8105 sets up Primary/Secondary and Master/Slave assignments depending on the state of input pads MSEL[0] and MSEL[1] as described in Table 10.

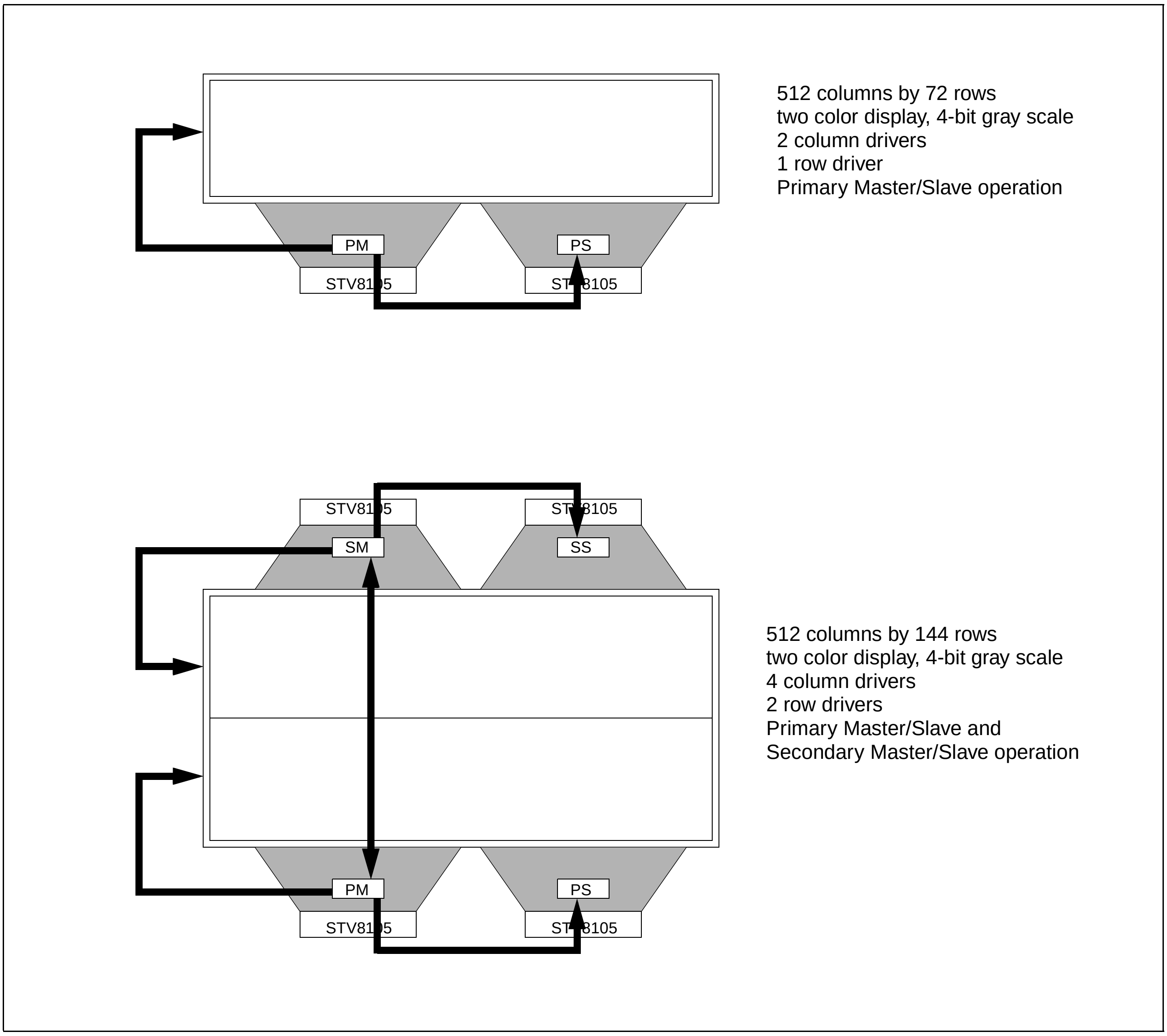
Table 10: Master/Slave Operation

MSEL[1]	MSEL[0]	Test Mode
L	L	Secondary Slave (SS) Interface signals from the Secondary Master are received by the Secondary Slave. The Secondary Slave operates synchronously with Secondary Master.
L	H	Secondary Master (SM) Interface signals from the Primary Master are received by the Secondary Master. A output synchronizing signal is sent to the Secondary Slave.
H	L	Primary Slave (PS) Interface signals from the Primary Master are received by the Primary Slave. The Primary Slave operates synchronously with Primary Master.
H	H	Primary Master (PM) Interface signals of VSYNCOUT, HSYNCOUT, SD/$\overline{\text{COUT}}$, etc. are activated Operation of the Primary Slave and Secondary Master are synchronous with the Primary Master. Row Driver Control signals RCTRLA/RCTRLB are activated.

Primary Master and Secondary Master operate by $\overline{\text{CS1}}$.

Primary Slave and Secondary Slave operate by $\overline{\text{CS2}}$.

Figure 26: Master/Slave and Primary/Secondary Operation



7 Brightness Adjustment

In the STV8105, a brightness (luminance) adjustment changes the current of the column drivers. The column current is a copy of a reference current which is defined by the ratio of a reference voltage on pad VREFx to the value of a precision resistor connected between pad VREFx and ground.

This reference voltage can range from 0.64 to 2.77V. Using a 20K precision resistor, for example, leads to a reference current of from 32 to 138.5µA. The maximum possible value of this reference current is 400µA; it can be set with either $(VREF)/(Rfef) = (0.64V)/(0.6K)$ or $(VREF)/(Rref) = (2.77V)/(6.925K)$.

The reference voltage is generated by an internal 7-bit DAC.

Input data to this DAC can come from an “initial brightness adjustment” register which is loaded by a BRIGHTx command or from data stored in an on-chip, one-time-programmable, non-volatile memory (Anti-Fuse OTP Memory). Input data to the DAC is selected with bit RSELx of command BRIGHTx. By default, the contents of OTP memory are selected as input to the DAC.

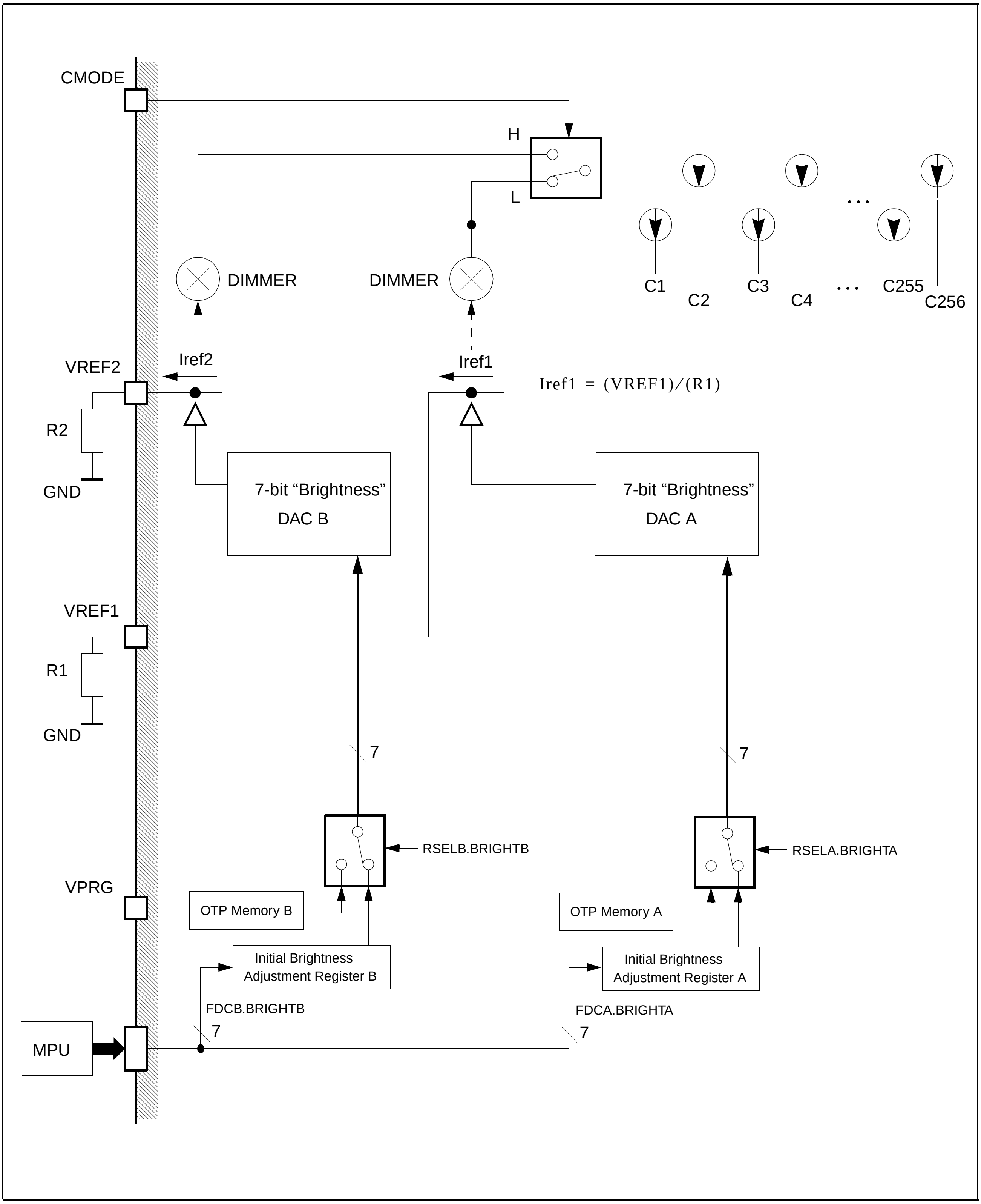
However, if the OTP memory is not already programmed, Section 11.2, the DAC will output an “undetermined” value between the minimum and the maximum possible for VREF. In this case, it is mandatory to program the DAC using the BRIGHTx command.

To support displays using “two” color pixels, the STV8105 has two independent brightness adjustments. Using bits RESLA and RSELB of commands BRIGHTA and BRIGHTB, DAC A and DAC B are loaded, respectively, with the contents of initial “brightness” registers A and B, or with the contents of two on-chip non-volatile memories A and B (Anti-Fuse OTP Memory), as shown in Figure 27.

See Section 13.2 regarding programming “brightness” register A using command BRIGHTA and “brightness” register B with command BRIGHTB.

As shown in Figure 27, the overall brightness of the display can also be adjusted by a dimmer control function - with the command DIMMERCTRL. For details regarding this function, refer to Section 9.2: Dimmer Control.

Figure 27: Control of Initial Brightness Adjustments



8 DC/DC Step-up Converter with VF Detection

8.1 General Description

The STV8105 contains a DC/DC converter controller capable of driving an external, 150 mA, switching power MOS transistor with 90% efficiency. With just few external components a step-up converter can be realized capable of generating up to 25 V from a 3 to 12 V battery. The switching frequency can be set in the range of 150 to 300 KHz which allows reducing inductor size. Normal protections such as under voltage lock-out (UVLO), detection against open loop operation and current overload are also included.

In general, a step-up converter design based on the DC/DC power controller of the STV8105 is capable of:

- operating from a 3 to 12 V battery
- operating from a gate buffer supply (VDC) of 3 to 10 V
- producing an adjustable output, V_H, ranging from 6 to 25 V
- sourcing up to 150 mA at 18 V
- requiring only 10 µA in standby
- operating at efficiencies of up to 90%
- operating at switching frequencies of 100, 200, 250 and 300 KHz
- protecting against overload, under voltage or open loop conditions

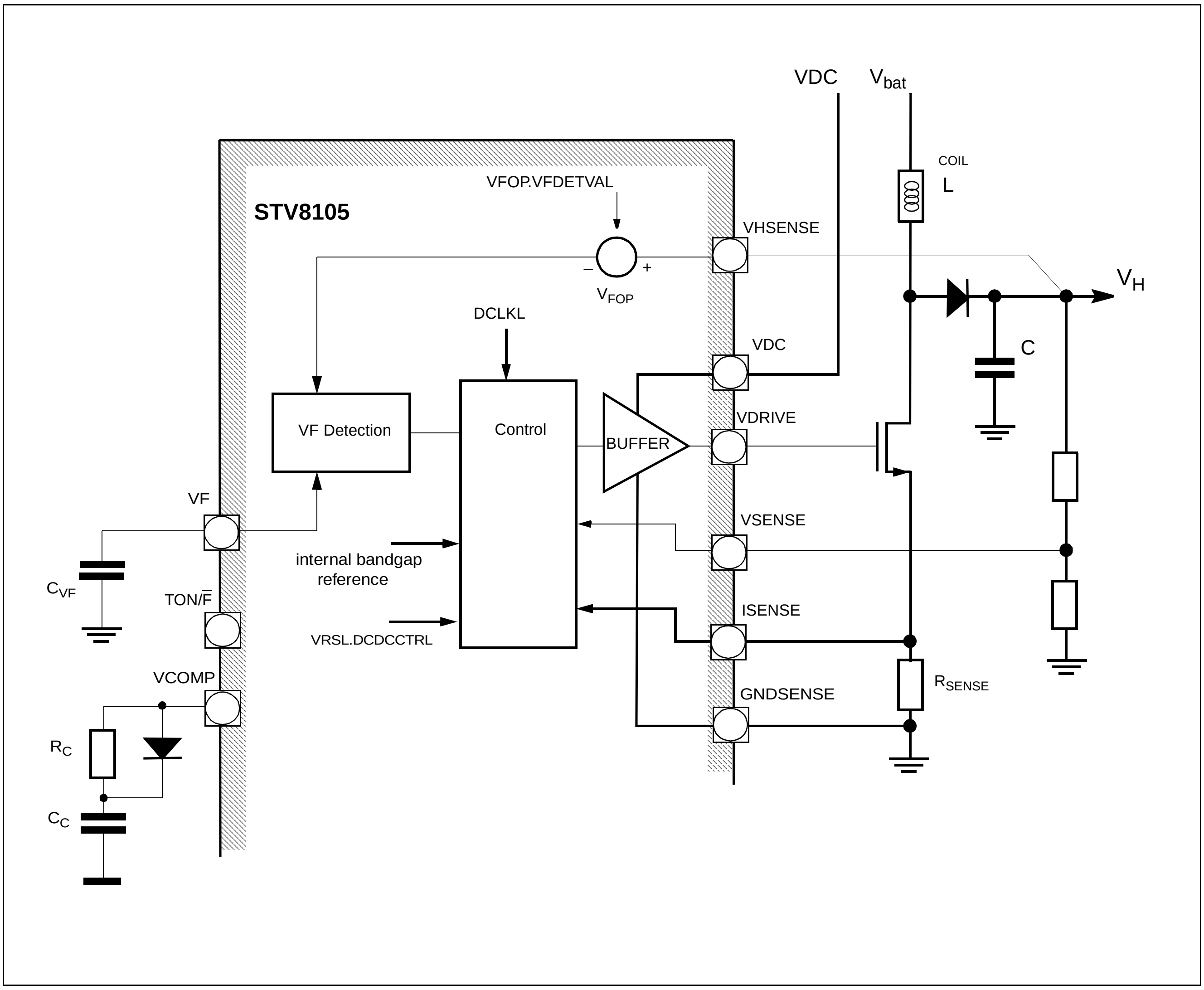
A block diagram of the converter is shown in Figure 28. The output of the converter is V_H. This output can be used to supply the row drivers with VROW1/VROW2 and the column drivers with VPP1/VPP2 and VCOL1/VCOL2.

The VF detection feature of the DC/DC controller monitors the voltage on column outputs C1 and C256 during constant current drive and stores an average of the two voltages on a capacitor connected to pad VF, see C_{VF} in Figure 28. This “detected” voltage is sampled and used by the control block in determining V_H. In addition, the VFOP bit-field of command VFDETVAL can be used to program a 3-bit DAC to output an adjustment to V_H according to

$$V_H = VF + V_{FOP}$$

where V_{FOP} can range from 1.5 to 3.5 V and one LSB = 286 mV.

Figure 28: DC/DC Step-up Converter - Block Diagram



Output V_H is “clamped” to V_H Max. which equals a constant $\times$ VBG at the time of VF detection. If V_H Max. is exceeded, then pad RCTRLB is pulled “High” to VDD by the STV8105 indicating a voltage fault.

8.2 Detailed Description

The converter combines the advantages of two control schemes, pulse width modulation (PWM) or constant switching frequency mode and pulse frequency modulation (PFM) also called constant t_{ON} mode, which together provide high efficiency over a wide range of output load current. Selection between the two modes is done with pad TON/$\overline{F}$.

Output V_H can be adjusted from 6 to 25V by means of two independent closed loops; one is through the VSENSE pad, the other through VHSENSE. The VSENSE-loop is enabled during power-on where V_H increases in proportion to the ramp-up characteristics of an internal bandgap source. The VHSENSE-loop is enabled when V_H is determined to have reached steady-state. Here, V_H tracks the voltage present on pad VF.

The DC/DC power controller also includes several protections designed to prevent damage to the STV8105 or external components. Under voltage lock-out (UVLO) shuts the gate drive buffer down if VDC becomes too low. The power-off threshold is 2.54V; the power-on threshold, 2.77V. VDC is internally filtered by the STV8105 so that the power controller does not react to glitches that might be present on this supply.

Over current protection on pad ISENSE senses the source current of the external switching MOS transistor and disables the gate drive buffer if this current exceeds 250mV/R_{SENSE}. If this condition persists for 16 “internal” cycles, the buffer remains off until either VDC is removed or a reset such as pad $\overline{RST}$ going “Low” occurs.

Detection of an open-loop condition, either on VSENSE or VHSENSE, causes the STV8105 to also shut down the gate drive buffer. If an open-loop condition occurs with VHSENSE, then V_H rises to a value fixed by the external feedback resistor divider.

8.2.1 PWM Mode

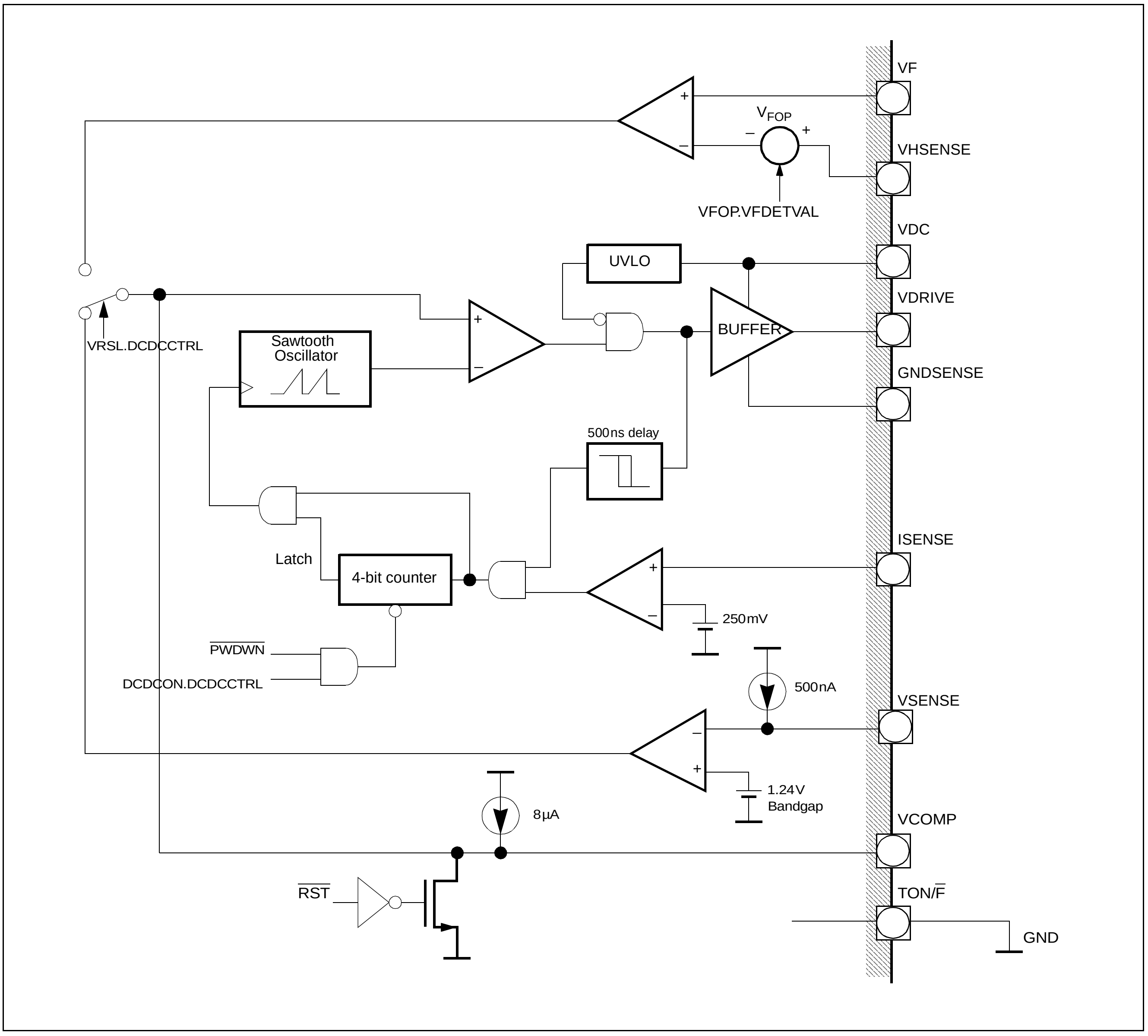
When pad TON/$\overline{F}$ is connected “Low” to GND, the DC/DC converter operates in PWM or constant switching frequency mode.

The PWM circuit consists of a fixed frequency sawtooth generator, an error amplifier and a PWM comparator. The frequency of the generator can range from 150 to 300KHz. The default is 150KHz; the other values are programmed, see Section 13.2, with field FDCDC of command DCDCCTRL. Referring to Figure 29, the error amplifier is a transconductance operational amplifier (OTA) that compares an internal bandgap voltage with the voltage on pad VSENSE. The output of the OTA, pad VCOMP, is available for frequency compensation. The feedback signal on VSENSE is obtained using an external resister divider across the converter output V_H.

The output of the error amplifier, VCOMP, is compared with the sawtooth waveform. If it is greater, the external switching MOS transistor is kept ON. If it is less, the MOS transistor is switched OFF.

Suppose V_H exceeds its steady state value by a small amount, then the output of the error amplifier goes “Low” causing the duty cycle to decrease. As a consequence V_H decreases. Thus the feedback is negative and can maintain V_H at its desired value.

Figure 29: PWM or Constant Switching Frequency Mode



8.2.2 PFM Mode

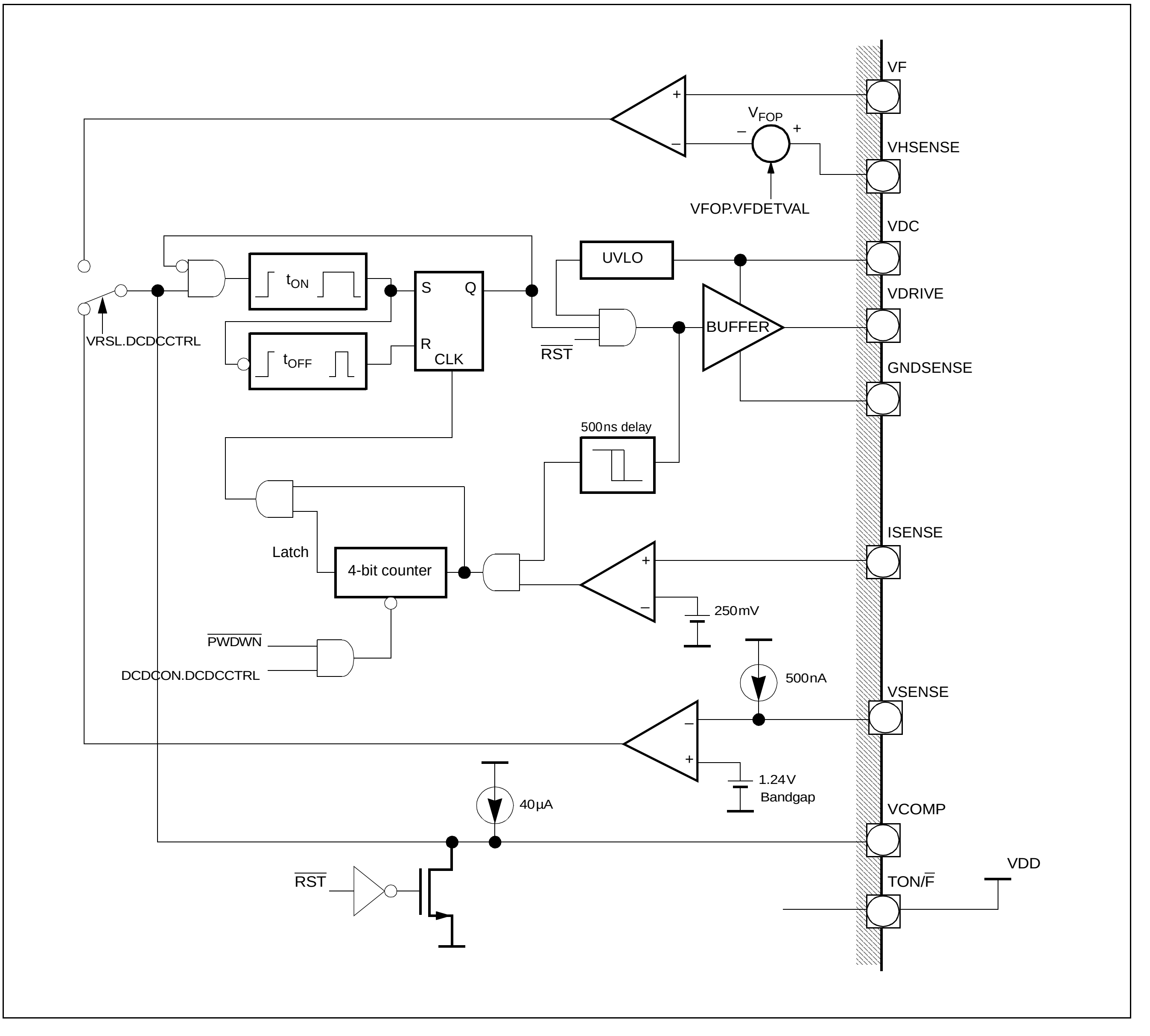
When pad TON/$\overline{F}$ is connected “High” to VDD, the DC/DC converter operates in PFM or constant t_{ON} mode.

Referring to Figure 30, the PFM circuit consists of a t_{ON}/t_{OFF} oscillator that can be locked in the t_{OFF} state by the output of the VSENSE error amplifier. During t_{ON} the external MOS transistor is kept ON. It is switched OFF when a current limit or a t_{OFF} period occurs.

If output V_H becomes less than its steady state value, the output of the error amplifier remains “High” and a t_{ON}/t_{OFF} period starts. The external MOS transistor is switched ON and OFF, repeatedly, until V_H exceeds the steady state value. Then the output of the error amp goes “Low”, and the clock is disabled. If a current limit is detected during a t_{ON} period, the oscillator is locked OFF until a another t_{ON} occurs. In this way, the switching frequency is varied until regulation is obtained.

In PFM mode the switching frequency scales roughly in proportion to the load current. Thus, this mode of operation enables high efficiency with light loads and is ideal to control the converter in standby mode. The PFM control technique does not need any frequency compensation. It is inherently stable.

Figure 30: PFM or Constant t_{ON} Mode



8.3 Compensation Network

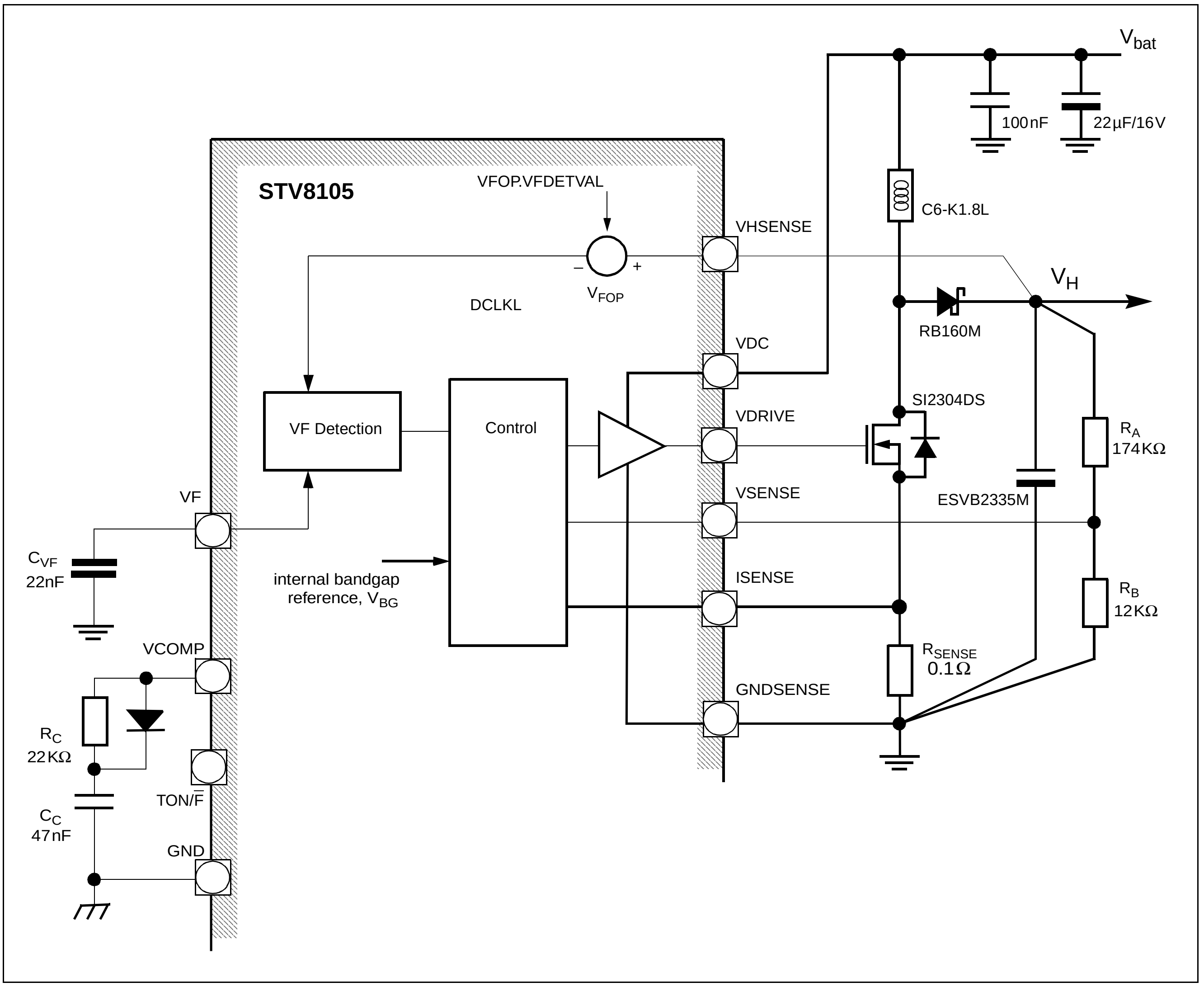
The LC output filter in Figure 28 has a two-pole transfer function. So to guarantee stability in PWM mode, it is necessary to frequency compensate the closed loop response of the converter.

The error amplifier plays a fundamental role in regulating the loop of the converter. This amplifier is an operational transconductance amplifier (OTA). Since the output of an OTA is high impedance, it is easy to compensate the converter by connecting an RC network between this node and ground. Thus the output of the OTA is bought out to a pad, VCOMP, where an external RC can be connected between it and ground, GND. See R_C and C_C in Figure 31 below.

The external RC introduces a dominant low-frequency pole in the response of the control loop. It also introduces a zero that can be placed to cancel the pole of the LC output filter.

Operation in PFM mode does not require frequency compensation.

Figure 31: DC/DC Converter - Application Circuit



8.4 Soft Start

Soft start is an essential feature for correct power-up of the DC/DC converter without overstressing the external switching MOS transistor. Soft start operates during start up of the converter when bit DCDCON of command DCDCCTRL becomes “1”. The soft start function is realized with the same capacitor, C_C, that is used for frequency compensation. The soft start ramp-up time can be calculated by simply taking into account the output sourcing current of the OTA which is 40µA in PWM mode and 8µA in PFM.

During power-up, the external MOS transistor starts switching with a duty cycle that gradually increases at the same rate as the voltage on pad VCOMP. In PFM mode, pad VCOMP is used only for soft start, and the voltage on this pad ramps-up to VDD.

8.5 Peak Current Detection

The drain-source voltage of the external switching MOS transistor is sensed by R_{SENSE}, Figure 31, and as soon as a comparator detects that this voltage has exceeded 250 mV, the gate drive of the external MOS transistor is switched OFF.

When the comparator senses an over-current condition, a flip-flop is set, and the external MOS transistor is switched OFF. The flip-flop remains set while the over-current condition persists. If this condition persists for 16 continuous “internal” cycles, a master latch turns the DC/DC converter off, and the converter can not be restarted with DCDCON.DCDCCTRL = “1” until after a new power-up or hardware reset ($\overline{RST}$ = “0”) is issued.

An internal low-pass filter in series with pad ISENSE with an inherent delay of 500 ns rejects voltage glitches caused by the external switching MOS transistor during its operation.

Refer to Section 13.2: Command Details Ordered by Command Code for details regarding registers DCDCCTRL and VFDETVAL which control operation of the DC/DC converter.

9 Column Drivers

The column drivers of STV8105 are described in Figure 32.

Together, the column driver outputs C1 to C256 can be connected to three different sources or placed in Hi-Z. The three different source types are: a constant current supplied on pads VPP_X, a constant voltage supplied on pads $VCOL_X$, or switched to GNDL.

Supply pads VPP1 and VCOL1 are for the odd numbered outputs.

Supply pads VPP2 and VCOL2 are for the even numbered outputs.

The GNDL pad is common to all columns pads.

A dedicated command register (COLCTRL 1Ah) provides 4 control bits to override the column output signals:

- the CLLM bit, when set to “1” (with CLLZ = “0”), forces all column outputs to VCOL1 and VCOL2. It overrides all other column commands. The inactive default value is “0”.
- bit CLLZ, when set, forces all column outputs in Hi-Z state and overrides all other commands. Inactive default value is “0”.
- bit HSLZ, when set, forces output HSYNCOUT to Hi-Z. HSYNCOUT is grounded to pad GNDL when HSLZ is “0”, the inactive default value.
- bit OFLZ, when set (with CLLM and CLLZ = “0” and after the PWM current sourcing period), forces all column outputs to Hi-Z, otherwise the outputs are grounded to GNDL when OFLZ is “0”, the inactive default value.

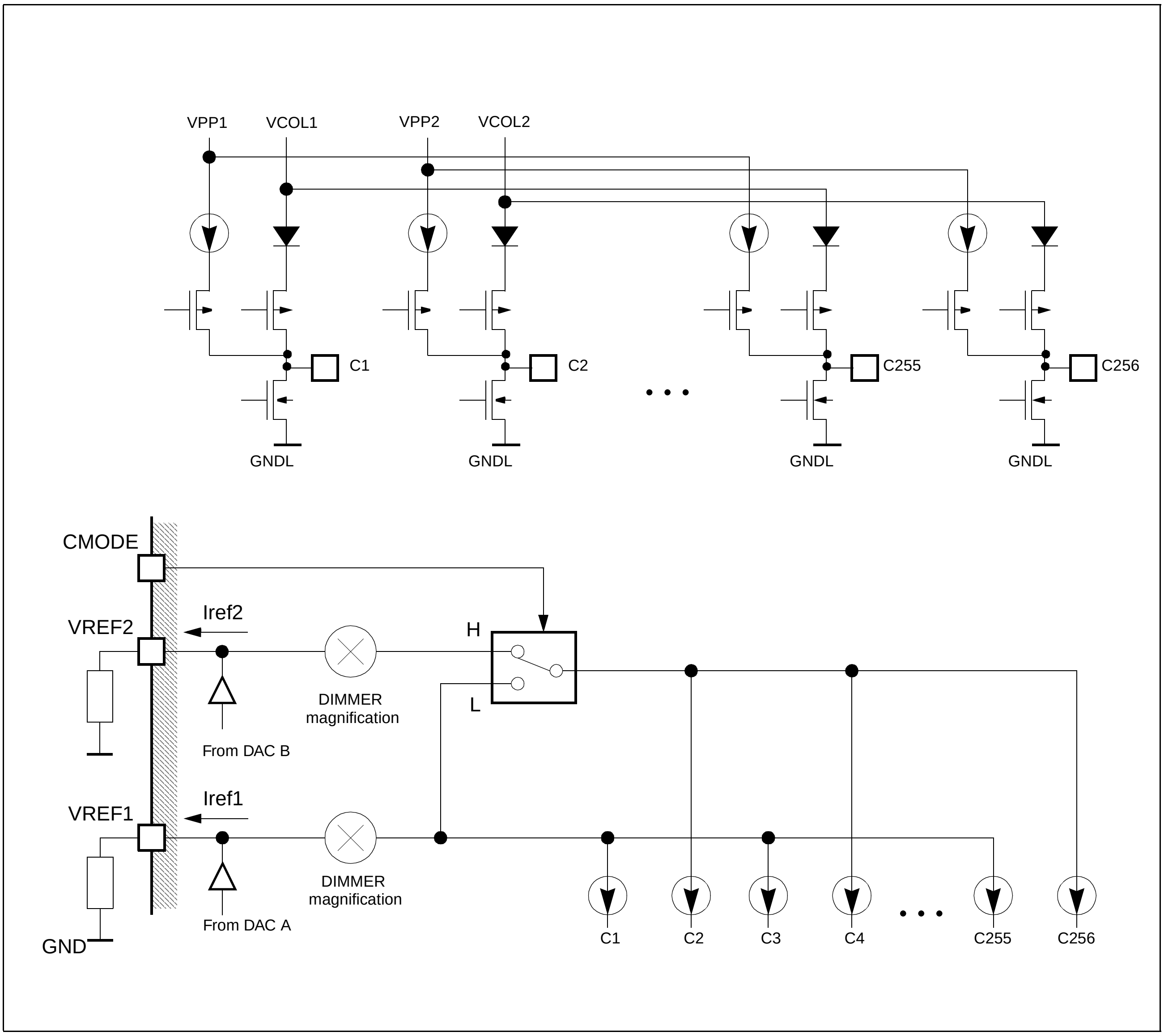
9.1 Color Selection Modes

The STV8105 can drive dual or “two” color displays: one color appears on the odd columns, the other on even columns. Supplies VPPx and VCOLx as well as the column current generators can be set to different levels to fit the driving characteristics of the two colors. Two reference currents are defined by the selected “brightness” DAC (DAC A or DAC B) and by two precision resistors connected on pads VREF1 and VREF2. These resistors can have the same or different values. The dual current reference mode is selected by pulling pad CMODE “High” to VDD.

Note:

- In the dual color mode, the same dimmer control applies to the two colors.
- When using the 64 level gray scale modes (resolutions of 128×72 and 256×36), the dual mode cannot be used, supplies VPP1 and VPP2 as well as VCOL1 and VCOL2 must be connected together, and only DAC A (VREF1) can be used.
- When pad CMODE is pulled “Low” to GND, only one current reference is used. It is defined by the resistor on pad VREF1 and controlled by DAC A along with the dimmer command. See Figure 32.

Figure 32: Column Drivers



Bit HTUR of the command DOTMTRXDIR can be used to reverse the horizontal display direction versus column pinout. Note that the picture must be reloaded because HTUR can only change the Display RAM write direction. Refer to Section 13.2 for details.

9.2 Dimmer Control

The brightness of the whole display panel can be changed with the DIMM bit-field of command DIMMERCTRL. DIMM selects what fraction of I_{ref} to use in establishing the column output current I_{COUT} which is given by

$$I_{COUT} = Iref \times fract[DIMM]$$

where fract[DIMM] is a fraction depending on the value of field DIMM according to Table 11 below. For more info on command DIMMERCTRL see Section 13.2.

Table 11: Dimmer command

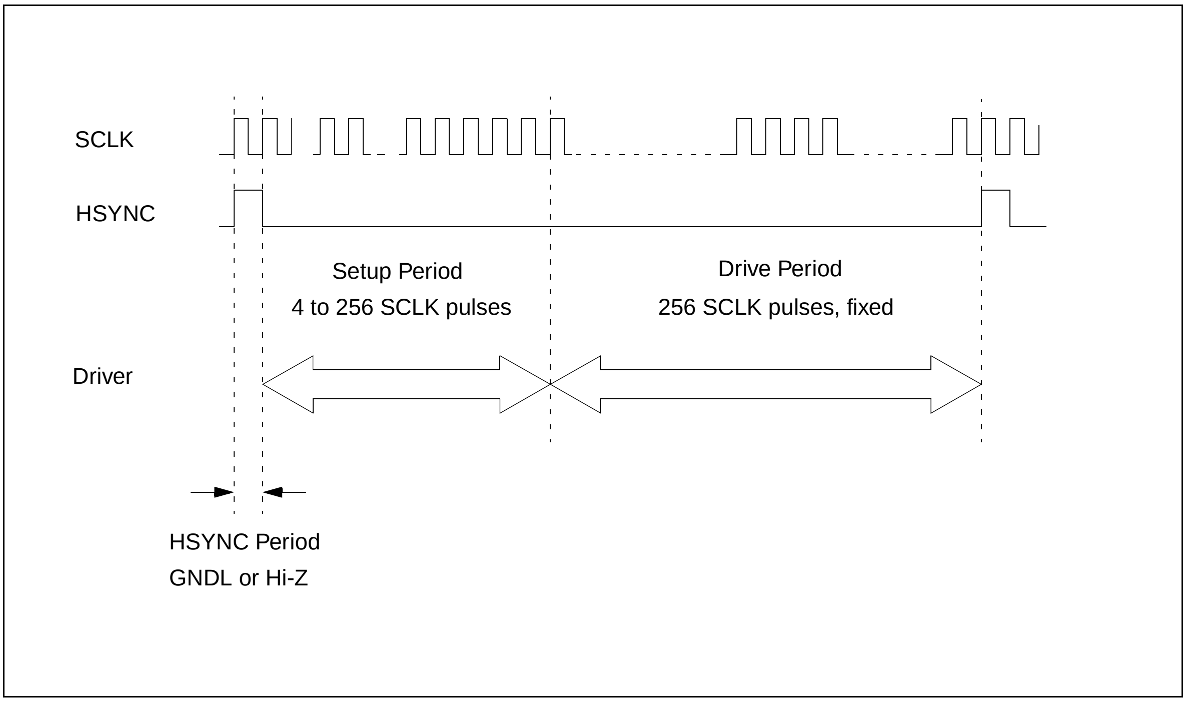
DIMM.DIMMERCTRL	fract[DIMM]	Ratio of Iref [%]
b4 b3 b2 b1 b0		
0 0000	1/16	6.25
0 0001	2/16	12.5
----	----	----
0 0011	4/16	25
----	----	----
0 0111	8/16	50
----	----	----
0 1011	12/16	75
----	----	----
0 1111	16/16	100
----	----	----
1 0011	20/16	125
----	----	----
1 0111	24/16	150
----	----	----
1 1011	28/16	175
----	----	----
1 1111	32/16	200

Note: Note: A "Dimmer" adjustment is performed synchronous with VSYNC when bit DISPON of register DCTRL is "1". Otherwise, when DISPON.DCTRL is "0", this adjustment is performed immediately after the command DIMMERCTRL is issued.

9.3 Drive Control

The STV8105 outputs a constant current on each column pad depending on the "Brightness" and "Dimmer" levels selected by the user. During the row period, the column current is PWM modulated according to the gray scale value of each pixel. A row (or scan line) period is divided into an OLED Setup Period for reset and precharge followed by a Drive Period (constant current gradation display).

Figure 33: Setup and Drive Periods



9.4 Setup Period

The Setup Period is composed of four programmable sub-periods. Each sub-period is programmed using a corresponding OELPERIOD1, 2, 3 or 4 (1Bh, 1Ch, 1Dh or 1Eh) command.

The duration of each sub-period can be programmed to be 1 to 64 SCLK clock periods long using the ExCL bit-field of the corresponding OELPERIODx command, x = 1, 2, 3 or 4. This leads to a total Setup Period of between 4 and 256 SCLK clock periods as shown in Figure 34.

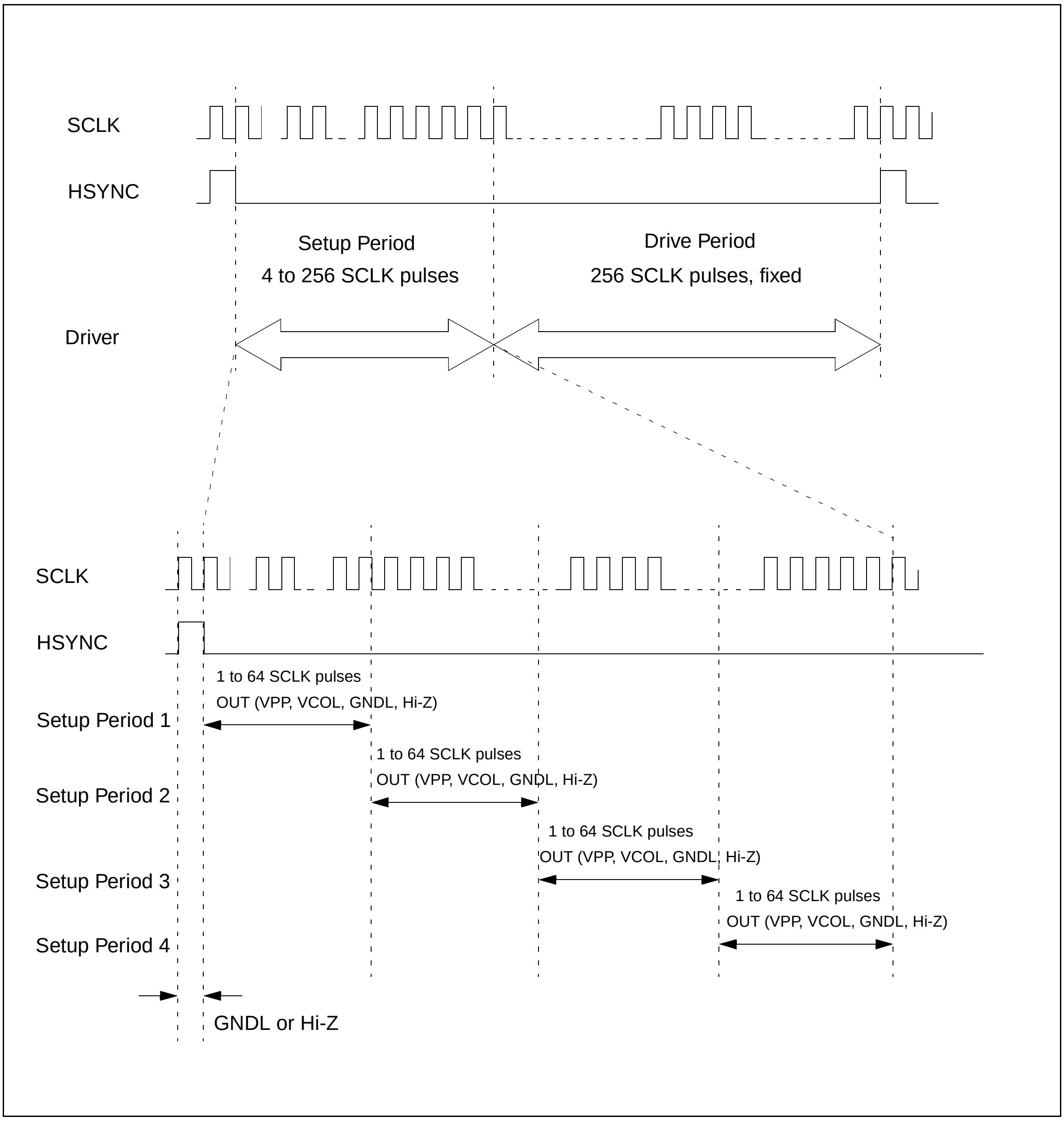
The column output signal of a column pad can be programmed independently during the four sub-periods using the ExST bit-field of the corresponding OELPERIODx command, x = 1, 2, 3 or 4, as explained below. The selected column driver output can:

1. source a constant current determined by the brightness and dimmer adjustments, Figure 32,
2. be forced to VCOLx,
3. be pulled down to ground GNDL or
4. be placed in a Hi-Z state.

If the pixel value to be displayed is 00h (i.e., black), then independent of whether the selected column output is programmed to be at VPPx, VCOLx or in Hi-Z during the setup period, the column output is pulled down to ground GNDL during the whole of the setup period and during the whole of the drive period as well.

Note: before the first setup period, 1 SCLK clock period is inserted in a row period sequence. During this time, the output HSYNCOUT can be pulled to ground GNDL or put in Hi-Z using bit OFLZ of the command COLCTRL (1Ah).

Figure 34: Setup Period Timing



9.5 Drive Period

The active duration of a row period (or scan line period) is named the drive period. The drive period is 256 SCLK clock periods long.

During the drive period, the column drivers are sourcing constant current defined by the brightness and dimmer levels selected by the user. The time the column current is sourced is proportional to the gray scale level of the pixel to be displayed, leading to a PWM modulation. This “sourcing” time can have 256 different values. After the “sourcing” time elapses, column current is turned off, and the column pad is switched to ground GNDL until the next setup period.

The STV8105 has a 30 byte lookup table to define the current sourcing duration of the drive sequence.

There are15 bytes dedicated to the odd columns and 15 bytes dedicated to the even columns. They can be loaded thanks to dedicated ODDx and EVENx commands (command codes 2Dh to 1Fh and 3Ch to 2Eh).

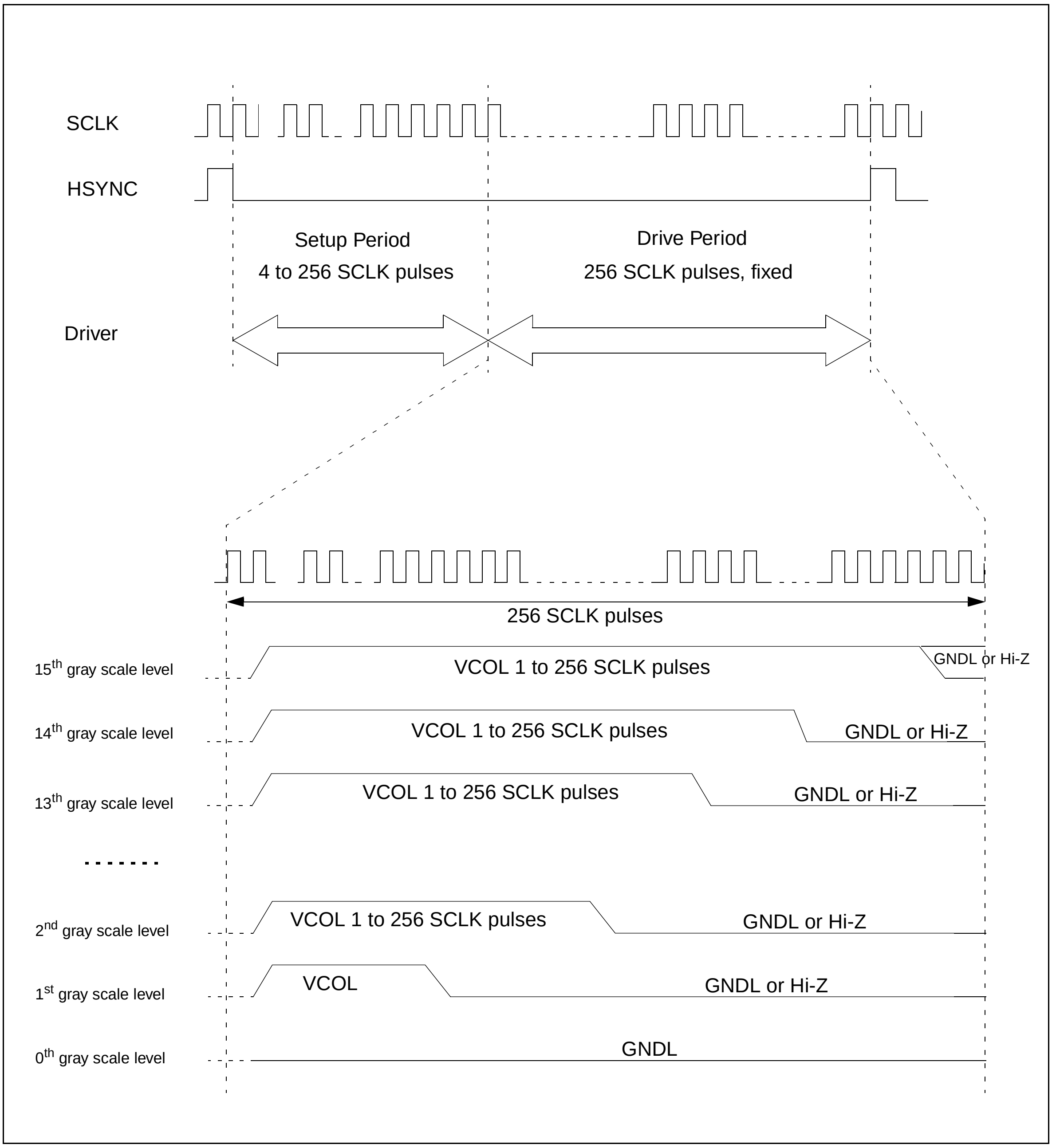
Separate ODDx and EVENx lookup tables can be used in case of “two” color modes. For a given level of gray, the odd and even bytes can be loaded with different values to fit each color brightness response. The STV8105 uses ODD and EVEN (or ODD only) lookup tables depending on the input level at pad CMODE. When CMODE is “High”, the ODD lookup table applies to the odd columns, and the EVEN lookup table applies to the even columns. When CMODE is “Low”, only the ODDx lookup table is used for both even and odd columns.

For some gray scale modes the lookup tables are not user accessible; see next sections. For details regarding the ODDx and EVENx commands, refer to Section 13.2: Command Details Ordered by Command Code.

9.5.1 16 Level Gray Scale Mode

In this mode the gray level of each pixel is defined by a 4-bit value stored in the Display RAM, leading to 16 levels of gray.

Figure 35: 16 Level Gray Scale Mode - Drive Timing



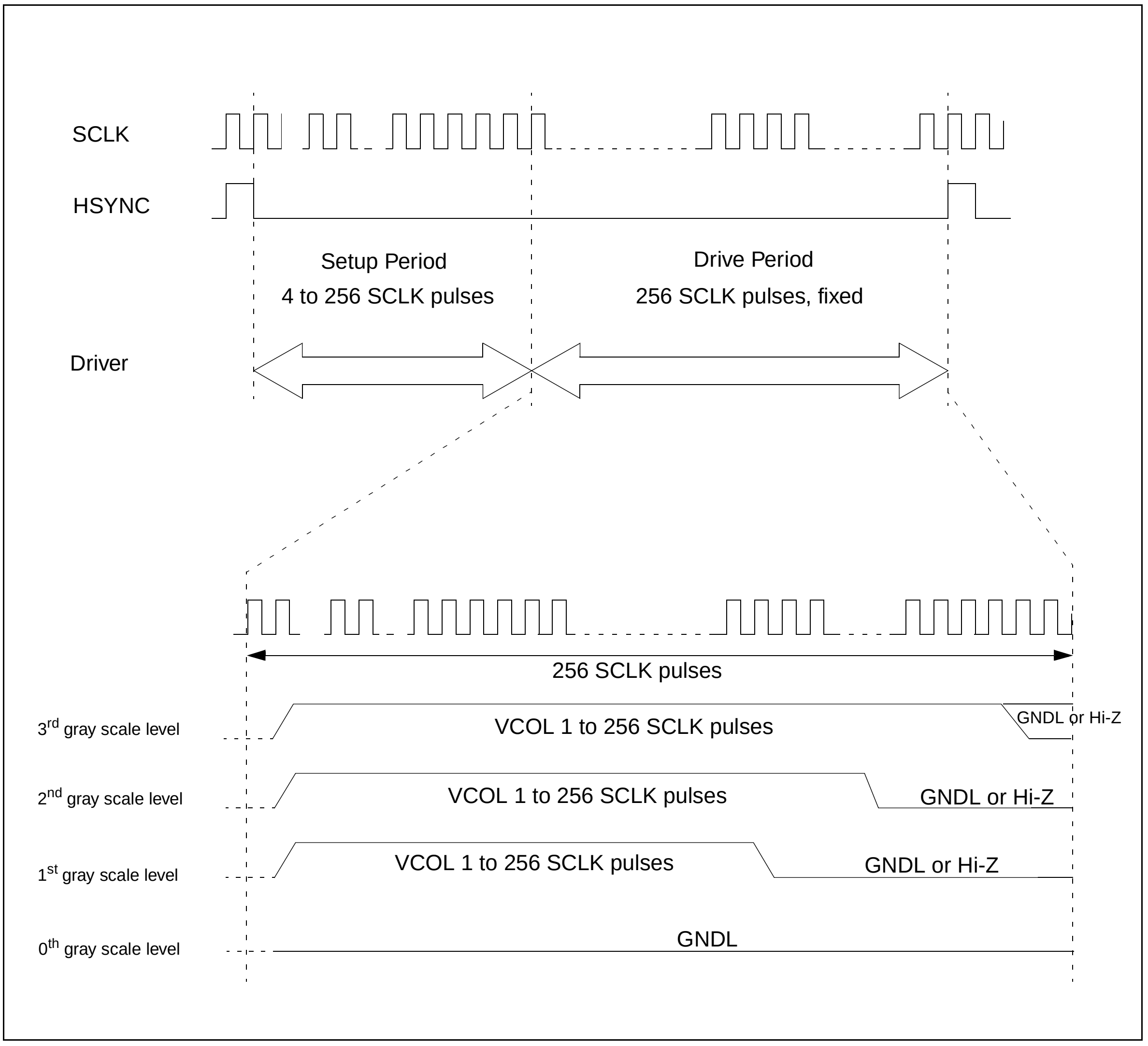
This mode uses the ODDx and EVENx, or ODDx only, lookup tables to define the column current sourcing time. There are 15 bytes corresponding to the 15 different, possible values of pixel data in Display RAM. When the pixel value is 0h, the column current source is off (to GNDL) for the entire drive period.

Each byte of the lookup table holds a value between 0 to 256 (00h to FFh). This value corresponds to the number of elementary SCLK clock periods. Each byte of the lookup table is loaded using the corresponding ODDx or EVENx command.These bytes must be loaded during the power-on/reset sequence.

9.5.2 4 Level Gray Scale Mode

In this mode the gray level of each pixel is defined by a 2-bit value stored in the Display RAM, leading to 4 levels of gray.

Figure 36: 4 Level Gray Scale Mode - Drive Timing



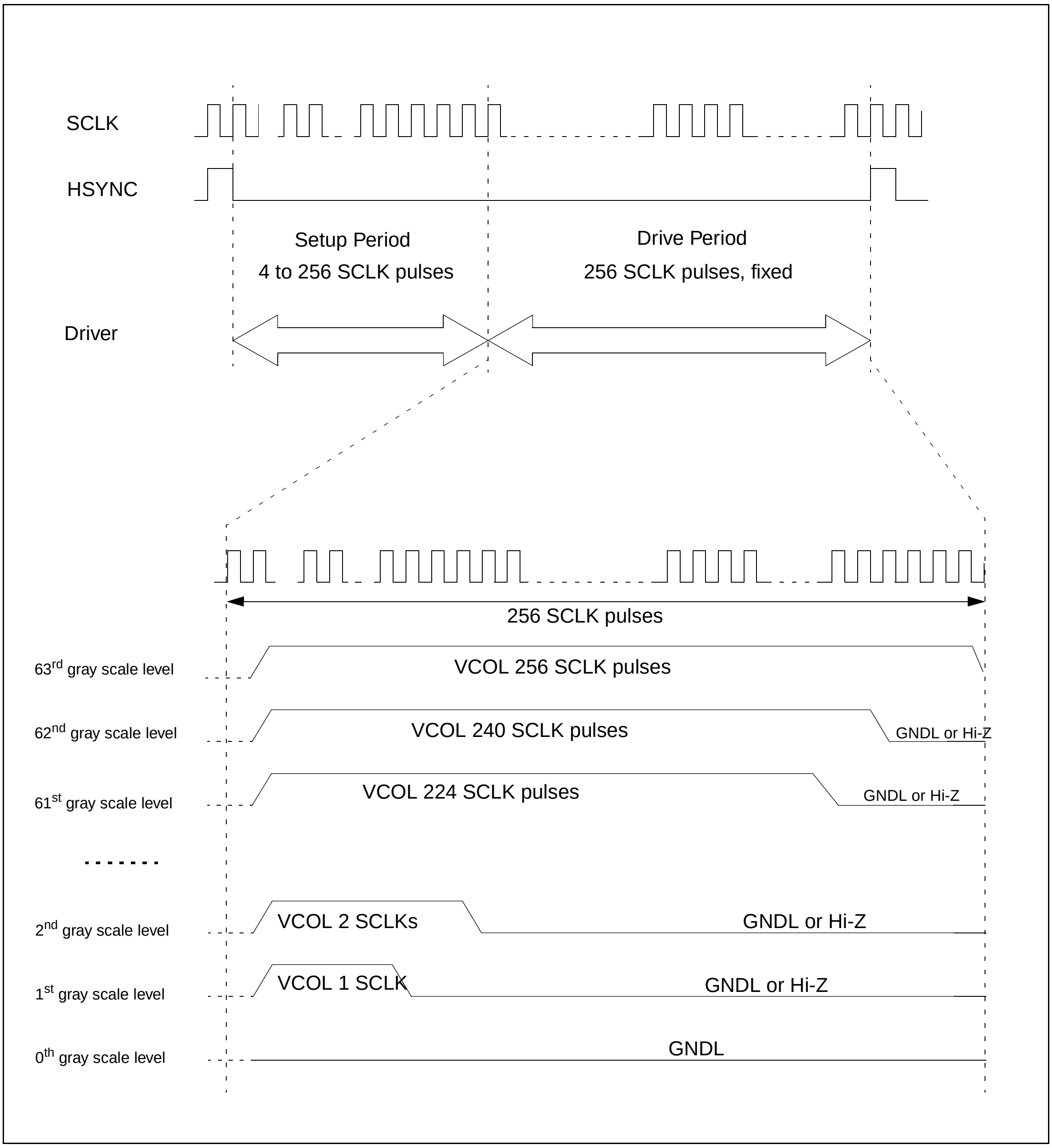
Because only 4 gray levels are used in this mode, only 3 or 6 from among the 15 or 30 lookup tables are needed:

ODD3, ODD2, ODD1 and EVEN3, EVEN2, EVEN1 when pad CMODE is “High” and ODD3, ODD2, ODD1 when CMODE is “Low”.

The lookup table bytes must be loaded during the power-on/reset sequence.

9.5.3 64 Level Gray Scale Mode

Figure 37: 64 Level Gray Scale Mode - Drive Timing



In this mode the lookup table is not user programmable. It is shown below in Table 12 which lists the number of SCLK clock pulses generated for each of the 64 possible values of a 6-bit pixel.

Table 12: Lookup Table for 64 Level Gray Scale Mode

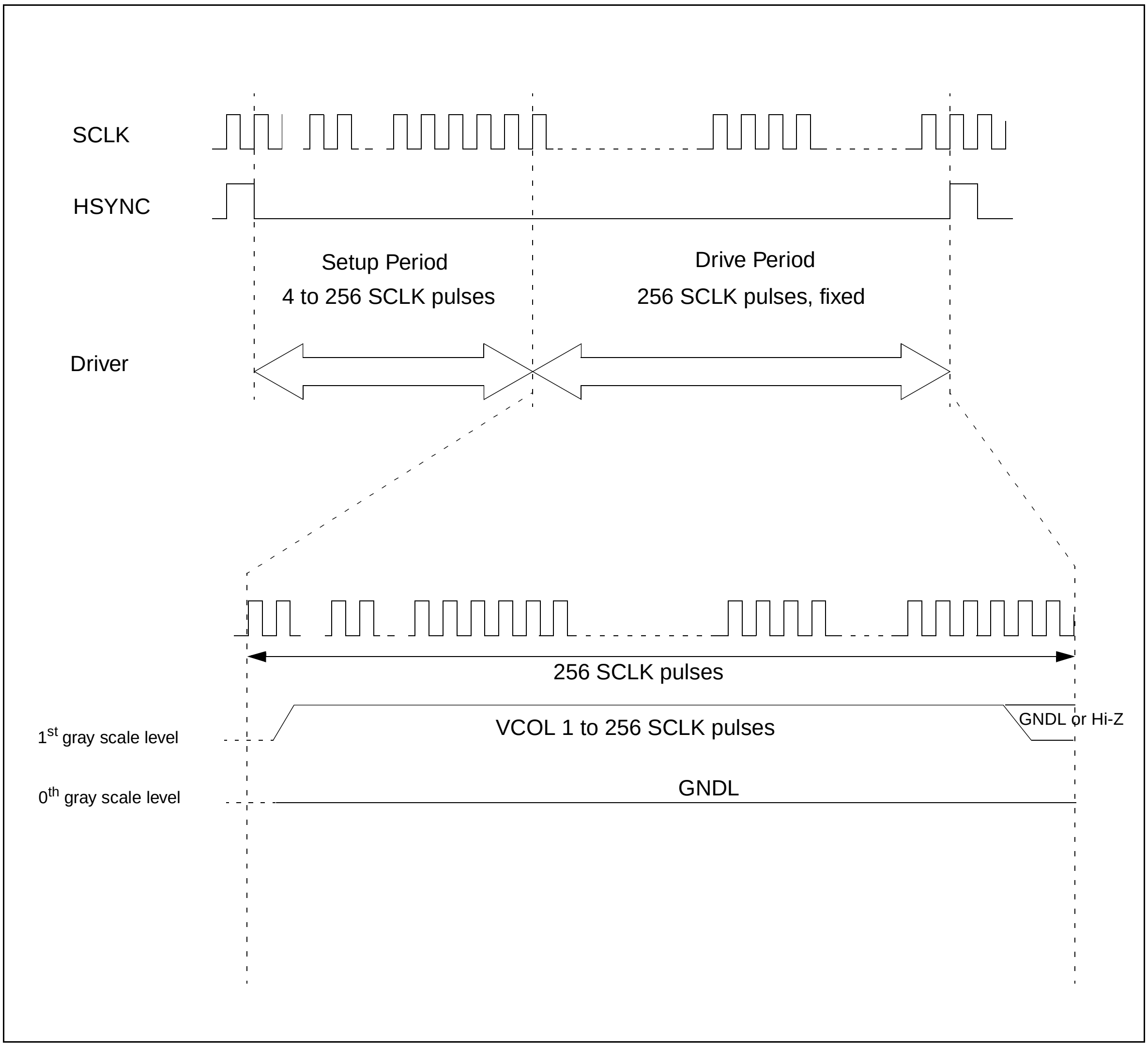
Pixel value	Lookup byte
binary	**number of SCLK pulses**
11 1111	256
11 1110	240
11 1101	224
11 1100	208
11 1011	200
11 1010	192
11 1001	184
11 1000	176
11 0111	168
11 0110	160
11 0101	152
11 0100	144
10 0011	136
11 0010	128
11 0001	120
11 0000	112
10 1111	108
10 1110	104
10 1101	100
10 1100	96
10 1011	92
10 1010	88
10 1001	84
10 1000	80
10 0111	76
10 0110	72
10 0101	68
10 0100	64
10 0011	60
10 0010	56
10 0001	52
10 0000	48
01 1111	46
01 1110	44
01 1101	42
01 1100	40
01 1011	38
01 1010	36
01 1001	34
01 1000	32
01 0111	30
01 0110	28
01 0101	26
01 0100	24
01 0011	22
01 0010	20
01 0001	18
01 0000	16
00 1111	15
00 1110	14
00 1101	13
00 1100	12
00 1011	11
00 1010	10
00 1001	9
00 1000	8
00 0111	7
00 0110	6
00 0101	5
00 0100	4
00 0011	3
00 0010	2
00 0001	1
00 0000	0

Note: odd and even columns have the same value, so there is NO “two” color mode in the 64 level gray scale modes.

9.5.4 Monochrome Mode

In this mode a pixel is ON or OFF depending on the value of the bit in Display RAM. The column current sourcing time is 0 when the pixel is OFF. It is equal, in terms of SCLK clock pulses, to the value of the byte loaded by the corresponding ODD1 or EVEN1 command (CMODE “High”) or by the ODD1 command (CMODE “Low”) when the pixel is ON. The lookup table byte(s) must be loaded during the power-on/reset sequence.

Figure 38: Monochrome Mode - Drive Timing



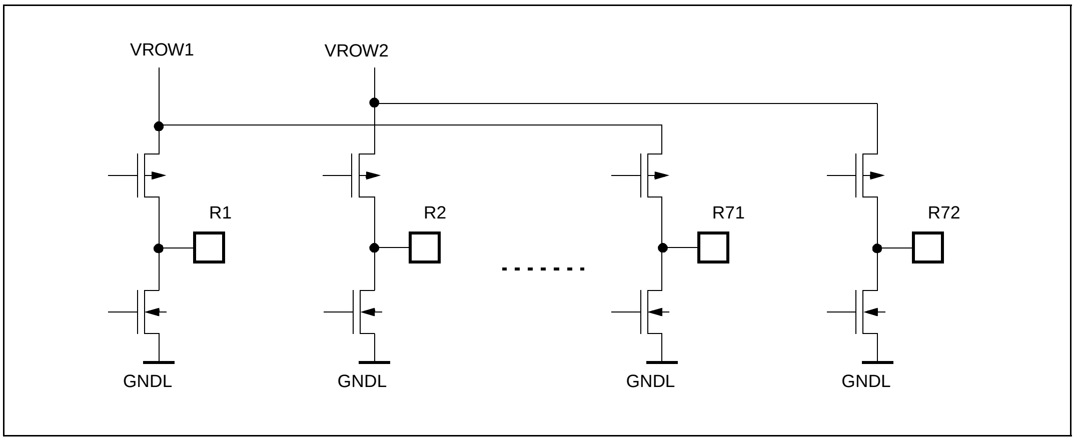
10 Row Driver Control

10.1 Row Drivers

The row driver of STV8105 is the 2-transistor structure shown below in Figure 39.

When activated, the row output pad is switched to GNDL. When not active, the row output pad is pulled-up to the voltage supplied on pads VROW1 and VROW2. The R_{ON} of the MOS transistor to GNDL is 10 ohms, max.

Figure 39: Row Drivers



Bit VTUR of command DOTMTRXDIR can be used to select the vertical display direction versus Display RAM contents. Refer to Section 13.2 for details.

The ROWDRVSEL command allows selecting the scanning direction as well as whether single or dual scanning mode is used.

10.2 Row Driver Scanning Modes

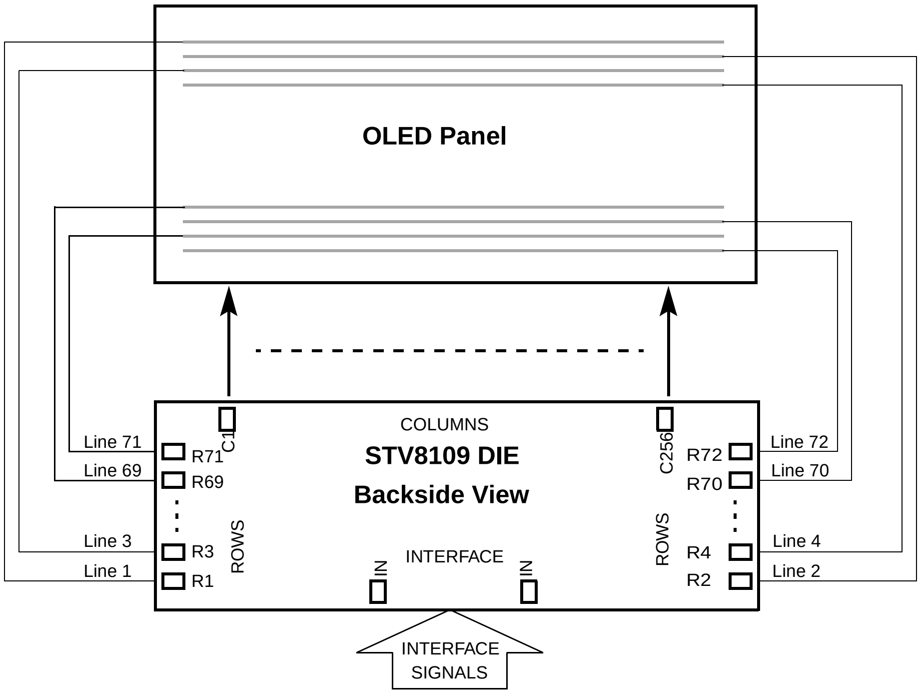
10.2.1 Single Scanning Mode

The single scanning mode is selected when the RMODE bit-field of command ROWDRVSEL is programmed to “10b”.

In single scanning mode when the RDIR bit of command ROWDRVSEL is “0”, the Row Drivers are scanned in increasing order from R1 to R72.

When RDIR.ROWDRVSEL is “1”, the rows are scanned in reverse order starting from R72.

Figure 40: Single Scanning



10.2.2 Dual Scanning Mode

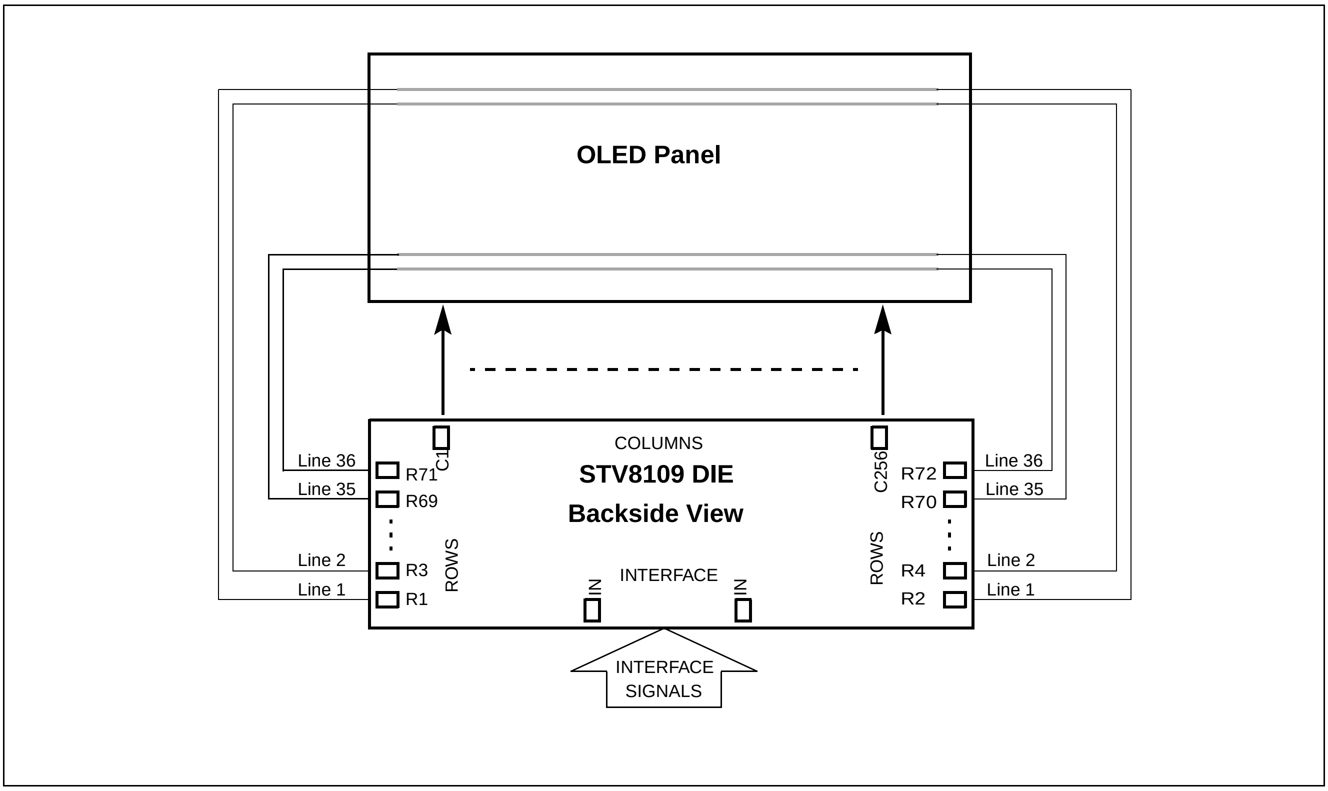
The dual scanning mode is selected when the RMODE bit-field of command ROWDRVSEL is programmed to “11b”.

In dual scanning mode the odd and even row driver scans are simultaneous.

A maximum of 36 lines can be scanned at once, and the 2 row pads can sink with an effective R_{ON} of 5 ohms, max.

The scanning direction is changed, again, with bit RDIR of command ROWDRVSEL.

Figure 41: Dual Scanning



11 OTP Memory

11.1 Introduction

The OTP (One Time Programmable) Memory consists of a Volatile Memory (VM) made of an array of flip-flops and a Non-Volatile Memory (NVM) made of an array of anti-fuses. Every time the STV8105 is powered-on or exits from reset, the OTP is automatically initialized. The NVM is powered on. Calibration and configuration parameters that are already stored in the NVM are read and latched into VM, then the NVM is powered off to avoid extra current consumption.

11.2 OTP Memory Programming

In order to store the calibration and configuration parameters permanently, the contents of VM has to be transferred to the NVM.

Below are details of the commands that allow permanently storing calibration and configuration data into the NVM.

Command	Function	Addr	Command Data								Default
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SHORT	VPRG internally shorted to GNDL, ON/OFF	F3	0	0	0	0	0	0	0	SHORT ON	01h
PRGOTP	OTP Programming	F5	0	0	0	0	0	0	0	1	-
CKMM	if SEAL bit = “1”, SW Reset, else NOP	F7	-	-	-	-	-	-	-	-	-

First of all, care has to be taken when the programming voltage is applied to pad VPRG. Before powering-up VPRG, the internal switch between VPRG and ground (GND) has to be opened by making sure bit SHORTON of command SHORT is “0”.

The OTP programming procedure is activated with the PRGOTP command. This procedure, which last about 50ms, autonomously involves blowing the anti-fuses. This procedure also terminates autonomously.

With the CKMM command it is possible to check if OTP memory has been correctly programmed. When CKMM is executed, the STV8105 checks the state of an internal “SEAL” bit. If this bit is “1”, meaning the OTP memory has been correctly programmed, the STV8105 gets reset. If the “SEAL” bit is not “1”, the CKMM command is ignored.

The recommended conditions for “blowing” and achieving a reliable short circuit of the anti-fuses are:

- Minimum programming current I_{PRG} > 250mA
- Programming voltage V_{PRG} = 16V, accepted range 14V < V_{PRG} < 18V
- Time to program all cells Twr > 50ms

11.3 A Short Routine for Programming the OTP

Below, a short routine that can be used to program and check the OTP memory of the STV8105.

```
                     # Power on VDD.
01h                  # Issue BRIGHTA command, initial brightness “A” adjustment.
00h to 7Fh           # Set desired default value for brightness “A”.
02h                  # Issue BRIGHTB command, initial brightness “B” adjustment.
00h to 7Fh           # Set desired default value for brightness “B”.
F3h                  # Issue SHORT command
00h                  # with Bit0 of next word, SHORTON, equal to “0”,
                     # i.e. short is off.
                     # Now power on VPRG.
F5h                  # Issue PRGOTP command
01h                  # with Bit0 of next word equal to “1”.
                     # Wait 50ms.
                     # Power down VPRG.
F2h                  # Issue SOFTRST command, i.e. issue a software reset.
                     # Power on OLED display supplies VPP1, VPP2, VCOL1,etc.
10h                  # Issue DCTRL, the dot-matrix display control command,
03h                  # with all pixels ON.
F7h                  # Issue the CKMM command to check OTP programming. If
                     # display goes blank, i.e. OFF, then OTP has been
                     # programmed correctly.
```

12 STV8105 Configurations

12.1 Reset Configuration

When pad RST is brought “Low”, the state of the STV8105 is as follows:

- oscillator OFF
- DC/DC Converter OFF
- Column drivers at GNDL
- internal Row drivers at GNDL
- external IC controls SCLKOUT, VSYNCOUT, HSYNCOUT, RCTRLA, RCTRLB and ROWDATA are at GND
- all Registers are loaded with their default values (see Table 13)

After RST is released, i.e. brought “High”, or after completion of a software reset, which is considered to be 200ns max after sending or issuing the command SOFTRST, the state of the STV8105 becomes:

- oscillator ON
- DC/DC Converter remains OFF but waiting for a command
- Column drivers at GNDL but also waiting for a command
- internal Row drivers at GNDL (waiting for a command)
- External Driver Control: SCLKOUT = SCLK Clock output
- external IC controls VSYNCOUT, HSYNCOUT, RCTRLA, RCTRLB and ROWDATA are at GND
- all Registers are at their default values (waiting for a command)

SOFTRST is a one byte command and is the only command that can perform a reset of the STV8105.

12.2 Sleep Configuration

The STV8105 can be placed into a sleep mode with command SLEEP (command code F1h). However, the STV8105 is forced out of sleep mode if either command DCDCCTRL (03h) or DCTRL (10h) is sent, irrespective of the data value that follows their command codes.

When placed IN sleep mode, the state of the STV8105 is as follows:

- oscillator ON
- DC/DC Converter OFF
- Column drivers at GNDL
- internal Row drivers at GNDL
- all analog circuits powered by VDD are OFF
- all registers as well as the SRAM retain their status
- bus interface active

13 Command and Control Registers

The STV8105 has a set of registers to command and control the display system. They are accessed via the interfaces described in Chapter 2: Bus Interfaces.

The following rules are used in this datasheet to describe bit, bit-fields and registers:

- ROWDRVSEL is the name of a register,

- RDIR.ROWDRVSEL is the RDIR bit of register ROWDRVSEL,

- RMODE.ROWDRVSEL is the RMODE bit-field of register ROWDRVSEL.

Unused bits are read as 0 and must be written as 0.

Dummy or irrelevant bits are noted “D”; their value when read is undefined, they must be written with 0 for future compatibility.

13.1 List of Commands Ordered by Command Code

Table 13: Register List Ordered by Increasing Command Code

Register name	Comd code & access	Reset	b7	b6	b5	b4	b3	b2	b1	b0	Comments
SCLKDIV	00h - W	00h	0	0	0	0	0	SDIV			SCLK clock divide ratio
BRIGHTA	01h - W	00h	RSELA	FDCA							Initial Brightness adj. A
BRIGHTB	02h - W	00h	RSELB	FDCB							Initial Brightness adj. B
DCDCCTRL	03h - W	00h	-	-	-	-	FDCDC			DCDC ON	DC/DC Converter Control
RESERVED	04h	- -	-----------								Do not use, reserved
RESERVED	05h	- -	-----------								Do not use, reserved
VFDETVAL	06h - W	00h	-	-	-	-	-	VFOP			Selection of voltage to add to VF to produce VH
RESERVED	07h	- -	-----------								Do not use, reserved
----	----	- -	-----------								Do not use, reserved
RESERVED	09h	- -	-----------								Do not use, reserved
DCTRL	10h - W	00h	-	-	-	-	-	DINV	DALI	DISP ON	Dot-Matrix Display Control
DOTMTRXDIR	11h - W	00h	-	-	DUMM		-	-	VTUR	HTUR	Dot-Matrix Direction select
DOTMTRXSCAN	12h - W	47h	-	SCLN							Dot-Matrix Scanning Line
RAMXSTART	13h - W	00h	X	X	X	X	X	X	X	X	Display RAM X Start Address
RAMYSTART	14h - W	00h	X	X	X	X	X	X	X	X	Display RAM Y Start Address
GSADDINC	15h - W	00h	GSMODE				-	-	YINC	XINC	Gray scale and Increment Mode Set
DIMMERCTRL	16h - W	0Fh	-	-	-	DIMM					Dimmer Control
ROWDRVSEL	17h - W	02h	-	-	-	RDIR	-	-	RMODE		Row Driver Mode Select
RESERVED	18h	- -	-----------								Do not use, reserved
RESERVED	19h	- -	-----------								Do not use, reserved
COLCTRL	1Ah - W	00h	-	-	-	-	CLLM	CLLZ	HSLZ	OFLZ	Column Output Control
OELPERIOD1	1Bh - W	0Fh	E1ST		E1CL						Setup Period 1
OELPERIOD2	1Ch - W	00h	E1ST		E1CL						Setup Period 2
OELPERIOD3	1Dh - W	00h	E2ST		E2CL						Setup Period 3
OELPERIOD4	1Eh - W	00h	E3ST		E3CL						Setup Period 4
ODD15	1Fh - W	FFh	ODFT								Odd 15 Level of Grayscale
ODD14	20h - W	AFh	ODET								Odd 14 Level of Grayscale
ODD13	21h - W	79h	ODDT								Odd 13 Level of Grayscale
ODD12	22h - W	53h	ODCT								Odd 12 Level of Grayscale
ODD11	23h - W	39h	ODBT								Odd 11 Level of Grayscale
ODD10	24h - W	27h	ODAT								Odd 10 Level of Grayscale
ODD9	25h - W	1Ah	OD9T								Odd 9 Level of Grayscale
ODD8	26h - W	12h	OD8T								Odd 8 Level of Grayscale

Register name	Comd code & access	Reset	b7	b6	b5	b4	b3	b2	b1	b0	Comments
ODD7	27h - W	0Ch	OD7T								Odd 7 Level of Grayscale
ODD6	28h - W	08h	OD6T								Odd 6 Level of Grayscale
ODD5	29h - W	05h	OD5T								Odd 5 Level of Grayscale
ODD4	2Ah - W	03h	OD4T								Odd 4 Level of Grayscale
ODD3	2Bh - W	02h	OD3T								Odd 3 Level of Grayscale
ODD2	2Ch - W	01h	OD2T								Odd 2 Level of Grayscale
ODD1	2Dh - W	00h	OD1T								Odd 1 Level of Grayscale
EVEN15	2Eh - W	FFh	EVFT								Even 15 Level of Grayscale
EVEN14	2Fh - W	AFh	EVET								Even 14 Level of Grayscale
EVEN13	30h - W	79h	EVDT								Even 13 Level of Grayscale
EVEN12	31h - W	53h	EVCT								Even 12 Level of Grayscale
EVEN11	32h - W	39h	EVBT								Even 11 Level of Grayscale
EVEN10	33h - W	27h	EVAT								Even 10 Level of Grayscale
EVEN9	34h - W	1Ah	EV9T								Even 9 Level of Grayscale
EVEN8	35h - W	12h	EV8T								Even 8 Level of Grayscale
EVEN7	36h - W	0Ch	EV7T								Even 7 Level of Grayscale
EVEN6	37h - W	08h	EV6T								Even 6 Level of Grayscale
EVEN5	38h - W	05h	EV5T								Even 5 Level of Grayscale
EVEN4	39h - W	03h	EV4T								Even 4 Level of Grayscale
EVEN3	3Ah - W	02h	EV3T								Even 3 Level of Grayscale
EVEN2	3Bh - W	01h	EV2T								Even 2 Level of Grayscale
EVEN1	3Ch - W	00h	EV1T								Even 1 Level of Grayscale
RESERVED	3Dh	- -	-----------								Do not use, reserved
----	----	- -	-----------								Do not use, reserved
RESERVED	F0h	- -	-----------								Do not use, reserved
SLEEP	F1h - W	00h	-	-	-	-	-	-	-	SLEEP	Software Sleep IN/OUT
SOFTRST	F2h - W	- -	-	-	-	-	-	-	-	-	Software reset
SHRT	F3h	- -	-----------								OTP programming
RESERVED	F4h	- -	-----------								Do not use, reserved
PRGOTP	F5h		-----------								OTP programming
RESERVED	F6h	- -	-----------								Do not use, reserved
CKMM	F8h		-----------								OTP programming
RESERVED	F8h	- -	-----------								Do not use, reserved
RESERVED	----	- -	-----------								Do not use, reserved
RESERVED	FFh	- -	-----------								Do not use, reserved

Note: For information about commands F3h, F5h and F7h, see Section 11.2: OTP Memory Programming.

13.2 Command Details Ordered by Command Code

SCLKDIV - W - SCLK Clock Divider Ratio Select **Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
00h								0	0	0	0	0	SDIV		

Bit/Field Name	Reset	Function
SDIV	000b	SCLK clock divider ratio selection 000b = 1/1 001b = 1/2 010b = 1/4 011b = 1/8 100b = 1/16 101b = 1/32 110b = 1/64 111b = 1/128

BRIGHTA - W - Initial Brightness Adjustment A **Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
01h								RSELA	FDCA						

Bit/Field Name	Reset	Function
FDCA	000 0000b (00h)	00h to 7Fh: data to be stored in initial adjustment Register A
RSELA	0	Selection of input data for A adjustment D/A converter - either OTP Memory A or Register A 0 =anti-fuse OTP Memory A, default 1 = initial adjustment Register A

BRIGHTB - W - Initial Brightness Adjustment B **Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
02h								RSELB	FDCB						

Bit/Field Name	Reset	Function
FDCB	000 0000b (00h)	00h to 7Fh: data to be stored in initial adjustment Register B

Bit/Field Name	Reset	Function
RSELB	0	Selection of input data for B adjustment D/A converter - either OTP Memory B or Register B 0 =anti-fuse OTP Memory B, default 1 = initial adjustment Register B

DCDCCTRL - W - DC/DC Step-up Converter Control   Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
03h								0	0	0	0	FDCDC		VRSL	DCDCON

Bit/Field Name	Reset	Function
DCDCON	0	DC/DC converter enable 0 = disabled (default) 1 = enabled
VRSL	0	DC/DC converter control loop tracking selection 0 = tracking with VF voltage (default) 1 =tracking with internal bandgap voltage, V_{BG} (see Figure 28)
FDCDC	00b	DC/DC converter operating frequency in PWM mode 00b = 150KHz (default) 01b = 200KHz 10b = 250KHz 11b = 300KHz

VFDETVAL - W - Selection of Voltage to Add as Adjustment to VH   Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
06h								0	0	0	0	0	VFOP		

Bit/Field Name	Reset	Function
VFOP	000b	Selection of voltage to add to pad VF to produce VH, the output of DC/DC converter. In general, VH = VF + V_{FOP} where according to field VFOP, V_{FOP} is: 000b = 1.5V 001b = 1.786V 010b = 2.072V … 110b = 3.214V 111b = 3.5V Note: 1LSB of field VFOP is approximately 286mV.

DCTRL - W - Dot-Matrix Display Control   Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
10h								0	0	0	0	0	DINV	DALI	DISP ON

Bit/Field Name	Reset	Function
DISPON	0	Dot-Matrix display ON/OFF 0 = Display OFF, DC/DC is ON or OFF according to bit DCDCON of register DCDCCTRL, Column and Row outputs are set to GNDL, Scanning is OFF 1 = Display ON
DALI	0	Dot-Matrix all points or pixel lights ON/OFF (applies with bit DISPON = 1) 0 = all pixel lights OFF (command disabled) 1 = all pixel lights ON
DINV	0	“Reversal” of Dot-Matrix display contents 0 = display contents not “reversed” (command disabled) 1 = display contents “reversed” (reversal operation is applied on data in Display RAM which is in read mode

DOTMTRXDIR - W - Dot-Matrix Display Direction   Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
11h								0	0	DUMM		0	0	VTUR	HTUR

Bit/Field Name	Reset	Function
HTUR	0	Invert image in horizontal direction (inversion is performed at the time of writing data) 0 = image inversion OFF 1 = image inversion ON (see Figure 24)
VTUR	0	Invert image in vertical direction 0 = image inversion OFF 1 = image inversion ON (see Figure 23)
DUMM	00b	Number of Dummy Lines to precede Scan line 00b = one dummy line to precede scan line 01b = two dummy lines to precede scan line 10b = four dummy lines ““ 11b = eight dummy lines ““

DOTMTRXSCAN - W - Dot-Matrix Scan Line Select   Default value: 47h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
12h								0	SCLN						

Bit/Field Name	Reset	Function
SCLN	1000111 (47h)	Scan line select 000 0000b = Line 1 selected as Scan line 000 0001b = Line 2 selected as Scan line … 100 0110b = Line 71 selected as Scan line 100 0111b = Line 72 selected as Scan line (default) 100 1000b = Do not use … 111 1110b = Do not use) 111 1111b = Do not use

RAMXSTART - W - Display RAM X Starting Address   Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
13h								X	X	X	X	X	X	X	X

Data	Reset	Function
00h to FFh	00h	Display RAM X Address starting value

RAMYSTART - W - Display RAM Y Starting Address   Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
14h								X	X	X	X	X	X	X	X

Data	Reset	Function
00h to FFh	00h	Display RAM Y Address starting value

GSADDINC - W - Grayscale Mode Sel. and Disp. RAM Addr. Increment   Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
15h								GSMODE				0	0	YINC	XINC

Bit/Field Name	Reset	Function
XINC	0	Automatic increment of Display RAM X address 0 = increment OFF 1 = increment ON

Bit/Field Name	Reset	Function
YINC	0	Automatic increment of Display RAM Y address 0 = increment OFF 1 = increment ON
GSMODE	0000b	Gray scale mode selection 0000b = 16 gray scale mode 0001b = do not use 0010b = 4 gray scale mode, picture 1 0011b = 4 gray scale mode, picture 2 0100b = 64 gray scale mode 1 0101b = 64 gray scale mode 2 0110b = do not use 0111b = do not use 1000b = monochrome mode, picture 1 1001b = monochrome mode, picture 2 1010b = monochrome mode, picture 3 1011b = monochrome mode, picture 4 1100b = do not use 1101b = do not use 1110b = do not use 1111b = do not use

DIMMERCTRL - W - Dimmer Control   Default value: 0Fh

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
16h								0	0	0	DIMM				

Bit/Field Name	Reset	Function
DIMM	0 1111 (0Fh)	Dimmer select, i.e. fraction of reference current to mirror as output current for each column. In general, I_{COUTn} = Irefn $\times$ fract[DIMM] where n = 1 or 2 and fract[DIMM] is related to the value of field DIMM as follows: 0 0000b = 1/16 0 0001b = 2/16 0 0010b = 3/16 … 0 1111b = 16/16 (default) 1 0000b = 17/16 … 1 1101b = 30/16 1 1110b = 31/16 1 1111b = 32/16 Note: A luminosity control adjustment is performed synchronous with VSYNCIN when bit DISPON of register DCTRL is “1”. Otherwise, i.e. when DISPON is “0”, it is performed immediately after the command DIMMERCTRL is issued.

ROWDRVSEL - W - Row Driver Mode Selection

Default value: 02h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
17h								0	0	0	RDIR	0	0	RMODE	

Bit/Field Name	Reset	Function
RMODE	10b	Row driver mode selection 00b = do not use, reserved 01b = do not use, reserved 10b = Internal Row driver, Single scanning 72 line mode (default) 11b = Internal Row driver, Dual scanning mode, max. 36 lines, even and odd Row outputs driven simultaneously
RDIR	0	Row driver scanning direction 0 = R1 to R72 (64 lines), default 1 = R72 (64 lines) to R1

COLCTRL - W - Column Output Control

Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
1Ah												CLLM	CLLZ	HSLZ	OFLZ

Bit/Field Name	Reset	Function
OFLZ	0	Column output control: during the drive period, after the PWM current sourcing period, the column output is forced to: 0 = GNDL 1 = Hi-Z (only if CLLM and CLLZ are “0”)
HSLZ	0	HSYNCOUT output control: during the HSYNC pulse, the HSYNCOUT output is forced to: 0 = GNDL 1 = Hi-Z (only if CLLM and CLLZ are “0”)
CLLZ	0	Column drivers all in Hi-Z. All column outputs are set to Hi-Z during the setup and drive periods. (Scanning operation is as usual. All outputs are in Hi-Z.) 0 = OFF (command disabled) 1 = All column outputs in Hi-Z (ON)
CLLM	0	Column outputs all at VCOL. All column outputs are set to VCOL1 or VCOL2 in all periods. (Scanning operation is as usual. All outputs are at VCOL1 or VCOL2.) This setup is effective at the time of CLLZ = “0” 0 = OFF (command disabled) 1 = All column outputs at VCOL (ON)

OELPERIOD1 - W - Setup Period 1 command **Default value: 0Fh**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
1Bh								E1ST		E1CL					

Bit/Field Name	Reset	Function
E1CL	00 1111b (0Fh)	Setup Period 1, number of clock pulses The number of clocks in setup period 1 is: 11 1111b = 64 SCLK 11 1110b = 63 SCLK … 00 1111b = 16SCLK (default) … 00 0001b = 2 SCLK 00 0000b = 1 SCLK
E1ST	00b	Selection of column output level during Setup Period 1 00 = column outputs at GNDL 01 = outputs placed in Hi-Z 10 = outputs connected to VCOL 11 = column outputs source a constant current determined by the dimmer and brightness adjustments This setup is effective at the time CLLM and CLLZ are “0” When the level of gray scale data is 0, Setup Period 1 is compulsorily set to GNDL even if VPP, VCOL or Hi-Z was chosen.

OELPERIOD2 - W - Setup Period 2 command **Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
1Ch								E2ST		E2CL					

Bit/Field Name	Reset	Function
E2CL	00 0000b	Setup Period 2, number of clock pulses The number of clocks in setup period 2 is: 11 1111b = 64 SCLK 11 1110b = 63 SCLK … 00 0001b = 2 SCLK 00 0000b = 1 SCLK (default)
E2ST	00b	Selection of column output level during Setup Period 2 00 = column outputs at GNDL 01 = outputs placed in Hi-Z 10 = outputs connected to VCOL 11 = column outputs source a constant current determined by the dimmer and brightness adjustments This setup is effective at the time CLLM and CLLZ are “0” When the level of gray scale data is 0, Setup Period 2 is compulsorily set to GNDL even if VPP, VCOL or Hi-Z was chosen.

OELPERIOD3 - W - Setup Period 3 command **Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
1Dh								E3ST		E3CL					

Bit/Field Name	Reset	Function
E3CL	00 0000b	Setup Period 3, number of clock pulses The number of clocks in setup period 3 is: 11 1111b = 64 SCLK 11 1110b = 63 SCLK … 00 0001b = 2 SCLK 00 0000b = 1 SCLK (default)
E3ST	00b	Selection of column output level during Setup Period 3 00 = column outputs at GNDL 01 = outputs placed in Hi-Z 10 = outputs connected to VCOL 11 = column outputs source a constant current determined by the dimmer and brightness adjustments This setup is effective at the time CLLM and CLLZ are “0” When the level of gray scale data is 0, Setup Period 3 is compulsorily set to GNDL even if VPP, VCOL or Hi-Z was chosen.

OELPERIOD4 - W - Setup Period 4 command Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
1Eh								E4ST		E4CL					

Bit/Field Name	Reset	Function
E4CL	00 0000b	Setup Period 4, number of clock pulses The number of clocks in setup period 4 is: 11 1111b = 64 SCLK 11 1110b = 63 SCLK … 00 0001b = 2 SCLK 00 0000b = 1 SCLK (default)
E4ST	00b	Selection of column output level during Setup Period 4 00 = column outputs at GNDL 01 = outputs placed in Hi-Z 10 = outputs connected to VCOL 11 = column outputs source a constant current determined by the dimmer and brightness adjustments This setup is effective at the time CLLM and CLLZ are “0” When the level of gray scale data is 0, Setup Period 4 is compulsorily set to GNDL even if VPP, VCOL or Hi-Z was chosen.

ODD15 - W - Loading byte 15 of the ODD gray scale lookup table Default value: FFh

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
1Fh								ODFT							

Bit/Field Name	Reset	Function
ODFT	FFh	Number of SCLK clock periods for the odd 15th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD14 - W - Loading byte 14 of the ODD gray scale lookup table **Default value: AFh**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
20h								ODET							

Bit/Field Name	Reset	Function
ODET	AFh	Number of SCLK clock periods for the odd 14th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD13 - W - Loading byte 13 of the ODD gray level lookup table **Default value: 79h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
21h								ODDT							

Bit/Field Name	Reset	Function
ODDT	79h	Number of SCLK clock periods for the odd 13th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD12 - W - Loading byte 12 of the ODD gray scale lookup table **Default value: 53h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
22h								ODCT							

Bit/Field Name	Reset	Function
ODCT	53h	Number of SCLK clock periods for the odd 12th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD11 - W - Loading byte 11 of the ODD gray scale lookup table **Default value: 39h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
23h								ODBT							

Bit/Field Name	Reset	Function
ODBT	39h	Number of SCLK clock periods for the odd 11th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD10 - W - Loading byte 10 of the ODD gray scale lookup table **Default value: 27h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
24h								ODAT							

Bit/Field Name	Reset	Function
ODAT	27h	Number of SCLK clock periods for the odd 10th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD9 - W - Loading byte 9 of the ODD gray scale lookup table **Default value: 1Ah**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
25h								OD9T							

Bit/Field Name	Reset	Function
OD9T	1Ah	Number of SCLK clock periods for the odd 9th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD8 - W - Loading byte 8 of the ODD gray scale lookup table **Default value: 12h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
26h								OD8T							

Bit/Field Name	Reset	Function
OD8T	12h	Number of SCLK clock periods for the odd 8th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD7 - W - Loading byte 7 of the ODD gray scale lookup table **Default value: 0Ch**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
27h								OD7T							

Bit/Field Name	Reset	Function
OD7T	0Ch	Number of SCLK clock periods for the odd 7th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD6 - W - Loading byte 6 of the ODD gray level lookup table Default value: 08h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
28h								OD6T							

Bit/Field Name	Reset	Function
OD6T	08h	Number of SCLK clock periods for the odd 6th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD5 - W - Loading byte 5 of the ODD gray level lookup table Default value: 05h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
29h								OD5T							

Bit/Field Name	Reset	Function
OD5T	05h	Number of SCLK clock periods for the odd5th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD4 - W - Loading byte 4 of the ODD gray level lookup table **Default value: 03h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
2Ah								OD4T							

Bit/Field Name	Reset	Function
OD4T	03h	Number of SCLK clock periods for the odd 4th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

ODD3 - W - Loading byte 3 of the ODD gray level lookup table **Default value: 02h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
2Bh								OD3T							

Bit/Field Name	Reset	Function
OD3T	02h	Number of SCLK clock periods for the odd 3rd level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 64 level gray scale and monochrome.

ODD2 - W - Loading byte 2 of the ODD gray level lookup table **Default value: 01h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
2Ch								OD2T							

Bit/Field Name	Reset	Function
OD2T	01h	Number of SCLK clock periods for the odd 2nd level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 64 level gray scale and monochrome.

ODD1 - W - Loading byte 1 of the ODD gray level lookup table **Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
2Dh								OD1T							

Bit/Field Name	Reset	Function
OD1T	00h	Number of SCLK clock periods for the odd 1st level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent while display is in 64 level gray scale mode

EVEN15 - W - Loading byte 15 of the EVEN gray level lookup table **Default value: FFh**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
2Eh								EVFT							

Bit/Field Name	Reset	Function
EVFT	FFh	Number of SCLK clock periods for the even 15th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN14 - W - Loading byte 14 of the EVEN gray level lookup table Default value: AFh

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
2Fh								EVET							

Bit/Field Name	Reset	Function
EVET	AFh	Number of SCLK clock periods for the even 14th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN13 - W - Loading byte 13 of the EVEN gray level lookup table Default value: 79h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
30h								EVDT							

Bit/Field Name	Reset	Function
EVDT	79h	Number of SCLK clock periods for the even 13th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN12 - W - Loading byte 12 of the EVEN gray level lookup table Default value: 53h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
31h								EVCT							

Bit/Field Name	Reset	Function
EVCT	53h	Number of SCLK clock periods for the even 12th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN11 - W - Loading byte 11 of the EVEN gray level lookup table Default value: 39h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
32h								EVBT							

Bit/Field Name	Reset	Function
EVBT	39h	Number of SCLK clock periods for the even 11th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN10 - W - Loading byte 10 of the EVEN gray level lookup table Default value: 27h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
33h								EVAT							

Bit/Field Name	Reset	Function
EVAT	27h	Number of SCLK clock periods for the even 10th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN9 - W - Loading byte 9 of the EVEN gray level lookup table   Default value: 1Ah

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
34h								EV9T							

Bit/Field Name	Reset	Function
EV9T	1Ah	Number of SCLK clock periods for the even 9th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN8 - W - Loading byte 8 of the EVEN gray level lookup table   Default value: 12h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
35h								EV8T							

Bit/Field Name	Reset	Function
EV8T	12h	Number of SCLK clock periods for the even 8th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN7 - W - Loading byte 7 of the EVEN gray level lookup table   Default value: 0Ch

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
36h								EV7T							

Bit/Field Name	Reset	Function
EV7T	0Ch	Number of SCLK clock periods for the even 7th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN6 - W - Loading byte 6 of the EVEN gray level lookup table Default value: 08h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
37h								EV6T							

Bit/Field Name	Reset	Function
EV6T	08h	Number of SCLK clock periods for the even 6th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN5 - W - Loading byte 5 of the EVEN gray level lookup table Default value: 05h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
38h								EV5T							

Bit/Field Name	Reset	Function
EV5T	05h	Number of SCLK clock periods for the even 5th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN4 - W - Loading byte 4 of the EVEN gray level lookup table   Default value: 03h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
39h								EV4T							

Bit/Field Name	Reset	Function
EV4T	03h	Number of SCLK clock periods for the even 4th level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 4 level gray scale, 64 level gray scale and monochrome.

EVEN3 - W - Loading byte 3 of the EVEN gray scale lookup table   Default value: 02h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
3Ah								EV3T							

Bit/Field Name	Reset	Function
EV3T	02h	Number of SCLK clock periods for the even 3rd level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 64 level gray scale and monochrome.

EVEN2 - W - Loading byte 2 of the EVEN gray level lookup table   Default value: 01h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
3Bh								EV2T							

Bit/Field Name	Reset	Function
EV2T	01h	Number of SCLK clock periods for the even 2nd level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent in the following display modes: 64 level gray scale and monochrome.

EVEN1 - W - Loading byte 1 of the EVEN gray level lookup table — Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
3Ch								EV1T							

Bit/Field Name	Reset	Function
EV1T	00h	Number of SCLK clock periods for the even 1st level of gray 0000 0000b = 1 SCLK … 0111 1111b = 128 SCLK … 1111 1111b = 256 SCLK Note: this command is not to be sent while display is in 64 level gray scale mode.

SLEEP - W - Software Sleep IN/OUT Select — Default value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
F1h								X	X	X	X	X	X	X	SLEEP

Bit/Field Name	Reset	Function
SLEEP	0	Software Sleep IN/OUT selection 0 = exit from sleep mode (OUT of sleep mode) 1 = enter sleep mode (IN sleep mode)

SOFTRST - W - Software Reset — Default value: - -h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
F2h								X	X	X	X	X	X	X	X

Bit/Field Name	Reset	Function
- -	- -	Approx. 200ns max after sending or issuing this command, the state of the STV8105 becomes: • oscillator ON • DC/DC Converter remains OFF but waiting for a command • Column drivers at GNDL but also waiting for a command • internal Row drivers at GNDL (waiting for a command) • external Driver Control: SCLK_OUT = SCLK Clock output • external IC controls VSYNCOUT, HSYNCOUT, RCTRLA, RCTRLB and ROWDATA are at GND • all Registers are at their default values (waiting for a command) For more information see Section 12.1.

Note: For information about commands F3h, F5h and F7h, see Section 11.2: OTP Memory Programming.

14 Electrical Characteristics

14.1 Absolute Maximum Ratings

Maximum ratings are the values beyond which damage to the device may occur. Functional operation should be restricted to the limits defined in the electrical characteristics table.

Symbol	Parameter	Value	Units
V_{DD}	Controller Supply Range	-0.3, +4.6	V
V_{bat}	Battery Supply Range	-0.3, +18	V
V_{PP}	Analog Display Supply Range	-0.3, +27	V
I_{PP}	DC Display Current Range	TBD	mA
V_{DC}	“Buffer” Supply Range	-0.3, +12	V
V_{PRG}	OTP Programming Supply	-0.3, +20	V
V_{INPUT}	Logic Input Voltage Range	-0.3, V_{DD}+0.3	V
I_{INPUT}	DC Logic Input Current Range	10	mA
V_{ESD}	ESD Susceptibility, Human Body Model (100pF discharged through 1.5Kohms)[1]	2.0	KV
T_J	Junction Temperature	125	°C
T_{STOR}	Storage Temperature	-50, +150	°C

1. Pad VHSENSE and pads R1 to R72 sustain 1KV

14.2 Thermal Data

Symbol	Parameter	Value	Units
R_{thJA}	Junction-ambient Thermal Resistance (Maximum) on a single-layer board	TBD	°C/W

14.3 Recommended Operating Conditions

VDD = 3.3V, VPP1 =VPP2 = 18V, GND = GNDL = 0V,
T_{amb} = 25°C and frame frequency f_{VSYNC} = 75Hz unless otherwise specified.

14.3.1 DC Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DD}	Controller Supply voltage		3.0	3.3	3.6	V
I_{DD}	Controller Supply current		-	TBD	-	µA
V_{bat}	Battery voltage range for step-up DCDC converter		3		12	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{PP}	Display Supplies, VPP1 and VPP2	From external step-up convertor	V_{bat} - V_{diode}	18	25	V
		From external supply	6.0	-	25	V
V_{PRG}	OTP Supply Voltage[1]		14.0		18.0	V
I_{PRG}	OTP Supply Current[2]		250		TBD	mA
$I_{STANDBY}$	Standby Current	Device biased but not operating (standby mode)			TBD	µA
V_{IL}	Low level of input logic signal		GND		0.2 x V_{DD}	V
V_{IH}	High level of input logic signal		0.8 x V_{DD}		V_{DD}	V
I_{IL}	Low level Input current of logic signals	$V_{IL} = 0V$			1	µA
I_{IH}	High level Input current of logic signals	$V_{IH} = 0V$			1	µA
V_{OL}	Low level output signal	Output sinking < 1mA	GND		0.2 x V_{DD}	V
V_{OH}	High level output signal	Output sourcing < 1mA	0.8 x V_{DD}		V_{DD}	V

1. V_{PRG} is to be applied only when programming the non-volatile OTP memory.
2. When applying V_{PRG}, I_{PRG} should forced to at least 250mA to assure complete “blowing” of the anti-fuse structure associated with an OTP memory bit.

14.3.2 Timing Generator

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{CLK}	Oscillation Frequency	External RC or Crystal		2.4	24	MHz
f_{CRC}	Internal Clock Frequency	Internal RC oscillator	2.04	2.40	2.76	MHz
f_{EXT}	External Clock Input		0.1		10	MHz
Duty	Clock Duty	Crystal, RC oscillation	45	50	55	%
		External Clock Input	45	50	55	%
f_{SYS}	System Operation Frequency	System Clock		2.4		MHz
f_{VSYNC}	Frame Frequency	Default configuration, 75Hz		75		Hz
f_{HSYNC}	Row Frequency			TBD		Hz

14.3.3 Row Drivers

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{ROW}	Sink row Supply Current	Maximum Brightness			110	mA
V_{ROWON}	ROW ON Voltage drop	I_{ROW} = 110mA, V_{DD} = 3.3V		TBD		V
R_{ROWOFF}	R_{DSON} of Row high side transistor			1.0	TBD	Kohms

14.3.4 Column Drivers

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{COL}	Column Supply Current	Minimum Brightness, 01h Maximum Brightness, 1Fh		-1.3 -800		µA µA
R_{COL}	Column output impedance during precharge	I_{OUT} = -200uA		1.0	TBD	Kohms
R_{COLDIS}	Column output impedance during discharge	I_{OUT} = +200uA		1.0	TBD	Kohms
D_{COL}	Column differential uniformity $D_{COL} = ABS(I_{COL\_N} - I_{COL\_N+1})/I_{AVG1}$, $I_{AVG1} = (I_{COL\_N} + I_{COL\_N+1})/2$	I_{OUT} = 200uA Intermediate All outputs		1.0 2.5		% %
D_{CHIP}	Device differential uniformity $D_{CHIP} = ABS(I_{COL\_MAX} - I_{COL\_MIN})/I_{AVG2}$, and $I_{AVG2} = (I_{COL\_1}$ + to + $I_{COL\_256})/256$			5		%
D_{ICOL}	Average current deviation against absolute level	Icol = 200µA RREF1 and RREF2: 1%		TBD		%
I_{OFF}	Output Leakage Current	All outputs OFF			2	µA

14.3.5 Current Reference and Brightness Adjustment D/A Converter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Vref1	Voltage Reference1		0.64		2.77	V
Iref1	Current Reference1		-400		-32	µA
Vref2	Voltage Reference2		0.64		2.77	V
Iref2	Current Reference2		-400		-32	µA
Dres	D/A Converter Resolution			7		Bit
VDH	D/A Output maximum Voltage	Reg 01h/Reg 02h = 1Fh	2.61	2.69	2.77	V
VDL	D/A Output minimum Voltage	Reg 01h/Reg 02h = 00h	0.64	0.66	0.68	V
DLE	D/A differentiation linearity error		-1/2		+1/2	LSB

14.3.6 DC/DC Converter

VDD = 3.3V, VDC = V_{bat} = 6.0V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_H	Step-up output voltage range	V_{bat} = 3.0V, I_{OUT} = 10 mA		18.0	25.0	V
I_{OUT}	Output current range	V_H = 18V, in PWM mode (pad TON/$\overline{F}$ = GND)		TBD	150	mA
V_{DC}	"Buffer" supply range		3.0	5.0	10.0	V
V_{SENSE}	VSENSE control voltage	VCOMP = VSENSE	1.21	1.25	1.29	V
DC_HUVLO	DC supply "start" voltage			2.77		V
DC_LUVLO	DC supply "off" voltage			2.54		V
IDC_STBY	DC supply standby current	VDC = 10V, Reg 03h, DCDCON = "0"		10		µA
f_{SWI}	Switching frequency	Reg 03h, FDCDC = 00b Reg 03h, FDCDC = 11b		150 300		KHz KHz
V_{DRIVEH}	External MOS gate drive ON	I_{DRIVE} = TBD		-	V_{DC}	V
V_{DRIVEL}	External MOS gate drive OFF	I_{DRIVE} = TBD	GND	-		V
$V_{DRIVECYCLE}$	External MOS gate: turn ON duty cycle		0		80	%
PFMDTY	PFM duty rate	No Load		90		%
Efficiency				TBD		%

14.3.7 Voltage Generators

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{COL1,2}$	Column precharge power supply		3		25	V
$V_{ROW1,2}$	Row-off power supply		6	12	25	V

14.3.8 Reset Input

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Tr	Reset Completed Time				50	µs
Trw	Reset Pulse Width (for valid reset)		5			µs
Trw	Reset Rejection				1	µs
Trs	Software Reset Completed Time				200	ns

Figure 42: Reset Timing

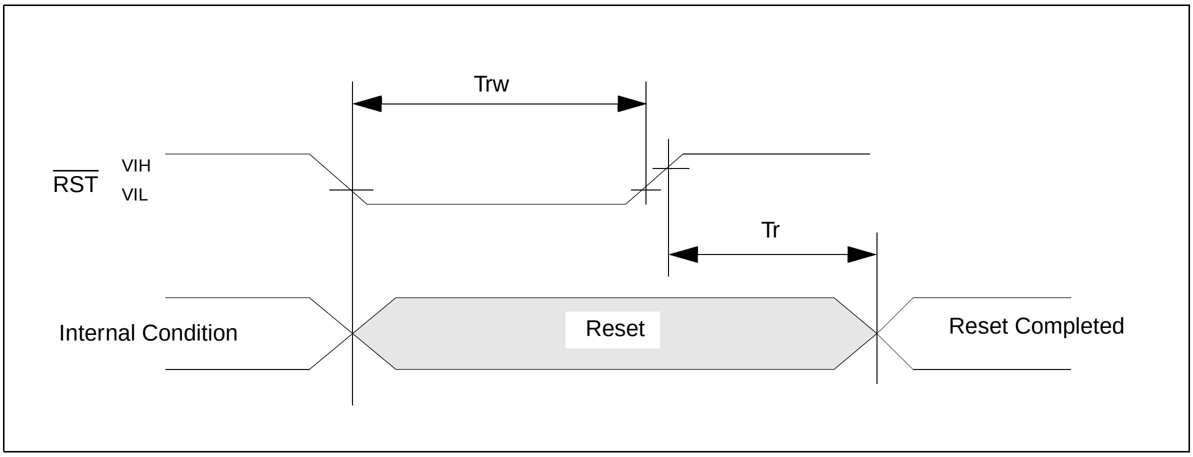
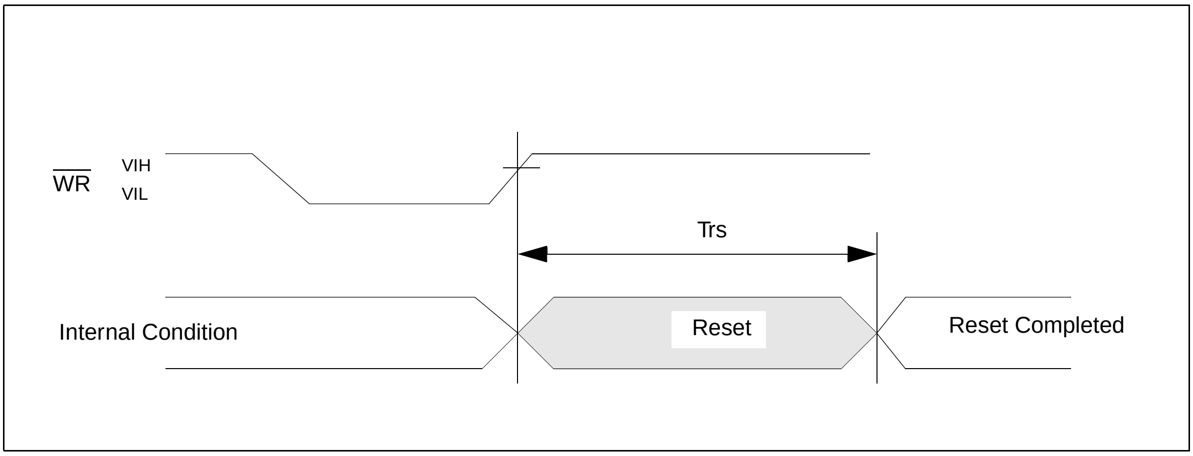


Figure 43: Reset Timing



15 Revision History

The following table summarizes the modifications applied to this document.

Date	Revision	Changes
05-Sep-2005	1	Draft
03-Mar-2006	1.1	Renaming and grouping of certain pad names reserved for test by ST.