ST7793

240RGB x 432 dot 262 Color with Frame Memory
Single-Chip TFT Controller/Driver

Datasheet
Version 1.2
2014/08

Sitronix Technology Corporation

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1 GENERAL DESCRIPTION

The ST7793 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 720 source lines and 432 gate lines driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts 8-bit/9-bit/16-bit/18-bit parallel interface, SPI, and MDDI. Display data can be stored in the on-chip display data RAM of 240x432x18 bits. It can perform display data RAM read-/write-operation with no external clock to minimize power consumption. In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with fewest components.
2 FEATURES

- Single chip TFT-LCD Controller/Driver with On-chip Frame Memory
- Display Resolution: 240*RGB (H) *432(V)
- Frame Memory Size: 240 x 432 x 18-bit = 1,866,240 bits
- LCD Driver Output Circuits
  - Source Outputs: 240 RGB Channels
  - Gate Outputs: 432 Channels
  - Common Electrode Output
- Display Colors (Color Mode)
  - Full Color: 262K, RGB=(666) max., Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- Programmable Pixel Color Format (Color Depth) for Various Display Data Input Format
  - 16-bit/pixel: RGB=(565)
  - 18-bit/pixel: RGB=(666)
- Interface
  - Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit, and 18-bit)
  - 16/18 RGB Interface (VSYNCX, HSYNCX, DOTCLK, ENABLE, DB[17:0])
  - Serial Peripheral Interface (SPI Interface)
  - VSYNC Interface (8080-series MCU Interface + VSYNCX)
  - FMARK Interface (8080-series MCU Interface + FMARK)
  - MDDI (Type 1)
- Display Features
  - Partial Display Function
  - 8-color Display Function
  - Vertical Scroll Function
- Support LC Type Option
  - MVA LC Type
  - Transflective LC Type
  - Transmissive LC Type
- On Chip Build-In Circuits
  - DC/DC Converter
  - Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
  - Internal Oscillator for Display Clock Generation
  - Timing Controller
- Build-In NV Memory for LCD Initial Register Setting
  - 8-bit for ID
- 7-bit for flicker adjustment

- Driving Algorithm
  - Dot Inversion
  - Column Inversion

- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ VDD
  - Voltage for Digital Circuit (VDD to DGND): 2.5V ~ 3.3V
  - Voltage for Analog Circuit (VDDA to AGND): 2.5V ~ 3.3V

- On-Chip Power System
  - Source Voltage: +6.4 ~ -4.2
  - VCOM Level: AGND
  - Gate Driver HIGH Level (VGH to AGND): +12.16V ~ +15.05V
  - Gate Driver LOW Level (VGL to AGND): -12.37V ~ -7.7V
  - Max. VGH – VGL: 27.4V

- Optimized layout for COG Assembly
- Operate temperature range: −30ºC to +85 ºC
- Lower Power Consumption
3 PAD ARRANGEMENT

3.1. Output Bump Dimension

<table>
<thead>
<tr>
<th>Au bump height</th>
<th>9 μm</th>
</tr>
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<tr>
<td>Au bump size</td>
<td></td>
</tr>
<tr>
<td>15μm×100μm</td>
<td></td>
</tr>
<tr>
<td>Gate : G1~G432</td>
<td></td>
</tr>
<tr>
<td>Source : S1~S720</td>
<td>(Pad263 to Pad1434)</td>
</tr>
<tr>
<td>50μm×90μm</td>
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<tr>
<td>(Pad1 to Pad262)</td>
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Bump View
3.2.. Bump Dimension

● Output Pads

Pad No.263~1434

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<tr>
<td>A</td>
<td>Bump Width</td>
<td>15 um</td>
</tr>
<tr>
<td>B</td>
<td>Bump Gap 1 (Horizontal)</td>
<td>15 um</td>
</tr>
<tr>
<td>C</td>
<td>Bump Height</td>
<td>100 um</td>
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<tr>
<td>D</td>
<td>Bump Gap 2 (Vertical)</td>
<td>19 um</td>
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● Input Pads

Pad No.1~262

<table>
<thead>
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<th>Symbol</th>
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<tr>
<td>E</td>
<td>Bump Width</td>
<td>50 um</td>
</tr>
<tr>
<td>F</td>
<td>Bump Gap</td>
<td>20 um</td>
</tr>
<tr>
<td>G</td>
<td>Bump Height</td>
<td>90 um</td>
</tr>
<tr>
<td>H</td>
<td>Bump Pitch</td>
<td>70 um</td>
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3.3. Alignment Mark Dimension

- Alignment Mark: \( A1(X,Y)=(-9381,-208) \)

![Alignment Mark A1](image1)

- Alignment Mark: \( A2(X,Y)=(9381,-208) \)

![Alignment Mark A2](image2)

3.4. Chip Information

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<th>19030(\mu)m x 837(\mu)m</th>
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<tr>
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<td>Pad center</td>
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<th>Y</th>
<th>PAD No.</th>
<th>PIN Name</th>
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<th>Y</th>
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<tr>
<td>1</td>
<td>DUMMYR1</td>
<td>-9135</td>
<td>-301</td>
<td>34</td>
<td>AGND</td>
<td>-6825</td>
<td>-301</td>
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<td>2</td>
<td>DUMMYR2</td>
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<td>-301</td>
<td>35</td>
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<td>AGNDDUM1</td>
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<td>-8872.5</td>
<td>200</td>
</tr>
<tr>
<td>1400</td>
<td>G61</td>
<td>-8887.5</td>
<td>319</td>
</tr>
<tr>
<td>1401</td>
<td>G59</td>
<td>-8902.5</td>
<td>319</td>
</tr>
<tr>
<td>1402</td>
<td>G57</td>
<td>-8917.5</td>
<td>319</td>
</tr>
<tr>
<td>1403</td>
<td>G55</td>
<td>-8932.5</td>
<td>319</td>
</tr>
<tr>
<td>1404</td>
<td>G53</td>
<td>-8947.5</td>
<td>319</td>
</tr>
<tr>
<td>1405</td>
<td>G51</td>
<td>-8962.5</td>
<td>319</td>
</tr>
<tr>
<td>1406</td>
<td>G49</td>
<td>-8977.5</td>
<td>319</td>
</tr>
<tr>
<td>1407</td>
<td>G47</td>
<td>-8992.5</td>
<td>319</td>
</tr>
<tr>
<td>1408</td>
<td>G45</td>
<td>-9007.5</td>
<td>319</td>
</tr>
<tr>
<td>1409</td>
<td>G43</td>
<td>-9022.5</td>
<td>319</td>
</tr>
<tr>
<td>1410</td>
<td>G41</td>
<td>-9037.5</td>
<td>319</td>
</tr>
<tr>
<td>1411</td>
<td>G39</td>
<td>-9052.5</td>
<td>319</td>
</tr>
<tr>
<td>1412</td>
<td>G37</td>
<td>-9067.5</td>
<td>319</td>
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<tr>
<td>1413</td>
<td>G35</td>
<td>-9082.5</td>
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</tr>
<tr>
<td>1414</td>
<td>G33</td>
<td>-9097.5</td>
<td>319</td>
</tr>
<tr>
<td>1415</td>
<td>G31</td>
<td>-9112.5</td>
<td>319</td>
</tr>
<tr>
<td>1416</td>
<td>G29</td>
<td>-9127.5</td>
<td>319</td>
</tr>
<tr>
<td>1417</td>
<td>G27</td>
<td>-9142.5</td>
<td>319</td>
</tr>
<tr>
<td>1418</td>
<td>G25</td>
<td>-9157.5</td>
<td>319</td>
</tr>
<tr>
<td>1419</td>
<td>G23</td>
<td>-9172.5</td>
<td>319</td>
</tr>
<tr>
<td>1420</td>
<td>G21</td>
<td>-9187.5</td>
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</tr>
<tr>
<td>1421</td>
<td>G19</td>
<td>-9202.5</td>
<td>319</td>
</tr>
<tr>
<td>1422</td>
<td>G17</td>
<td>-9217.5</td>
<td>319</td>
</tr>
<tr>
<td>1423</td>
<td>G15</td>
<td>-9232.5</td>
<td>319</td>
</tr>
<tr>
<td>1424</td>
<td>G13</td>
<td>-9247.5</td>
<td>319</td>
</tr>
<tr>
<td>1425</td>
<td>G11</td>
<td>-9262.5</td>
<td>319</td>
</tr>
<tr>
<td>1426</td>
<td>G9</td>
<td>-9277.5</td>
<td>319</td>
</tr>
<tr>
<td>PAD No.</td>
<td>PIN Name</td>
<td>X</td>
<td>Y</td>
</tr>
<tr>
<td>---------</td>
<td>------------</td>
<td>--------</td>
<td>-----</td>
</tr>
<tr>
<td>1427</td>
<td>G7</td>
<td>-9292.5</td>
<td>200</td>
</tr>
<tr>
<td>1428</td>
<td>G5</td>
<td>-9307.5</td>
<td>319</td>
</tr>
<tr>
<td>1429</td>
<td>G3</td>
<td>-9322.5</td>
<td>200</td>
</tr>
<tr>
<td>1430</td>
<td>G1</td>
<td>-9337.5</td>
<td>319</td>
</tr>
<tr>
<td>1431</td>
<td>VGLDMY4</td>
<td>-9352.5</td>
<td>200</td>
</tr>
<tr>
<td>1432</td>
<td>DUMMY</td>
<td>-9367.5</td>
<td>319</td>
</tr>
<tr>
<td>1433</td>
<td>DUMMYR3</td>
<td>-9382.5</td>
<td>200</td>
</tr>
<tr>
<td>1434</td>
<td>DUMMYR4</td>
<td>-9397.5</td>
<td>319</td>
</tr>
</tbody>
</table>

Unit: µm
5 BLOCK DIAGRAM

- 720 Source Buffer
- DAC
- Level Shifter
- Data Latch
- Display Ram 240x432x18 bits
- Gamma Circuit
- Gamma Table
- Display Control
- Instruction Register
- NVM
- Booster
- Interface
- 432 Gate Buffer
- Level Shifter
- Gate Decoder
- OSC
- S1 ~ S720
- G1 ~ G432
- AVDD
- VDD
- VCOM
- AVCL
- VDDI
- DB[17:0]/MDDI Data/MDDI STB
- RDX
- WRX/SCL
- CSX
- DCX
- IM[2:0]
- RESET
- DOTCLK
- ENABLE
- VSYNCX
- HSYNCX
- VGH
- VGL
- DOTCLK
- HDIS
- DSYNC
- DGT
- DDATA
- G1 ~ G432
- S1 ~ S720
### 6 DISPLAY RAM ADDRESS MAP


<table>
<thead>
<tr>
<th>X Address</th>
<th>Y Address</th>
<th>X Address</th>
<th>Y Address</th>
<th>X Address</th>
<th>Y Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;0000&quot;h</td>
<td>&quot;0000&quot;h</td>
<td>&quot;0001&quot;h</td>
<td>&quot;0001&quot;h</td>
<td>&quot;0001&quot;h</td>
<td>&quot;0001&quot;h</td>
</tr>
<tr>
<td>&quot;00EE&quot;h</td>
<td>&quot;00EE&quot;h</td>
<td>&quot;00EF&quot;h</td>
<td>&quot;00EF&quot;h</td>
<td>&quot;0000&quot;h</td>
<td>&quot;0000&quot;h</td>
</tr>
<tr>
<td>&quot;001E&quot;h</td>
<td>&quot;001E&quot;h</td>
<td>&quot;001E&quot;h</td>
<td>&quot;001E&quot;h</td>
<td>&quot;001E&quot;h</td>
<td>&quot;001E&quot;h</td>
</tr>
<tr>
<td>&quot;001F&quot;h</td>
<td>&quot;001F&quot;h</td>
<td>&quot;001F&quot;h</td>
<td>&quot;001F&quot;h</td>
<td>&quot;001F&quot;h</td>
<td>&quot;001F&quot;h</td>
</tr>
</tbody>
</table>

**Note:**

- **X Address Start Instruction**: R210h
- **X Address End Instruction**: R211h
- **Y Address Start Instruction**: R212h
- **Y Address End Instruction**: R213h
- **SS Setting Instruction**: R001h
- **GS Setting Instruction**: R400h
- **BGR Setting Instruction**: R003h

---

**Figure 1 Display RAM Address Map Table**
### 7.1. Power Supply Pins

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
<th>Connect Pin</th>
</tr>
</thead>
</table>
| VDDI  | I   | - Power supply for I/O system.  
- VDDI must be lower than or equal to VDD.                                                                                                                                  | VDDI        |
| VDD   | I   | - Power supply for digital system. Input voltage level should be the same as VDDA.                                                                                                                   | VDD         |
| VDDA  | I   | - Power supply for analog and booster circuits. Input voltage level should be the same as VDD.                                                                                                         | VDDA        |
| AGND  | I   | - System ground for analog system and booster circuit.                                                                                                                                                     | GND         |
| DGND  | I   | - System ground for I/O system and digital system.                                                                                                                                                         | GND         |
| VPP   | I   | - Power supply for internal NVM.  
- When writing NVM, it needs external power supply voltage (7.5V/10mA).  
- Leaves these pins open if not used.                                                                                                                                          | -           |
### 7.2. Interface Logic Pins

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
<th>Connect Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IM2, IM1, IM0/ID</strong></td>
<td>I</td>
<td>- The MCU interface mode select.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>IM2</strong></td>
<td><strong>IM1</strong></td>
</tr>
<tr>
<td>0 0 0</td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0 0 1</td>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0 1 0</td>
<td></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 1</td>
<td></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1 0</td>
<td></td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1 1</td>
<td></td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1 1 1</td>
<td></td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PROTECT</strong></td>
<td>I</td>
<td>Reset protect pin. The ST7793 enters a reset protect status by fixing PROTECT to GND level to prevent hardware reset from noise.</td>
<td>VDDI</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low: Hardware reset is disabled (Reset protect status)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High: Hardware reset is enabled. (Normal status)</td>
<td></td>
</tr>
<tr>
<td><strong>RESET</strong></td>
<td>I</td>
<td>- This signal will reset the device and it must be applied to properly initialize the chip.</td>
<td>MCU</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Signal is active low.</td>
<td></td>
</tr>
<tr>
<td><strong>CSX</strong></td>
<td>I</td>
<td>- Chip selection pin. Low-active.</td>
<td>MCU</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, please fix this pin at VDDI level.</td>
<td></td>
</tr>
<tr>
<td><strong>DCX (MDDIGND)</strong></td>
<td>I</td>
<td>- Display data/command selection (RS) pin in MCU interface.</td>
<td>MCU / GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCX='1': display data or parameter.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCX='0': register index / command.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In MDDI mode, connect this pin to DGND.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, please fix this pin at VDDI or DGND level.</td>
<td></td>
</tr>
<tr>
<td><strong>RDX (MDDIGND)</strong></td>
<td>I</td>
<td>- Read enable in 8080 MCU parallel interface. Low-active.</td>
<td>MCU / GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In MDDI mode, connect this pin to DGND.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, please fix this pin at VDDI or DGND level.</td>
<td></td>
</tr>
<tr>
<td><strong>WRX (SCL / MDDI_STB_M)</strong></td>
<td>I</td>
<td>- Write enable in MCU parallel interface.</td>
<td>MCU</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In SPI mode, this pin is used as SCL.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- MDDI mode, this pin is used as MDDI_STB_M.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, please fix this pin at VDDI level.</td>
<td></td>
</tr>
<tr>
<td><strong>VSYNCX</strong></td>
<td>I</td>
<td>- Vertical (Frame) synchronizing input signal for RGB interface</td>
<td>MCU</td>
</tr>
</tbody>
</table>

*NOTE: When the SPI interface is selected, IM0 pin is used for the ID setting.*
<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSPL</td>
<td>I/O</td>
<td>Connect Pin</td>
</tr>
<tr>
<td>VSPL</td>
<td></td>
<td>- When using MDDI Sub-Display function, this pin is used as CSX for Sub-Display.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Fix to the GND level when not in use.</td>
</tr>
<tr>
<td>HSYNCX</td>
<td>I</td>
<td>- Horizontal (Line) synchronizing input signal for RGB interface operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HSYNCX = “0”: Low-active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HSYNCX = “1”: High-active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- When using MDDI Sub-Display function, this pin is used as DCX for Sub-Display.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Fix to the VDDI or GND level when not in use.</td>
</tr>
<tr>
<td>ENABLE</td>
<td>I</td>
<td>- Data enable signal for RGB interface operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low: Select (access enabled)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High: Not select (access disabled)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The EPL bit inverts the polarity of the ENABLE signal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- When using MDDI Sub-Display function, this pin is used as write-strobe for Sub-Display.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, please fix this pin at VDDI or DGND level.</td>
</tr>
<tr>
<td>DOTCLK</td>
<td>I</td>
<td>- Dot clock signal for RGB interface operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DOTCLK = “0”: Input data on the rising edge of DOTCLK</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DOTCLK = “1”: Input data on the falling edge of DOTCLK</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, please fix this pin at VDDI or DGND level.</td>
</tr>
<tr>
<td>SDI</td>
<td>I</td>
<td>- SPI interface input pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- The data is latched on the rising edge of the SCL signal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, please fix this pin at VDDI or DGND level.</td>
</tr>
<tr>
<td>SDO</td>
<td>O</td>
<td>- SPI interface output pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- The data is outputted on the falling edge of the SCL signal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If not used, please fix this pin at floating.</td>
</tr>
<tr>
<td>DB[17:0]</td>
<td>I/O</td>
<td>Connect Pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In MCU 8080 parallel interface, DB[17:0] are used as data bus. 8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. - In RGB interface, DB[17:0] are used as data bus.</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In MDDI mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MDDIGND(DB[8, 6, 4, 3, 1]): connect these to VDDI or DGND level.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MDDI_DATA_P(DB[7])</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MDDI_DATA_M(DB[5])</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MDDI_STB_P(DB[2])</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In MDDI mode with 8-/16-bit Sub-Display DB[17:10] is used as data[7:0] for sub-display.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In MDDI mode with 9-/18-bit Sub-Display DB[17:9] is used as data[8:0] for sub-display.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, please fix this pin at VDDI or DGND level.</td>
</tr>
<tr>
<td>FMARK</td>
<td>O</td>
<td>- Output a frame head pulse signal is used as synchronies MCU to frame rate</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, leave this pin open</td>
</tr>
<tr>
<td>EPROGEN</td>
<td>I</td>
<td>- NVM write enable. When EPROGEN = 1, NVM can be written.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If not used, leave it open</td>
</tr>
</tbody>
</table>

Note1. “1” = VDDI level, “0” = DGND level.

Note2. When in parallel mode, unused data pins must be connected to “1” or “0”.

Note3. When CSX=“1”, there is no influence to the parallel and serial interface.
7.3.. Driver Output Pins

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
<th>Connect pin</th>
</tr>
</thead>
</table>
| S1 to S720| O   | - Source driver output pins  
- To change the shift direction of signal outputs, use the SS bit.  
SS = "0", the data in the RAM address “00000h” is output from S1.  
SS = “1”, the data in the RAM address “00000h” is output from S720.  
- When SS="0"  
  S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9 ... display blue (B) | LCD         |
| G1 to G432| O   | - Gate driver output pins.  
VGH: Selecting Gate Lines Level.  
VGL: Non-selecting Gate Lines Level. | LCD         |
| AVDD      | O   | - Power output pin for monitoring analogy circuit.  
- Leave open when not in use. | -           |
| AVCL      | O   | - Power output pin for monitoring analogy circuit.  
- Leave open when not in use. | -           |
| VGH       | O   | - Power output pin for gate driver  
- Leave open when not in use. | -           |
| VGL       | O   | - Power output (Negative) pin for gate driver  
- Leave open when not in use. | -           |
| VCC       | O   | - Monitoring pin of internal digital reference voltage.  
- Leave open when not in use. | -           |
| VCOM      | O   | - A power supply for the TFT-LCD common electrode. | Common Electrode |
### 7.4. Test and Other Pins

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
<th>Connect pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>DGNDDUM1-10</td>
<td>O</td>
<td>- Use these pins to fix the electrical potentials of unused interface and test pins.</td>
<td>-</td>
</tr>
<tr>
<td>AGNDDUM1-5</td>
<td></td>
<td>- Leave open when not in use.</td>
<td>-</td>
</tr>
<tr>
<td>VDDDUM1</td>
<td></td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>VDDIDUM1-2</td>
<td></td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>DUMMYR1-4</td>
<td>-</td>
<td>- For use of COG contact resistance measurement.</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Leave open when not in use.</td>
<td>-</td>
</tr>
<tr>
<td>VGLDMY1-4</td>
<td>O</td>
<td>- Output VGL level.</td>
<td>Unused Gate Lines</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Used for fixing unused gate line of the panel.</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Leave open when not in use.</td>
<td>-</td>
</tr>
<tr>
<td>PVAN, PVSFTN, PVSFTP, PVAP</td>
<td>O</td>
<td>- Used for monitoring</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Leave open.</td>
<td>-</td>
</tr>
<tr>
<td>TS[11:0]</td>
<td>O</td>
<td>- In MDDI mode with 16-bit Sub-Display</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In MDDI mode with 18-bit Sub-Display</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TS[11:9] &amp; TS[5:0] are used as data[17:9] for sub-display.</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Leave open when not in use.</td>
<td>-</td>
</tr>
<tr>
<td>TEST[5:1]</td>
<td>I</td>
<td>- Used for Driver vendor test.</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Leave open.</td>
<td>-</td>
</tr>
<tr>
<td>VDDS PV22 VDDGX</td>
<td>O</td>
<td>- Used for monitoring</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Leave open.</td>
<td>-</td>
</tr>
<tr>
<td>Dummy</td>
<td>-</td>
<td>- These pins are dummy</td>
<td>-</td>
</tr>
</tbody>
</table>
### 8.1. Absolute Operation Range

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (Analog)</td>
<td>VDDA</td>
<td>-0.3 ~ +4.6</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage (I/O)</td>
<td>VDDI</td>
<td>-0.3 ~ +4.6</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage (Logic)</td>
<td>VDD</td>
<td>-0.3 ~ +4.6</td>
<td>V</td>
</tr>
<tr>
<td>Driver Supply Voltage</td>
<td>VGH-VGL</td>
<td>-0.3 ~ +30.0</td>
<td>V</td>
</tr>
<tr>
<td>NVM Supply Voltage (Write)</td>
<td>VPP</td>
<td>-0.3 ~ +8.0</td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Voltage Range</td>
<td>VIN</td>
<td>-0.3 ~ VDDI + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Logic Output Voltage Range</td>
<td>VO</td>
<td>-0.3 ~ VDDI + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>TOPR</td>
<td>-30 ~ +85</td>
<td>℃</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>TSTG</td>
<td>-40 ~ +110</td>
<td>℃</td>
</tr>
</tbody>
</table>

Table 1 Absolute Operation Range

*Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.*
8.2.. DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Specification</th>
<th>Unit</th>
<th>Related Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power &amp; Operation Voltage</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System Voltage</td>
<td>VDD / VDDA</td>
<td>Operating voltage</td>
<td>MIN. 2.5</td>
<td>TYP. 2.75</td>
<td>MAX. 3.3</td>
</tr>
<tr>
<td>Interface Operation Voltage</td>
<td>VDDI</td>
<td>I/O Supply voltage</td>
<td>MIN. 1.65</td>
<td>TYP. 1.8</td>
<td>MAX. VDD</td>
</tr>
<tr>
<td>Gate Driver High Voltage</td>
<td>VGH</td>
<td></td>
<td>MIN. 12.16</td>
<td></td>
<td>MAX. 15.05</td>
</tr>
<tr>
<td>Gate Driver Low Voltage</td>
<td>VGL</td>
<td></td>
<td>MIN. -12.37</td>
<td></td>
<td>MAX. -7.7</td>
</tr>
<tr>
<td>Gate Driver Supply Voltage</td>
<td></td>
<td></td>
<td>MIN.</td>
<td>-</td>
<td>MAX. 27.4</td>
</tr>
<tr>
<td>Current consumption</td>
<td>IDDA</td>
<td>Shutdown operation</td>
<td>MIN. 12</td>
<td></td>
<td>MAX. 30</td>
</tr>
</tbody>
</table>

| **Input / Output**                       |            |                                 |                      |      |              |
| Logic-High Input Voltage                 | VIH        |                                 | MIN. 0.8VDDI         |      | MAX. VDDI    | Note 1 |
| Logic-Low Input Voltage                  | VIL        |                                 | MIN. VSS             |      | MAX. 0.2VDDI | Note 1 |
| Differential Input High Threshold Voltage| VIT+       |                                 | MIN. 0               |      | MAX. 50      | mV |
| Differential Input Low Threshold Voltage  | VIT-       |                                 | MIN. -50             |      | MAX. 0       | mV |
| Single-ended Receiver Input Operation Voltage Range | VIR      |                                 | MIN. 0.5            |      | MAX. 1.2     | V |
| Logic-High Output Voltage                | VOH        | IOH = -1.0mA                    | MIN. 0.8VDDI         |      | MAX. VDDI    | Note 1 |
| Logic-Low Output Voltage                 | VOL        | IOL = +1.0mA                    | MIN. VSS             |      | MAX. 0.2VDDI | Note 1 |
| Logic-High Input Current                 | IIH        | VIN = VDDI                      | MIN. 1               |      | MAX. uA      | Note 1 |
| Logic-Low Input Current                  | IIL        | VIN = VSS                       | MIN. -1              |      | MAX. uA      | Note 1 |
| Input Leakage Current                    | ILI        | IOH = -1.0mA                    | MIN. -0.1            |      | MAX. +0.1    | uA |

| **VCOM Voltage**                         | VCOM       |                                 | MIN. -                   |      | MAX. 0       | V |

| **Source Driver**                        |            |                                 |                      |      |              |
| Source Output Range                       | VSout      |                                 | MIN. -4.2             |      | MAX. +6.4    | V |
| Source Output Settling Time               | Tr         | Below with 99% precision        | MIN. 20               |      | MAX. uS      | Note 2 |
| Output Offset Voltage                     | VOFFSET    |                                 | MIN. 35               |      | MAX. mV      | Note 3 |

Table 2 Basic DC Characteristics
Notes:

1. $TA = -30$ to $85 \degree C$.

2. Source channel loading = 2kΩ+12pF/channel, Gate channel loading = 5kΩ+40pF/channel.

3. The max. value is between measured point of source output and gamma setting value.
8.3. AC Characteristics

8.3.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCX</td>
<td>TAST</td>
<td>Address Setup Time</td>
<td>0</td>
<td>--</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TAHT</td>
<td>Address Hold Time (Write/Read)</td>
<td>2</td>
<td>--</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>WRX</td>
<td>TWC</td>
<td>Write Cycle</td>
<td>75</td>
<td>--</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TWRH</td>
<td>Control Pulse “H” Duration</td>
<td>25</td>
<td>--</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TWRL</td>
<td>Control Pulse “L” Duration</td>
<td>30</td>
<td>--</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>RDX</td>
<td>TRC</td>
<td>Read Cycle (ID)</td>
<td>450</td>
<td>--</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TRDH</td>
<td>Control Pulse “H” Duration (ID)</td>
<td>250</td>
<td>--</td>
<td>ns</td>
<td>When Read ID Data</td>
</tr>
<tr>
<td></td>
<td>TRDL</td>
<td>Control Pulse “L” Duration (ID)</td>
<td>170</td>
<td>--</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Figure 2 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 °C
<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB[17:0]</td>
<td>TDST</td>
<td>Data Setup Time</td>
<td>20</td>
<td>--</td>
<td>ns</td>
<td>TRAT, TRATFM: 3K ohm Pull up or Down and 30pF Parallel Cap. To GND.</td>
</tr>
<tr>
<td></td>
<td>TDHT</td>
<td>Data Hold Time</td>
<td>10</td>
<td>--</td>
<td>ns</td>
<td>TODH: 3K ohm Pull up or Down.</td>
</tr>
<tr>
<td></td>
<td>TRAT</td>
<td>Read Access Time (ID)</td>
<td>--</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TODH</td>
<td>Output Disable Time</td>
<td>10</td>
<td>--</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Table 3 8080 Parallel Interface Characteristics

Figure 3 Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.
8.3.2 Serial Data Transfer Interface Characteristics:

![Figure 4 SPI Interface Timing Characteristics](image)

**Table 4 SPI Interface Characteristics**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSX</td>
<td>TCSU</td>
<td>Chip Select Setup Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>TCH</td>
<td>Chip Select Hold Time</td>
<td>60</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SCL</td>
<td>TSCH</td>
<td>SCL “H” pulse width (Write)</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>TSCH</td>
<td>SCL “H” pulse width (Read)</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>TSCYC</td>
<td>Serial clock cycle (Write)</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>TSCYC</td>
<td>Serial clock cycle (Read)</td>
<td>350</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>TSCL</td>
<td>SCL “L” pulse width (Write)</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>TSCL</td>
<td>SCL “L” pulse width (Read)</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SDI</td>
<td>TSISU</td>
<td>Serial Input Data Setup Time</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>TSIH</td>
<td>Serial Input Data Hold Time</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SDO</td>
<td>TSOD</td>
<td>Serial Output Data Setup Time</td>
<td>--</td>
<td>130</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>TSOH</td>
<td>Serial Output Data Hold Time</td>
<td>10</td>
<td>--</td>
<td>ns</td>
</tr>
</tbody>
</table>

**VDDI=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25°C**
8.3.3 RGB Interface Characteristics:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSYNCX</td>
<td>TSYNCS</td>
<td>VSYNCS, HSYNC Setup Time</td>
<td>30</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>VSYNCX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENABLE</td>
<td>TENS</td>
<td>Enable Setup Time</td>
<td>30</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TENH</td>
<td>Enable Hold Time</td>
<td>30</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DOTCLK</td>
<td>PWDH</td>
<td>DOTCLK High-level Pulse Width</td>
<td>40</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PWDL</td>
<td>DOTCLK Low-level Pulse Width</td>
<td>40</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCYCD</td>
<td>DOTCLK Cycle Time</td>
<td>100</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DB</td>
<td>TPDS</td>
<td>PD Data Setup Time</td>
<td>40</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TPDH</td>
<td>PD Data Hold Time</td>
<td>40</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Table 5 RGB Interface Timing Characteristics

VDD=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 °C
9 INTERFACE

9.1. MPU Interface Type Selection

For communicating with MCU, ST7793 supports 8-/9-/16-/18-bit 8080-series interface, SPI, and MDDI. Selection of these interfaces are set by IM[2:0] pins as shown below.

<table>
<thead>
<tr>
<th>IM2</th>
<th>IM1</th>
<th>IM0</th>
<th>Interface</th>
<th>Read Back Data Bus Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8080-series MCU 18-bit</td>
<td>Pixel Data: 18-bit, Parameter: 16-bit</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>8080-series MCU 9-bit</td>
<td>Pixel Data: 9-bit, Parameter: 8-bit</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>8080-series MCU 16-bit</td>
<td>Pixel Data: 16-bit, Parameter: 16-bit</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>8080-series MCU 8-bit</td>
<td>Pixel Data: 8-bit, Parameter: 8-bit</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>ID</td>
<td>Serial Peripheral Interface(SPI)</td>
<td>Pixel Data: 16-bit, Parameter: 16-bit</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>MDDI</td>
<td>N/A</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>MDDI with Sub-panel Support</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table 6 Interface Type Selection
9.2.. 8080-Series MCU Interface

9.2.1 8080-Series MCU Write Cycle Sequence

The write cycle means that the host writes information (register index / parameter) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[17:0]). DCX is a control signal, which tells if the data is an index or a parameter. The data signals represent index number if the signal is low (DCX='0') and vice versa the data signals represent parameter (DCX='1').

Note: WRX is an synchronized signal (It can be stopped).

Figure 6 8080-Series WRX Protocol
9.2.2 18-bit 8080-Series Interface Write Format

The 18-bit 8080-series interface is selected by setting the IM [2:0] = "000".

![Figure 8 18-bit 8080-Series Interface Connection](image-url)

This mode accepts only 262k colors format in display. In this interface, index, parameter, and pixel-data...
should be written according to the following figures.

Figure 9 18-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)
9.2.3 16-bit 8080-Series Interface Write Format

The 16-bit 8080-series interface is selected by setting IM[2:0] = "010".

ST7793 accepts 262k-color or 65k-color format in this mode. When the 262k-color format is used, two transfers for each pixel are required.
Figure 11 16-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)

9.2.4 9-bit 8080-Series Interface Write Format

The 9-bit 8080-series interface is selected by setting the IM [2:0] = “011” and the DB [17:9] pins are used to transfer data. Since the register data-width is 16-bit, the data is divided into upper byte and lower byte, and the upper byte is transferred first. The display data is also divided into upper part and lower part (9-bit for each part), and the upper part is transferred first. The unused DB [8:0] pins must be tied to either VDDI or DGND.

Figure 12 9-bit 8080-Series Interface Connection
Figure 13 9-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)
### 9.2.5 8-bit 8080-Series Interface Write Format

The 8080 8-bit interface is selected by setting the IM [2:0] as “011” and the DB [17:10] pins are used to transfer data. The mode accepts 262k-color or 65k-color format. When writing the 16-bit register, the data is divided into two bytes and the upper byte is transferred first. The display data is also divided into upper byte and lower byte, and the upper byte is transferred first. The written data is expanded into 18-bit internally (see the figure below) and then written into DRAM. The unused DB [9:0] pins must be tied to either VDDI or DGND.

![Diagram of 8-bit 8080-Series Interface Connection](image)

**Figure 14 8-bit 8080-Series Interface Connection**

<table>
<thead>
<tr>
<th>Input Pins</th>
<th>Index/Parameter</th>
<th>Pixel Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB17, DB16, DB15, DB14, DB13, DB12, DB11, DB10</td>
<td>IB15, IB14, IB13, IB12, IB11, IB10, IB9, IB8</td>
<td>R5, R4, R3, R2, R1, R0, G5, G4, G3, G2, G1, G0, B5, B4, B3, B2, B1, B0</td>
</tr>
<tr>
<td>First transfer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Second transfer</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Normal display in 65k colors (TRI=0)

![Diagram of 8-bit 8080-Series Interface Data Format](image)

**Figure 15 8-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)**

<table>
<thead>
<tr>
<th>Input Pins</th>
<th>Pixel Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB17, DB16, DB15, DB14, DB13, DB12</td>
<td>R5, R4, R3, R2, R1, R0, G5, G4, G3, G2, G1, G0, B5, B4, B3, B2, B1, B0</td>
</tr>
<tr>
<td>First transfer</td>
<td></td>
</tr>
<tr>
<td>Second transfer</td>
<td></td>
</tr>
<tr>
<td>3th transfer</td>
<td></td>
</tr>
</tbody>
</table>

Note: Normal display in 262k colors (TRI=1, DFM=1)
9.2.6 8080-series MCU Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The driver sends data (DB [17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

Note1: RDX is an unsynchronized signal (It can be stopped)

Figure 16 8080-Series RDX Protocol
Figure 17 8080-Series Parallel Bus Protocol, Read from Register or Display RAM

Signals on DB[17:0], DCX, WRX and RDX pins are ignored when CSX=1*
9.2.7 18-bit 8080-Series Interface Read Format

Figure 18 18-bit 8080-Series Interface Data Format (Register/Pixel Data Read)
9.2.8 16-bit 8080-Series Interface Read Format

![Diagram of 16-bit 8080-Series Interface Data Format (Register/Pixel Data Read)]

Figure 19 16-bit 8080-Series Interface Data Format (Register/Pixel Data Read)
9.2.9 9-bit 8080-Series Interface Read Format

**Register Data**

<table>
<thead>
<tr>
<th>First</th>
<th>Second</th>
</tr>
</thead>
<tbody>
<tr>
<td>IB15</td>
<td>IB7</td>
</tr>
<tr>
<td>IB14</td>
<td>IB6</td>
</tr>
<tr>
<td>IB13</td>
<td>IB5</td>
</tr>
<tr>
<td>IB12</td>
<td>IB4</td>
</tr>
<tr>
<td>IB11</td>
<td>IB3</td>
</tr>
<tr>
<td>IB10</td>
<td>IB2</td>
</tr>
<tr>
<td>IB9</td>
<td>IB1</td>
</tr>
<tr>
<td>IB8</td>
<td>IB0</td>
</tr>
</tbody>
</table>

**Output Pins**

<table>
<thead>
<tr>
<th>First</th>
<th>Second</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB17</td>
<td>DB17</td>
</tr>
<tr>
<td>DB16</td>
<td>DB16</td>
</tr>
<tr>
<td>DB15</td>
<td>DB15</td>
</tr>
<tr>
<td>DB14</td>
<td>DB14</td>
</tr>
<tr>
<td>DB13</td>
<td>DB13</td>
</tr>
<tr>
<td>DB12</td>
<td>DB12</td>
</tr>
<tr>
<td>DB11</td>
<td>DB11</td>
</tr>
<tr>
<td>DB10</td>
<td>DB10</td>
</tr>
<tr>
<td>DB9</td>
<td>DB9</td>
</tr>
</tbody>
</table>

**Pixel Data**

<table>
<thead>
<tr>
<th>First</th>
<th>Second</th>
</tr>
</thead>
<tbody>
<tr>
<td>R5</td>
<td>G5</td>
</tr>
<tr>
<td>R4</td>
<td>G4</td>
</tr>
<tr>
<td>R3</td>
<td>G3</td>
</tr>
<tr>
<td>R2</td>
<td>G2</td>
</tr>
<tr>
<td>R1</td>
<td>G1</td>
</tr>
<tr>
<td>R0</td>
<td>G0</td>
</tr>
<tr>
<td>G5</td>
<td>B5</td>
</tr>
<tr>
<td>G4</td>
<td>B4</td>
</tr>
<tr>
<td>G3</td>
<td>B3</td>
</tr>
<tr>
<td>G2</td>
<td>B2</td>
</tr>
<tr>
<td>G1</td>
<td>B1</td>
</tr>
<tr>
<td>G0</td>
<td>B0</td>
</tr>
</tbody>
</table>

**Output Pins**

<table>
<thead>
<tr>
<th>First</th>
<th>Second</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB17</td>
<td>DB17</td>
</tr>
<tr>
<td>DB16</td>
<td>DB16</td>
</tr>
<tr>
<td>DB15</td>
<td>DB15</td>
</tr>
<tr>
<td>DB14</td>
<td>DB14</td>
</tr>
<tr>
<td>DB13</td>
<td>DB13</td>
</tr>
<tr>
<td>DB12</td>
<td>DB12</td>
</tr>
<tr>
<td>DB11</td>
<td>DB11</td>
</tr>
<tr>
<td>DB10</td>
<td>DB10</td>
</tr>
<tr>
<td>DB9</td>
<td>DB9</td>
</tr>
</tbody>
</table>

Figure 20 9-bit 8080-Series Interface Data Format (Register/Pixel Data Read)
9.2.10 8-bit 8080-Series Interface Read Format

<table>
<thead>
<tr>
<th>Register Data</th>
<th>Output Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>IB15 IB14 IB13 IB12 IB11 IB10 IB9 IB8</td>
<td>DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10</td>
</tr>
<tr>
<td>IB7 IB6 IB5 IB4 IB3 IB2 IB1 IB0</td>
<td>DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10</td>
</tr>
</tbody>
</table>

| Pixel Data |
| R5 R4 R3 R2 R1 R0 G5 G4 G3 C5 C4 C3 B5 B4 B3 B2 B1 B0 |

<table>
<thead>
<tr>
<th>Output Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10</td>
</tr>
</tbody>
</table>

Figure 21 8-bit 8080-Series Interface Data Format (Register/Pixel Data Read)
9.3. RGB Interface

9.3.1 RGB Interface Display Operation

The display operation via the RGB interface is synchronized with the VSYNCX, HSYNCX, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing. Polarities of VSYNCX, HSYNCX, ENABLE, and DOTCLK can be changed by setting the DPL, EPL, HSPL, and VSPL bits (R00Fh). When RGB interface is used, instructions should be transferred via SPI interface. RGB and 8080-series interface cannot be used simultaneously.

Figure 22 Display RAM Access Area via RGB Interface
9.3.2 RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as the following.

![Timing Chart](image)

- **VLW**: VSYNCX low period
- **HLW**: HSYNCX low period
- **DTST**: data transfer startup time

Figure 23 18-/16-bit RGB Interface Signal Relationship
Figure 24 RGB Interface Timing Chart

The timing chart of RGB interface must meet the following table:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbols</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Horizontal Synchronization</td>
<td>Hsync</td>
<td>2</td>
<td>10</td>
<td>16</td>
<td>DOTCLK</td>
</tr>
<tr>
<td>Horizontal Back Porch</td>
<td>HBP</td>
<td>2</td>
<td>20</td>
<td>24</td>
<td>DOTCLK</td>
</tr>
<tr>
<td>Horizontal Address</td>
<td>HAdr</td>
<td>-</td>
<td>240</td>
<td>-</td>
<td>DOTCLK</td>
</tr>
<tr>
<td>Horizontal Front Porch</td>
<td>HFP</td>
<td>2</td>
<td>10</td>
<td>16</td>
<td>DOTCLK</td>
</tr>
<tr>
<td>Vertical Synchronization</td>
<td>Vsync</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>Line</td>
</tr>
<tr>
<td>Vertical Back Porch</td>
<td>VBP</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>Line</td>
</tr>
<tr>
<td>Vertical Address</td>
<td>VAdr</td>
<td>-</td>
<td>432</td>
<td>-</td>
<td>Line</td>
</tr>
<tr>
<td>Vertical Front Porch</td>
<td>VFP</td>
<td>3</td>
<td>4</td>
<td>-</td>
<td>Line</td>
</tr>
</tbody>
</table>
9.3.3 Moving Picture Mode

ST7793 has the RGB interface to display moving picture and incorporates Display RAM to store display data (DRAM), which has following merits in displaying a moving picture.

- The window address function defined the update area of Display RAM.
- The Display RAM is updated only the moving picture area.
- It can contribute to lower the power consumption of the system by reducing data transfer.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched to system interface (8080-series) to update still picture area and registers, such as icons.

**RAM access via a system interface in RGB-I/F mode**

ST7793 allows Display RAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal Display RAM in synchronization with DOTCLK while ENABLE signal is “Low”. When write data to the internal Display RAM by the system interface, set ENABLE("High") to stop write data via RGB interface. Then set RM = ‘0’ to enable RAM access via system interface. When restarting DRAM access in RGB interface mode, wait for one read/write cycle, set RM = ‘1’ and then the index register (R202h) to start accessing RAM via the RGB interface. If Display RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal Display RAM.

The following figure illustrates the operation of the ST7793 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.
9.3.4 18-bit RGB Interface

The RGB Interface mode for ST7793 is selected by setting the RIM bit as following table.

<table>
<thead>
<tr>
<th>RIM</th>
<th>RGB Interface Mode</th>
<th>Data Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>18-bit RGB Interface</td>
<td>DB[17:0]</td>
</tr>
<tr>
<td>1</td>
<td>16-bit RGB Interface</td>
<td>DB[17:13], DB[11:1]</td>
</tr>
</tbody>
</table>

The 18-bit RGB interface is selected by setting the RIM bits to ‘0’. The display operation is synchronized with VSYNCX, HSYNCX, and DOTCLK signals. Display data are transferred to the Display RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.

When RIM='0', the display data format is as the following figure:

![18-bit RGB Interface Data Format](image)

Figure 26 18-bit RGB Interface Data Format

9.3.5 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM bits to ‘1’. The display operation is synchronized with VSYNCX, HSYNCX, and DOTCLK signals. Display data are transferred to the Display RAM in synchronization with the display operation via 16-bit RGB data bus (DB[17:13], DB[11:1]) according to the data enable signal (ENABLE). Registers are set only via the system interface.

When RIM='1', the display data format is as the following figure:
5. In RGB interface mode, a RAM address (AD[16:0]) is set in the address counter every frame on the
1. The following are the functions not available in RGB Input Interface mode.

<table>
<thead>
<tr>
<th>Function</th>
<th>RGB Interface</th>
<th>Internal Display Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Partial display</td>
<td>Not available</td>
<td>Available</td>
</tr>
<tr>
<td>Scroll function</td>
<td>Not available</td>
<td>Available</td>
</tr>
</tbody>
</table>

2. VSYNCX, HSYNCX, and DOTCLK signals must be supplied during a display operation period.
3. In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.
4. In RGB interface mode, the front porch period continues until the next VSYNCX input is detected after drawing one frame.
5. In RGB interface mode, a RAM address (AD[16:0]) is set in the address counter every frame on the falling edge of VSYNCX.
6. When switching between the internal operation mode and the external display interface operation mode, the sequences below should be followed.
Figure 28 Internal Clock Operation / RGB Interface Mode Switching Sequences

Note 1: Input RGB interface signals (VSYNC, HSYNC, DOTCLK) before setting DM[1:0] and RM to the RGB interface mode.
Note 2: Continue RGB interface signals at least for one frame period after setting DM[1:0] and RM bits to internal clock operation.
9.4.. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[2:0] pins as “10x” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND.

The SPI interface operation enables from the falling edge of CSX and ends of data transfer on the rising edge of CSX. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ST7793.

The seventh bit of start byte is RS bit. When RS = ‘0’, either index write operation or status read operation is executed. When RS = ‘1’, either parameter write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is ‘0’ and read back when the R/W bit is ‘1’.

After receiving the start byte, ST7793 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ST7793 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Start Byte Format

<table>
<thead>
<tr>
<th>Transfer Bit-Order</th>
<th>S</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start Byte Format</td>
<td></td>
<td></td>
<td>Device ID Code</td>
<td>RS</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ID</td>
<td>1/0</td>
</tr>
</tbody>
</table>

Notes: ID bit is selected by setting the IM0/ID pin

RS and R/W Bit Function

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Set index register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>(Setting inhibited)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Write to register or Display RAM</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Read from register or Display RAM</td>
</tr>
</tbody>
</table>
Figure 29 Data Format of SPI Interface
Figure 30 Data transmission through serial peripheral interface (SPI)
(e) Basic data transmission through SPI

SCL (input)

SDI (input)

SDO (output)

Start Byte

DRAM data write

Start Byte

DRAM data read

(f) Display RAM data write transmission

SCL (input)

SDI (input)

SDO (output)

Start

DRAM data (1)

execution time

DRAM data (2)

execution time

(g) DRAM data read transmission

SCL (input)

SDI (input)

SDO (output)

Start byte

RS=1, RW=1

Dummy read 1

Dummy read 2

Dummy read 3

Dummy read 4

Dummy read 5

RAM read 1st byte

RAM read 2nd byte

RAM read 3rd byte

Note: Five bytes of invalid dummy data read after the start byte.

RAM data transfer in SPI mode when TRI = 1 and DFM = 1 or 0

Figure 31 Data transmission through serial peripheral interface (SPI, TRI="1" and DFM="1 or 0")
9.5. VSYNC Interface

9.5.1 VSYNC Interface Operation

The ST7793 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

When DM[1:0]="10" and RM='0', VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables tearing-free display of motion pictures with the conventional interface.
Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

Figure 34 Timing Diagram of VSYNC Interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writes should be performed with higher speed than the result obtained from the calculation shown below. The internal RAM address counter is reset by VSYNC. So, insure interval time between VSYNC falling and DISPLAY RAM data writing.

Note:
1. VSYNC period should always be constant. If not, some degradation of display such as flicker may occur in LCD system.
2. Display data don’t need to be written for every VSYNC period. For example, any system is working under 60Hz frame rate and 30-fps motion picture condition. So being written display data for every other frame would be enough.
9.5.2 VSYNC Interface Modes

9.5.2.1 Leading Mode

Figure 35 Operation for Leading Mode of VSYNC Interface

9.5.2.2 Lagging Mode

Figure 36 Operation for Lagging Mode of VSYNC Interface
Notes:

1. When RAM writing does not start immediately after the falling edge of VSYNCX, the time between the falling edge of VSYNCX and the RAM writing start timing must also be considered.

2. The minimum Display RAM write speed must be satisfied and the frequency variation must be taken into consideration.

3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display and vertical scroll functions are not available in VSYNC interface mode.

5. Set the AM bit to ‘0’ to transfer display data correctly in VSYNC interface.

![Diagram of VSYNC and Internal Clock Operation Mode Switching Sequences](image_url)
9.6. Mobile Display Digital Interface (MDDI)

MDDI (Mobile display digital interface) is a differential small amplitude serial interface for high-speed data transfer via following 4 lines: Stb+/− (MDDI_STB_P_B, MDDI_STB_M_B), Data+/− (MDDI_DATA_P_B, MDDI_DATA_M_B).

The specifications of MDDI supported by the ST7793 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the ST7793 MDDI.

9.6.1 ST7793 MDDI Specification

- MDDI Type-I
- High-speed, differential, small-amplitude data transfer via Stb+/−, Data+/− lines
- MDDI client: the ST7793 enables direct connection to the base band (BB) chip without bridge chip
- Cost-performance optimized interface for mobile display systems

1. Only internal mode (one client) and Forward Link are supported
2. Hibernation mode to save power consumption
3. Tearing-free moving picture display via FMARK/VSYNC interface
4. Moving picture display with low power consumption, realized by the features 2 ~ 3
5. Shutdown mode for saving power consumption in the standby state

ST7793 incorporates an output port for sub-display interface or peripheral control providing single-chip solution for MDDI mobile display systems.
9.6.2 Supported MDDI Packets

The MDDI Link Protocol of the ST7793 is in line with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the ST7793 are as follows. Do not send packets which are not supported by ST7793.

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame and some sub-frame construct media-frame together. The following table describes 5 types of packet which is supported in ST7793.

<table>
<thead>
<tr>
<th>Packet</th>
<th>Function</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-frame header packet</td>
<td>Header of each sub frame</td>
<td>Forward</td>
</tr>
<tr>
<td>Register access packet</td>
<td>Register setting</td>
<td>Forward</td>
</tr>
<tr>
<td>Video stream packet</td>
<td>Video data transfer</td>
<td>Forward</td>
</tr>
<tr>
<td>Filler packet</td>
<td>Fill empty packet space</td>
<td>Forward</td>
</tr>
<tr>
<td>Link shut down packet</td>
<td>End of frame</td>
<td>Forward</td>
</tr>
</tbody>
</table>

Figure 39 MDDI Frame and Packet Structure
<table>
<thead>
<tr>
<th>Bytes</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Packet Length</td>
<td>(0014h)</td>
</tr>
<tr>
<td>1</td>
<td>Packet Type</td>
<td>(3BFFh)</td>
</tr>
<tr>
<td>2</td>
<td>Unique Word</td>
<td>(005Ah)</td>
</tr>
<tr>
<td>3</td>
<td>Reserved 1</td>
<td>(0000h)</td>
</tr>
<tr>
<td>4</td>
<td>Sub-Frame Length</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Protocol Version</td>
<td>(0000h)</td>
</tr>
<tr>
<td>6</td>
<td>Sub-Frame Count</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Media-Frame Count</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CRC</td>
<td>(0000h)</td>
</tr>
</tbody>
</table>

Figure 40 Sub-Frame Header Packet
The ST7793 writes pixel data to Display RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.

<table>
<thead>
<tr>
<th>Packet Length</th>
<th>Packet Type</th>
<th>bClient ID</th>
<th>Video Data Format Descriptor</th>
<th>Pixel Data Attributes</th>
<th>X Left Edge</th>
<th>Y Top Edge</th>
<th>X Right Edge</th>
<th>Y Bottom Edge</th>
</tr>
</thead>
</table>

*Note: The parameters colored in gray are not supported by the ST7793.*
**ST7793**

**Video Data Format Descriptor:** Sets the pixel data format. ST7793 supports only the following format. Set the same pixel format (bpp) as selected by DSS[1:0] in Video Data Format Descriptor.

<table>
<thead>
<tr>
<th>[15:13]</th>
<th>[12]</th>
<th>[11:8]</th>
<th>[7:4]</th>
<th>[3:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>“010”</td>
<td>1</td>
<td>5h</td>
<td>6h</td>
<td>5h</td>
</tr>
<tr>
<td>“010”</td>
<td>1</td>
<td>6h</td>
<td>6h</td>
<td>6h</td>
</tr>
<tr>
<td>Others</td>
<td></td>
<td></td>
<td></td>
<td>Setting Prohibited</td>
</tr>
</tbody>
</table>

- Packed 16bpp RGB Format (R:G:B = 5:6:5)
- Packed 18bpp RGB Format (R:G:B = 6:6:6)

**Pixel Data Attributes:** the image data sent via Video Stream Packet is recognized as either the data for the main-panel or for the sub-panel according to the setting in [1:0] bits in this field.

<table>
<thead>
<tr>
<th>Pixel Data Attributes</th>
<th>Bits[1:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000h</td>
<td>00</td>
<td>The video stream packet data is recognized as the sub-panel data so that it is outputted via sub-display interface and not written to the ST7793.</td>
</tr>
<tr>
<td>0001h</td>
<td>01</td>
<td>Setting Prohibited</td>
</tr>
<tr>
<td>0002h</td>
<td>10</td>
<td>Setting Prohibited</td>
</tr>
<tr>
<td>0003h</td>
<td>11</td>
<td>The video stream packet data is recognized as the data written to the ST7793. The Video stream packet data is written to the ST7793 and not outputted via sub-display interface.</td>
</tr>
<tr>
<td>Others</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**9.6.2.2 Register Access Packet**

Register Access Packet is used when setting instruction to the ST7793.
### ST7793

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Packet Length</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>Packet Type</td>
<td>(0092h)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>bClient ID</td>
<td>(0000h)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td>Read/Write Info.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td>Register Address</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
<td></td>
<td>Parameter CRC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
<td></td>
<td>Register Data</td>
<td>(Packet Length – 14 Bytes)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Register Data CRC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: The parameters colored in gray are not supported by the ST7793.

**Read/Write Info**: Read or Write information in register access. ST7793 supports the following access setting.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;00&quot;</td>
<td>0001h</td>
<td>Write one register by register access packet</td>
</tr>
<tr>
<td>Others</td>
<td>-</td>
<td>Setting Prohibited</td>
</tr>
</tbody>
</table>

**Register Address**: The index of the register to be accessed is set in Register Address area and the Register Address Packet is directed to the ST7793 or the sub display is determined by the setting in Register Address area.

<table>
<thead>
<tr>
<th>Bits[31:16]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000h</td>
<td>The Register Access Packet is directed to the ST7793 via main-display interface.</td>
</tr>
<tr>
<td>0001h</td>
<td>The Register Access Packet is directed to the sub display via sub-display interface.</td>
</tr>
<tr>
<td>0002h~7FFFh</td>
<td>Setting disable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bits[15:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000h~FFFFh</td>
<td>Bits[15:0] are used as register index [15:0].</td>
</tr>
</tbody>
</table>

**Register Data**: The data for register access is written in Register Data. The length of Register Data depends on the parameter length of command.
### Example of Register Access Packet (e.g. write to the ST7793)

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Packet Length</td>
<td>(12h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>(00h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Packet Type</td>
<td>(92h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>(00h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>bClient ID</td>
<td>(00h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>(00h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Read/Write Info.</td>
<td>(01h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>(00h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Register Address</td>
<td>(Index ID[7:0])</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>(Index ID[15:8])</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>(00h) -&gt; Main Display (ST7793)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>(01h) -&gt; Sub Display</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Parameter CRC</td>
<td>(00h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Register Data List (Variable Length)</td>
<td></td>
<td>1&lt;sup&gt;st&lt;/sup&gt; Parameter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
<td>2&lt;sup&gt;nd&lt;/sup&gt; Parameter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
<td>3&lt;sup&gt;rd&lt;/sup&gt; Parameter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
<td>Parameter CRC</td>
<td>(00h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
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<td></td>
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<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** The parameters colored in gray are not supported by the ST7793.

### Register Access Packet Restrictions:
ST7793's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

#### 9.6.2.3 Link Shutdown Packet

This packet is used to bring Link to the Hibernation state.

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Packet Length</td>
<td>(0014h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Packet Type</td>
<td>(0045h)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Parameter CRC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>All Zeros</td>
<td>(Type-I : 16 Bytes)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** The parameters colored in gray are not supported by the ST7793.
9.6.3 Hibernation Setting

The ST7793 Client MDDI supports Hibernation setting. There are two ways to cancel the Hibernation setting, which can be selected according to the condition of use.

<table>
<thead>
<tr>
<th>Hibernation Cancellation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Host-Initiated Wake Up</td>
</tr>
<tr>
<td>TE-Initiated Wake Up</td>
</tr>
</tbody>
</table>

The Hibernation setting and cancellation sequence must be compatible with the VESA-MDDI specifications.
Host-Initiated Wake up from Hibernation

The host initiated wake up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the figures below!

- The host sends a Link Shutdown Packet to inform the client that the link will transition to the low power hibernation state.

- Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. During the interval the host initially sets MDDI_Data0 to a logic zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

- The host enters the low power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low power hibernation state. It is also allowable for MDDI_Stb to be driven to logic zero level or to continue toggling during hibernation. The client is also in the low power hibernation state.

- After a while, the host begins the line restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drivers MDDI_Data0 to a logic one level and MDDI_Stb to logic zero level for at least 200ns after MDDI_Data0 reaches a valid logic one level and MDDI_Stb reaches a valid logic zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high speed pulses on MDDI_Stb. The client first detects the wake up pulse using a low power differential receiver having a +125mV input offset voltage.

- The host drivers are fully enabled and MDDI_Data0 is being driven to a logic one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.

- The host drives MDDI_Data0 to a logic zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub frame Header Packet after MDDI_Data0 is at a logic zero level for 40 MDDI_Stb cycles.

- The host begins to transmit data on the forward link by sending a Sub-frame Header packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences form point G.
9.6.4 Sub-Display Interface

The ST7793 supports the sub-display interface which connects to sub-display driver IC with parallel interface. Depending on the packet header, ST7793 automatically receive and convert MDDI packet to parallel data and send to sub panel driver IC.
9.6.4.1 Sub-Display Interface Timing

**Internal Clock for Sub-Panel Signal Generation**

The Sub-Display interface is driven by an internal clock which is generated from MDDI interface data transmission. Once there are four bits transmitted via MDDI, one cycle of internal clock for sub-display interface is generated.

Mode 1 Sub-Display Interface Timing (8-/9-bit)

```
<table>
<thead>
<tr>
<th>Internal Clock</th>
<th>CSX</th>
<th>WRX (80 Mode)</th>
<th>Enable (68 Mode)</th>
<th>DCX</th>
</tr>
</thead>
</table>
```

**Mode 1 Sub-Display Interface Timing (16-/18-bit)**

```
<table>
<thead>
<tr>
<th>Internal Clock</th>
<th>CSX</th>
<th>WRX (80 Mode)</th>
<th>Enable (68 Mode)</th>
<th>DCX</th>
</tr>
</thead>
</table>
```

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Mode 2 Sub-Display Interface Timing (8-/9-bit)
Mode 2 Sub-Display Interface Timing (16-/18-bit)
### 10 REGISTER

#### 10.1.. Register List

<table>
<thead>
<tr>
<th>No</th>
<th>Registers</th>
<th>W/R</th>
<th>RS</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IR</td>
<td>Index Register</td>
<td>W</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>ID10</td>
<td>ID9</td>
<td>ID8</td>
<td>ID7</td>
<td>ID6</td>
<td>ID5</td>
<td>ID4</td>
<td>ID3</td>
<td>ID2</td>
<td>ID1</td>
<td>ID0</td>
</tr>
<tr>
<td>000h</td>
<td>Driver Code</td>
<td>R</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>001h</td>
<td>Driver Output Control</td>
<td>W/R</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>SM</td>
<td>SS</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>002h</td>
<td>Entry Mode</td>
<td>W/R</td>
<td>1</td>
<td>TRI</td>
<td>DFM</td>
<td>0</td>
<td>BGR</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ORG</td>
<td>0</td>
<td>ID[1:0]</td>
<td>AM</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>007h</td>
<td>Display Control 1</td>
<td>W/R</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>PTDE</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>BASEE</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>008h</td>
<td>Display Control 2</td>
<td>W/R</td>
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<td>0</td>
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<td></td>
<td></td>
<td></td>
<td>FP[7:0]</td>
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<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>008h</td>
<td>B-Color Control</td>
<td>W/R</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tr>
<tr>
<td>00Ch</td>
<td>External Display</td>
<td>W/R</td>
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<td>0</td>
<td>ENC[2:0]</td>
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<td>0</td>
<td>RM</td>
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<td>0</td>
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<td>DM[1:0]</td>
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<td>RIM</td>
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<td></td>
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</tr>
<tr>
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<td>W/R</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>VSPL</td>
<td>HSPL</td>
<td>0</td>
<td>EPL</td>
<td>DPL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>090h</td>
<td>Frame Marker Control</td>
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<td>FMKM</td>
<td>FMI[2:0]</td>
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<td>CMD2_EN</td>
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<td></td>
</tr>
<tr>
<td>0FFh</td>
<td>Ext Register Control</td>
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<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>100h</td>
<td>Power Control 1</td>
<td>W/R</td>
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<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
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</tr>
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<td>102h</td>
<td>Power Control 3</td>
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<td>PON</td>
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</tr>
<tr>
<td>200h</td>
<td>Horizontal DRAM Address Set</td>
<td>W/R</td>
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<td>AD[7:0]</td>
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</tr>
<tr>
<td>200h</td>
<td>Vertical DRAM Address Set</td>
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<td>0</td>
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<td>0</td>
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<td>AD[16:8]</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>202h</td>
<td>Write Data to DRAM</td>
<td>W</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DRAM Write Data (WD[17:0]) / Read Data (RD[17:0])</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>202h</td>
<td>Read Data from DRAM</td>
<td>R</td>
<td>1</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>210h</td>
<td>Horizontal Address Start Position</td>
<td>W/R</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>HAS[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
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### Table 7 Register List

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<th>Bits 9-16</th>
<th>Bits 17-24</th>
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### 10.2.1 Index (IR)

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**Description**: The index register specifies the index R000h to R7Fh of the control register or RAM control to be accessed. The access to unassigned registers and instruction bits is prohibited.

### 10.2.2 Device ID Code Read (R000h)

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**Description**: When read this register, the device output device ID code (7793h)

### 10.2.3 Device Output Control (R001h)

<table>
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<th>Device Output Control (R001h)</th>
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<tbody>
<tr>
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<tr>
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</table>

**Default value**: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

**Description**: SS: Select the shift direction of outputs from the source driver. When SS = 0, the shift direction of outputs is from S1 to S720. When SS = 1, the shift direction of outputs is from S720 to S1. In addition to the shift direction, the settings for both SS and BGR bits are required to change the Assignment of R, G, B dots to the source driver pins. To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0 and RGB = 0. To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1 and RGB = 1.

**Note**: When changing SS or BGR bits, DRAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

### 10.2.4 Entry Mode (R003h)

<table>
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<tr>
<th>Entry Mode (R003h)</th>
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</table>

**Description**: SS: Select the shift direction of outputs from the source driver. When SS = 0, the shift direction of outputs is from S1 to S720. When SS = 1, the shift direction of outputs is from S720 to S1. In addition to the shift direction, the settings for both SS and BGR bits are required to change the Assignment of R, G, B dots to the source driver pins. To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0 and RGB = 0. To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1 and RGB = 1.

**Note**: When changing SS or BGR bits, DRAM data must be rewritten.
<table>
<thead>
<tr>
<th>AM</th>
<th>ID[1:0]</th>
<th>Write DRAM Direction</th>
<th>AM</th>
<th>ID[1:0]</th>
<th>Write DRAM Direction</th>
</tr>
</thead>
<tbody>
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<td>“00”</td>
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<tr>
<td>0</td>
<td>“10”</td>
<td></td>
<td>1</td>
<td>“10”</td>
<td></td>
</tr>
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</table>
ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the DRAM address map within the window address area.
ORG = 1: The original address 00000h moves according to the I/D[1:0] setting.

Note 1: When ORG=1, only the origin address 00000h can be set in the RAM address set registers R200h, and R201h.

Note2: In RAM read operation, make sure to set ORG=0.

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the DRAM.

BGR = 0: Write data in the order of RGB to the DRAM.

BGR = 1: Reverse the order from RGB to BGR in writing data to the DRAM.

TRI: When TRI = 1, data are transferred to the internal DRAM in 8-bit x 3 transfers mode via the 8-bit interface and in. It is also possible to send data via the 16-bit interface in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = 0.

DFM: Set the mode of transferring data to the internal RAM when TRI = 1.
8-bit 8080-Series Interface Color Format

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<th>DFM</th>
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### Display Control 1 (R007h)

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<th>D14</th>
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<th>D11</th>
<th>D10</th>
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<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Default value**

| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Description**

- **BASEE**: Base image display enable bit.
  - BASEE = 0: No base image is displayed. The ST7793 drives liquid crystal with non-lit display level or drives only partial image display areas.
  - BASEE = 1: A base image is displayed on the screen.

- **PTDE**: Partial display enable bits
  - PTDE = 0: turns off partial image. Only base image is displayed.
  - PTDE = 1: turns on partial image. Please set BASEE = 0 to turn off base image.
10.2.6 Display Control 2 (R008h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Default value: 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0

**BP [7:0]**: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

**FP [7:0]**: Sets the number of lines for a front porch period (a blank period following the end of display).

**Note**: Make sure that BP+FP must be even number of lines and BP+FP ≤ 256 lines

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNCX signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNCX input is detected.

<table>
<thead>
<tr>
<th>FP [7:0]</th>
<th>Front Porch Lines</th>
<th>Back Porch Lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Setting Prohibited</td>
<td>Setting Prohibited</td>
</tr>
<tr>
<td>01h</td>
<td>Setting Prohibited</td>
<td>Setting Prohibited</td>
</tr>
<tr>
<td>02h</td>
<td>Setting Prohibited</td>
<td>2 lines</td>
</tr>
<tr>
<td>03h</td>
<td>3 lines</td>
<td>3 lines</td>
</tr>
<tr>
<td>04h</td>
<td>4 lines</td>
<td>4 lines</td>
</tr>
<tr>
<td>05h</td>
<td>5 lines</td>
<td>5 lines</td>
</tr>
<tr>
<td>06h</td>
<td>6 lines</td>
<td>6 lines</td>
</tr>
<tr>
<td>…</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>7Fh</td>
<td>127 lines</td>
<td>127 lines</td>
</tr>
<tr>
<td>80h</td>
<td>128 lines</td>
<td>128 lines</td>
</tr>
<tr>
<td>81h</td>
<td>Setting Prohibited</td>
<td>Setting Prohibited</td>
</tr>
<tr>
<td>…</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>FFh</td>
<td>Setting Prohibited</td>
<td>Setting Prohibited</td>
</tr>
</tbody>
</table>

Note: The output timing to the LCD is delayed by 1 line period from the input VSYNCX signal.
### Eight Color Control (R00Bh)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Default value**: 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0

**Description**: COL: When COL = 1, the ST7793 enters 8-color display mode. No RAM-rewrite is required for 8-color display mode.
### External Display Interface Control 1 (R00Ch)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Default value:**

<table>
<thead>
<tr>
<th>RIM</th>
<th>RGB Interface Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>18-bit RGB interface (1 transfer/pixel), DB[17:0], 262,144 colors</td>
</tr>
<tr>
<td>1</td>
<td>16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1], 65,536 colors</td>
</tr>
</tbody>
</table>

**RIM:** Select the RGB interface data format. Set RIM bit one or more frames before starting display operation via external display interface.

**DM [1:0]:** Select the display operation mode.

<table>
<thead>
<tr>
<th>DM[1:0]</th>
<th>Display Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>“00”</td>
<td>Internal Clock Operation</td>
</tr>
<tr>
<td>“01”</td>
<td>RGB interface</td>
</tr>
<tr>
<td>“10”</td>
<td>VSYNC interface</td>
</tr>
<tr>
<td>“11”</td>
<td>Setting prohibited</td>
</tr>
</tbody>
</table>

**Note:** The DM[1:0] setting allows switching between internal clock operation mode and external display interface only. i.e. switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

**RM:** Select the interface to access the RAM. When RM = 1, display data is written via RGB interface. When RM = 0, display data is written via system interface or VSYNC interface.

**ENC [2:0]:** Set the RAM write cycle through the RGB interface

<table>
<thead>
<tr>
<th>ENC[2:0]</th>
<th>RAM Write Cycle(Frame periods)</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1 Frame</td>
</tr>
</tbody>
</table>

**Description**

**Note1:** Registers are set only by the system interface.

**Note2:** Be sure that previous pixel data transfer is completed before interface switch.
<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>2 Frames</td>
<td></td>
</tr>
<tr>
<td>010</td>
<td>3 Frames</td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>4 Frames</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>5 Frames</td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>6 Frames</td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>7 Frames</td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>8 Frames</td>
<td></td>
</tr>
</tbody>
</table>
### External Display Interface Control (R00Fh)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Default value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

**DPL**: Sets the signal polarity of the DOTCLK pin.
- DPL = 0: The data is input on the rising edge of DOTCLK
- DPL = 1: The data is input on the falling edge of DOTCLK

**EPL**: Sets the signal polarity of the ENABLE pin.
- EPL = 0: The data DB17-0 is written when ENABLE = 0. Disable data write operation when ENABLE = 1.
- EPL = 1: The data DB17-0 is written when ENABLE = 1. Disable data write operation when ENABLE = 0.

**HSPL**: Sets the signal polarity of the HSYNCX pin.
- HSPL= 0: Low active
- HSPL= 1: High active

**VSPL**: Sets the signal polarity of the VSYNCX pin.
- VSPL= 0: Low active
- VSPL= 1: High active
### 10.2.10 Frame Marker Control (R090h)

<table>
<thead>
<tr>
<th>Frame Marker Control 4 (R090h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS</td>
</tr>
<tr>
<td>----</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

**Default value**

<table>
<thead>
<tr>
<th>FMP[8:0]</th>
<th>FMARK output position</th>
</tr>
</thead>
<tbody>
<tr>
<td>000h</td>
<td>0</td>
</tr>
<tr>
<td>001h</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>1BEh</td>
<td>446</td>
</tr>
<tr>
<td>1BFh</td>
<td>447</td>
</tr>
<tr>
<td>Others</td>
<td>Setting Prohibited</td>
</tr>
</tbody>
</table>

**FMP [8:0]:** Sets the output position of FMARK signal. A pulse (FMARK) is output by starting from back porch during a 1H period when FMP[8:0] = 000h. FMP setting must meet the following constraint: 000h ≤ FMP ≤ BP + NL + FP.

**FMI [2:0]:** Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

<table>
<thead>
<tr>
<th>FMI[2:0]</th>
<th>Output Interval</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;000&quot;</td>
<td>1 Frame</td>
</tr>
<tr>
<td>&quot;001&quot;</td>
<td>2 Frames</td>
</tr>
<tr>
<td>&quot;011&quot;</td>
<td>4 Frames</td>
</tr>
<tr>
<td>&quot;101&quot;</td>
<td>6 Frames</td>
</tr>
<tr>
<td>Others</td>
<td>Setting Prohibited</td>
</tr>
</tbody>
</table>

**FMKM:** Set FMKM = 1 when FMARK signal is output from FMARK pin.
### 10.2.11 Ext Register Control (R0FFh)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CMD2_EN</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Default value:** 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

**Description:** CMD2_EN: Set to ‘1’ to enable access to extended registers, including R380h~R389h, R702h, R708h, R710h, R712h, R713h, R724h, and R7E1h.

### 10.2.12 Power Control 1 (R100h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>DSTB</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Default value:** 0 0 0 0 0 0 0 1 1 0 0 1 1 0 0 0 0 0

**Description:** DSTB: When DSTB = 1, ST7793 enters the shutdown mode and stops display. In the shutdown mode, the internal logic power supply is turned off to reduce power consumption. The RAM data and register settings are not maintained while in the shutdown mode. Set this register again after the shutdown mode is exited.

### 10.2.13 Power Control 3 (R102h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>PSON</td>
<td>PSON</td>
<td>PSON</td>
<td>PSON</td>
<td>PSON</td>
<td>PSON</td>
<td>PSON</td>
</tr>
</tbody>
</table>

**Default value:** 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0

**Description:** PON, PSON: Turn on power supply. PON and PSON must be written to start the internal power supply operation.
10.2.14 DRAM Horizontal/Vertical Address Set (R200h, R201h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>AD[7:0]</td>
</tr>
</tbody>
</table>

Default value

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>AD[16:8]</td>
</tr>
</tbody>
</table>

Default value

**AD [16:0]:** A DRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, /D[1:0] settings as the ST7793 writes data to the internal DRAM so that data can be written consecutively without resetting the address in the AC.

**Note 1:** In RGB interface operation (RM = 1), the AD[16:0] is set to address counter every frame on the falling edge of VSYNCX.

**Note 2:** In internal clock operation and VSYNC interface operation (RM = 0), the AD[16:0] is set to address counter when the R200h and R201h are executed.

### RAM Data Map

<table>
<thead>
<tr>
<th>AD[16:0]</th>
<th>RAM Data Map</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000h~000EFh</td>
<td>1st line DRAM Data</td>
</tr>
<tr>
<td>00100h~001EFh</td>
<td>2nd line DRAM Data</td>
</tr>
<tr>
<td>00200h~002EFh</td>
<td>3rd line DRAM Data</td>
</tr>
<tr>
<td>00300h~003EFh</td>
<td>4th line DRAM Data</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>1AD00h~1ADEFh</td>
<td>430th line DRAM Data</td>
</tr>
<tr>
<td>1AE00h~1AEFh</td>
<td>431th line DRAM Data</td>
</tr>
<tr>
<td>1AF00h~1AFEFh</td>
<td>432h line DRAM Data</td>
</tr>
</tbody>
</table>
### Write Data to DRAM (R202h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Description**  

WD [17:0]: The ST7793 develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation. The DRAM data represents the grayscale level. The DRAM data represents the grayscale level. ST7793 automatically updates the address to the begin point according to AM and I/D[1:0] settings as it is written to this register. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.
10.2.16 Read Data from DRAM (R202h)

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<th>RDX</th>
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</table>

**RD [17:0]**: 18-bit data read from the Display RAM. RAM read data RD [17:0] is transferred via different data bus in different interface operation. When the ST7793 reads data from the Display RAM to the microcomputer, the first word read immediately after RAM address set is executed is taken in the internal read-data latch and invalid data is sent to the data bus. Valid data is sent to the data bus when the ST7793 reads out the second and subsequent words. When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

![Diagram](image)

**Description**

The ST7793 also supports function that automatically updates the address according to AM and I/D[1:0] settings when reading data of continuously addresses in the Display RAM.
10.2.17 Horizontal and Vertical Window Address Position (R210h, R211h, R212h, R213h)

<table>
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</table>
HSA [7:0], HEA [7:0], HSA [7:0], and HEA [7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA [7:0] and HEA [7:0] specify the horizontal range to write data. Set HSA [7:0] and HEA [7:0] before starting RAM write operation. In setting, make sure that 00h ≤ HSA < HEA ≤ EFh.

VSA [8:0], VEA [8:0], VSA [8:0], and VEA [8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA [8:0] and VEA [8:0] specify the vertical range to write data. Set VSA [8:0] and VEA [8:0] before starting RAM write operation. In setting, make sure that 00h ≤ VSA < VEA ≤ 1AFh.

Legend

00h ≤ HSA[7:0] ≤ HEA[7:0] ≤ EFh
4 ≤ HEA - HSA
00h ≤ VSA[7:0] ≤ VEA[7:0] ≤ 1AFh

Note1. The window address range must be within the DRAM address space.
Note2. Address must be set within the window.

10.2.18 NVM Data Read / NVM Data Write (R280h)

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Default value

| VCM[6:0], UID[4:0]: Used to temporarily store NVM data. The write data is loaded to NVM data write register (NVDAT[4:0]) and then is written to NVM. NVM data is loaded to UID[4:0] when power-on reset, when shutdown mode is exited, or when CALB = 1 is written. |
## Gamma Control (R380h~R389h)

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</table>

**Description**

- **PR0P00[4:0]**: Adjusts reference level for positive polarity output R0
- **PR0N00[4:0]**: Adjusts reference level for negative polarity output R0
- **PR0P01[4:0]**: Adjusts reference level for positive polarity output R1
- **PR0N01[4:0]**: Adjusts reference level for negative polarity output R1
- **PR0P02[4:0]**: Adjusts reference level for positive polarity output R2
- **PR0N02[4:0]**: Adjusts reference level for negative polarity output R2
- **PR0P03[3:0]**: Adjusts reference level for positive polarity output R3
- **PR0N03[3:0]**: Adjusts reference level for negative polarity output R3
- **PR0P04[3:0]**: Adjusts reference level for positive polarity output R4
PR0N04[3:0]: Adjusts reference level for negative polarity output R4
PR0P05[3:0]: Adjusts reference level for positive polarity output R5
PR0N05[3:0]: Adjusts reference level for negative polarity output R5
PR0P06[4:0]: Adjusts reference level for positive polarity output R6
PR0N06[4:0]: Adjusts reference level for negative polarity output R6
PR0P07[4:0]: Adjusts reference level for positive polarity output R7
PR0N07[4:0]: Adjusts reference level for negative polarity output R7
PR0P08[4:0]: Adjusts reference level for positive polarity output R8
PR0N08[4:0]: Adjusts reference level for negative polarity output R8
PI0P0~1[1:0]: Adjusts interpolation level for positive polarity output (V2~V7)
PI0N0~1[1:0]: Adjusts interpolation level for negative polarity output (V2~V7)
PI0P2~3[1:0]: Adjusts interpolation level for positive polarity output (V56~V61)
PI0N2~3[1:0]: Adjusts interpolation level for negative polarity output (V56~V61)

Note: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.
### Base Image Display Control (R400h, R401h, R404h)

<table>
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<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>↑</td>
<td></td>
<td>GS</td>
<td></td>
<td></td>
<td>NL[5:0]</td>
<td>0</td>
<td>0</td>
<td>SCN[5:0]</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Default value</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>R401h</td>
<td>1</td>
<td>↑</td>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Default value</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>R404h</td>
<td>1</td>
<td>↑</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Default value</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**SCN [5:0]:** Specifies the gate line where the gate driver starts scan.

<table>
<thead>
<tr>
<th>SCN[5:0]</th>
<th>Scanning Start Position</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SM=0</td>
</tr>
<tr>
<td>00h</td>
<td>G1</td>
</tr>
<tr>
<td>01h</td>
<td>G9</td>
</tr>
<tr>
<td>02h</td>
<td>G17</td>
</tr>
<tr>
<td>03h</td>
<td>G25</td>
</tr>
<tr>
<td>04h</td>
<td>G33</td>
</tr>
<tr>
<td>05h</td>
<td>G41</td>
</tr>
<tr>
<td>06h</td>
<td>G49</td>
</tr>
<tr>
<td>07h</td>
<td>G57</td>
</tr>
<tr>
<td>08h</td>
<td>G65</td>
</tr>
<tr>
<td>09h</td>
<td>G73</td>
</tr>
<tr>
<td>0Ah</td>
<td>G81</td>
</tr>
<tr>
<td>0Bh</td>
<td>G89</td>
</tr>
<tr>
<td>0Ch</td>
<td>G97</td>
</tr>
<tr>
<td>0Dh</td>
<td>G105</td>
</tr>
<tr>
<td>0 Eh</td>
<td>G113</td>
</tr>
<tr>
<td>0Fh</td>
<td>G121</td>
</tr>
<tr>
<td>10h</td>
<td>G129</td>
</tr>
<tr>
<td>11h</td>
<td>G137</td>
</tr>
<tr>
<td>12h</td>
<td>G145</td>
</tr>
<tr>
<td>13h</td>
<td>G153</td>
</tr>
<tr>
<td>14h</td>
<td>G161</td>
</tr>
<tr>
<td>15h</td>
<td>G169</td>
</tr>
<tr>
<td>Address</td>
<td>Gate 1</td>
</tr>
<tr>
<td>---------</td>
<td>--------</td>
</tr>
<tr>
<td>16h</td>
<td>G177</td>
</tr>
<tr>
<td>17h</td>
<td>G185</td>
</tr>
<tr>
<td>18h</td>
<td>G193</td>
</tr>
<tr>
<td>19h</td>
<td>G201</td>
</tr>
<tr>
<td>1Ah</td>
<td>G209</td>
</tr>
<tr>
<td>1Bh</td>
<td>G217</td>
</tr>
<tr>
<td>1Ch</td>
<td>G225</td>
</tr>
<tr>
<td>1Dh</td>
<td>G233</td>
</tr>
<tr>
<td>1 Eh</td>
<td>G241</td>
</tr>
<tr>
<td>1Fh</td>
<td>G249</td>
</tr>
<tr>
<td>20h</td>
<td>G257</td>
</tr>
<tr>
<td>21h</td>
<td>G265</td>
</tr>
<tr>
<td>22h</td>
<td>G273</td>
</tr>
<tr>
<td>23h</td>
<td>G281</td>
</tr>
<tr>
<td>24h</td>
<td>G289</td>
</tr>
<tr>
<td>25h</td>
<td>G297</td>
</tr>
<tr>
<td>26h</td>
<td>G305</td>
</tr>
<tr>
<td>27h</td>
<td>G313</td>
</tr>
<tr>
<td>28h</td>
<td>G321</td>
</tr>
<tr>
<td>29h</td>
<td>G329</td>
</tr>
<tr>
<td>2Ah</td>
<td>G337</td>
</tr>
<tr>
<td>2Bh</td>
<td>G345</td>
</tr>
<tr>
<td>2Ch</td>
<td>G353</td>
</tr>
<tr>
<td>2 Dh</td>
<td>G361</td>
</tr>
<tr>
<td>2 Eh</td>
<td>G369</td>
</tr>
<tr>
<td>2 Fh</td>
<td>G377</td>
</tr>
<tr>
<td>30h</td>
<td>G385</td>
</tr>
<tr>
<td>31h</td>
<td>G393</td>
</tr>
<tr>
<td>32h</td>
<td>G401</td>
</tr>
<tr>
<td>33h</td>
<td>G409</td>
</tr>
<tr>
<td>34h</td>
<td>G417</td>
</tr>
<tr>
<td>35h ~ 3Fh</td>
<td>Setting prohibited</td>
</tr>
</tbody>
</table>

Note: "N" is the number of line decided by NL[5:]. Make sure that "Gate scan start position + NL " does not exceed 432 lines.

**NL [5:0]:** Sets the number of lines to drive the LCD at an interval of 8 lines. The DRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the...
same or more than the number of lines necessary for the size of the liquid crystal panel.

<table>
<thead>
<tr>
<th>NL[5:0]</th>
<th>LCD Drive Line</th>
<th>NL[5:0]</th>
<th>LCD Drive Line</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Setting inhibited</td>
<td>1Dh</td>
<td>240 lines</td>
</tr>
<tr>
<td>01h</td>
<td>16 lines</td>
<td>1Eh</td>
<td>248 lines</td>
</tr>
<tr>
<td>02h</td>
<td>24 lines</td>
<td>1Fh</td>
<td>256 lines</td>
</tr>
<tr>
<td>03h</td>
<td>32 lines</td>
<td>20h</td>
<td>264 lines</td>
</tr>
<tr>
<td>04h</td>
<td>40 lines</td>
<td>21h</td>
<td>272 lines</td>
</tr>
<tr>
<td>05h</td>
<td>48 lines</td>
<td>22h</td>
<td>280 lines</td>
</tr>
<tr>
<td>06h</td>
<td>56 lines</td>
<td>23h</td>
<td>288 lines</td>
</tr>
<tr>
<td>07h</td>
<td>64 lines</td>
<td>24h</td>
<td>296 lines</td>
</tr>
<tr>
<td>08h</td>
<td>72 lines</td>
<td>25h</td>
<td>304 lines</td>
</tr>
<tr>
<td>09h</td>
<td>80 lines</td>
<td>26h</td>
<td>312 lines</td>
</tr>
<tr>
<td>0Ah</td>
<td>88 lines</td>
<td>27h</td>
<td>320 lines</td>
</tr>
<tr>
<td>0Bh</td>
<td>96 lines</td>
<td>28h</td>
<td>328 lines</td>
</tr>
<tr>
<td>0Ch</td>
<td>104 lines</td>
<td>29h</td>
<td>336 lines</td>
</tr>
<tr>
<td>0Dh</td>
<td>112 lines</td>
<td>2Ah</td>
<td>344 lines</td>
</tr>
<tr>
<td>0 Eh</td>
<td>120 lines</td>
<td>2Bh</td>
<td>352 lines</td>
</tr>
<tr>
<td>0Fh</td>
<td>128 lines</td>
<td>2Ch</td>
<td>360 lines</td>
</tr>
<tr>
<td>10h</td>
<td>136 lines</td>
<td>2Dh</td>
<td>368 lines</td>
</tr>
<tr>
<td>11h</td>
<td>144 lines</td>
<td>2 Eh</td>
<td>376 lines</td>
</tr>
<tr>
<td>12h</td>
<td>152 lines</td>
<td>2Fh</td>
<td>384 lines</td>
</tr>
<tr>
<td>13h</td>
<td>160 lines</td>
<td>30h</td>
<td>392 lines</td>
</tr>
<tr>
<td>14h</td>
<td>168 lines</td>
<td>31h</td>
<td>400 lines</td>
</tr>
<tr>
<td>15h</td>
<td>176 lines</td>
<td>32h</td>
<td>408 lines</td>
</tr>
<tr>
<td>16h</td>
<td>184 lines</td>
<td>33h</td>
<td>416 lines</td>
</tr>
<tr>
<td>17h</td>
<td>192 lines</td>
<td>34h</td>
<td>424 lines</td>
</tr>
<tr>
<td>18h</td>
<td>200 lines</td>
<td>35h</td>
<td>432 lines</td>
</tr>
<tr>
<td>19h</td>
<td>208 lines</td>
<td>Others</td>
<td>Setting inhibited</td>
</tr>
<tr>
<td>1Ah</td>
<td>216 lines</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Bh</td>
<td>224 lines</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Ch</td>
<td>232 lines</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**GS**: Sets the direction of scan of the gate driver. Set GS bit in combination with SM bit for the convenience of the display module configuration and the display direction. When GS=0, the scan direction is from G1 to G432.
When GS=1, the scan direction is from G432 to G1

**NDL:** Sets the source output level in non display area in partial mode.

<table>
<thead>
<tr>
<th>NDL</th>
<th>Non-Display Area</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Positive Polarity</td>
</tr>
<tr>
<td>0</td>
<td>V63</td>
</tr>
<tr>
<td>1</td>
<td>V0</td>
</tr>
</tbody>
</table>

**REV:** Enables the grayscale inversion of the image by setting REV = 1. This enables the ST7793 to display the same image from the same set of data whether the liquid crystal panel is normally black or white.

<table>
<thead>
<tr>
<th>REV</th>
<th>DRAM Data</th>
<th>Display Area</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Positive Polarity</td>
</tr>
<tr>
<td>0</td>
<td>00000h</td>
<td>V63</td>
</tr>
<tr>
<td></td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td></td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td></td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td></td>
<td>3FFFFh</td>
<td>V0</td>
</tr>
<tr>
<td>1</td>
<td>00000h</td>
<td>V0</td>
</tr>
<tr>
<td></td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td></td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td></td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td></td>
<td>3FFFFh</td>
<td>V63</td>
</tr>
</tbody>
</table>

**VLE:** Vertical scroll display enable bit. When VLE = 1, the ST7793 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = 0

<table>
<thead>
<tr>
<th>VLE</th>
<th>Base Image Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Fixed</td>
</tr>
<tr>
<td>1</td>
<td>Enable Scrolling</td>
</tr>
</tbody>
</table>

**VL[8:0]:** Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0] \(\leq 432\).
### 10.2.21 Partial Display Control (R500h, R501h, R502h)

<table>
<thead>
<tr>
<th>Partial Display Control (R500h,R501h, R502h)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>R500h</strong></td>
</tr>
<tr>
<td>RS</td>
</tr>
<tr>
<td>----</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>Default value</td>
</tr>
</tbody>
</table>

**Description**

PTDP [8:0]: Sets the display position of partial image.

PTSA [8:0] and PTEA [8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image. In setting, make sure that PTSA ≤ PTEA.

### 10.2.22 Test Register (R600h)

<table>
<thead>
<tr>
<th>Test Register (R600h)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RS</strong></td>
</tr>
<tr>
<td>------</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>Default value</td>
</tr>
</tbody>
</table>

**Description**

TRST: When TRST=1, settings for R380h~R389h, R710h, R712h, R713h, and R724h are reset to default values. When finished, please set TRST to 0.
### 10.2.23 NVM Access Control (R6F0h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Default value**: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

**Description**
CALB: When CALB = 1, all data in NVM is read out and written to internal registers. When finished, CALB is set to 0.

### 10.2.24 VCOM Control (R702h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>VCMS[6:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Default value**: 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0

**Description**
VCMS[6:0]: Set the relative VCOM offset.

VCMWREN: Selection the VCM setting. When the NV memory is programmed, the VCMWREN will be set as ‘1’ automatically.

VCMWREN = 1 Register 702h for VCM setting
VCMWREN = 0 NV Memory selected for VCM setting

<table>
<thead>
<tr>
<th>VCMS[6:0]</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h~21h</td>
<td>420 mV</td>
</tr>
<tr>
<td>22h</td>
<td>440 mV</td>
</tr>
<tr>
<td>23h</td>
<td>460 mV</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>41h</td>
<td>1060 mV</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>5Eh</td>
<td>1640 mV</td>
</tr>
<tr>
<td>5Fh</td>
<td>1660 mV</td>
</tr>
<tr>
<td>60h~7Fh</td>
<td>1680 mV</td>
</tr>
</tbody>
</table>

**Note**: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.

VCMWREN is set by R709h.
### 10.2.25 ID2 (R708h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Default value**

|             | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

**Description**

ID2[4:0]: 5-bit NVM for ID usage.

*Note: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.*

### 10.2.26 NVM VCMWREN Setting (R709h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Default value**

|             | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

**Description**

VCMWREN: Selection the VCM setting. When the NV memory is programmed, the VCMWREN will be set as ‘1’ automatically.

VCMWREN =1 Register 702h for VCM setting

VCMWREN =0 NV Memory selected for VCM setting

*Note: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.*
## Source Control 1 (R710h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>VRH[4:0]</td>
</tr>
</tbody>
</table>

**Default value**: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

### VRH[3:0]

Sets amplitude of VAP to VBP and VAN to VBN.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>00h~0Fh</td>
<td>Setting Prohibited</td>
<td>18h</td>
<td>4.489 V</td>
</tr>
<tr>
<td>10h</td>
<td>4.034 V</td>
<td>19h</td>
<td>4.553 V</td>
</tr>
<tr>
<td>11h</td>
<td>4.086 V</td>
<td>1Ah</td>
<td>4.619 V</td>
</tr>
<tr>
<td>12h</td>
<td>4.139 V</td>
<td>1Bh</td>
<td>4.687 V</td>
</tr>
<tr>
<td>13h</td>
<td>4.194 V</td>
<td>1Ch</td>
<td>4.757 V</td>
</tr>
<tr>
<td>14h</td>
<td>4.250 V</td>
<td>1Dh</td>
<td>4.829 V</td>
</tr>
<tr>
<td>15h</td>
<td>4.307 V</td>
<td>1Eh</td>
<td>4.903 V</td>
</tr>
<tr>
<td>16h</td>
<td>4.366 V</td>
<td>1Fh</td>
<td>4.980 V</td>
</tr>
<tr>
<td>17h</td>
<td>4.427 V</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Note**: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.
### Source Control 2 (R712h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Default value:**

| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 1   | 1   |

**Description:**

**VDV[4:0]:** Sets the voltage difference between VBP and VBN.

<table>
<thead>
<tr>
<th>VDV [4:0]</th>
<th>VBP - VBN</th>
</tr>
</thead>
<tbody>
<tr>
<td>00~0Eh</td>
<td>Setting Prohibited</td>
</tr>
<tr>
<td>0Fh</td>
<td>0 mV</td>
</tr>
<tr>
<td>10h</td>
<td>40mV</td>
</tr>
<tr>
<td>11h</td>
<td>80mV</td>
</tr>
<tr>
<td>12h</td>
<td>120mV</td>
</tr>
<tr>
<td>13h</td>
<td>160mV</td>
</tr>
<tr>
<td>14h</td>
<td>200mV</td>
</tr>
<tr>
<td>15h</td>
<td>240mV</td>
</tr>
<tr>
<td>16h</td>
<td>280mV</td>
</tr>
<tr>
<td>17h</td>
<td>320mV</td>
</tr>
<tr>
<td>18h</td>
<td>360mV</td>
</tr>
<tr>
<td>19h</td>
<td>400mV</td>
</tr>
<tr>
<td>1Ah</td>
<td>440mV</td>
</tr>
<tr>
<td>1Bh</td>
<td>480mV</td>
</tr>
<tr>
<td>1Ch</td>
<td>520mV</td>
</tr>
<tr>
<td>1Dh</td>
<td>560mV</td>
</tr>
<tr>
<td>1Eh</td>
<td>600mV</td>
</tr>
<tr>
<td>1Fh</td>
<td>640mV</td>
</tr>
</tbody>
</table>

**Note:** `CMD2_EN (R0FFh)` must be set to ‘1’ before accessing this register.
10.2.29 Gate Control (R713h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Default value**

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Description**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0h</td>
<td>-12.87 V</td>
<td>8h</td>
<td>-10.38 V</td>
</tr>
<tr>
<td>1h</td>
<td>-12.56 V</td>
<td>9h</td>
<td>-10.07 V</td>
</tr>
<tr>
<td>2h</td>
<td>-12.25 V</td>
<td>Ah</td>
<td>-9.75 V</td>
</tr>
<tr>
<td>3h</td>
<td>-11.94 V</td>
<td>Bh</td>
<td>-9.44 V</td>
</tr>
<tr>
<td>4h</td>
<td>-11.52 V</td>
<td>Ch</td>
<td>-9.13 V</td>
</tr>
<tr>
<td>5h</td>
<td>-11.31 V</td>
<td>Dh</td>
<td>-8.82 V</td>
</tr>
<tr>
<td>6h</td>
<td>-11.00 V</td>
<td>Eh</td>
<td>-8.51 V</td>
</tr>
<tr>
<td>7h</td>
<td>-10.69 V</td>
<td>Fh</td>
<td>-8.20 V</td>
</tr>
</tbody>
</table>

**VGHS[3:0]**: VGH voltage level selection.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0h</td>
<td>12.16 V</td>
<td>8h</td>
<td>13.70 V</td>
</tr>
<tr>
<td>1h</td>
<td>12.36 V</td>
<td>9h</td>
<td>13.89 V</td>
</tr>
<tr>
<td>2h</td>
<td>12.55 V</td>
<td>Ah</td>
<td>14.09 V</td>
</tr>
<tr>
<td>3h</td>
<td>12.74 V</td>
<td>Bh</td>
<td>14.28 V</td>
</tr>
<tr>
<td>4h</td>
<td>12.93 V</td>
<td>Ch</td>
<td>14.47 V</td>
</tr>
<tr>
<td>5h</td>
<td>13.13 V</td>
<td>Dh</td>
<td>14.66 V</td>
</tr>
<tr>
<td>6h</td>
<td>13.32 V</td>
<td>Eh</td>
<td>14.86 V</td>
</tr>
<tr>
<td>7h</td>
<td>13.51 V</td>
<td>Fh</td>
<td>15.05 V</td>
</tr>
</tbody>
</table>

**Note:** CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.
### Frame Rate Control (R724h)

#### RTNI[4:0] : Sets the fOSC value so that the line period will be affected.

<table>
<thead>
<tr>
<th>RTNI[4:0]</th>
<th>fOSC Value (MHz)</th>
<th>1 Line Period (μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h~0Fh</td>
<td>Setting Prohibited</td>
<td></td>
</tr>
<tr>
<td>10h</td>
<td>5.38</td>
<td>23.8</td>
</tr>
<tr>
<td>11h</td>
<td>5.06</td>
<td>25.3</td>
</tr>
<tr>
<td>12h</td>
<td>4.78</td>
<td>26.8</td>
</tr>
<tr>
<td>13h</td>
<td>4.53</td>
<td>28.3</td>
</tr>
<tr>
<td>14h</td>
<td>4.30</td>
<td>29.8</td>
</tr>
<tr>
<td>15h</td>
<td>4.10</td>
<td>31.2</td>
</tr>
<tr>
<td>16h</td>
<td>3.91</td>
<td>32.7</td>
</tr>
<tr>
<td>17h</td>
<td>3.74</td>
<td>34.2</td>
</tr>
<tr>
<td>18h</td>
<td>3.58</td>
<td>35.8</td>
</tr>
<tr>
<td>19h</td>
<td>3.4</td>
<td>37.2</td>
</tr>
<tr>
<td>1Ah</td>
<td>3.31</td>
<td>38.7</td>
</tr>
<tr>
<td>1Bh</td>
<td>3.19</td>
<td>40.1</td>
</tr>
<tr>
<td>1Ch</td>
<td>3.07</td>
<td>41.7</td>
</tr>
<tr>
<td>1Dh</td>
<td>2.97</td>
<td>43.1</td>
</tr>
<tr>
<td>1 Eh</td>
<td>2.87</td>
<td>44.6</td>
</tr>
<tr>
<td>1Fh</td>
<td>2.77</td>
<td>46.2</td>
</tr>
</tbody>
</table>

#### DIVI[1:0] : Sets the division ratio of internal clock frequency.

<table>
<thead>
<tr>
<th>DIVI[1:0]</th>
<th>Division Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>0h</td>
<td>1</td>
</tr>
<tr>
<td>1h</td>
<td>2</td>
</tr>
<tr>
<td>2h</td>
<td>4</td>
</tr>
<tr>
<td>3h</td>
<td>8</td>
</tr>
</tbody>
</table>

*Note: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.*
### 10.2.31 Source Driving Control (R752h)

**Source Driving Control (R752h)**

| RS | WRX | RDX | D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | ↑   | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | SD[1]| SD[0]| 1   | 1   | 1   |

**Default value**

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

**Description**

**SD[1:0]**: Source Driving Control

<table>
<thead>
<tr>
<th>WCMD[7:0]</th>
<th>Driving</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Fh</td>
<td>Small</td>
</tr>
<tr>
<td>1Fh</td>
<td>Medium</td>
</tr>
<tr>
<td>2Fh</td>
<td>Medium High</td>
</tr>
<tr>
<td>3Fh</td>
<td>Large</td>
</tr>
</tbody>
</table>

*Note: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.*

### 10.2.32 Gate Turn on Timing Control (R754)

**Gate Turn on Timing Control (R754h)**

| RS | WRX | RDX | D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|

**Default value**

0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

**TGO[5:0]**: Gate turn Timing Control

<table>
<thead>
<tr>
<th>TGO[5:0]</th>
<th>Turn on Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Large</td>
</tr>
<tr>
<td>3Fh</td>
<td>Small</td>
</tr>
</tbody>
</table>

*Note: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.*
### NVM Write Control (R7E1h)

<table>
<thead>
<tr>
<th>RS</th>
<th>WRX</th>
<th>RDX</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>WCMD[7:0]</td>
</tr>
</tbody>
</table>

**Default value:**

| RS | WRX | RDX | D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Description:**

**RCMD[7:0] : NVM Write Operation Selection**

<table>
<thead>
<tr>
<th>WCMD[7:0]</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>3Ah</td>
<td>Program</td>
</tr>
<tr>
<td>A5h</td>
<td>Active Code</td>
</tr>
<tr>
<td>C5h</td>
<td>Erase</td>
</tr>
<tr>
<td>Others</td>
<td>Setting Prohibited</td>
</tr>
</tbody>
</table>

After writing Program (3Ah) / Erase (C5h) parameter, Active Code (A5h) must be appended as the second parameter to activate the operation specified by the first parameter.

*Note: CMD2_EN (R0FFh) must be set to ‘1’ before accessing this register.*
11 RESET FUNCTION

The ST7793 is initialized by the RESET input. During reset period, the ST7793 is in a busy state and instruction from the MCU and DRAM access are not accepted. The ST7793’s internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, DRAM access and initial instruction setting are prohibited.

11.1. Register Values

See the Instruction description. The default value is shown in the parenthesis of each instruction bit cell.

11.2. Display RAM Data Initialization

The Display RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period (BASEE=0).

11.3. Reset Timing Characteristic

![Figure 41 Reset Timing](image)

Table 8 Reset timing Characteristics

<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>TRESL</td>
<td>Reset Low Level Width</td>
<td>1</td>
<td>-</td>
<td>ms</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>TREST</td>
<td>Reset Complete Time</td>
<td>1</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

VDD1=1.65 to VDD, VDD2=2.5 to 3.3V, AGND=DGND=0V, Ta=25°C
12 FMARK FUNCTION

The ST7793 outputs an FMARK pulse when the ST7793 is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

<table>
<thead>
<tr>
<th>FMI[2:0]</th>
<th>Output Interval</th>
</tr>
</thead>
<tbody>
<tr>
<td>“000”</td>
<td>1 Frame</td>
</tr>
<tr>
<td>“001”</td>
<td>2 Frame</td>
</tr>
<tr>
<td>“011”</td>
<td>4 Frame</td>
</tr>
<tr>
<td>“101”</td>
<td>6 Frame</td>
</tr>
<tr>
<td>Others</td>
<td>Setting Prohibited</td>
</tr>
</tbody>
</table>

Table 9 FMARK Interval

<table>
<thead>
<tr>
<th>FMP[8:0]</th>
<th>FMARK Output Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>000h</td>
<td>0 th line</td>
</tr>
<tr>
<td>001h</td>
<td>1 st line</td>
</tr>
<tr>
<td>002h</td>
<td>2 nd line</td>
</tr>
<tr>
<td>003h</td>
<td>3 rd line</td>
</tr>
<tr>
<td>1BDh</td>
<td>445 th line</td>
</tr>
<tr>
<td>1BEh</td>
<td>446 th line</td>
</tr>
<tr>
<td>1BFh</td>
<td>447 th line</td>
</tr>
<tr>
<td>177h</td>
<td>Setting Prohibited</td>
</tr>
</tbody>
</table>

Table 10 FMARK Output Position
12.1.. FMP Setting Example

Figure 42 FMARK Setting Example
12.2. Display Operation Synchronous Data Transfer Using FMARK

The ST7793 uses FMARK signal as a trigger output for indicating the start of data-writing to the internal DRAM in synchronization with display scan operation.

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture DRAM area without causing flicker on the display. The data is written in the internal RAM in order to transfer only the data written over the moving picture display area and minimize the data transfer required for moving picture display.

When transferring data in synchronization with FMARK signal, frame frequency and minimum DRAM data write speed must be taken into consideration. First, all DRAM writes must be completed within one frame. Secondly, each write operation of pixel data must be done within the minimum DRAM Write Speed. They can be calculated from the following equations.
\[
\text{Frame Period} = \frac{(\text{Display Lines} + \text{FrontPorch} + \text{BackPorch}) \times 128}{f_{\text{OSC}} \times (RTNI)}
\]

\[
\text{DRAM Write Speed (min)} > \frac{f_{\text{OSC}} \times (RTNI) \times 240}{128}
\]

Note: When RAM write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

Examples of DRAM writes speed and the frequency of the internal clocks are as follows.

**Example:**

- **Display size:** 240 RGB x 432 lines,
- **Total number of lines (NL):** 432 lines
- **Back/Front porch:** 13/3 lines
- **Internal Clock Frequency (RTNI[4:0]):** 3.44MHz

\[
\text{Frame Data Update Period} < \frac{(432 + 3 + 13) \times 128}{3.44 \times 10^6} = 16.669 \text{ ms}
\]

Note1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one FMARK cycle.

Note2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

\[
\text{Minimum Speed for DRAM Writing [Hz]} > \frac{3.44 \times 10^6 \times 240}{128} = 6.45 \text{ MHz}
\]

Note1. In this example, it is assumed that the ST7793 starts writing data in the internal DRAM on the rising edge of FMARK.

Note2. There must be at least a margin of 2 lines between the line to which the ST7793 has just written data and the line where display operation on the LCD is performed.

Note3. The FMARK signal output position is set to the line specified by FMP[8:0] bits.

In this example, DRAM write operation at a speed of 6.45MHz or more, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the ST7793 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.
13 8 - COLOR DISPLAY MODE

The ST7793 has a function to display in 8 colors. In this display mode, only V0 and V63 are used and power supplies to other grayscales are turned off to reduce power consumption. The ST7793 does not need DRAM data rewrite for 8-color display. ST7793 uses the MSB of each sub-pixel as the rest part in each dot data to display in 8 colors.

Figure 45 8-Color Display Mode

Follow the figures below to switch between 8-color display mode and 262k-color display mode.

**262k-Color to 8-Color**

**State**
262k-Color Display Mode

Enable 8-Color Display Mode
RDISBk COL=1

**State**
8-Color Display Mode

**State**
262k-Color Display Mode

**8-Color to 262k-Color**

**State**
8-Color Display Mode

Disable 8-Color Display Mode
RDISBk COL=0

**State**
262k-Color Display Mode

Figure 46 8-Color / 262k-Color Switch Sequences
The ST7793 allows selectively driving partial image on the screen at arbitrary positions set in the screen drive position registers. To switch between full-screen display and partial display mode, follow the sequences below.

**Full Screen to Partial Display**

1. State: Full Screen Display
   - Partial Display Setting
     - $R000h$: PTDR[8:0]
     - $R01h$: PTSA[8:0]
     - $R02h$: PTEA[8:0]
   - Partial Display On
     - $R007h$: BASEE=0, PTDE=1
   - State: Partial Display

**Partial to Full Screen Display**

1. State: Partial Display
   - Base Image Display On
     - $R007h$: BASEE=1, PTDE=0
   - State: Full Screen Display

Figure 47 Shutdown Mode Enter/Exit Sequences
The following example shows the setting for partial display function:

### Base Image Display Setting

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>BASEE</td>
<td>1</td>
</tr>
<tr>
<td>PTDE</td>
<td>0</td>
</tr>
</tbody>
</table>

### Partial Image Display Setting

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>BASEE</td>
<td>0</td>
</tr>
<tr>
<td>PTDE</td>
<td>1</td>
</tr>
<tr>
<td>PTSA[8:0]</td>
<td>020h</td>
</tr>
<tr>
<td>PTEA[8:0]</td>
<td>02Fh</td>
</tr>
<tr>
<td>PTDP[8:0]</td>
<td>0C0h</td>
</tr>
</tbody>
</table>

Table 11 Partial Setting Example

<table>
<thead>
<tr>
<th>Partial Image Display RAM Area</th>
<th>LCD Panel</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTSA = 9'h000</td>
<td>0 (1st line)</td>
</tr>
<tr>
<td>PTEA = 9'h02F</td>
<td>1 (2nd line)</td>
</tr>
<tr>
<td></td>
<td>2 (3rd line)</td>
</tr>
</tbody>
</table>

Figure 48 Partial Display Example
15 SCAN MODE

The ST7793 can set the gate pin assignment and the scan direction in the following 4 ways by setting SM and GS bits to meet various connections between the ST7793 and the LCD panel.

<table>
<thead>
<tr>
<th>SM</th>
<th>Scan Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Interchanging Forward Direction (GS=0)</td>
</tr>
<tr>
<td></td>
<td><img src="#" alt="Scan Order (Gate Line No.)" /> G1&gt;&lt;G2&gt;&lt;G3&gt;&lt;G4&gt;&lt;G430&gt;&lt;G431&gt;&lt;G432</td>
</tr>
<tr>
<td>1</td>
<td>Interchanging Backward Direction (GS=1)</td>
</tr>
<tr>
<td></td>
<td><img src="#" alt="Scan Order (Gate Line No.)" /> G432&gt;&lt;G431&gt;&lt;G430&gt;&lt;G429&gt;&lt;G431&gt;&lt;G430</td>
</tr>
<tr>
<td></td>
<td><img src="#" alt="Scan Order (Gate Line No.)" /> G1&gt;&lt;G2&gt;&lt;G3&gt;&lt;G4&gt;&lt;G430&gt;&lt;G431&gt;&lt;G432</td>
</tr>
<tr>
<td></td>
<td><img src="#" alt="Scan Order (Gate Line No.)" /> G432&gt;&lt;G431&gt;&lt;G430&gt;&lt;G429&gt;&lt;G431&gt;&lt;G430</td>
</tr>
</tbody>
</table>

Figure 49 Scan Mode Settings
16 WINDOW ADDRESS FUNCTION

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal Display RAM. The window address area is made by setting the horizontal address register (start: HSA [7:0], end HEA [7:0] bits) and the vertical address register (start: VSA [8:0], end: VEA [8:0] bits) The AM and ID bits sets the transition direction of RAM address (either increment or decrement, horizontal or vertical). These bits enable the ST7793 to write data including image data consecutively without taking data wrap positions into account.

The window address area must be made within the DRAM address map area. Also, DRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]
(Horizontal direction) 00H ≤ HSA[7:0] ≤ HEA[7:0] ≤ EFh
(Vertical direction) 00H ≤ VSA[8:0] ≤ VEA[8:0] ≤ 1AFh

[RAM address, AD (an address within a window address area)]
(RAM address) HSA[7:0] ≤ AD[7:0] ≤ HEA[7:0]
VSA[8:0] ≤ AD[16:8] ≤ VEA[8:0]

![Figure 50 Display RAM Access Window Map](image)
17 GAMMA CORRECTION

The ST7793 supports $\gamma$-correction function to make the optimal colors according to the characteristics of the panel. The ST7793 has registers for positive and negative polarities.

17.1. Gamma Correction Circuits

The following figure shows the $\gamma$-correction circuit. According to the settings of variable resistors R0 to R8, the voltage level, the difference between VAP/VBP and VAN/VBN, is evenly divided into 8 grayscale reference voltages (V0, V1, V8, V20, V43, V55, V62, and V63). Other 56-grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltage, see "Grayscale Voltage Calculation Formula".

![Grayscale Voltage Generation Diagram]

VAP / VAN

0~31R (1R)

1~32R (1R)

2~33R (1R)

4~19R (1R)

8~23R (1R)

4~19R (1R)

2~33R (1R)

1~32R (1R)

2~33R (1R)

VBP / VBN

R : Resistor Outputting Voltage Evenly Divided into 12 (1R) : Trimming Step

VAP/VBP for Positive Grayscale Voltage Generation

VAN/VBN for Negative Grayscale Voltage Generation

Interpolation Adjustment

Linear Interpolation

Interpolation Adjustment

Figure 51 Grayscale Voltage Generation
17.2. Gamma Correction Registers

The $\gamma$-correction registers include 42 bits for each of R, G, and B dots and 8-bit interpolation adjustment registers.

1. Reference Level Adjustment Registers

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Positive Polarity</th>
<th>Negative Polarity</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>PR0P00[4:0]</td>
<td>PR0N00[4:0]</td>
</tr>
<tr>
<td>R1</td>
<td>PR0P01[4:0]</td>
<td>PR0N01[4:0]</td>
</tr>
<tr>
<td>R2</td>
<td>PR0P02[4:0]</td>
<td>PR0N02[4:0]</td>
</tr>
<tr>
<td>R3</td>
<td>PR0P03[3:0]</td>
<td>PR0N03[3:0]</td>
</tr>
<tr>
<td>R4</td>
<td>PR0P04[3:0]</td>
<td>PR0N04[3:0]</td>
</tr>
<tr>
<td>R5</td>
<td>PR0P05[3:0]</td>
<td>PR0N05[3:0]</td>
</tr>
<tr>
<td>R6</td>
<td>PR0P06[4:0]</td>
<td>PR0N06[4:0]</td>
</tr>
<tr>
<td>R7</td>
<td>PR0P07[4:0]</td>
<td>PR0N07[4:0]</td>
</tr>
<tr>
<td>R8</td>
<td>PR0P08[4:0]</td>
<td>PR0N08[4:0]</td>
</tr>
</tbody>
</table>

Table 12 Reference Level Adjustment Registers
### Table 13 Reference Level Adjustment Registers and Resistors

#### 2. Interpolation Registers

<table>
<thead>
<tr>
<th>Interpolation Adjustment</th>
<th>Positive Polarity</th>
<th>Negative Polarity</th>
</tr>
</thead>
<tbody>
<tr>
<td>V2~V7</td>
<td>P10*0[1:0]</td>
<td>P10N0[1:0]</td>
</tr>
<tr>
<td></td>
<td>P10*1[1:0]</td>
<td>P10N1[1:0]</td>
</tr>
<tr>
<td>V56~V61</td>
<td>P10*2[1:0]</td>
<td>P10N2[1:0]</td>
</tr>
<tr>
<td></td>
<td>P10*3[1:0]</td>
<td>P10N3[1:0]</td>
</tr>
</tbody>
</table>

#### Table 14 Interpolation Registers

<table>
<thead>
<tr>
<th>P10*0[1:0]</th>
<th>P10*1[1:0]</th>
<th>IPV2</th>
<th>IPV3</th>
<th>IPV4</th>
<th>IPV5</th>
<th>IPV6</th>
<th>IPV7</th>
</tr>
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<tbody>
<tr>
<td>0h</td>
<td>0h</td>
<td>81%</td>
<td>67%</td>
<td>52%</td>
<td>39%</td>
<td>26%</td>
<td>13%</td>
</tr>
<tr>
<td></td>
<td>1h</td>
<td>78%</td>
<td>61%</td>
<td>43%</td>
<td>33%</td>
<td>22%</td>
<td>11%</td>
</tr>
<tr>
<td></td>
<td>2h</td>
<td>73%</td>
<td>52%</td>
<td>31%</td>
<td>23%</td>
<td>15%</td>
<td>8%</td>
</tr>
<tr>
<td></td>
<td>3h</td>
<td>72%</td>
<td>50%</td>
<td>28%</td>
<td>21%</td>
<td>14%</td>
<td>7%</td>
</tr>
<tr>
<td>1h</td>
<td>0h</td>
<td>80%</td>
<td>68%</td>
<td>56%</td>
<td>42%</td>
<td>28%</td>
<td>14%</td>
</tr>
<tr>
<td></td>
<td>1h</td>
<td>76%</td>
<td>62%</td>
<td>48%</td>
<td>36%</td>
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</tr>
<tr>
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<td>26%</td>
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<td>9%</td>
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<td>3h</td>
<td>69%</td>
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<td>23%</td>
<td>16%</td>
<td>8%</td>
</tr>
<tr>
<td>2h</td>
<td>0h</td>
<td>78%</td>
<td>70%</td>
<td>61%</td>
<td>46%</td>
<td>30%</td>
<td>15%</td>
</tr>
<tr>
<td></td>
<td>1h</td>
<td>74%</td>
<td>63%</td>
<td>53%</td>
<td>39%</td>
<td>26%</td>
<td>13%</td>
</tr>
<tr>
<td></td>
<td>2h</td>
<td>66%</td>
<td>53%</td>
<td>39%</td>
<td>29%</td>
<td>20%</td>
<td>10%</td>
</tr>
<tr>
<td></td>
<td>3h</td>
<td>64%</td>
<td>50%</td>
<td>36%</td>
<td>27%</td>
<td>18%</td>
<td>9%</td>
</tr>
<tr>
<td>3h</td>
<td>0h</td>
<td>78%</td>
<td>70%</td>
<td>63%</td>
<td>47%</td>
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</tr>
<tr>
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<td>1h</td>
<td>73%</td>
<td>64%</td>
<td>54%</td>
<td>41%</td>
<td>27%</td>
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</tr>
<tr>
<td></td>
<td>2h</td>
<td>65%</td>
<td>53%</td>
<td>41%</td>
<td>31%</td>
<td>20%</td>
<td>10%</td>
</tr>
<tr>
<td></td>
<td>3h</td>
<td>63%</td>
<td>50%</td>
<td>37%</td>
<td>28%</td>
<td>19%</td>
<td>9%</td>
</tr>
</tbody>
</table>

*Note: * could be P or N.*

#### Table 15 Interpolation Factor for V2 to V7

<table>
<thead>
<tr>
<th>P10*0[1:0]</th>
<th>P10*1[1:0]</th>
<th>IPV2</th>
<th>IPV3</th>
<th>IPV4</th>
<th>IPV5</th>
<th>IPV6</th>
<th>IPV7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0h</td>
<td>0h</td>
<td>81%</td>
<td>67%</td>
<td>52%</td>
<td>39%</td>
<td>26%</td>
<td>13%</td>
</tr>
<tr>
<td></td>
<td>1h</td>
<td>78%</td>
<td>61%</td>
<td>43%</td>
<td>33%</td>
<td>22%</td>
<td>11%</td>
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<td>7%</td>
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<td>56%</td>
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<td>76%</td>
<td>62%</td>
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<td>36%</td>
<td>24%</td>
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<td>35%</td>
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<tr>
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<td>3h</td>
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<td>31%</td>
<td>23%</td>
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<td>8%</td>
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<td>0h</td>
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<td>46%</td>
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<tr>
<td></td>
<td>1h</td>
<td>74%</td>
<td>63%</td>
<td>53%</td>
<td>39%</td>
<td>26%</td>
<td>13%</td>
</tr>
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<td>2h</td>
<td>66%</td>
<td>53%</td>
<td>39%</td>
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<tr>
<td></td>
<td>3h</td>
<td>64%</td>
<td>50%</td>
<td>36%</td>
<td>27%</td>
<td>18%</td>
<td>9%</td>
</tr>
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<td>3h</td>
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<td>70%</td>
<td>63%</td>
<td>47%</td>
<td>31%</td>
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</tr>
<tr>
<td></td>
<td>1h</td>
<td>73%</td>
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<td>54%</td>
<td>41%</td>
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</tr>
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<td>50%</td>
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</tr>
</tbody>
</table>

*Note: * could be P or N.*
<table>
<thead>
<tr>
<th>PI0*3[1:0]</th>
<th>PI0*2[1:0]</th>
<th>IPV56</th>
<th>IPV57</th>
<th>IPV58</th>
<th>IPV59</th>
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<th>IPV61</th>
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<td>87%</td>
<td>74%</td>
<td>61%</td>
<td>48%</td>
<td>33%</td>
<td>19%</td>
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<td>1h</td>
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<td>78%</td>
<td>67%</td>
<td>57%</td>
<td>39%</td>
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<td>72%</td>
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</tr>
<tr>
<td></td>
<td>3h</td>
<td>92%</td>
<td>84%</td>
<td>77%</td>
<td>69%</td>
<td>50%</td>
<td>31%</td>
</tr>
<tr>
<td>2h</td>
<td>0h</td>
<td>85%</td>
<td>70%</td>
<td>54%</td>
<td>39%</td>
<td>30%</td>
<td>22%</td>
</tr>
<tr>
<td></td>
<td>1h</td>
<td>87%</td>
<td>74%</td>
<td>61%</td>
<td>47%</td>
<td>37%</td>
<td>26%</td>
</tr>
<tr>
<td></td>
<td>2h</td>
<td>90%</td>
<td>80%</td>
<td>71%</td>
<td>61%</td>
<td>47%</td>
<td>34%</td>
</tr>
<tr>
<td></td>
<td>3h</td>
<td>91%</td>
<td>82%</td>
<td>73%</td>
<td>64%</td>
<td>50%</td>
<td>36%</td>
</tr>
<tr>
<td>3h</td>
<td>0h</td>
<td>84%</td>
<td>69%</td>
<td>53%</td>
<td>38%</td>
<td>30%</td>
<td>22%</td>
</tr>
<tr>
<td></td>
<td>1h</td>
<td>86%</td>
<td>73%</td>
<td>59%</td>
<td>46%</td>
<td>36%</td>
<td>27%</td>
</tr>
<tr>
<td></td>
<td>2h</td>
<td>90%</td>
<td>80%</td>
<td>69%</td>
<td>59%</td>
<td>47%</td>
<td>35%</td>
</tr>
<tr>
<td></td>
<td>3h</td>
<td>91%</td>
<td>81%</td>
<td>72%</td>
<td>63%</td>
<td>50%</td>
<td>37%</td>
</tr>
</tbody>
</table>

*Note: * could be P or N.*

Table 16 Interpolation Factor for V56 to V61
<table>
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<tr>
<th>Grayscale Voltage</th>
<th>Formula</th>
<th>Grayscale Voltage</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>V0</td>
<td>(\Delta V \times \frac{\sum (R1...R8)}{SUMR})</td>
<td>V32</td>
<td>V43 + ((V20 - V43) \times 11/23)</td>
</tr>
<tr>
<td>V1</td>
<td>(\Delta V \times \frac{\sum (R2...R8)}{SUMR})</td>
<td>V33</td>
<td>V43 + ((V20 - V43) \times 10/23)</td>
</tr>
<tr>
<td>V2</td>
<td>(V8 + (V1 - V8) \times IPV2)</td>
<td>V34</td>
<td>V43 + ((V20 - V43) \times 9/23)</td>
</tr>
<tr>
<td>V3</td>
<td>(V8 + (V1 - V8) \times IPV3)</td>
<td>V35</td>
<td>V43 + ((V20 - V43) \times 8/23)</td>
</tr>
<tr>
<td>V4</td>
<td>(V8 + (V1 - V8) \times IPV4)</td>
<td>V36</td>
<td>V43 + ((V20 - V43) \times 7/23)</td>
</tr>
<tr>
<td>V5</td>
<td>(V8 + (V1 - V8) \times IPV5)</td>
<td>V37</td>
<td>V43 + ((V20 - V43) \times 6/23)</td>
</tr>
<tr>
<td>V6</td>
<td>(V8 + (V1 - V8) \times IPV6)</td>
<td>V38</td>
<td>V43 + ((V20 - V43) \times 5/23)</td>
</tr>
<tr>
<td>V7</td>
<td>(V8 + (V1 - V8) \times IPV7)</td>
<td>V39</td>
<td>V43 + ((V20 - V43) \times 4/23)</td>
</tr>
<tr>
<td>V8</td>
<td>(\Delta V \times \frac{\sum (R3...R8)}{SUMR})</td>
<td>V40</td>
<td>V43 + ((V20 - V43) \times 3/23)</td>
</tr>
<tr>
<td>V9</td>
<td>(V20 + (V8 - V20) \times 11/12)</td>
<td>V41</td>
<td>V43 + ((V20 - V43) \times 2/23)</td>
</tr>
<tr>
<td>V10</td>
<td>(V20 + (V8 - V20) \times 10/12)</td>
<td>V42</td>
<td>V43 + ((V20 - V43) \times 1/23)</td>
</tr>
<tr>
<td>V11</td>
<td>(V20 + (V8 - V20) \times 9/12)</td>
<td>V43</td>
<td>(\Delta V \times \frac{\sum (R5...R8)}{SUMR})</td>
</tr>
<tr>
<td>V12</td>
<td>(V20 + (V8 - V20) \times 8/12)</td>
<td>V44</td>
<td>V55 + ((V43 - V55) \times 11/12)</td>
</tr>
<tr>
<td>V13</td>
<td>(V20 + (V8 - V20) \times 7/12)</td>
<td>V45</td>
<td>V55 + ((V43 - V55) \times 10/12)</td>
</tr>
<tr>
<td>V14</td>
<td>(V20 + (V8 - V20) \times 6/12)</td>
<td>V46</td>
<td>V55 + ((V43 - V55) \times 9/12)</td>
</tr>
<tr>
<td>V15</td>
<td>(V20 + (V8 - V20) \times 5/12)</td>
<td>V47</td>
<td>V55 + ((V43 - V55) \times 8/12)</td>
</tr>
<tr>
<td>V16</td>
<td>(V20 + (V8 - V20) \times 4/12)</td>
<td>V48</td>
<td>V55 + ((V43 - V55) \times 7/12)</td>
</tr>
<tr>
<td>V17</td>
<td>(V20 + (V8 - V20) \times 3/12)</td>
<td>V49</td>
<td>V55 + ((V43 - V55) \times 6/12)</td>
</tr>
<tr>
<td>V18</td>
<td>(V20 + (V8 - V20) \times 2/12)</td>
<td>V50</td>
<td>V55 + ((V43 - V55) \times 5/12)</td>
</tr>
<tr>
<td>V19</td>
<td>(V20 + (V8 - V20) \times 1/12)</td>
<td>V51</td>
<td>V55 + ((V43 - V55) \times 4/12)</td>
</tr>
<tr>
<td>V20</td>
<td>(\Delta V \times \frac{\sum (R4...R8)}{SUMR})</td>
<td>V52</td>
<td>V55 + ((V43 - V55) \times 3/12)</td>
</tr>
<tr>
<td>V21</td>
<td>(V43 + (V20 - V43) \times 22/23)</td>
<td>V53</td>
<td>V55 + ((V43 - V55) \times 2/12)</td>
</tr>
<tr>
<td>V22</td>
<td>(V43 + (V20 - V43) \times 21/23)</td>
<td>V54</td>
<td>V55 + ((V43 - V55) \times 1/12)</td>
</tr>
<tr>
<td>V23</td>
<td>(V43 + (V20 - V43) \times 20/23)</td>
<td>V55</td>
<td>(\Delta V \times \frac{\sum (R6...R8)}{SUMR})</td>
</tr>
<tr>
<td>V24</td>
<td>(V43 + (V20 - V43) \times 19/23)</td>
<td>V56</td>
<td>V62 + ((V55 - V62) \times IPV56)</td>
</tr>
<tr>
<td>V25</td>
<td>(V43 + (V20 - V43) \times 18/23)</td>
<td>V57</td>
<td>V62 + ((V55 - V62) \times IPV57)</td>
</tr>
<tr>
<td>V26</td>
<td>(V43 + (V20 - V43) \times 17/23)</td>
<td>V58</td>
<td>V62 + ((V55 - V62) \times IPV58)</td>
</tr>
<tr>
<td>V27</td>
<td>(V43 + (V20 - V43) \times 16/23)</td>
<td>V59</td>
<td>V62 + ((V55 - V62) \times IPV59)</td>
</tr>
<tr>
<td>V28</td>
<td>(V43 + (V20 - V43) \times 15/23)</td>
<td>V60</td>
<td>V62 + ((V55 - V62) \times IPV60)</td>
</tr>
<tr>
<td>V29</td>
<td>(V43 + (V20 - V43) \times 14/23)</td>
<td>V61</td>
<td>V62 + ((V55 - V62) \times IPV61)</td>
</tr>
<tr>
<td>V30</td>
<td>(V43 + (V20 - V43) \times 13/23)</td>
<td>V62</td>
<td>(\Delta V \times (R7 + R8) / SUMR)</td>
</tr>
<tr>
<td>V31</td>
<td>(V43 + (V20 - V43) \times 12/23)</td>
<td>V63</td>
<td>(\Delta V \times R8 / SUMR)</td>
</tr>
</tbody>
</table>

Note:  
\(\Delta V = GVDD - GND\) when calculating positive grayscale voltage  
\(\Delta V = GVCL - GND\) when calculating negative grayscale voltage  

\(SUMR = \sum (R0...R8) \geq 70R\)
### Table 17 Grayscale Voltage Calculation Formula

3. Display RAM Data and the Grayscale Voltage

<table>
<thead>
<tr>
<th>Frame Memory Data</th>
<th>Grayscale Voltage</th>
<th>Frame Memory Data</th>
<th>Grayscale Voltage</th>
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<tbody>
<tr>
<td></td>
<td>REV = 1</td>
<td>REV = 0</td>
<td>REV = 1</td>
</tr>
<tr>
<td>Positive Polarity</td>
<td>Negative Polarity</td>
<td>Positive Polarity</td>
<td>Negative Polarity</td>
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<tr>
<td>00h</td>
<td>V0 V63 V63 V0</td>
<td>20h</td>
<td>V32 V31 V31 V32</td>
</tr>
<tr>
<td>01h</td>
<td>V1 V62 V62 V1</td>
<td>21h</td>
<td>V33 V30 V30 V33</td>
</tr>
<tr>
<td>02h</td>
<td>V2 V61 V61 V2</td>
<td>22h</td>
<td>V34 V29 V29 V34</td>
</tr>
<tr>
<td>03h</td>
<td>V3 V60 V60 V3</td>
<td>23h</td>
<td>V35 V28 V28 V35</td>
</tr>
<tr>
<td>04h</td>
<td>V4 V59 V59 V4</td>
<td>24h</td>
<td>V36 V27 V27 V36</td>
</tr>
<tr>
<td>05h</td>
<td>V5 V58 V58 V5</td>
<td>25h</td>
<td>V37 V26 V26 V37</td>
</tr>
<tr>
<td>06h</td>
<td>V6 V57 V57 V6</td>
<td>26h</td>
<td>V38 V25 V25 V38</td>
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<tr>
<td>07h</td>
<td>V7 V56 V56 V7</td>
<td>27h</td>
<td>V39 V24 V24 V39</td>
</tr>
<tr>
<td>08h</td>
<td>V8 V55 V55 V8</td>
<td>28h</td>
<td>V40 V23 V23 V40</td>
</tr>
<tr>
<td>09h</td>
<td>V9 V54 V54 V9</td>
<td>29h</td>
<td>V41 V22 V22 V41</td>
</tr>
<tr>
<td>0Ah</td>
<td>V10 V53 V53 V10</td>
<td>2Ah</td>
<td>V42 V21 V21 V42</td>
</tr>
<tr>
<td>0Bh</td>
<td>V11 V52 V52 V11</td>
<td>2Bh</td>
<td>V43 V20 V20 V43</td>
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<tr>
<td>0Ch</td>
<td>V12 V51 V51 V12</td>
<td>2Ch</td>
<td>V44 V19 V19 V44</td>
</tr>
<tr>
<td>0Dh</td>
<td>V13 V50 V50 V13</td>
<td>2Dh</td>
<td>V45 V18 V18 V45</td>
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<tr>
<td>0 Eh</td>
<td>V14 V49 V49 V14</td>
<td>2 Eh</td>
<td>V46 V17 V17 V46</td>
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<tr>
<td>0Fh</td>
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<td>V47 V16 V16 V47</td>
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<td>10h</td>
<td>V16 V47 V47 V16</td>
<td>30h</td>
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<td>33h</td>
<td>V51 V12 V12 V51</td>
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<td>14h</td>
<td>V20 V43 V43 V20</td>
<td>34h</td>
<td>V52 V11 V11 V52</td>
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<td>15h</td>
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<td>35h</td>
<td>V53 V10 V10 V53</td>
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<td>V24 V39 V39 V24</td>
<td>38h</td>
<td>V56 V7 V7 V56</td>
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<td>19h</td>
<td>V25 V38 V38 V25</td>
<td>39h</td>
<td>V57 V6 V6 V57</td>
</tr>
<tr>
<td>1Ah</td>
<td>V26 V37 V37 V26</td>
<td>3Ah</td>
<td>V58 V5 V5 V58</td>
</tr>
<tr>
<td>1Bh</td>
<td>V27</td>
<td>V36</td>
<td>V36</td>
</tr>
<tr>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
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<td>V28</td>
<td>V35</td>
<td>V35</td>
</tr>
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<td>V33</td>
</tr>
<tr>
<td>1Fh</td>
<td>V31</td>
<td>V32</td>
<td>V32</td>
</tr>
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</table>

Table 18 Mapping of Frame Memory Data and Grayscale Voltage
18.1. Configuration of Power Supply Circuit

Figure 52 Power Supply Circuit Connection
18.2.. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ST7793 are as follows.

Figure 53 Power Booster Level
18.3. Applied Voltage to the TFT panel

![Diagram showing Voltage Output to TFT LCD Panel]

Figure 54 Voltage Output to TFT LCD Panel

18.4. Power Supply Configuration

When supplying and cutting off power, the sequences below must be followed.

**Power On Sequence**

1. **Power Supply on Sequence**
   - VDD, VDDA, VDDI
   - VDD, VDDA, VDDI or VDD, VDDI, VDDA simultaneously

2. **Power Stabilization**

3. **Reset Procedure & NVM Auto-load**

4. **Reset**

5. **State**
   - Liquid Crystal Power Supply Off
   - Display Off

6. **User Setting**
   - F4000/tc
   - F008/tc
   - F0801/F089/tc
   - NL[55:0]
   - BF[70:0], FR[70:0]
   - Gamma+Control

7. **Turn On Internal Power Supply**
   - PSON=1, PON=1

8. **Other Setting & Frame Data**
   - Initialize
   - 1. Other mode setting instructions
   - 2. RAM write operation
   - 3. etc.

9. **State**
   - Liquid Crystal Power Supply On
   - Display Off

10. **Display On Sequence**

![Diagram showing Power Supply On Sequence]

Figure 55 Power Supply On Sequence
Power Off Sequence

- **State**: Liquid Crystal Power Supply On
  Display Off

- **Turn Off Internal Power Supply**
  R102h: \( PSON=0, PON=0 \)

- **State**: Liquid Crystal Power Supply Off
  Display Off

- **Power Supply Off Sequence**
  - VDDI
  - VDD, VDDA
  - VDDI \( \rightarrow \) VDD, VDDA
  - VDDA, VDDI, VDD Simultaneously
  - GND

Figure 56 Power Supply Off Sequence
18.5. Display On/Off Sequences

To switch between display-on and display-off mode, follow the sequences below.

**Display On Sequence**

| State                      | Liquid Crystal Power Supply On
|                           | Display Off
|                           | Display On
| R007h: BASEE=1             |
| State                      | Liquid Crystal Power Supply On
|                           | Display On

**Display Off Sequence**

| State                      | Liquid Crystal Power Supply On
|                           | Display Off
|                           | Display On
| R007h: BASEE=0             |
| State                      | Liquid Crystal Power Supply On
|                           | Display On

Figure 57 Display On/Off Sequences

18.6. Refresh Sequences

To reduce malfunction caused by noise, execute refresh sequence 1 regularly. To exit shutdown mode, execute refresh sequence 2.

**Refresh Sequence 1**

1. Test Register Initialization
   - R000h: TRSP=1

2. NVM Data load
   - R000h: CALD=1

3. > 0.3ms NVM Data Load
   - R000h: TRSP=0

4. Initial Setting & User Setting

**Refresh Sequence 2**

1. Test Register Initialization
   - R000h: TRSP=1

2. > 0.1ms

3. R000h: TRSP=0

4. Initial Setting & User Setting

Figure 58 Refresh Sequences
18.7. Shutdown Mode Sequences

Shutdown mode can be used to save power when display function is not required. To enter or exit from shutdown mode, refer to the following sequence.

**Enter and Exit Shutdown Mode Sequence**

- **State**: Liquid Crystal Power Supply On, Display Off
  - LCD Power Supply Off
  - R102h: PSON=0, PON=0
  - >5 frames
  - Set Shutdown Mode
  - R100h: DSTB=1
  - Transfer Synchronization
  - Write 00h with RS=0 for 4 times
  - >0.3 ms (Required for 8-9-bit interface only)
  - Refresh Sequence 2
  - LCD Power Supply On
  - R102h: PSON=1, PON=1
  - >6 frames
  - RAM Data Setting
  - Display On Sequence
  - State
  - Liquid Crystal Power Supply Off, Display Off

Note: The CSX pulse and write-cycle must meet the AC timing specification.

Figure 59 Shutdown Mode Enter/Exit Sequences
## REVISION HISTORY

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<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
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<td>2010/11/11</td>
<td>Draft</td>
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<td>V0.1</td>
<td>2011/11</td>
<td>Modified scan mode block / function default value</td>
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<td>Addition 709h &amp; 752h Command</td>
</tr>
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<td>Addition 754 Gate turn on Timing control</td>
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<td>Modify the Au bump height to 9um</td>
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<td>Modify the VGL Voltage</td>
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<td>Modify Register 708h &amp; 280h</td>
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<td>Modify the TSCL timing for SPI interface</td>
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<tr>
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<td>Modify Chip thickness</td>
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With collaboration of https://www.displayfuture.com