Sitronix

ST7571

4 Gray Scale Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7571 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI), IIC or 8-bit parallel display data and stores in an on-chip display data RAM of 128 x 129 x 2 bits. It performs display data RAM write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM and FRC Methods

DDRAM data [2n : 2n+1]		Gray Scale
2n	2n + 1	
0	0	White
0	1	Light gray
1	0	Dark gray
1	1	Black

(Accessible column address, n = 0, 1, 2, ……, 125, 126, 127)

Driver Output Circuits

128 segment outputs / 128+1 common outputs

Applicable Duty Ratios

– Various partial display

– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 128 × 129 × 2= 33,024 bits

Microprocessor Interface

– 8-bit parallel interface with 6800-series or 8080-series

– 4-line serial interface (4-line-SPI)

– 3-line serial interface (3-line 8 bits SPI)

– IIC serial interface

On-chip Low Power Analog Circuit

– On-chip oscillator circuit

– Build-in Voltage converter (x8)

– Voltage regulator (temperature coefficient: -0.13%/°C)

– On-chip electronic contrast control function

(64 steps x 8)

– Voltage follower (LCD bias : 1/5 to 1/12)

Operating Voltage Range

– Supply voltage (VDD1): 1.8 to 3.3V

– Supply voltage (VDD2): 2.4 to 3.3V

Package Type

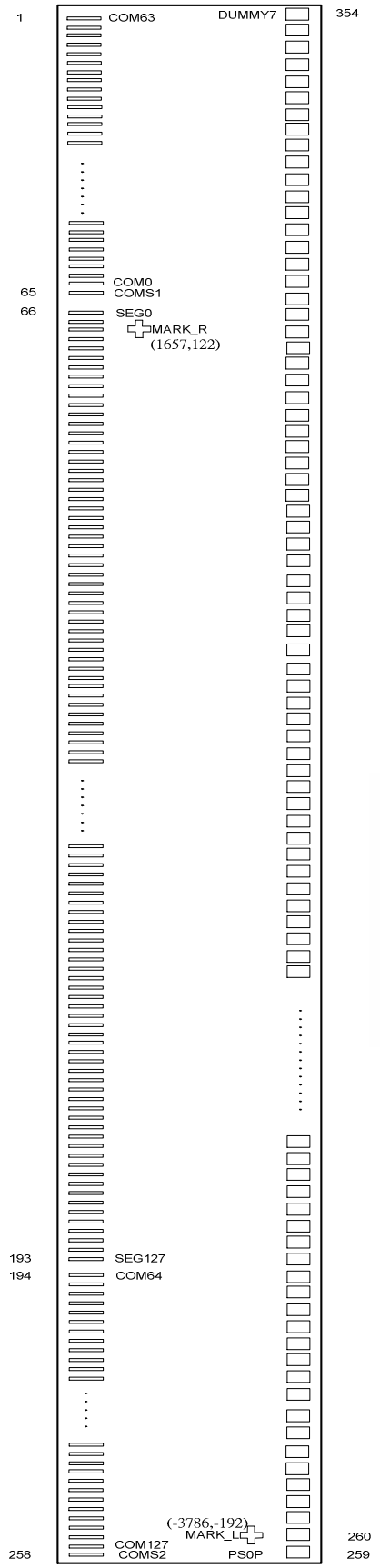
– Application for COG

LCD Driving Voltage(EEPROM)

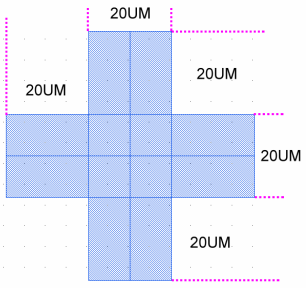
– To store contrast adjustment value for best display

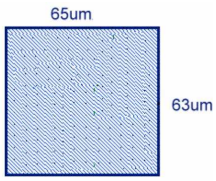
ST7571	**6800 , 8080 , 4-Line , 3-Line interface (without IIC interface)**	ST
ST7571i	**IIC interface**	I²C BUS

3. ST7571 Pad Arrangement (COG)



- **Chip Size：7956um X 780um**
- **Bump Pitch：**
  - **I/O PAD：80um**
  - **COM PAD：33um**
  - **SEG PAD： 27um**
- **Bump Size：**
  - **I/O PAD：65um X 63 um**
  - **COM/SEG PAD：14um X 128um**
- **Bump Height：15um**
- **Chip Thickness: 300 um**





I/O Pad

COM/SEG Pad

Fig. 1 ST7571 pad arrangement diagram

4. Pad Center Coordinates

PAD No.	Pin Name		X	Y
	CSEL=L	CSEL=H		
1	COM[63]	COM[126]	3896.50	283.00
2	COM[62]	COM[124]	3863.50	283.00
3	COM[61]	COM[122]	3830.50	283.00
4	COM[60]	COM[120]	3797.50	283.00
5	COM[59]	COM[118]	3764.50	283.00
6	COM[58]	COM[116]	3731.50	283.00
7	COM[57]	COM[114]	3698.50	283.00
8	COM[56]	COM[112]	3665.50	283.00
9	COM[55]	COM[110]	3632.50	283.00
10	COM[54]	COM[108]	3599.50	283.00
11	COM[53]	COM[106]	3566.50	283.00
12	COM[52]	COM[104]	3533.50	283.00
13	COM[51]	COM[102]	3500.50	283.00
14	COM[50]	COM[100]	3467.50	283.00
15	COM[49]	COM[98]	3434.50	283.00
16	COM[48]	COM[96]	3401.50	283.00
17	COM[47]	COM[94]	3368.50	283.00
18	COM[46]	COM[92]	3335.50	283.00
19	COM[45]	COM[90]	3302.50	283.00
20	COM[44]	COM[88]	3269.50	283.00
21	COM[43]	COM[86]	3236.50	283.00
22	COM[42]	COM[84]	3203.50	283.00
23	COM[41]	COM[82]	3170.50	283.00
24	COM[40]	COM[80]	3137.50	283.00
25	COM[39]	COM[78]	3104.50	283.00
26	COM[38]	COM[76]	3071.50	283.00
27	COM[37]	COM[74]	3038.50	283.00
28	COM[36]	COM[72]	3005.50	283.00
29	COM[35]	COM[70]	2972.50	283.00
30	COM[34]	COM[68]	2939.50	283.00
31	COM[33]	COM[66]	2906.50	283.00
32	COM[32]	COM[64]	2873.50	283.00
33	COM[31]	COM[62]	2840.50	283.00
34	COM[30]	COM[60]	2807.50	283.00
35	COM[29]	COM[58]	2774.50	283.00

PAD No.	Pin Name		X	Y
	CSEL=L	CSEL=H		
36	COM[28]	COM[56]	2741.50	283.00
37	COM[27]	COM[54]	2708.50	283.00
38	COM[26]	COM[52]	2675.50	283.00
39	COM[25]	COM[50]	2642.50	283.00
40	COM[24]	COM[48]	2609.50	283.00
41	COM[23]	COM[46]	2576.50	283.00
42	COM[22]	COM[44]	2543.50	283.00
43	COM[21]	COM[42]	2510.50	283.00
44	COM[20]	COM[40]	2477.50	283.00
45	COM[19]	COM[38]	2444.50	283.00
46	COM[18]	COM[36]	2411.50	283.00
47	COM[17]	COM[34]	2378.50	283.00
48	COM[16]	COM[32]	2345.50	283.00
49	COM[15]	COM[30]	2312.50	283.00
50	COM[14]	COM[28]	2279.50	283.00
51	COM[13]	COM[26]	2246.50	283.00
52	COM[12]	COM[24]	2213.50	283.00
53	COM[11]	COM[22]	2180.50	283.00
54	COM[10]	COM[20]	2147.50	283.00
55	COM[9]	COM[18]	2114.50	283.00
56	COM[8]	COM[16]	2081.50	283.00
57	COM[7]	COM[14]	2048.50	283.00
58	COM[6]	COM[12]	2015.50	283.00
59	COM[5]	COM[10]	1982.50	283.00
60	COM[4]	COM[8]	1949.50	283.00
61	COM[3]	COM[6]	1916.50	283.00
62	COM[2]	COM[4]	1883.50	283.00
63	COM[1]	COM[2]	1850.50	283.00
64	COM[0]	COM[0]	1817.50	283.00
65	COMS1		1784.50	283.00
66	SEG[0]		1714.50	283.00
67	SEG[1]		1687.50	283.00
68	SEG[2]		1660.50	283.00
69	SEG[3]		1633.50	283.00
70	SEG[4]		1606.50	283.00

PAD No.	Pin Name	X	Y
71	SEG[5]	1579.50	283.00
72	SEG[6]	1552.50	283.00
73	SEG[7]	1525.50	283.00
74	SEG[8]	1498.50	283.00
75	SEG[9]	1471.50	283.00
76	SEG[10]	1444.50	283.00
77	SEG[11]	1417.50	283.00
78	SEG[12]	1390.50	283.00
79	SEG[13]	1363.50	283.00
80	SEG[14]	1336.50	283.00
81	SEG[15]	1309.50	283.00
82	SEG[16]	1282.50	283.00
83	SEG[17]	1255.50	283.00
84	SEG[18]	1228.50	283.00
85	SEG[19]	1201.50	283.00
86	SEG[20]	1174.50	283.00
87	SEG[21]	1147.50	283.00
88	SEG[22]	1120.50	283.00
89	SEG[23]	1093.50	283.00
90	SEG[24]	1066.50	283.00
91	SEG[25]	1039.50	283.00
92	SEG[26]	1012.50	283.00
93	SEG[27]	985.50	283.00
94	SEG[28]	958.50	283.00
95	SEG[29]	931.50	283.00
96	SEG[30]	904.50	283.00
97	SEG[31]	877.50	283.00
98	SEG[32]	850.50	283.00
99	SEG[33]	823.50	283.00
100	SEG[34]	796.50	283.00
101	SEG[35]	769.50	283.00
102	SEG[36]	742.50	283.00
103	SEG[37]	715.50	283.00
104	SEG[38]	688.50	283.00
105	SEG[39]	661.50	283.00

PAD No.	Pin Name	X	Y
106	SEG[40]	634.50	283.00
107	SEG[41]	607.50	283.00
108	SEG[42]	580.50	283.00
109	SEG[43]	553.50	283.00
110	SEG[44]	526.50	283.00
111	SEG[45]	499.50	283.00
112	SEG[46]	472.50	283.00
113	SEG[47]	445.50	283.00
114	SEG[48]	418.50	283.00
115	SEG[49]	391.50	283.00
116	SEG[50]	364.50	283.00
117	SEG[51]	337.50	283.00
118	SEG[52]	310.50	283.00
119	SEG[53]	283.50	283.00
120	SEG[54]	256.50	283.00
121	SEG[55]	229.50	283.00
122	SEG[56]	202.50	283.00
123	SEG[57]	175.50	283.00
124	SEG[58]	148.50	283.00
125	SEG[59]	121.50	283.00
126	SEG[60]	94.50	283.00
127	SEG[61]	67.50	283.00
128	SEG[62]	40.50	283.00
129	SEG[63]	13.50	283.00
130	SEG[64]	-13.50	283.00
131	SEG[65]	-40.50	283.00
132	SEG[66]	-67.50	283.00
133	SEG[67]	-94.50	283.00
134	SEG[68]	-121.50	283.00
135	SEG[69]	-148.50	283.00
136	SEG[70]	-175.50	283.00
137	SEG[71]	-202.50	283.00
138	SEG[72]	-229.50	283.00
139	SEG[73]	-256.50	283.00
140	SEG[74]	-283.50	283.00

PAD No.	Pin Name	X	Y
141	SEG[75]	-310.50	283.00
142	SEG[76]	-337.50	283.00
143	SEG[77]	-364.50	283.00
144	SEG[78]	-391.50	283.00
145	SEG[79]	-418.50	283.00
146	SEG[80]	-445.50	283.00
147	SEG[81]	-472.50	283.00
148	SEG[82]	-499.50	283.00
149	SEG[83]	-526.50	283.00
150	SEG[84]	-553.50	283.00
151	SEG[85]	-580.50	283.00
152	SEG[86]	-607.50	283.00
153	SEG[87]	-634.50	283.00
154	SEG[88]	-661.50	283.00
155	SEG[89]	-688.50	283.00
156	SEG[90]	-715.50	283.00
157	SEG[91]	-742.50	283.00
158	SEG[92]	-769.50	283.00
159	SEG[93]	-796.50	283.00
160	SEG[94]	-823.50	283.00
161	SEG[95]	-850.50	283.00
162	SEG[96]	-877.50	283.00
163	SEG[97]	-904.50	283.00
164	SEG[98]	-931.50	283.00
165	SEG[99]	-958.50	283.00
166	SEG[100]	-985.50	283.00
167	SEG[101]	-1012.50	283.00
168	SEG[102]	-1039.50	283.00
169	SEG[103]	-1066.50	283.00
170	SEG[104]	-1093.50	283.00
171	SEG[105]	-1120.50	283.00
172	SEG[106]	-1147.50	283.00
173	SEG[107]	-1174.50	283.00
174	SEG[108]	-1201.50	283.00
175	SEG[109]	-1228.50	283.00

PAD No.	Pin Name		X	Y
176	SEG[110]		-1255.50	283.00
177	SEG[111]		-1282.50	283.00
178	SEG[112]		-1309.50	283.00
179	SEG[113]		-1336.50	283.00
180	SEG[114]		-1363.50	283.00
181	SEG[115]		-1390.50	283.00
182	SEG[116]		-1417.50	283.00
183	SEG[117]		-1444.50	283.00
184	SEG[118]		-1471.50	283.00
185	SEG[119]		-1498.50	283.00
186	SEG[120]		-1525.50	283.00
187	SEG[121]		-1552.50	283.00
188	SEG[122]		-1579.50	283.00
189	SEG[123]		-1606.50	283.00
190	SEG[124]		-1633.50	283.00
191	SEG[125]		-1660.50	283.00
192	SEG[126]		-1687.50	283.00
193	SEG[127]		-1714.50	283.00
194	COM[64]	COM[1]	-1784.50	283.00
195	COM[65]	COM[3]	-1817.50	283.00
196	COM[66]	COM[5]	-1850.50	283.00
197	COM[67]	COM[7]	-1883.50	283.00
198	COM[68]	COM[9]	-1916.50	283.00
199	COM[69]	COM[11]	-1949.50	283.00
200	COM[70]	COM[13]	-1982.50	283.00
201	COM[71]	COM[15]	-2015.50	283.00
202	COM[72]	COM[17]	-2048.50	283.00
203	COM[73]	COM[19]	-2081.50	283.00
204	COM[74]	COM[21]	-2114.50	283.00
205	COM[75]	COM[23]	-2147.50	283.00
206	COM[76]	COM[25]	-2180.50	283.00
207	COM[77]	COM[27]	-2213.50	283.00
208	COM[78]	COM[29]	-2246.50	283.00
209	COM[79]	COM[31]	-2279.50	283.00
210	COM[80]	COM[33]	-2312.50	283.00

PAD No.	Pin Name		X	Y
	CSEL=L	CSEL=H		
211	COM[81]	COM[35]	-2345.50	283.00
212	COM[82]	COM[37]	-2378.50	283.00
213	COM[83]	COM[39]	-2411.50	283.00
214	COM[84]	COM[41]	-2444.50	283.00
215	COM[85]	COM[43]	-2477.50	283.00
216	COM[86]	COM[45]	-2510.50	283.00
217	COM[87]	COM[47]	-2543.50	283.00
218	COM[88]	COM[49]	-2576.50	283.00
219	COM[89]	COM[51]	-2609.50	283.00
220	COM[90]	COM[53]	-2642.50	283.00
221	COM[91]	COM[55]	-2675.50	283.00
222	COM[92]	COM[57]	-2708.50	283.00
223	COM[93]	COM[59]	-2741.50	283.00
224	COM[94]	COM[61]	-2774.50	283.00
225	COM[95]	COM[63]	-2807.50	283.00
226	COM[96]	COM[65]	-2840.50	283.00
227	COM[97]	COM[67]	-2873.50	283.00
228	COM[98]	COM[69]	-2906.50	283.00
229	COM[99]	COM[71]	-2939.50	283.00
230	COM[100]	COM[73]	-2972.50	283.00
231	COM[101]	COM[75]	-3005.50	283.00
232	COM[102]	COM[77]	-3038.50	283.00
233	COM[103]	COM[79]	-3071.50	283.00
234	COM[104]	COM[81]	-3104.50	283.00
235	COM[105]	COM[83]	-3137.50	283.00
236	COM[106]	COM[85]	-3170.50	283.00
237	COM[107]	COM[87]	-3203.50	283.00
238	COM[108]	COM[89]	-3236.50	283.00
239	COM[109]	COM[91]	-3269.50	283.00
240	COM[110]	COM[93]	-3302.50	283.00
241	COM[111]	COM[95]	-3335.50	283.00
242	COM[112]	COM[97]	-3368.50	283.00
243	COM[113]	COM[99]	-3401.50	283.00
244	COM[114]	COM[101]	-3434.50	283.00
245	COM[115]	COM[103]	-3467.50	283.00

PAD No.	Pin Name		X	Y
	CSEL=L	CSEL=H		
246	COM[116]	COM[105]	-3500.50	283.00
247	COM[117]	COM[107]	-3533.50	283.00
248	COM[118]	COM[109]	-3566.50	283.00
249	COM[119]	COM[111]	-3599.50	283.00
250	COM[120]	COM[113]	-3632.50	283.00
251	COM[121]	COM[115]	-3665.50	283.00
252	COM[122]	COM[117]	-3698.50	283.00
253	COM[123]	COM[119]	-3731.50	283.00
254	COM[124]	COM[121]	-3764.50	283.00
255	COM[125]	COM[123]	-3797.50	283.00
256	COM[126]	COM[125]	-3830.50	283.00
257	COM[127]	COM[127]	-3863.50	283.00
258	COMS2		-3896.50	283.00
259	PS0		-3858.00	-315.50
260	VSS1		-3778.00	-315.50
261	PS1		-3698.00	-315.50
262	VDD1		-3618.00	-315.50
263	PS2		-3538.00	-315.50
264	VSS1		-3458.00	-315.50
265	CSB		-3378.00	-315.50
266	RST		-3298.00	-315.50
267	A0		-3218.00	-315.50
268	EWR		-3138.00	-315.50
269	ERD		-3058.00	-315.50
270	D0		-2978.00	-315.50
271	D1		-2898.00	-315.50
272	D2		-2818.00	-315.50
273	D3		-2738.00	-315.50
274	D4		-2658.00	-315.50
275	D5		-2578.00	-315.50
276	D6		-2498.00	-315.50
277	D7		-2418.00	-315.50
278	RST		-2338.00	-315.50
279	CSB		-2258.00	-315.50
280	VDD1		-2178.00	-315.50

PAD No.	Pin Name	X	Y
281	VDD1	-2098.00	-315.50
282	VDD1	-2018.00	-315.50
283	VDD2	-1938.00	-315.50
284	VDD2	-1858.00	-315.50
285	VDD2	-1778.00	-315.50
286	VDD2	-1698.00	-315.50
287	VDD3	-1618.00	-315.50
288	VDD3	-1538.00	-315.50
289	VSS3	-1458.00	-315.50
290	VSS3	-1378.00	-315.50
291	VSS2	-1298.00	-315.50
292	VSS2	-1218.00	-315.50
293	VSS2	-1138.00	-315.50
294	VSS2	-1058.00	-315.50
295	VSS1	-978.00	-315.50
296	VSS1	-898.00	-315.50
297	VSS1	-818.00	-315.50
298	VSS1	-738.00	-315.50
299	VDD2	-658.00	-315.50
300	VDD2	-578.00	-315.50
301	VDD2	-498.00	-315.50
302	VDD2	-418.00	-315.50
303	VDD3	-338.00	-315.50
304	VDD3	-258.00	-315.50
305	MF2	-178.00	-315.50
306	MF1	-98.00	-315.50
307	MF0	-18.00	-315.50
308	DS0	62.00	-315.50
309	DS1	142.00	-315.50
310	VMO	222.00	-315.50
311	VMO	302.00	-315.50
312	VMO	382.00	-315.50
313	VSS2	462.00	-315.50
314	V0I	542.00	-315.50
315	V0I	622.00	-315.50

PAD No.	Pin Name	X	Y
316	V0I	702.00	-315.50
317	V0I	782.00	-315.50
318	V0S	862.00	-315.50
319	V0O	942.00	-315.50
320	V0O	1022.00	-315.50
321	XV0O	1102.00	-315.50
322	XV0O	1182.00	-315.50
323	XV0S	1262.00	-315.50
324	XV0I	1385.00	-315.50
325	XV0I	1465.00	-315.50
326	XV0I	1545.00	-315.50
327	XV0I	1625.00	-315.50
328	VDD1	1705.00	-315.50
329	VEXT	1785.00	-315.50
330	OSC1	1865.00	-315.50
331	DCPS	1945.00	-315.50
332	VSS1	2025.00	-315.50
333	CSEL	2105.00	-315.50
334	VD1I	2185.00	-315.50
335	VD1I	2265.00	-315.50
336	VD1O	2345.00	-315.50
337	VGO	2425.00	-315.50
338	VGO	2505.00	-315.50
339	VGS	2585.00	-315.50
340	VGI	2665.00	-315.50
341	VGI	2745.00	-315.50
342	VGI	2825.00	-315.50
343	VGI	2905.00	-315.50
344	VPP	2985.00	-315.50
345	VPP	3065.00	-315.50
346	VPP	3145.00	-315.50
347	VE	3225.00	-315.50
348	DUMMY1	3341.00	-315.50
349	DUMMY2	3421.00	-315.50
350	DUMMY3	3501.00	-315.50

PAD No.	Pin Name	X	Y
351	DUMMY4	3581.00	-315.50
352	DUMMY5	3661.00	-315.50
353	DUMMY6	3741.00	-315.50
354	DUMMY7	3821.00	-315.50

5.BLOCK DIAGRAM

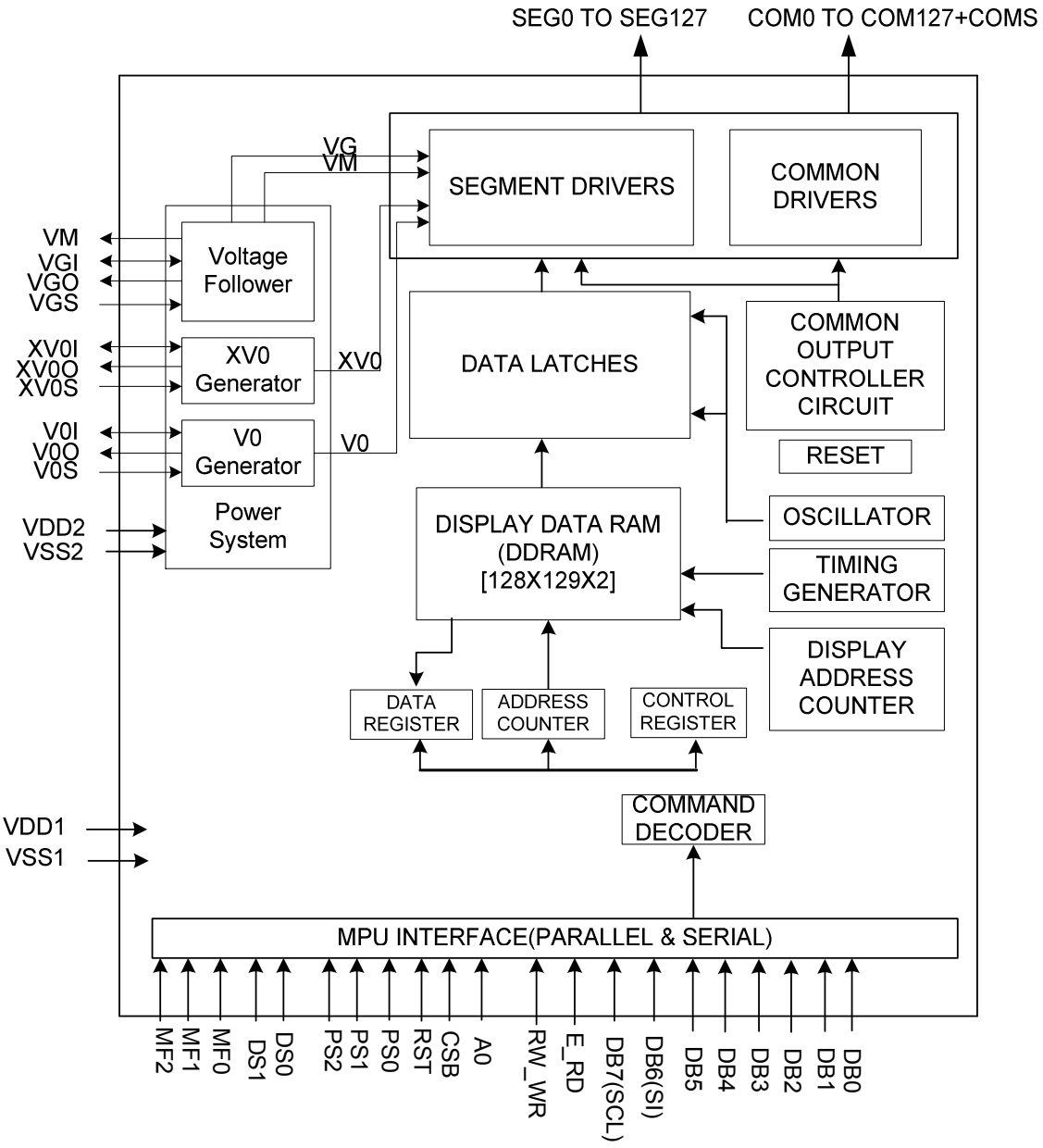


Fig.2 Block diagram

6. PIN DESCRIPTION

6.1 POWER SUPPLY

Power Supply Pin Description

Name	I/O	Description
VDD1	Power	Power supply for digital circuit
VDD2	Power	Power supply for analog circuit(booster)
VDD3	Power	Power supply for analog circuit(regulator)
VSS1	Power	Ground for digital circuit
VSS2	Power	Ground for analog circuit(booster)
VSS3	Power	Ground for analog circuit(regulator)

6.2 LCD DRIVER SUPPLY

LCD Driver Supply Pin Description

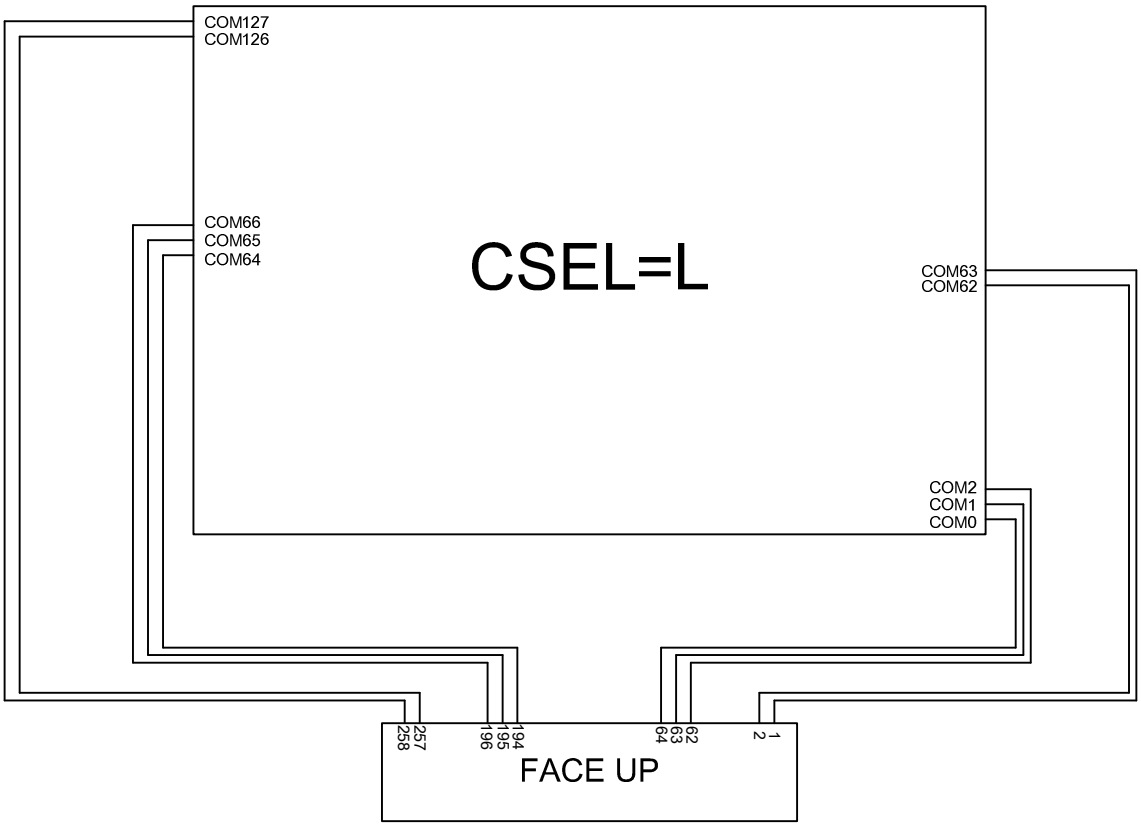
<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>V0O
V0I
V0S</td><td>I/O</td><td>Positive LCD driver supply voltages.
$V0_{OUT}$ is the output voltage of V0 generated by ST7571
$V0_{IN}$ is the input pin of power supply to generate V0 voltage for LCD.
$V0_S$ is the input pin of power supply to sense the V0 voltage.
$V0_{OUT}$, $V0_{IN}$, $V0_S$ should be connected together by FPC.</td></tr>
<tr><td>XV0O
XV0I
XV0S</td><td>I/O</td><td>Negative LCD driver supply voltages.
$XV0_{OUT}$ is the output voltage of XV0 generated by ST7571.
$XV0_{IN}$ is the input pin of power supply to generate XV0 voltage for LCD.
$XV0_S$ is the input pin of power supply to sense the XV0 voltage.
$XV0_{OUT}$, $XV0_{IN}$, $XV0_S$ should be connected together by FPC.</td></tr>
<tr><td>VGO
VGI
VGS
VMO</td><td>I/O</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. VG,VM need the capacitor between with VSS
Voltages should have the following relationship;
V0 ≧ Vg ≧ Vm ≧ VSS ≧ XV0
0.7V< Vm< VDD2-0.7V and 1.8V < Vg < VDD2.
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><td>LCD bias</td><td>VG</td><td>VM</td></tr>
<tr><td>1/N bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
NOTE: N = 5 to 12</td></tr>
</table>

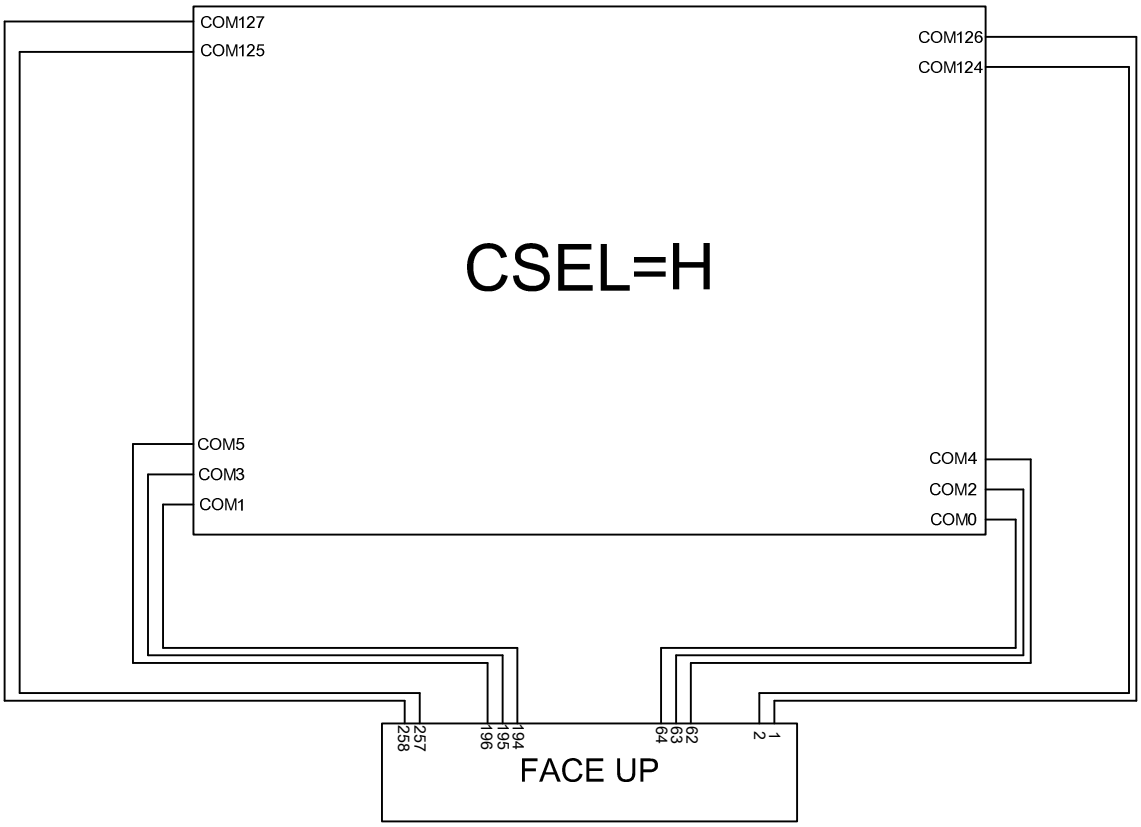
6.3 SYSTEM CONTROL

System Control Pin Description

Name	I/O	Description
VEXT	O	For testing, must set with floating.
OSC1	I	Connect OSC1 to VDD1.
DCPS	I	Digital Circuit Power Select **L: When VDD1 > 2.8V, used Internal Regulator as digital circuit power.** **H: When VDD1 <=2.8V, used VDD1 as digital circuit power.**
CSEL	I	Select COM output direction . H: **Interlace mode** (recommended), COM2n(even number) is in the one side, COM(2n+1) (odd number) is in the opposite side. L: **Non-interlace mode**, COM0~COM63 is in one side, COM64~COM127 is in the opposite side.
VD1I VD1O	O	DCPS=L, Output voltage=2.4V DCPS=H, Output voltage=VDD1
VE	I	When writing EEPROM, VE should be pull up.
VPP	I	When writing EEPROM, it needs external power supply voltage
MF[2:0]	I	Reserve for testing only, recommend setting to [MF2.MF1.MF0 = 0.0.0]
DS[1:0]	I	Reserve for testing only, recommend setting to [DS1.DS0 = 0.0]

CSEL SETTING & REFERENCE CIRCUIT





6.4 MICROPROCESSOR INTERFACE

Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin
When RST is “L”, initialization is executed.</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>Interface mode</th><th>Data / Command</th><th>Data</th><th>Read, Write</th><th>Serial clock</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Parallel 80</td><td>A0</td><td>DB0 to DB7</td><td>Write only</td><td>-</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Parallel 68</td><td>A0</td><td>DB0 to DB7</td><td>Write only</td><td>-</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>3Line Serial</td><td>-</td><td>SID (DB7)</td><td>Write only</td><td>DB6</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>4Line Serial</td><td>A0</td><td>SID (DB7)</td><td>Write only</td><td>DB6</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>IIC Serial</td><td>-</td><td>SDA</td><td>Write only</td><td>DB7</td></tr>
</table>
*NOTE: It is impossible to read data from the on-chip DDRAM.
In 3-Line or 4-Line interface:
DB0 to DB5, E_RD and RW_WR must be fixed to “H” or “L”.
In IIC and 3-Line interface:
A0 must be fixed to “H” or “L”</td></tr>
</table>

<table>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is "L". When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
– A0 = "H": DB0 to DB7 are display data
– A0 = "L": DB0 to DB7 are control command</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Write execution control pin
<table>
<tr><td>PS2</td><td>PS1</td><td>PS0</td><td>MPU type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>6800-series</td><td>RW</td><td>Write control input pin
Keep this PIN on “L” level.</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>8080-series</td><td>/WR</td><td>The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><td>PS2</td><td>PS1</td><td>PS0</td><td>MPU Type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>6800-series</td><td>E</td><td>The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>8080-series</td><td>/RD</td><td>Keep this PIN on “H” level.</td></tr>
</table></td></tr>
<tr><td rowspan="3">DB0
to
DB7</td><td rowspan="3">I/O</td><td>8-bit data bus that is connected to the standard 8-bit microprocessor data bus.
When chip select is not active (CSB=H), DB0 to DB7 may be high impedance.</td></tr>
<tr><td>When the 3-Line/4-Line serial interface selected (PS[2:0] = "000" or “010”);
– DB0 to DB5: high impedance, the pins must be fixed to “H”.
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 is high impedance.</td></tr>
<tr><td>When the IIC serial interface selected (PS[2:0] = "100");
DB7: serial clock input (SCL)
DB6 , DB5 , DB4: serial input data (SDA_IN)
DB3, DB2: (SDA_OUT) serial data acknowledge for the IIC interface. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully IIC interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. In COG application where the track resistance from the SDA_OUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible during the acknowledge cycle the ST7571 will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level.
<u>DB6, DB5, ….DB2 must be connected together (SDA)</u>
DB0, DB1: Is slave address (SA) bit1, 0, must connect to VDD1 or VSS1.
When chip select is not active, DB0 to DB7 is floating.</td></tr>
</table>

6.5 LCD DRIVER OUTPUTS

LCD Driver Output Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG127</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">Frame</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>Positive</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>Negative</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>Positive</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>Negative</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display off / Power save mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM127</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td>Scan data</td><td>Frame</td><td>Common driver output voltage</td></tr>
<tr><td>H</td><td>Positive</td><td>XV0</td></tr>
<tr><td>H</td><td>Negative</td><td>V0</td></tr>
<tr><td>L</td><td>Positive</td><td>VM</td></tr>
<tr><td>L</td><td>Negative</td><td>VM</td></tr>
<tr><td colspan="2">Display off / Power save mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS2
COMS1</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

Recommend I/O Resistance

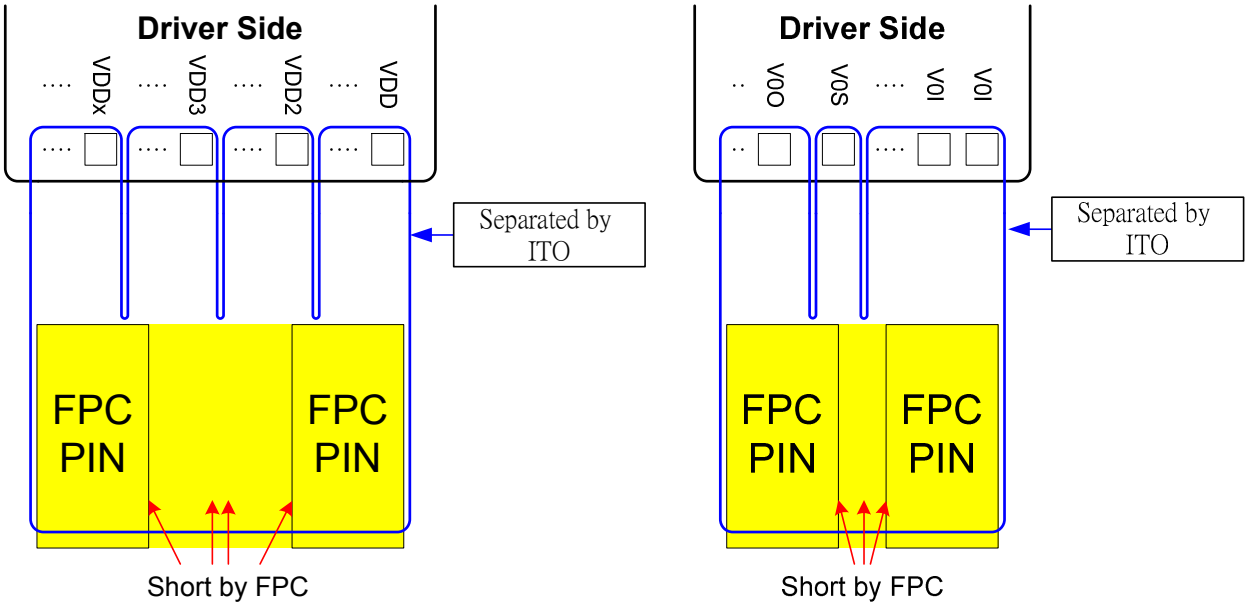
PIN Name	ITO Resister
PS2,PS1,PS0, OCS1, VEXT, DCPS, MF[2:0], DS[1:0]	<5kΩ
VDD1, VDD2, VDD3, VSS1, VSS2 , VSS3 , VPP, VD1I, VD1O	<100Ω
CSB , E_RD , RW_WR , A0 , DB0 …DB7, VE	<1KΩ
V0, VG, VM, XV0, VD1	<500Ω
RST	<10KΩ

NOTE:

1. Make sure that the ITO resistance of COM0 ~ COM127 is equal, and so it is of SEG0 ~ SEG127. These Limitations include the bottleneck of ITO layout.

2. To avoid the noise in different power system affect other power system, please separate different power source on ITO layout.

3. The V0, XV0 and Vg power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC.



7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7571 can interface with an MPU when CSB is "L". When these pins are set to any other combination, A0, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7571 has types of interface for kinds of an MPU. The interface is determined by PS0~PS2 pin as shown in Table 1. The reading feature does not support.

Table 1 Parallel / Serial Interface Mode

Type	PS2	PS1	PS0	CSB	Interface mode
Parallel	L	H	H	CSB	6800-series interface
	L	L			8080-series interface
Serial	L	L	L	CSB	3-Line SPI interface
	L	H	L	CSB	4-Line SPI interface
	H	L	L	CSB	IIC SPI interface

Parallel Interface (PS0 = "H")

The 8-bit data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in Table 2. The type of data transfer is determined by signals at A0, E_RD and RW_WR as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

PS1	CSB	A0	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CSB	A0	E	RW	DB0 to DB7	6800-series
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	L	H	L	Display data write
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface

3-Line / 4-Line (PS[2:0] = "000" or “010”)

Serial mode	PS2	PS1	PS0	CSB	A0
3-Line SPI mode	L	L	L	CSB	No used
4-Line SPI mode	L	H	L	CSB	A0
IIC SPI mode	H	L	L	No Used	No Used

The un-used pins should fix to “H”.

4-Line SPI Mode (PS0 = "L", PS1 = "H", PS2 = "L")

When ST7571 is active (CSB=“L”), serial data (SDA) and serial clock (SCLK) inputs are enabled. When ST7571 is not active (CSB=“H”), the internal 8-bit shift register and 3-bit counter are reset. The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. The read feature is not supported in this mode. Serial data on SDA is latched at the rising edge of serial clock on SCLK. After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

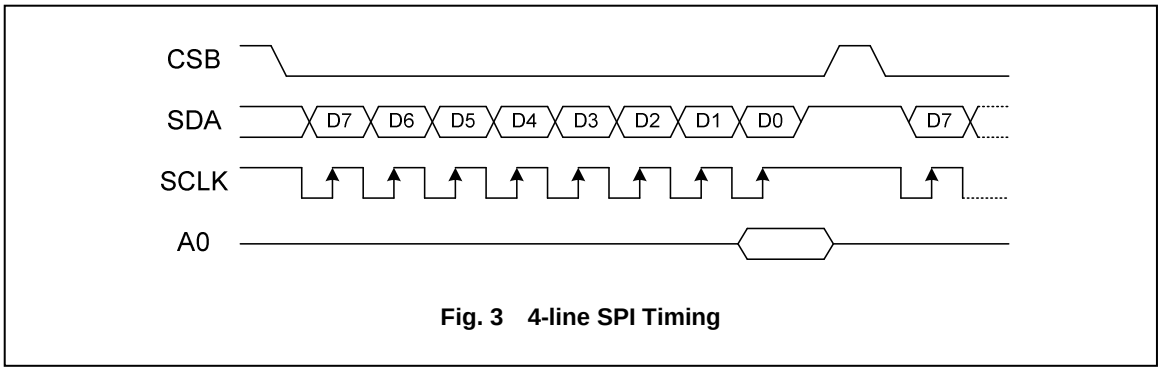
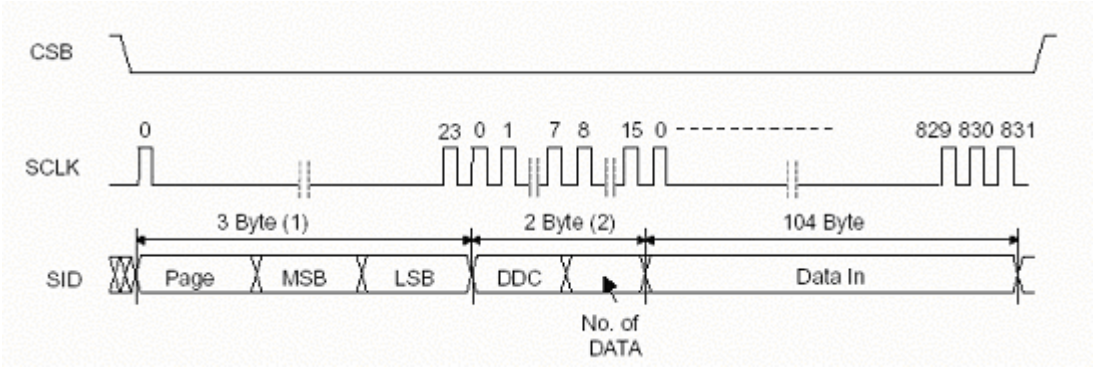


Fig. 3 4-line SPI Timing

3-Line SPI Mode (PS0 = "L", PS1 = "L" ,PS2= "L")

In 3-Line mode, default message from MCU is command, the 2 bytes command of **Display Data Length** must be set before display data send from MCU, after the display data is sent over, the next message is turned to be command. To write data to the DDRAM, send Display Data Length Command in 3-Line SPI mode. Data is latched at the rising edge of SCLK. And the DDRAM column address pointer will be increased by one automatically.



(1) Set Page and Column Address.

Set Page Address : 1 0 1 1 P3 P2 P1 P0

Set Column Address MSB : 0 0 0 1 0 Y7 Y6 Y5

Set Column Address LSB : 0 0 0 0 Y4 Y3 Y2 Y1

(2) Set DDC (Display Data Length Command) and No. of Data Bytes.

Set Display Data Length (For SPI mode Only):

1 1 1 0 1 0 0 0

Set No. of Data Bytes : D7 D6 D5 D4 D3 D2 D1 D0

(3) This figure is example for 104 Data bytes to be transferred.

Fig. 4 3-pin SPI Timing (A0 is not used)

This command is used in 3-Line SPI mode only. It will be two continuous commands, the first byte informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

NOTE: In spite of transmission of data, if CSB will be disable, state terminates abnormally. Next state is initialized.

I2C Interface (PS0= "L", PS1= "L", PS2= "H")

The I2C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCLK). Both lines must be connected with a pull-up resistor which drives SDA and SCLK to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

The I2C interface of ST7571 supports write access and read of acknowledge-bit. The I2C interface receives and executes the commands sent via the I2C Interface. It also receives RAM data and sends it to the Display RAM.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig 5.

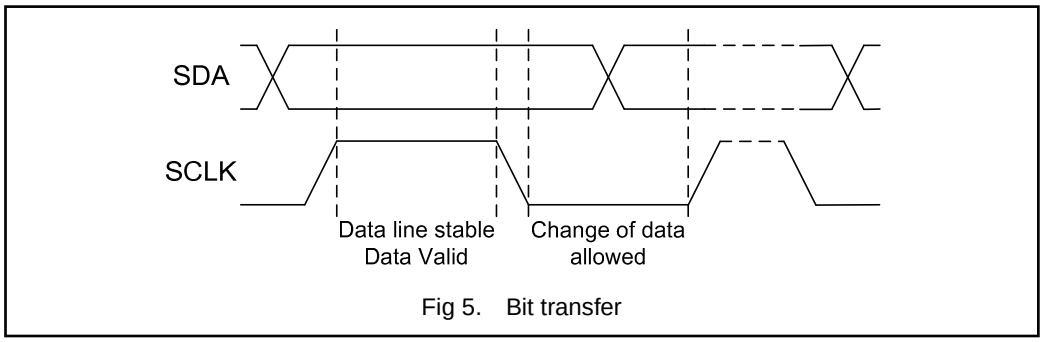


Fig 5. Bit transfer

START AND STOP CONDITIONS

Both SDA and SCLK lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCLK is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCLK is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.

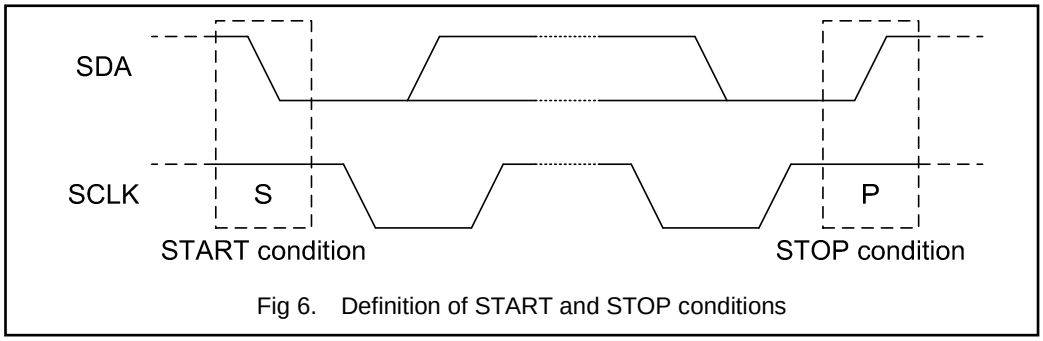


Fig 6. Definition of START and STOP conditions

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig 7 and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

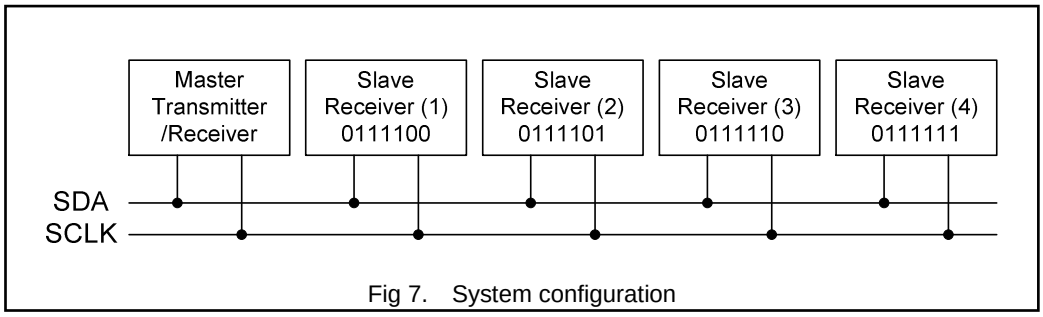


Fig 7. System configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating a acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated in Fig 8.

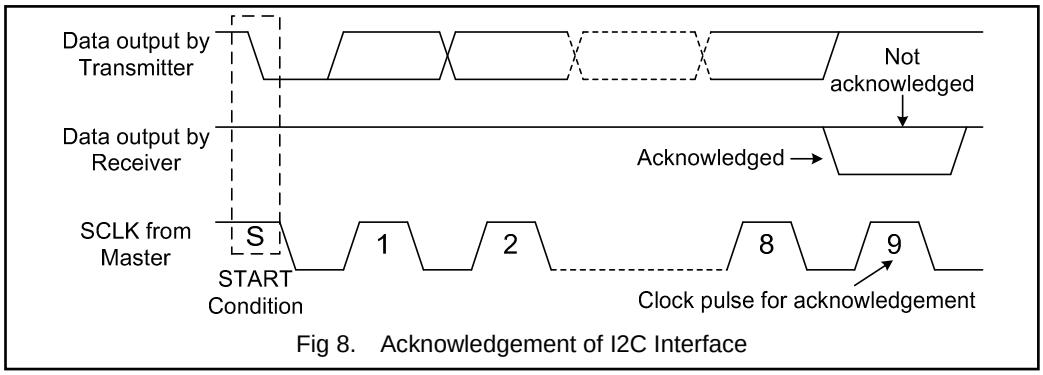


Fig 8. Acknowledgement of I2C Interface

I2C INTERFACE PROTOCOL

ST7571 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for ST7571. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1).

The I2C Interface protocol is illustrated in Fig 9.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words are followed and define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).
If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7571 device.
If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7571 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

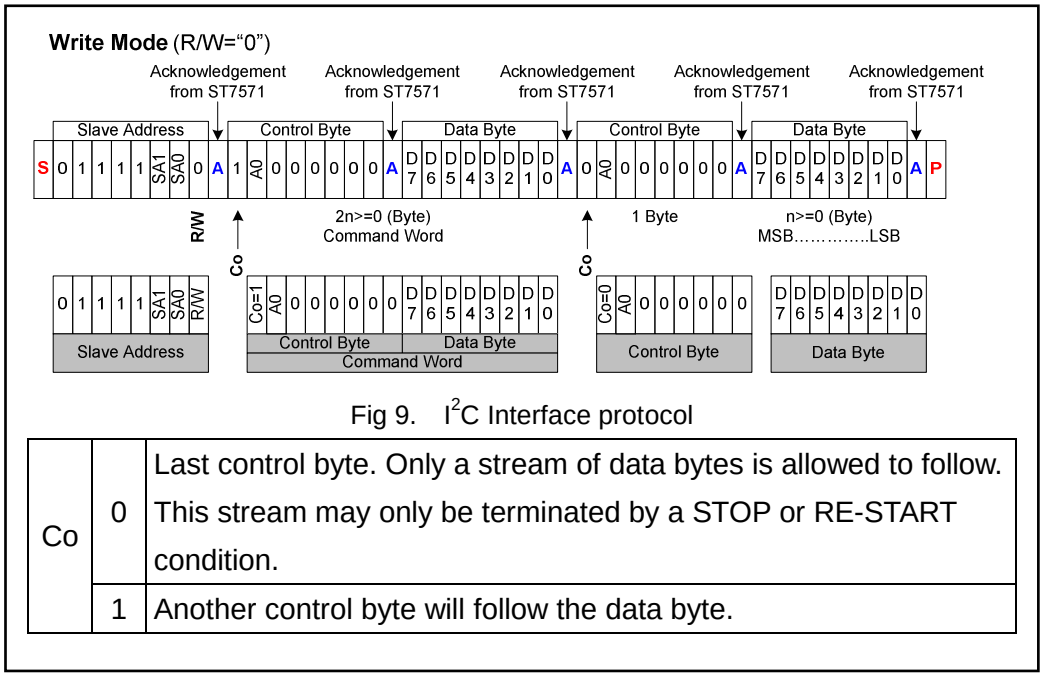


Fig 9. I^2C Interface protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

Data Transfer

The ST7571 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig. 10, Fig. 11.

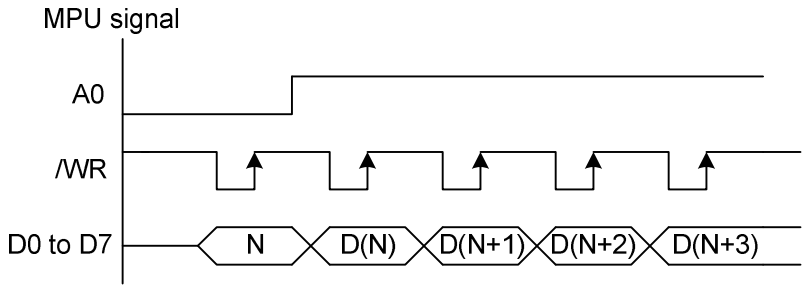


Fig. 10 Timing of MPU

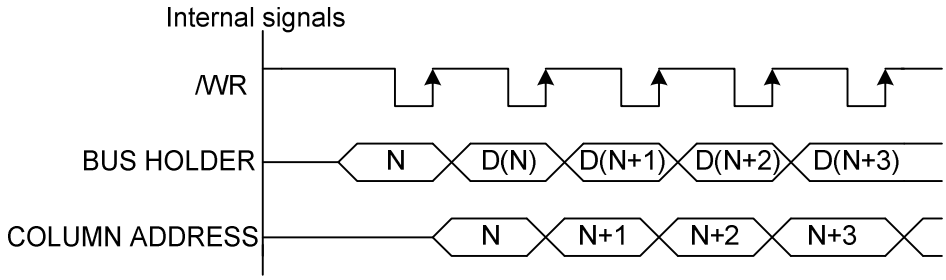


Fig. 11 Timing of driver IC

7.2 DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 129-row (17 pages by 8 bits) by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 15, and Page 16 is for Icon page.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

When set Column Address MSB / LSB instruction is issued, 7-bit [Y7:Y1] are set and lowest bit, Y0 is set to “0”. The column address is increased by 1 after each write data Refer to the following Fig.12.

(Note: in mode write in twice, the column address will turn to next column address)

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

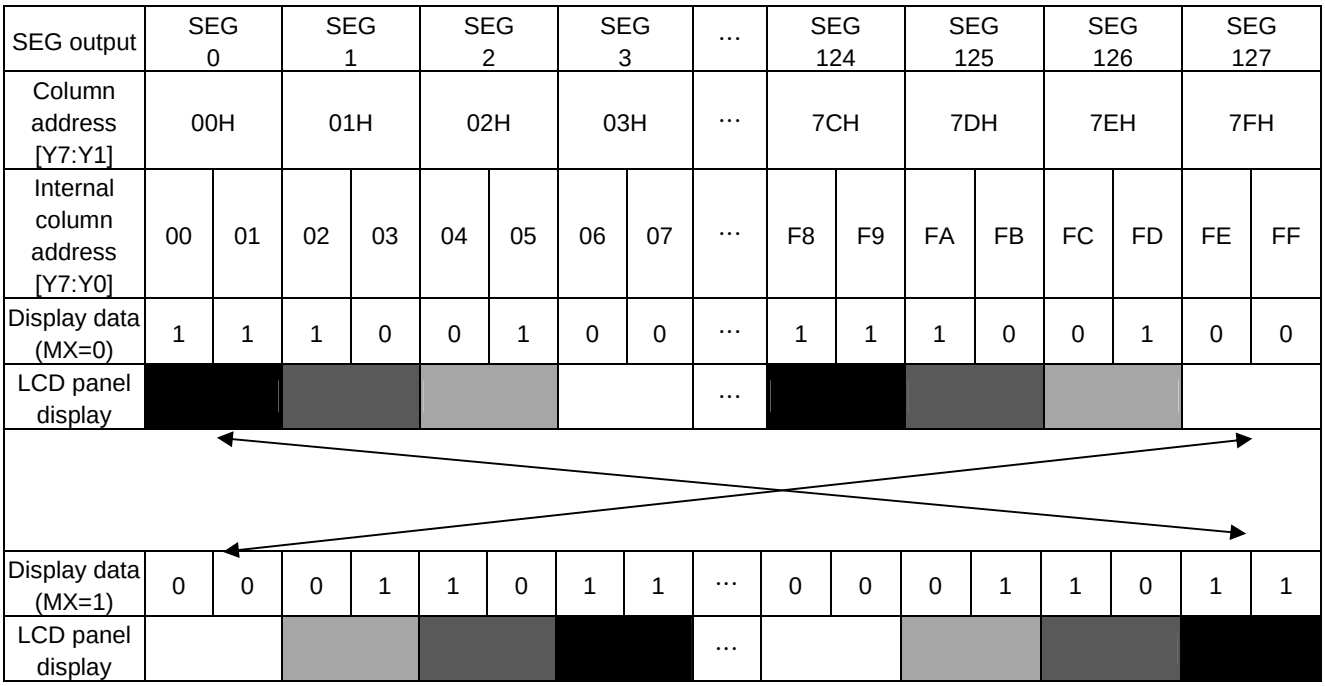


Fig. 12 The Relationship between the Column Address and The Segment Outputs

7.3 LCD DISPLAY CIRCUITS

Oscillator

This is on-chip Oscillator without external resistor. When the internal oscillator is used, this pin must connect to VDD1; when the external oscillator is used, this pin could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (FR) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Fig. 13.

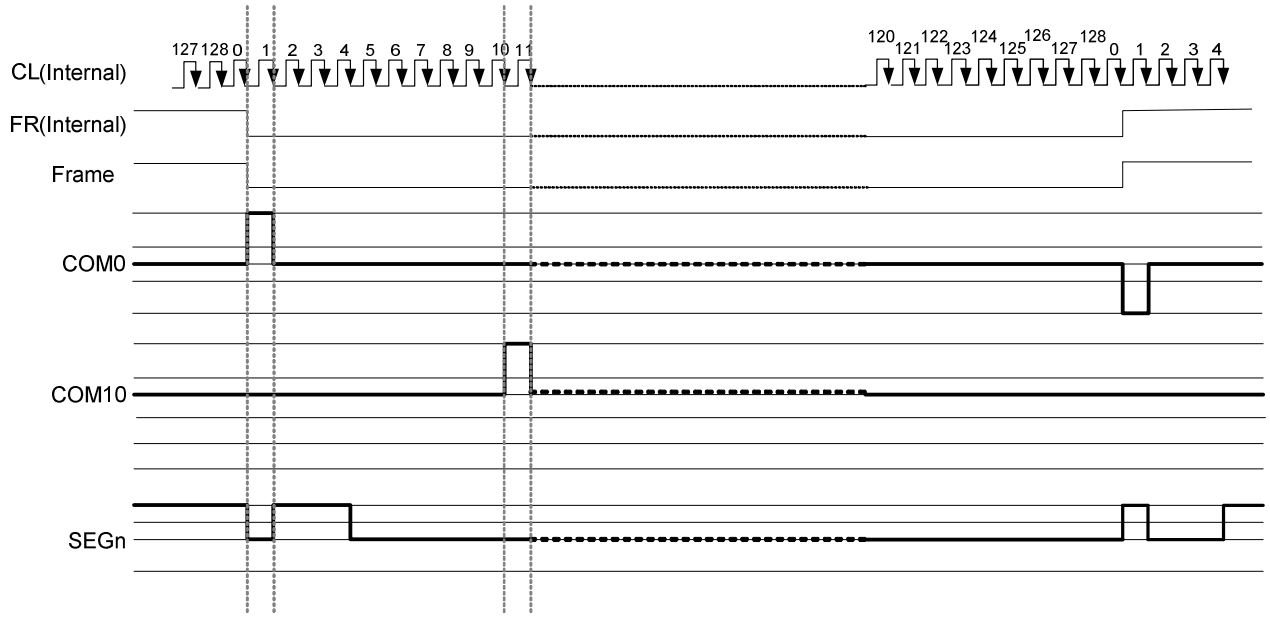


Fig. 13 frame AC Driving Waveform (Duty Ratio: 1/129)

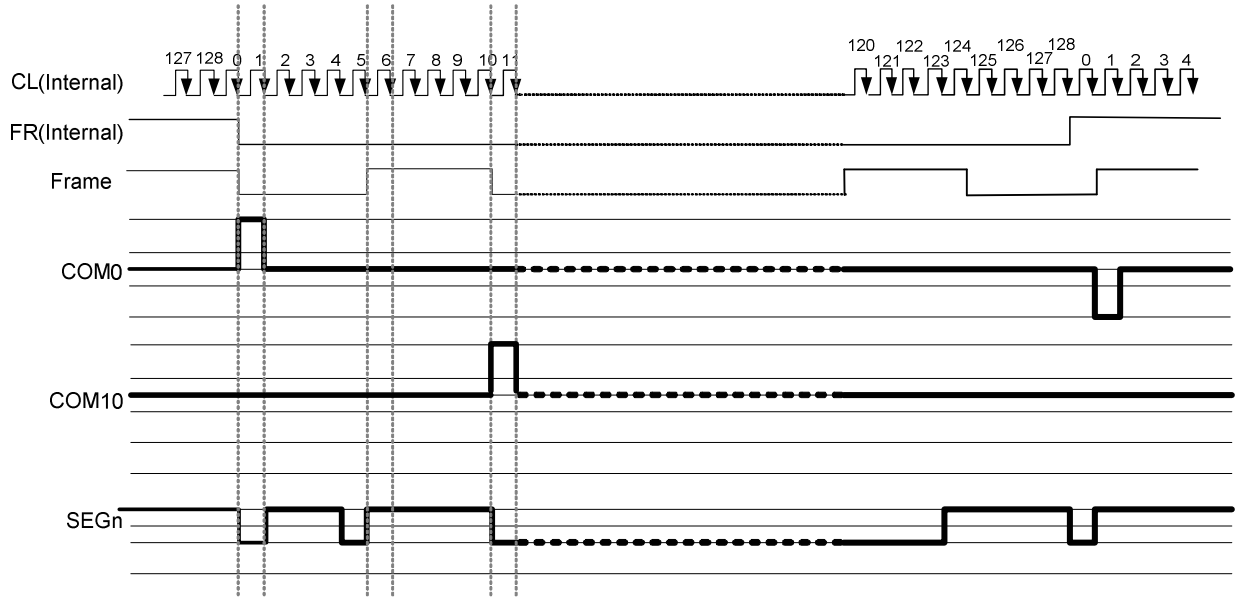


Fig. 14 N-Line Inversion Driving Waveform (N=5,Duty Ratio=1/129)

Partial Display on LCD

The ST7571 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages. The partial display duty ratio could be set from 16 ~ 128.

If the partial display region is out of the Max. Display range, it would be no operation.

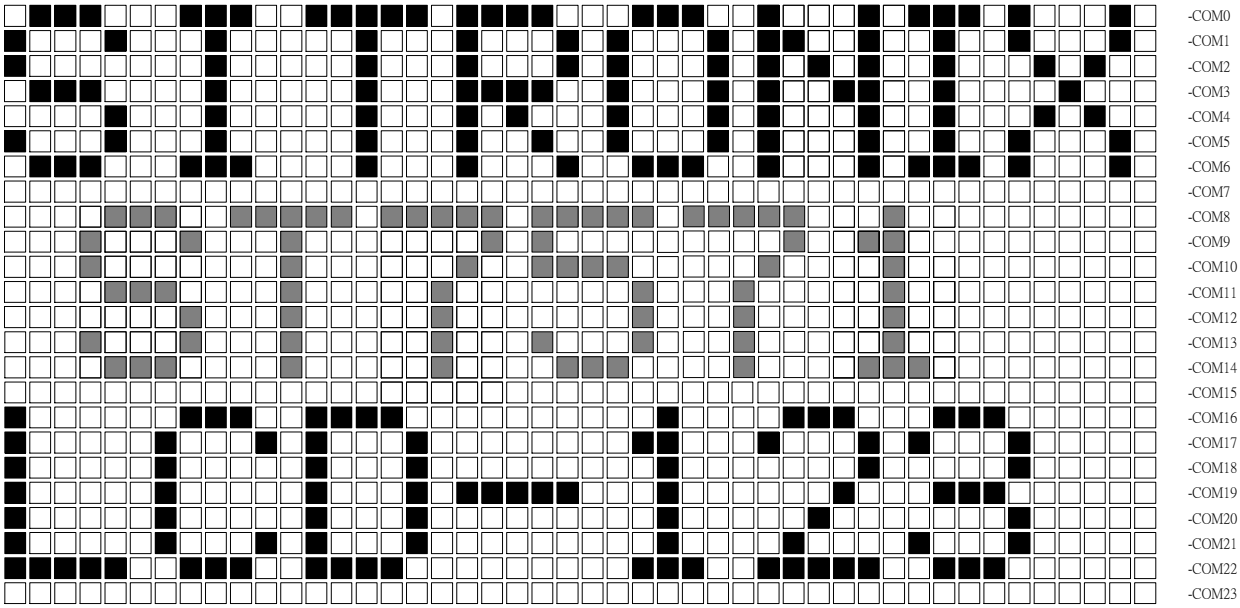


Fig. 15 Reference Example for Partial Display

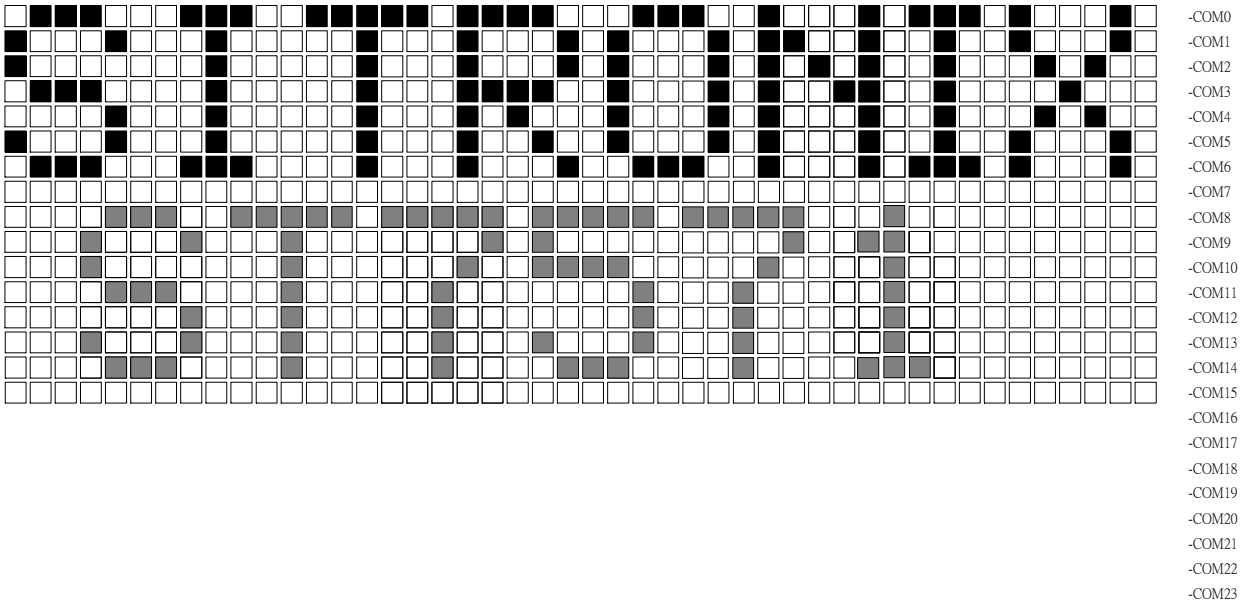


Fig. 16 Partial Display (Partial Display Duty=16,initial COM0=0)

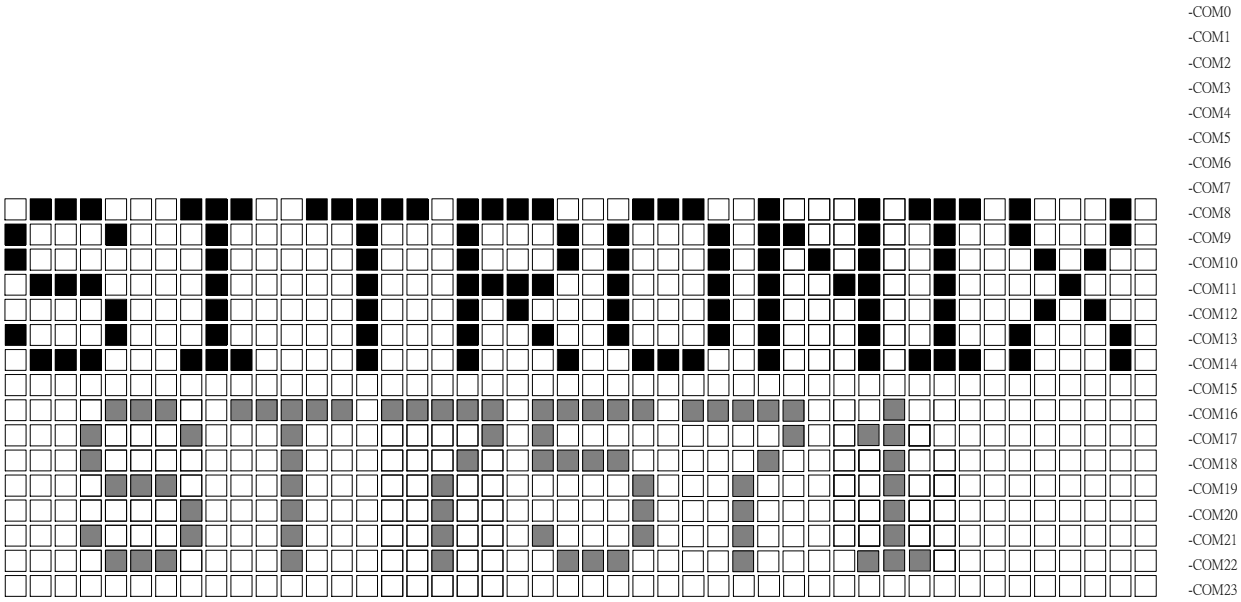


Fig. 17 Moving Display (Partial Display Duty=16,Initial COM0=8)

7.4 POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors,SRR and EV.

The parameter SRR can be set by “Select Regulator Register”.

The parameter EV can be set by “Set Electronic Volume Register”, the range of EV value is 0~63.

$$V0 = SRR \times \left(1 - \frac{(63 - EV)}{210}\right) \times 2.1$$

Table 5 Internal regulator Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
SRR (Select Regulator Ratio)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Fig. 18 Shows V0 voltage measured by adjusting regulator register ratio and 6-bit electronic registers for each temperature coefficient at Ta = 25℃. The recommended range of EV setting is level 16 ~ 47.

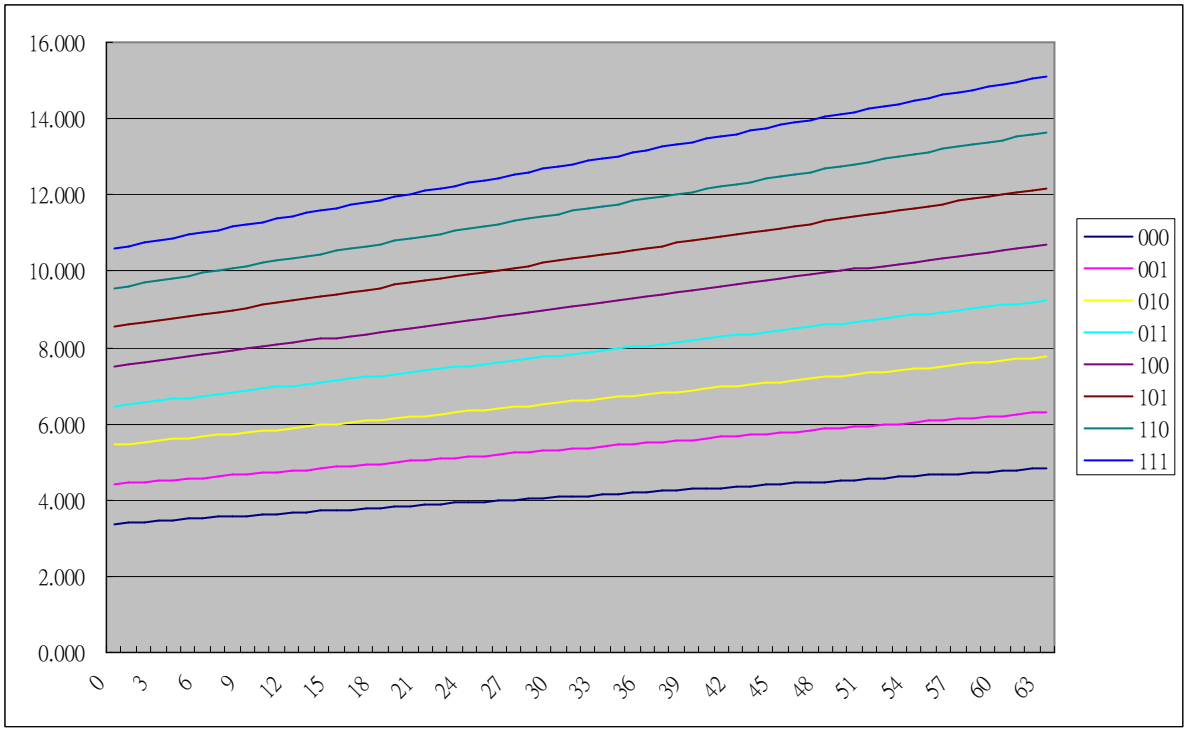


Fig. 18 Electronic Volume Level (25℃)

Voltage Follower Circuits

V0 is resistively divided into two voltage levels (VG, VM), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 6 shows the relationship between VG to VM level and each duty ratio.

Table 6 The Relationship between V1 to V4 Level and Each Duty Ratio

LCD bias	VG	VM	Remarks
1/N	2/N x V0	1/N x V0	N = 5 to 12

Booster Efficiency

Booster Efficiency (Level1~4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level2 is higher than level1), The Boost Efficiency is better than lower level, and it just need few more power consumption current. It could be applied to each multiple voltage Condition. When the LCD Panel loading is heavier, then the Performance of Booster will be not in a good working condition. We could set the BE level to be higher. We do not need to change to higher Booster Stage, and just need few more current. The Booster Efficiency Command could be used together with Booster Stage Command to choose one best Boost output condition. We could see the Boost Stage Command as a large scale operation, and see the Booster Efficiency Command as a small scale operation. These commands are very convenient for using.

7.5 RESET CIRCUITS

Setting RST to “L” or Reset instruction can initialize internal function.
When RST becomes “L”, following procedure is occurred.
Page address: 0
Column address: 0
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display duty ratio: 1/128
Reverse display ON / OFF: OFF (normal)
N-line inversion register: 0 (disable)
Entire Display ON/OFF: OFF
ICON Control register ON/OFF: OFF (ICON disable)
Power control register (VC, VR, VF) = (0, 0, 0)
Booster Efficiency BE = (1)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Contrast Level: 32
LCD bias ratio: 1/12
COM Scan Direction: 0
ADC Select: 0
Oscillator: OFF
Power Save Mode: Release
Display Data Length register: 0 (for SPI mode)

When RST instruction is issued, following procedure is occurred.
Page address: 0
Column address: 0
Initial display line: 0 (First)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Contrast Level: 32
Display Data Length register: 0 (for SPI mode)

8. INSTRUCTIONS

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	
Mode Set	0	0	0	0	1	1	1	0	0	0	2-byte instruction to set Mode and FR(Frame frequency control) BE(Booster efficiency control)	9.1.1
	0	0	FR3	FR2	FR1	FR0	BE1	BE0	x'	0		
Write display data	1	0	Write data								Write data into DDRAM	9.1.2
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable(default) ICON=1: ICON enable & set the page address to 16	9.1.3
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address	9.1.4
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB	9.1.5
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB	9.1.6
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON	9.1.7
Set initial display line register	0	0	0	1	0	0	0	0	x'	x'	2-byte instruction to specify the initial display line to realize vertical scrolling	9.1.8
	0	0	x'	S6	S5	S4	S3	S2	S1	S0		
Set initial COM0 register	0	0	0	1	0	0	0	1	x'	x'	2-byte instruction to specify the initial COM0 to realize window scrolling	9.1.9
	0	0	x'	C6	C5	C4	C3	C2	C1	C0		
Set partial display duty ration	0	0	0	1	0	0	1	0	x'	x'	2-byte instruction to set partial display duty ratio	9.1.10
	0	0	D7	D6	D5	D4	D3	D2	D1	D0		
Set N-line inversion	0	0	0	1	0	0	1	1	x'	x'	2-byte instruction to set N-line inversion register	9.1.11
	0	0	x'	x'	x'	N4	N3	N2	N1	N0		
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode	9.1.12
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1: reverse display	9.1.13
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display EON=1: entire display ON	9.1.14

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation	9.1.15
Select regulator register	0	0	0	0	1	0	0	R2	R1	R0	Select the internal resistance ratio of the regulator resistor	9.1.16
Select electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the reference voltage	9.1.17
	0	0	x'	x'	EV5	EV4	EV3	EV2	EV1	EV0		
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias	9.1.18
SHL select	0	0	1	1	0	0	SHL	x'	x'	x'	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction	9.1.19
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0: normal direction ADC=1: reverse direction	9.1.20
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator	9.1.21
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode	9.1.22
Release power save mode	0	0	1	1	1	0	0	0	0	1	release power save mode	9.1.23
Reset	0	0	1	1	1	0	0	0	1	0	initial the internal function	9.1.24
Display data length	x'	x'	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI mode)	9.1.25
	x'	x'	D7	D6	D5	D4	D3	D2	D1	D0		
NOP	0	0	1	1	1	0	0	0	1	1	No operation	9.1.26
Test Command set 1	0	0	1	1	1	1	x'	x'	x'	x'	Enter test command set 1 Use for Burning EE	9.1.27
Test Command set 2	0	0	1	1	0	1	0	0	0	1	Enter test command set 2 Use for Burning EE	9.1.28
Test Command set 3	0	0	0	1	1	1	1	0	1	1	Don't use this instruction	9.1.29

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
COMMAND SET 1											
Disable autoread	0	0	1	0	1	0	1	0	1	0	Disable autoread
Enter EEPROM mode	0	0	0	0	0	1	0	0	1	1	Enter EEPROM mode
Enable read mode	0	0	0	0	1	0	0	0	0	0	Enable read mode
Set read pulse	0	0	0	1	1	1	0	0	0	1	Set read pulse width (Do not modify this value)
Exit EEPROM mode	0	0	1	0	0	0	0	0	1	1	Exit EEPROM mode
Enable erase mode	0	0	0	1	0	0	1	0	1	0	Enable erase mode
Set erase pulse	0	0	0	1	0	1	0	1	0	1	Set erase pulse width (Do not modify this value)
Enable write mode	0	0	0	0	1	1	0	1	0	1	Enable write mode
Set write pulse	0	0	0	1	1	0	1	0	1	0	Set write pulse width (Do not modify this value)
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
COMMAND SET 2											
Increase vop offset	0	0	0	1	0	1	0	0	0	1	Increase vop offset 1 level
Decrease vop offset	0	0	0	1	0	1	0	0	1	0	Decrease vop offset 1 level
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode

EE Burning Flow

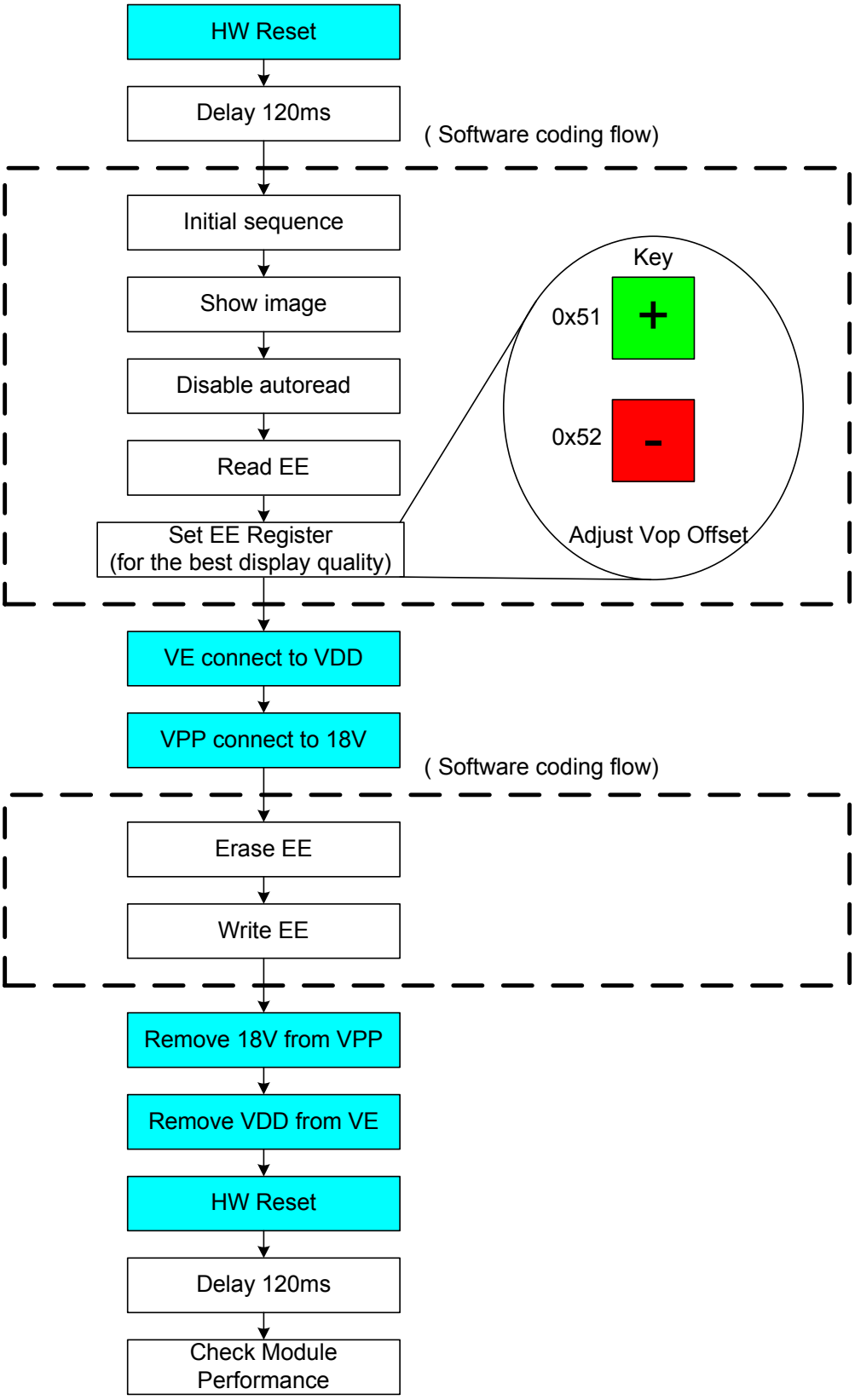


Fig. 19 EE Burning flow chart

Software function

void Disable_autoread(void)			
{			
	Write(COMMAND, 0x00D1);		//Enter test command set 2
	Write(COMMAND, 0x00AA);		//Disable autoread
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

void Read_EE (void)			
{			
	Write(COMMAND, 0x00D1);		//Enter test command set 2
	Write(COMMAND, 0x00AA);		//Autoread disable
	Write(COMMAND, 0x0013);		//Enter EEPROM mode
	Write(COMMAND, 0x0020);		//Enable read mode
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0071);		//Set read pulse
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0083);		//Exit EEPROM mode
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

void Set_EE _Register (void)			

{ // Adjust Vop offset here
//command 0x51 and 0x52 can be set many times for adjusting a suitable vop
//Maxmum adjusting range are +-16 levels.			

	Write(COMMAND, 0x00FD);		//Enter test command set 1
	Write(COMMAND, 0x0051); or Write(COMMAND, 0x0052);		//0x0051 for increase Vop offset //0x0052 for decrease Vop offset
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

void Erase_EE (void)			
{			
	Write(COMMAND, 0x00D1);		//Enter test command set 2
	Write(COMMAND, 0x0013);		//Enter EEPROM mode
	Write(COMMAND, 0x004A);		//Enable erase mode
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0055);		//Set erase pulse
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0083);		//Exit EEPROM mode
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

void Write_EE (void)			
{			
	Write(COMMAND, 0x00D1);		//Enter test command set 2
	Write(COMMAND, 0x0013);		//Enter EEPROM mode
	Write(COMMAND, 0x0035);		//Enable write mode
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x006A);		//Set write pulse
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0083);		//Exit EEPROM mode
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

9.1.1 Set Mode Register

2-byte instruction to set FR (Frame frequency control) and BE (Booster efficiency control)

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	FR3	FR2	FR1	FR0	0	BE	x'	0

Frame frequency

This command is used to set the frame frequency.

FR_3	FR_2	FR_1	FR_0	FR frequency
0	0	0	0	77 Hz ±10%
0	0	0	1	51 Hz ±20%
0	0	1	0	55 Hz ±20%
0	0	1	1	58 Hz ±20%
0	1	0	0	63 Hz ±20%
0	1	0	1	67 Hz ±20%
0	1	1	0	68 Hz ±20%
0	1	1	1	70 Hz ±20%
1	0	0	0	73 Hz ±20%
1	0	0	1	75 Hz ±20%
1	0	1	0	80 Hz ±20%
1	0	1	1	85 Hz ±20%
1	1	0	0	91 Hz ±20%
1	1	0	1	102 Hz ±20%
1	1	1	0	113 Hz ±20%
1	1	1	1	123 Hz ±20%

Booster Efficiency

The ST7571 incorporates software configurable Booster Efficiency Command. It could be used with Voltage multiplier to get the suitable Vop and Power consumption. Default setting is Level 2.

BE1	BE0	Description
0	0	Booster Efficiency Level 1
0	1	Booster Efficiency Level 2
1	0	Booster Efficiency Level 3
1	1	Booster Efficiency Level 4

9.1.2 Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

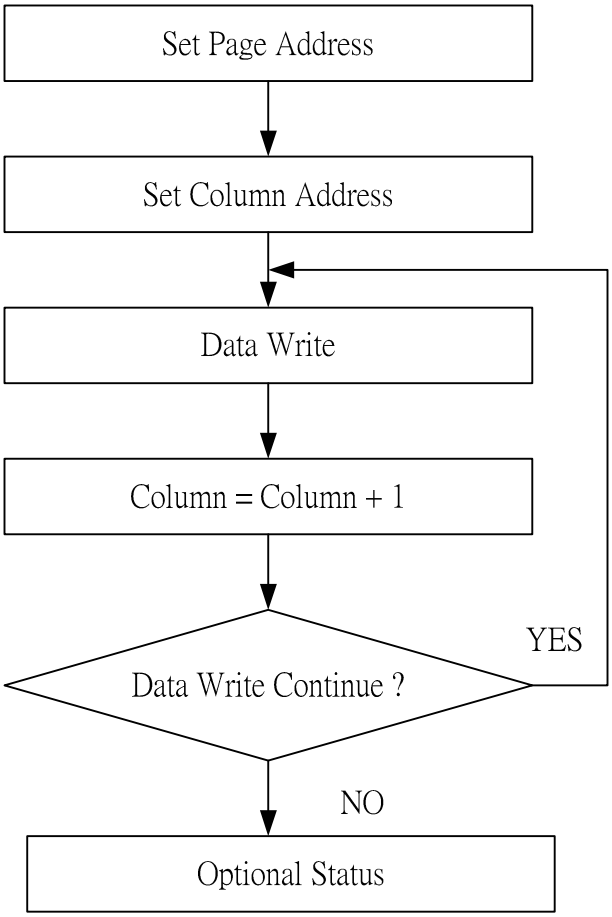


Fig. 20 Sequence for Writing Display Data

9.1.3 ICON Control Register ON/OFF

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0). When ICON control register is set to “1”, ICON display is enabled and page address is set to “16”. Then user can write data for icons. It is impossible to set the page address to “16” by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to “16”. When ICON control register is set to “0”, ICON display is disabled.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ICON

ICON=0: ICON disable (default)

ICON=1: ICON enable & set the page address to 16

9.1.4 Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write display data. Changing the Page Address doesn't affect the display status. Set Page Address instruction can not be used to set the page address to “16”. Use ICON control register ON/OFF instruction to set the page address to “16”.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	**Page**
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

9.1.5 & 9.1.6 Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write display data.

When the microprocessor writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set Column Address LSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y7	Y6	Y5	Y4	Y3	Y2	Y1	**Column address [Y7:Y1]**
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

9.1.7 Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON

DON = 0: display OFF

9.1.8 Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row(COM0) of LCD panel.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	S6	S5	S4	S3	S2	S1	S0
S6	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**	**Line address**		
0	0	0	0	0	0	0	0		
0	0	0	0	0	0	1	1		
0	0	0	0	0	1	0	2		
0	0	0	0	0	1	1	3		
:	:	:	:	:	:	:	:		
1	1	1	1	1	0	0	124		
1	1	1	1	1	0	1	125		
1	1	1	1	1	1	0	126		
1	1	1	1	1	1	1	127		

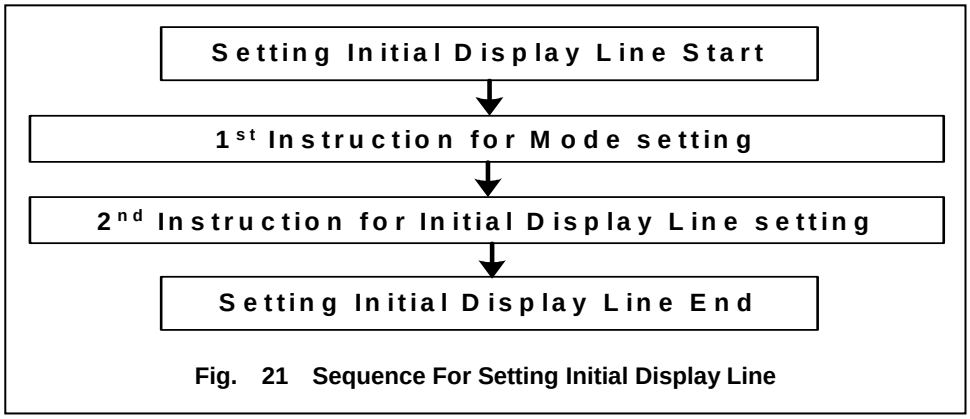


Fig. 21 Sequence For Setting Initial Display Line

9.1.9 Set Initial COM0 Register

Set the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127

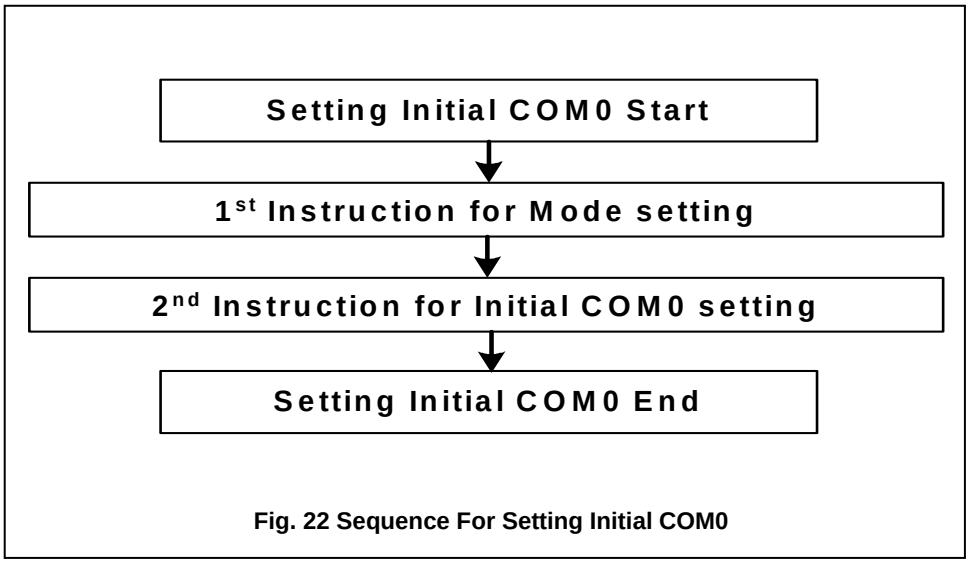


Fig. 22 Sequence For Setting Initial COM0

9.1.10 Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio
0	0	0	0	0	0	0	0	No operation
:	:	:	:	:	:	:	:	
0	0	0	0	1	1	1	1	
0	0	0	1	0	0	0	0	1/17
0	0	0	1	0	0	0	1	1/18
:	:	:	:	:	:	:	:	:
0	1	1	0	0	1	0	0	1/101
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/128
1	0	0	0	0	0	0	0	1/129
1	0	0	0	0	0	0	1	No Operation
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	

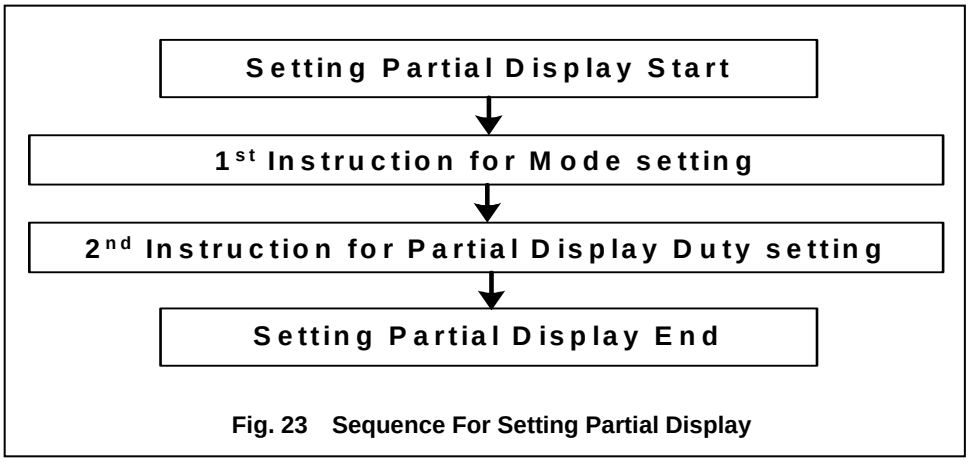


Fig. 23 Sequence For Setting Partial Display

9.1.11 Set N-line Inversion Register (For 128 duty condition, recommended 13-line inversion)

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K : D/N

D: The number of display duty ratio (D is selectable by customers)

N: N for N-line inversion (N is selectable by customers).

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

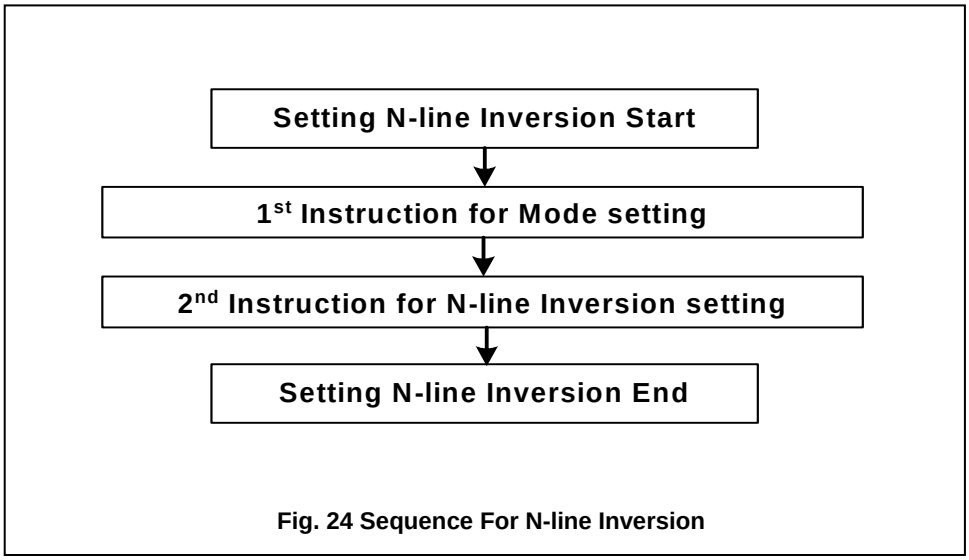


Fig. 24 Sequence For N-line Inversion

9.1.12 Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

9.1.13 Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DDRAM data = “00” – White	DDRAM data = “01” – Light gray	DDRAM data = “10” – Dark gray	DDRAM data = “11” – Dark
0 (normal)	White (“00”)	Light gray (“01”)	Dark gray (“10”)	Dark (“11”)
1 (reverse)	Dark (“11”)	Dark gray (“10”)	Light gray (“01”)	White (“00”)

9.1.14 Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

Entire	DDRAM data = “00” – White	DDRAM data = “01” – Light gray	DDRAM data = “10” – Dark gray	DDRAM data = “11” – Dark
0 (normal)	White (“00”)	Light gray (“01”)	Dark gray (“10”)	Dark (“11”)
1 (Entire)	Dark (“11”)	Dark gray (“11”)	Light gray (“11”)	White (“11”)

9.1.15 Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VF	Status of internal power supply circuits
0		Internal voltage converter circuit is OFF
1		Internal voltage converter circuit is ON
	0	Internal voltage follower circuit is OFF
	1	Internal voltage follower circuit is ON

9.1.16 Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

9.1.17 Set Electronic Volume Register

Consist of 2-byte Instructions

The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register.

After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

9.1.18 Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

9.1.19 SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	x	x	x

SHL = 0: normal direction (COM0 → COM127)

SHL = 1: reverse direction (COM127 → COM0)

9.1.20 ADC Select

Change the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG127)

ADC = 1: reverse direction (SEG127 → SEG0)

9.1.21 Oscillator ON Start

This instruction enables the built-in oscillator circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

9.1.22 & 9.1.23 Power Save

The ST7571 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode , P = 1: sleep mode

Release Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

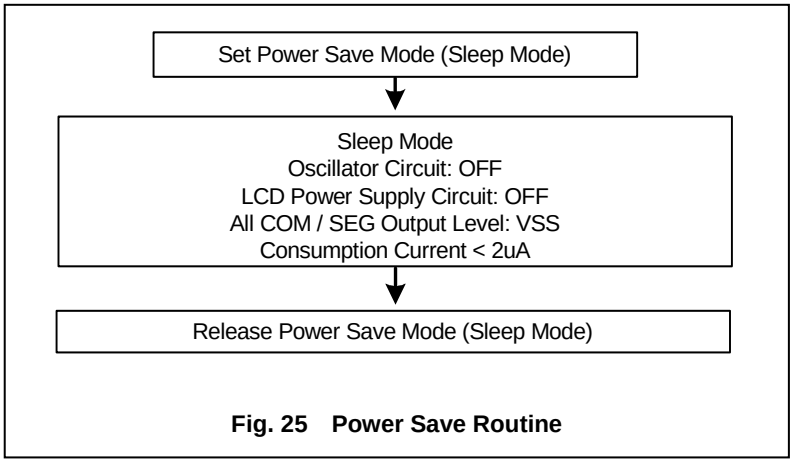


Fig. 25 Power Save Routine

9.1.24 Reset

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

9.1.25 Display Data Length (8 bits 3-Line SPI Mode)

This command is used in 3-Line SPI mode only. It concludes two continuous commands, the first byte is command code, the second byte will indicate how many data bytes will be written. When A0 is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command.

The 1st Instruction: Set Data Length Command (Only Write Mode)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

9.1.26 NOP

No operation

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

9.1.27 Test Command set 1

This instruction is for testing IC. Use for burning EE.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	x	1

9.1.28 Test Command set 2

This instruction is for testing Use for burning EE.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	1	0	0	0	1

9.1.29 Test Command set 3

This instruction is for testing IC. Please do not use it.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	1	0	1	1

10. COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

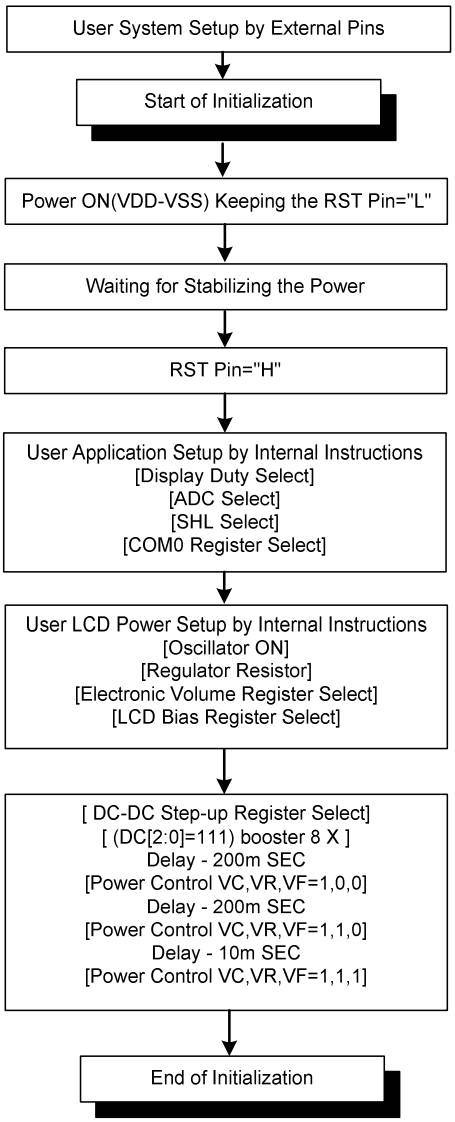
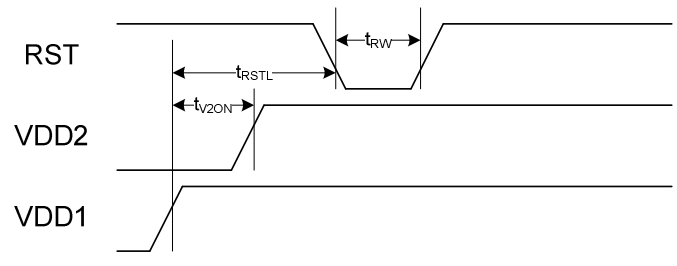


Fig. 26 Initializing with the Built-in Power Supply Circuits

Power Sequence



1. tV2ON: VDD2 power ON delay.
   => 0 ≤ tV2ON ≤ No Limitation.
2. tRSTL: Reset Low time after VDD1 is stable.
   => 0 ≤ tRSTL ≤ 50 ms*1.
3. tRW: Reset low pulse width.
   Please refer to RESB timing specification.

Note:

1. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON. The specification listed here is to prevent abnormal display on LCD module.
2. Be sure the power is stable and the internal reset is finished (refer to RST timing specification).

Referential Instruction Setup Flow: Data Displaying

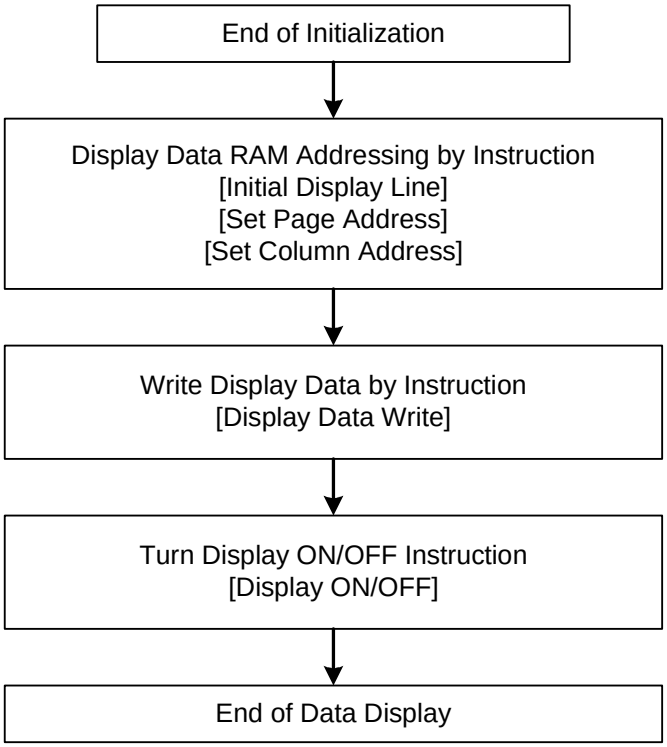


Fig. 27 Data Displaying

Referential Instruction Setup Flow: Power OFF

Power OFF Flow and Sequence

By setting 0xA9, ST7571 will go into power save mode. The LCD driving outputs are fixed to VSS, built-in power circuits are turned OFF and a discharge process starts.

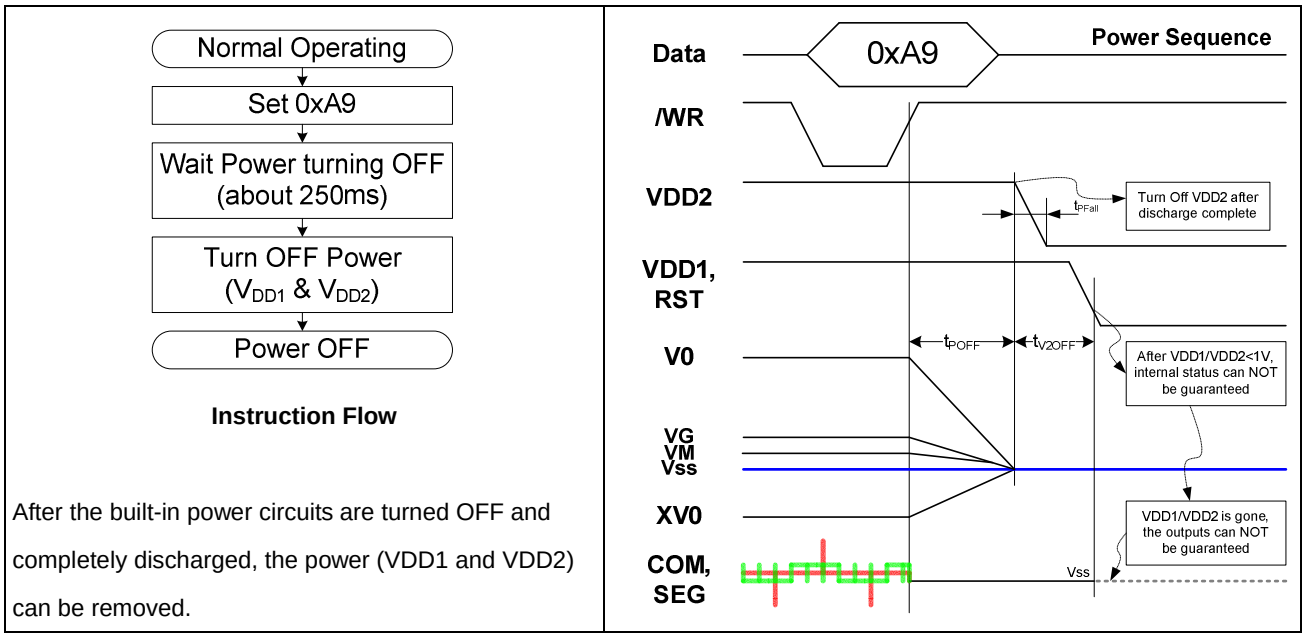
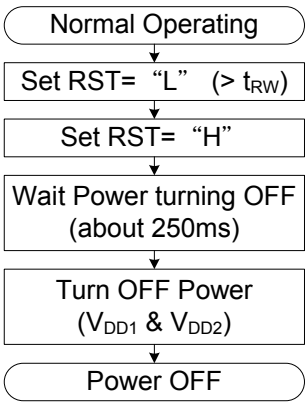


Fig. 28 Power off instruction flow

An alternate method is to use the RST signal to set ST7571 into power save mode. After hardware reset, ST7571 is in power save mode (same as previous case).



Operating Flow

After the built-in power circuits are turned OFF and completely discharged, the power (VDD1 and VDD2) can be removed.

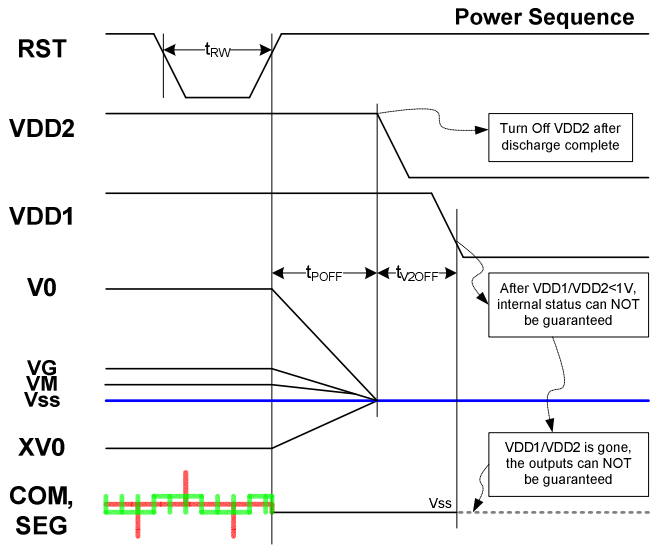


Fig. 29 Power off operating flow

Note:

1. t_{IPOFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDD1 and VDD2 OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDD1 OFF before VDD2. Without VDD1, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.8".
7. When turning VDD2 OFF, the falling time should follow the specification:
   300ms ≤ t_{PFall} ≤ 1sec

LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD1	1.8~3.3	V
Power supply voltage	VDD2	2.4~3.3	V
Power supply voltage	VDD3	2.4~3.3	V
Power supply voltage	V0	0~15.12	V
Power supply voltage	XV0	-12.6 ~ 0	V
Power supply voltage	VG	1.8 to VDD2	V
Power supply voltage	VM	0.7 to (VDD2-0.7)	V
Operating temperature	TOPR	–30 to +85	℃
Storage temperature	TSTR	–65 to +150	℃

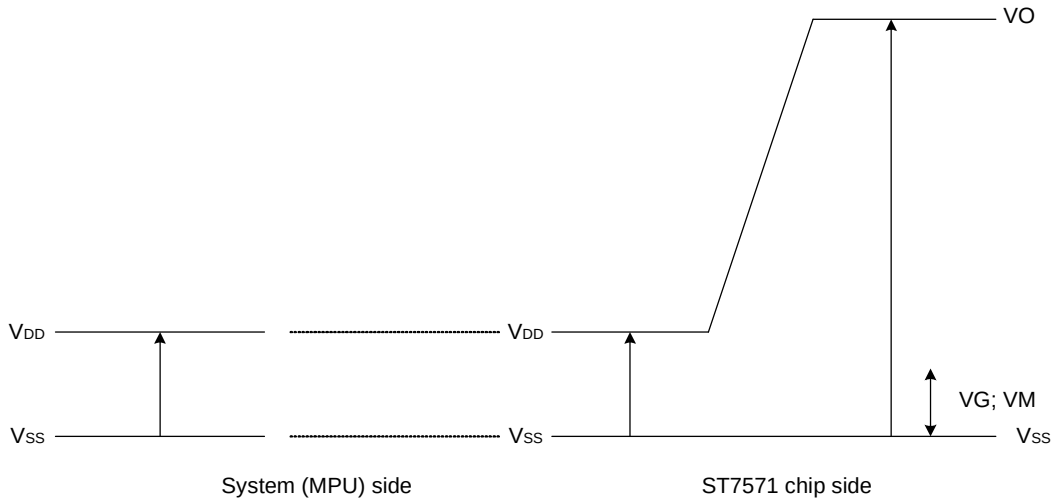


Fig. 30

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of VG, VM are always such that

   VO > VG > VM > VSS > XV0

Referential LCD Module Setting

VDD1=1.8V, VDD2=2.8V, N-Line=0, Panel Size=1.5”

Duty	Vop	Bias
1/129	10.5V~12V	1/9,
1/81	10.5V~11.5V	1/10
1/65	9.5V ~ 10.5V,	1/9

Note: It is recommended to reserve some range for user adjustment and temperature effect.

DC CHARACTERISTICS

V_{DD1} = 1.8 V to 3.3V; V_{SS} = 0 V; T_{emp} = -30℃ to +85℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD1			1.8	—	3.3	V	VDD1
Operating Voltage (2)		VDD2	(Relative to VSS)		2.4	—	3.3	V	*3
Operating Voltage (3)		VDD3	(Relative to VSS)		2.4	—	3.3	V	*3
High-level Input Voltage		VIHC			0.7 x VDD1	—	VDD1	V	*2
Low-level Input Voltage		VILC			VSS	—	0.3 x VDD1	V	*2
Input leakage current		ILI	VIN = VDD1 or VSS		–1.0	—	1.0	μA	*4
Booster output voltage range		V0			3.38	—	15.12	V	
Voltage follower output voltage		Vm			0.7	Vg/2	VDD2-0.7	V	
Vg output voltage range		Vg			1.8	—	VDD2	V	
XV0 output voltage range		XV0			Vg-3.38	—	—	V	
Output leakage current		ILO	VIN = VDD1 or VSS		–3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance		RON	Ta = 25℃	Vop=12V ΔV=1.2V	—	0.7		KΩ	SEGn COMn *6
				VG=2V ΔV=0.2V	—	0.7			
Oscillator Frequency	Frame frequency	fFRAME	1/129 duty Ta = 25℃ FR[3:0]=0000(77Hz)		70	77	84	Hz	

Bare Dice Consumption Current : During Display, with the Internal Power Supply, Current consumed by total ICs when an external power supply(VDD1,VDD2,VDD3) is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDD1=1.8V, VDD2=VDD3=2.8V Vop=10.5V, 8X booster, 1/9BIAS, Ta = 25℃ , N-Line=1	—	450	600	μA	*7
Power Down	ISS	VDD1=1.8V, VDD2=VDD3=2.8V , Ta = 25℃	—	5	10	μA	*8

Notes to the DC characteristics

1. The maximum possible V_{OUT} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. Power-down mode. During power down all static currents are switched off.

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR (R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.

*3 For analog power.

*4 The A0, /RD (E), /WR, /(R/W), CSB, IMS, OSC, P/S, /DOF, RESB and MODE terminals.

*5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.

*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (VG, VM). These are specified for the operating voltage range.

RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*7,8 It indicates the current consumed on IC alone when the internal oscillator circuit and display are turned on.

TIMING CHARACTERISTICS

System Bus Write Characteristics 1 (For the 8080 Series MPU)

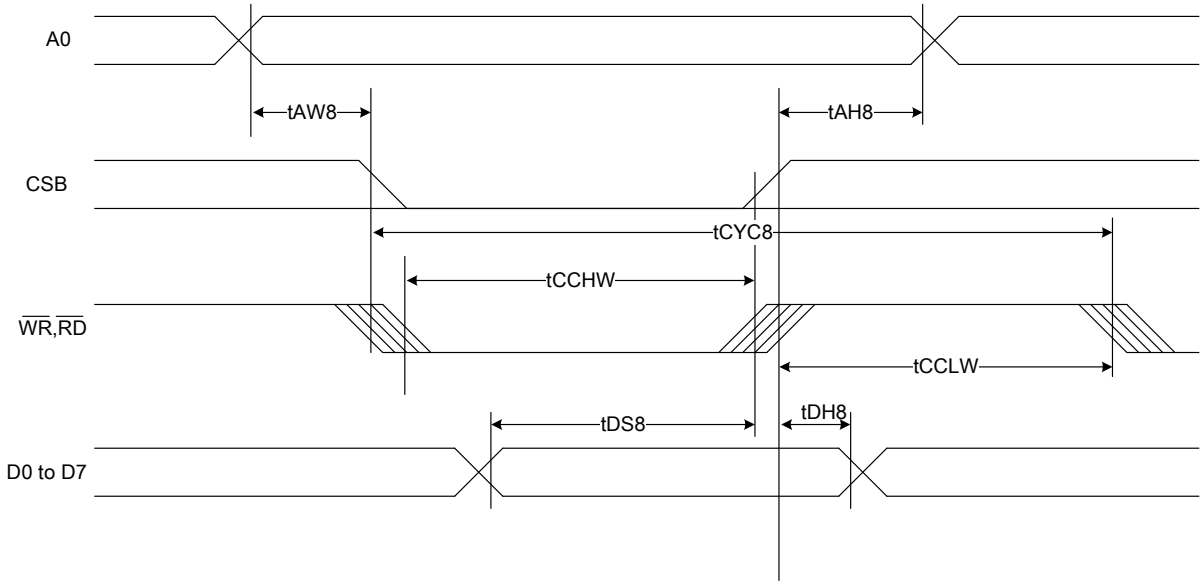


Fig. 31

(VDD1 = 1.8~3.3V , Ta =-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Write L pulse width	WR	tCCLW		360	—	
Write H pulse width		tCCHW		280	—	
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leq$ (tCYC8 – tCCLW – tCCHW) is specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW is specified as the overlap between CSB being “L” and WR being at the “L” level.

System Bus Write Characteristics 1 (For the 6800 Series MPU)

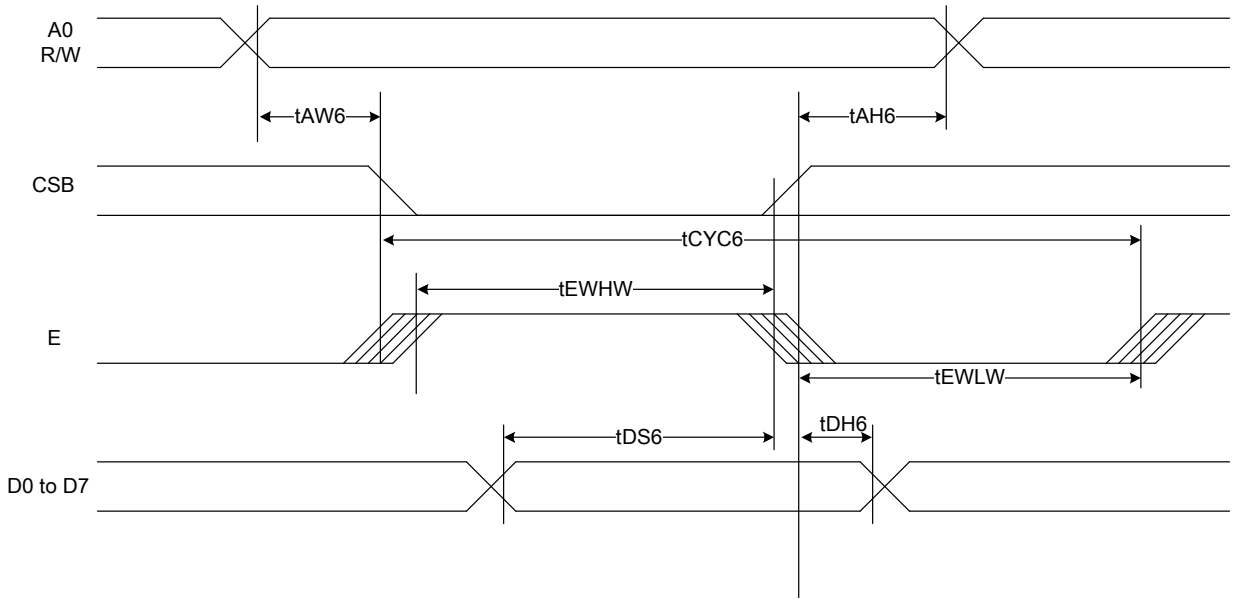


Fig. 32

(VDD1 =1.8V~3.3V , Ta =-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) is specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW is specified as the overlap between CSB being “H” and E being “L”.

SERIAL INTERFACE(4-Line Interface)

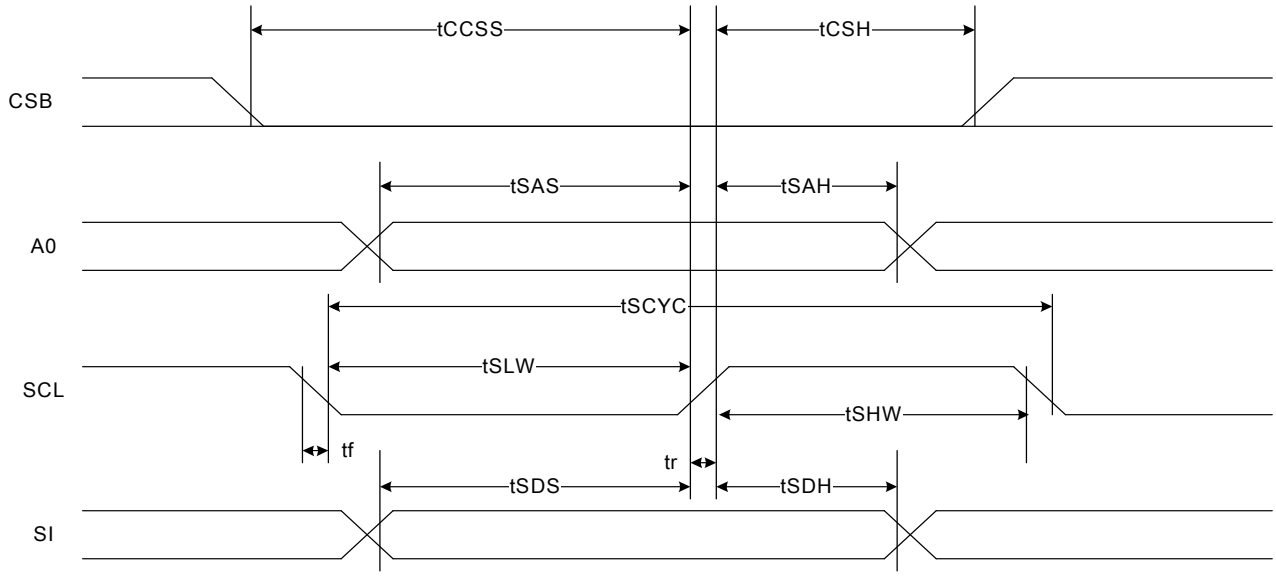


Fig. 33

(VDD1=1.8V~3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

SERIAL INTERFACE(3-Line Interface)

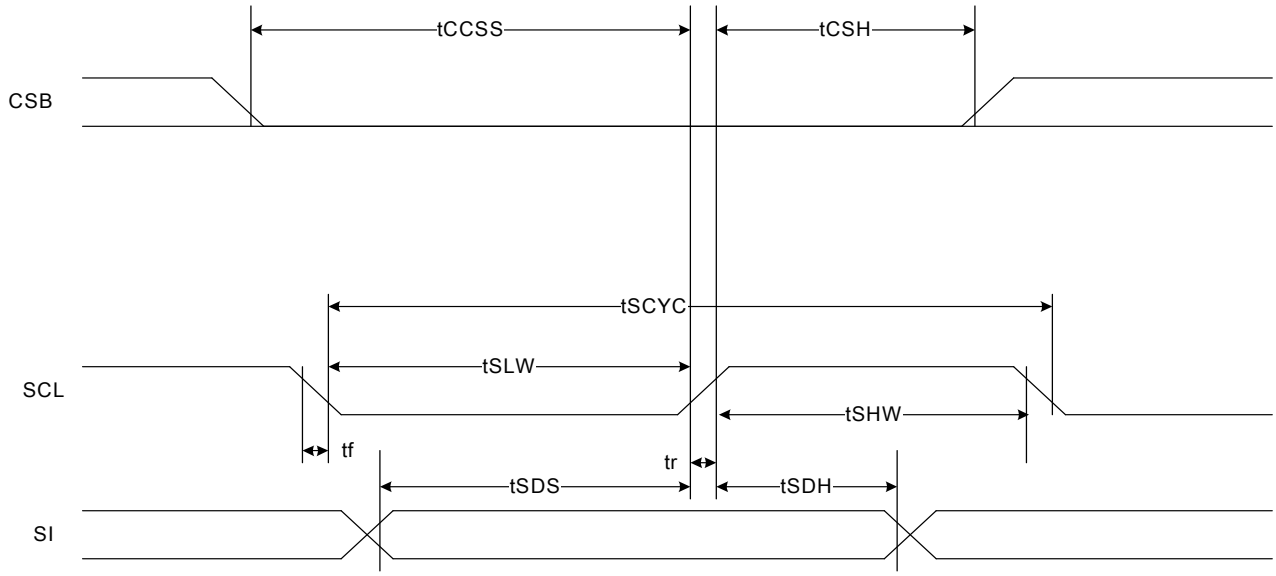


Fig. 34

(VDD1=1.8V~3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

SERIAL INTERFACE(IIC Interface)

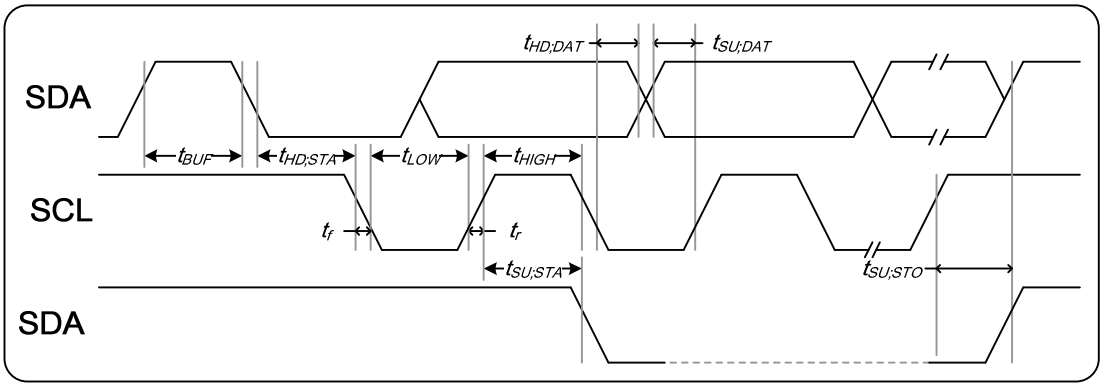


Fig. 35

(VDD1=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SDA	TSU;Data		100	-	ns
Data hold time	SDA	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SDA	TSU;SUA		0.6	-	us
Start condition hold time	SDA	THD;STA		0.6	-	us
Setup time for STOP ondition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and StART condition	SCL	TBUF		1.3		us

RESET TIMING

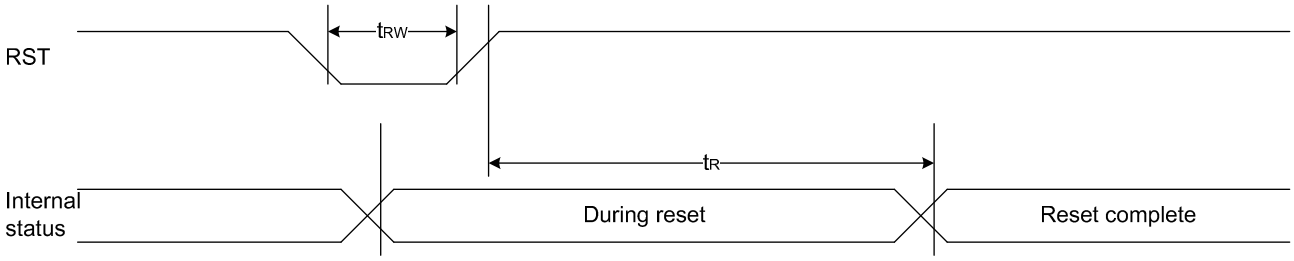


Fig. 36

(VDD1 = 1.8V~3.3V , Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		120	—	—	ms
Reset “L” pulse width	RST	tRW		2.0	—	—	us

POWER PAD CONNECT

The pinning of the ST7571 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 129 X 128 pixels.

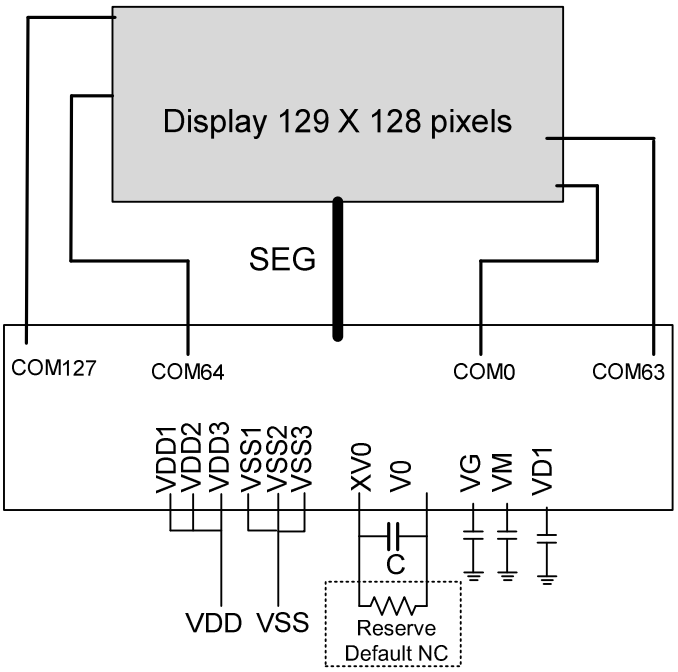


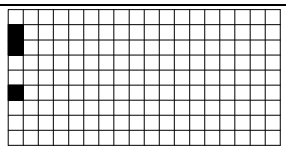
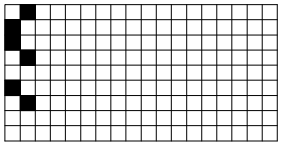
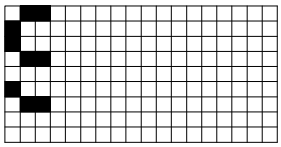
Fig. 37 Application diagram: internal charge pump is used and single V_{DD}

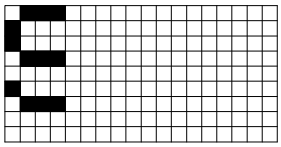
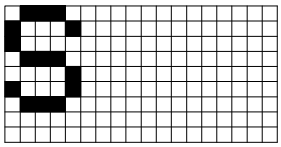
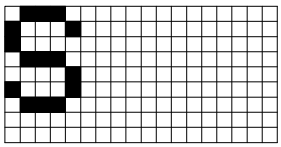
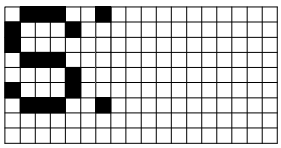
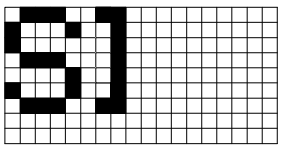
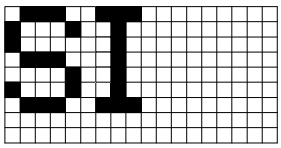
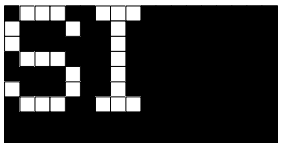
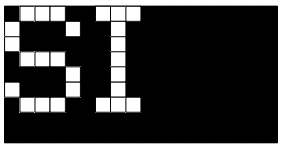
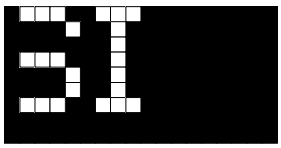
The required minimum value for the external capacitors in an application with the ST7571 are: C = 1uF.

Higher capacitor values are recommended for ripple reduction.

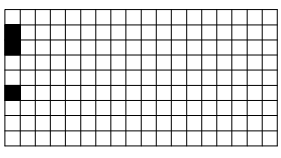
APPLICATION Program Example

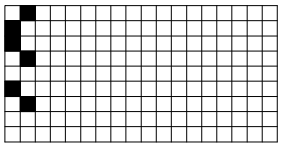
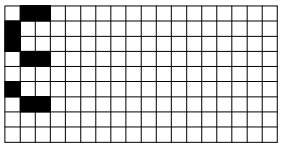
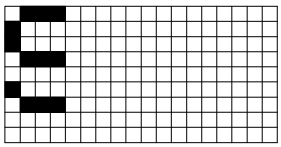
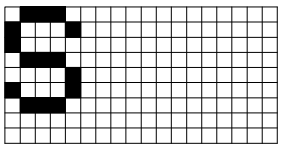
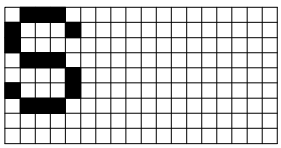
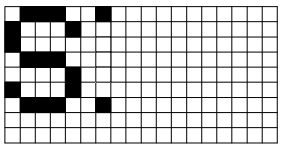
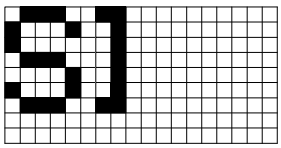
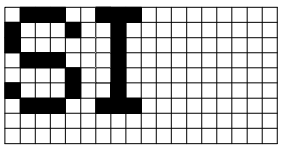
4-Gray programming example for ST7571

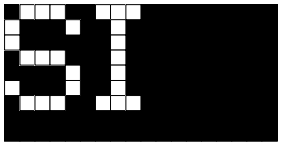
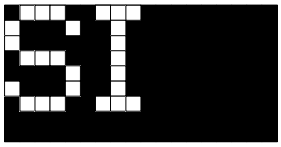
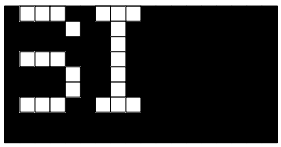
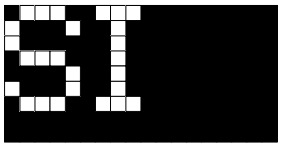
SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
0	Start		CSB IS going low.
1	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 0		Mode Set. FR[3:0] = 0000 BE= 1
2	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 1 0 1 1		OSC ON
3.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 R2 R1 R0		Set Ra/Rb Set R[2:0]
3.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0 1 0 x' x' Ev5 Ev4 Ev3 Ev2 Ev1 Ev0		Set EV Set Ev[5:0]
3.c	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 1 0 B2 B1 B0		Set Bias Set B[2:0]
4	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 0		Mode Set.
5.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 1 1 1 1		SET Power Control Booster ON Regulator ON Follower ON
5.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 1 1 1 1		Display control. Display on
6	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…
7	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
8	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.

9	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
10	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 1 0 0 1 0 1 0 0 1 1 0 0 1 0		Data Write.
11	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.
12	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
13	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.
14	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
15	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 0 1 1 1		Display Control. Set Reverse display mode REV=1
16	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0		Set column address of RAM. Set address to “00000000”. Y[7:0]=00000000 (Y0 default is 0)
17	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.

Programming example for ST7571(Use IIC Interface)

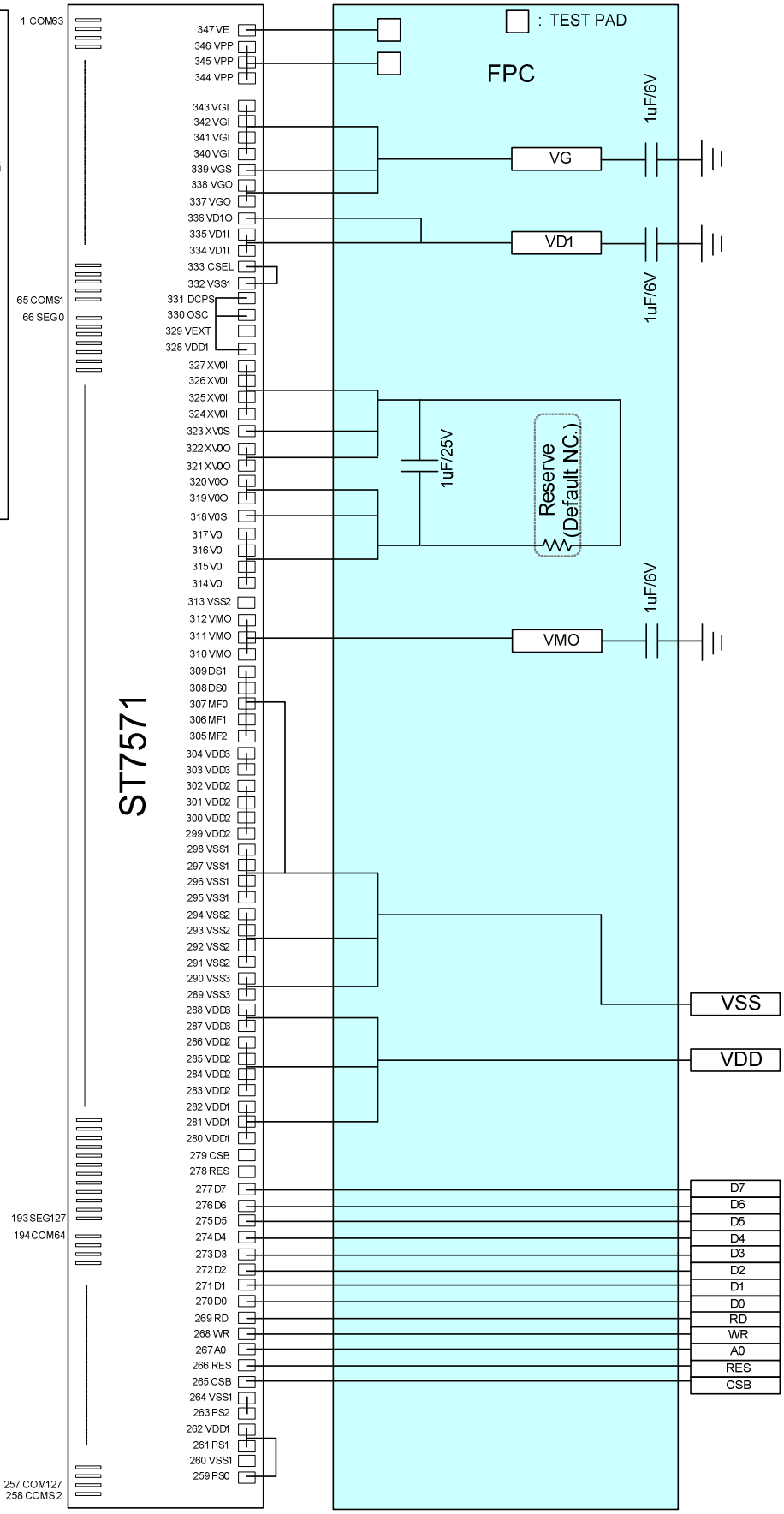
SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
1	IIC INTERFACE Start		
2	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
3	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0
4	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 1 0 x' 0		Mode Set. FR[3:0] = 0000 BE= 1
5	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 1 0 1 1		OSC ON
6.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 R2 R1 R0		Set Ra/Rb Set R[2:0]
6.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 1 x' x' Ev5 Ev4 Ev3 Ev2 Ev1 Ev0		Set EV Set Ev[5:0]
6.c	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 B2 B1 B0		Set Bias Set B[2:0]
7	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 x' 0		Mode Set.
8.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 1 1 1 1		SET Power Control Booster ON Regulator ON Follower ON
8.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 1 1 1 1		Display control. Display on
9	IIC INTERFACE Start		restart
10	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
11	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0		Control byte with clear Co bit and A0 set to logic 1
12	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 1 1 0 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…

13	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
14	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
15	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
16	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 0 0 1 0 0 0 1 1 0 0 1 0		Data Write.
17	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
18	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1		Data Write.
19	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.
20	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1		Data Write.
21	IIC INTERFACE start		restart
22	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
23	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0

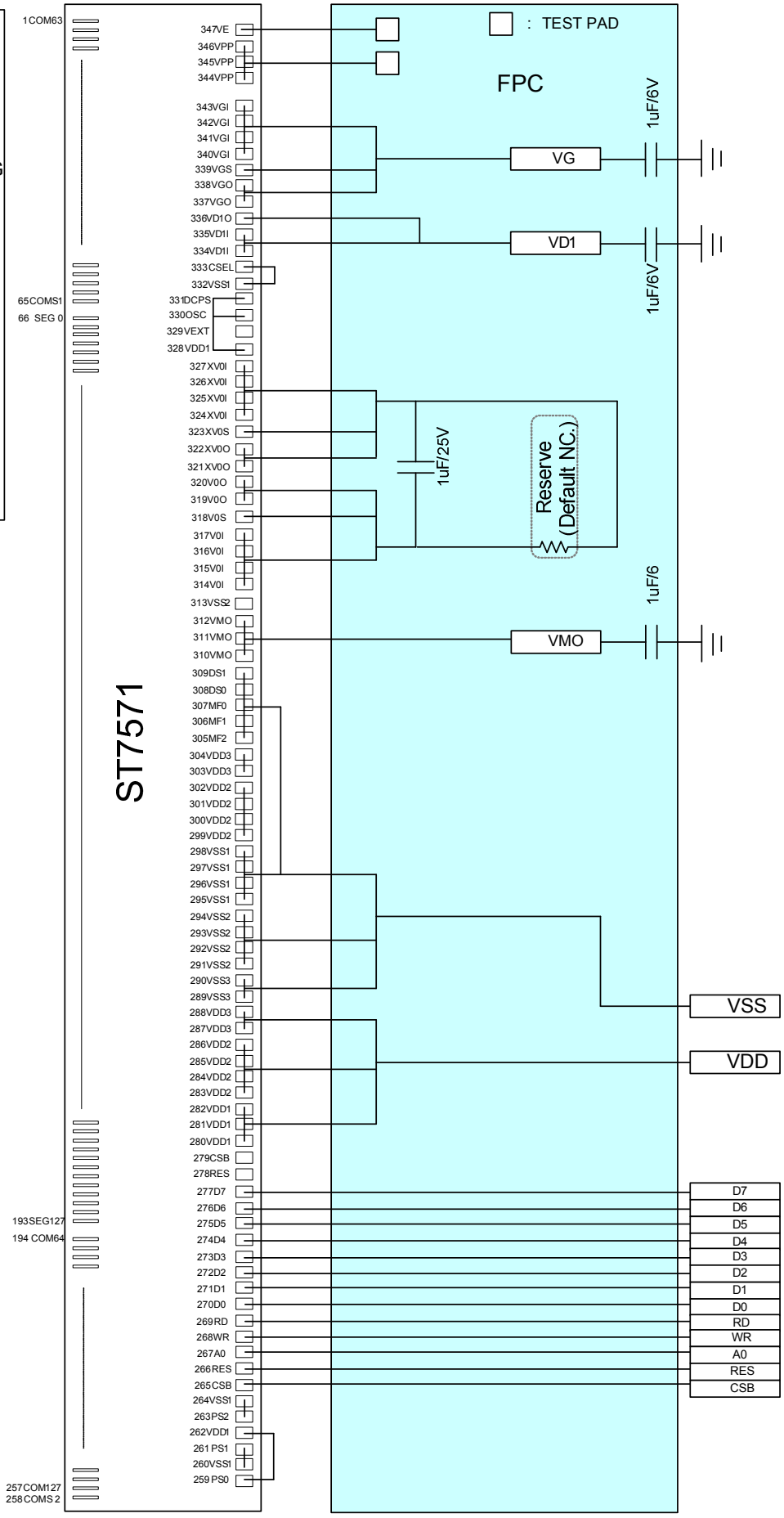
24	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 1 1		Display Control. Set Reverse display mode REV=1
25	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
26	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0		Set column address of RAM. Set address to “00000000”. Y[7:0]=00000000 (Y0 default is 00)
27	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 1 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 1
28	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
29	IIC INTERFACE start		restart
30	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
31	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
32	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Set X address of RAM. Set address to “0000000”.
33	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0

APPLICATION NOTES

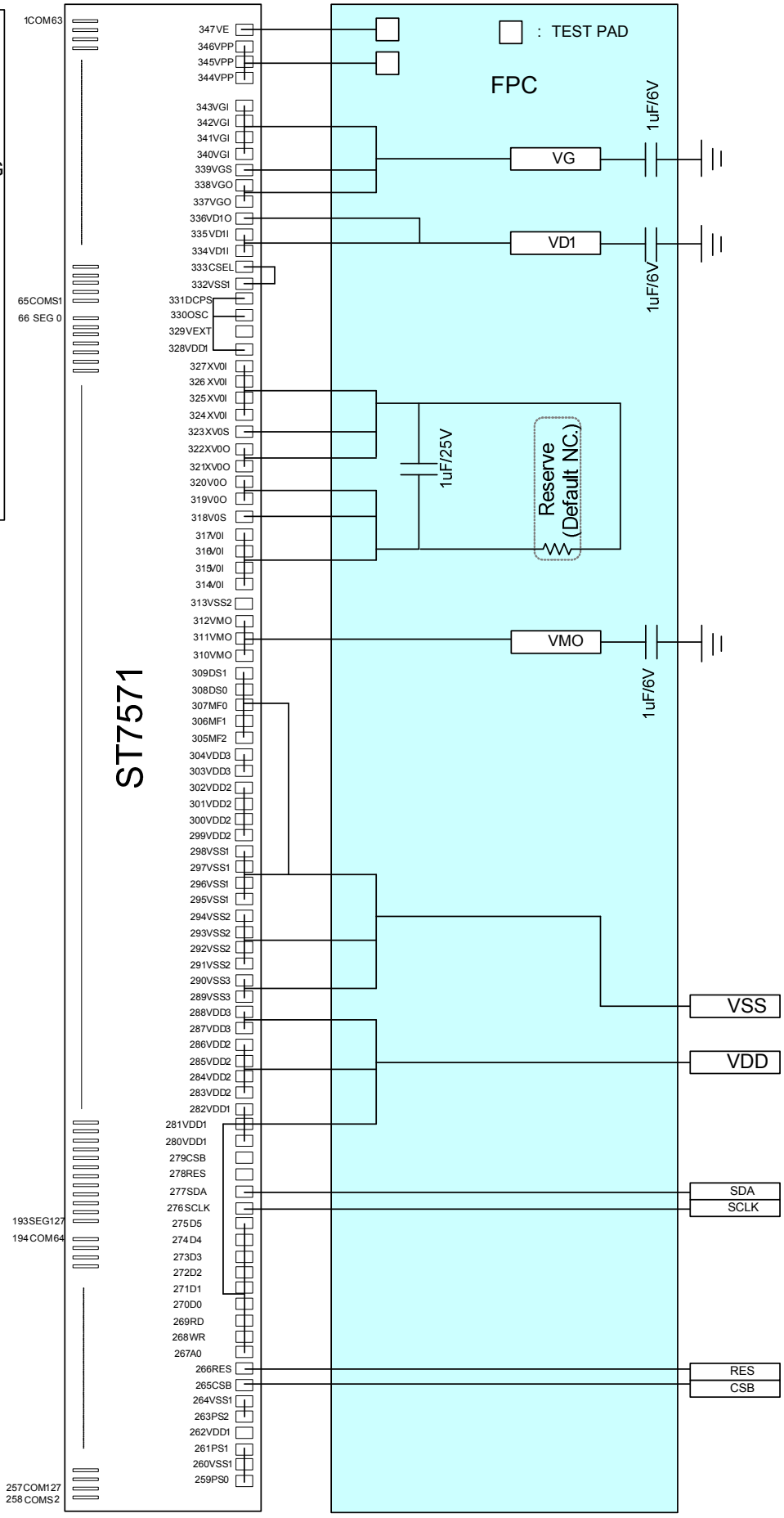
ST7571
Resolution:
129(128com+ICOM)*128SEG
Interface: 6800
PS0 : H
PS1 : H
PS2 : L
OSC: H
DCPS: L(VDD1>2.8V)
DCPS: H(VDD1<=2.8V)
CSEL: L
MF[2:0]: VDD1 or VSS1
DS[1:0]: VDD1 or VSS1



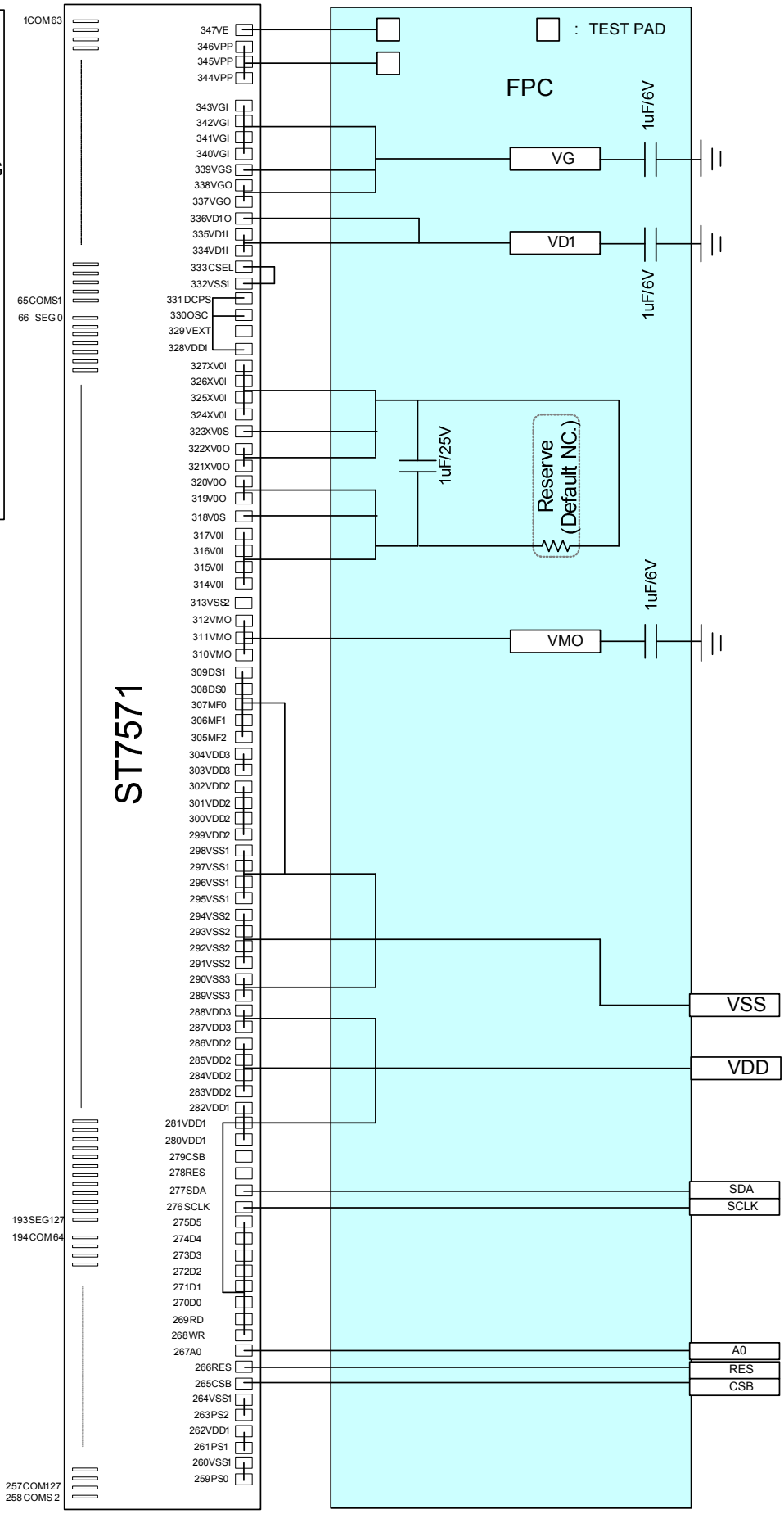
ST7571
Resolution
129(128com+ICOM)*128SEG
Interface 8080
PS0 :H
PS1 :L
PS2 :L
OSC:H
DCPS: L(VDD1>2.8V)
DCPS: H(VDD1<=2.8V)
CSEL:L
MF[2:0]: VDD1 or VSS1
DS[1:0]: VDD1 or VSS1



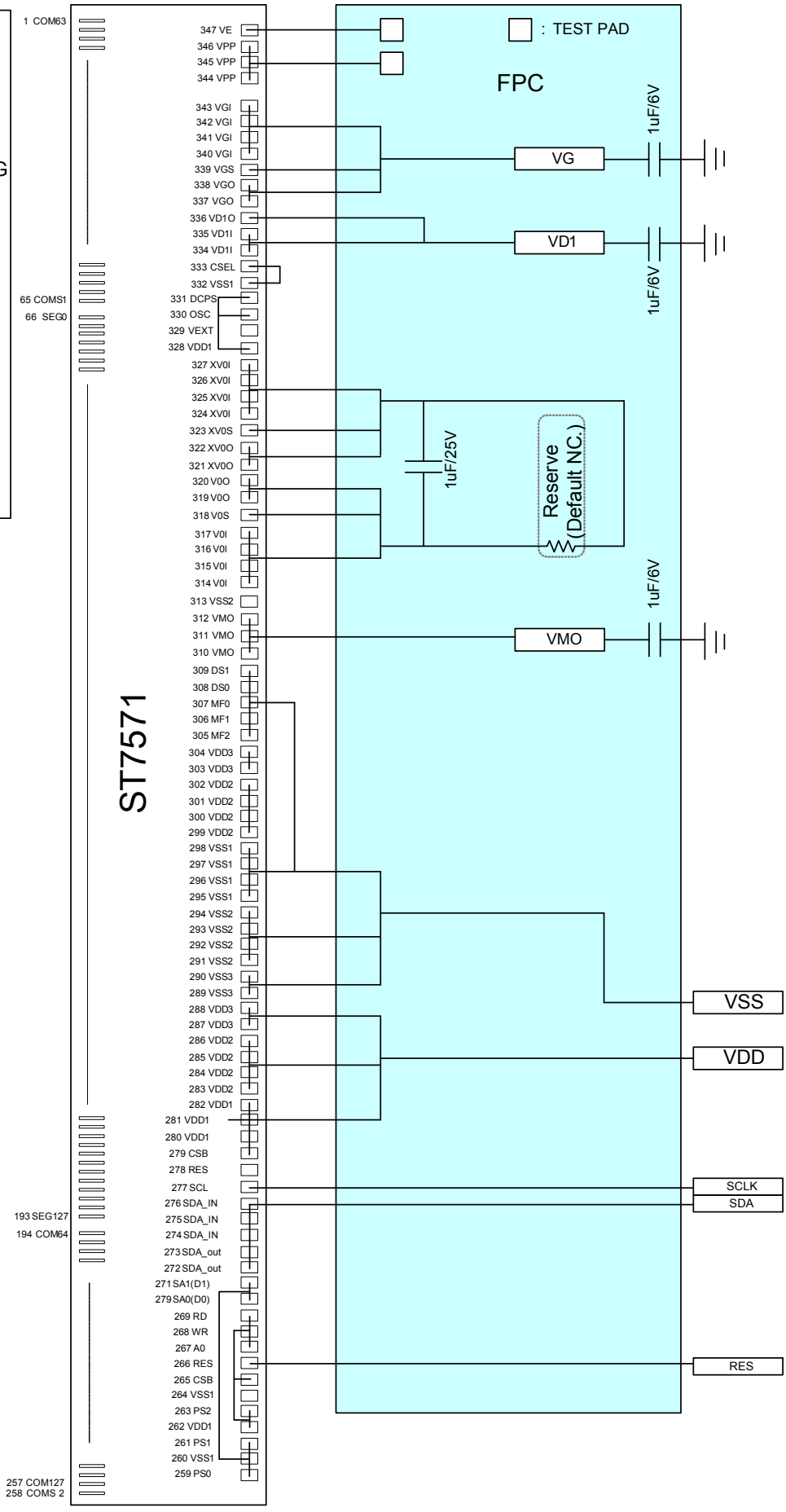
ST 7571
Resolution
129(128com+ICOM)*128SEG
Interface:3- SPI
PS0 :L
PS1 :L
PS2 :L
OSC:H
DCPS: L(VDD1>2.8V)
DCPS: H(VDD1<=2.8V)
CSEL:L
MF[2:0]: VDD1 or VSS1
DS[1:0]: VDD1 or VSS1



ST7571
Resolution
129(128com+ICOM)*128SEG
Interface:4- SPI
PS0 :L
PS1 :H
PS2 :L
OSC:H
DCPS: L(VDD1>2.8V)
DCPS: H(VDD1<=2.8V)
CSEL:L
MF[2:0]: VDD1 or VSS1
DS[1:0]: VDD1 or VSS1



ST7571
Resolution:
129(128com+ICOM)*128SEG
Interface: I2C
PS0 : L
PS1 : L
PS2 : H
OSC: H
DCPS: L (VDD1>2.8V)
DCPS: H (VDD1<=2.8V)
CSEL: L
MF[2:0]: VDD1 or VSS1
DS[1:0]: VDD1 or VSS1



ST7571 Specification Revision History		
Version	**Date**	**Description**
0.1	2007/02/08	1. Added Pad Arrangement 2. Added Pad Center Coordinates 3. Added Application notes
0.2	2007/3/15	1. Modified Pad Center Coordinates PAD No.351~354
0.3	2007/8/2	1. Modify the description about un-used pins of serial interface 2. Correct the VE pin status, when writing the EE. 3. Add EE writing flow.
0.4	2007/10/30	1. Remove some dummy commands 2. Add 2 test commands 3. Correct description for CSEL
1.0	2007/01/29	1. Remove TBD. 2. Add DCPS and COMMON reference circuit 3. Add some commands for burning EE in command table. 4. Modify the power consumption current for N-Line=1 condition. 5. Reserve read function