SSD1783B

Advance Information

132 RGB x 160 CSTN
LCD Segment / Common COLOR Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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1 General Description

SSD1783B is a single-chip CMOS color STN LCD driver with controller for dot-matrix graphic liquid crystal display system. SSD1783B consists of 556 high voltage driving output pins for driving maximum 132 RGB Segments, 160 Commons CSTN panel.

SSD1783B consists of 132 RGB x 168 x 18 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through 16-bit/8-bit 6800-series / 8080-series compatible Parallel Interface or 3-wires / 4-wires Serial Peripheral Interface by pins selection.

SSD1783B embeds On-Chip Oscillator, DC-DC Converter, bias divider so as to reduce the number of external component. With the advanced design, low power consumption, stable LCD operating voltage and flexible die package layout, SSD1783B is suitable for any portable battery-driven applications requiring long operation period with compact size.

2 FEATURES

- Power Supply: V_{DDIO} = 1.2V – V_{DD}
  V_{DD} = 2.4V – 3.6V
  V_{CI} = V_{DD} – 3.6V
- LCD Driving Output Voltage: 19V max
- Low Current Sleep Mode
- Maximum display size: 132 RGB columns by 160 rows.
- Display color support: 262K/65K/4K/256 color selectable, with preset/programmable color look up table (CLUT)
- 16-bit/8-bit 6800-series Parallel Interface, 16-bit/8-bit 8080-series Parallel Interface, 3-wires Serial Peripheral Interface and 4-wires Serial Peripheral Interface
- On-Chip (132 RGB) X (168) x 18 = 399168 bits Graphic Display Data RAM
- Column Re-mapping and RAM Page scan direction control
- Center Screen Scrolling, Top Screen Scrolling, Bottom Screen Scrolling and Whole Screen Scrolling
- 4X / 5X / 6X/ 7X On-Chip DC-DC Converter
- 64 Levels Internal Contrast Control
- Programmable LCD Driving Voltage Temperature Compensation Coefficients
- Programmable drive duty ratio: 1/32 to 1 /160
- Non-Volatile Memory (OTP) for calibration
- On-Chip 2-D Graphic Acceleration Engine featuring Line/Rectangle/Circle Drawing, Dim/Clear/Copy operation in Window mode.
- FRC or PWM Driving Scheme
- Interlace/progressive LCD common pins sequence selectable

3 ORDERING INFORMATION

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1783BZ	132x3 (396)	160	Gold Bump Die	Figure 2 on page 7	
SSD1783BU2R1	128x3 (384)	160	COF		

Table 1 - Ordering Information

4 BLOCK DIAGRAM

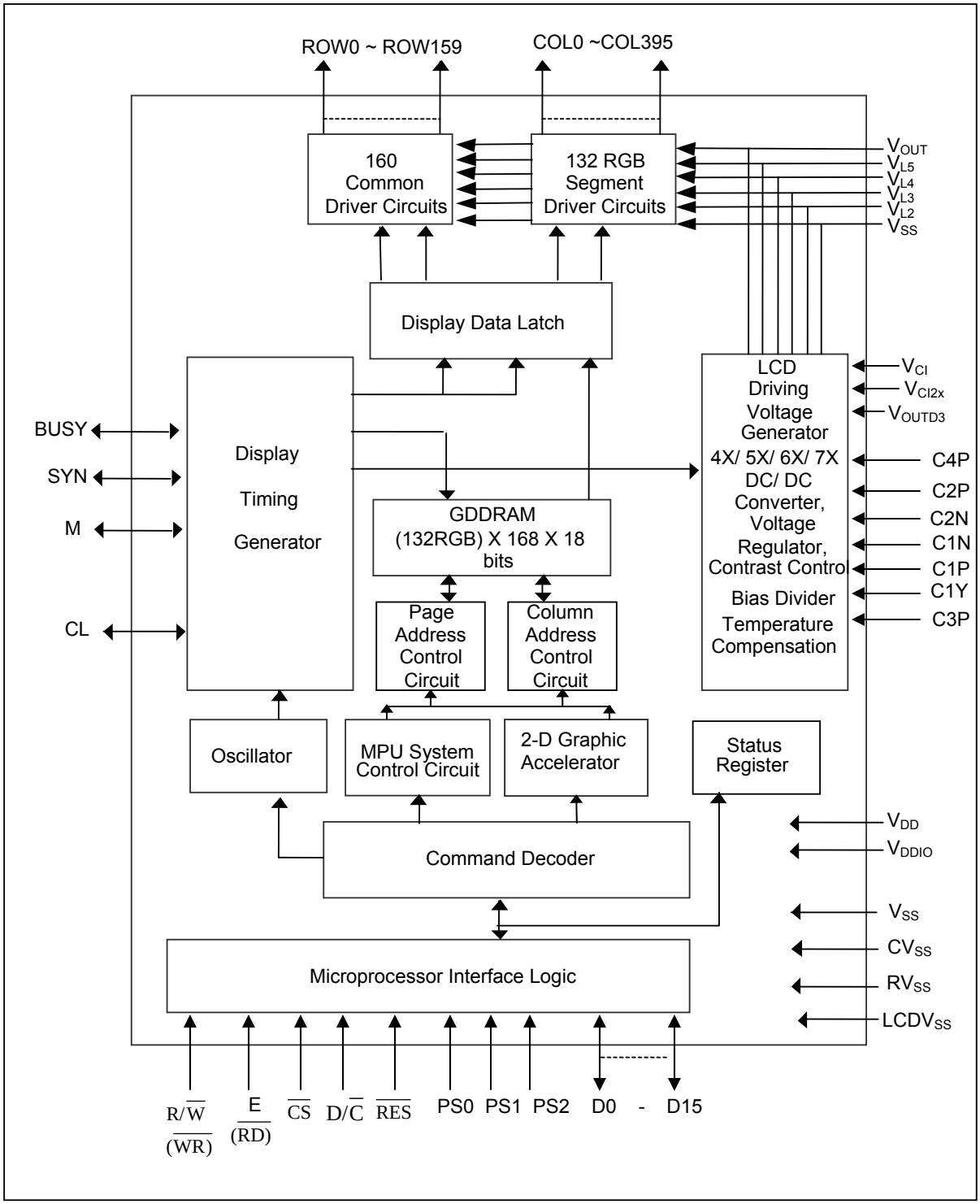
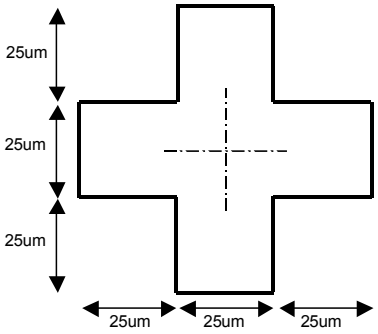
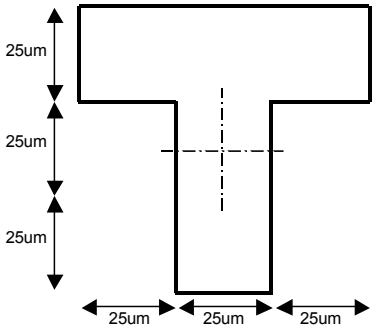
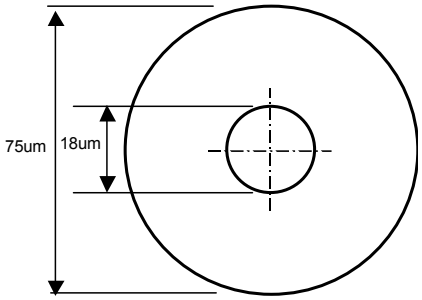


Figure 1 - SSD1783B Block Diagram

5 DIE PAD FLOOR PLAN







Note:
1. Diagram showing die face up
2. Coordinates are reference to die centre (in um)
3. All alignment keys do not contain gold bump

Die size: 22.10 x 1.96 sq mm
Die thickness: 457 +/- 25 um
Bump height: 15um (normal)
Bump co-planarity: <3um (within die)

Bump size:

PAD #	x (um)	y (um)
1-278	56	92
279	118	50
280-303	118	27
304	118	50
305-306	50	118
307-814	27	118
815-816	50	118
817	118	50
818-841	118	27
842	118	50

Figure 2 - SSD1783B Die Pad Floor Plan

Table 2 - SSD1783B Series Bump Die Pad Coordinates (Bump center)

Pad no.	Signal	x coor	y coor	Pad no.	Signal	x coor	y coor	Pad no.	Signal	x coor	y coor
1	DUMMY	-10842.40	-818.00	51	NC	-6752.55	-818.00	101	V_{OUT}	-2937.55	-818.00
2	DUMMY	-10491.25	-818.00	52	NC	-6676.25	-818.00	102	V_{OUT}	-2861.25	-818.00
3	DUMMY	-10414.95	-818.00	53	C1Y	-6599.95	-818.00	103	V_{OUT}	-2784.95	-818.00
4	C4P	-10338.65	-818.00	54	C1Y	-6523.65	-818.00	104	V_{OUT}	-2708.65	-818.00
5	C4P	-10262.35	-818.00	55	C1Y	-6447.35	-818.00	105	V_{OUT}	-2632.35	-818.00
6	C4P	-10186.05	-818.00	56	C1Y	-6371.05	-818.00	106	V_{OUT}	-2556.05	-818.00
7	C4P	-10109.75	-818.00	57	C1Y	-6294.75	-818.00	107	V_{OUT}	-2479.75	-818.00
8	C4P	-10033.45	-818.00	58	C1Y	-6218.45	-818.00	108	NC	-2403.45	-818.00
9	C4P	-9957.15	-818.00	59	C1Y	-6142.15	-818.00	109	NC	-2327.15	-818.00
10	C4P	-9880.85	-818.00	60	C1Y	-6065.85	-818.00	110	NC	-2250.85	-818.00
11	C4P	-9804.55	-818.00	61	C3P	-5989.55	-818.00	111	NC	-2174.55	-818.00
12	C2P	-9728.25	-818.00	62	C3P	-5913.25	-818.00	112	NC	-2098.25	-818.00
13	C2P	-9651.95	-818.00	63	C3P	-5836.95	-818.00	113	M	-2021.95	-818.00
14	C2P	-9575.65	-818.00	64	C3P	-5760.65	-818.00	114	SYN	-1945.65	-818.00
15	C2P	-9499.35	-818.00	65	C3P	-5684.35	-818.00	115	CL	-1869.35	-818.00
16	C2P	-9423.05	-818.00	66	C3P	-5608.05	-818.00	116	$\overline{RES}$	-1793.05	-818.00
17	C2P	-9346.75	-818.00	67	C3P	-5531.75	-818.00	117	D/ $\overline{C}$	-1716.75	-818.00
18	C2P	-9270.45	-818.00	68	C3P	-5455.45	-818.00	118	D/ $\overline{C}$	-1640.45	-818.00
19	C2P	-9194.15	-818.00	69	NC	-5379.15	-818.00	119	D/ $\overline{C}$	-1564.15	-818.00
20	C2N	-9117.85	-818.00	70	NC	-5302.85	-818.00	120	$\overline{CS}$	-1487.85	-818.00
21	C2N	-9041.55	-818.00	71	NC	-5226.55	-818.00	121	$\overline{CS}$	-1411.55	-818.00
22	C2N	-8965.25	-818.00	72	NC	-5150.25	-818.00	122	V_{SS}	-1335.25	-818.00
23	C2N	-8888.95	-818.00	73	NC	-5073.95	-818.00	123	PS2	-1258.95	-818.00
24	C2N	-8812.65	-818.00	74	NC	-4997.65	-818.00	124	V_{DD}	-1182.65	-818.00
25	C2N	-8736.35	-818.00	75	V_{OUTD3}	-4921.35	-818.00	125	PS1	-1106.35	-818.00
26	C2N	-8660.05	-818.00	76	V_{OUTD3}	-4845.05	-818.00	126	V_{SS}	-1030.05	-818.00
27	C2N	-8583.75	-818.00	77	V_{OUTD3}	-4768.75	-818.00	127	PS0	-953.75	-818.00
28	NC	-8507.45	-818.00	78	V_{OUTD3}	-4692.45	-818.00	128	V_{DD}	-877.45	-818.00
29	NC	-8431.15	-818.00	79	V_{OUTD3}	-4616.15	-818.00	129	V_{SS}	-801.15	-818.00
30	NC	-8354.85	-818.00	80	V_{OUTD3}	-4539.85	-818.00	130	R/ $\overline{W}$ ($\overline{WR}$)	-724.85	-818.00
31	NC	-8278.55	-818.00	81	V_{OUTD3}	-4463.55	-818.00	131	R/ $\overline{W}$ ($\overline{WR}$)	-648.55	-818.00
32	NC	-8202.25	-818.00	82	V_{OUTD3}	-4387.25	-818.00	132	E ($\overline{RD}$)	-572.25	-818.00
33	C1N	-8125.95	-818.00	83	V_{OUTD3}	-4310.95	-818.00	133	E ($\overline{RD}$)	-495.95	-818.00
34	C1N	-8049.65	-818.00	84	V_{OUTD3}	-4234.65	-818.00	134	V_{DD}	-419.65	-818.00
35	C1N	-7973.35	-818.00	85	V_{OUTD3}	-4158.35	-818.00	135	D0	-343.35	-818.00
36	C1N	-7897.05	-818.00	86	V_{OUTD3}	-4082.05	-818.00	136	D1	-267.05	-818.00
37	C1N	-7820.75	-818.00	87	V_{OUTD3}	-4005.75	-818.00	137	D2	-190.75	-818.00
38	C1N	-7744.45	-818.00	88	V_{SS}	-3929.45	-818.00	138	D3	-114.45	-818.00
39	C1N	-7668.15	-818.00	89	V_{SS}	-3853.15	-818.00	139	D4	-38.15	-818.00
40	C1N	-7591.85	-818.00	90	V_{SS}	-3776.85	-818.00	140	D5	38.15	-818.00
41	C1P	-7515.55	-818.00	91	V_{SS}	-3700.55	-818.00	141	D6 (SCK)	114.45	-818.00
42	C1P	-7439.25	-818.00	92	V_{SS}	-3624.25	-818.00	142	D7 (SDA)	190.75	-818.00
43	C1P	-7362.95	-818.00	93	V_{OUT}	-3547.95	-818.00	143	D8	267.05	-818.00
44	C1P	-7286.65	-818.00	94	V_{OUT}	-3471.65	-818.00	144	D9	343.35	-818.00
45	C1P	-7210.35	-818.00	95	V_{OUT}	-3395.35	-818.00	145	D10	419.65	-818.00
46	C1P	-7134.05	-818.00	96	V_{OUT}	-3319.05	-818.00	146	D11	495.95	-818.00
47	C1P	-7057.75	-818.00	97	V_{OUT}	-3242.75	-818.00	147	D12	572.25	-818.00
48	C1P	-6981.45	-818.00	98	V_{OUT}	-3166.45	-818.00	148	D13	648.55	-818.00
49	V_{SS}	-6905.15	-818.00	99	V_{OUT}	-3090.15	-818.00	149	D14	724.85	-818.00
50	NC	-6828.85	-818.00	100	V_{OUT}	-3013.85	-818.00	150	D15	801.15	-818.00

Pad no.	Signal	x coor	y coor	Pad no.	Signal	x coor	y coor	Pad no.	Signal	x coor	y coor
151	BUSY	877.45	-818.00	201	V_{DD}	4692.45	-818.00	251	V_{L2}	8507.45	-818.00
152	NC	953.75	-818.00	202	V_{DD}	4768.75	-818.00	252	V_{L2}	8583.75	-818.00
153	NC	1030.05	-818.00	203	V_{DD}	4845.05	-818.00	253	V_{L2}	8660.05	-818.00
154	NC	1106.35	-818.00	204	V_{DD}	4921.35	-818.00	254	V_{L2}	8736.35	-818.00
155	RV_{SS}	1182.65	-818.00	205	V_{DD}	4997.65	-818.00	255	V_{L2}	8812.65	-818.00
156	CV_{SS}	1258.95	-818.00	206	V_{DD}	5073.95	-818.00	256	V_{L3}	8888.95	-818.00
157	CV_{SS}	1335.25	-818.00	207	V_{DD}	5150.25	-818.00	257	V_{L3}	8965.25	-818.00
158	CV_{SS}	1411.55	-818.00	208	V_{DD}	5226.55	-818.00	258	V_{L3}	9041.55	-818.00
159	CV_{SS}	1487.85	-818.00	209	V_{DD}	5302.85	-818.00	259	V_{L3}	9117.85	-818.00
160	CV_{SS}	1564.15	-818.00	210	V_{DD}	5379.15	-818.00	260	V_{L3}	9194.15	-818.00
161	CV_{SS}	1640.45	-818.00	211	V_{DD}	5455.45	-818.00	261	V_{L3}	9270.45	-818.00
162	CV_{SS}	1716.75	-818.00	212	V_{DDIO}	5531.75	-818.00	262	V_{L4}	9346.75	-818.00
163	CV_{SS}	1793.05	-818.00	213	V_{DDIO}	5608.05	-818.00	263	V_{L4}	9423.05	-818.00
164	CV_{SS}	1869.35	-818.00	214	V_{CIX2}	5684.35	-818.00	264	V_{L4}	9499.35	-818.00
165	CV_{SS}	1945.65	-818.00	215	V_{CIX2}	5760.65	-818.00	265	V_{L4}	9575.65	-818.00
166	V_{SS}	2021.95	-818.00	216	V_{CIX2}	5836.95	-818.00	266	V_{L4}	9651.95	-818.00
167	V_{SS}	2098.25	-818.00	217	V_{CIX2}	5913.25	-818.00	267	V_{L4}	9728.25	-818.00
168	V_{SS}	2174.55	-818.00	218	V_{CIX2}	5989.55	-818.00	268	V_{L4}	9804.55	-818.00
169	V_{SS}	2250.85	-818.00	219	V_{CIX2}	6065.85	-818.00	269	V_{L4}	9880.85	-818.00
170	V_{SS}	2327.15	-818.00	220	V_{CIX2}	6142.15	-818.00	270	V_{L5}	9957.15	-818.00
171	V_{SS}	2403.45	-818.00	221	V_{CIX2}	6218.45	-818.00	271	V_{L5}	10033.45	-818.00
172	V_{SS}	2479.75	-818.00	222	V_{CIX2}	6294.75	-818.00	272	V_{L5}	10109.75	-818.00
173	V_{SS}	2556.05	-818.00	223	NC	6371.05	-818.00	273	V_{L5}	10186.05	-818.00
174	V_{SS}	2632.35	-818.00	224	V_{CI}	6447.35	-818.00	274	V_{L5}	10262.35	-818.00
175	V_{SS}	2708.65	-818.00	225	V_{CI}	6523.65	-818.00	275	NC	10338.65	-818.00
176	V_{SS}	2784.95	-818.00	226	V_{CI}	6599.95	-818.00	276	DUMMY	10414.95	-818.00
177	V_{SS}	2861.25	-818.00	227	V_{CI}	6676.25	-818.00	277	DUMMY	10491.25	-818.00
178	$LCDV_{SS}$	2937.55	-818.00	228	V_{CI}	6752.55	-818.00	278	DUMMY	10842.40	-818.00
179	$LCDV_{SS}$	3013.85	-818.00	229	V_{CI}	6828.85	-818.00				
180	$LCDV_{SS}$	3090.15	-818.00	230	V_{CI}	6905.15	-818.00				
181	$LCDV_{SS}$	3166.45	-818.00	231	V_{CI}	6981.45	-818.00				
182	$LCDV_{SS}$	3242.75	-818.00	232	V_{CI}	7057.75	-818.00				
183	$LCDV_{SS}$	3319.05	-818.00	233	V_{CI}	7134.05	-818.00				
184	$LCDV_{SS}$	3395.35	-818.00	234	NC	7210.35	-818.00				
185	$LCDV_{SS}$	3471.65	-818.00	235	NC	7286.65	-818.00				
186	$LCDV_{SS}$	3547.95	-818.00	236	NC	7362.95	-818.00				
187	$LCDV_{SS}$	3624.25	-818.00	237	NC	7439.25	-818.00				
188	$LCDV_{SS}$	3700.55	-818.00	238	NC	7515.55	-818.00				
189	$LCDV_{SS}$	3776.85	-818.00	239	NC	7591.85	-818.00				
190	$LCDV_{SS}$	3853.15	-818.00	240	NC	7668.15	-818.00				
191	V_{DD}	3929.45	-818.00	241	NC	7744.45	-818.00				
192	V_{DD}	4005.75	-818.00	242	V_{SS}	7820.75	-818.00				
193	V_{DD}	4082.05	-818.00	243	V_{SS}	7897.05	-818.00				
194	V_{DD}	4158.35	-818.00	244	V_{SS}	7973.35	-818.00				
195	V_{DD}	4234.65	-818.00	245	V_{SS}	8049.65	-818.00				
196	V_{DD}	4310.95	-818.00	246	V_{SS}	8125.95	-818.00				
197	V_{DD}	4387.25	-818.00	247	NC	8202.25	-818.00				
198	V_{DD}	4463.55	-818.00	248	V_{CIX2}	8278.55	-818.00				
199	V_{DD}	4539.85	-818.00	249	V_{L3}	8354.85	-818.00				
200	V_{DD}	4616.15	-818.00	250	V_{L2}	8431.15	-818.00				

Pad no.	Name	x coor	y coor
279	DUMMY	10812.40	-523.70
280	ROW0	10812.40	-470.40
281	ROW1	10812.40	-428.60
282	ROW2	10812.40	-386.80
283	ROW3	10812.40	-345.00
284	ROW4	10812.40	-303.20
285	ROW5	10812.40	-261.40
286	ROW6	10812.40	-219.60
287	ROW7	10812.40	-177.80
288	ROW8	10812.40	-136.00
289	ROW9	10812.40	-94.20
290	ROW10	10812.40	-52.40
291	ROW11	10812.40	-10.60
292	ROW12	10812.40	31.20
293	ROW13	10812.40	73.00
294	ROW14	10812.40	114.80
295	ROW15	10812.40	156.60
296	ROW16	10812.40	198.40
297	ROW17	10812.40	240.20
298	ROW18	10812.40	282.00
299	ROW19	10812.40	323.80
300	ROW20	10812.40	365.60
301	ROW21	10812.40	407.40
302	ROW22	10812.40	449.20
303	ROW23	10812.40	491.00
304	DUMMY	10812.40	544.30
305	DUMMY	10846.40	791.00
306	DUMMY	10733.20	791.00
307	ROW24	10679.90	791.00
308	ROW25	10638.10	791.00
309	ROW26	10596.30	791.00
310	ROW27	10554.50	791.00
311	ROW28	10512.70	791.00
312	ROW29	10470.90	791.00
313	ROW30	10429.10	791.00
314	ROW31	10387.30	791.00
315	ROW32	10345.50	791.00
316	ROW33	10303.70	791.00
317	ROW34	10261.90	791.00
318	ROW35	10220.10	791.00
319	ROW36	10178.30	791.00
320	ROW37	10136.50	791.00
321	ROW38	10094.70	791.00
322	ROW39	10052.90	791.00
323	ROW40	10011.10	791.00
324	ROW41	9969.30	791.00
325	ROW42	9927.50	791.00
326	ROW43	9885.70	791.00
327	ROW44	9843.90	791.00
328	ROW45	9802.10	791.00
329	ROW46	9760.30	791.00
330	ROW47	9718.50	791.00
331	ROW48	9676.70	791.00
332	ROW49	9634.90	791.00
333	ROW50	9593.10	791.00
334	ROW51	9551.30	791.00
335	ROW52	9509.50	791.00
336	ROW53	9467.70	791.00
337	ROW54	9425.90	791.00
338	ROW55	9384.10	791.00
339	ROW56	9342.30	791.00
340	ROW57	9300.50	791.00
341	ROW58	9258.70	791.00
342	ROW59	9216.90	791.00
343	ROW60	9175.10	791.00
344	ROW61	9133.30	791.00
345	ROW62	9091.50	791.00
346	ROW63	9049.70	791.00
347	ROW64	9007.90	791.00
348	ROW65	8966.10	791.00
349	ROW66	8924.30	791.00
350	ROW67	8882.50	791.00
351	ROW68	8840.70	791.00
352	ROW69	8798.90	791.00
353	ROW70	8757.10	791.00
354	ROW71	8715.30	791.00
355	ROW72	8673.50	791.00
356	ROW73	8631.70	791.00
357	ROW74	8589.90	791.00
358	ROW75	8548.10	791.00
359	ROW76	8506.30	791.00
360	ROW77	8464.50	791.00
361	ROW78	8422.70	791.00
362	ROW79	8380.90	791.00
363	COL395	SEG131	B	8255.50	791.00
364	COL394		G	8213.70	791.00
365	COL393		R	8171.90	791.00
366	COL392	SEG130	B	8130.10	791.00
367	COL391		G	8088.30	791.00
368	COL390		R	8046.50	791.00
369	COL389	SEG129	B	8004.70	791.00
370	COL388		G	7962.90	791.00
371	COL387		R	7921.10	791.00
372	COL386	SEG128	B	7879.30	791.00
373	COL385		G	7837.50	791.00
374	COL384		R	7795.70	791.00
375	COL383	SEG127	B	7753.90	791.00
376	COL382		G	7712.10	791.00
377	COL381		R	7670.30	791.00
378	COL380	SEG126	B	7628.50	791.00
379	COL379		G	7586.70	791.00
380	COL378		R	7544.90	791.00
381	COL377	SEG125	B	7503.10	791.00
382	COL376		G	7461.30	791.00
383	COL375		R	7419.50	791.00
384	COL374	SEG124	B	7377.70	791.00
385	COL373		G	7335.90	791.00
386	COL372		R	7294.10	791.00
387	COL371	SEG123	B	7252.30	791.00
388	COL370		G	7210.50	791.00
389	COL369		R	7168.70	791.00
390	COL368	SEG122	B	7126.90	791.00
391	COL367		G	7085.10	791.00
392	COL366		R	7043.30	791.00
393	COL365	SEG121	B	7001.50	791.00
394	COL364		G	6959.70	791.00
395	COL363		R	6917.90	791.00
396	COL362	SEG120	B	6876.10	791.00
397	COL361		G	6834.30	791.00
398	COL360		R	6792.50	791.00
399	COL359	SEG119	B	6750.70	791.00
400	COL358		G	6708.90	791.00
401	COL357		R	6667.10	791.00
402	COL356	SEG118	B	6625.30	791.00
403	COL355		G	6583.50	791.00
404	COL354		R	6541.70	791.00
405	COL353	SEG117	B	6499.90	791.00
406	COL352		G	6458.10	791.00
407	COL351		R	6416.30	791.00
408	COL350	SEG116	B	6374.50	791.00
409	COL349		G	6332.70	791.00
410	COL348		R	6290.90	791.00
411	COL347	SEG115	B	6249.10	791.00
412	COL346		G	6207.30	791.00
413	COL345		R	6165.50	791.00

Pad no.	Name	Signal	Color	x coor	y coor	Pad no.	Name	Signal	Color	x coor	y coor
414	COL344		B	6123.70	791.00	465	COL293		B	3991.90	791.00
415	COL343	SEG114	G	6081.90	791.00	466	COL292	SEG97	G	3950.10	791.00
416	COL342		R	6040.10	791.00	467	COL291		R	3908.30	791.00
417	COL341		B	5998.30	791.00	468	COL290		B	3866.50	791.00
418	COL340	SEG113	G	5956.50	791.00	469	COL289	SEG96	G	3824.70	791.00
419	COL339		R	5914.70	791.00	470	COL288		R	3782.90	791.00
420	COL338		B	5872.90	791.00	471	COL287		B	3741.10	791.00
421	COL337	SEG112	G	5831.10	791.00	472	COL286	SEG95	G	3699.30	791.00
422	COL336		R	5789.30	791.00	473	COL285		R	3657.50	791.00
423	COL335		B	5747.50	791.00	474	COL284		B	3615.70	791.00
424	COL334	SEG111	G	5705.70	791.00	475	COL283	SEG94	G	3573.90	791.00
425	COL333		R	5663.90	791.00	476	COL282		R	3532.10	791.00
426	COL332		B	5622.10	791.00	477	COL281		B	3490.30	791.00
427	COL331	SEG110	G	5580.30	791.00	478	COL280	SEG93	G	3448.50	791.00
428	COL330		R	5538.50	791.00	479	COL279		R	3406.70	791.00
429	COL329		B	5496.70	791.00	480	COL278		B	3364.90	791.00
430	COL328	SEG109	G	5454.90	791.00	481	COL277	SEG92	G	3323.10	791.00
431	COL327		R	5413.10	791.00	482	COL276		R	3281.30	791.00
432	COL326		B	5371.30	791.00	483	COL275		B	3239.50	791.00
433	COL325	SEG108	G	5329.50	791.00	484	COL274	SEG91	G	3197.70	791.00
434	COL324		R	5287.70	791.00	485	COL273		R	3155.90	791.00
435	COL323		B	5245.90	791.00	486	COL272		B	3114.10	791.00
436	COL322	SEG107	G	5204.10	791.00	487	COL271	SEG90	G	3072.30	791.00
437	COL321		R	5162.30	791.00	488	COL270		R	3030.50	791.00
438	COL320		B	5120.50	791.00	489	COL269		B	2988.70	791.00
439	COL319	SEG106	G	5078.70	791.00	490	COL268	SEG89	G	2946.90	791.00
440	COL318		R	5036.90	791.00	491	COL267		R	2905.10	791.00
441	COL317		B	4995.10	791.00	492	COL266		B	2863.30	791.00
442	COL316	SEG105	G	4953.30	791.00	493	COL265	SEG88	G	2821.50	791.00
443	COL315		R	4911.50	791.00	494	COL264		R	2779.70	791.00
444	COL314		B	4869.70	791.00	495	COL263		B	2737.90	791.00
445	COL313	SEG104	G	4827.90	791.00	496	COL262	SEG87	G	2696.10	791.00
446	COL312		R	4786.10	791.00	497	COL261		R	2654.30	791.00
447	COL311		B	4744.30	791.00	498	COL260		B	2612.50	791.00
448	COL310	SEG103	G	4702.50	791.00	499	COL259	SEG86	G	2570.70	791.00
449	COL309		R	4660.70	791.00	500	COL258		R	2528.90	791.00
450	COL308		B	4618.90	791.00	501	COL257		B	2487.10	791.00
451	COL307	SEG102	G	4577.10	791.00	502	COL256	SEG85	G	2445.30	791.00
452	COL306		R	4535.30	791.00	503	COL255		R	2403.50	791.00
453	COL305		B	4493.50	791.00	504	COL254		B	2361.70	791.00
454	COL304	SEG101	G	4451.70	791.00	505	COL253	SEG84	G	2319.90	791.00
455	COL303		R	4409.90	791.00	506	COL252		R	2278.10	791.00
456	COL302		B	4368.10	791.00	507	COL251		B	2236.30	791.00
457	COL301	SEG100	G	4326.30	791.00	508	COL250	SEG83	G	2194.50	791.00
458	COL300		R	4284.50	791.00	509	COL249		R	2152.70	791.00
459	COL299		B	4242.70	791.00	510	COL248		B	2110.90	791.00
460	COL298	SEG99	G	4200.90	791.00	511	COL247	SEG82	G	2069.10	791.00
461	COL297		R	4159.10	791.00	512	COL246		R	2027.30	791.00
462	COL296		B	4117.30	791.00	513	COL245		B	1985.50	791.00
463	COL295	SEG98	G	4075.50	791.00	514	COL244	SEG81	G	1943.70	791.00
464	COL294		R	4033.70	791.00	515	COL243		R	1901.90	791.00

Pad no.	Name	Signal	Color	x coor	y coor	Pad no.	Name	Signal	Color	x coor	y coor
516	COL242		B	1860.10	791.00	567	COL191		B	-271.70	791.00
517	COL241	SEG80	G	1818.30	791.00	568	COL190	SEG63	G	-313.50	791.00
518	COL240		R	1776.50	791.00	569	COL189		R	-355.30	791.00
519	COL239		B	1734.70	791.00	570	COL188		B	-397.10	791.00
520	COL238	SEG79	G	1692.90	791.00	571	COL187	SEG62	G	-438.90	791.00
521	COL237		R	1651.10	791.00	572	COL186		R	-480.70	791.00
522	COL236		B	1609.30	791.00	573	COL185		B	-522.50	791.00
523	COL235	SEG78	G	1567.50	791.00	574	COL184	SEG61	G	-564.30	791.00
524	COL234		R	1525.70	791.00	575	COL183		R	-606.10	791.00
525	COL233		B	1483.90	791.00	576	COL182		B	-647.90	791.00
526	COL232	SEG77	G	1442.10	791.00	577	COL181	SEG60	G	-689.70	791.00
527	COL231		R	1400.30	791.00	578	COL180		R	-731.50	791.00
528	COL230		B	1358.50	791.00	579	COL179		B	-773.30	791.00
529	COL229	SEG76	G	1316.70	791.00	580	COL178	SEG59	G	-815.10	791.00
530	COL228		R	1274.90	791.00	581	COL177		R	-856.90	791.00
531	COL227		B	1233.10	791.00	582	COL176		B	-898.70	791.00
532	COL226	SEG75	G	1191.30	791.00	583	COL175	SEG58	G	-940.50	791.00
533	COL225		R	1149.50	791.00	584	COL174		R	-982.30	791.00
534	COL224		B	1107.70	791.00	585	COL173		B	-1024.10	791.00
535	COL223	SEG74	G	1065.90	791.00	586	COL172	SEG57	G	-1065.90	791.00
536	COL222		R	1024.10	791.00	587	COL171		R	-1107.70	791.00
537	COL221		B	982.30	791.00	588	COL170		B	-1149.50	791.00
538	COL220	SEG73	G	940.50	791.00	589	COL169	SEG56	G	-1191.30	791.00
539	COL219		R	898.70	791.00	590	COL168		R	-1233.10	791.00
540	COL218		B	856.90	791.00	591	COL167		B	-1274.90	791.00
541	COL217	SEG72	G	815.10	791.00	592	COL166	SEG55	G	-1316.70	791.00
542	COL216		R	773.30	791.00	593	COL165		R	-1358.50	791.00
543	COL215		B	731.50	791.00	594	COL164		B	-1400.30	791.00
544	COL214	SEG71	G	689.70	791.00	595	COL163	SEG54	G	-1442.10	791.00
545	COL213		R	647.90	791.00	596	COL162		R	-1483.90	791.00
546	COL212		B	606.10	791.00	597	COL161		B	-1525.70	791.00
547	COL211	SEG70	G	564.30	791.00	598	COL160	SEG53	G	-1567.50	791.00
548	COL210		R	522.50	791.00	599	COL159		R	-1609.30	791.00
549	COL209		B	480.70	791.00	600	COL158		B	-1651.10	791.00
550	COL208	SEG69	G	438.90	791.00	601	COL157	SEG52	G	-1692.90	791.00
551	COL207		R	397.10	791.00	602	COL156		R	-1734.70	791.00
552	COL206		B	355.30	791.00	603	COL155		B	-1776.50	791.00
553	COL205	SEG68	G	313.50	791.00	604	COL154	SEG51	G	-1818.30	791.00
554	COL204		R	271.70	791.00	605	COL153		R	-1860.10	791.00
555	COL203		B	229.90	791.00	606	COL152		B	-1901.90	791.00
556	COL202	SEG67	G	188.10	791.00	607	COL151	SEG50	G	-1943.70	791.00
557	COL201		R	146.30	791.00	608	COL150		R	-1985.50	791.00
558	COL200		B	104.50	791.00	609	COL149		B	-2027.30	791.00
559	COL199	SEG66	G	62.70	791.00	610	COL148	SEG49	G	-2069.10	791.00
560	COL198		R	20.90	791.00	611	COL147		R	-2110.90	791.00
561	COL197		B	-20.90	791.00	612	COL146		B	-2152.70	791.00
562	COL196	SEG65	G	-62.70	791.00	613	COL145	SEG48	G	-2194.50	791.00
563	COL195		R	-104.50	791.00	614	COL144		R	-2236.30	791.00
564	COL194		B	-146.30	791.00	615	COL143		B	-2278.10	791.00
565	COL193	SEG64	G	-188.10	791.00	616	COL142	SEG47	G	-2319.90	791.00
566	COL192		R	-229.90	791.00	617	COL141		R	-2361.70	791.00

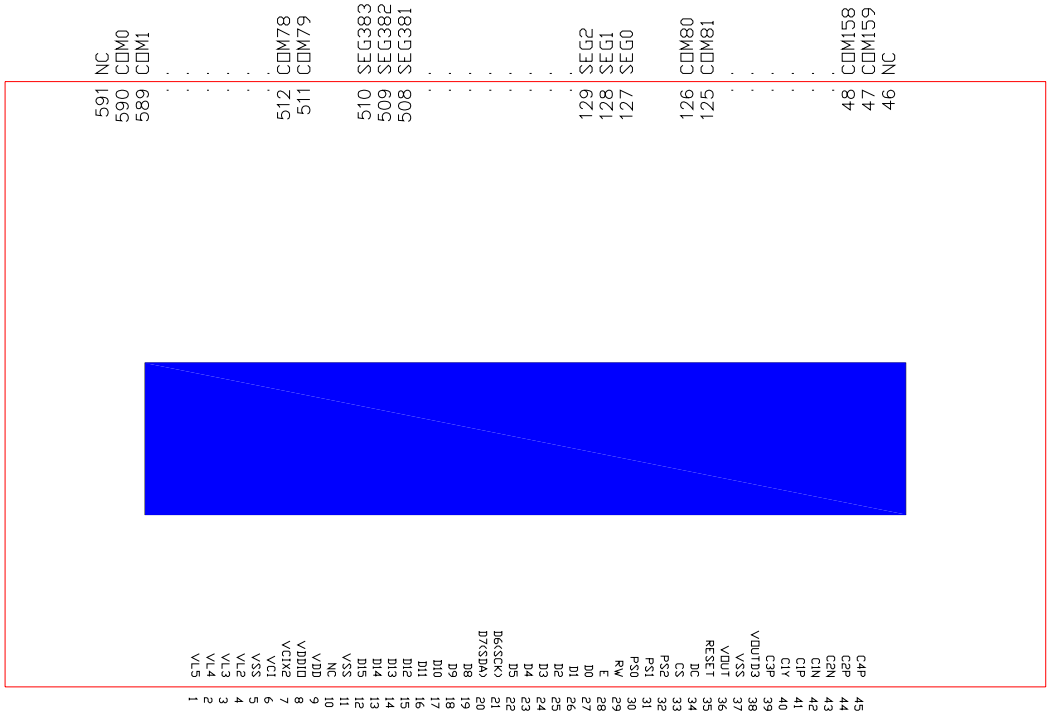
Pad no.	Name	Signal	Color	x coor	y coor	Pad no.	Name	Signal	Color	x coor	y coor
618	COL140	SEG46	B	-2403.50	791.00	669	COL89	SEG29	B	-4535.30	791.00
619	COL139		G	-2445.30	791.00	670	COL88		G	-4577.10	791.00
620	COL138		R	-2487.10	791.00	671	COL87		R	-4618.90	791.00
621	COL137	SEG45	B	-2528.90	791.00	672	COL86	SEG28	B	-4660.70	791.00
622	COL136		G	-2570.70	791.00	673	COL85		G	-4702.50	791.00
623	COL135		R	-2612.50	791.00	674	COL84		R	-4744.30	791.00
624	COL134	SEG44	B	-2654.30	791.00	675	COL83	SEG27	B	-4786.10	791.00
625	COL133		G	-2696.10	791.00	676	COL82		G	-4827.90	791.00
626	COL132		R	-2737.90	791.00	677	COL81		R	-4869.70	791.00
627	COL131	SEG43	B	-2779.70	791.00	678	COL80	SEG26	B	-4911.50	791.00
628	COL130		G	-2821.50	791.00	679	COL79		G	-4953.30	791.00
629	COL129		R	-2863.30	791.00	680	COL78		R	-4995.10	791.00
630	COL128	SEG42	B	-2905.10	791.00	681	COL77	SEG25	B	-5036.90	791.00
631	COL127		G	-2946.90	791.00	682	COL76		G	-5078.70	791.00
632	COL126		R	-2988.70	791.00	683	COL75		R	-5120.50	791.00
633	COL125	SEG41	B	-3030.50	791.00	684	COL74	SEG24	B	-5162.30	791.00
634	COL124		G	-3072.30	791.00	685	COL73		G	-5204.10	791.00
635	COL123		R	-3114.10	791.00	686	COL72		R	-5245.90	791.00
636	COL122	SEG40	B	-3155.90	791.00	687	COL71	SEG23	B	-5287.70	791.00
637	COL121		G	-3197.70	791.00	688	COL70		G	-5329.50	791.00
638	COL120		R	-3239.50	791.00	689	COL69		R	-5371.30	791.00
639	COL119	SEG39	B	-3281.30	791.00	690	COL68	SEG22	B	-5413.10	791.00
640	COL118		G	-3323.10	791.00	691	COL67		G	-5454.90	791.00
641	COL117		R	-3364.90	791.00	692	COL66		R	-5496.70	791.00
642	COL116	SEG38	B	-3406.70	791.00	693	COL65	SEG21	B	-5538.50	791.00
643	COL115		G	-3448.50	791.00	694	COL64		G	-5580.30	791.00
644	COL114		R	-3490.30	791.00	695	COL63		R	-5622.10	791.00
645	COL113	SEG37	B	-3532.10	791.00	696	COL62	SEG20	B	-5663.90	791.00
646	COL112		G	-3573.90	791.00	697	COL61		G	-5705.70	791.00
647	COL111		R	-3615.70	791.00	698	COL60		R	-5747.50	791.00
648	COL110	SEG36	B	-3657.50	791.00	699	COL59	SEG19	B	-5789.30	791.00
649	COL109		G	-3699.30	791.00	700	COL58		G	-5831.10	791.00
650	COL108		R	-3741.10	791.00	701	COL57		R	-5872.90	791.00
651	COL107	SEG35	B	-3782.90	791.00	702	COL56	SEG18	B	-5914.70	791.00
652	COL106		G	-3824.70	791.00	703	COL55		G	-5956.50	791.00
653	COL105		R	-3866.50	791.00	704	COL54		R	-5998.30	791.00
654	COL104	SEG34	B	-3908.30	791.00	705	COL53	SEG17	B	-6040.10	791.00
655	COL103		G	-3950.10	791.00	706	COL52		G	-6081.90	791.00
656	COL102		R	-3991.90	791.00	707	COL51		R	-6123.70	791.00
657	COL101	SEG33	B	-4033.70	791.00	708	COL50	SEG16	B	-6165.50	791.00
658	COL100		G	-4075.50	791.00	709	COL49		G	-6207.30	791.00
659	COL99		R	-4117.30	791.00	710	COL48		R	-6249.10	791.00
660	COL98	SEG32	B	-4159.10	791.00	711	COL47	SEG15	B	-6290.90	791.00
661	COL97		G	-4200.90	791.00	712	COL46		G	-6332.70	791.00
662	COL96		R	-4242.70	791.00	713	COL45		R	-6374.50	791.00
663	COL95	SEG31	B	-4284.50	791.00	714	COL44	SEG14	B	-6416.30	791.00
664	COL94		G	-4326.30	791.00	715	COL43		G	-6458.10	791.00
665	COL93		R	-4368.10	791.00	716	COL42		R	-6499.90	791.00
666	COL92	SEG30	B	-4409.90	791.00	717	COL41	SEG13	B	-6541.70	791.00
667	COL91		G	-4451.70	791.00	718	COL40		G	-6583.50	791.00
668	COL90		R	-4493.50	791.00	719	COL39		R	-6625.30	791.00

Pad no.	Name	Signal	Color	x coor	y coor
720	COL38	SEG12	B	-6667.10	791.00
721	COL37		G	-6708.90	791.00
722	COL36		R	-6750.70	791.00
723	COL35	SEG11	B	-6792.50	791.00
724	COL34		G	-6834.30	791.00
725	COL33		R	-6876.10	791.00
726	COL32	SEG10	B	-6917.90	791.00
727	COL31		G	-6959.70	791.00
728	COL30		R	-7001.50	791.00
729	COL29	SEG9	B	-7043.30	791.00
730	COL28		G	-7085.10	791.00
731	COL27		R	-7126.90	791.00
732	COL26	SEG8	B	-7168.70	791.00
733	COL25		G	-7210.50	791.00
734	COL24		R	-7252.30	791.00
735	COL23	SEG7	B	-7294.10	791.00
736	COL22		G	-7335.90	791.00
737	COL21		R	-7377.70	791.00
738	COL20	SEG6	B	-7419.50	791.00
739	COL19		G	-7461.30	791.00
740	COL18		R	-7503.10	791.00
741	COL17	SEG5	B	-7544.90	791.00
742	COL16		G	-7586.70	791.00
743	COL15		R	-7628.50	791.00
744	COL14	SEG4	B	-7670.30	791.00
745	COL13		G	-7712.10	791.00
746	COL12		R	-7753.90	791.00
747	COL11	SEG3	B	-7795.70	791.00
748	COL10		G	-7837.50	791.00
749	COL9		R	-7879.30	791.00
750	COL8	SEG2	B	-7921.10	791.00
751	COL7		G	-7962.90	791.00
752	COL6		R	-8004.70	791.00
753	COL5	SEG1	B	-8046.50	791.00
754	COL4		G	-8088.30	791.00
755	COL3		R	-8130.10	791.00
756	COL2	SEG0	B	-8171.90	791.00
757	COL1		G	-8213.70	791.00
758	COL0		R	-8255.50	791.00

Pad no.	Name	x coor	y coor
759	ROW80	-8380.90	791.00
760	ROW81	-8422.70	791.00
761	ROW82	-8464.50	791.00
762	ROW83	-8506.30	791.00
763	ROW84	-8548.10	791.00
764	ROW85	-8589.90	791.00
765	ROW86	-8631.70	791.00
766	ROW87	-8673.50	791.00
767	ROW88	-8715.30	791.00
768	ROW89	-8757.10	791.00
769	ROW90	-8798.90	791.00
770	ROW91	-8840.70	791.00
771	ROW92	-8882.50	791.00
772	ROW93	-8924.30	791.00
773	ROW94	-8966.10	791.00
774	ROW95	-9007.90	791.00
775	ROW96	-9049.70	791.00
776	ROW97	-9091.50	791.00
777	ROW98	-9133.30	791.00
778	ROW99	-9175.10	791.00
779	ROW100	-9216.90	791.00
780	ROW101	-9258.70	791.00
781	ROW102	-9300.50	791.00
782	ROW103	-9342.30	791.00
783	ROW104	-9384.10	791.00
784	ROW105	-9425.90	791.00
785	ROW106	-9467.70	791.00
786	ROW107	-9509.50	791.00
787	ROW108	-9551.30	791.00
788	ROW109	-9593.10	791.00
789	ROW110	-9634.90	791.00
790	ROW111	-9676.70	791.00
791	ROW112	-9718.50	791.00
792	ROW113	-9760.30	791.00
793	ROW114	-9802.10	791.00
794	ROW115	-9843.90	791.00
795	ROW116	-9885.70	791.00
796	ROW117	-9927.50	791.00
797	ROW118	-9969.30	791.00
798	ROW119	-10011.10	791.00
799	ROW120	-10052.90	791.00
800	ROW121	-10094.70	791.00
801	ROW122	-10136.50	791.00
802	ROW123	-10178.30	791.00
803	ROW124	-10220.10	791.00
804	ROW125	-10261.90	791.00
805	ROW126	-10303.70	791.00
806	ROW127	-10345.50	791.00
807	ROW128	-10387.30	791.00
808	ROW129	-10429.10	791.00

Pad no.	Name	x coor	y coor
809	ROW130	-10470.90	791.00
810	ROW131	-10512.70	791.00
811	ROW132	-10554.50	791.00
812	ROW133	-10596.30	791.00
813	ROW134	-10638.10	791.00
814	ROW135	-10679.90	791.00
815	DUMMY	-10733.20	791.00
816	DUMMY	-10846.40	791.00
817	DUMMY	-10812.40	544.30
818	ROW136	-10812.40	491.00
819	ROW137	-10812.40	449.20
820	ROW138	-10812.40	407.40
821	ROW139	-10812.40	365.60
822	ROW140	-10812.40	323.80
823	ROW141	-10812.40	282.00
824	ROW142	-10812.40	240.20
825	ROW143	-10812.40	198.40
826	ROW144	-10812.40	156.60
827	ROW145	-10812.40	114.80
828	ROW146	-10812.40	73.00
829	ROW147	-10812.40	31.20
830	ROW148	-10812.40	-10.60
831	ROW149	-10812.40	-52.40
832	ROW150	-10812.40	-94.20
833	ROW151	-10812.40	-136.00
834	ROW152	-10812.40	-177.80
835	ROW153	-10812.40	-219.60
836	ROW154	-10812.40	-261.40
837	ROW155	-10812.40	-303.20
838	ROW156	-10812.40	-345.00
839	ROW157	-10812.40	-386.80
840	ROW158	-10812.40	-428.60
841	ROW159	-10812.40	-470.40
842	DUMMY	-10812.40	-523.70

6 SSD1783BU2 COF Pin Assignment (Copper View)



7 PIN DESCRIPTION

7.1 $\overline{CS}$

This pin is the chip selection input. The chip is enabled for MCU communication only when $\overline{CS}$ is pulled low.

7.2 $\overline{RES}$

This pin is the reset signal input. Initialization of the chip is started once the reset pin is pulled low. The minimum pulse width for reset sequence is 10us.

7.3 D/$\overline{C}$

This pin is Data/Command control pin. When the pin is pulled high, the input at D7-D0 is treated as display data. When the pin is pulled low, the input at D7-D0 will be transferred to the command register.

7.4 R / $\overline{W}$ ($\overline{WR}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as Read/Write (R / $\overline{W}$) selection input. Read mode will be carried out when this pin is pulled high and write mode when this pin is pulled low.

When 8080 interface mode is selected, this pin is the Write ($\overline{WR}$) control signal input. Data write operation is initiated when this pin is pulled low and the chip is selected.

7.5 E ($\overline{RD}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/ write operation is initiated when this pin is pulled high and the chip is selected.

When 8080 interface mode is selected, this pin is the Read ($\overline{RD}$) control signal input. Data read operation is initiated when this pin is pulled low and the chip is selected.

7.6 PS0 – PS2

These pins are the bus interface mode selection input. Different bus interface can be selected changing the setting of these pins.

PS2	PS1	PS0	MPU Interface
H	H	H	16-bit 8080 parallel interface
H	H	L	8-bit 8080 parallel interface
H	L	L	16-bit 6800 parallel interface
L	H	H	8-bit 6800 parallel interface
L	L	H	3-lines serial peripheral interface (SPI)
L	L	L	4-lines serial peripheral interface (SPI)

Table 3 - Bus interface mode selection by PS2-PS0

Note1: For serial applications, D0 – D5, D8 – D15, R / $\overline{W}$ ($\overline{WR}$), E($\overline{RD}$) are recommended to connect V_{DD}.
Note2: Read back operation is only available in parallel mode

7.7 D0-D15

These pins are the 16-bit bi-directional data bus in parallel interface mode. D15 is the MSB while D0 is the LSB. In serial mode, D7 is the serial data input SDA and D6 is the serial clock input SCK.

7.8 V_{DD}

This pin is the system power supply pin of the logic block.

7.9 V_{DDIO}

This pin is the system power supply pin of IO buffer. Please refer to Page 66 for connection example.

7.10 V_{CI}

This pin is the reference voltage input for internal DC-DC converter. The DC-DC converter output is equal to the multiple factor (4X, 5X, 6X or 7X) times V_{CI} with respect to V_{SS}.
Note: Voltage at this input pin must be larger than or equal to V_{DD}. ($V_{CI} \geq V_{DD}$)

7.11 V_{CIX2}

This pin is a voltage reference output that is equal to 2x V_{CI}.

7.12 V_{SS}

This pin is the ground of logic.

7.13 RV_{SS}

This pin is the ground of Vref where Vref is the reference voltage of internal regulator.

7.14 CV_{SS}

This pin is the ground of analog.

7.15 $LCDV_{SS}$

This pin is the ground of segment and common output pins.

7.16 V_{OUT}

This is the most positive voltage supply pin of the chip. It is generated by the internal regulator. This voltage level is used for internal referencing only and the voltage level at V_{OUT} pin is not used for driving external circuitry.

7.17 V_{OUTD3}

This pin is a voltage reference output.

7.18 V_{L5}, V_{L4}, V_{L3} and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$

	1 : a bias
V_{L5}	(a-1)/a * V_{OUT}
V_{L4}	(a-2)/a * V_{OUT}
V_{L3}	2/a * V_{OUT}
V_{L2}	1/a * V_{OUT}

Table 4 - $V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$ Relationship

7.19 ROW0 – ROW159

These pins provide the driving signals, COMMON, to the LCD panel.

7.20 COL0 – COL395

These pins provide the LCD driving signals, SEGMENT, to the LCD panel. The Red, Green, Blue colors signal are sent out from the SEGMENT output at the same time. The output voltage level of these pins is V_{DD} during sleep mode or standby mode.

7.21 C1P, C1N, C2P, C2N, C1Y, C3P, C4P

When internal DC-DC voltage converter is used, external capacitor is connected between these pins. Please refer to the system block diagram for external capacitors connection in Figure 5 on page 24.

7.22 CL

This pin is the system clock I/O. This pin is the external clock input for the device, which is enabled by using extended command. It should be left open under normal operation. The internal oscillator will be used after power on reset.

7.23 M

This pin is used for cascade purpose only. It should be left open under normal operation.

7.24 SYN

This pin is used for cascade purpose only. It should be left open under normal operation.

7.25 BUSY

This pin will be high during RAM buffer read/write operation and during graphic commands executing. System programmer should read this pin (low is ready, high is busy) before sending next RAM buffer related command (e.g. RAM write – 5CH; RAM read – 5DH OR any graphic commands)
Remark: Wait time for update GDDRAM content after execution of graphic command: 100ns/pixel (VDD = 3.0V ~ 3.6V) / 125ns/pixel (VDD = 2.4V ~ 3.0V)

7.26 NC

The No connection (NC) pin should NOT be connected to any signal pin nor shorted to other NC pins in application. It should be left open.

7.27 DUMMY

This pin is a floating dummy pin with no internal circuit connection.

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 Microprocessor Interface Logic

The Microprocessor Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS2, PS1 and PS0 pins. Please refer to the pin descriptions on page 16.

a) MPU Parallel 6800-series Interface

The parallel Interface consists of 16 bi-directional data pins (D15 – D0), R / $\overline{W}$, D/$\overline{C}$, E and $\overline{CS}$. R / $\overline{W}$ input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. R / $\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Figure 16 & Figure 17 for Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

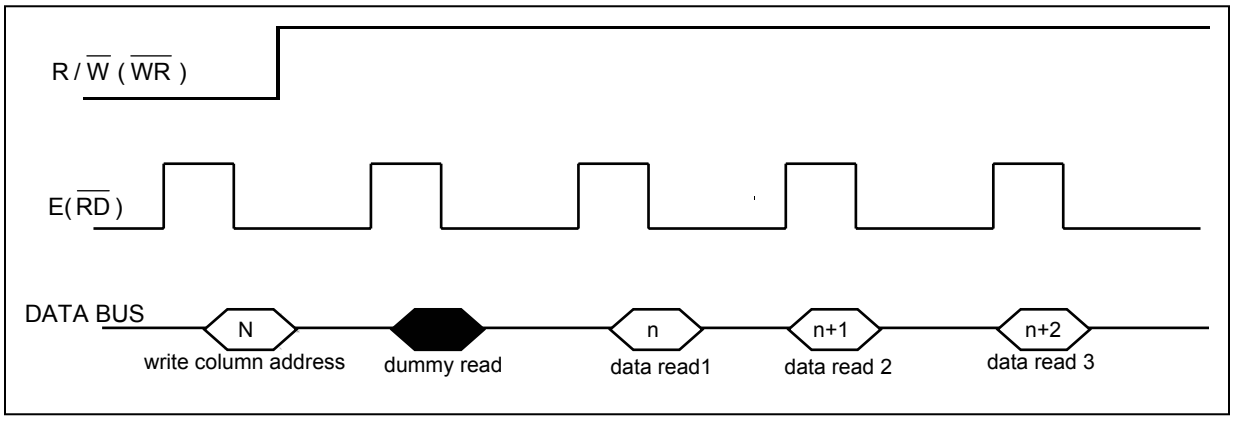


Figure 3 – Read Display Data

b) MPU Parallel 8080-series Interface

The parallel interface consists of 16 bi-directional data pins D15 – D0, $\overline{RD}$, $\overline{WR}$, D/$\overline{C}$ and $\overline{CS}$. $\overline{RD}$ input serves as data read latch signal (clock) when low provided that $\overline{CS}$ is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by D/$\overline{C}$. $\overline{WR}$ input serves as data write latch signal (clock) when low provided that $\overline{CS}$ is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/$\overline{C}$. A dummy read is also required before the first actual display data read for 8080-series interface.

c) MPU 4-lines Serial Peripheral Interface

The 4-lines serial peripheral Interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$ and $\overline{CS}$. SDA is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 …… data bit 0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock. Please refer to Figure 20 on page 61 for serial interface timing.

d) MPU 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while $D/\overline{C}$ is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: $D/\overline{C}$ bit, D7 to D0 bit. The $D/\overline{C}$ bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM ($D/\overline{C}$ bit = 1) or the command register ($D/\overline{C}$ bit = 0).

	6800 – series Parallel Interface	**8080 – series Parallel Interface**	**3-lines or 4-lines Serial peripheral Interface**
Data Read	16/8-bits	16/8-bits	No
Data Write	16/8-bits	16/8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

Table 5 - Data bus selection modes

8.2 Reset Circuit

This block is integrated into the Microprocessor Interface Logic which includes Power On Reset circuitry and the hardware reset pin, $\overline{RES}$. Both of these having the same reset function. Once the $\overline{RES}$ pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given by:

When $\overline{RES}$ input is low, the chip is initialized to the following:

1.	Display ON/OFF:	Display is OFF
2.	Normal/Inverse Display:	Normal Display
3.	COM Scan Direction:	ROW0-ROW159 = COM0-COM159
4.	Internal Oscillator:	Disable
5.	Reference Voltage Generation Circuit:	Disable
6.	Voltage regulator and Voltage Follower:	Disable
7.	Booster:	Disable
8.	Bias ratio:	1/9
9.	Multiplex ratio:	160 Mux
10.	Contrast level	32
11.	Internal Regulator gain	7.02
12.	Average temperature gradient:	-0.21%/^{o}C
13.	Partial display mode:	Disable
	Start COM address:	0
	End COM address:	0
14.	Area Scroll set	
	Top block address:	0
	Bottom block address:	0
	Number of specified block:	0
	Area scroll mode:	Whole screen scroll mode
15.	Scroll start set	
	Start block address:	0
16.	Data Scan Direction	
	Normal/inverse display of page address:	Normal
	Normal/inverse display of column address:	Normal
	Address-scan direction:	Column direction
	RGB arrangement:	RGB
	Gray-scale setup:	4K color
17.	Start Page Address set:	0
18.	End Page Address set:	0
19.	Start Column address set:	0
20.	End Column address set:	0
21.	Select PWM/FRC	5-bit PWM + 1-bit FRC mode

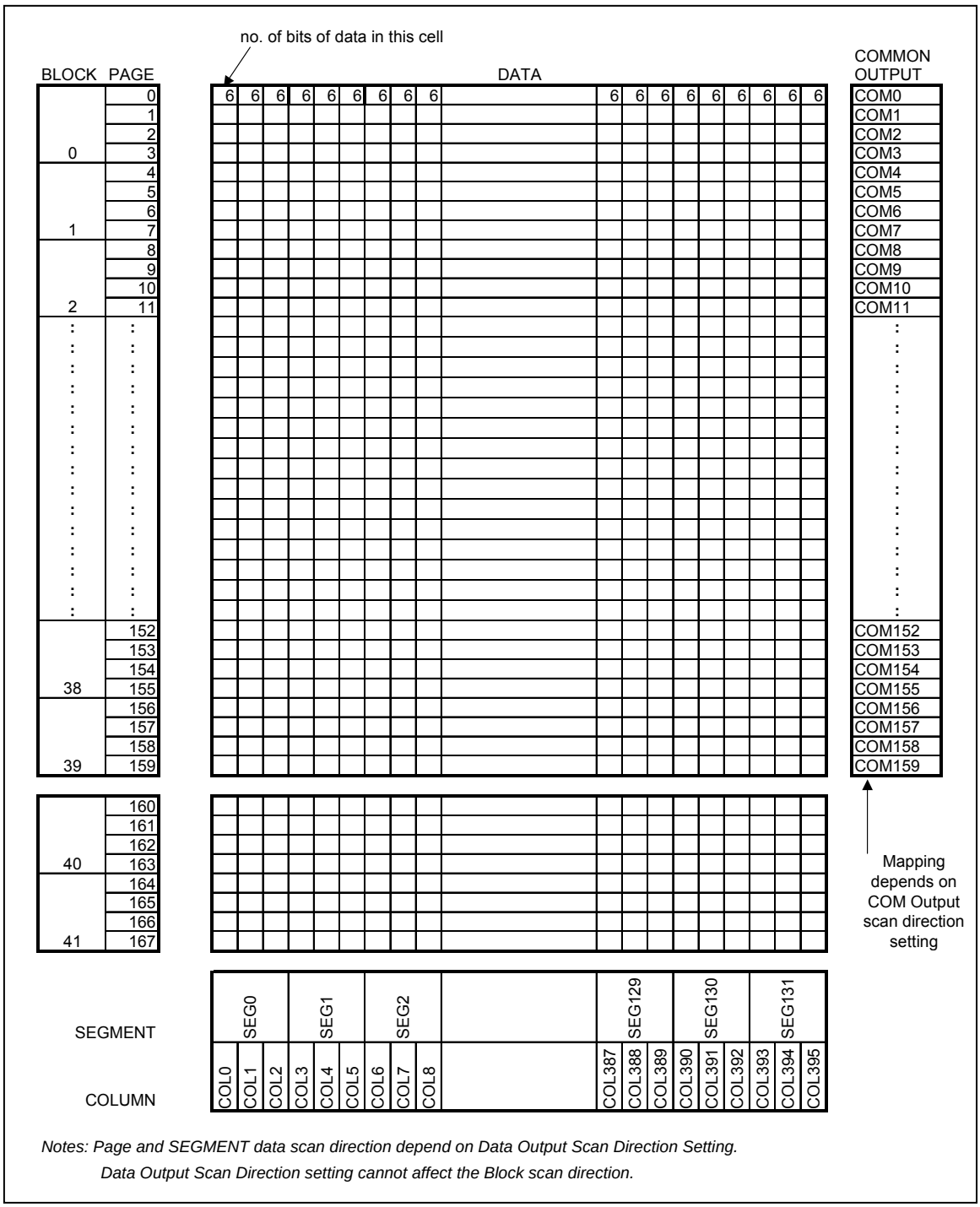
8.3 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ pin is high, data is written to Graphic Display data RAM (GDDRAM). If it is low, the input at D7 – D0 is interpreted as a Command and it will be decoded. The decoded command will be written to the corresponding command register.

8.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 RGB x 168 x 18 = 399168 bits. Figure 4 on page 23 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command “Data Output/Scan direction” in Table 6 on page 26 for detail description.

Four pages of display data form a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command “Set area Scroll” and “Set Scroll Start” in Table 13 on page 39.



Notes: Page and SEGMENT data scan direction depend on Data Output Scan Direction Setting.
Data Output Scan Direction setting cannot affect the Block scan direction.

Figure 4 – Graphic Display Data RAM Map

8.5 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of:

1. 4X, 5X, 6X and 7X DC-DC voltage converter.
2. Bias Divider - If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{OUT}) to give the LCD driving levels (V_{L2} - V_{L5}).
3. Contrast Control -Software control of 64 voltage levels of LCD voltage.
4. Bias Ratio Selection circuitry -Software control of 1/7 to 1/14 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry - Provide 5 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is -0.21%/°C.

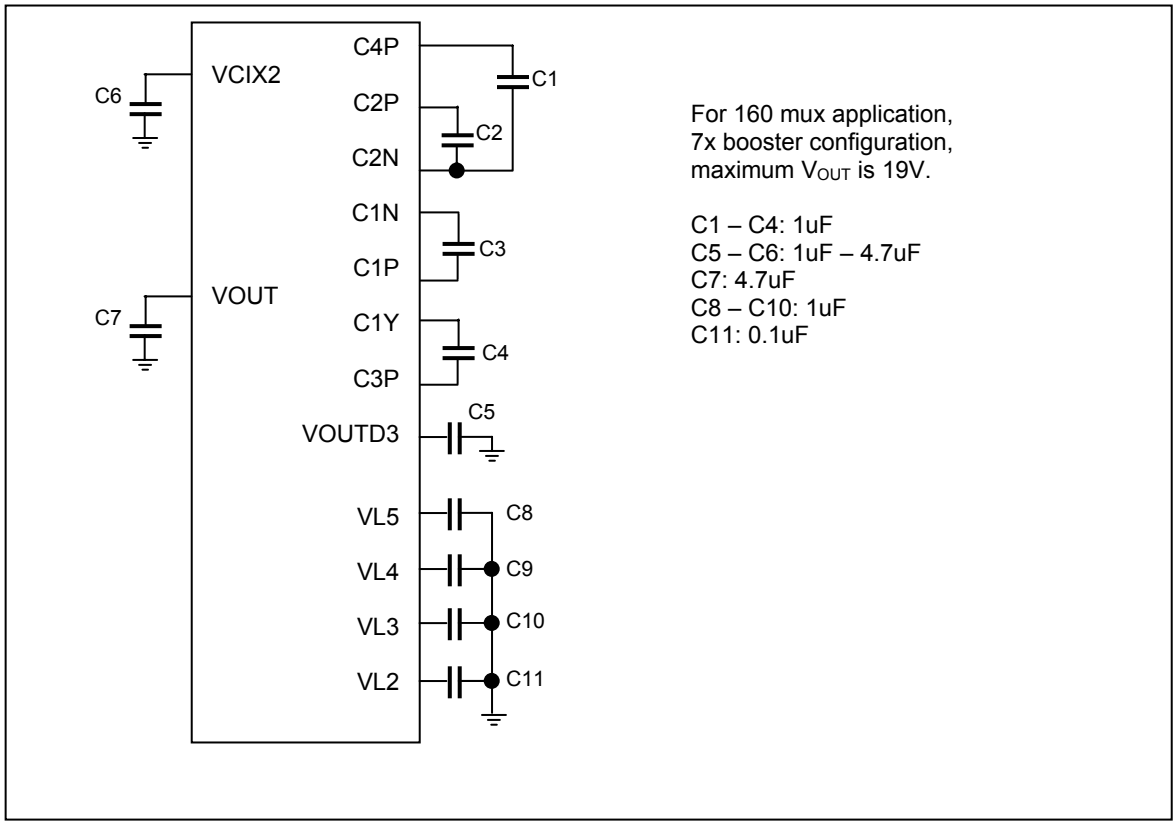


Figure 5 - SSD1783B Booster and Divider Configurations

8.6 Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 6). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

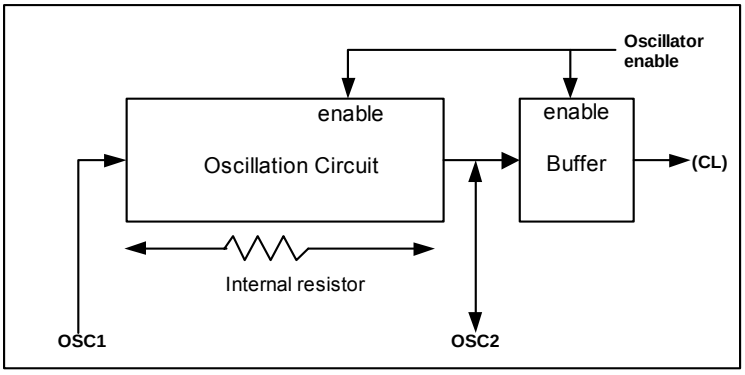


Figure 6 - Oscillator structural block diagram

8.7 Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

8.8 HV Buffer Cell (Level Shifter)

This block is embedded in the Segment/Common Driver Circuits. HV Buffer Cell works as a level shifter, which translates the low voltage output signal to the required driving voltage. The output is shifted out with reference to the internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

8.9 Level Selector

This block is embedded in the Segment/Common Driver circuits. Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

9 COMMAND TABLE

Table 6 - COMMAND TABLE

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	15	0 X_7 Y_7	0 X_6 Y_6	0 X_5 Y_5	1 X_4 Y_4	0 X_3 Y_3	1 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Column Address	Set the start column address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end column address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ Column address = 00000000b (POR) Column address is in a range of 0~131.
0 1 1	75	0 X_7 Y_7	1 X_6 Y_6	1 X_5 Y_5	1 X_4 Y_4	0 X_3 Y_3	1 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Page Address	Set the start page address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end page address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ Page address = 00000000b (POR) Page address is in a range of 0~167.
0 1	BB	1 *	0 *	1 *	1 *	1 *	0 X_2	1 X_1	1 X_0	Set COM Output Scan Direction	X_2 X_1 X_0 ROW0…ROW79 ROW80…ROW159 0 0 0 COM0 ->COM79 COM80 -> COM159 (POR) 0 0 1 COM0 ->COM79 COM159<-COM80 0 1 0 COM79<-COM0 COM80 -> COM159 0 1 1 COM79<-COM0 COM159<-COM80
0 1 1 1	BC	1 * * *	0 * * *	1 * * *	1 * * P_{34}	1 * * P_{33}	1 P_{12} P_{22} P_{32}	0 P_{11} P_{21} P_{31}	0 P_{10} P_{20} P_{30}	Set Data Output Scan Direction	a) Normal or Reverse page/column/scan directions P_{10} = 0: set page address to normal display (POR) P_{10} = 1: set page address to inverse display P_{11} = 0: set column address to normal rotation (POR) P_{11} = 1: set column address to inverse rotation P_{12} = 0: set scan direction to column scan (POR) P_{12} = 1: set scan direction to page scan Please refer to the Figure 7 on page 36 for detail description of column/page scan direction modes b) RGB color arrangement P_{22}, P_{21}, P_{20}: The control bits are used for setting the (RGB) color arrangement of segment output. 000 is the POR value. Please refer to the Table 11 on page 37 for detail mapping of the segment output. c) Gray-scale selection P_{31} P_{30} Gray-scale modes 0 0 16-bit/pixel mode 0 1 8-bit/pixel mode 1 0 12-bit/pixel mode (POR) 1 1 18-bit/pixel mode P_{32} = 0: direct write mode (POR) P_{32} = 1: use gamma correction P_{34} P_{33} 0 0 type A (if using 18-bit/pixel mode) (POR) 0 1 type B (if using 18-bit/pixel mode) 1 0 type C (if using 18-bit/pixel mode) Please refer to the Table 12 on page 37 for detail description of different gray-scale selection modes. Different gray-scale selection modes.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	CE	1	1	0	0	1	1	1	0	Set 262K/65K/4K/256 Color Look Up Table (LUT)	N=32 for 18 bit mode N=32 for 16 bit mode N=16 for 12 bit mode N=10 for 8 bit mode
1		*	*	X_{51}	X_{41}	X_{31}	X_{21}	X_{11}	X_{01}		
1		*	*	X_{52}	X_{42}	X_{32}	X_{22}	X_{12}	X_{02}		
					:						
					:						
1		*	*	X_{58}	X_{48}	X_{38}	X_{28}	X_{18}	X_{08}		
1		*	*	X_{59}	X_{49}	X_{39}	X_{29}	X_{19}	X_{09}		
					:						
					:						
1		*	*	X_{516}	X_{416}	X_{316}	X_{216}	X_{116}	X_{016}		
1		*	*	X_{517}	X_{417}	X_{317}	X_{217}	X_{117}	X_{017}		
					:						
					:						
1		*	*	X_{5N}	X_{4N}	X_{3N}	X_{2N}	X_{1N}	X_{0N}		
0	CA	1	1	0	0	1	0	1	0	Set Display Control	Driver duty selection Select driver duty from 1/32 to 1/160. As Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 is increased from 000111b to 100111b, the number of display lines, N is increased at the same rating. To specify the Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 = (N/4)-1
1		0	0	0	0	0	0	0	0		
1		*	*	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0		
1		0	0	0	0	0	0	0	0		
0	AA	1	0	1	0	1	0	1	0	Set Area Scroll	a) Top Block Address $X_5X_4X_3X_2X_1X_0$ is used to specify the block address (1 block = 4 lines) at the top of the scrolling area. Top block address = 000000b (POR) b) Bottom Block Address $Y_5Y_4Y_3Y_2Y_1Y_0$ is used to specify the block address (1 block = 4 lines) at the bottom of the scrolling area. Bottom block address = 000000b (POR) c) Number of specified Blocks The number of specified blocks = Number of (Top fixed area + Scroll area) blocks –1. If bottom scroll or whole screen scroll mode is chosen, the number of specified blocks is set to Z_5~ Z_0 Number of specified blocks = 000000b (POR) d) Area Scroll Mode There are four types of area scroll. P_{41} P_{40} Types of Area Scroll 0 0 Center Screen Scroll 0 1 Top Screen Scroll 1 0 Bottom Screen Scroll 1 1 Whole Screen Scroll Type of area scroll = Whole Screen Scroll (POR)
1		*	*	X_5	X_4	X_3	X_2	X_1	X_0		
1		*	*	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0		
1		*	*	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0		
1		*	*	*	*	*	*	P_{41}	P_{40}		

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	AB	1 *	0 *	1 X_5	0 X_4	1 X_3	0 X_2	1 X_1	1 X_0	Set Scroll Start	$X_5X_4X_3X_2X_1X_0$ specify the start block address (1 block = 4 lines) of area scrolling. Start block address = 000000b (POR)
0 1	20	0 *	0 *	1 *	0 *	0 X_3	0 X_2	0 X_1	0 X_0	Set Power Control Register	X_0=0: turns off the reference voltage generator (POR) X_0=1: turns on the reference voltage generator X_1=0: turns off the internal regulator and voltage follower (POR) X_1=1: turns on the internal regulator and voltage follower Select booster level X_3 X_2 Boost level 0 0 4X 0 1 5X 1 0 6X (POR) 1 1 7X
0 1 1	81	1 * *	0 * *	0 X_5 *	0 X_4 *	0 X_3 *	0 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Contrast Level & Internal Regulator Resistor Ratio	a) Select contrast level from 64 contrast steps Contrast increases as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 100000b (POR) b) The internal regulator gain (1+R2/R1) V_{OUT} increases as $Y_2Y_1Y_0$ is increased from 000b to 111b. The factor, 1+R2/R1, is given by: $Y_2Y_1Y_0$ = 000: 7.02 (POR) $Y_2Y_1Y_0$ = 001: 7.89 $Y_2Y_1Y_0$ = 010: 8.76 $Y_2Y_1Y_0$ = 011: 9.63 $Y_2Y_1Y_0$ = 100: 10.5 $Y_2Y_1Y_0$ = 101: 11.37 $Y_2Y_1Y_0$ = 110: 12.24 $Y_2Y_1Y_0$ = 111: 13.11
0	D6 – D7	1	1	0	1	0	1	1	X_0	Increment / Decrement of the contrast set	X_0=0: The contrast set of voltage regulator is incremented by 1 X_0=1: The contrast set of voltage regulator is decremented by 1
0	A6 - A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
0 1 1	A8	1 X_7 Y_7	0 X_6 Y_6	1 X_5 Y_5	0 X_4 Y_4	1 X_3 Y_3	0 X_2 Y_2	0 X_1 Y_1	0 X_0 Y_0	Enter partial Display	$X_7X_6X_5X_4X_3X_2X_1X_0$: Start COM Address = 0000000b (POR) $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$: End COM Address = 0000000b (POR)
0	A9	1	0	1	0	1	0	0	1	Exit partial Display	Exit the “partial display mode” by executing the command 10101001b (POR)
0	AE - AF	1	0	1	0	1	1	1	X_0	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
0	94 - 95	1	0	0	1	0	1	0	X_0	Enter/Exit sleep mode	X_0=0: exit the sleep mode. X_0=1: enter sleep mode. (POR)
0	D1 - D3	1	1	0	1	0	0	X_1	X_0	Enable/disable internal oscillator	X_1 X_0 Internal oscillator status 0 1 ON 1 0 OFF (POR)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	82	1 *	0 *	0 *	0 *	0 *	0 *	1 X_1	0 X_0	Set temperature compensation coefficient	Average temperature gradients X1 X0 Average Temperature Gradient [%/ºC] 0 0 -0.10 0 1 -0.13 1 0 -0.21(POR) 1 1 -0.26
0 1 1 1 1	F4 08 00 58 03	1 0 0 0 0	1 0 0 1 0	1 0 0 0 0	1 0 0 1 0	0 1 0 1 0	1 0 0 0 0	0 0 0 0 1	0 0 0 0 1	Set the smallest temperature compensation coefficient	The average temperature gradient will be set to -0.03%/ºC. This command will overwrite the command from 0X82.
0	25	0	0	1	0	0	1	0	1	NOP	Command result in No Operation The command should be issued after the execution of the Status Read command
0 1	5C	0 Y_{71}	1 Y_{61}	0 Y_{51}	1 Y_{41}	1 Y_{31}	1 Y_{21}	0 Y_{11}	0 Y_{01}	Write display data	Enter the “write display data mode ” by executing the command 01011100b. The following byte is used to specify the data byte to be written to the GDDRAM directly. The D/C bit should be stated at logic “1” during the display data is written to the GDDRAM.

Remark: “” denote DON’T CARE* bit

Table 7 - Graphic command table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	83	1	0	0	0	0	0	1	1	Draw Line	Enter the “Draw line mode” by executing the command 10000011. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The remaining two bytes are used to specify the color. 16-bits color will be used for 18/16-bit pixel mode, 12 bit color will be used for 12/8-bit pixel mode.
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
		For 16-bit color									
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
		For 12-bit color									
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		*Remark: A, C ≤ 131, A < C; B, D ≤ 159, B < D*
0	92	1	0	0	1	0	0	1	0	Fill Enable/Disable	Enter the “Fill Enable/Disable mode” by executing the command 10010010. A_0=0: Filled color option is disabled (POR) A_0=1: Filled color option is enabled A_3A_2=00: no gradient fill (POR) A_3A_2=01: enable x-direction gradient fill A_3A_2=10: enable y-direction gradient fill A_3A_2=11: enable x and y direction gradient fill A_5A_4=00: set gradient slope to pixel distance /1 (largest) (POR) A_5A_4=01: set gradient slope to pixel distance /2 A_5A_4=10: set gradient slope to pixel distance /4 A_5A_4=11: set gradient slope to pixel distance /8 (smallest) A_6=0: dim to white (POR) A_6=1: dim to black
1		*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	84	1	0	0	0	0	1	0	0	Draw rectangle	Enter the “Draw rectangle mode” by executing the command 10000100. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The next two bytes are used to specify the border color. The last two bytes are used to specify the fill color. (depends on fill option of command 0x92). If gradient fill is enabled in command 0x92, the data byte which specific the border color is also used to specify the x,y coordinate of gradient start, and it should be within the rectangle.
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
		For 16-bit color									
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
		For 12-bit color									
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		*Remark: A, C ≤ 131, A < C; B, D ≤ 159, B < D*

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	86	1	0	0	0	0	1	1	0	Draw circle	Enter the “Draw circle mode” by executing the command 10000110. The first three bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7) are used to specify the centre’s X coordinate, Y coordinate, circle’s radius respectively. The next two bytes are used to specify the border color. The last two bytes are used to specify the fill color (depends on fill option of command 0x92).
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
		For 16-bit color									
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
		For 12-bit color									
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		*Remark: $0 \le A7\sim A0 \le 255$; $0 \le B7\sim B0 \le 255$; $1 \le C7\sim C0 \le 255$*
0	8A	1	0	0	0	1	0	1	0	Copy	Enter the “Copy mode” by executing the command. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The remaining two bytes (E_0 to E_7, F_0 to F_7) are used to specify the new location of X coordinates and Y coordinates.
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		*Remarks: A, C ≤ 131, A < C; B, D ≤ 159, B < D*
0	8C	1	0	0	0	1	1	0	0	Dim Window	Enter the “Dim Window mode” by executing the command 10001100. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The selected window area will be dimmed by 75% white or black according to data bit A6 of command 0x92
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		*Remarks: A, C ≤ 131, A < C; B, D ≤ 159, B < D*
0	8E	1	0	0	0	1	1	1	0	Clear Window	Enter the “Clear Window mode” by executing the command 10001110. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. All pixels contrast will be set to 0.
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		*Remarks: A, C ≤ 131, A < C; B, D ≤ 159, B < D*

Remark: *“*” denote DON’T CARE* bit

After executed the graphic command, waiting time is required for update GDDRAM content.
(When V_{DD}=2.4~3.0V, waiting time = 135ns/pixel; When V_{DD}=3.0~3.6V, waiting time = 110ns/pixel)

Table 8 - Extended command table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	FB	1	1	1	1	1	0	1	1	Set biasing ratio	Allow user to set bias from 1/ 7 to 1/14
1		*	*	*	*	0	B_2	B_1	B_0		$B_2B_1B_0$ Bias ratio 0 0 0 1/7 bias 0 0 1 1/8 bias 0 1 0 1/9 bias (POR) 0 1 1 1/10 bias 1 0 0 1/11 bias 1 0 1 1/12 bias 1 1 0 1/13 bias 1 1 1 1/14 bias
0	F2	1	1	1	1	0	0	1	0	Set Frame frequency and N-line Inversion	This command uses to change the frame frequency; set the N-line inversion and N-line inversion mode Frame Frequency Reference Value*
1		0	0	0	0	F_3	F_2	F_1	F_0		$F_3F_2F_1F_0$
1		0	N_6	N_5	N_4	N_3	N_2	N_1	N_0		1 1 1 1 : 144 Hz 1 1 1 0 : 124 Hz 1 1 0 1 : 111 Hz 1 1 0 0 : 100 Hz 1 0 1 1 : 94 Hz 1 0 1 0 : 86 Hz 1 0 0 1 : 80 Hz 1 0 0 0 : 75 Hz (POR) 0 1 1 1 : 73 Hz 0 1 1 0 : 69 Hz 0 1 0 1 : 65 Hz 0 1 0 0 : 62 Hz 0 0 1 1 : 60 Hz 0 0 1 0 : 57 Hz 0 0 0 1 : 54 Hz 0 0 0 0 : 52 Hz *remark: the frame frequency are typical values only. The second byte data $N_5N_4N_3N_2N_1N_0$ sets the n-line inversion register from 2 to 64 lines to reduce display crosstalk. Register values from 000001b to 111111b are mapped to 2 lines to 64 lines respectively. Value 00000b disables the N-line inversion. 010000 is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux should NOT be a multiple of the lines of inversion (n). N_6 0 – reset n-line counter per frame (POR) 1 – will not reset n-line counter per frame

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A2 - A3	1	0	1	0	0	0	1	X0	Reserved	
0	F7	1	1	1	1	0	1	1	1	Select PWM/FRC Select Full Color/ "8 Color" mode	X_7 0 0 0 1 1 1 0
1	28	0	0	1	0	1	0	0	0		0 0 0 0 1 1 1 0 : 5 bits PWM + 1 bit FRC (POR)
1		X_7	0	0	0	1	1	1	0		1 0 0 0 1 1 1 0 : 4 bits PWM + 2 bits FRC
1		0	Y_6	0	0	0	1	0	1		Y_6 = 0: Full Color Mode (POR) Y_6 = 1: "8 Color" Mode for power saving purpose
0	F1	1	1	1	1	0	0	0	1	Set COM sequence	X_1 X_0 COM0 – 79 COM80 – 159
1		1	1	X_1	X_0	0	0	0	0		0 0 : COM0 - COM79 COM80 - COM159 (POR)
1	0	0	0	0	0	0	0	0	0		0 1 : COM0 - COM31, COM32 - COM63,
1	0	0	0	0	0	0	0	0	0		COM64 – COM111 COM112 - COM159
											1 0 : COM1 - COM159 (odd) COM0 - COM158 (even)
											1 1 : COM0 - COM158 (even) COM1 - COM159 (odd)
0	F6	1	1	1	1	0	1	1	0	OTP setting	This command set the offset value of contrast
1		0	0	0	1	X_4	X_3	X_2	X_1		$X_4X_3X_2X_1X_0$
1		0	0	X_0	0	1	0	1	0		00000 : original contrast 00001 : original contrast + 1 step 00010 : original contrast + 2 steps 00011 : original contrast + 3 steps 00100 : original contrast + 4 steps 00101 : original contrast + 5 steps 00110 : original contrast + 6 steps 00111 : original contrast + 7 steps 01000 : original contrast + 8 steps 01001 : original contrast + 9 steps 01010 : original contrast + 10 steps 01011 : original contrast + 11 steps 01100 : original contrast + 12 steps 01101 : original contrast + 13 steps 01110 : original contrast + 14 steps 01111 : original contrast + 15 steps 10000 : original contrast - 16 steps 10001 : original contrast - 15 steps 10010 : original contrast - 14 steps 10011 : original contrast - 13 steps 10100 : original contrast - 12 steps 10101 : original contrast - 11 steps 10110 : original contrast - 10 steps 10111 : original contrast - 9 steps 11000 : original contrast - 8 steps 11001 : original contrast - 7 steps 11010 : original contrast - 6 steps 11011 : original contrast - 5 steps 11100 : original contrast - 4 steps 11101 : original contrast - 3 steps 11110 : original contrast - 2 steps 11111 : original contrast - 1 step
0	F8	1	1	1	1	1	0	0	0	OTP programming	This command starts to program LCD driver with OTP offset value. This command can be executed once only. Detail of OTP programming procedure on page 45
0 1	44	0 A_7	1 A_6	0 A_5	0 A_4	0 A_3	1 A_2	0 A_1	0 A_0	Scroll-by-com	Set Scroll-by-com command. Byte A specifies the number of scroll lines. $A_7A_6A_5A_4A_3A_2A_1A_0$ = 00000000 (POR)

Table 9 - Read Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	5D	0 Y_{71}	1 Y_{61}	0 Y_{51}	1 Y_{41}	1 Y_{31}	1 Y_{21}	0 Y_{11}	1 Y_{01}	Read display data	Enter the “read display data mode ” by executing the command 01011101b. The next byte is a dummy data. The GDDRAM data will be read form the second byte. The GDDRAM column address pointer will be increased by one automatically after each 2-bytes data read. (64K color mode).
0 0	5D	0 D7	1 D6	0 D5	1 D4	1 D3	1 D2	0 D1	1 D0	Status Register Read	D_7D_6 = 00: Center Screen Scroll Mode D_7D_6 = 01: Top Screen Scroll Mode D_7D_6 = 10: Bottom Screen Scroll Mode D_7D_6 = 11: Whole Screen Scroll Mode D_4 = 0: Scan Direction is column direction D_4 = 1: Scan Direction is page direction D_3 = 0: Display is OFF D_3 = 1: Display is ON D_2 = 0: Sleep Mode is disabled D_2 = 1: Sleep Mode is enabled D_1 = 0: Display is Inverse D_1 = 1: Display is Normal D_0 = 0: Partial display is disabled D_0 = 1: Partial display is enabled

Note: Command patterns other than that given in Command Table are prohibited. Otherwise, unexpected result will occur.

Remark: “” denote DON’T CARE* bit

9.1 Data Read / Write

To read data from the GDDRAM, 5DH command should be executed then input High to R/$\overline{W}$ ($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode. Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read in 8-levels gray scale mode OR after each 3-bytes data read in 16-levels gray scale mode. Also, a dummy read is required before the first data is read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/$\overline{W}$ ($\overline{WR}$) pin and High to D/$\overline{C}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write in 8-levels gray scale mode OR each 3-bytes data write in 16-levels scale mode. The address will be reset to 0 in next data read/write operation is executed when it is 103.

10 COMMAND DESCRIPTIONS

10.1 Set Column Address (15 H)

This command specifies the 8-bit column address of the display data RAM. The start and the end column address are specified by this command. The driver supports up to 132 columns. As the addresses are incremented from the start column to the end column in the column direction scan, the page address is incremented by 1. The column address is then returned to the start column. The column address will be increased by each data access after it is preset by the MCU. Start column < End column must be maintained.

RGB Alignment using 262K color mode

			Column																					
	P11=0		0						1							65								
	Color		R1	G1	B1	R2	G2	B2	R1	G1	B1	R2	G2	B2		R1	G1	B1	R2	G2	B2			
	Data		D15	D7	D15	D7	D15	D7	D15	D7	D15	D7	D15	D7		D15	D7	D15	D7	D15	D7			
			D14	D6	D14	D6	D14	D6	D14	D6	D14	D6	D14	D6		D14	D6	D14	D6	D14	D6			
			D13	D5	D13	D5	D13	D5	D13	D5	D13	D5	D13	D5		D13	D5	D13	D5	D13	D5			
			D12	D4	D12	D4	D12	D4	D12	D4	D12	D4	D12	D4		D12	D4	D12	D4	D12	D4			
			D11	D3	D11	D3	D11	D3	D11	D3	D11	D3	D11	D3		D11	D3	D11	D3	D11	D3			
	Page		D10	D2	D10	D2	D10	D2	D10	D2	D10	D2	D10	D2		D10	D2	D10	D2	D10	D2			
LCD Read Direction																								
	P11=1		65						64							0								
	Color		R2	G2	B2	R1	G1	B1	R2	G2	B2	R1	G1	B1		R2	G2	B2	R1	G1	B1			
	Data		D7	D15	D7	D15	D7	D15	D7	D15	D7	D15	D7	D15		D7	D15	D7	D15	D7	D15			
			D6	D14	D6	D14	D6	D14	D6	D14	D6	D14	D6	D14		D6	D14	D6	D14	D6	D14			
			D5	D13	D5	D13	D5	D13	D5	D13	D5	D13	D5	D13		D5	D13	D5	D13	D5	D13			
			D4	D12	D4	D12	D4	D12	D4	D12	D4	D12	D4	D12		D4	D12	D4	D12	D4	D12			
	Page		D3	D11	D3	D11	D3	D11	D3	D11	D3	D11	D3	D11		D3	D11	D3	D11	D3	D11			
BLOCK	P10=0	P10=1	D2	D10	D2	D10	D2	D10	D2	D10	D2	D10	D2	D10		D2	D10	D2	D10	D2	D10			
0	0	167																						
	1	166																						
	2	165																						
	3	164																						
1	4	163																						
	5	162																						
	6	161																						
	7	160																						
:	:	:													:									
:	:	:													:									
:	:	:													:									
:	:	:													:									
:	:	:													:									
:	:	:													:									
:	:	:													:									
:	:	:													:									
:	:	:													:									
39	156	11																						
	157	10																						
	158	9																						
	159	8																						
40	160	7																						
	161	6																						
	162	5																						
	163	4																						
41	164	3																						
	165	2																						
	166	1																						
	167	0																						

SEGMENT OUTPUTS	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	COL8	COL9	COL10	COL11		COL390	COL391	COL392	COL393	COL394	COL395

Table 10 - RAM arrangements of 18-bit/pixel, direct write mode.

10.2 Set Page Address (75 H)

This command enters the page address from 0 to 167 to the RAM page register for read/write operations. The driver supports up to 160 lines. All in all, there are 168 pages. As the addresses are incremented from the start page to the end page in the page direction scan, the column address is incremented by 1. The page address is then returned to the start page. Start page < End page must be maintained.

10.3 Set COM Output Scan Direction (BB H)

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. Please refer to the Table 6 on Page 26 for detail mapping. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

10.4 Set Data Output Scan Direction (BC H)

This command sets the DDRAM such that the MPU operates the display data in the internal RAM.
A. Normal or Inverse page/column/scan directions
The Data Scan direction can be set to either normal or inverse display page and column address scan direction. The column and the page direction are illustrated in the following figure.

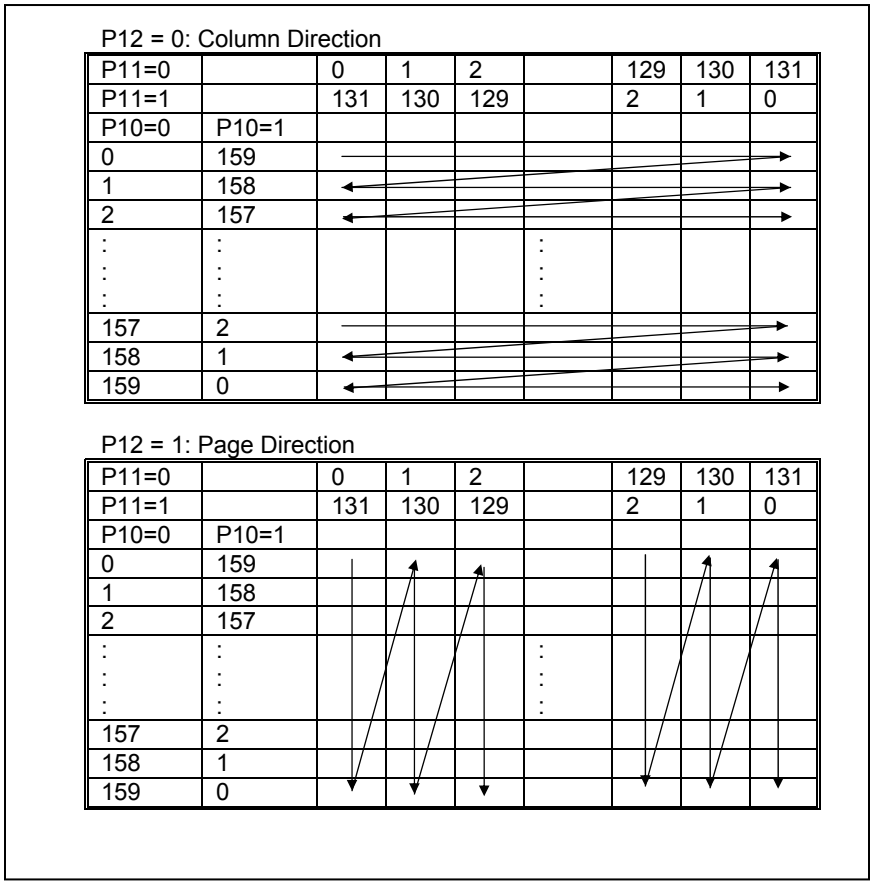


Figure 7 - column and page scan direction

The parameters following the command set data output scan direction specifies the RGB arrangement and the selection of various gray-scale modes. Please find the information of the RGB arrangement and the gray scale mode in the following section.

B. RGB arrangement mode
The RGB arrangement mode can be selected according to the following table. Three selection bits will give eight combinations of the RGB arrangements. Each combination set will specify the Red, Green and Blue segment output arrangement in odd and even page.

P22, P21, P20	LINE	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	…	COL395
000 (POR)	Even page Odd page	R R	G G	B B	R R	G G	B B	R R	G G	…	B B
001	1 2	B B	G G	R R	B B	G G	R R	B B	G G	…	R R
010	1 2	R R	G G	B B	B B	G G	R R	R R	G G	…	R R
011	1 2	B B	G G	R R	R R	G G	B B	B B	G G	…	B B
100	1 2	R B	G G	B R	R B	G G	B R	R B	G G	…	B R
101	1 2	B R	G G	R B	B R	G G	R B	B R	G G	…	R B
110	1 2	R B	G G	B R	B R	G G	R B	R B	G G	…	R B
111	1 2	B R	G G	R B	R B	G G	B R	B R	G G	…	B R

Table 11 - RGB Arrangement modes

C. Gray scale mode
Gray scale selection and corresponding data bus arrangement for different bus interface mode are illustrated in the following table.

P31, P30	Gray Scale selection	Bus interface mode (select by PS2-PS0, ref to Table 3)	P34, P33	Data bus arrangement (D15……D0) for 16 bit bus mode, (D7……D0) for 8 bit bus mode ("*" denote don't care bit)	Note
00	16-bit / pixel	16 bit	**	RRRRRGGGGGGBBBBB	1 word / 1 pixel
		8 bit		RRRRRGGG (byte 1) GGGBBBBB (byte 2)	2 byte/ 1 pixel
01	8-bit / pixel	8 bit	**	RRRGGGBB	1 byte / 1 pixel
10	12-bit / pixel	16 bit	**	RRRRGGGGBBBB****	1 word / 1 pixel
		8 bit		RRRRGGGG (byte 1) BBBBRRRR (byte 2) GGGGBBBB (byte 3)	3 byte / 2 pixel
11	18-bit / pixel	16 bit	00	RRRRRR**GGGGGG** (word 1) BBBBBB**RRRRRR** (word 2) GGGGGG**BBBBBB** (word 3)	3 word / 2 pixel
			01	RRRRRR**GGGGGG** (word 1) ********BBBBBB** (word 2)	2 word / 1 pixel
			11	RRRRRR**GGGGGG** (word 1) BBBBBB********** (word 2)	2 word / 1 pixel
		8 bit	**	RRRRRR** (byte 1) GGGGGG** (byte 2) BBBBBB** (byte 3)	3 byte / 1 pixel

Table 12 – Data bus arrangement for different pixel and bus mode

10.5 Set Color Look Up Table (CE H)

This command is used to set the color look up table (LUT) for different pixel mode. The LUT has 32 6-bit entries, the number of entry to write depends on different pixel mode, the 6 LSB of each of the data byte following this command correspond to one entry of the LUT.

Pixel mode	No. of entry	Note
18 or 16 bit/pixel	32	32 data byte (6 LSB of each) define the LUT
12 bit/pixel	16	16 data byte (6 LSB of each) define the LUT
8 bit/pixel	10	10 data byte (6 LSB of each) define the LUT with 1st 8 byte define all 8 colors of Red and Green, while Blue will use 1st and 8th byte for data 00, 11 correspondingly, and will use 9th and 10th byte for data 01 and 10 correspondingly.

10.6 Set Display Control (CA H)

This command is used to select the duty ratio of the IC. All available driving duty can be selected using this command. The driving duty can be changed from 1/32 to 1/160

10.7 Set Area Scroll (AA H)

This command specifies the portion of screen for scrolling. The command sets the starting block address, finishing block address, number of specific blocks and the area scroll mode of the area scrolling. Please be noted that the starting block address should be smaller than the finishing block address.
The block address increment direction is started at 0th block such that the GDDRAM address corresponds to the top of the fixed area. Similarly, the block address decrement direction is started at the 41st block such that the GDDRAM address corresponds to the bottom fixed area. The remaining block address excluding the top and the bottom fixed areas are assigned to the scroll plus the background areas.
The set area scroll function is divided into four parts.

Part I -Specify the top block address of the scroll + the background areas. Specify the 0th block for the top screen scroll or the whole screen scroll. The scroll start block address is also set at this top block address until the scroll start set command is executed.

Part II – Specify the bottom address of the scroll + background areas. Specify the 41st block for the bottom or the whole screen scroll.

Part III – Specify number of scrolled blocks = number of (Top fixed area + scroll area) blocks –1. When the bottom scroll or whole screen scroll is chosen, the resulted value is identical to the value stated in part II.

Part IV
Specify the area scroll type. Altogether there are four types of area scroll. Please refer to Table 13 for detail.

P41	P40	Types of Area Scroll
0	0	Center Screen Scroll
0	1	Top Screen Scroll
1	0	Bottom Screen Scroll
1	1	Whole Screen Scroll

Table 13 - Area scrolling selection modes

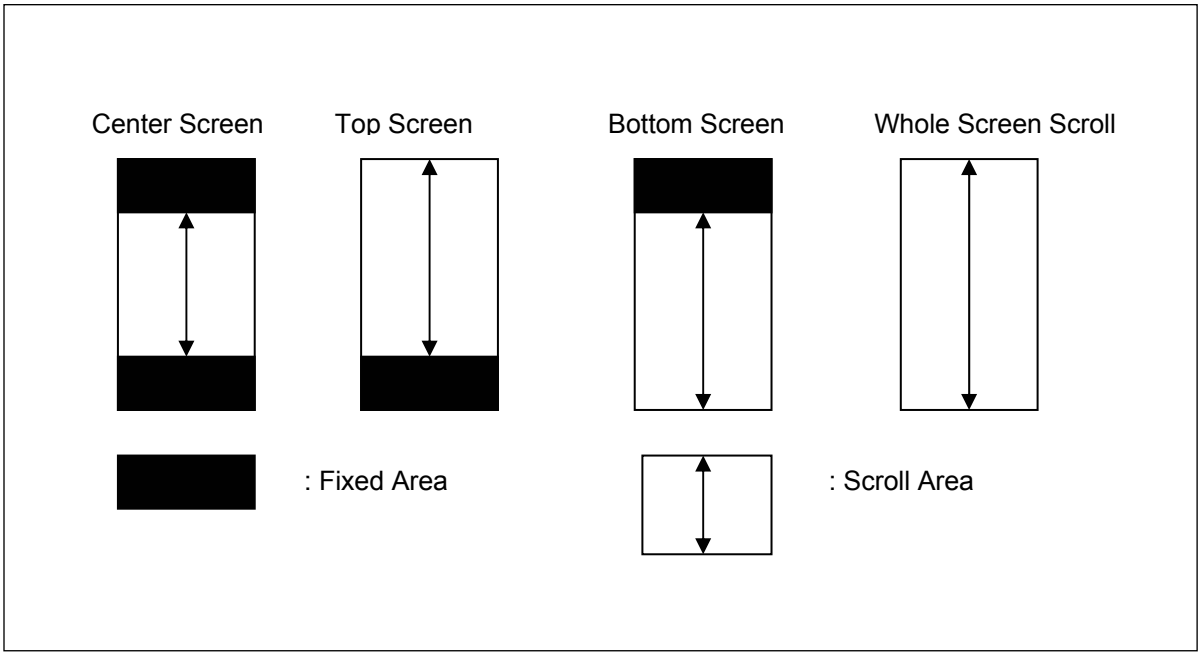


Figure 8 - Area scrolling selection modes

The area scroll function is executed by prompt in the set area scroll command following by changing the start block address by the set scroll start command.

Figure 8 illustrates the operation model of the scrolling function.

Example: In the Center screen scroll of 1/128 duty (display range: 128 lines = 32 blocks)

Description	Command	Data
- Set Area Scroll	AA H	
- 8 lines (block 0 and block 1) is specified for the top fixed area Top block address = Number of lines in top fixed area / 4 = 8 / 4 = 2		02 H
- 8 lines (block 40 & block 41) are specified for the bottom fixed area Bottom block address = 41 – (number of lines in bottom fixed area / 4) = 41 – (8 / 4) = 41 – 2 = 39		27 H
- 112 lines (block 2 to block 29) are specified the scroll area Number of specified block = Top block address + (number of lines in scroll area/4) – 1 = 2 + (112 / 4) –1 = 2 + 28 – 1 = 29		1D H
- 40 lines (block 30 to block 39) are specified the background areas		
- Set area scroll mode – Center screen mode		00 H
- Set Scroll start (Scroll range form 02H ~ 0DH)	ABH	02 H

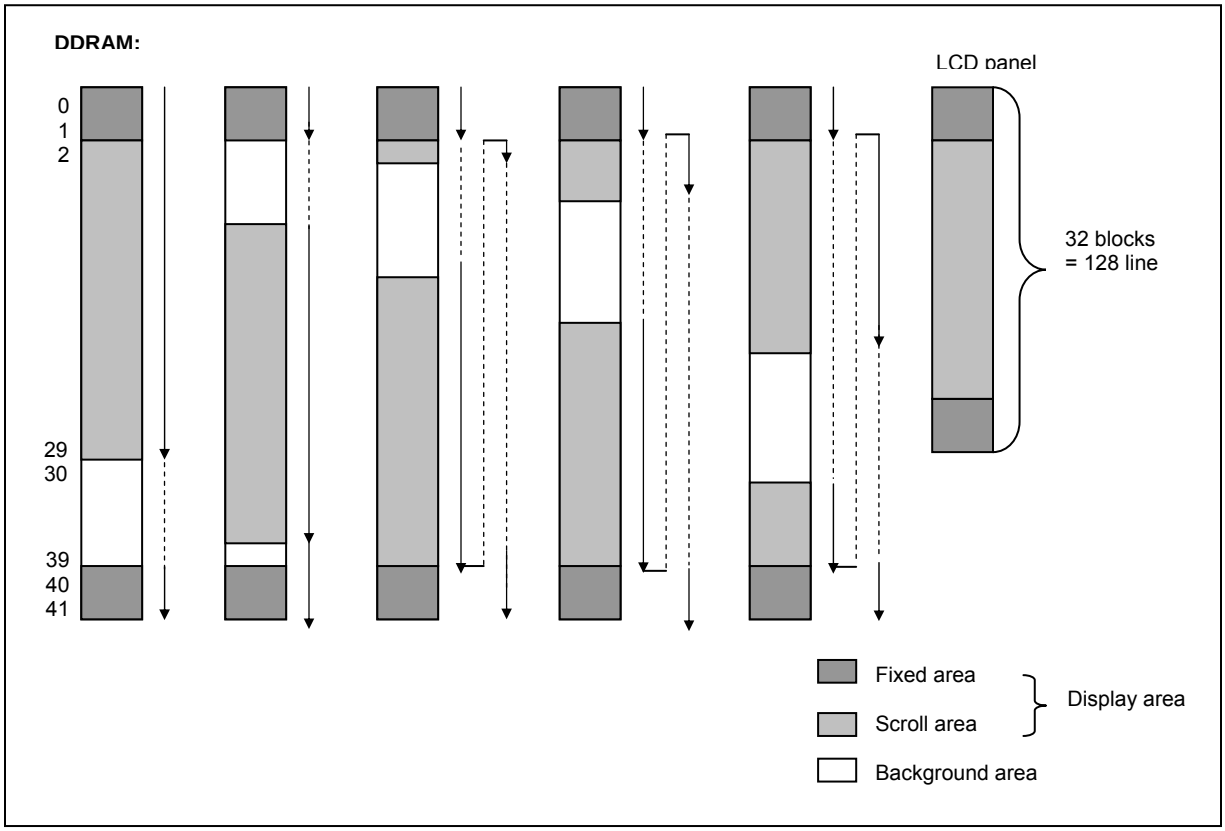
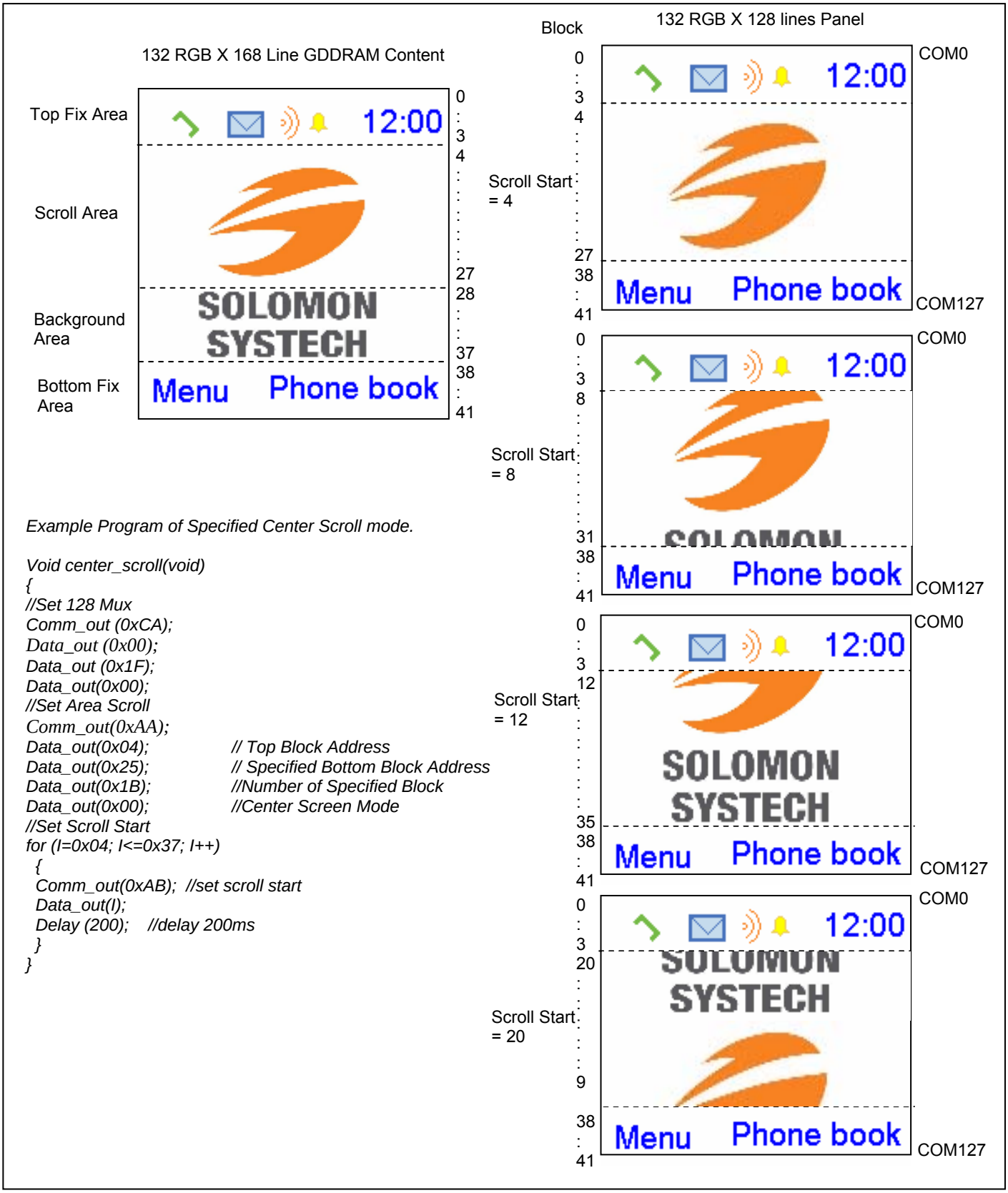


Figure 9 - GDDRAM updates for area scrolling



Example Program of Specified Center Scroll mode.

```
Void center_scroll(void)
{
//Set 128 Mux
Comm_out (0xCA);
Data_out (0x00);
Data_out (0x1F);
Data_out(0x00);
//Set Area Scroll
Comm_out(0xAA);
Data_out(0x04);          // Top Block Address
Data_out(0x25);          // Specified Bottom Block Address
Data_out(0x1B);          //Number of Specified Block
Data_out(0x00);          //Center Screen Mode
//Set Scroll Start
for (I=0x04; I<=0x37; I++)
  {
  Comm_out(0xAB);  //set scroll start
  Data_out(I);
  Delay (200);    //delay 200ms
  }
}
```

Figure 10 - Example of center scroll mode

10.8 Set Scroll Start (AB H)

This command specifies the starting block address of the area scrolling and then executes the area scroll by changing the start block address dynamically. Start block < End block must be maintained. Please be noted that the set scroll start command should be executed after the set area scroll command.

10.9 Set Power Control Register (20 H)

This command turns on/off the various power circuits associated with the chip. There are three power sub-circuits (reference voltage generator, internal regulator and voltage follower) could be turned on/off by this command. In addition, the configuration of the internal primary booster (4X/5X/6X/7X) can be selected by this command.

10.10 Set Contrast Level and Internal Regulator Resistor Ratio (IR) (81 H)

This command adjusts the contrast of the LCD panel by changing the LCD driving voltage, V_{OUT}, provided by the On-Chip power circuits. V_{OUT} is set with 64 steps (6-bit) in the contrast control register by a set of compound commands. Please refer to the Figure 11 for the contrast control process flow diagram.

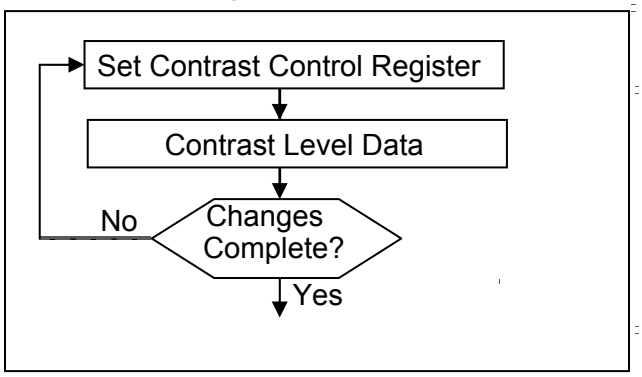


Figure 11 - Contrast Control Flow Set Segment Re-map

This command also sets the feedback gain of the internal regulator. There are altogether 8 internal regulator gains, which are used for the adjustment of V_{OUT} level. This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network. The Contrast Control Voltage Range curves is referred to the following formula:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) * V_{con}$$

$$, where\ Vref = 1.7V$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref}$$

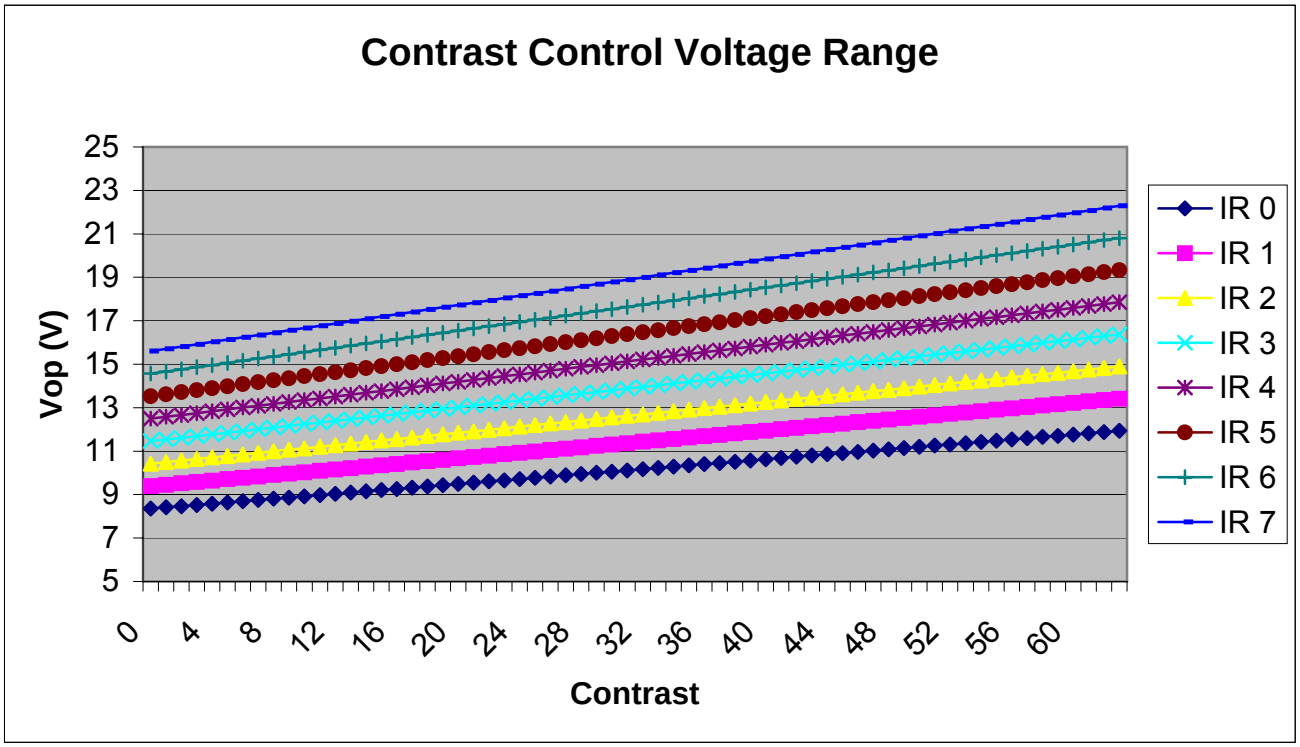


Figure 12 - Contrast Control Voltage Range Curve

10.11 Set Increment/Decrement of the contrast set (D6/D7 H)

This command can increase the contrast step by +1 (D6 H) and decrease the contrast step by –1 (D7 H). It is the most convenient way to change the contrast of the display by programming.

10.12 Set Normal/Inverse Display (A6/A7 H)

This command turns the display to be either normal (A6 H) or inverse (A7). In normal display mode, a RAM data of 1 indicates an illumination on the corresponding pixel in the normal white panel. In inverse display mode, a RAM data of 0 will turn on the pixel. It should be noted that the icon line is not affected. The icon line is not inversed by this command.

Example:
For a normal white display panel (Set Normal Display: A6Hex):

RAM Content			Color
R	G	B	
0	0	0	White
F	F	F	Black
0	F	F	Red
F	0	F	Green
F	F	0	Blue

10.13 Enter Partial Display (A8 H)

This command and the following parameters specify the display area of the partial display mode. The following figure shows the display and non-display area when the partial display mode is executed.

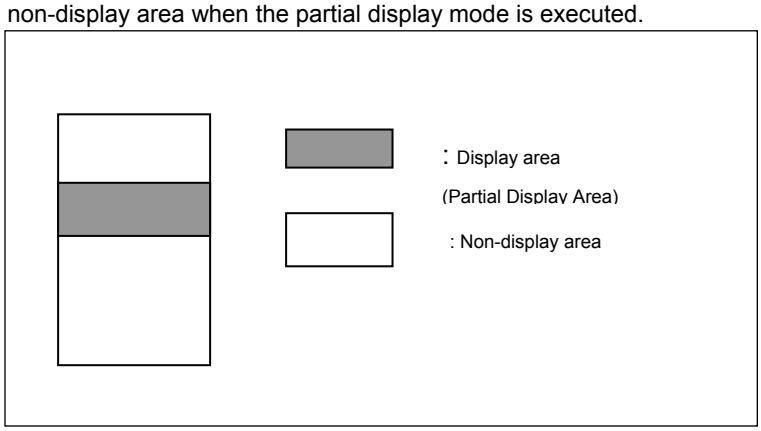


Figure 13 - Partial display mode

10.14 Exit Partial Display (A9 H)

This command exits the partial display mode.

10.15 Set Display On/Off (AF/AE H)

This command is used to turn the display on (AF H) or off (AE H). When display off is issued with entire display is on, power save mode will be entered.

10.16 Enter/Exit sleep mode (95/94 H)

This command enters (95 H) or exit (94 H) the sleep mode. After enter the sleep mode, 100us delay time is needed before other command input.

10.17 Enable/Disable the internal oscillator (D1/D2 H)

This command enables (D1 H) or disables (D2 H) the internal oscillator. The internal oscillator is turned off after reset.

10.18 Set Temperature compensation coefficient (82 H)

This command sets the average temperature gradients. Four sets of average temperature gradients can be selected. Please refer to the command table for detail description of the average temperature gradients. The default value of the temperature gradient is –0.21 %/^{0}C

10.19 NOP (25 H)

A command causing the chip takes No Operation.

10.20 Write display data mode (5C H)

This command is used to execute the write display data mode. The display data byte is directly written to the GDDRAM. Please be noted that the D/$\overline{C}$ signal should be set to high during the display data is written to the GDDRAM.

10.21 Read display data mode (5D H)

This command is used to execute the read display data mode. The display data byte is directly read from the GDDRAM. Please be noted that the D/$\overline{C}$ signal should be set to high during the display data is red from to the GDDRAM.

10.22 Set biasing ratio (FB H)

This command selects a suitable bias ratio (1/7 to 1/14) required for driving the particular LCD panel in use.

10.23 Set Frame Frequency (F2 H)

This command specifies the frame frequency so as to minimize the flickering due to the ac main frequency. The frequency is set to 75 Hz after POR.

10.24 Set N-line inversion (F2 H)

Number of line inversion is set by this command for reducing crosstalk noise. 2 to 64-line inversion operations could be selected. At POR, this operation is set to 10000b (17 lines). It should be noted that the total number of mux should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change. The n-line counter can be set such that it will be reset per display frame (POR).

10.25 Select PWM/FRC & Full Color/ “8 Color” Mode (F7 H)

This command set the Pulse Width Modulation, Frame Rate Control or mix of FWM & FRC. This command also selects the full color or “8 color” mode. “8 Color” mode is intended for power saving purpose.

10.26 OTP setting (F6 H)

OTP (One Time Programming) is a method to adjust V_{OUT}. In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules. Each OTP bit can be programmed to ‘1’ one time.

OTP setting and programming should include two major steps. Find the OTP offset and OTP programming as following,

10.27 Set Scroll-by-com (44 H)

This command specifies scroll-by-com function. Byte A specifies the scroll lines. At POR, the scroll line is set to 00000000b (0 lines).

Step 1. Find OTP offset

(1) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Adjust the contrast value (C:0x81, D:0x00~0x3F, D: 0x00 ~ 0x07) until there is the best visual contrast
(5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x24
OTP offset value = 0x24 - 0x20 = +4
OTP setting command should be (C: 0xF6, D: 0x12, D: 0x0A)

Example 2:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x1B
OTP setting = 0x1B - 0x20 = -5
OTP setting command should be (C:0xF6, D: 0x1D, D: 0x2A)

Step 2. OTP programming

(6) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(7) Enable Oscillator (C: 0xD1) and Exit Sleep Mode (C: 0x94)
(8) Connect an external V_{OUT} by closing SW1 (see diagram below)
(9) Send OTP setting commands that we find in step 1 (C: 0xF6, D: 0x10~0x1F, D: 0x0A~0x2A)
(10) Send OTP programming command (C: 0xF8)
(11) Wait at least 2 seconds
(12) Disconnect the external Vout by opening SW1
(13) Discharge the capacitor C by closing the switch SW2 and wait for 1 second
(14) Hardware Reset
(15) Verify the result by repeating step 1. (2) – (3)

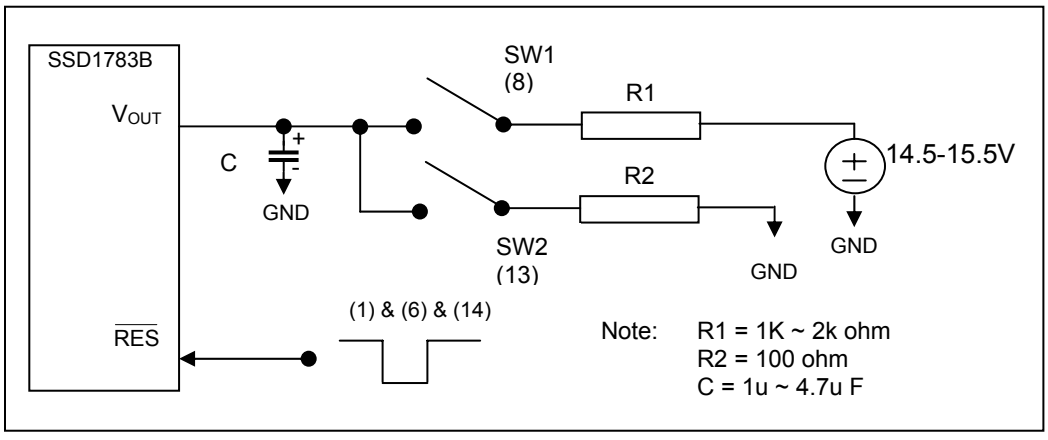


Figure 14 - OTP programming circuitry

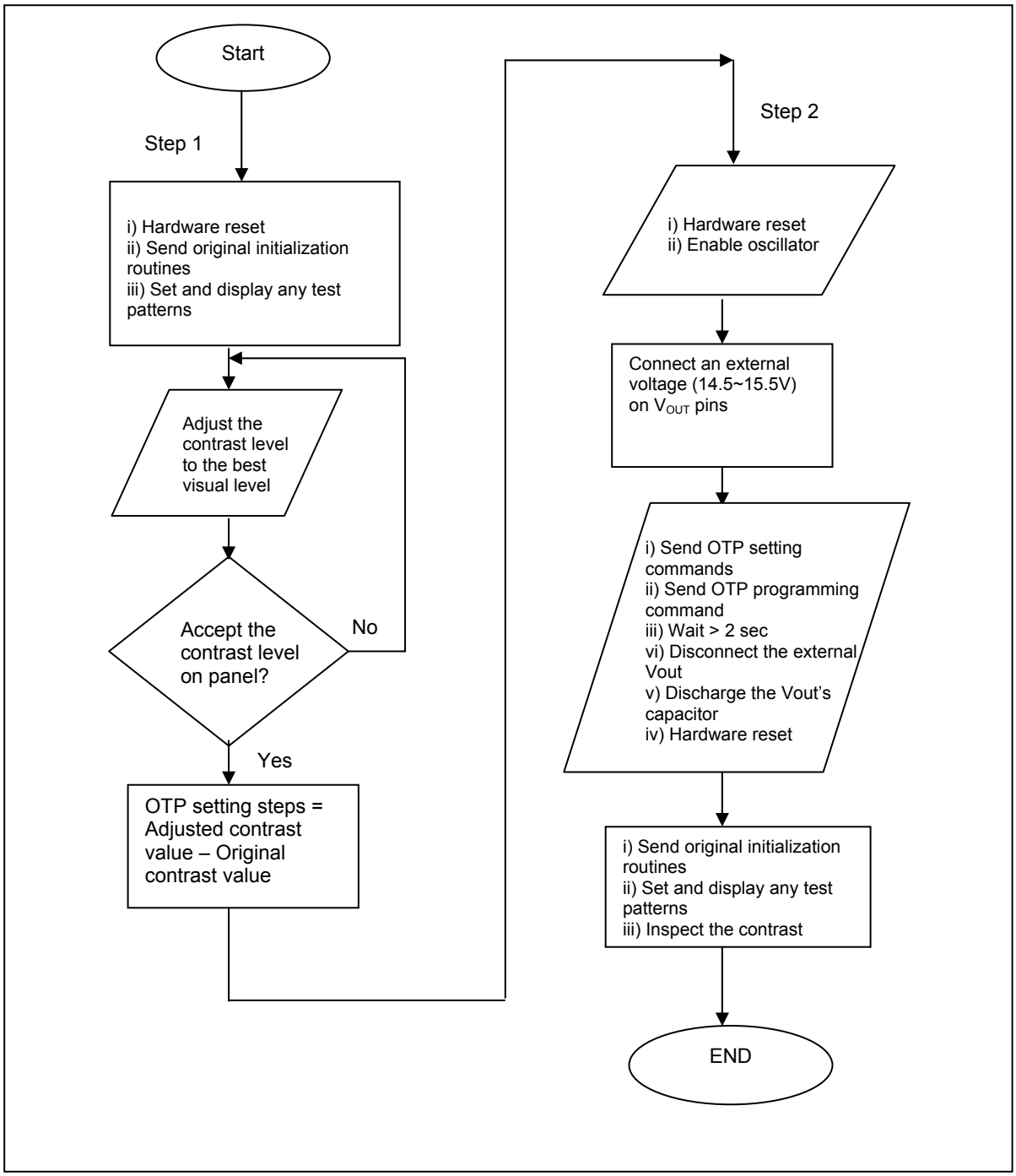


Figure 15 - Flow chart of OTP programming Procedure

OTP Example program

Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
2. COMMAND(0XD1); \\Enable oscillator;
   COMMAND(0X94); \\ exit sleep mode;
3. COMMAND(0X20); \\ turn on the reference voltage generator, internal regulator and voltage follower; Select booster level.
   DATA(0x0F);
4. COMMAND(0XFB) \\ Set Biasing ratio
   DATA(0X2) \\ 1/9
5. COMMAND(0X81) \\Set target gain and contrast.
   DATA(0X14) \\ contrast = 20 in decimal
   DATA(0X05) \\ Internal Regulator Gain = 11.37
6. \\ Set target display contents
   COMMAND(0X15) \\ set column address
   DATA(0x00) \\ set start column address at 0
   DATA(0X83) \\ set end column address at 131
   COMMAND(0X75) \\ set page address
   DATA(0X00) \\ set start page address at 0
   DATA(0X9F) \\ set end page address at 159
   COMMAND(0X5C) \\ write target content to GDDRAM
   DATA(…)
   COMMAND(0xAF) \\ display on
7. OTP offset calculation… target OTP offset value is +3

OTP programming:

8. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
9. COMMAND(0XD1) \\ Enable Oscillator
10. COMMAND(0x94) \\ Exit Sleep Mode
11. Connect a external V_{OUT} (14.5V~15.5V)
12. COMMAND(0XF6) \\ Set OTP offset value to +3 (0011)
    DATA(0X11) \\ 00011 $X_3X_2X_1X_0Y_5$, where $X_3X_2X_1X_0Y_5$ is the OTP offset value
    DATA(0x2A)
13. COMMAND(0XF8) \\ Send the OTP programming command.
14. Wait at least 2 seconds for programming wait time.
15. Disconnect an external Vout
16. Discharge the Vout's capacitor
17. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin

Verify the result:

18. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel.

10.28 Draw Line (83 H)

Given the starting point (X1, Y1) and the ending point (X2, Y2), a line will be drawn with the color specified.

The following example illustrates the line drawing procedure.

1. Enter the “draw line mode” by execute the command 83H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 01H
5. Set the finishing Y-coordinates, Y2. E.g., 01H
6. Set the color to RGB = (0,1,0) e.g., 07H followed by E0H

Result: A green line will be drawn between coordinates (0,0) and (1,1)

Remark: X1, X2 ≤131; X1 < X2

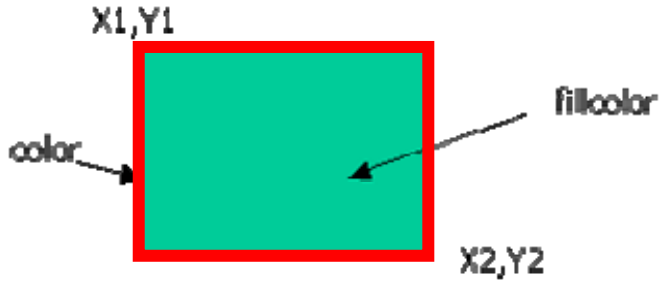
Y1, Y2 ≤159; Y1 < Y2

10.29 Fill Enable/Disable (92 H)

This command allows the fill color option to be enabled or disabled. This command is applicable to the Draw Rectangle feature. When the selection bit is “0”, the fill color option is disabled. When the selection bit is “1”, the fill color option is enabled.

10.30 Draw rectangle (84 H)

Given the starting point (X1, Y1) and the ending point (X2, Y2), specify the width and height of a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.



The following example illustrates the rectangle drawing procedure.

1. Enter the “draw rectangle mode” by execute the command 8AH
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 02H
5. Set the finishing Y-coordinates, Y2. E.g., 02H
6. Set the color to RGB = (1,0,0) e.g., F8H following by 00H
7. Set the filled color to RGB = (0,1,0) e.g., 07H following by E0H

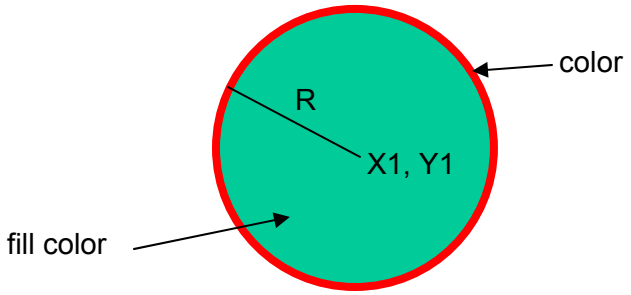
Result: A rectangle will be drawn at (0,0) to (2,2), filled green with red border

Remark: X1, X2 ≤131; X1 < X2

Y1, Y2 ≤159; Y1 < Y2

10.31 Draw Circle (86 H)

Given the center point (X1, Y1) and the radius R, a circle will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.



The following example illustrates the rectangle drawing procedure.

1. Enter the “draw circle mode” by execute the command 86H
2. Set the center X-coordinates, X1. E.g., 40H.
3. Set the center Y-coordinates, Y1. E.g., 40H.
4. Set the radius, R. E.g., 20H
5. Set the color to RGB = (1,0,0) e.g., F8H following by 00H
6. Set the filled color to RGB = (0,1,0) e.g., 07H following by E0H

Result: A circle will be drawn with center (64,64) and radius 32, filled green with red border

Remark: 0 ≤X1,Y1 ≤255

1 ≤R ≤255

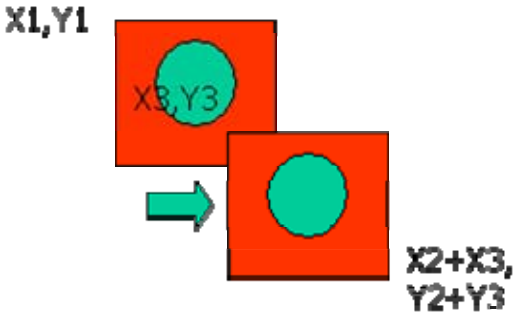
10.32 Copy (8A H)

Copy the rectangular region defined by the starting point (X1, Y1) and the ending point (X2, Y2) to location (X3, Y3). There are two possible results with the command copy executed depending on the setting of the start point coordinates and end point coordinates.

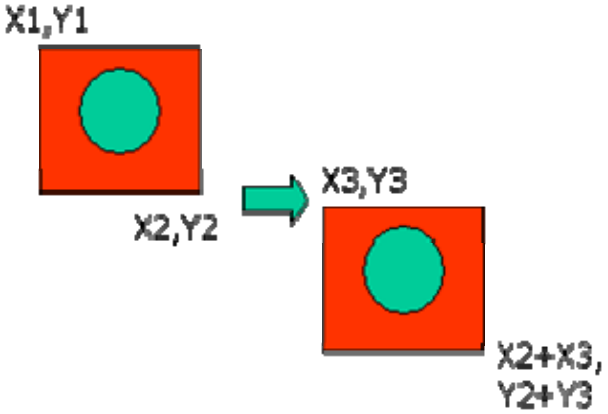
The following example illustrates the copy procedure.

Case 1 – The overlap region will superimpose.

1. Enter the “copy mode” by execute the command 84H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 02H
5. Set the finishing Y-coordinates, Y2. E.g., 02H
6. Set the New X-coordinates, X3. E.g., 01H
7. Set the New Y-coordinates, Y3. E.g., 01H



Case 2 – The original content remains unchanged



1. Enter the “copy mode” by execute the command 84H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 01H
5. Set the finishing Y-coordinates, Y2. E.g., 01H
6. Set the New X-coordinates, X3. E.g., 09H
7. Set the New Y-coordinates, Y3. E.g., 09H

Remark: X1, X2 ≤131; X1 < X2
Y1, Y2 ≤159; Y1 < Y2

10.33 Dim Window (8C H)

This command will dim the window area specify by starting point (X1, Y1) and the ending point (X2, Y2). After the execution of this command, the selected window area will be dimmed by 75% white. Additional execution of this command over the same window area will not change the data content.

Remark: X1, X2 ≤131; X1 < X2
Y1, Y2 ≤159; Y1 < Y2

10.34 Clear Window (8E H)

This command sets the window area specify by starting point (X1, Y1) and the ending point (X2, Y2) to clear the window display. The GDDRAM content of the window will be set to zero.

Remark: X1, X2 ≤131; X1 < X2
Y1, Y2 ≤159; Y1 < Y2

10.35 Status register read

The following parameters can be monitored by the status read register.

1. Various area scroll mode
2. Read modify mode ON/OFF
3. Column scan direction
4. Page scan direction
5. Display ON/OFF
6. Sleep mode ON/OFF
7. Display Normal/Inverse
8. Partial display mode ON/OFF

11 MAXIMUM RATINGS

Table 14 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{OUT}		-0.3 to 18	V
V_{CI}	Input Voltage	V_{SS}-0.3 to 4.0	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} and Vout be constrained to the range $V_{SS} < V_{DD} \leq V_{CI} < V_{OUT}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Table 15 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.6V, T_A = -40 to 85°C, measurement performs on IC level)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	System power supply pins of the logic block Range	Recommend Operating Voltage Possible Operating Voltage	2.4	2.7	3.6	V
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.2	V_{DD}	V_{DD}	V
V_{CI}	Booster Reference Supply Voltage Range (3)	Recommend Operating Voltage Possible Operating Voltage	V_{DD}	V_{DD}	3.6	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 7X DC-DC, 16-bit 8080 parallel bus writing AAAA HTcyc =3MHz, Typ. Osc. Freq., Display On, no panel attached.	-	650	950	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{OUT} = 16V, Voltage Generator On, 7X DC-DC Converter Enabled, R/W(WR) Halt, Typ. Osc. Freq., Display On, no panel attached.	-	500	800	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, R/W(WR) halt.	-	2	5	µA
V_{OUT}	LCD Driving Voltage Generator Output (V_{OUT} Pin)	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	8	-	19	V
V_{OH1}	Logic High Output Voltage	I_{OUT}=-100µA	0.9* V_{DD}	-	V_{DD}	V
V_{OL1}	Logic Low Output Voltage	I_{OUT}=100µA	0	-	0.1*V_{DD}	V
V_{IH1}	Logic High Input voltage		0.8* V_{DD}	-	V_{DD}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2* V_{DD}	V
I_{OH}	Logic High Output Current Source	V_{OUT} = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	V_{OUT} = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
ΔV_{OUT}	Variation of V_{OUT} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-2	0	2	%
R_O	SEG/COM output resistance		-	500	-	ohm
TC0	Average Temperature Gradient Flat Temperature Coefficient	Voltage Regulator Enabled	0	-0.10	-0.11	%/°C
TC1	Temperature Coefficient 1*		-0.12	-0.13	-0.16	%/°C
TC2	Temperature Coefficient 2* (POR)		-0.17	-0.21	-0.24	%/°C
TC3	Temperature Coefficient 3*		-0.25	-0.26	-0.27	%/°C

*The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref} \text{ at } 50^oC - V_{ref} \text{ at } 0\ ^oC}{50\ ^oC - 0\ ^oC} \times \frac{1}{V_{ref} \text{ at } 25\ ^oC} \times 100\ \%$$

13 AC CHARACTERISTICS

Table 16 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.7V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Fosc	Oscillation Frequency of Display Timing Generator for: 160 MUX Mode	Internal Oscillator Enabled (default), V_{DD} = 2.7V	374	380	394	kHz
F_{FRM}	Frame Frequency for: 160 MUX Mode	132 RGB x 160 Graphic Display Mode, Display ON, Internal Oscillator Enabled	73	75	77	Hz

Remarks: Fosc stands for the frequency value of internal oscillator

Table 17 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	130	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
PW_{CSH}	CS Pulse High Width	65	-	-	ns
PW_{CSL}	CS Pulse Low Width	65	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	50	ns
t_{ACC}	Data Access Time	15	-	200	ns
t_{OH}	Output Hold time	20	-	60	ns

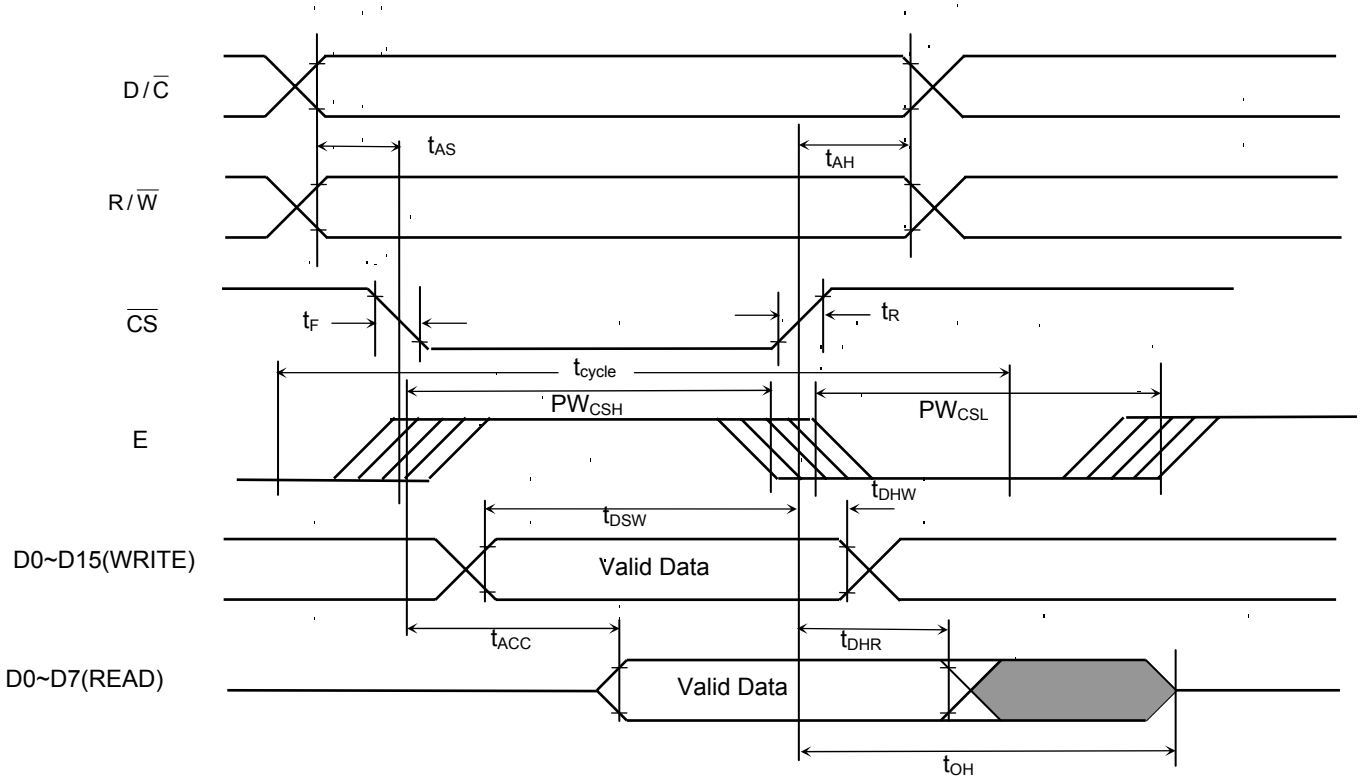
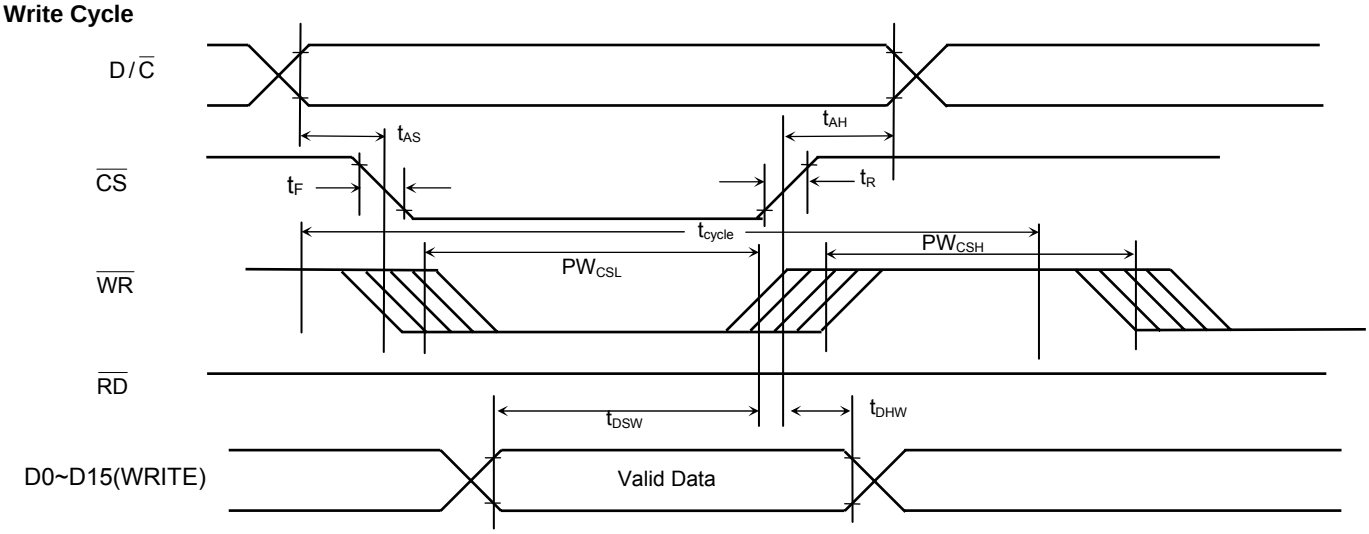


Figure 16 – 8-bit/16-bit Parallel 6800-series Interface Timing Characteristics

Table 18 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	130	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
PW_{CSH}	CS Pulse High Width	65	-	-	ns
PW_{CSL}	CS Pulse Low Width	65	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	50	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns

Write Cycle



Read Cycle

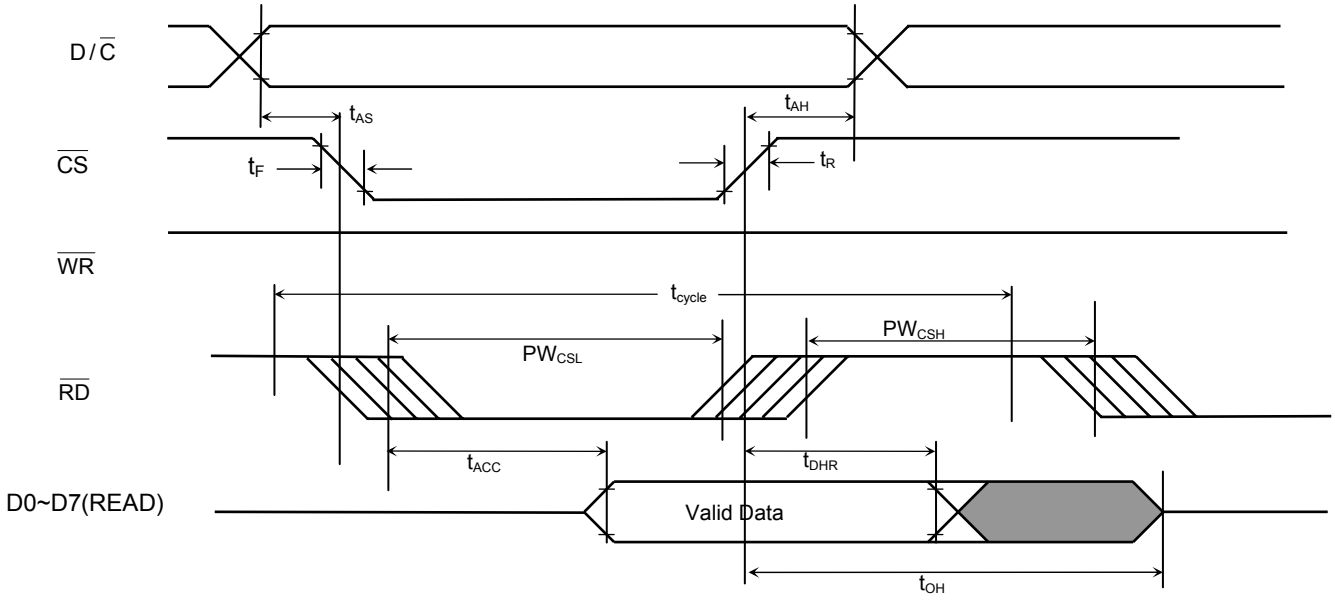


Figure 17 – 8-bit/16-bit Parallel 8080-series Interface Timing Characteristics

Table 19 – Parallel Timing Characteristics (TA = -40 to 85°C, V_{DD} = 2.4V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	250	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
PW_{CSH}	CS Pulse High Width	125	-	-	ns
PW_{CSL}	CS Pulse Low Width	125	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	50	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns

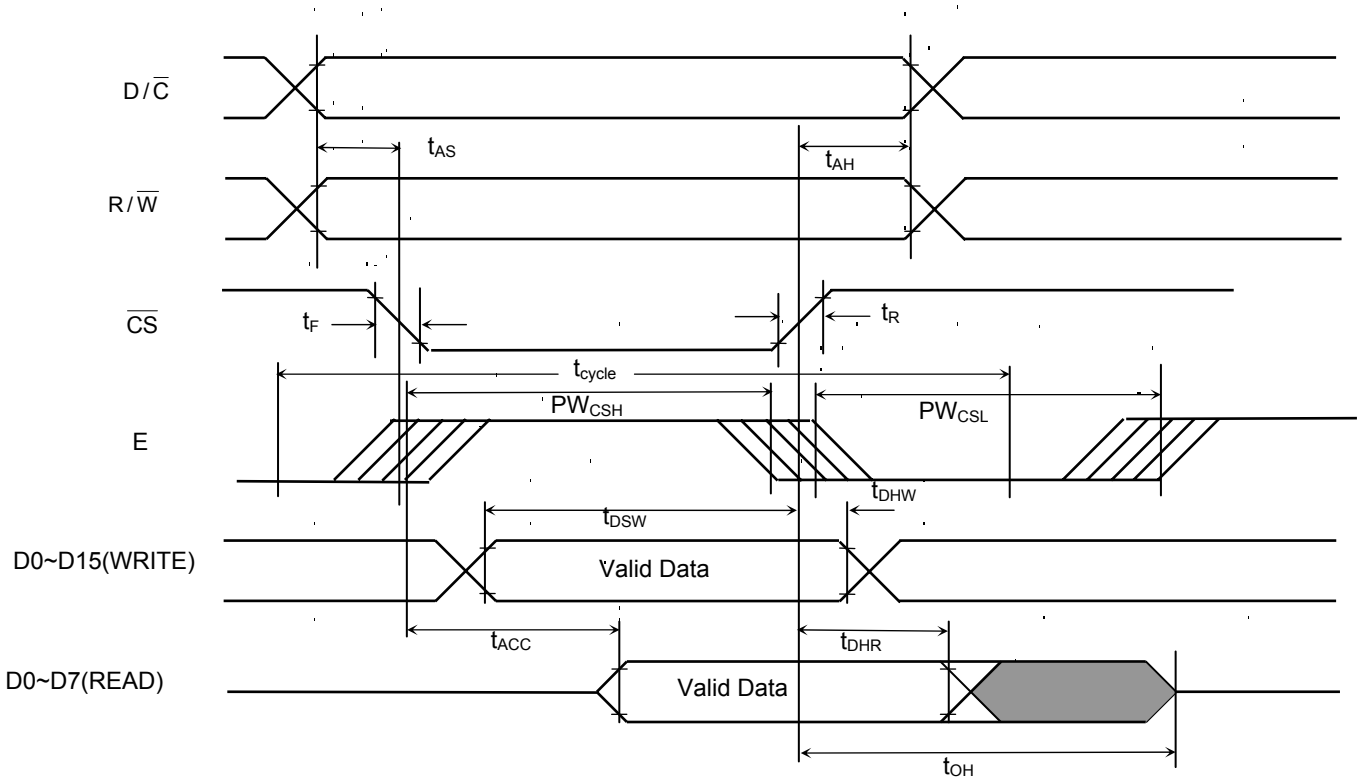
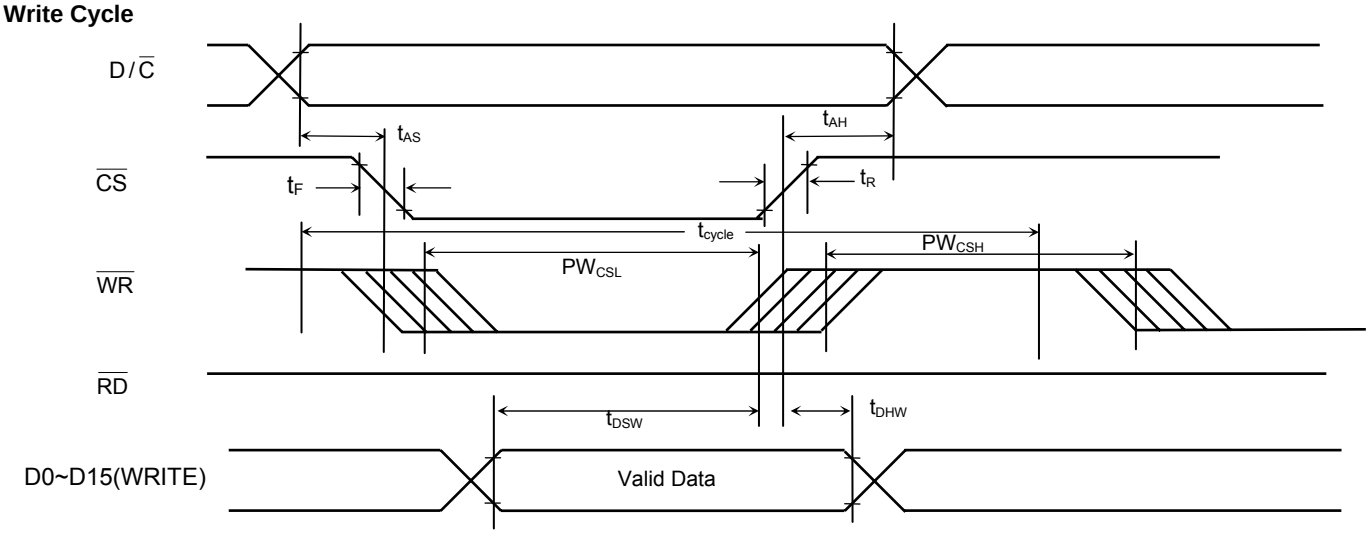


Figure 18 – 8-bit/16-bit Parallel 6800-series Interface Timing Characteristics

Table 20 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	250	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
PW_{CSH}	CS Pulse High Width	125	-	-	ns
PW_{CSL}	CS Pulse Low Width	125	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	50	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns

Write Cycle



Read Cycle

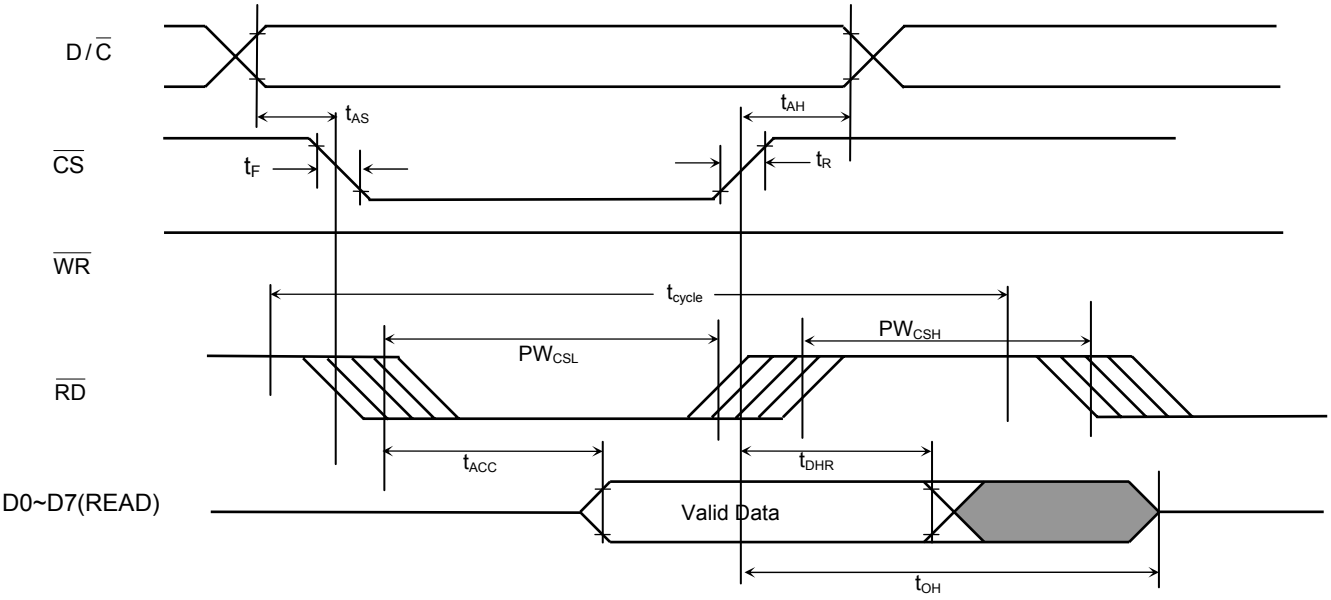


Figure 19 – 8-bit/16-bit Parallel 8080-series Interface Timing Characteristics

Table 21 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	66	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

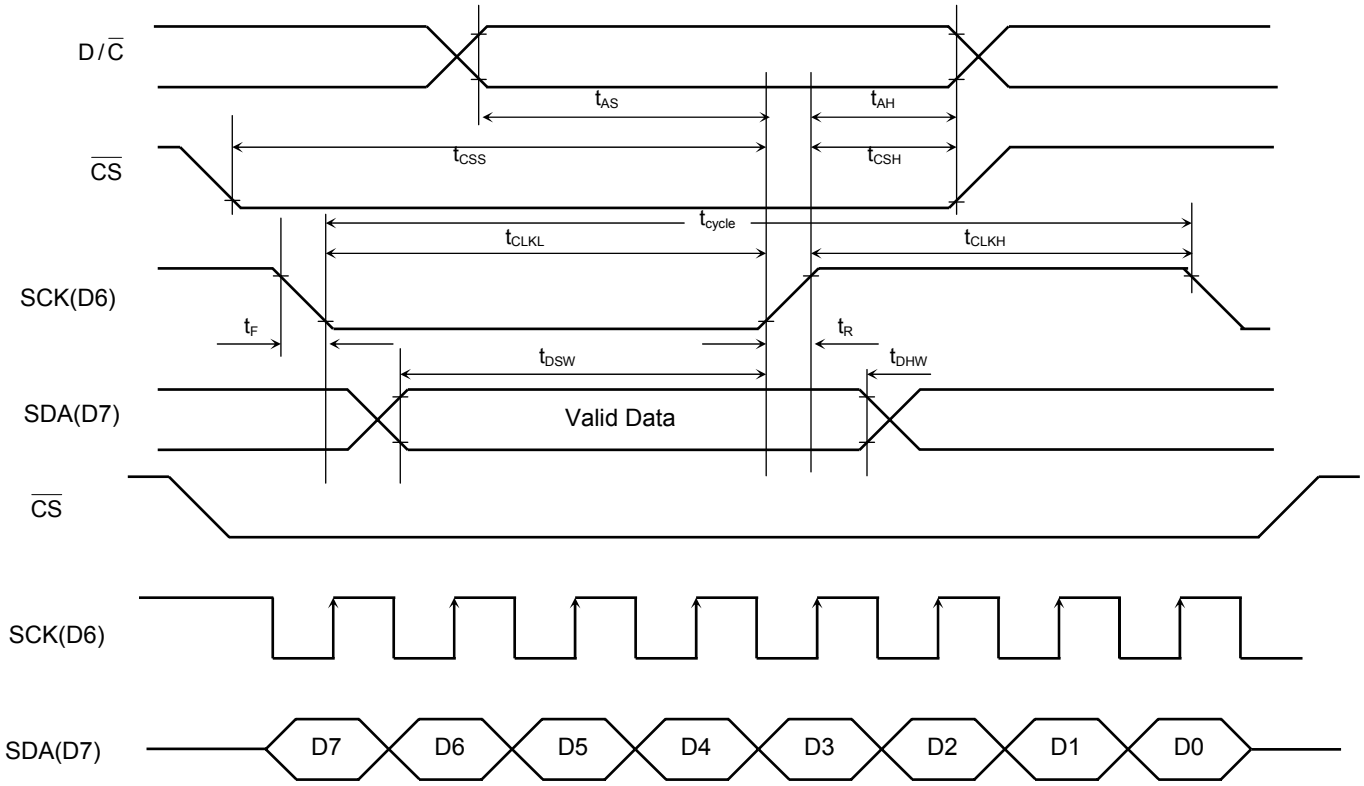


Figure 20 – 4 wire Serial Timing Characteristics (PS2=PS1=PS0=L)

Table 22 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	66	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

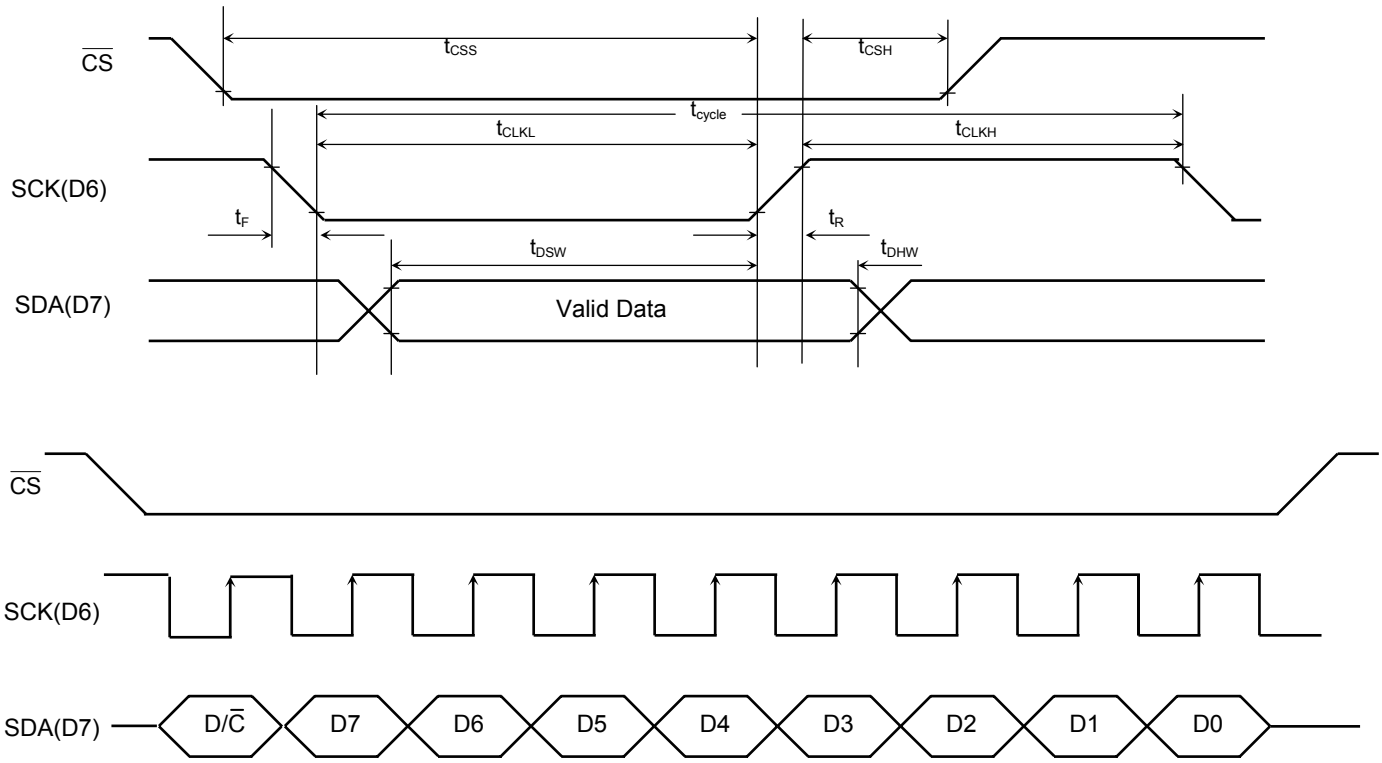


Figure 21 – 3 wire Serial Timing Characteristics (PS2=PS1=L, PS0=H)

Table 23 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	10	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

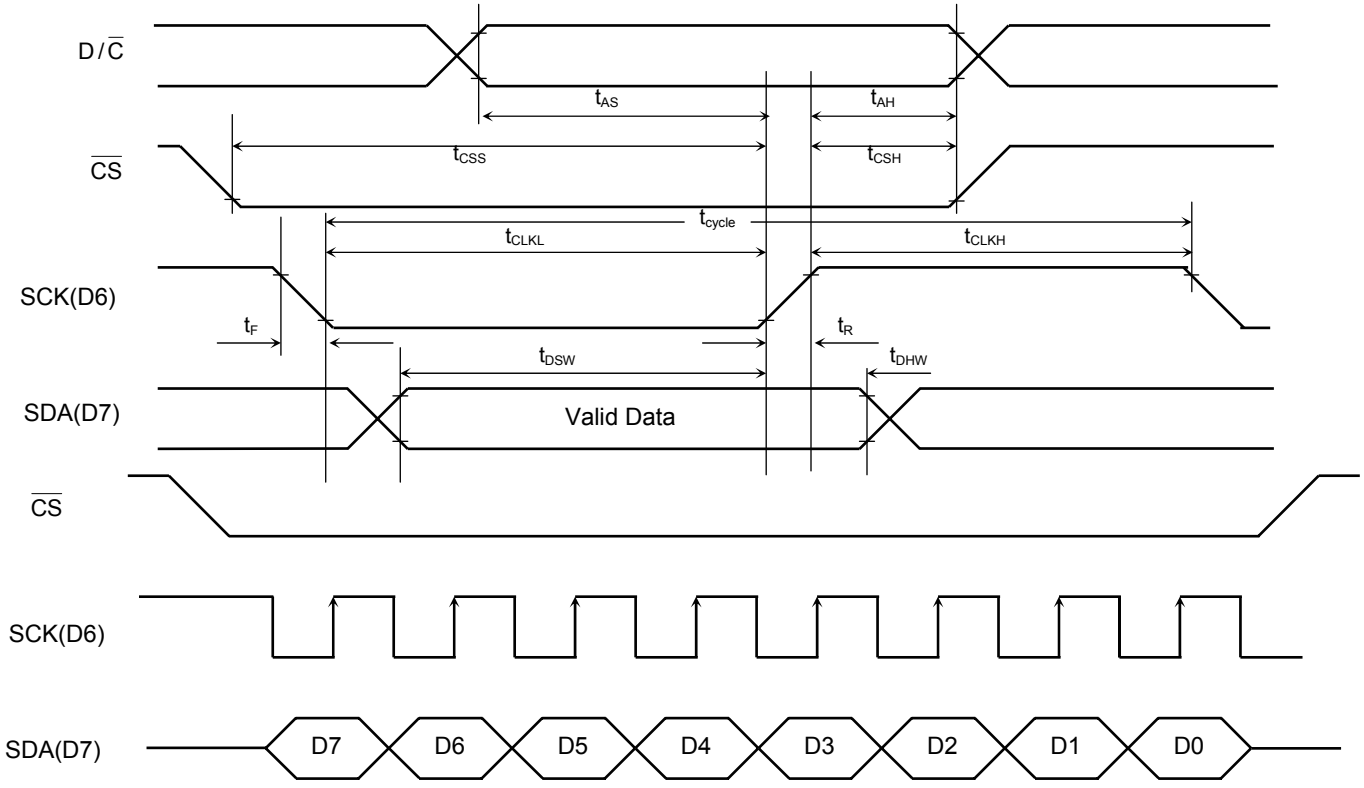


Figure 22 – 4 wire Serial Timing Characteristics (PS2=PS1=PS0=L)

Table 24 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	10	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

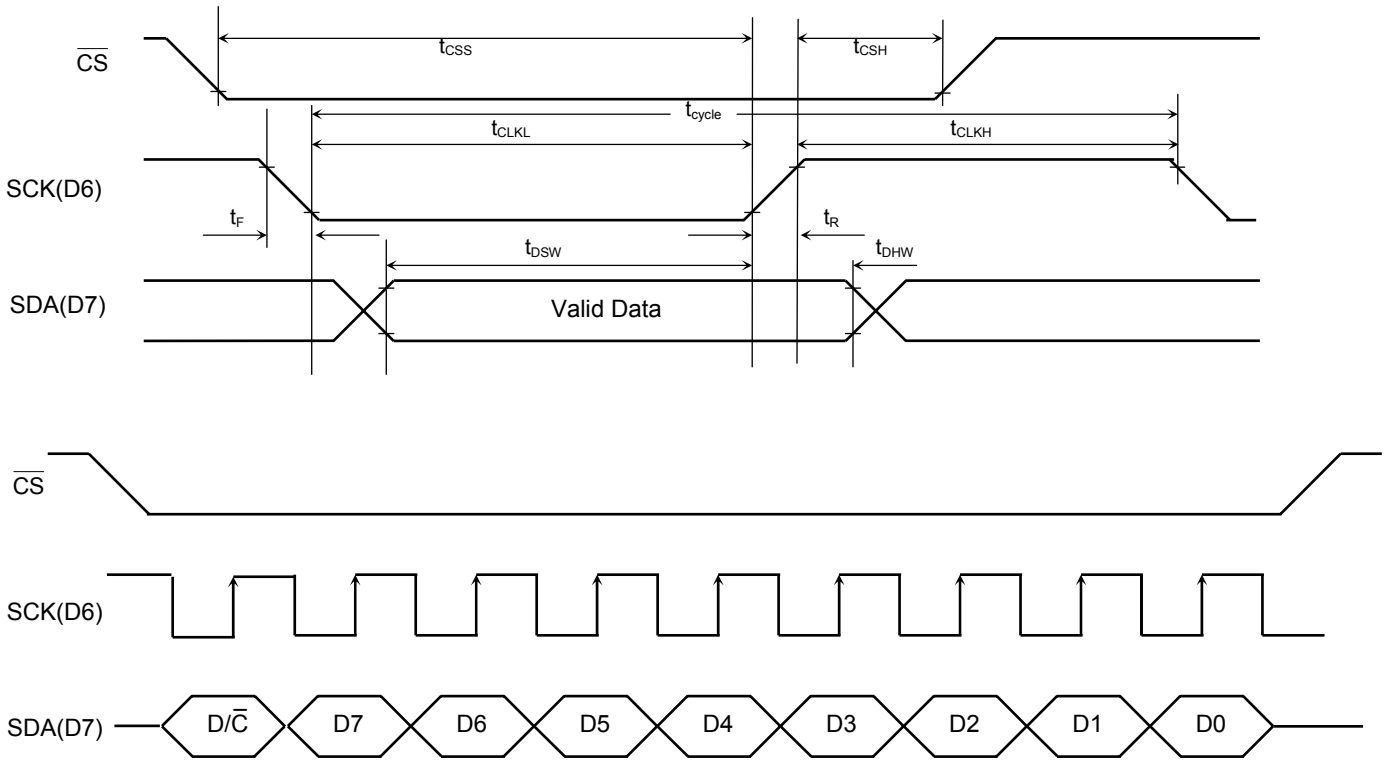
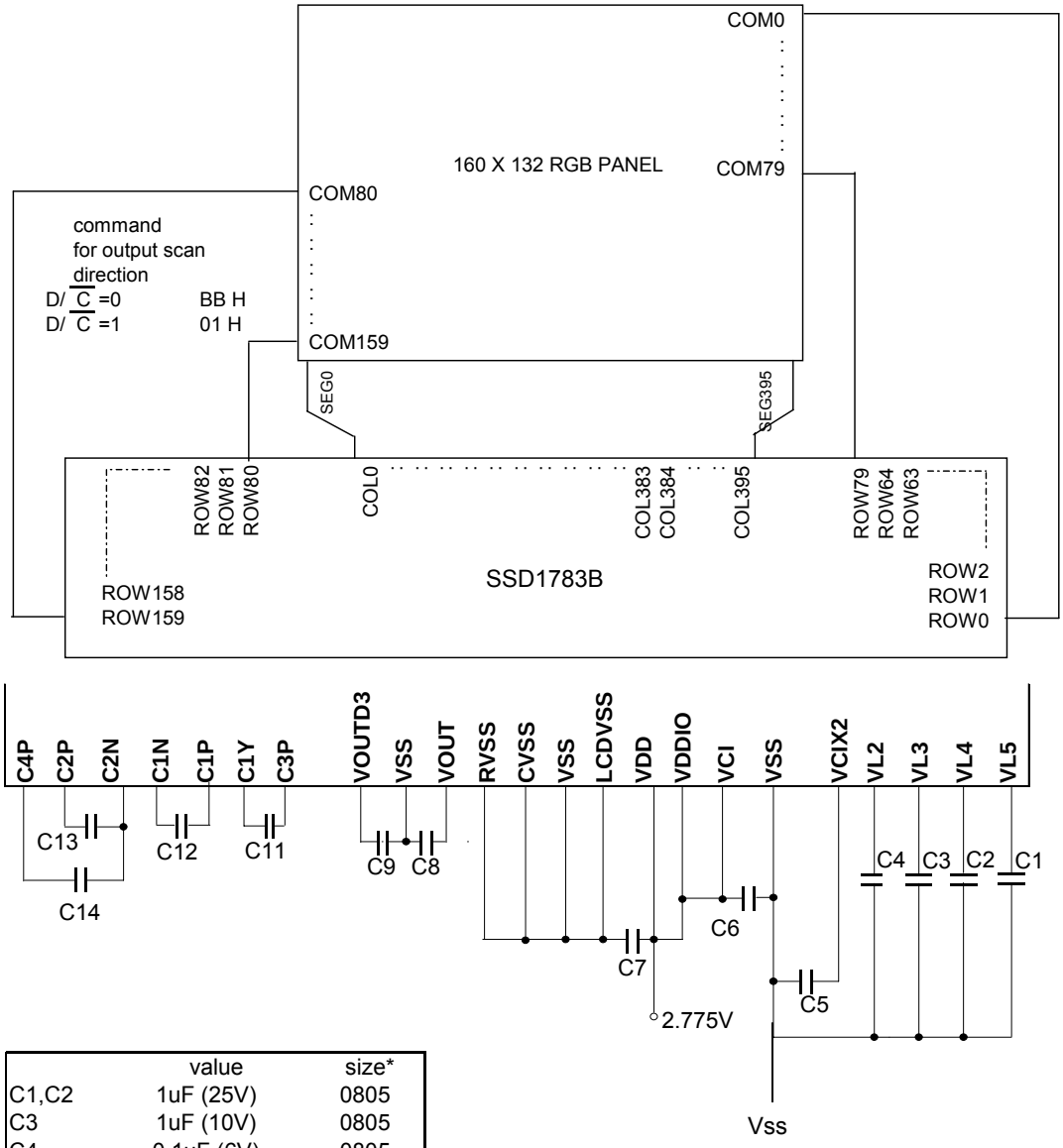


Figure 23 – 3 wire Serial Timing Characteristics (PS2=PS1=L, PS0=H)

14 APPLICATION EXAMPLES

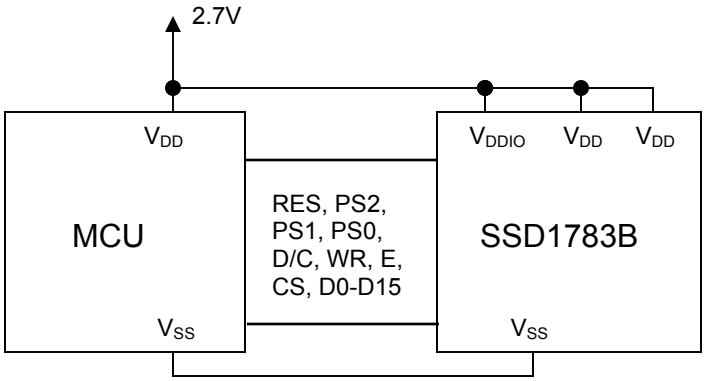


	value	size*
C1,C2	1uF (25V)	0805
C3	1uF (10V)	0805
C4	0.1uF (6V)	0805
C5	1uF (10V)	0805
C6,C7	1uF (6V)	0805
C8*	4.7uF (25V)	1210
C9	1uF (16V)	0805
C11,C12	1uF (25V)	0805
C13,C14	1uF (25V)	0805

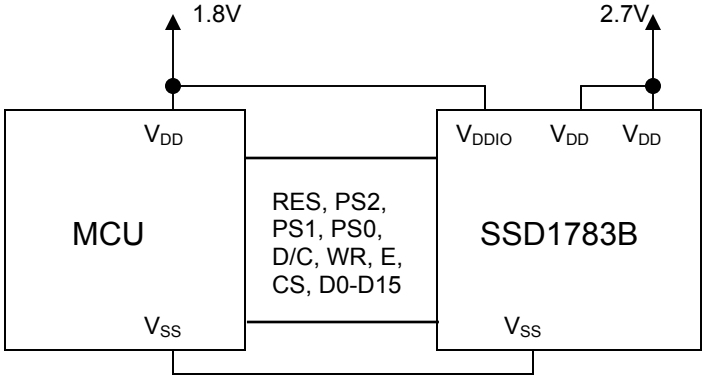
*For C8, part of it could be put on PCB to make the total cap value ~4.7uF if cap size is too big to place on COF
*the size is for reference only

V_{DD} = V_{DDIO} = V_{CI} = 2.775V
PS2='H', PS1=PS0='L' (16 bit 6800 bus)

Figure 24 - Application example



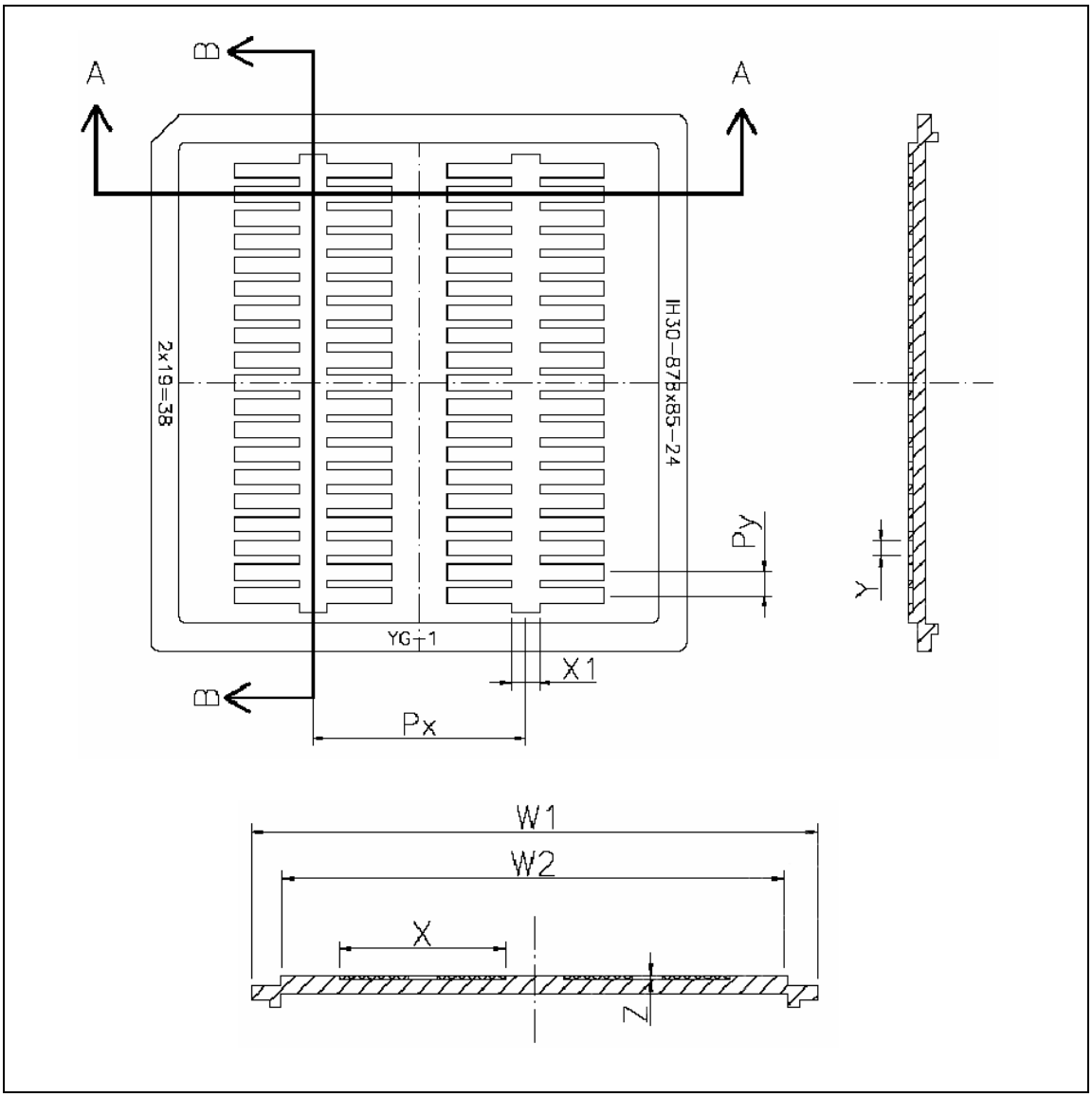
a) V_{DD}= V_{DDIO}= V_{CI}= V_{DD}(MCU) =2.7V



b) V_{DD}= V_{CI}=2.7V, V_{DDIO}= V_{DD}(MCU)=1.8V

Figure 25 - V_{DD}, V_{DDIO}, V_{CI} connections for (a) typical voltage MCU and (b) low voltage MCU

15 SSD1783BZ DIE TRAY DIMENSIONS

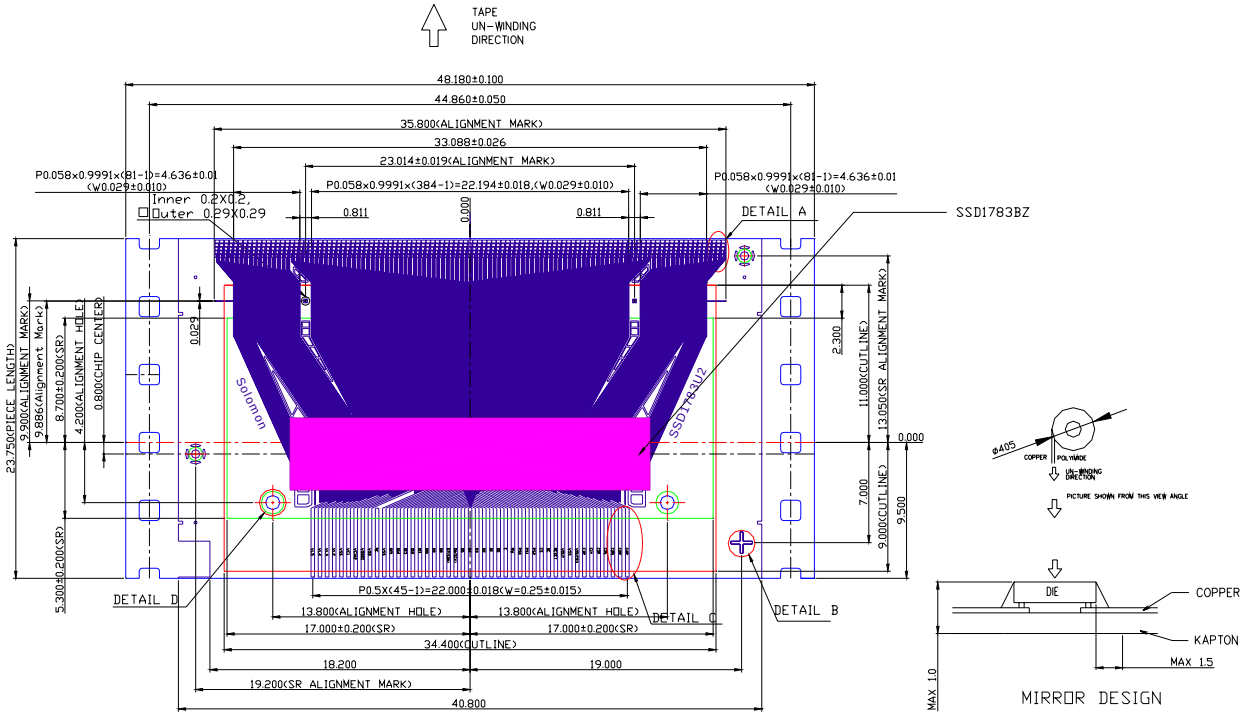


Spec	mm	(mil)
W1	$76.0^{+0.2}_{-0.1}$	(2992)
W2	$68.0^{+0.2}_{-0.1}$	(2677)
X1	4.0 ± 0.1	(158)
Px	30.10 ± 0.1	(1185)
Py	3.34 ± 0.1	(132)
X	22.30 ± 0.1	(878)
Y	2.16 ± 0.1	(85)
Z	0.61 ± 0.05	(24)
N	38	

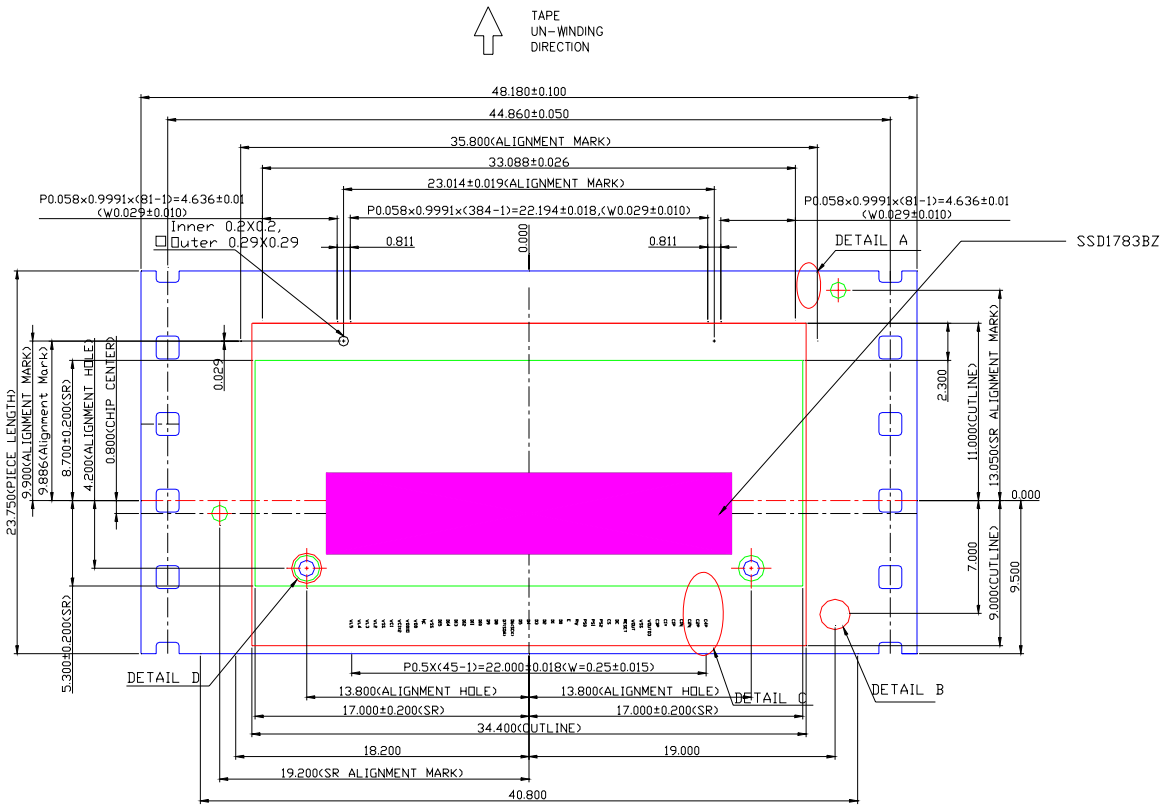
Figure 26 – SSD1783BZ Die Tray Dimension

16 APPENDIX

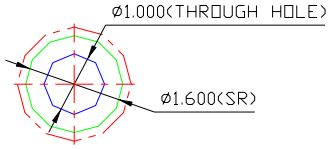
SSD1783BU2 Drawing 1



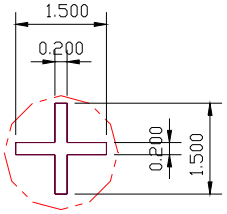
SSD1783BU2 Drawing 2



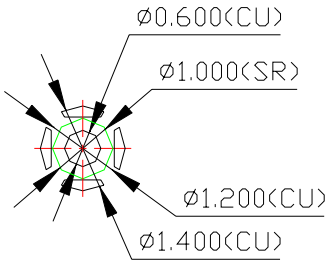
SSD1783BU2 Drawing 3



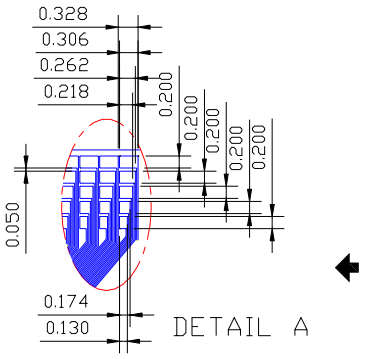
DETAIL D



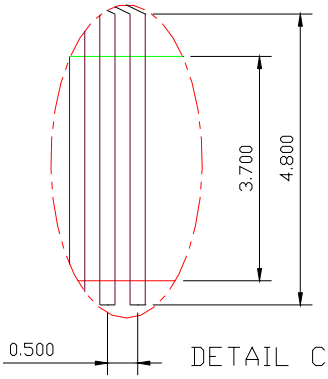
DETAIL B



SR ALIGNMENT MARK



DETAIL A



DETAIL C

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