SH1122

256 X 64 16 Grayscale
Dot Matrix OLED/PLED Driver with Controller

Features

- Support maximum 256 X 64 dot matrix panel with 16 grayscale
- Embedded 256 X 64 X 4bits SRAM
- Operating voltage:
  - I/O voltage supply: V_{DD1} = 1.65V - 3.5V
  - Logic voltage supply: V_{DD2} = 1.65V - 3.5V
    $V_{DD1} = V_{DD2}$
  - DC-DC voltage supply: AV_{DD} = 2.4V - 3.5V
  - OLED Operating voltage supply: V_{PP} = 7.0V -14V
- Maximum segment output current: 500μA
- Maximum common sink current: 128mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, 3 wire/4 wire serial peripheral interface
- 400KHz fast I^2C bus interface
- Programmable frame frequency and multiplexing ratio
- Row re-mapping and column re-mapping (ADC)
- Vertical scrolling
- On-chip oscillator
- Available internal DC-DC converter
- 256-step contrast control on monochrome passive OLED panel
- Low power consumption
  - Sleep mode: < 5μA
- Wide range of operating temperatures: -40 to +85°C
- Available in COG form

General Description

SH1122 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SH1122 consists of 256 segments, 64 commons with 16 grayscale that can support a maximum display resolution of 256 X 64. It is designed for Common Cathode type OLED panel.

SH1122 embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. SH1122 is suitable for a wide range of compact portable applications, such as car audio, and calculator, etc.

Block Diagram

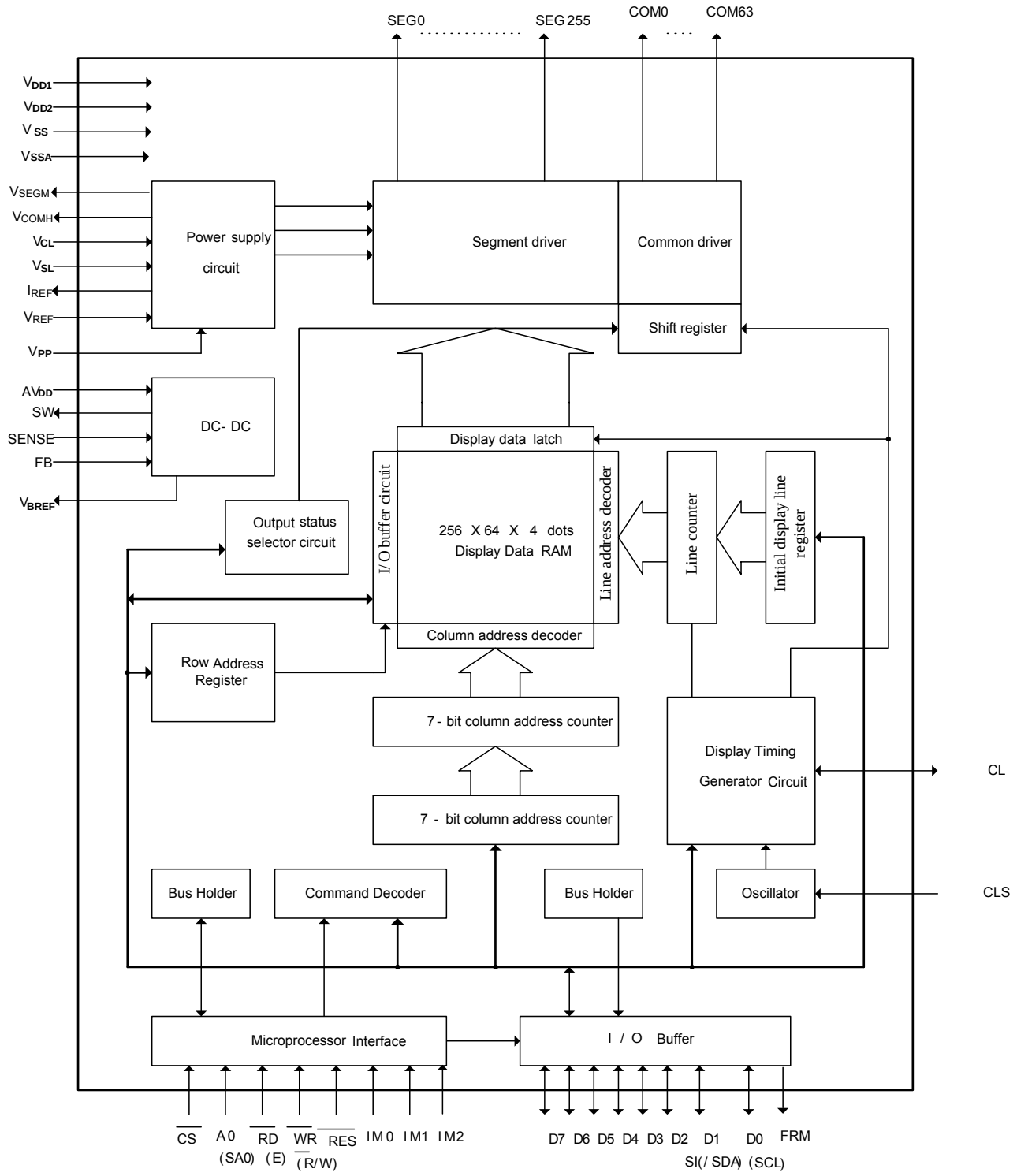


Figure. 1 SH1122 Block Diagram

Pad Description

Power Supply

Pad No.	Symbol	I/O	Description
57,58	V_{DD2}	Supply	1.65 - 3.5V power supply input pad for logic.VDD2 should be equal to VDD1.
64,65	V_{DD1}	Supply	1.65 - 3.5Vpower supply input pad
60	V_{DD1}	Supply	1.65 - 3.5V power supply output for pad option
52,53	AV_{DD}	Supply	2.4- 3.5V power supply pad for the internal buffer of the DC-DC voltage converter
40	V_{SSA}	Supply	Ground for VSL.
41,42,43	V_{SS}	Supply	Ground for analog, logic&buffer respectively.
62,67	V_{SS}	Supply	Ground output for pad option
2~5,36~39,86~89	V_{PP}	Supply	This is the most positive voltage supply pad of the chip It should be supplied externally
29~31	V_{SL}	Supply	This is a segment voltage reference pad A capacitor should be connected between this pad and Vss
44~50	V_{CL}	Supply	This is a common voltage reference pad This pad should be connected to Vss externally

OLED Driver Supplies

Pad No.	Symbol	I/O	Description
32,33	V_{REF}	I	This is a voltage reference pad for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to V_{PP}.
34,35	I_{REF}	O	This is a segment current reference pad A resistor should be connected between this pad and Vss. Set the current at 15.625μA
26~28	V_{COMH}	O	This is a pad for the voltage output high level for common signals A capacitor should be connected between this pad and Vss
23~25	V_{SEGM}	O	This is a pad for the voltage output level for segment pre-charge. A capacitor should be connected between this pad and Vss.
56	SW	O	This is an output pad driving the gate of the external NMOS of the booster circuit
54	FB	I	This is a feedback resistor input pad for the booster circuit It is used to adjust the booster output voltage level, V_{PP}
51	SENSE	I	This is a source current pad of the external NMOS of the booster circuit
55	V_{BREF}	O	This is an internal voltage reference pad for booster circuit

System Bus Connection Pads

<table>
<tr><th>Pad No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>73</td><td>CL</td><td>I/O</td><td>This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.</td></tr>
<tr><td>59</td><td>CLS</td><td>I</td><td>This is the internal clock enable pad.
CLS = “H”: Internal oscillator circuit is enabled.
CLS = “L”: Internal oscillator circuit is disabled (requires external input).
When CLS = “L”, an external clock source must be connected to the CL pad for normal operation.</td></tr>
<tr><td>61
63
66</td><td>IM0
IM1
IM2</td><td>I</td><td>These are the MPU interface mode select pads.
<table>
<tr><th></th><th>8080</th><th>I²C</th><th>6800</th><th>4-wire SPI</th><th>3-wire SPI</th></tr>
<tr><td>IM0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>IM1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>IM2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>68</td><td>$\overline{CS}$</td><td>I</td><td>This pad is the chip select input. When $\overline{CS}$ = “L”, then the chip select becomes active, and data/command I/O is enabled.</td></tr>
<tr><td>69</td><td>$\overline{RES}$</td><td>I</td><td>This is a reset signal input pad. When $\overline{RES}$ is set to “L”, the settings are initialized.
The reset operation is performed by the $\overline{RES}$ signal level.</td></tr>
<tr><td>70</td><td>A0
(SA0)</td><td>I</td><td>This is the Data/Command control pad that determines whether the data bits are data or a command.
A0 = “H”: the inputs at D0 to D7 are treated as display data.
A0 = “L”: the inputs at D0 to D7 are transferred to the command registers.
In I²C interface, this pad serves as SA0 to distinguish the different address of OLED driver.</td></tr>
<tr><td>71</td><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
When connected to a 6800 Series MPU: This is the read/write control signal input terminal.
When R/$\overline{W}$ = “H”: Read.
When R/$\overline{W}$ = “L”: Write.</td></tr>
<tr><td>72</td><td>$\overline{RD}$
(E)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the SH1122 data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.</td></tr>
<tr><td>78~85</td><td>D0 - D7
(SCL)
(SI /SDA)</td><td>I/O
I
I</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance.
When the I₂C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDA). At this time, D2 to D7 are set to high impedance.
When the chip select is inactive, D0 to D7 are set to high impedance.</td></tr>
<tr><td>77</td><td>FRM</td><td>O</td><td>This pad is No Connection pad. Its signal varies with the frame frequency. Its voltage is equal to VDD1 when the last common output of every frame is active, and is equal to Vss during other time.</td></tr>
</table>

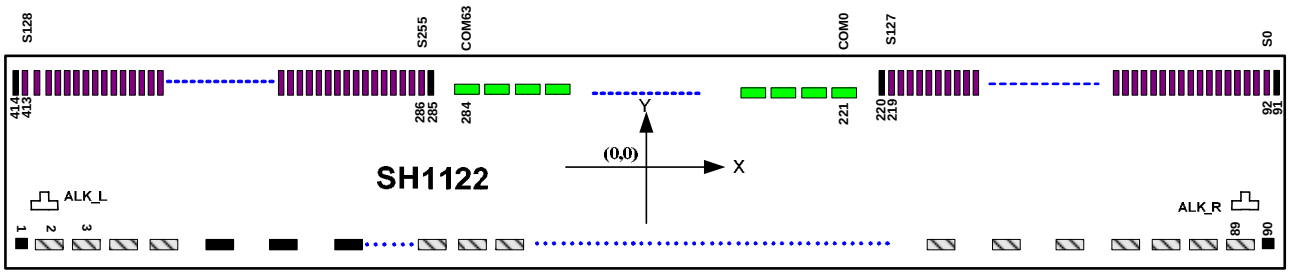
OLED Drive Pads

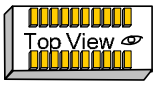
Pad No.	Symbol	I/O	Description
221~284	COM0 - 63	O	These pads are Common signal output for OLED display.
92~219,413~286	SEG0 - 255	O	These pads are Segment signal output for OLED display.

Test Pads

Pad No.	Symbol	I/O	Description
74	TEST1	I	Test pads, internal pull low, no connection for user.
75	TEST2	O	Test pads, no connection for user.
76	TEST3	I	Test pads, no connection for user.
1, 6~22,90, 91,220,285,414	Dummy	-	Dummy pads, no connection for user.

Pad Configuration





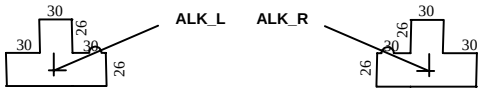
Chip Outline Dimensions

Item	Pad No.	Size (μm)	
		X	Y
Chip boundary	-	16454	920
Chip height	All pads	300	
Bump size	I/O	110	40
	SEG	26	70
	COM	64	39
	Dummy (No.1,90)	46	40
	Dummy (No.91,220,285,414)	26	70
	Dummy (No.6~22)	110	40
Pad pitch	COM	80	
	SEG	41	
	I/O	130 & 195 & 260	
Bump height	All pads	9±2	

Alignment Mark Location

unit: μm

NO	X	Y
ALK_L	-8052	-289
ALK_R	8052	-289



Pad location(Total :414 pads)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY	-8130	-355.00	82	D[4]	6672	-355.00	163	SEG[71]	5117	353.50	244	COM[23]	760	324.50
2	VPP	-8037	-355.00	83	D[5]	6932	-355.00	164	SEG[72]	5076	353.50	245	COM[24]	680	324.50
3	VPP	-7907	-355.00	84	D[6]	7192	-355.00	165	SEG[73]	5035	353.50	246	COM[25]	600	324.50
4	VPP	-7777	-355.00	85	D[7]	7452	-355.00	166	SEG[74]	4994	353.50	247	COM[26]	520	324.50
5	VPP	-7647	-355.00	86	VPP	7647	-355.00	167	SEG[75]	4953	353.50	248	COM[27]	440	324.50
6	DUMMY	-7452	-355.00	87	VPP	7777	-355.00	168	SEG[76]	4912	353.50	249	COM[28]	360	324.50
7	DUMMY	-7192	-355.00	88	VPP	7907	-355.00	169	SEG[77]	4871	353.50	250	COM[29]	280	324.50
8	DUMMY	-6932	-355.00	89	VPP	8037	-355.00	170	SEG[78]	4830	353.50	251	COM[30]	200	324.50
9	DUMMY	-6672	-355.00	90	DUMMY	8130	-355.00	171	SEG[79]	4789	353.50	252	COM[31]	120	324.50
10	DUMMY	-6412	-355.00	91	DUMMY	8151	353.50	172	SEG[80]	4748	353.50	253	COM[32]	40	324.50
11	DUMMY	-6152	-355.00	92	SEG[0]	8110	353.50	173	SEG[81]	4707	353.50	254	COM[33]	-120	324.50
12	DUMMY	-5892	-355.00	93	SEG[1]	8069	353.50	174	SEG[82]	4666	353.50	255	COM[34]	-200	324.50
13	DUMMY	-5632	-355.00	94	SEG[2]	8028	353.50	175	SEG[83]	4625	353.50	256	COM[35]	-280	324.50
14	DUMMY	-5372	-355.00	95	SEG[3]	7987	353.50	176	SEG[84]	4584	353.50	257	COM[36]	-360	324.50
15	DUMMY	-5112	-355.00	96	SEG[4]	7946	353.50	177	SEG[85]	4543	353.50	258	COM[37]	-440	324.50
16	DUMMY	-4852	-355.00	97	SEG[5]	7905	353.50	178	SEG[86]	4502	353.50	259	COM[38]	-520	324.50
17	DUMMY	-4592	-355.00	98	SEG[6]	7864	353.50	179	SEG[87]	4461	353.50	260	COM[39]	-600	324.50
18	DUMMY	-4332	-355.00	99	SEG[7]	7823	353.50	180	SEG[88]	4420	353.50	261	COM[40]	-680	324.50
19	DUMMY	-4072	-355.00	100	SEG[8]	7782	353.50	181	SEG[89]	4379	353.50	262	COM[41]	-760	324.50
20	DUMMY	-3812	-355.00	101	SEG[9]	7741	353.50	182	SEG[90]	4338	353.50	263	COM[42]	-840	324.50
21	DUMMY	-3552	-355.00	102	SEG[10]	7700	353.50	183	SEG[91]	4297	353.50	264	COM[43]	-920	324.50
22	DUMMY	-3273	-355.00	103	SEG[11]	7659	353.50	184	SEG[92]	4256	353.50	265	COM[44]	-1080	324.50
23	VSEGM	-3143	-355.00	104	SEG[12]	7618	353.50	185	SEG[93]	4215	353.50	266	COM[45]	-1160	324.50
24	VSEGM	-3013	-355.00	105	SEG[13]	7577	353.50	186	SEG[94]	4174	353.50	267	COM[46]	-1240	324.50
25	VSEGM	-2883	-355.00	106	SEG[14]	7536	353.50	187	SEG[95]	4133	353.50	268	COM[47]	-1320	324.50
26	VCOMH	-2753	-355.00	107	SEG[15]	7495	353.50	188	SEG[96]	4092	353.50	269	COM[48]	-1400	324.50
27	VCOMH	-2623	-355.00	108	SEG[16]	7454	353.50	189	SEG[97]	4051	353.50	270	COM[49]	-1480	324.50
28	VCOMH	-2493	-355.00	109	SEG[17]	7413	353.50	190	SEG[98]	4010	353.50	271	COM[50]	-1560	324.50
29	VSL	-2363	-355.00	110	SEG[18]	7372	353.50	191	SEG[99]	3969	353.50	272	COM[51]	-1640	324.50
30	VSL	-2233	-355.00	111	SEG[19]	7331	353.50	192	SEG[100]	3928	353.50	273	COM[52]	-1720	324.50
31	VSL	-2103	-355.00	112	SEG[20]	7290	353.50	193	SEG[101]	3887	353.50	274	COM[53]	-1800	324.50
32	VREF	-1973	-355.00	113	SEG[21]	7249	353.50	194	SEG[102]	3846	353.50	275	COM[54]	-1880	324.50
33	VREF	-1843	-355.00	114	SEG[22]	7208	353.50	195	SEG[103]	3805	353.50	276	COM[55]	-1960	324.50
34	IREF	-1713	-355.00	115	SEG[23]	7167	353.50	196	SEG[104]	3764	353.50	277	COM[56]	-2040	324.50
35	IREF	-1583	-355.00	116	SEG[24]	7126	353.50	197	SEG[105]	3723	353.50	278	COM[57]	-2120	324.50
36	VPP	-1453	-355.00	117	SEG[25]	7085	353.50	198	SEG[106]	3682	353.50	279	COM[58]	-2200	324.50
37	VPP	-1323	-355.00	118	SEG[26]	7044	353.50	199	SEG[107]	3641	353.50	280	COM[59]	-2280	324.50
38	VPP	-1193	-355.00	119	SEG[27]	7003	353.50	200	SEG[108]	3600	353.50	281	COM[60]	-2360	324.50
39	VPP	-1063	-355.00	120	SEG[28]	6962	353.50	201	SEG[109]	3559	353.50	282	COM[61]	-2440	324.50
40	VSSA	-933	-355.00	121	SEG[29]	6921	353.50	202	SEG[110]	3518	353.50	283	COM[62]	-2520	324.50
41	VSS(ana)	-803	-355.00	122	SEG[30]	6880	353.50	203	SEG[111]	3477	353.50	284	COM[63]	-2600	324.50
42	VSS(logic)	-673	-355.00	123	SEG[31]	6839	353.50	204	SEG[112]	3436	353.50	285	DUMMY	-2780	353.50
43	VSS(buf)	-543	-355.00	124	SEG[32]	6798	353.50	205	SEG[113]	3395	353.50	286	SEG[255]	-2821	353.50
44	VCL	-413	-355.00	125	SEG[33]	6757	353.50	206	SEG[114]	3354	353.50	287	SEG[254]	-2862	353.50
45	VCL	-283	-355.00	126	SEG[34]	6716	353.50	207	SEG[115]	3313	353.50	288	SEG[253]	-2903	353.50
46	VCL	-153	-355.00	127	SEG[35]	6675	353.50	208	SEG[116]	3272	353.50	289	SEG[252]	-2944	353.50
47	VCL	-23	-355.00	128	SEG[36]	6634	353.50	209	SEG[117]	3231	353.50	290	SEG[251]	-2985	353.50
48	VCL	107	-355.00	129	SEG[37]	6593	353.50	210	SEG[118]	3190	353.50	291	SEG[250]	-3026	353.50
49	VCL	237	-355.00	130	SEG[38]	6552	353.50	211	SEG[119]	3149	353.50	292	SEG[249]	-3067	353.50
50	VCL	367	-355.00	131	SEG[39]	6511	353.50	212	SEG[120]	3108	353.50	293	SEG[248]	-3108	353.50
51	SENSE	562	-355.00	132	SEG[40]	6470	353.50	213	SEG[121]	3067	353.50	294	SEG[247]	-3149	353.50
52	AVDD	757	-355.00	133	SEG[41]	6429	353.50	214	SEG[122]	3026	353.50	295	SEG[246]	-3190	353.50
53	AVDD	887	-355.00	134	SEG[42]	6388	353.50	215	SEG[123]	2985	353.50	296	SEG[245]	-3231	353.50
54	FB	1017	-355.00	135	SEG[43]	6347	353.50	216	SEG[124]	2944	353.50	297	SEG[244]	-3272	353.50
55	VBREF	1147	-355.00	136	SEG[44]	6306	353.50	217	SEG[125]	2903	353.50	298	SEG[243]	-3313	353.50
56	SW	1342	-355.00	137	SEG[45]	6265	353.50	218	SEG[126]	2862	353.50	299	SEG[242]	-3354	353.50
57	VDD2	1537	-355.00	138	SEG[46]	6224	353.50	219	SEG[127]	2821	353.50	300	SEG[241]	-3395	353.50
58	VDD2	1667	-355.00	139	SEG[47]	6183	353.50	220	DUMMY	2780	353.50	301	SEG[240]	-3436	353.50
59	CLS	1862	-355.00	140	SEG[48]	6142	353.50	221	COM[0]	2600	324.50	302	SEG[239]	-3477	353.50
60	VDD1	2057	-355.00	141	SEG[49]	6101	353.50	222	COM[1]	2520	324.50	303	SEG[238]	-3518	353.50
61	IM0	2252	-355.00	142	SEG[50]	6060	353.50	223	COM[2]	2440	324.50	304	SEG[237]	-3559	353.50
62	VSS	2447	-355.00	143	SEG[51]	6019	353.50	224	COM[3]	2360	324.50	305	SEG[236]	-3600	353.50
63	IM1	2642	-355.00	144	SEG[52]	5978	353.50	225	COM[4]	2280	324.50	306	SEG[235]	-3641	353.50
64	VDD1	2837	-355.00	145	SEG[53]	5937	353.50	226	COM[5]	2200	324.50	307	SEG[234]	-3682	353.50
65	VDD1	2967	-355.00	146	SEG[54]	5896	353.50	227	COM[6]	2120	324.50	308	SEG[233]	-3723	353.50
66	IM2	3162	-355.00	147	SEG[55]	5855	353.50	228	COM[7]	2040	324.50	309	SEG[232]	-3764	353.50
67	VSS	3357	-355.00	148	SEG[56]	5814	353.50	229	COM[8]	1960	324.50	310	SEG[231]	-3805	353.50
68	CSB	3552	-355.00	149	SEG[57]	5773	353.50	230	COM[9]	1880	324.50	311	SEG[230]	-3846	353.50
69	RESB	3812	-355.00	150	SEG[58]	5732	353.50	231	COM[10]	1800	324.50	312	SEG[229]	-3887	353.50
70	A0	4072	-355.00	151	SEG[59]	5691	353.50	232	COM[11]	1720	324.50	313	SEG[228]	-3928	353.50
71	WRB	4332	-355.00	152	SEG[60]	5650	353.50	233	COM[12]	1640	324.50	314	SEG[227]	-3969	353.50
72	RDB	4592	-355.00	153	SEG[61]	5609	353.50	234	COM[13]	1560	324.50	315	SEG[226]	-4010	353.50
73	CL	4787	-355.00	154	SEG[62]	5568	353.50	235	COM[14]	1480	324.50	316	SEG[225]	-4051	353.50
74	TEST1	4917	-355.00	155	SEG[63]	5527	353.50	236	COM[15]	1400	324.50	317	SEG[224]	-4092	353.50
75	TEST2	5047	-355.00	156	SEG[64]	5404	353.50	237	COM[16]	1320	324.50	318	SEG[223]	-4133	353.50
76	TEST3	5177	-355.00	157	SEG[65]	5363	353.50	238	COM[17]	1240	324.50	319	SEG[222]	-4174	353.50
77	FRM	5372	-355.00	158	SEG[66]	5322	353.50	239	COM[18]	1160	324.50	320	SEG[221]	-4215	353.50
78	D[0]	5632	-355.00	159	SEG[67]	5281	353.50	240	COM[19]	1080	324.50	321	SEG[220]	-4256	353.50
79	D[1]	5892	-355.00	160	SEG[68]	5240	353.50	241	COM[20]	1000	324.50	322	SEG[219]	-4297	353.50
80	D[2]	6152	-355.00	161	SEG[69]	5199	353.50	242	COM[21]	920	324.50	323	SEG[218]	-4338	353.50
81	D[3]	6412	-355.00	162	SEG[70]	5158	353.50	243	COM[22]	840	324.50	324	SEG[217]	-4379	353.50

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
325	SEG[216]	-4420	353.50	406	SEG[135]	-7823	353.50
326	SEG[215]	-4461	353.50	407	SEG[134]	-7864	353.50
327	SEG[214]	-4502	353.50	408	SEG[133]	-7905	353.50
328	SEG[213]	-4543	353.50	409	SEG[132]	-7946	353.50
329	SEG[212]	-4584	353.50	410	SEG[131]	-7987	353.50
330	SEG[211]	-4625	353.50	411	SEG[130]	-8028	353.50
331	SEG[210]	-4666	353.50	412	SEG[129]	-8069	353.50
332	SEG[209]	-4707	353.50	413	SEG[128]	-8110	353.50
333	SEG[208]	-4748	353.50	414	DUMMY	-8151	353.50
334	SEG[207]	-4789	353.50				
335	SEG[206]	-4830	353.50				
336	SEG[205]	-4871	353.50				
337	SEG[204]	-4912	353.50				
338	SEG[203]	-4953	353.50				
339	SEG[202]	-4994	353.50				
340	SEG[201]	-5035	353.50				
341	SEG[200]	-5076	353.50				
342	SEG[199]	-5117	353.50				
343	SEG[198]	-5158	353.50				
344	SEG[197]	-5199	353.50				
345	SEG[196]	-5240	353.50				
346	SEG[195]	-5281	353.50				
347	SEG[194]	-5322	353.50				
348	SEG[193]	-5363	353.50				
349	SEG[192]	-5404	353.50				
350	SEG[191]	-5527	353.50				
351	SEG[190]	-5568	353.50				
352	SEG[189]	-5609	353.50				
353	SEG[188]	-5650	353.50				
354	SEG[187]	-5691	353.50				
355	SEG[186]	-5732	353.50				
356	SEG[185]	-5773	353.50				
357	SEG[184]	-5814	353.50				
358	SEG[183]	-5855	353.50				
359	SEG[182]	-5896	353.50				
360	SEG[181]	-5937	353.50				
361	SEG[180]	-5978	353.50				
362	SEG[179]	-6019	353.50				
363	SEG[178]	-6060	353.50				
364	SEG[177]	-6101	353.50				
365	SEG[176]	-6142	353.50				
366	SEG[175]	-6183	353.50				
367	SEG[174]	-6224	353.50				
368	SEG[173]	-6265	353.50				
369	SEG[172]	-6306	353.50				
370	SEG[171]	-6347	353.50				
371	SEG[170]	-6388	353.50				
372	SEG[169]	-6429	353.50				
373	SEG[168]	-6470	353.50				
374	SEG[167]	-6511	353.50				
375	SEG[166]	-6552	353.50				
376	SEG[165]	-6593	353.50				
377	SEG[164]	-6634	353.50				
378	SEG[163]	-6675	353.50				
379	SEG[162]	-6716	353.50				
380	SEG[161]	-6757	353.50				
381	SEG[160]	-6798	353.50				
382	SEG[159]	-6839	353.50				
383	SEG[158]	-6880	353.50				
384	SEG[157]	-6921	353.50				
385	SEG[156]	-6962	353.50				
386	SEG[155]	-7003	353.50				
387	SEG[154]	-7044	353.50				
388	SEG[153]	-7085	353.50				
389	SEG[152]	-7126	353.50				
390	SEG[151]	-7167	353.50				
391	SEG[150]	-7208	353.50				
392	SEG[149]	-7249	353.50				
393	SEG[148]	-7290	353.50				
394	SEG[147]	-7331	353.50				
395	SEG[146]	-7372	353.50				
396	SEG[145]	-7413	353.50				
397	SEG[144]	-7454	353.50				
398	SEG[143]	-7495	353.50				
399	SEG[142]	-7536	353.50				
400	SEG[141]	-7577	353.50				
401	SEG[140]	-7618	353.50				
402	SEG[139]	-7659	353.50				
403	SEG[138]	-7700	353.50				
404	SEG[137]	-7741	353.50				
405	SEG[136]	-7782	353.50				

Functional Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface, Serial Interface (SPI) or I^2C Interface can be selected by different selections of IM0~2 as shown in Table 1.

Table. 1

Interface	Configure			Data signal								Control signal				
	IM0	IM1	IM2	D7	D6	D5	D4	D3	D2	D1	D0	E/$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
6800	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	E	R/$\overline{W}$	$\overline{CS}$	A0	$\overline{RES}$
8080	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
4-Wire SPI	0	0	0	Hz(Note1)						SI	SCL	Pull High or Low		$\overline{CS}$	A0	$\overline{RES}$
3-Wire SPI	1	0	0	Hz(Note1)						SI	SCL	Pull High or Low		$\overline{CS}$	Pull Low	$\overline{RES}$
I^2C	0	1	0	Hz(Note1)						SDA	SCL	Pull High or Low		Pull Low	SA0	$\overline{RES}$

Note1: When Serial Interface (SPI) or I2C Interface is selected, D7~D2 is Hz. D7~ D2 is recommended to connect the VDD1 or VSS. It is also allowed to leave D7~ D2 unconnected.

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. When $\overline{WR}$ (R/$\overline{W}$) = "H", read operation from the display RAM or the status register occurs. When $\overline{WR}$ (R/$\overline{W}$) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The $\overline{RD}$ (E) input serves as data latch signal (clock) when it is "H", provided that $\overline{CS}$ = "L" as shown in Table. 2.

Table. 2

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
0	0	1	6800 microprocessor bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D0 to D7

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. 2 below.

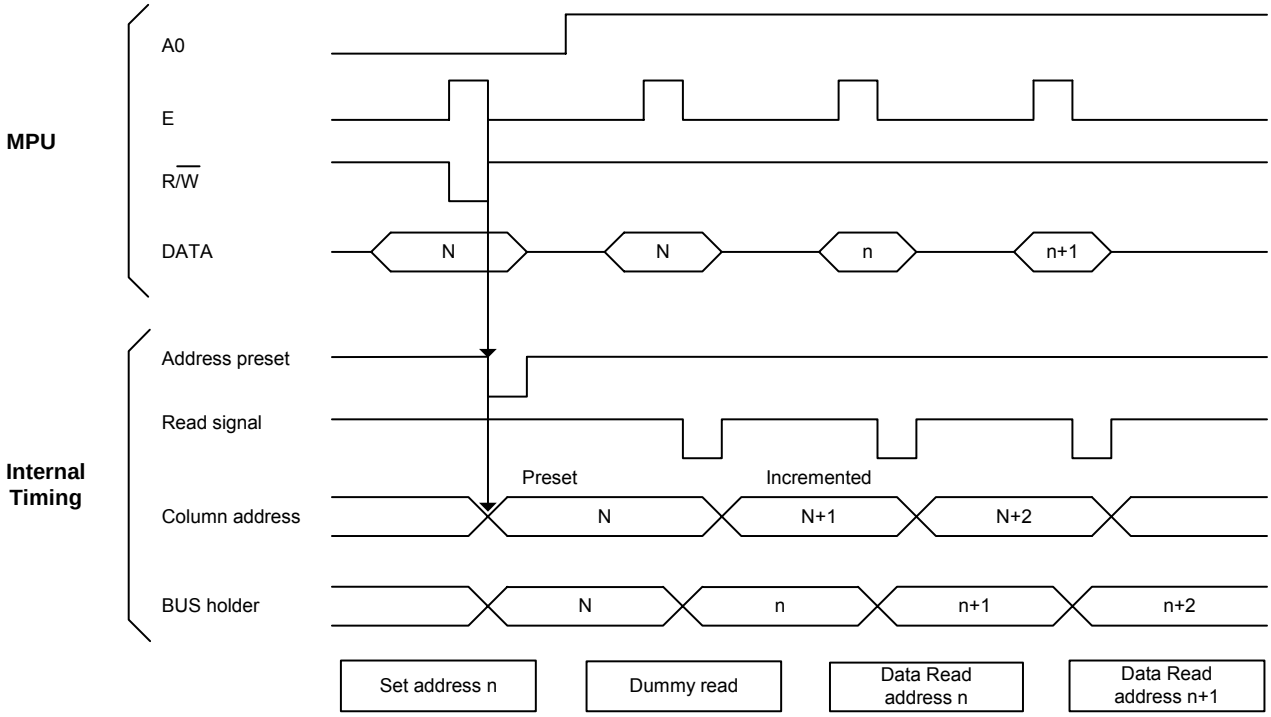


Figure. 2

8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. The $\overline{RD}$ (E) input serves as data read latch signal (clock) when it is "L" provided that $\overline{CS}$ = "L". Display data or status register read is controlled by A0 signal. The $\overline{WR}$ (R/$\overline{W}$) input serves as data write latch signal (clock) when it is "L" and provided that $\overline{CS}$ = "L". Display data or command register write is controlled by A0 as shown in Table. 3.

Table. 3

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
0	1	1	8080 microprocessor bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Data Bus Signals

The SH1122 identifies the data bus signal according to A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals.

Table. 4

Common	6800 processor	8080 processor		Function
A0	(R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and $\overline{CS}$. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM or command register in the same clock. See Figure. 3.

Table. 5

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	0	0	4-wire SPI	$\overline{CS}$	A0	-	-	SCL	SI	(HZ)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or V_{SS}. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

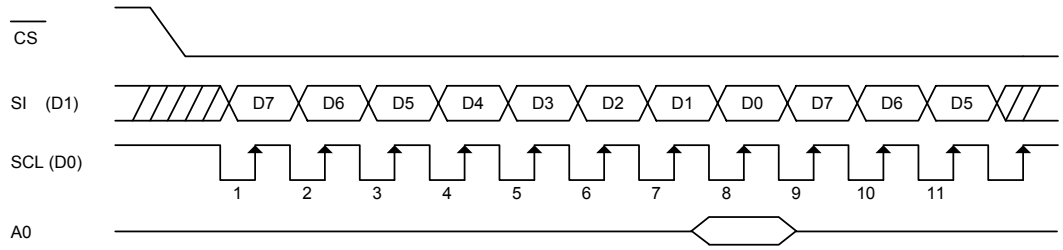


Figure. 3 4-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

3 Wire Serial Interface (3-wire SPI)

The 3 wire serial interface consists of serial clock SCL, serial data SI, and $\overline{CS}$. SI is shifted into an 9-bit shift register on every rising edge of SCL in the order of $D/\overline{C}$, D7, D6, … and D0. The $D/\overline{C}$ bit (first of the 9 bit) will determine the transferred data is written to the display data RAM ($D/\overline{C}$=1) or command register ($D/\overline{C}$=0). See Figure. **3** 4.

Table. 6

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
1	0	0	3-wire SPI	$\overline{CS}$	Pull Low	-	-	SCL	SI	(HZ)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or V_{SS}. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

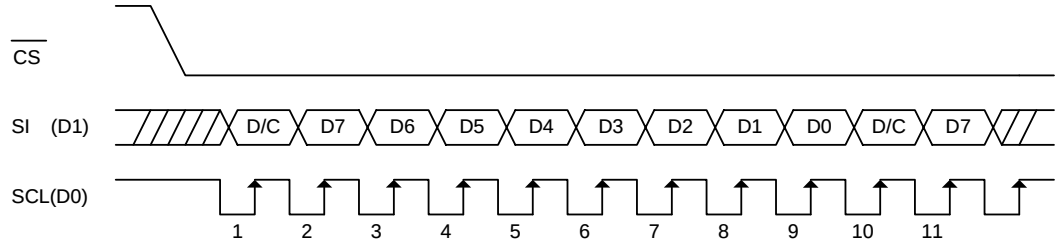


Figure. 4 3-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

I^2C-bus Interface

The SH1122 can transfer data via a standard I^2C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status and RAM data can be read out of the chip.

Table. 7

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	1	0	I^2C Interface	Pull Low	SA0	-	-	SCL	SDA	(HZ)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or V_{SS}. It is also allowed to leave D7~ D2 unconnected.

$\overline{CS}$ signal could always pull low in I^2C-bus application.

Characteristics of the I^2C-bus

The I^2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of V_{DD1}.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

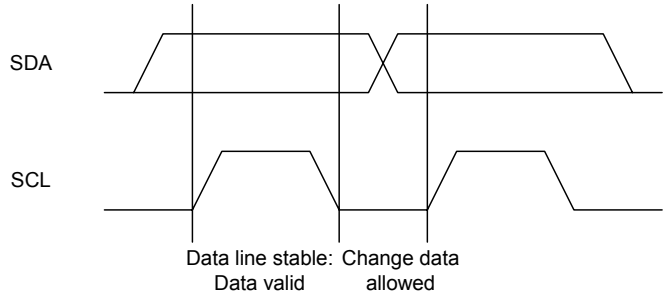


Figure. 5 Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

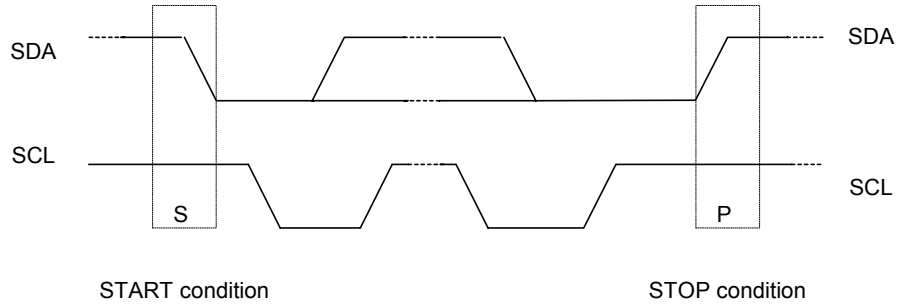


Figure. 6 Start and Stop conditions

System configuration

- Transmitter: The device that sends the data to the bus.
- Receiver: The device that receives the data from the bus.
- Master: The device that initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

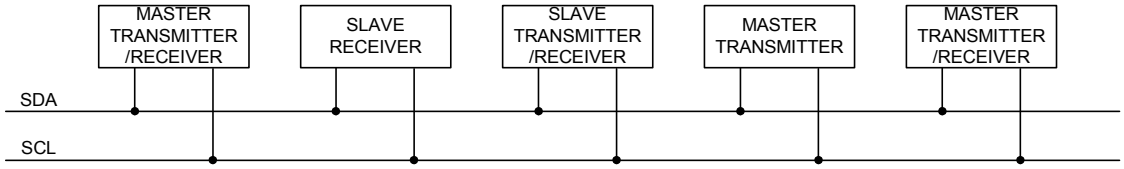


Figure. 7 System configuration

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

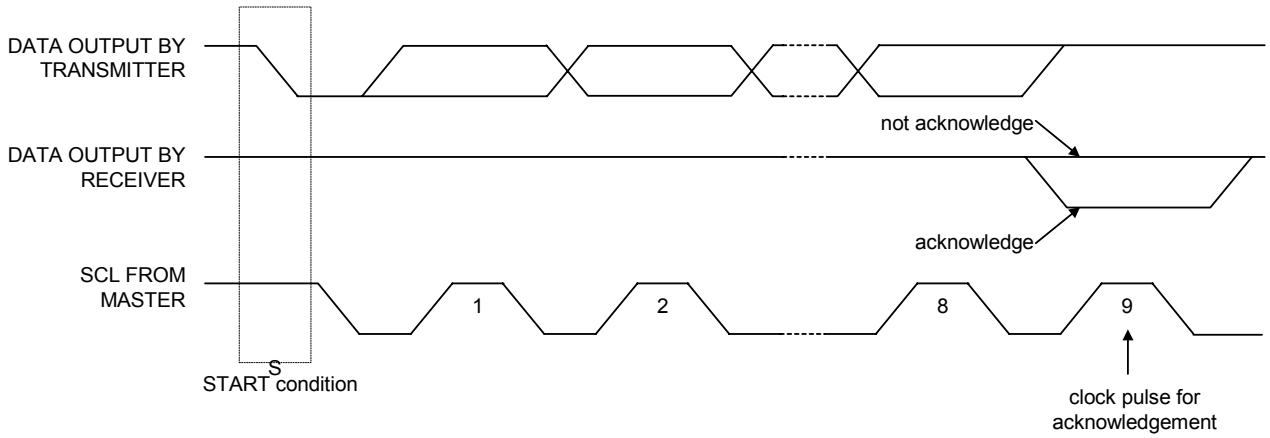


Figure 8 Acknowledge

Protocol

The SH1122 supports both read and write access. The $R/\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I^2C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the SH1122. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(Vss) or 1 (VDD1). The I^2C-bus protocol is illustrated in Fig.9. The sequence is initiated with a START condition (S) from the I^2C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and $D/\overline{C}$ (note1), plus a data byte (see Fig.7). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the $D/\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the $D/\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the $D/\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SH1122 device. If the $D/\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I^2C-bus master issues a stop condition (P). If the $R/\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the $D/\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

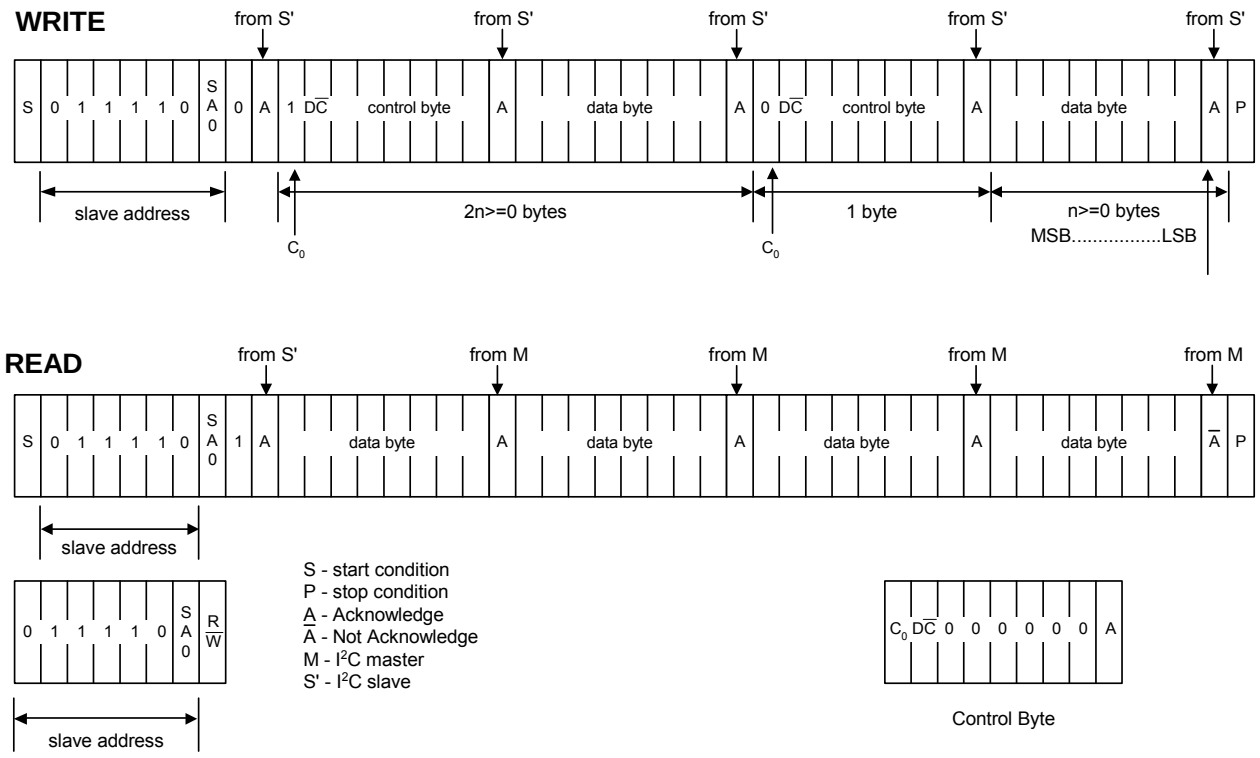


Figure 9 I²C Protocol

Note1:

1. Co＝“ 0 ”: The last control byte , only data bytes to follow,
   Co＝“ 1 ”: Next two bytes are a data byte and another control byte;
2. D/C̄ ＝“ 0 ”: The data byte is for command operation,
   D/C̄ ＝“ 1 ”: The data byte is for RAM operation.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = “H”, the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = “L”, the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 256 X 64 X 4 bits as shown in Figure. 10.

For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Row \ Column		COL0								---	COL127							
0		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
1		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
2		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
---		---								---								
62		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
63		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
ADC	= 0	SEG0				SEG1				---	SEG254				SEG255			
	= 1	SEG255				SEG254				---	SEG1				SEG0			

Figure. 10

The Column/Row Address

As shown in **Figure. 11**, the display data RAM column address is specified by the Column and Row Address Set command. The specified column address is incremented (+1) with each display data read/ write command. When the Column address reaches the edge, it will be cleared and the row address will be incremented 1.

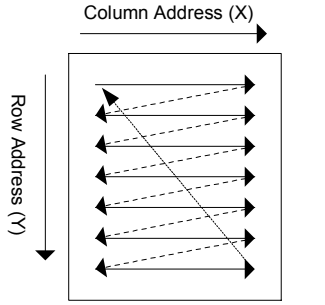


Figure. 11

Furthermore, as shown in Table 8, the Column re-mapping (ADC) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table. 8

Segment Output	SEG0		SEG255
ADC "0"	0 (H) →	Column Address	→ 7F (H)
ADC "1"	7F (H) ←	Column Address	← 0 (H)

The Row Address Circuit

The Row address circuit specifies the Row address of display RAM and the Row address relating to the common output using the display start line set command, what is normally the top line of the display can be specified.

The screen scrolling function is active by changing display start line dynamically using the display start line set command.

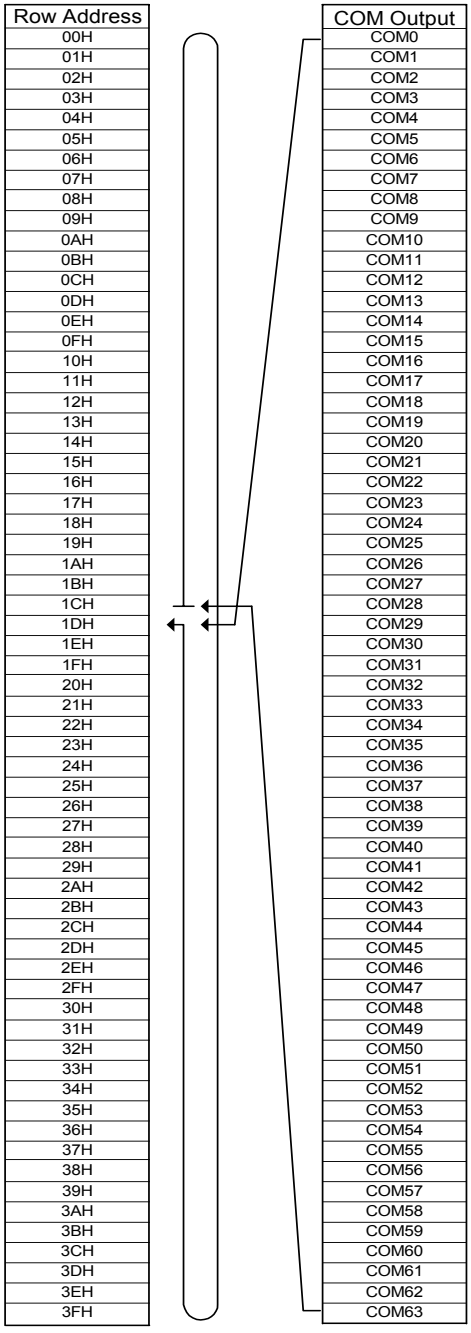


Figure. 12 Display Start Line Setting Function

The Oscillator Circuit

This is a RC type oscillator (Figure. 13) that produces the display clock. The oscillator circuit is only enabled when CLS = “H”. When CLS = “L”, the oscillation stops and the display clock is inputted through the CL terminal.

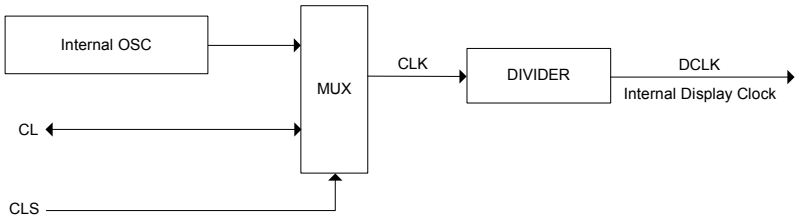


Figure. 13

DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for hand held applications. In SH1122, built-in DC-DC voltage converter accompanied with an external application circuit (shown in Figure.) can generate a high voltage supply V_{PP} from a low voltage supply input AV_{DD}. V_{PP} is the voltage supply to the OLED driver block.

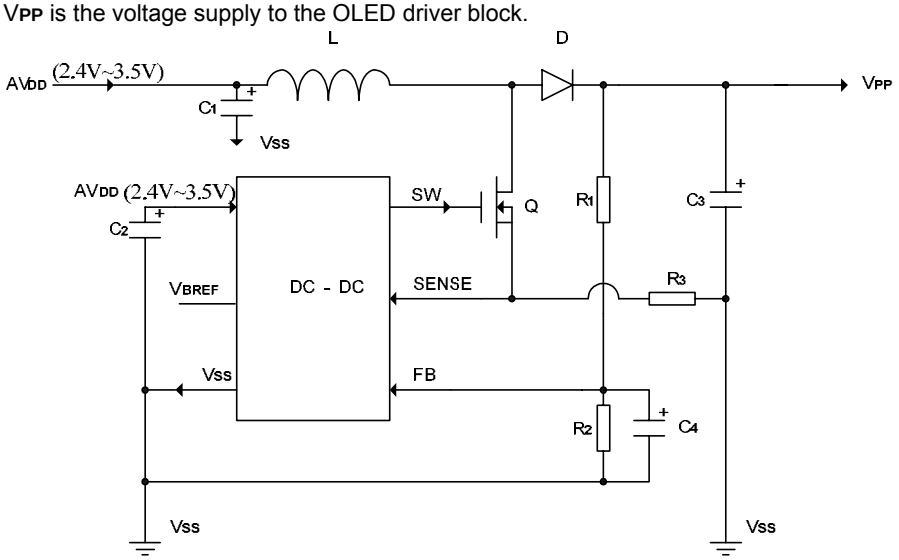


Figure. 14

$V_{PP}=(1+\frac{R1}{R2})$ X V_{BREF}, (R_2: 80 - 120kΩ)

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. V_{PP} and V_{DD2} are external power supplies. I_{REF} is a reference current source for segment current drivers.

Common Drivers/Segment Drivers

Segment drivers deliver 256 current sources to drive OLED panel. The driving current can be adjusted up to 500μA with 256 steps. Common drivers generate voltage scanning pulses.

16 Grayscale

There are 16 level grayscale for segment driver. The grayscale table is as following.

RAM Data	Pulse Duty	Pulse width
0000	0	0 (DCLK)
0001	1/15	4 (DCLK)
0010	2/15	8 (DCLK)
0011	3/15	12 (DCLK)
…	…	…
1110	14/15	56 (DCLK)
1111	15/15	60 (DCLK)

Reset Circuit

When the $\overline{RES}$ input falls to “L”, these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 256 X 64 Display mode.
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 mapped to row address 00H).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM Row address 00H.
6. Column address counter is set at 0.
7. Normal scanning direction of the common outputs.
8. Contrast control register is set at 80H.
9. Internal DC-DC is selected.

Commands

The SH1122 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/$\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1 (HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Set Lower Column Address of display RAM: (00H - 0FH)

2. Set Higher Column Address of display RAM: (10H - 17H)

Specify column address of display RAM. Divide the column address into 3 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 127 is accessed. The row address is not changed during this time.

	A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	0	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	1	1	1	1	1	1	127

Note: Don't use any commands not mentioned above.

3. - 5. Blank

6. Set Display Start Line: (40H - 7FH)

Specify Row address to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the Row address, the smooth scrolling or page change takes place.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3A	A2	A1	A0	Row address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

7. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: I_{SEG} = α/256 X I_{REF} X scale factor

Where: α is contrast step; I_{REF} is reference current equals to 15.625μA; Scale factor = 32.

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register，the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	I_{SEG}
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	0	1	0	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	POR
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

8. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the column address section of ADC. When display data is written or read, the column address is incremented by 1 as shown in Figure. 2.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

When ADC = “L”, the right rotates (normal direction). (POR)

When ADC = “H”, the left rotates (reverse direction).

Note:

The Set Segment Re-map command will change the address counter value, so it is recommended to set segment re-map in the initial program.

9. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turn the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = “L”, the normal display status is provided. (POR)

When D = “H”, the entire display ON status is provided.

10. Set Normal/Reverse Display: (A6H - A7H)

Reverse the display ON/OFF status without rewriting the contents of the display data RAM.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = “L”, the RAM data is high, being OLED ON potential (normal display). (POR)

When D = “H”, the RAM data is low, being OLED ON potential (reverse display)

11. Set Multiplex Ration: (Double Bytes Command)

This command switches default 64 multiplex modes to any multiplex ratio from 1 to 64. The output pads COM0-COM63 will be switched to corresponding common signal.

■ Multiplex Ration Mode Set: (A8H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

■ Multiplex Ration Data Set: (00H - 3FH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio
0	1	0	*	*	0	0	0	0	0	0	1
0	1	0	*	*	0	0	0	0	0	1	2
0	1	0	*	*	0	0	0	0	1	0	3
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	63
0	1	0	*	*	1	1	1	1	1	1	64 (POR)

12. DC-DC Setting: (Double Bytes Command)

This command is to control the DC-DC voltage converter status and the switch frequency. Issuing this command then display ON command will turn on the converter. The panel display must be off while issuing this command.

■ DC-DC Control Mode Set: (ADH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1

■ DC-DC ON/OFF Mode Set:

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	F2	F1	F0	D

When D = “L”, DC-DC is disable.
When D = “H”, DC-DC will be turned on when display on. (POR)

DC-DC STATUS	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External V_{PP} must be used
1	0	Sleep mode
1	1	Built-in DC-DC is used, Normal Display

F2	F1	F0	Switch Frequency
0	0	0	0.6SF (POR)
0	0	1	0.7SF
0	1	0	0.8SF
0	1	1	0.9SF
1	0	0	SF
1	0	1	1.1SF
1	1	0	1.2SF
1	1	1	1.3SF

SF =500kHZ ± 25%

13. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = “L”, Display OFF OLED. (POR)
When D = “H”, Display ON OLED.
When the display OFF command is executed, power saver mode will be entered.

Sleep Mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and DC-DC circuit.
(2) Stops the OLED drive and outputs HZ as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

14. Set Row Address of Display RAM: (Double Bytes Command)

Specify Row address to load display RAM data to Row address register. Any RAM data bit can be accessed when its Row address and column address are specified. The display remains unchanged even when the Row address is changed.

■ Row address Mode Setting: (B0H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	0	0	0

■ Row address setting:

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	*	*	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Row address
0	0	0	0	0	0	0 (POR)
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
…	…	…	…	…	…	…
1	1	1	1	0	1	3DH
1	1	1	1	1	0	3EH
1	1	1	1	1	1	3FH

15. Set Common Output Scan Direction: (C0H - C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

When D = “L”, Scan from COM0 to COM [N-1]. (POR)
When D = “H”, Scan from COM [N-1] to COM0.

16. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-63 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (64-16), so the second byte should be 100000.

■ Display Offset Mode Set: (D3H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

■ Display Offset Data Set: (00H - 3FH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	*	*	0	0	0	0	0	0	0 (POR)
0	1	0	*	*	0	0	0	0	0	1	1
0	1	0	*	*	0	0	0	0	1	0	2
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	62
0	1	0	*	*	1	1	1	1	1	1	63

Note: “*” stands for “Don’t care”

17. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

■ Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

■ Divide Ratio/Oscillator Frequency Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A_3 - A_0 defines the divide ration of the display clocks (DCLK). Divide Ration = A[3:0]+1.

A_3	A_2	A_1	A_0	Divide Ration
0	0	0	0	1 (POR)
		:		:
1	1	1	1	16

A_7 - A_4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A_7	A_6	A_5	A_4	Oscillator Frequency of fosc
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	fosc (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%
1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%

18. Set Discharge/Precharge Period: (Double Bytes Command)

This command is used to set the duration of the Precharge/Discharge period. The interval is counted in number of DCLK. POR is 2 DCLKs.

■ Precharge/Discharge Period Mode Set: (D9H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1

■ Precharge/Discharge Period Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Precharge Period Adjust: (A3 - A0)

A_3	A_2	A_1	A_0	Pre-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Discharge Period Adjust: (A_7 - A_4)

A_7	A_6	A_5	A_4	Dis-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

19. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (DBH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

■ VCOM Deselect Level Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$V_{COMH} = \beta_1 \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β_1	A[7:0]	β_1
00H	0.430	20H	
01H		21H	
02H		22H	
03H		23H	
04H		24H	
05H		25H	
06H		26H	
07H		27H	
08H		28H	
09H		29H	
0AH		2AH	
0BH		2BH	
0CH		2CH	
0DH		2DH	
0EH		2EH	
0FH		2FH	
10H		30H	
11H		31H	
12H		32H	
13H		33H	
14H		34H	
15H		35H	0.770 (POR)
16H		36H	
17H		37H	
18H		38H	
19H		39H	
1AH		3AH	
1BH		3BH	
1CH		3CH	
1DH		3DH	
1EH		3EH	
1FH		3FH	
40H - FFH	1		

20. Set VSEGM Level: (Double Bytes Command)

This command is to set the segment pad output voltage level at pre-charge stage.

■ V_{SEGM} Level Mode Set: (DCH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1	0	0

■ V_{SEGM} Level Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$V_{SEGM} = \beta_2 \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β_2	A[7:0]	β_2
00H	0.430	20H	
01H		21H	
02H		22H	
03H		23H	
04H		24H	
05H		25H	
06H		26H	
07H		27H	
08H		28H	
09H		29H	
0AH		2AH	
0BH		2BH	
0CH		2CH	
0DH		2DH	
0EH		2EH	
0FH		2FH	
10H		30H	
11H		31H	
12H		32H	
13H		33H	
14H		34H	
15H		35H	0.770 (POR)
16H		36H	
17H		37H	
18H		38H	
19H		39H	
1AH		3AH	
1BH		3BH	
1CH		3CH	
1DH		3DH	
1EH		3EH	
1FH		3FH	
40H - FFH	1		

21. Set Discharge VSL Level (30H - 3FH)

This command is to set the Segment output discharge voltage level.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	D_3	D_2	D_1	D_0

This command is to set the segment discharge voltage level

D[3:0]	VSL
00H	0V (Default)
01H	0.1 VREF
02H	0.125 VREF
03H	0.150 VREF
04H	0.175 VREF
05H	0.2 VREF
06H	0.225 VREF
07H	0.250 VREF
08H	0.275 VREF
09H	0.3 VREF
0AH	0.325 VREF
0BH	0.350 VREF
0CH	0.375 VREF
0DH	0.4 VREF
0EH	0.425 VREF
0FH	0.450 VREF

22. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. Once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

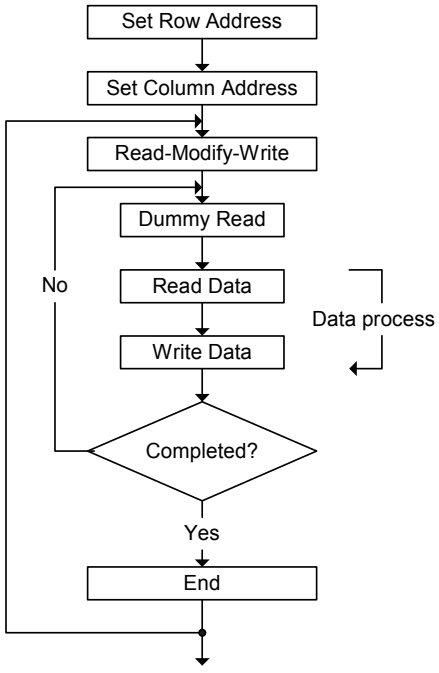


Figure. 15

23. End: (EEH)

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued.)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

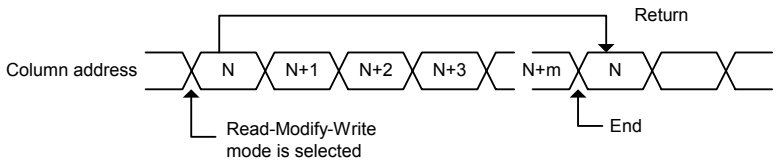


Figure. 16

24. NOP: (E3H)

Non-Operation Command.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

25. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

26. Read Status

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ON/OFF	*	*	*	0	0	0

BUSY: When high, the SH1122 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF: Indicates whether the display is on or off. When it goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

27. Read Display Data

Reads 8-bit data from display RAM area specified by column address and Row address. As the column address is increment by 1 automatically after each writing, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							

Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 3 higher bits	0	1	0	0	0	0	1	0	Higher column address			Sets 3 higher bits of column address of display RAM in register. (POR = 10H)
3. Reserved Command	0	1	0	0	0	1	0	0	1	0	0	Reserved
4. Reserved Command	0	1	0	0	0	1	0	0	1	1	0	Reserved
5. Reserved Command	0	1	0	0	0	1	0	1	1	1	D	Reserved
6. Set Display Start Line	0	1	0	0	1	Start Line address						Specifies RAM display line for COM0. (POR = 40H)
7. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								
8. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
9. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
10. Set Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
11. Multiplex Ration Mode Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH)
Multiplex Ration Data Set	0	1	0	*	*	Multiplex Ratio						
12. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage and the switch frequency. (POR = 81H)
DC-DC ON/OFF Mode Set	0	1	0	1	0	0	0	F2	F1	F0	D	
13. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
14. Row Address Set	0	1	0	1	0	1	1	0	0	0	0	Specifies Row address to load display RAM data to Row address register. (POR = 00H)
Row Address	0	1	0	*	*	Row Address						
15. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
16. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command that specifies the mapping of display start line to one of COM0-63. (POR = 00H)
Display Offset Data Set	0	1	0	*	*	COMx						
17. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				

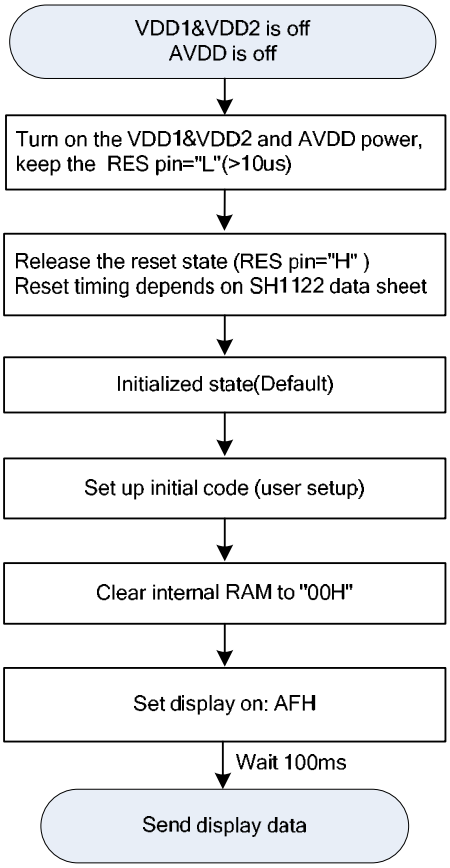
Command Table (Continued)

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
18. Dis-charge/Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge/Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
19. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOMH= (β_1 X V_{REF})								
20. VSEGM Level Mode Set	0	1	0	1	1	0	1	1	1	0	0	This command is to set the segment pad output voltage level at pre-charge stage. (POR = 35H)
VSEGM Level Data Set	0	1	0	VSEGM= (β_2 X V_{REF})								
21. Discharge voltage VSL level setting	0	1	0	0	0	1	1	D3	D2	D1	D0	Set the discharge voltage level.
22. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
23. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
24. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
25. Write Display Data	1	1	0	Write RAM data								
26. Read Status	0	0	1	BUSY	ON/OFF			*	*	*	0	0	0	
27. Read Display Data	1	0	1	Read RAM data								

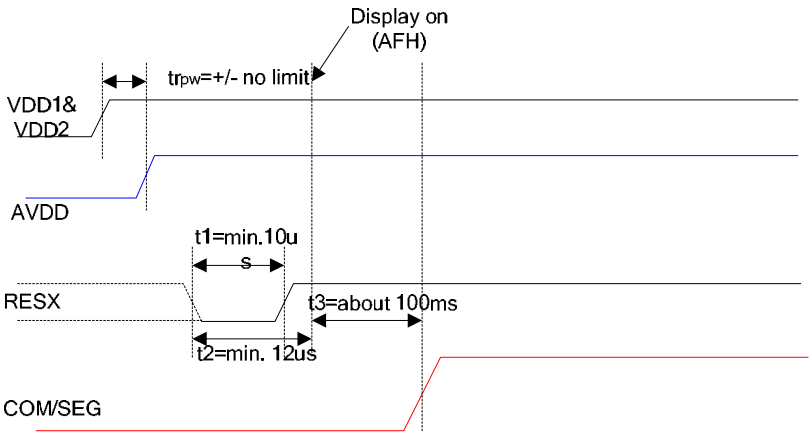
Note: Do not use any others command, otherwise it will cause system malfunction.

1. Power On and Off sequence

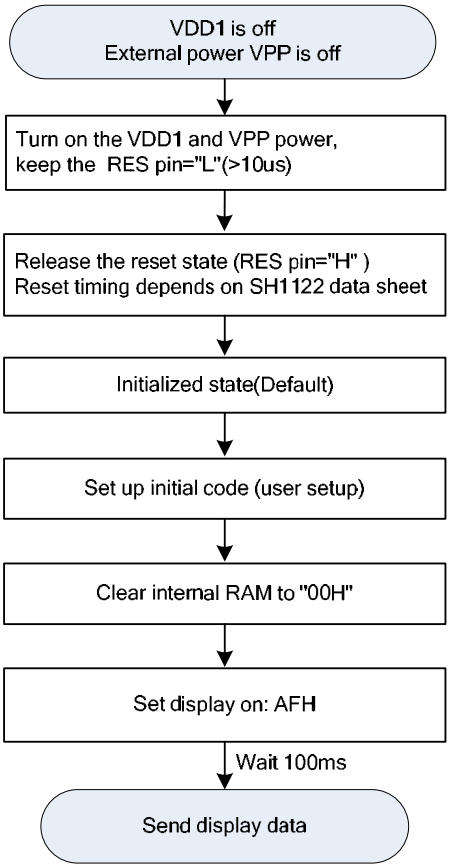
1.1. Built-in DC-DC pump power is being used immediately after turning on the power:



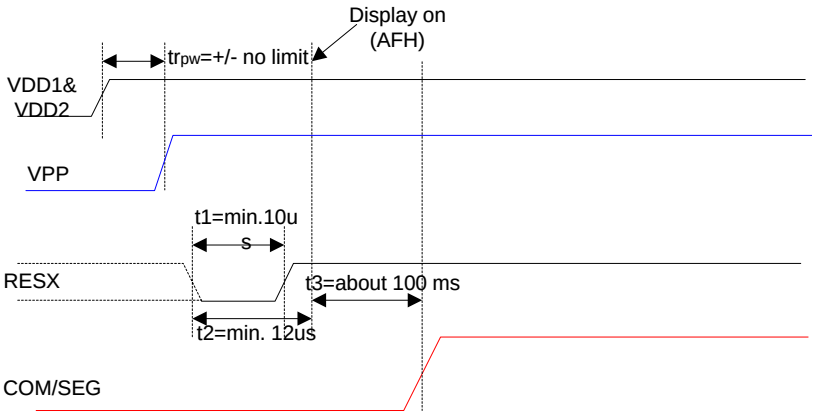
Power on sequence:



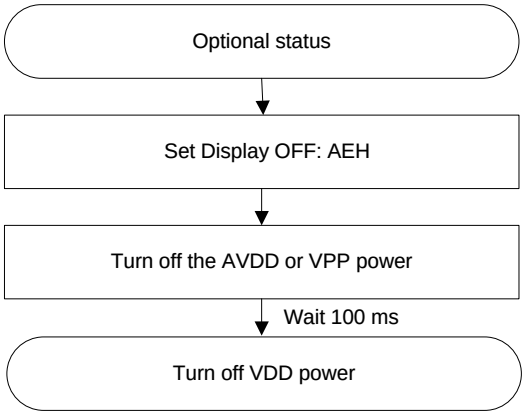
1.2. External DC-DC pump power is being used immediately after turning on the power:



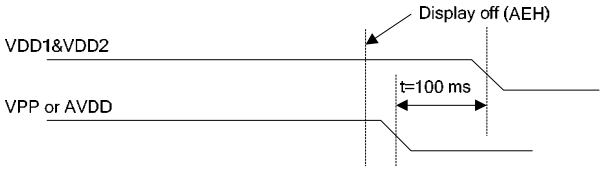
Power on sequence:



3. Power Off



Power off sequence:



Note：There will be no damages to the display module if the power on/off sequences are not met.

Absolute Maximum Rating*

DC Supply Voltage (VDD1)…….-0.3V to +3.6V

DC Supply Voltage (VDD2)…… -0.3V to +3.6V

DC Supply Voltage (V_{PP})…….. -0.3V to +14.5V

Input Voltage…….. -0.3V to V_{DD1} + 0.3V

Operating Ambient Temperature …… -40°C to +85°C

Storage Temperature …… -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (V_{SS} = 0V, V_{DD1} = 1.65 – 3.5V, V_{DD2} = 1.65 – 3.5V, AV_{DD} =2.4-3.5V, T_A = +25°C, unless otherwise specified)

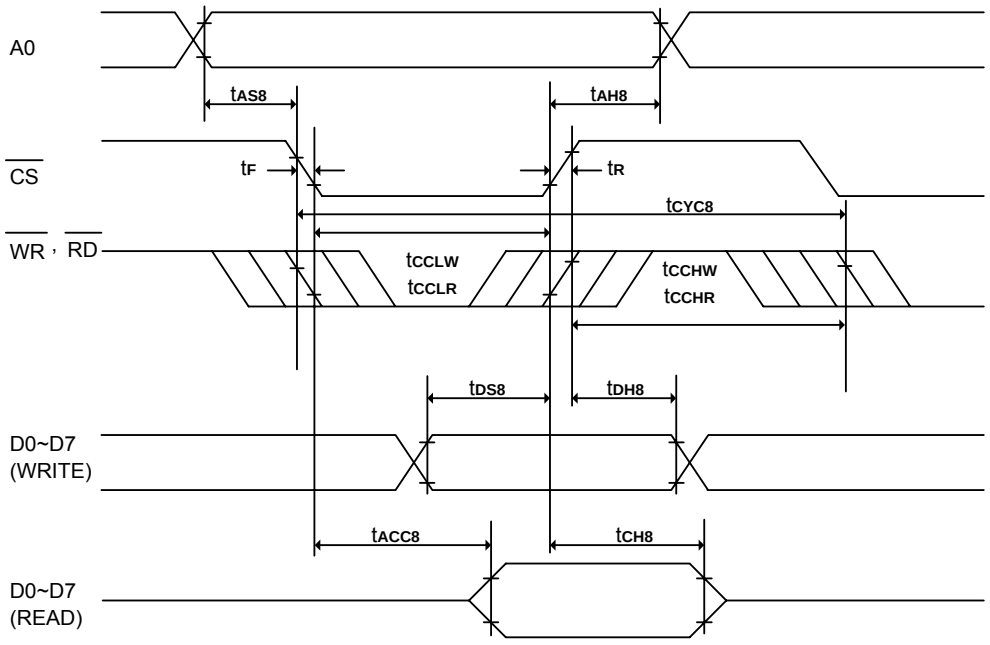
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD1}	Power supply of I/O	1.65	-	3.5	V	
V_{DD2}	Power supply of logic device	1.65	-	3.5	V	
AV_{DD}	DC-DC voltage supply	2.4		3.5		
V_{PP}	OLED Operating voltage	7.0	-	14.0	V	
V_{BREF}	Internal voltage reference	1.20	1.26	1.32	V	
I_{DD1}	Dynamic current Consumption 1(in V_{DD1}& V_{DD2})	-	110	160	μA	V_{DD1} = 3V, V_{DD2} = 3V, AV_{DD} =3V ,I_{REF} = -15.625μA, Contrast α = 256, Bulid-in DC-DC OFF, Display ON, display data = All ON, No panel attached
I_{DD2}	Dynamic current Consumption 2 (in AV_{DD})	-	190	285	μA	V_{DD1} = 3V, V_{DD2} = 3V, AV_{DD} =3V ,V_{PP} = 12V, I_{REF} =-15.625μA, Contrast α = 256, Bulid-in DC-DC ON, Display ON, Display data = All ON, No panel attached
I_{PP}	OLED dynamic current consumption	-	1	1.27	mA	V_{DD1} = 3V, V_{DD2} = 3V, AV_{DD} =3V ,V_{PP} = 12V, I_{REF} =-15.625μA, Contrast α = 256, Display ON, Display data = All ON, No panel attached
I_{SP}	Sleep mode current Consumption in V_{DD1} & V_{DD2}& AV_{DD}	-	0.01	5	μA	During sleep, T_A = +25°C, V_{DD1} = 3V, V_{DD2} = 3V, AV_{DD} =3V
	Sleep mode current Consumption in V_{PP}	-	0.01	5	μA	During sleep, T_A = +25°C, V_{PP} = 12V
I_{SEG}	Segment output current		-500		μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} =-15.625μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 256
		-	-343.75	-	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} = -15.625μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 176
		-	-187.5	-	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} =-15.625μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 96
		-	-31.25	-	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} = -15.625μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 16
ΔI_{SEG1}	Segment output current uniformity	-	-	±3	%	ΔI_{SEG1} = (I_{SEG} – I_{MID})/I_{MID} X 100% I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} [0:255] at contrast α = 256
ΔI_{SEG2}	Adjacent segment output Current uniformity	-	-	±2	%	ΔI_{SEG2} = (I_{SEG} [N] – I_{SEG} [N+1])/(I_{SEG} [N] + I_{SEG} [N+1]) X 100% I_{SEG} [0:255] at contrast α = 256

DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHC}	High-level input voltage	0.8 X V_{DD1}	-	V_{DD1}	V	A0, D0 – D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, CL, IM0, IM1, IM2 and $\overline{RES}$
V_{ILC}	Low-level input voltage	V_{SS}	-	0.2 X V_{DD1}	V	
V_{OHC}	High-level output voltage	0.8 X V_{DD1}	-	V_{DD1}	V	I_{OH} = -0.5mA (D0 – D7, and CL)
V_{OLC}	Low –level output voltage	V_{SS}	-	0.2 X V_{DD1}	V	I_{OL} = 0.5mA (D0 – D7, and CL)
V_{OLCS}	SDA low –level output voltage	V_{SS}	-	0.2 X V_{DD1}	V	VDD1<2V; I_{OL}=2mA (SDA)
				0.4		VDD1 ≥ 2V; I_{OL}=3mA (SDA)
I_{LI}	Input leakage current	-1.0	-	1.0	μA	V_{IN} = V_{DD1} or V_{SS} (A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, IM0, IM1, IM2 and $\overline{RES}$)
I_{HZ}	HZ leakage current	-1.0	-	1.0	μA	When the D0 – D7, and CL are in high impedance
f_{OSC}	Oscillation frequency	-	512	-	KHz	T_A = +25°C
f_{FRM}	Frame frequency for 64 Commons	-	125	-	Hz	When f_{OSC} = 512kHz, Divide ratio = 1, common width = 64 DCLKs
R_{ON1}	Common switch resistance	-	10	12	Ω	V_{PP} = 12V, V_{COM} = V_{SS} + 0.4V
R_{ON2}	Common switch resistance	-	350	-	Ω	V_{PP} = 12V, V_{COM} = 0.770 X V_{PP} – 0.4V

AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



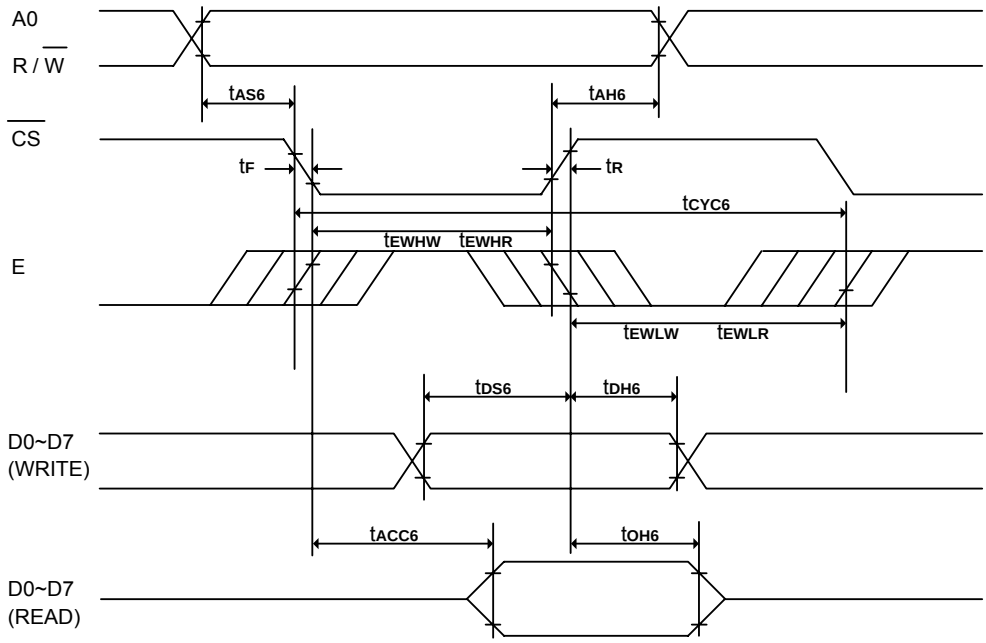
(V_{DD1} = V_{DD2} = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	600	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	80	-	-	ns	
t_{DH8}	Data hold time	30	-	-	ns	
t_{CH8}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	280	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	200	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	240	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	200	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = V_{DD2} = 2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DH8}	Data hold time	15	-	-	ns	
t_{CH8}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	100	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	120	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	100	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

2. **System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)**



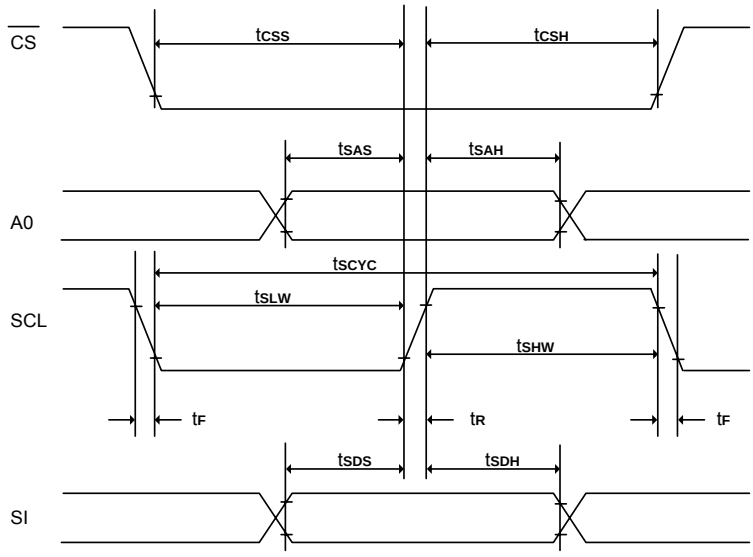
(V_{DD1} = V_{DD2} = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	600	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	80	-	-	ns	
t_{DH6}	Data hold time	30	-	-	ns	
t_{OH6}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	200	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	240	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	200	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = V_{DD2} = 2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	15	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

2. **System buses Write characteristics 3 (For 4 wire SPI)**



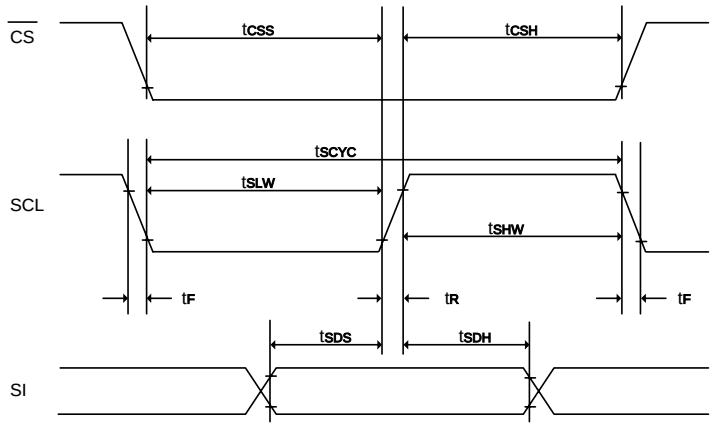
(V_{DD1} = V_{DD2} =1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SAS}	Address setup time	300	-	-	ns	
t_{SAH}	Address hold time	300	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = V_{DD2} = 2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SAS}	Address setup time	150	-	-	ns	
t_{SAH}	Address hold time	150	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

2. **System buses Write characteristics 4(For 3 wire SPI)**



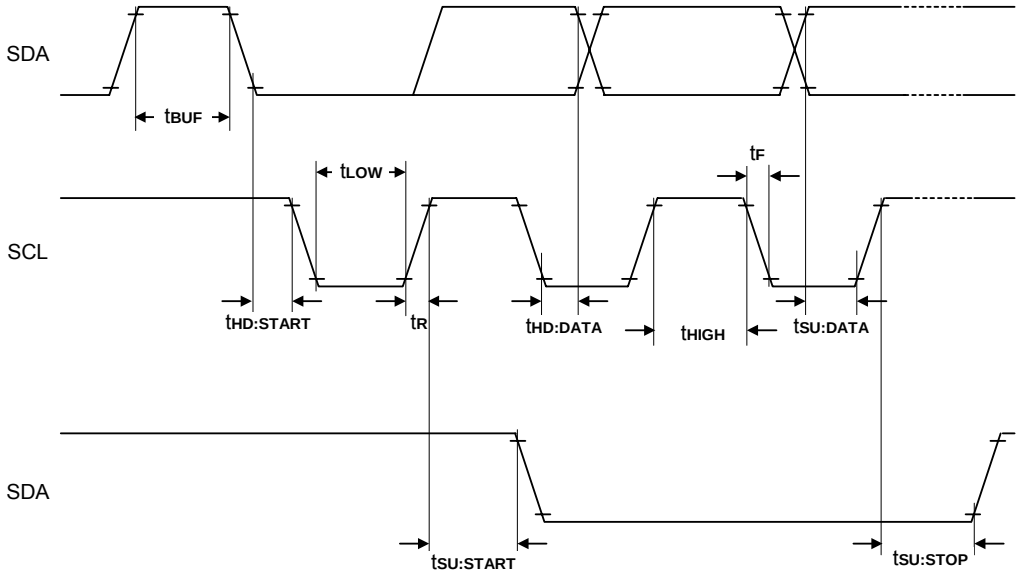
(V_{DD1} = V_{DD2} = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = V_{DD2} =2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

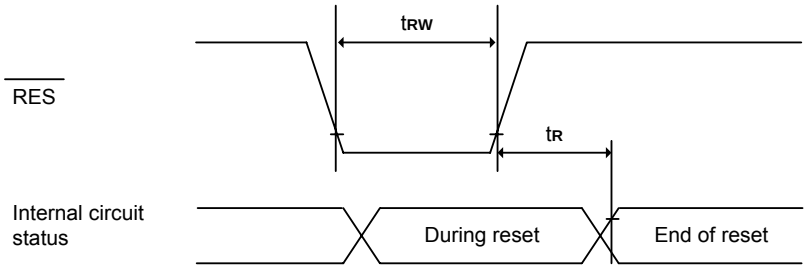
2. **I²C interface characteristics**



(V_{DD1} = V_{DD2} =1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{SCL}	SCL clock frequency	DC	-	400	kHz	
T_{LOW}	SCL clock Low pulse width	1.3	-	-	uS	
T_{HIGH}	SCL clock H pulse width	0.6	-	-	uS	
$T_{SU:DATA}$	data setup time	100	-	-	nS	
$T_{HD:DATA}$	data hold time	0	-	0.9	uS	
T_R	SCL, SDA rise time	20+0.1Cb	-	300	nS	
T_F	SCL, SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
$T_{SU:START}$	Setup timefor re-START	0.6	-	-	uS	
$T_{HD:START}$	START Hold time	0.6	-	-	uS	
$T_{SU:STOP}$	Setup time for STOP	0.6	-	-	uS	
T_{BUF}	Bus free times between STOP and START condition	1.3	-	-	uS	

2. **Reset Timing**



(V_{DD1} = V_{DD2} =1.65 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	μs	
t_{RW}	Reset low pulse width	10.0	-	-	μs	

(V_{DD1} = V_{DD2} =2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	1.0	μs	
t_{RW}	Reset low pulse width	5.0	-	-	μs	

Application Circuit (for reference only)

Reference Connection to MPU:

2. **8080 Series Interface: (Internal Oscillator, External V_{PP})**

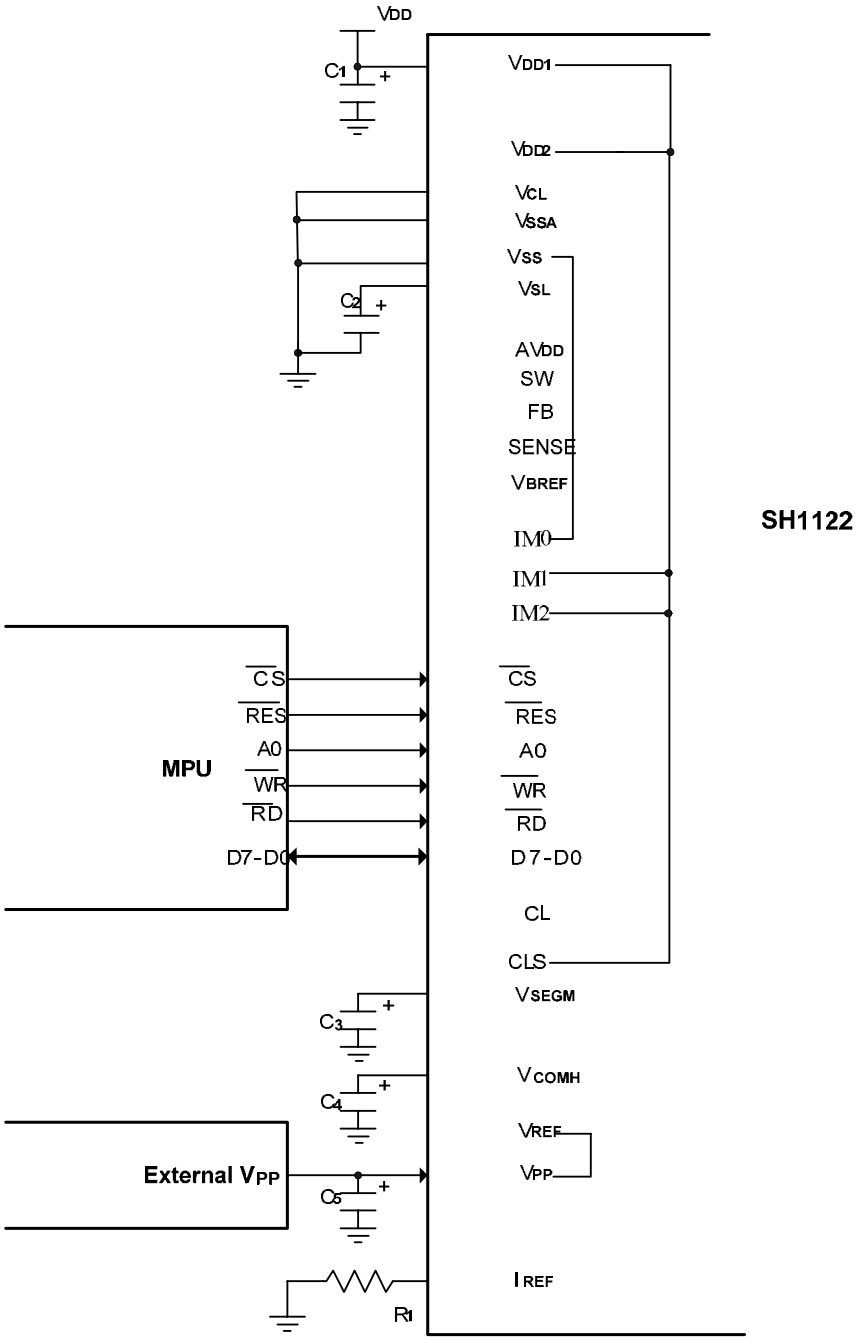


Figure. 17

Note:

C_1 – C_5: 4.7μF

R_1: about 620kΩ, R_1 = (Voltage at I_{REF} – V_{SS})/I_{REF}

2. 6800 Series Interface: (Internal Oscillator, Built-in DC-DC)

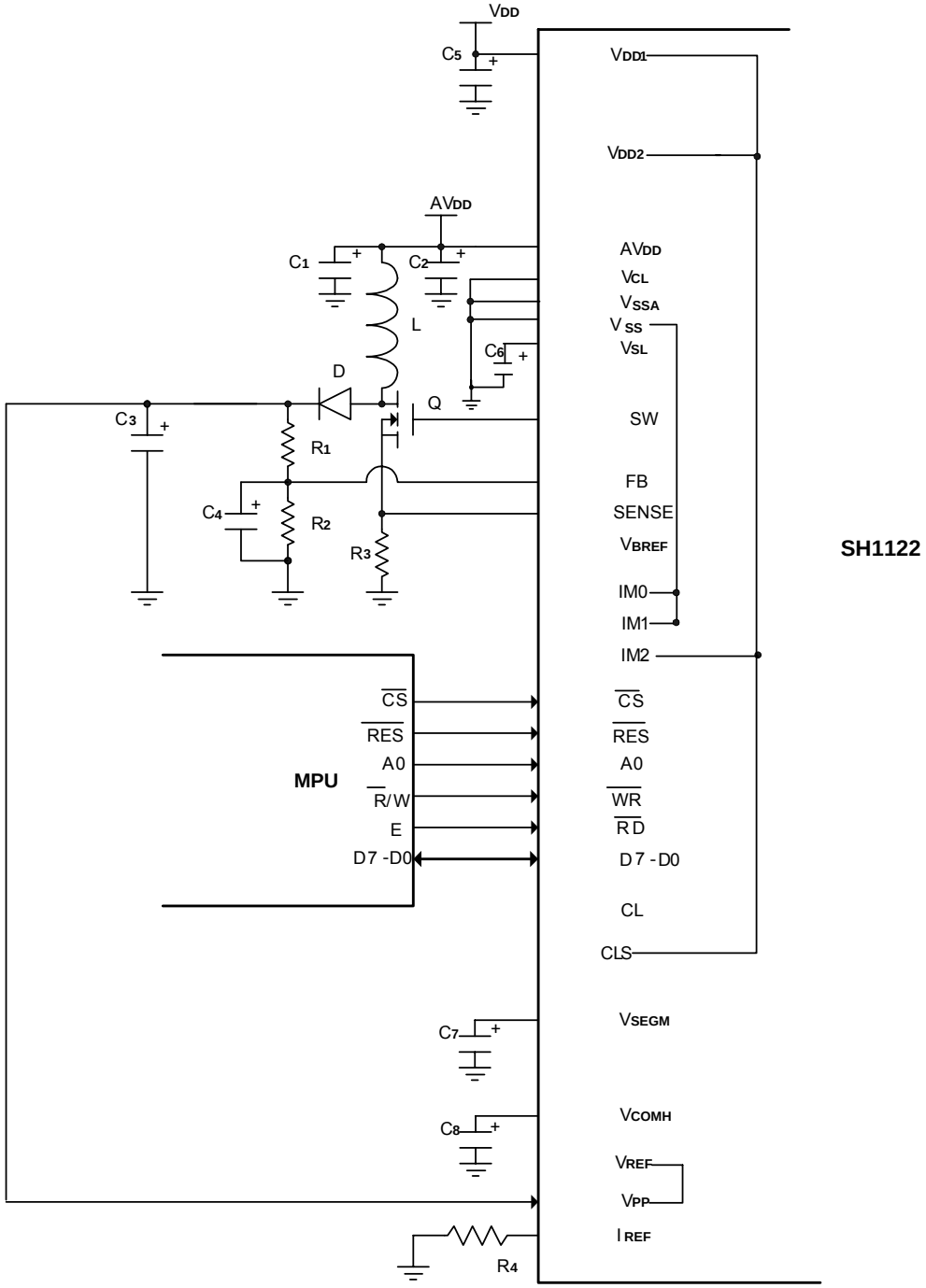


Figure. 18

Note:

L, D, Q, R_1, R_2, R_3, C_1 – C_4: Please refer to following description of DC-DC module.
C_5, C_6, C_7, C_8: 4.7μF
R_4: about 620kΩ, R_4 = (Voltage at I_{REF} – V_{SS})/I_{REF}

2. **Serial Interface (3-wire or 4-wire SPI): (External Oscillator, External V_{PP})**

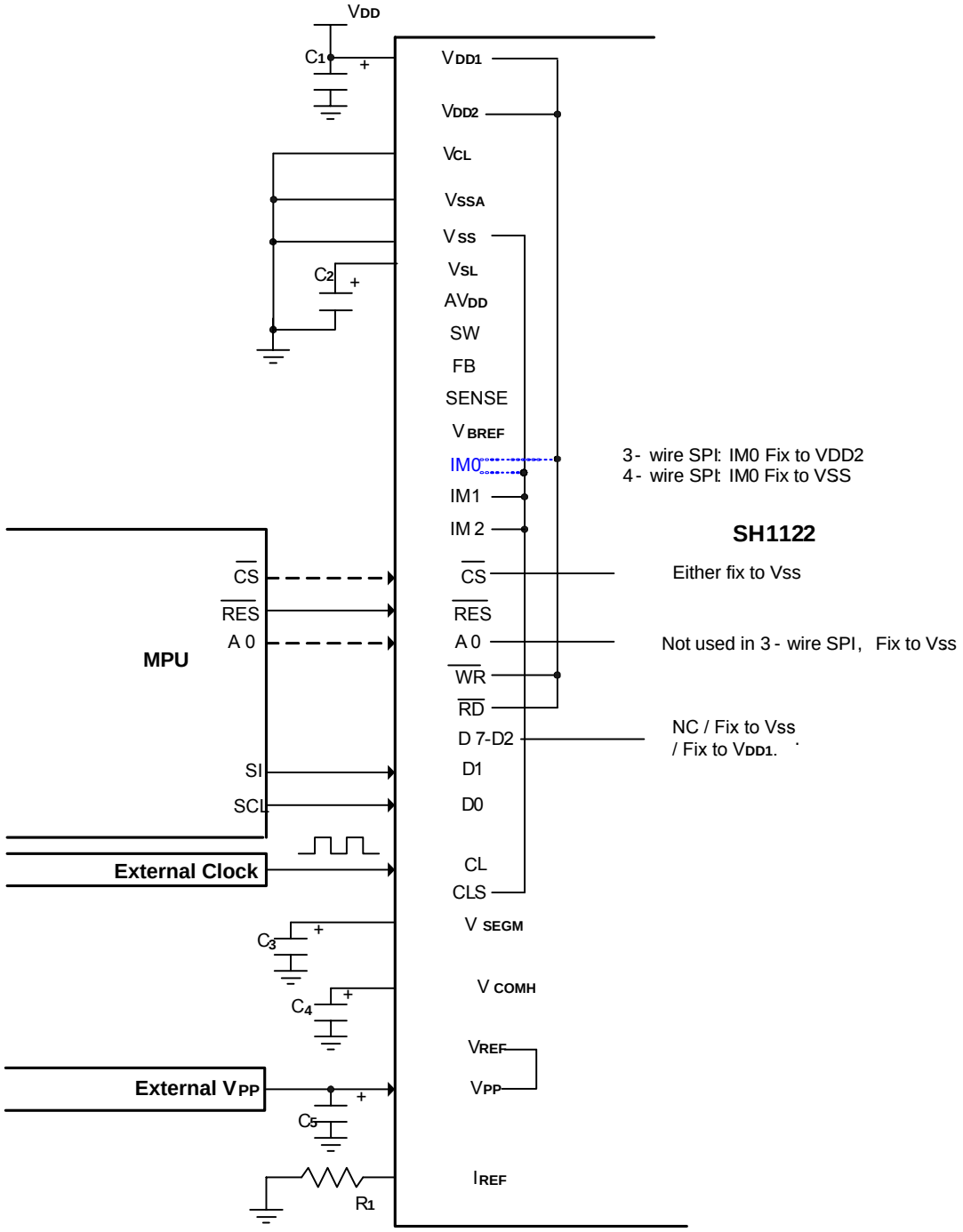


Figure. 19

Note:

C_1 – C_5: 4.7μF

R_1: about 620kΩ, R_1 = (Voltage at I_{REF} – V_{SS})/I_{REF}

2. **I²C Interface: (Internal oscillator, External VPP)**

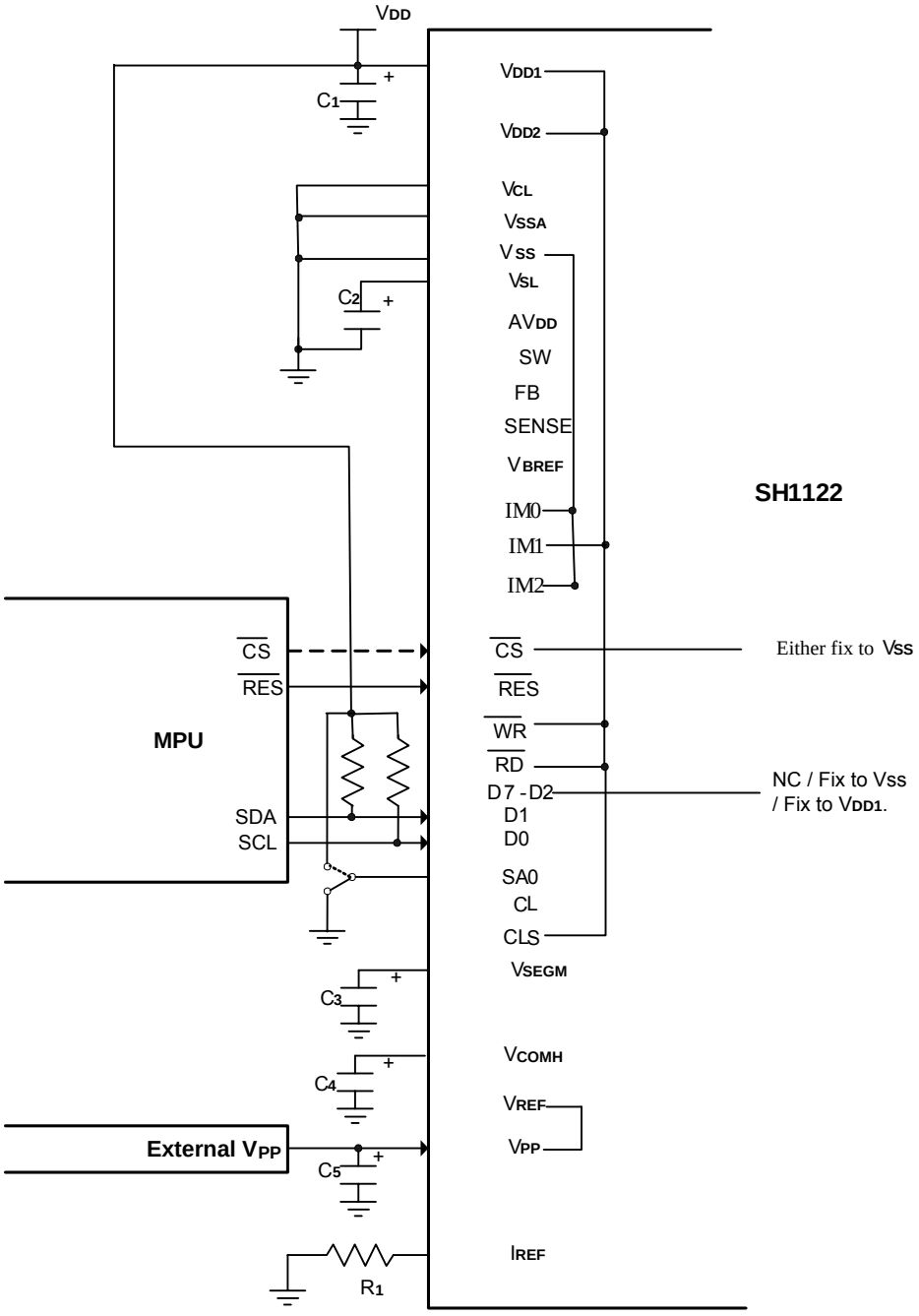


Figure. 20

Note:

C1 – C5: 4.7μF

R1: about 620kΩ, R1 = (Voltage at IREF – VSS)/IREF

The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(Vss) or 1 (VDD1).

WR and RD are not used in I²C mode, should fix to Vss or VDD1.

CS can fix to Vss in I²C mode.

The positive supply of pull-up resistor must equal to the value of VDD1.

DC-DC:

Below application circuit is an example for the input voltage of 3V AV_{DD} to generate V_{PP} of about 12V@10mA-25mA application.

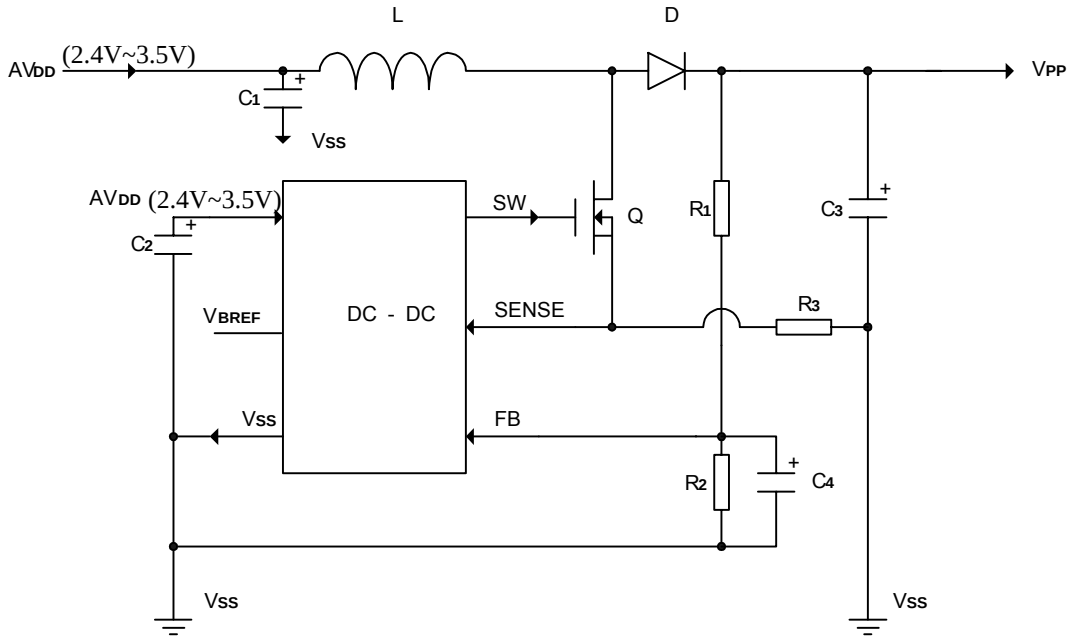
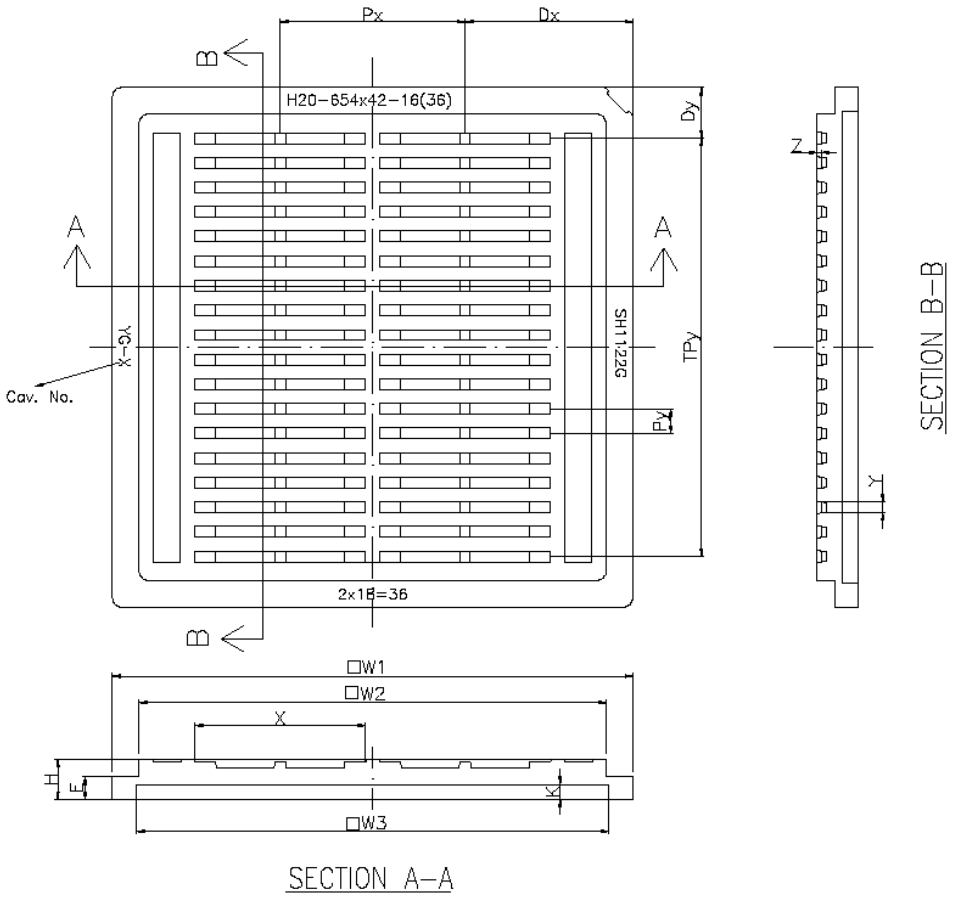


Figure. 21

Symbol	Value	Recommendation
L	10μH	LQH3C100K24
D	SCHOTTKY DIODE	20V@0.5A, MBR0520
Q	MOSFET	N-FET with low $R_{DS(ON)}$ and low V_{TH}, MGSF1N02LT1
R_1	820kΩ	1%, 1/8W
R_2	100kΩ	1%, 1/8W
R_3	0.12Ω	1%, 1/2W
C_1	22μF	Ceramic / 16V
C_2	0.1 – 1μF	Ceramic/16V
C_3	10μF	Low ESR/16V
C_4	56pF	Ceramic/16V

Package Information



SECTION A-A

	Spec	
	mm	(mil)
W1	50.70±0.10	(1996)
W2	45.50±0.10	(1791)
W3	45.95±0.10	(1809)
H	3.95±0.10	(156)
E	2.20±0.05	(87)
K	1.45±0.10	(57)
Dx	16.35±0.05	(644)
Dy	4.95±0.05	(195)
TPy	40.80±0.10	(1606)
Px	18.00±0.05	(709)
Py	2.40±0.05	(94)
X	16.60±0.05	(654)
Y	1.07±0.05	(42)
Z	0.40±0.05	(16)
N	36(pocket number)	

Ordering Information

Part No.	Package
SH1122G	Gold bump on chip tray

Spec Revision History

Version	Content	Date
1.0	Original	Jul. 2012
2.0	P1: change 'V_{PP} = 7.0V – 13.5V' to 'V_{PP} = 7.0V – 14V' P36: change the maximum value of V_{PP} to 14V	Aug. 2012
2.1	P37: modify the the value of I_{OL} when VDD1<2V P37: modify the min. and max. value of fosc	Dec. 2012
2.2	P33~P35: modify the power on/off sequence	Jun. 2013