

**RAiO**

**RA8806**

**Two Layers  
Character/Graphic  
LCD Controller  
Specification**

Simplify Version 1.1

October 15, 2008

## 1. General Description

RA8806 is a LCD controller for Dot-Matrix type STN-LCD which supports both character and graphic mode display. The RA8806 has built-in two Display Data RAM(DDRAM) for two layers display, and has an embedded font ROM which is capable of displaying the full-size(16x16 pixels) traditional Chinese font(BIG5, 13973 characters) or simplified Chinese font(GB, 9216 characters). RA8806-J is one controller in this series that consisting of Kanji and Hiragana according to the JIS standard Level-1 & 2 Kanji font (6,355 characters). RA8806 also contains 4x256 embedded half-size (8x16 pixels) characters that can display ISO8859-1 ~ 4(or called Latin-1 ~ 4) alphabets using at most of English speaking and Europe countries.

RA8806 supports 8080/6800 MPU protocol interface, which is capable of switching the interface with 4-bits or 8-bits data bus. For LCD driver interface, it can be set to 4-bits/8-bits data bus. The maximum resolution of RA8806 is 320x240 pixels in normal mode, and 640x240 or 320x480 pixels in extension mode. By using the font rotation mode, which can implement the “vertical” font display. The embedded intelligence touch panel controller provides the 4-wires resistance-type Touch Panel interface. The PWM output provides an easy contrast or back-light control method for LCD panel. RA8806 also provides a 4x8(32 keys) or 8x8(64 keys) powerful and smart Key-Scan interface includes long-key function. The flexible interrupt and polling mechanism can make it easy to control touch panel, key-scan and power mode functions. Also it can greatly reduce the MPU loading. The embedded 512Byte character generation RAM (CGRAM) allows user to build maximum 16 full-size or 32 half-size fonts. Even with the single layer display, the other unused layer can be used as CGRAM too. In this setting, the amazing 300 full-size and 600 half-size user created fonts or symbols are supported.

In addition, RA8806 supports 4 gray scale display in FRC mode. The bit-arrangement is compatible for most gray level picture and easy to program. RA8806 also includes many useful functions, like area scroll, font inverse/bold/enlargement, memory clear function and so on. An innovative mechanism of “no-flicker” mode is provided in RA8806. It’s effective for removing the “flicker” in frequently display data R/W. User can easily improve the display quality by RA8806.

RA8806 is a powerful and flexible LCD controller. It provides the total solution for the middle-size mono LCD controller. User can save large amount of time for system development and the cost of hardware system.

## 2. Feature

- ◆ Support text and graphics Mode.
- ◆ Maximum resolution: 320x240 with 2-Layers overlay display (AND, OR, NOR and XOR).
- ◆ Extension Mode: 640x240 or 320x480 with single layer.
- ◆ Support 4/8-bit of 6800/8080 MPU interface and 4/8-bits driver interface.
- ◆ Built-In smart 8x8 or 4x8 key-scan circuit with programmable long key function.
- ◆ Support horizontal and vertical area scrolling
- ◆ Built-In GB/BIG5/JIS standard Kanji Level 1 & 2 and ASCII Font ROM.
- ◆ Support 90°, 180°, 270° font and display rotation.
- ◆ Support Font enlargement (x1~x4 in Horizontal and Vertical direction)
- ◆ Built-In 512Byte CGRAM for user-created font:
  - \_ Half-size: 8x16
  - \_ Full-size: 16x16
- ◆ Un-used DPRAM can be used as a CGRAM of 300 full-size or 600 half-size characters.
- ◆ Flexible interrupt/polling mechanism for touch panel, key-scan and power mode programming.
- ◆ Support font alignment function.
- ◆ Support 4 gray scale display (FRC mode).
- ◆ Support bold font and row-row interval setting
- ◆ Built-In smart resistor type touch panel controller.
- ◆ Built-In PWM for contrast or back-light control
- ◆ Power mode to reduce power consumption.
- ◆ Clock source: 4~12MHz crystal or external clock
- ◆ Built-In a 5V-to-3V DC-DC converter
- ◆ Power supply: 2.4~5.5V
- ◆ Package: Die, LQFP-100, TQFP-80 Pins

### 3. Block Diagram

Figure 3-1 is the internal block diagram of RA8806. The RA8806 consists of Display Data RAM, Font ROM, Register Block, Analog to Digital Converter (ADC), Pulse Width Modulation (PWM), LCD driver interface and microprocessor interface. Figure 3-2 is the system block for application of RA8806.

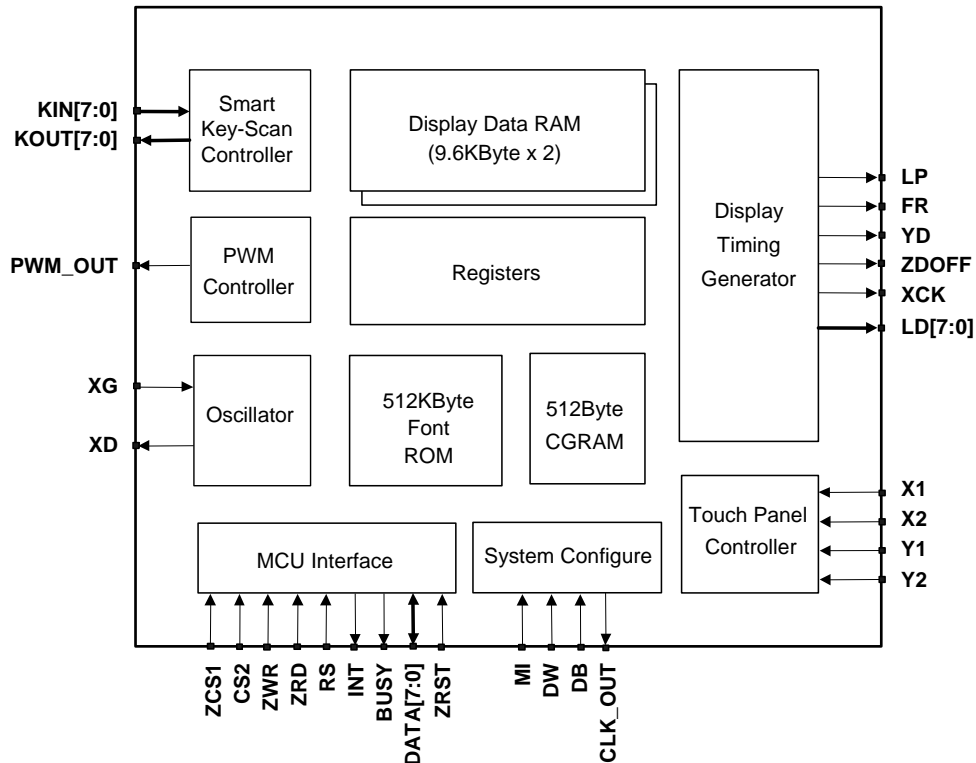


Figure 3-1: RA8806 Block Diagram

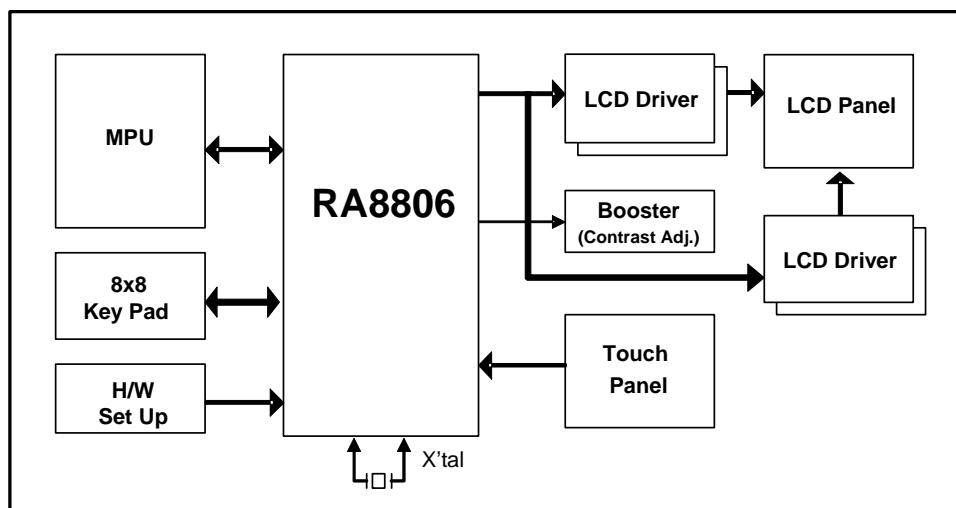


Figure 3-2: RA8806 System Block Diagram

## 4. Pin Definition

### 4-1 MPU Interface

Pin Name	I/O	Description															
DATA[7:0]	I/O	<p><b>Data Bus</b> These are data bus for data transfer between MPU and RA8806. The high nibble DATA[7:4] is output and should keep floating when 4-bits data bus mode is used.</p>															
ZRD (EN)	I	<p><b>Enable/Read Enable</b> When MPU I/F is 8080 series, this pin (ZRD) is used as data read, active low. When MPU I/F is 6800 series, this pin (EN) is used as Enable, active high.</p>															
ZWR (ZRW)	I	<p><b>Write/Read-Write</b> When MPU I/F is 8080 series, this pin (ZWR) is used as data write, active low. When MPU I/F is 6800 series, this pin(ZRW) is used as data read/write control. Active high for read and active low for write.</p>															
RS	I	<p><b>Command / Data Select Input</b> The pin is used to select command/data cycle. RS = 0, data Read/Write cycle is selected. RS = 1, status read/command write cycle is selected. In 8080 interface, usually it connects to "A0" address pin.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RS</th> <th>ZWR</th> <th>Access Cycle</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Data Write</td> </tr> <tr> <td>0</td> <td>1</td> <td>Data Read</td> </tr> <tr> <td>1</td> <td>0</td> <td>CMD Write</td> </tr> <tr> <td>1</td> <td>1</td> <td>Status Read</td> </tr> </tbody> </table>	RS	ZWR	Access Cycle	0	0	Data Write	0	1	Data Read	1	0	CMD Write	1	1	Status Read
RS	ZWR	Access Cycle															
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ZCS1 CS2	I	<p><b>Chip Select Input</b> The MPU interface of RA8806 is active only when ZCS1 is low and CS2 is high.</p>															
INT	O	<p><b>Interrupt Signal Output</b> The interrupt output for MPU to indicate the status of RA8806. It could be setup active high or low.</p>															
BUSY	O	<p><b>Busy Signal Output</b> This is a busy output to indicate the RA8806 is in busy state. It could be set to active high or active low by register. The RA8806 can't access MPU cycle when BUSY pin is active. It could be used for MPU to poll busy status by connecting it to I/O port.</p>															

### 4-2 Clock Interface

Pin Name	I/O	Description
XG	I	<p><b>X'tal Input</b> In internal clock mode, this pin connects to external X'tal(4M ~ 12MHz). In external clock mode, it connects to external clock.</p>
XD	O	<p><b>X'tal Output</b> This pin connects to external X'tal(4M ~ 12MHz). In external clock mode, it keeps floating.</p>

### 4-3 Peripheral Interface

Pin Name	I/O	Description
ZRST	I	<b>Reset Signal Input</b> This active-low input performs a hardware reset on the RA8806. It is a Schmitt-trigger input with pull-up resistor for enhanced noise immunity; however, care should be taken to ensure that it is not triggered if the supply voltage is lowered.
X1	I	<b>Touch Panel Input</b> The left analog input pin(XL) of 4-wire touch panel.
X2	I	<b>Touch Panel Input</b> The right analog input pin(XR) of 4-wire touch panel.
Y1	I	<b>Touch Panel Input</b> The top analog input pin(YU) of 4-wire touch panel. If user want to use Touch Panel function, please add a 39K~51Kohm external pull-up resistor on this pin.
Y2	I	<b>Touch Panel Input</b> The bottom analog input pin(YD) of 4-wire touch panel.
PWM_OUT	O	<b>PWM Output Signal</b> This output signal is used to control back-light module or booster circuit.
KIN[7:0]	I	<b>Key Pad Input</b> These pins are keypad inputs with pull-up resistors. For un-used input, please keep floating.
KOUT[7:0]	O	<b>Key Pad Output</b> These pins are keypad outputs. For un-used pin, please keep floating.
CLK_OUT	O	<b>Clock Output</b> This is a multi-function output pin that depending on the value of register REG[01h] Bit-6. REG[01h] Bit-6 = 0: The pin is the output of internal system clock. REG[01h] Bit-6 = 1: The pin indicate the SLEEP state of Status Register(0: Normal Mode, 1: Sleep Mode).
DW	I	<b>LCD Driver Data Bus Select</b> This pin is used to select data bus of LCD driver is 8-bits or 4-bits: 0 : LCD driver data bus is 4-bits, LD[3:0] is used. 1 : LCD driver data bus is 8-bits, LD[7:0] is used. When 4-bits data bus is used, LD[7:4] need to keep floating. RA8806T1N does not support this function, its LCD driver data bus is fix 4-bits.
MI	I	<b>MPU Type Select</b> This pin is used to select MPU interface protocol: 0 : Intel 8080 series MPU interface. 1 : Motorola 6800 series MPU interface.
DB	I	<b>8080/6800 MPU Data Bus Select</b> This pin is used to select data bus width. 0 : 4-bits MPU I/F, DATA[3:0] is used. 1 : 8-bits MPU I/F, DATA[7:0] is used. When 4-bits data bus is used, DATA[7:4] need to keep floating.

#### 4-4 LCD Driver Interface

Pin Name	I/O	Description
YD	O	<b>Start Signal of LCD Per Frame</b> YD is the reset pulse for the COM driver, it's active during the last COM period of each frame and latched by LP signal.
FR	O	<b>LCD AC Wave Output</b> This signal controls the Level Shift of LCD driver. Normally it works as VDD/GND interlacing to prevent the liquid crystal polarization.
LP	O	<b>LCD Common Latch</b> LP is the latch pulse for the shift register of SEG driver to SEG output. It is also used as COM driver shift clock.
XCK	O	<b>LCD Clock</b> XCK is the latch pulse of the LCD driver data(LD[7:0]) for SEG driver. The falling edge of XCK will latch the LD[7:0] (or LD[3:0] for 4-bits driver) to the shift register.
ZDOFF	O	<b>LCD Display OFF</b> This signal is used to control the LCD Display On or Off. 0 : Display off. 1 : Display on.
LD[7:0]	O	<b>LCD Driver Data Bus</b> When 8-bits LCD driver IC is used. LD[7:0] are connected to LCD driver data bus. When 4-bits driver is used, LD[3:0] are connected to LCD driver data bus and LD[7:4] keep floating. RA8806T1N supports LD[3:0] only.

#### 4-5 Power

Pin Name	I/O	Description
VDDH	P	<b>5V Power</b> This is the source power for DC to DC converter. In 5V power application, it is connected to 5V. If 3V application is used, then keep this pin floating.
VDD	P	<b>3V Power</b> If the pin VDDH connects to 5V power then the pin will driving 3V power, and must add an external 1uF capacitor to GND. If 3V application is used, then connecting this pin to external 3V power directly.
VDDP	P	<b>Power for I/O Buffer</b> VDDP can be 3V or 5V.
AVDD	P	<b>Analog Power for ADC Touch Panel Controller</b> AVDD can be 3V or 5V.
GND GNDP	P	<b>Ground</b>
AGND	P	<b>Analog Ground for ADC Touch Panel Controller</b> Connect this pin to 0V earth ground(GND).
TESTMD	I	<b>Test Mode</b> This pin is used for test only. It has internal pull-low and need to keep floating.
TESTI	I	<b>Test Pin</b> The pin is used for test function, It has internal pull-low and need to keep floating.

**5. Package**

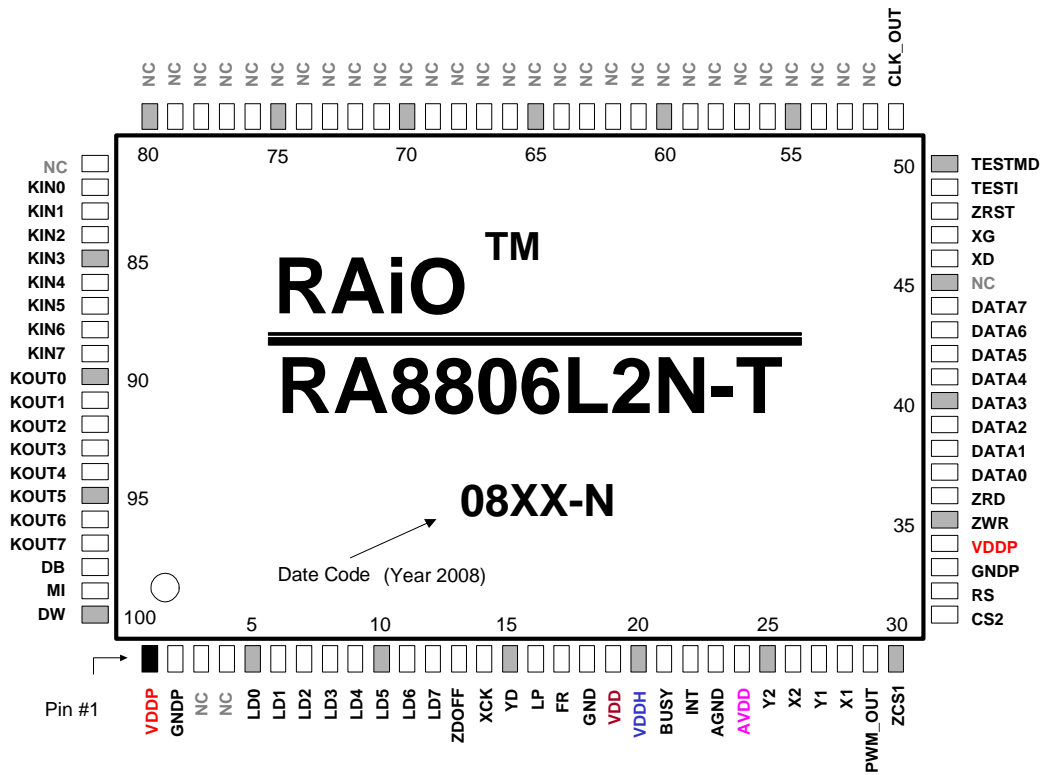


Figure 5-1: LQFP-100Pins Pin Assignment

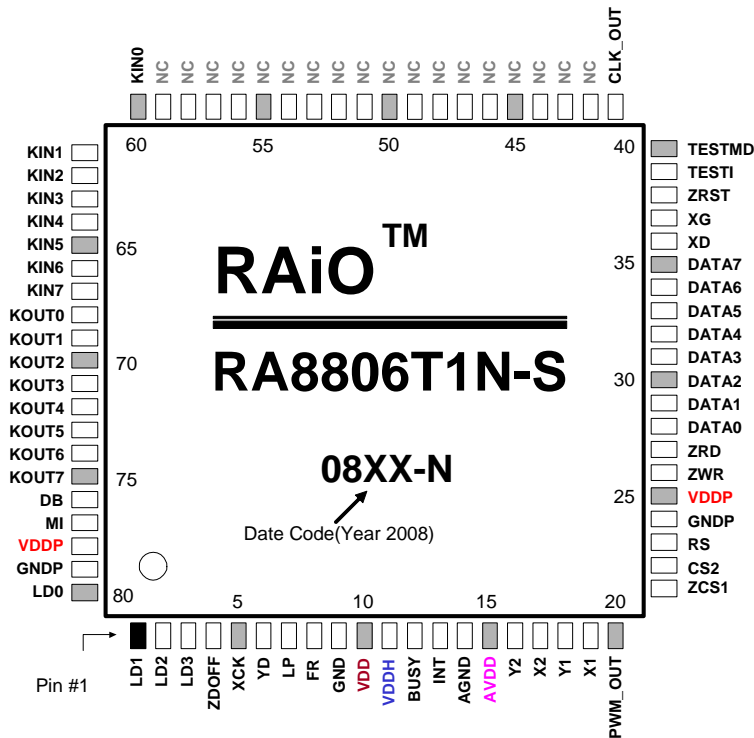


Figure 5-2: TQFP-80Pins Pin Assignment

## 6. Part Number

Table 6-1 : Part Number

Product Name (Full Name)	Resolution (Max)	Package	Font ROM	ASCII ROM	RoHs Compliance
RA8806L2N-T	320x240 (Note 1)	LQFP-100 (20x14)	Traditional Chinese (Note 2)	ISO-8859-1 ~ 4	Yes
RA8806L2N-S			Simple Chinese (Note 2)	ISO-8859-1 ~ 4	Yes
RA8806L2N-J			Japanese Kanji	ISO-8859-1 ~ 4	Yes
RA8806T1N-T		TQFP-80 (10x10)	Traditional Chinese (Note 2, 3)	ISO-8859-1 ~ 4	Yes
RA8806T1N-S			Simple Chinese (Note 2, 3)	ISO-8859-1 ~ 4	Yes
RA8806T1N-J			Japanese Kanji (Note 3)	ISO-8859-1 ~ 4	Yes
RA8806-T		Die	Traditional Chinese	ISO-8859-1 ~ 4	Yes
RA8806-S			Simple Chinese	ISO-8859-1 ~ 4	Yes

**Notes:**

1. In Extension Mode, the maximum resolution is 640x240 or 320x480.
2. In both Traditional and Simple Chinese font, it built-in 52 basic Japanese font.
3. LCD driver data bus of RA8806T1N is 4-bits.

Table 6-2 : RA8806L2N vs. RA8806T1N

Difference	RA8806L2N	RA8806T1N
Package	LQFP-100Pins 20mm x 14mm	TQFP-80Pins 10mm x 10mm
LCD Data Bus	4-bits or 8-bits	4-bits