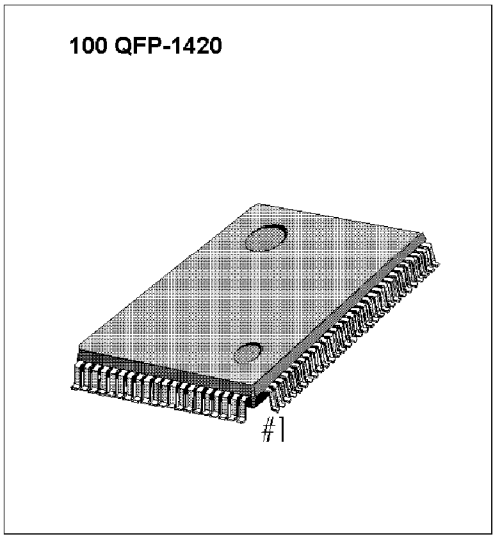
INTRODUCTION

The KS0107B is a LCD driver LSI with 64 channel output for dot matrix liquid crystal graphic display system. This device provides 64 shift register and 64 output driver. It generates the timing signal to control the KS0108B segment driver. The KS0107B is fabricated by low power CMOS high voltage process technology and compose of the liquid crystal display system in combination with the KS0108B segment driver.



FEATURES

- Dot matrix LCD common driver with 64 channel output.
- 64 bits shift register ot internal LCD driver circuit.
- Internal timing generator circuit for dynamic display.
- Selectable master/slave mode.

- Applicable LCD duty: 1/48, 1/64,1/96,1/128
- Power supply voltage: + 5V ± 10%
- LCD driving voltage: 8V~17V(V_{DD}-V_{EE})
- Interface

Driver		controller
COMMON	SEGMENT	
Other KS0107B	KS0108B	MPU

- High voltage CMOS process.
- 100QFP and bare chip available.

BLOCK DIAGRAM

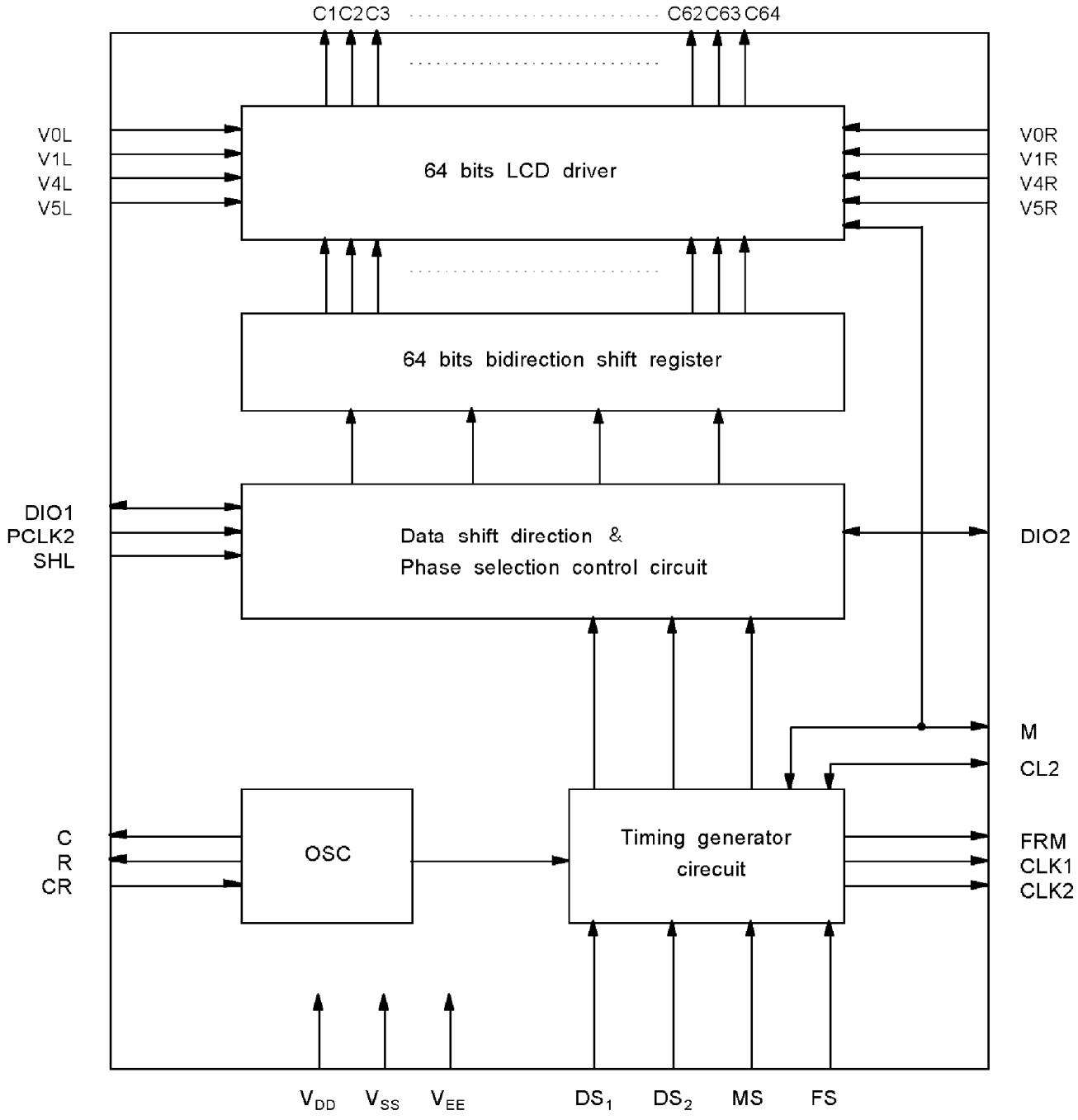


Fig. 1. KS0107B Functional block diagram

PIN CONFIGURATION

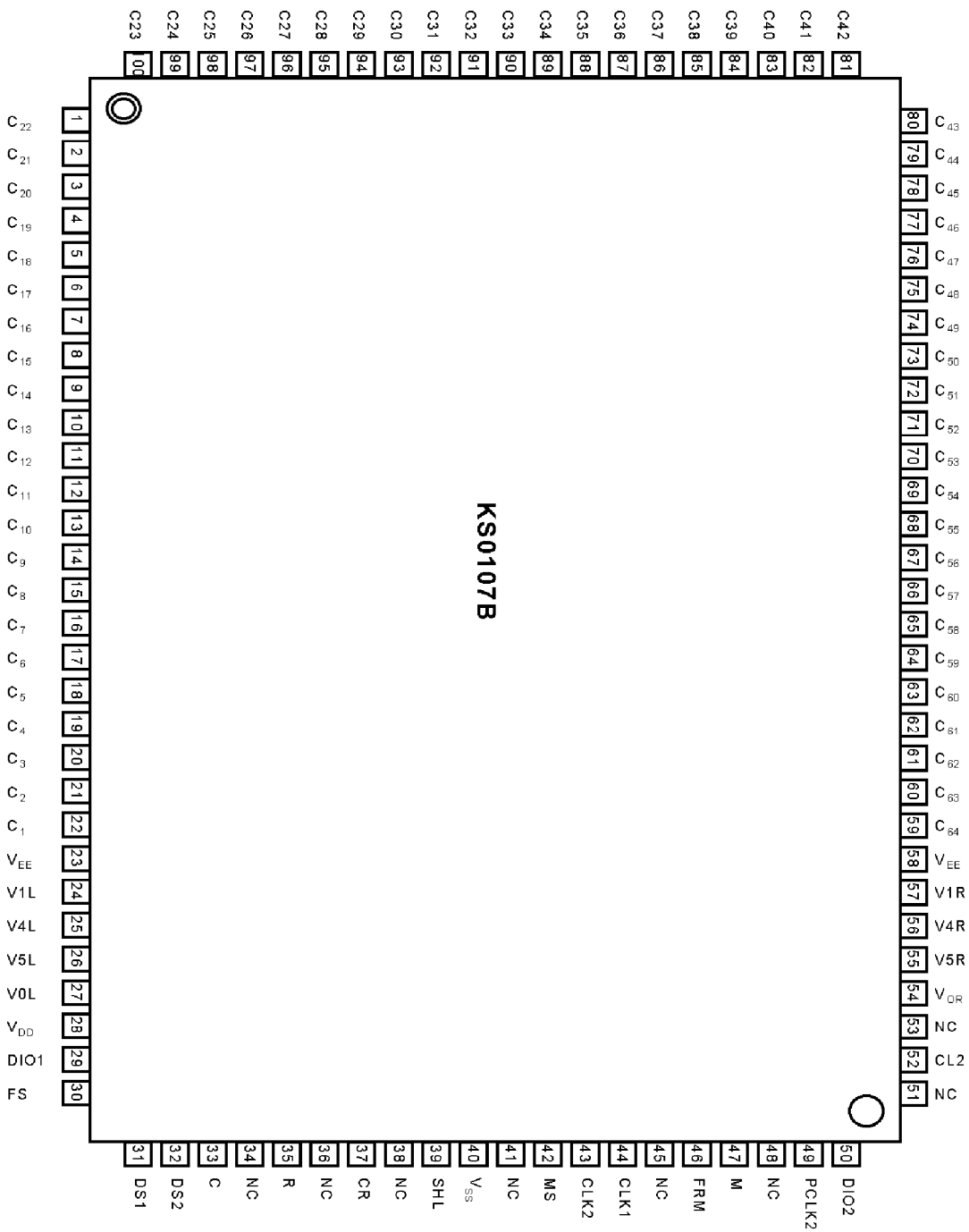
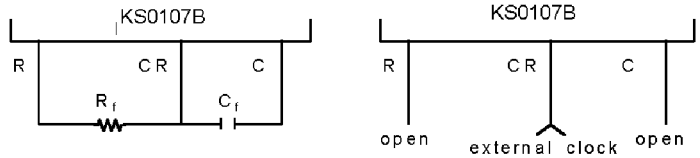


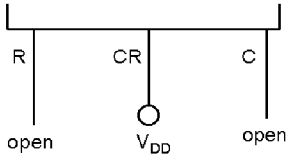
Fig. 2. 100 QFP Top View

PIN DESCRIPTION

<table>
<tr><th>PIN(NO)</th><th>SYMBOL</th><th>INPUT/OUTPUT</th><th>DESCRIPTION</th></tr>
<tr><td>28
40
23,58</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Power</td><td>For internal logic circuit (+5V ± 10%)
GND (0V)
For LCD driver circuit</td></tr>
<tr><td>27, 54
24, 57
25, 56
26, 55</td><td>V0L, V0R
V1L, V1R
V4L, V4R
V5L, V5R</td><td>Power</td><td>Bias supply voltage terminals to drive LCD.
<table><tr><th>Select Level</th><th>Non-Select Level</th></tr><tr><td>V0L(R), V5L(R)</td><td>V1L(R), V4L(R)</td></tr></table>V0L and V0R is connected by the same voltage.</td></tr>
<tr><td>42</td><td>MS</td><td>Input</td><td>Selection of master/slave mode
i) Master mode (MS=1)
DIO1, DIO2, CL2 and M is output state.
ii) Slave mode (MS=0)
SHL=1 → DIO1 is input state(DIO2 is output state)
SHL=0 → DIO2 is input state(DIO1 is output state)
CL2 and M is input state.</td></tr>
<tr><td>39</td><td>SHL</td><td>Input</td><td>Selction of data shift direction.
<table><tr><th>SHL</th><th>Data shift direction</th></tr><tr><td>H</td><td>DIO1 → C1 → ... → C64 → DIO2</td></tr><tr><td>L</td><td>DIO2 → C64 → ... → C1 → DIO1</td></tr></table></td></tr>
<tr><td>49</td><td>PCLK2</td><td>Input</td><td>Selection of shift clock (CL2) phase.
<table><tr><th>PCLK2</th><th>shift clock(CL2) phase</th></tr><tr><td>H</td><td>data shift at the rising edge of CL2</td></tr><tr><td>L</td><td>data shift at the falling edge of CL2</td></tr></table></td></tr>
<tr><td>30</td><td>FS</td><td>Input</td><td>Selection of oscillation frequency.
i) Master mode
When the freme frequency is 70Hz, the oscillation frequency should be
fosc=430KHz at FS=1 (V_{DD})
fosc=215KHz at FS=0 (V_{SS})
ii) Slave mode
Connect to V_{DD}.</td></tr>
<tr><td>31
32</td><td>DS1,
DS2</td><td>Input</td><td>Selectiom of display duty.
i) Master mode
<table><tr><th>DS1</th><th>DS2</th><th>Duty</th></tr><tr><td>L</td><td>L</td><td>1/48</td></tr><tr><td>L</td><td>H</td><td>1/64</td></tr><tr><td>H</td><td>L</td><td>1/96</td></tr><tr><td>H</td><td>H</td><td>1/128</td></tr></table>ii) Slave mode : Connect to V_{DD}.</td></tr>
</table>

PIN DESCRIPTION (continued)

<table>
<tr><th>PIN(NO)</th><th>SYMBOL</th><th>INPUT/OUTPUT</th><th>DESCRIPTION</th></tr>
<tr><td>33
35
37</td><td>C
R
CR</td><td></td><td>RC Oscillator
i) Master mode
 

ii) Slave mode
 
</td></tr>
<tr><td>44, 43</td><td>CLK1,
CLK2</td><td>Output</td><td>Operating clock output for the KS0108B
i) Master mod Connection to CLK1 and CLK2 of the KS0108B
ii) Slave mode Open</td></tr>
<tr><td>46</td><td>FRM</td><td>Output</td><td>Synchronous frame signal.
i) Master mode Connection to FRM of the KS0108B
ii) Slave mode Open</td></tr>
<tr><td>47</td><td>M</td><td>Input/Output</td><td>Alternating signal input for LCD driving.
i) Master mode: output state
Connection to M of the KS0108B
ii) Slave mode: input state
Connection to the controller</td></tr>
<tr><td>52</td><td>CL2</td><td>Input/Output</td><td>Data shift clock
i) Master mode: output state
Connection to CL of the KS0108B
ii) Slave mode: input state
Connection to shift clock terminal of the controller.</td></tr>
<tr><td>29

50</td><td>DIO1

DIO2</td><td>Input/Output</td><td>Data input/output pin of internal shift register.
<table>
<tr><th>MS</th><th>SHL</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>22~1
100~59</td><td>C1~C64</td><td>Output</td><td>Common signal output for LCD driving.
<table>
<tr><th>DATA</th><th>M</th><th>OUT</th></tr>
<tr><td>L</td><td>L</td><td>V_1</td></tr>
<tr><td>L</td><td>H</td><td>V_4</td></tr>
<tr><td>H</td><td>L</td><td>V_5</td></tr>
<tr><td>H</td><td>H</td><td>V_0</td></tr>
</table></td></tr>
<tr><td>34,36,38,41
45,48,51,53</td><td>NC</td><td></td><td>No Connection</td></tr>
</table>

MAXIUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating Voltage	V_{DD}	-0.3~+7.0	V	*1
Supply Voltage	V_{EE}	V_{DD}-19.0~V_{DD}+0.3	V	*4
Driver Supply Voltage	V_B	-0.3~V_{DD}+0.3	V	*1,2
	V_{LCD}	V_{EE}-0.3~V_{DD}+0.3	V	*3,4
Operating Temperature	T_{OPR}	-30~+85	℃	-
Storage Temperature	T_{STG}	-55~+125	℃	-

*1. Based on V_{SS}=0V
*2. Applies to input terminals and I/O terminals at high impedance.
(Except V0L(R), V1L(R), V4L(R) and V5L(R))
*3. Applies to V0L(R), V1L(R), V4L(R) and V5L(R).
*4. Voltgae level: $V_{DD} \geq$ V0L=V0R $\geq$ V1L=V1R $\geq$ V4L=V4R $\geq$ V5L=V5R $\geq V_{EE}$.

ELECTRICAL CHARACTERISTICS

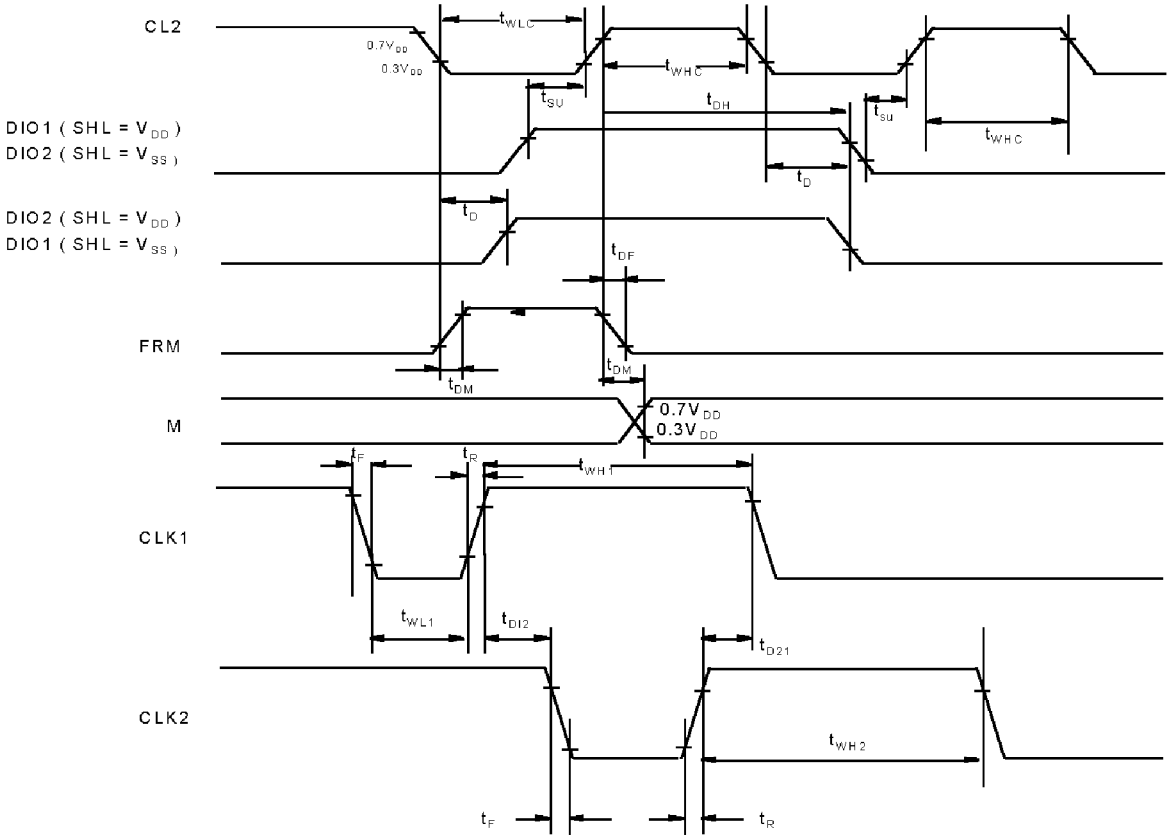
DC Characteristics (V_{DD}=+5V ± 10%, V_{SS}=0V, | V_{DD}-V_{EE} | =8~17V, T_a=-30 ~ +85 ℃)

Characteristic		Symbol	condition	Min	Typ	Max	Unit	Note
Input Voltage	High	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V	*1
	Low	V_{IL}		V_{SS}	-	0.3V_{DD}		
Output Voltage	Hogh	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	-	V	*2
	Low	V_{OL}	I_{OL}=0.4mA	-	-	0.4		
Input Leakage Current		I_{LKG}	V_{IN}=V_{DD}~V_{SS}	-1.0	-	1.0	μA	*1
OSC Frequency		f_{OSC}	Rf=47K Ω ± 2% Cf=20pf ± 5%	315	450	585	KHz	
On Resistance (Vdiv-Ci)		R_{ON}	V_{DD}-V_{EE}=17V Load current ± 150 μA	-	-	1.5	K Ω	
Operating Current		I_{DD1}	Master mode 1/128 Duty	-	-	1.0	mA	*3
		I_{DD2}	Slave mode 1/128 Duty	-	-	200	μA	*4
Supply Current		I_{EE}	Master mode 1/128 Duty	-	-	100		*5
Operating Frequency		f_{op1}	Master mode External clock	50	-	600	KHz	
		f_{op2}	Slave mode	0.5	-	1500		

*1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
*2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the output state.
*3. This value is specified about current flowing through V_{SS}.
Internal oscillation circuit: Rf=47k Ω, Cf=20pF
Each terminals of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
*4. This value is specified about current flowing through V_{SS}.
Each terminals is DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD}, MS is connected to V_{SS} and CL2, M, DIO1 is external clock.
*5. This value is specified about current flowing through V_{EE}.
Don't connect to V_{LCD} (V1~V5).

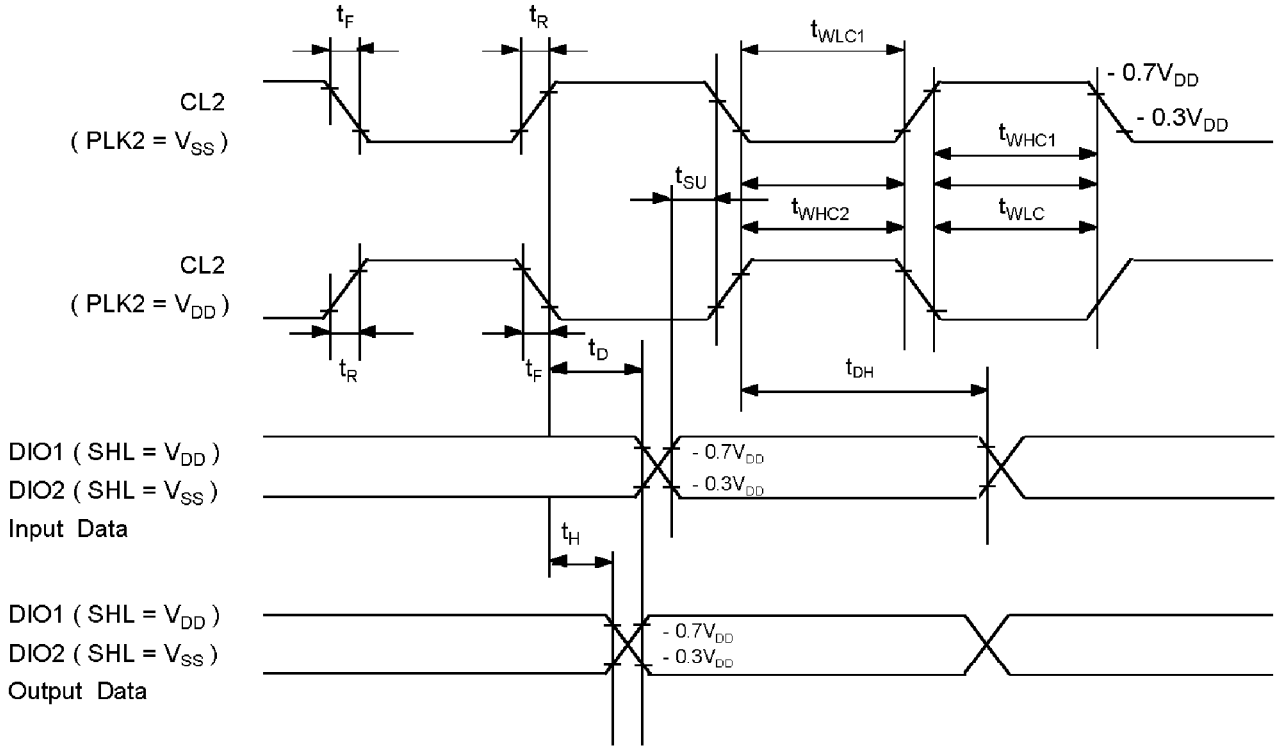
AC Charcteristics (VDD=5V ± 10%, Ta=-30 ℃~+85 ℃)

(1)Master mode (MS=V_{DD}, PCLK2=V_{DD}, Cf=20pF, Rf=47K Ω)



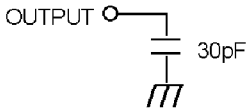
Characteristic	Symbol	Min	Typ	Max	Unit
Data Setup Time	t_{SU}	20	-	-	μs
Data Hold Time	t_{DH}	40	-	-	
Data Delay Time	t_D	5	-	-	
FRM Delay Time	t_{DF}	-2	-	2	
M Delay Time	t_{DM}	-2	-	2	
CL2 Low Level Width	t_{WLC}	35	-	-	
CL2 High Level Width	t_{WHC}	35	-	-	
CLK1 Low Level Width	t_{WL1}	700	-	-	ns
CLK2 Low Level Width	t_{WL2}	700	-	-	
CLK1 High Level Width	t_{WH1}	2100	-	-	
CLK2 High Level Width	t_{WH2}	2100	-	-	
CLK1-CLK2 Phase Difference	t_{D12}	700	-	-	
CLK2-CLK1 Phase Difference	t_{D21}	700	-	-	
CLK1, CLK2 Rise/Fall Time	t_R/t_F	-	-	150	

(2) Slave mode (MS=V_{SS})



Characteristics	Symbol	Min	Typ	Max	Unit	Note
CL2 Low Level Width	t_{WLC1}	450	-	-	ns	PCLK2=V_{SS}
CL2 High Level Width	t_{WHC1}	150	-	-	ns	PCLK2=V_{SS}
CL2 Low Level Width	t_{WLC2}	150	-	-	ns	PCLK2=V_{DD}
CL2 High Level Width	t_{WHL}	450	-	-	ns	PCLK2=V_{DD}
Data Setup Time	t_{SU}	100	-	-	ns	
Data Hold Time	t_{DH}	100	-	-	ns	
Data Delay Time	t_D	-	-	200	ns	*1
Output Data Hold Time	t_H	10	-	-	ns	
CL2 Rise/Fall Time	t_R/t_F	-	-	30	ns	

*1; Connect load CL=30pF



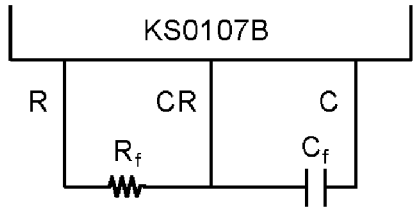
FUNCTIONAL DESCRIPTION

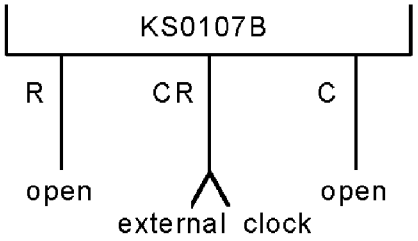
1.RC Oscillator

The RC Oscillator generates CL2, M,FRM, of the KS0107B and CLK1, CLK2 of the KS0108B by the oscillation resister R and capacitor C.

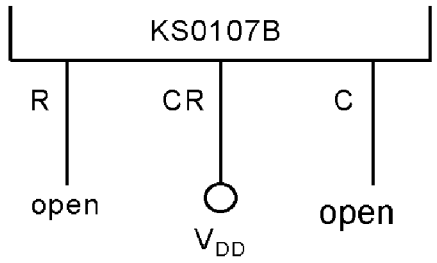
When selecting the master/slave, oscillation circuit is as following:

1) Master Mode





2) Slave Mode



2. Timing Genertion Circuit

It generates CL2, M, FRM, CLK1, and CLK2 by the frequency from oscillation circuit.

1) Selection of Master/Slave (M/S)

When M/S, is "H", it generates CL2, M, FRM, CLK1, and CLK2 internally. When M/S is "L", it operates by receiving M, CL2 from master device.

2) Frequency Selection (FS)

To adjust FRM by 70Hz, the oscillation frequency should be as following:

FS	Oscillation Frequency
H	f_{OSC}=430KHz
L	f_{OSC}=215Khz

In the slave mode, it is connected to V_{DD}.

3) Duty Selection (DS1, DS2)

It provides various duty selection according to DS1, DS2.

DS1	DS2	DUTY
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

3. Data Shift & Phase Select Control

1) Phase Selection

It is a circuit to shift data on synchronization or rising edge or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

2) Data Shift Direction Selection

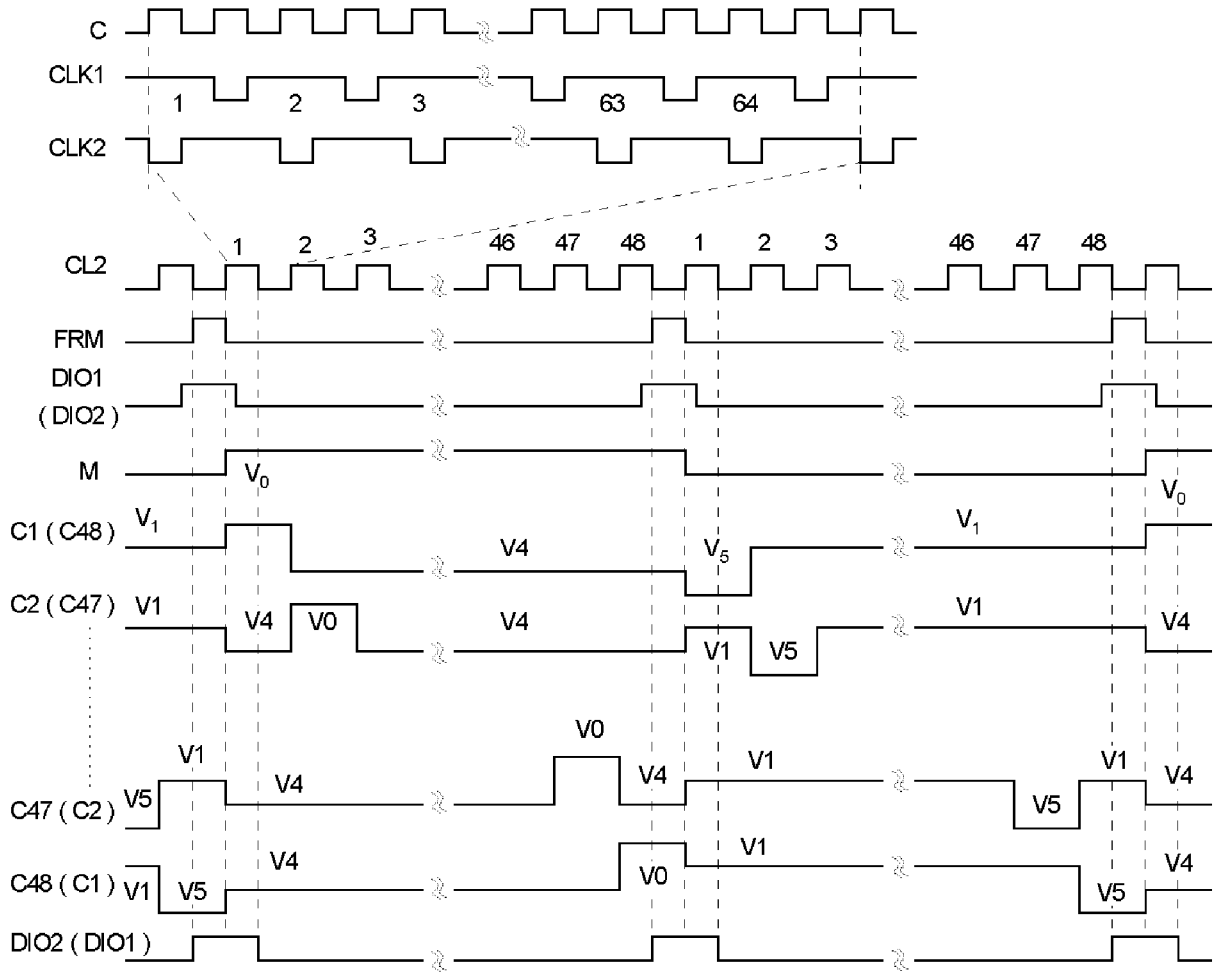
When M/S is connected to V_{DD}, DIO1 and DIO2 terminal is only output.
When M/S is connected to V_{SS}, it depends on the SHL.

MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1 → C64
	L	Output	Output	C64 → C1
L	H	Input	Output	DIO1 → C1 → C64 → DIO2
	L	Output	Input	DIO2 → C64 → C1 → DIO1

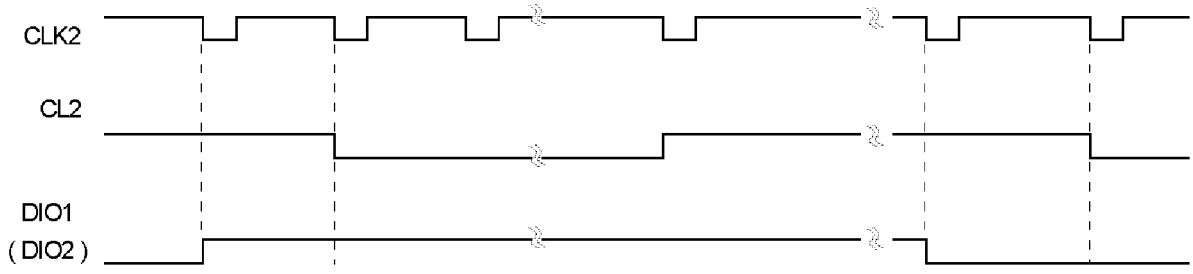
TIMING DIAGRAM

(1) 1/48 duty timing (Master mode)

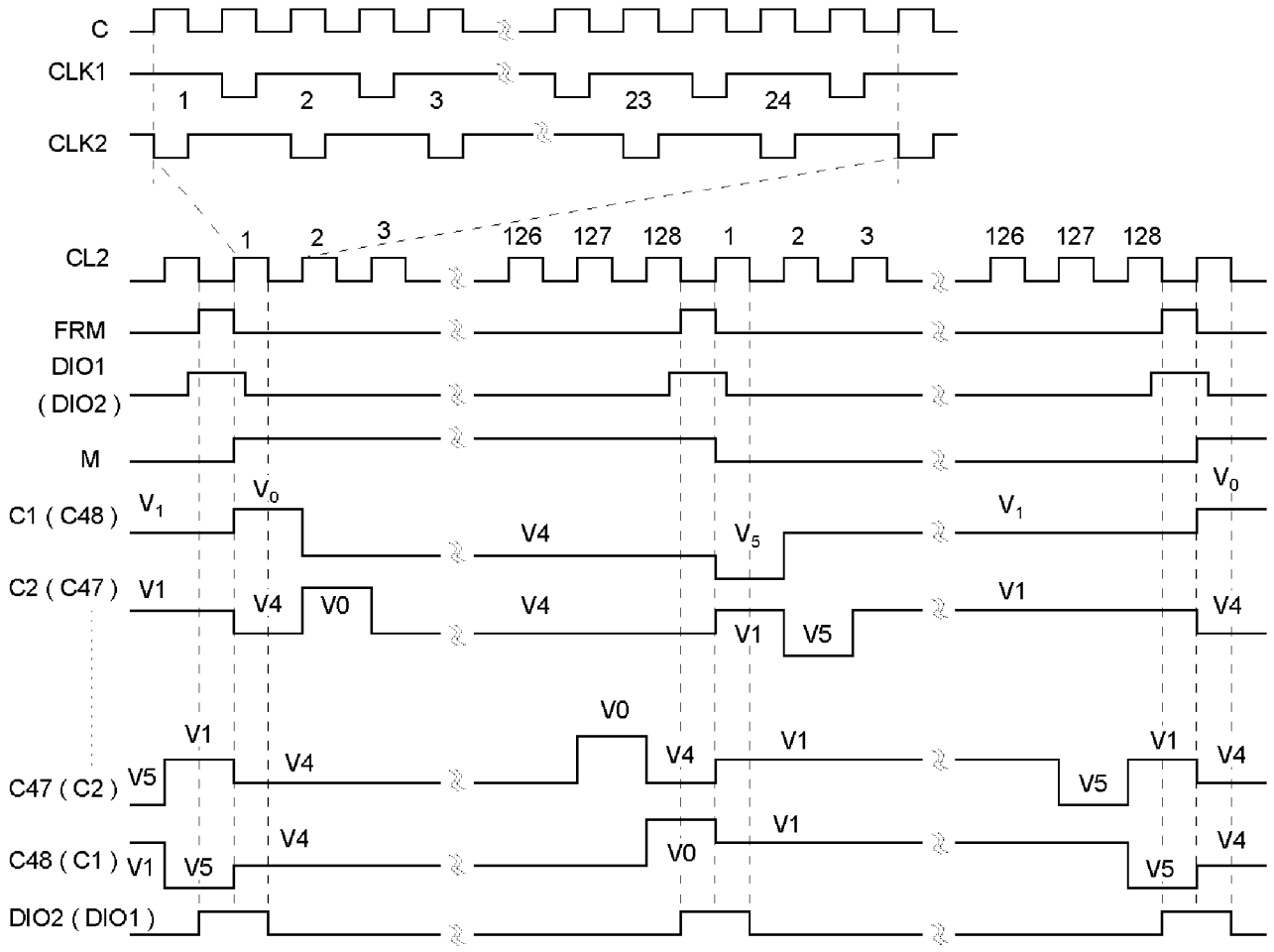
Condition: DS1=L, DS=L, SHL=H(L), PCLK2=H



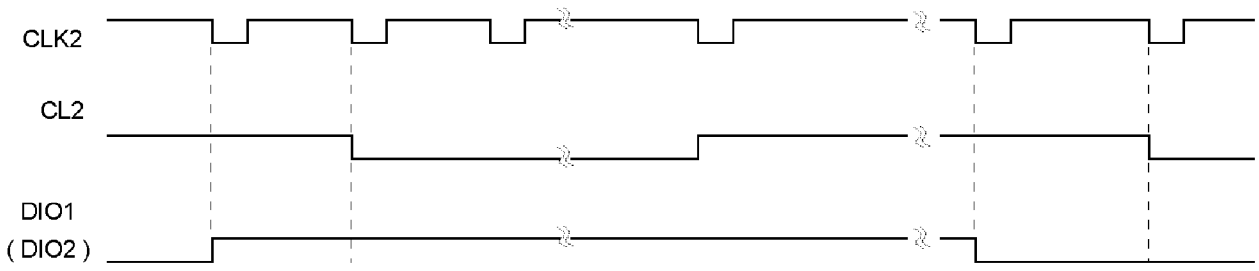
- relation of CL2 & DIO1 (DIO2)



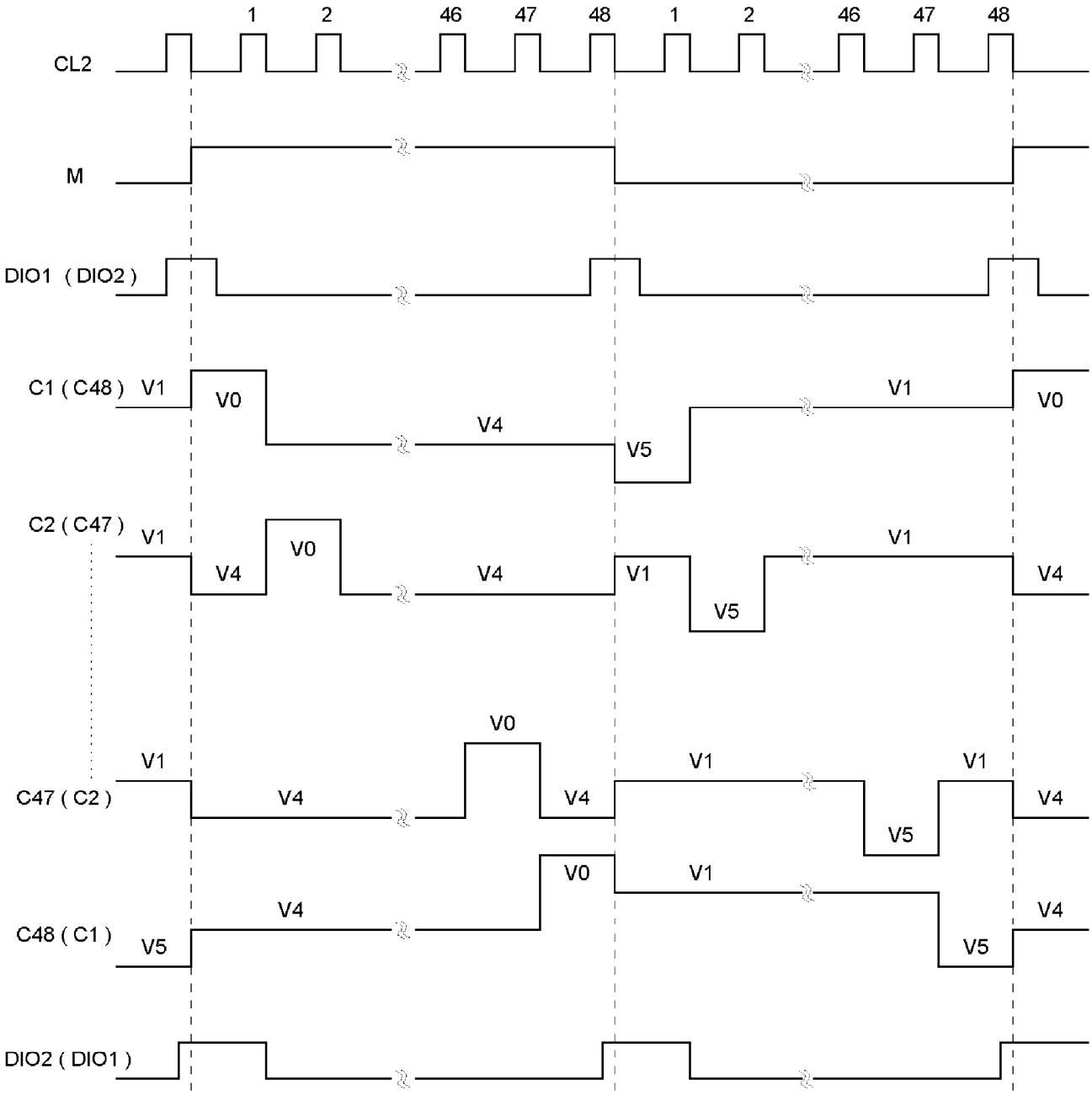
(2) 1/128 duty timing (Master mode)
- Condition: DS1=H, DS2=H, SHL=H(L), PCLK2=H



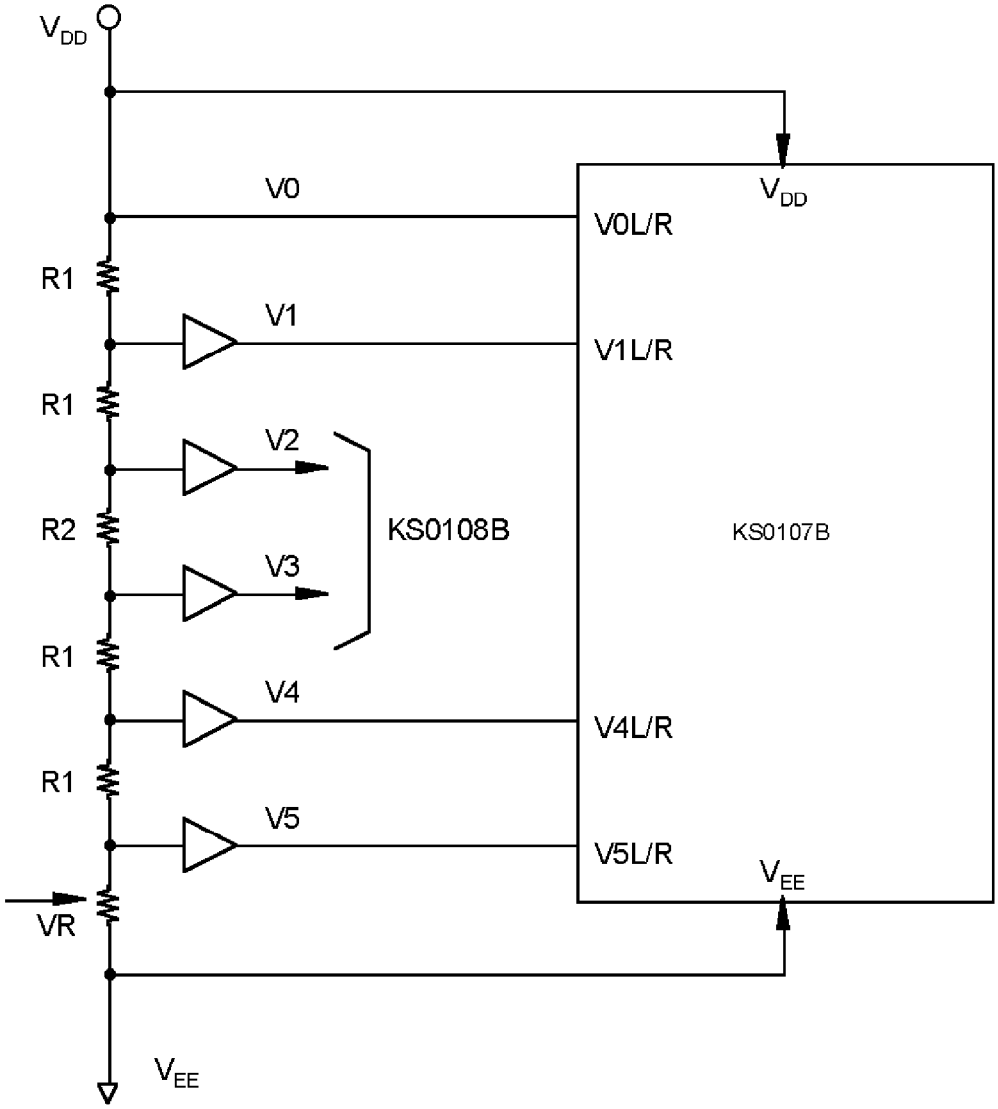
- relation of CL2 & DIO1 (DIO2)



(3) 1/48 duty timing (Slave mode)
- Condition: PCLK2=L, SHL=H(L)



(4) Power driver circuit



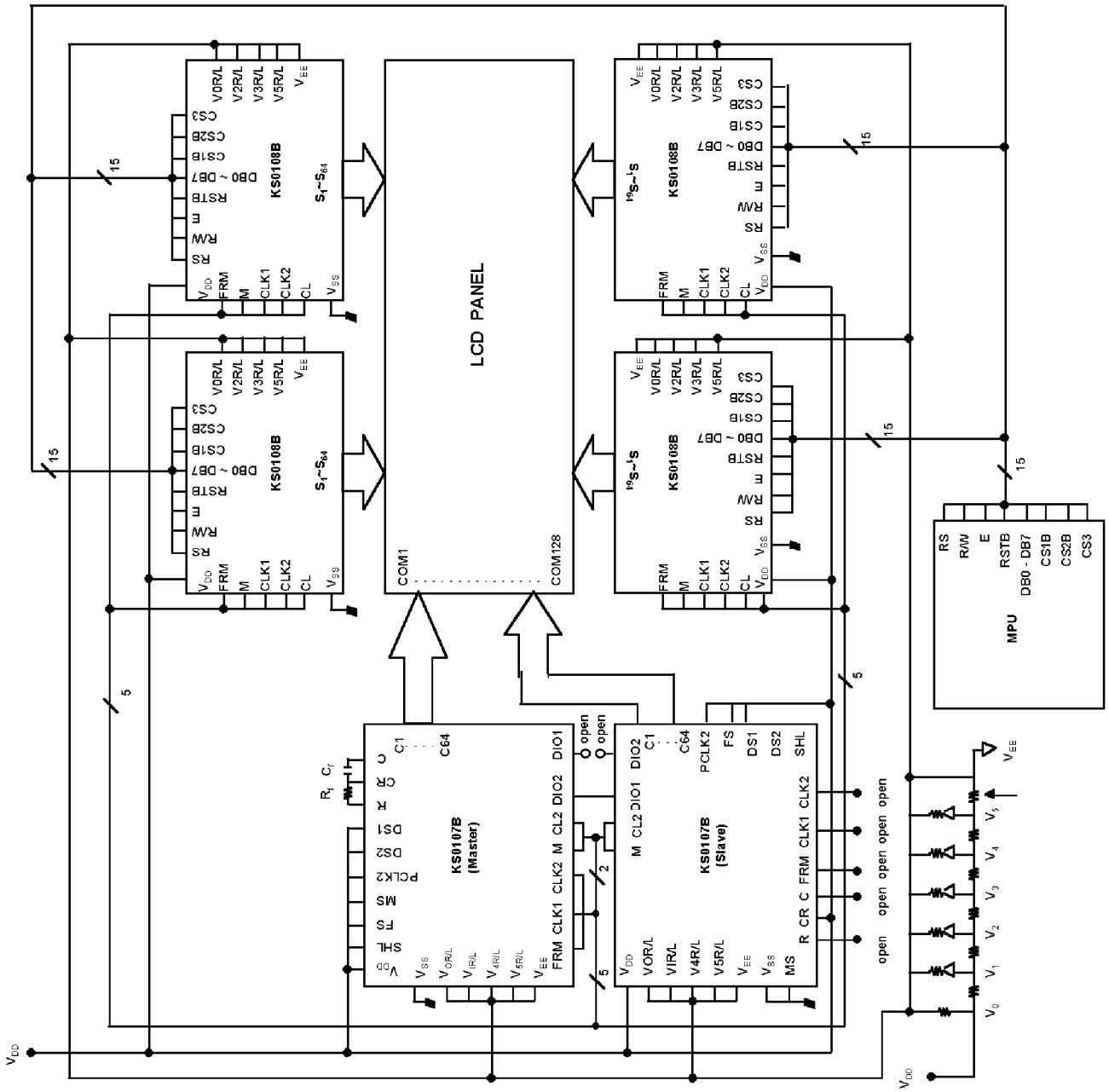
relation of duty & bias

DUTY	BIAS	Rdiv
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

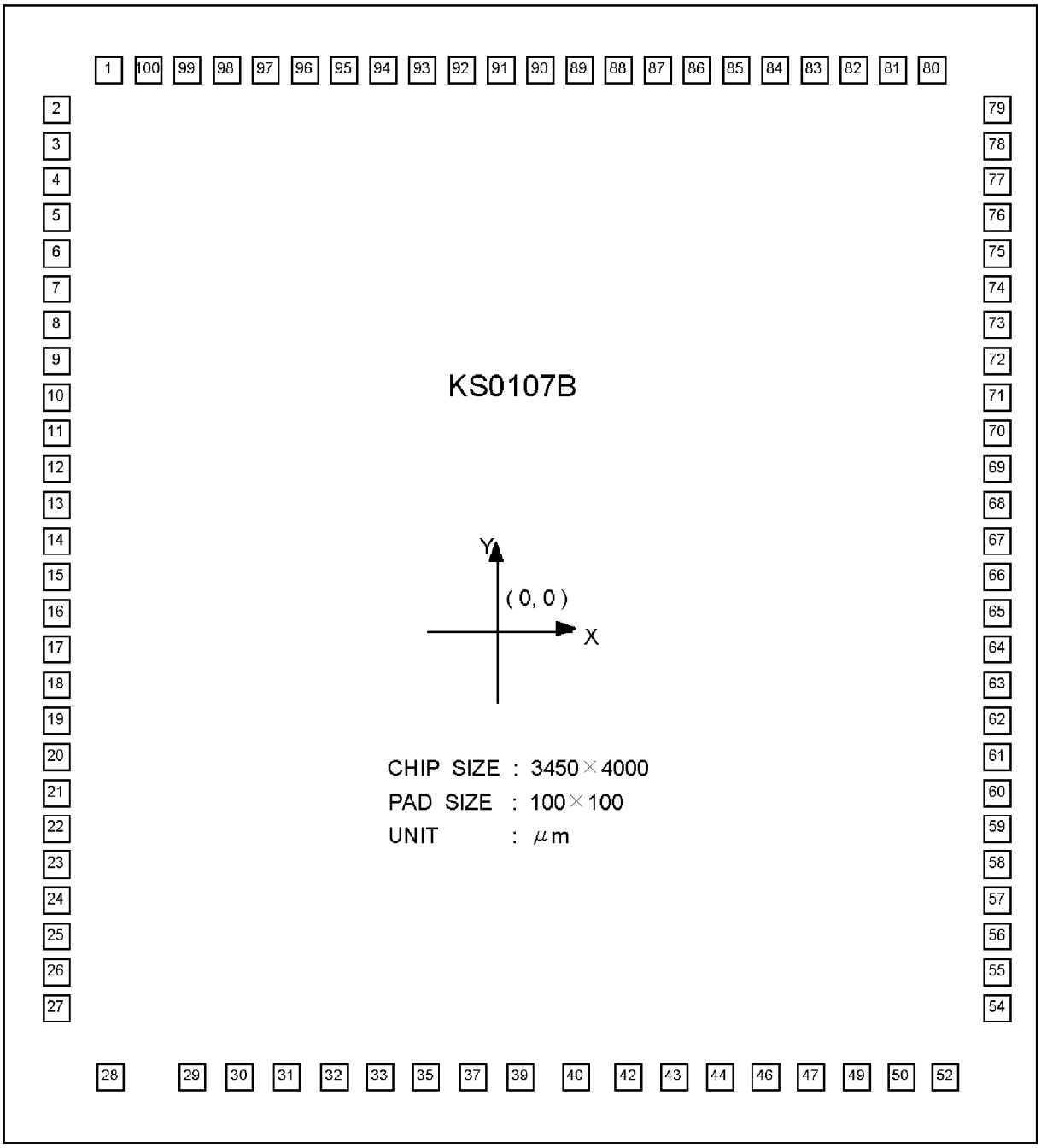
*When duty factor is 1/48, the value of R1 & R2 should satisfy.
R1/(4R1+R2)=1/8
R1=3K Ω , R2=12K Ω

APPLICATION CIRCUIT

-1/128 duty Segment drive(KS0108B) Interface circuit



PAD DIAGRAM



* There is mark of KS0107B on the center in chip

PAD LOCATION

UNIT (μ m)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	C22	-1314.5	1775.4	37	CR	-227.6	-1775	77	C46	1500.9	1380
2	C21	-1499.9	1630	39	SHL	-77.6	-1775	78	C45	1500.9	1505
3	C20	-1499.9	1505	40	VSS	113.8	-1775	79	C44	1500.9	1630
4	C19	-1499.9	1380	42	MS	308.7	-1775	80	C43	1310.5	1775.4
5	C18	-1499.9	1255	43	CLK2	458.7	-1775	81	C42	1185.5	1775.4
6	C17	-1499.9	1130	44	CLK1	608.7	-1775	82	C41	1060.5	1775.4
7	C16	-1499.9	1005	46	FRM	758.7	-1775	83	C40	935.5	1775.4
8	C15	-1499.9	880	47	M	908.7	-1775	84	C39	810.5	1775.4
9	C14	-1499.9	775	49	PCLK2	1058.7	-1775	85	C38	685.5	1775.4
10	C13	-1499.9	630	50	DIO2	1208.7	-1775	86	C37	560.5	1775.4
11	C12	-1499.9	505	52	CL2	1358.7	-1775	87	C36	435.5	1775.4
12	C11	-1499.9	380	54	V0R	1500.9	-1495	88	C35	310.5	1775.4
13	C10	-1499.9	255	55	V5R	1500.9	-1370	89	C34	185.5	1775.4
14	C9	-1499.9	130	56	V4R	1500.9	-1245	90	C33	60.5	1775.4
15	C8	-1499.9	5	57	V1R	1500.9	-1120	91	C32	-64.5	1775.4
16	C7	-1499.9	-120	58	VEE	1500.9	-995	92	C31	-189.5	1775.4
17	C6	-1499.9	-245	59	C64	1500.9	-870	93	C30	-314.5	1775.4
18	C5	-1499.9	-370	60	C63	1500.9	-745	94	C29	-439.5	1775.4
19	C4	-1499.9	-495	61	C62	1500.9	-620	95	C28	-564.5	1775.4
20	C3	-1499.9	-620	62	C61	1500.9	-495	96	C27	-689.5	1775.4
21	C2	-1499.9	-745	63	C60	1500.9	-370	97	C26	-814.5	1775.4
22	C1	-1499.9	-870	64	C59	1500.9	-245	98	C25	-939.5	1775.4
23	VEE	-1499.9	-995	65	C58	1500.9	-120	99	C24	-1064.5	1775.4
24	V1L	-1499.9	-1120	66	C57	1500.9	5	100	C23	-1189.5	1775.4
25	V4L	-1499.9	-1245	67	C56	1500.9	130				
26	V5L	-1499.9	-1370	68	C55	1500.9	255				
27	V0L	-1499.9	-1495	69	C54	1500.9	380				
28	VDD	-1345.6	-1775	70	C53	1500.9	505				
29	DIO1	-1127.6	-1775	71	C52	1500.9	630				
30	FS	-979.6	-1775	72	C51	1500.9	755				
31	DS1	-827.6	-1775	73	C50	1500.9	880				
32	DS2	-677.6	-1775	74	C49	1500.9	1005				
33	C	-527.6	-1775	75	C48	1500.9	1130				
35	R	-377.6	-1775	76	C47	1500.9	1255				

Dimensions in Milimeters