Specification

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
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Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	生效日期 Eff. Date
001	--	New Release	E07060011	07/25/2006
002	Page18	Figure error	E12060017	12/13/2006
	Page41	Command “Power Save” decode error		
	Page46	Add “Built-in Oscillator ON”		
	Page47	Figure23 change		
003	Page11	PS=“L”DB0 to DB5 must be fixed to either “H” or “L”	E01070012	01/17/2007
	Page12	I/O PIN ITO Resister Limitation		
004	--	Modify oscillator frequency range (17.6 ~ 26.4 KHz)	E04070025	04/30/2007
005	Page5,9,12,50,51	Change pin “VDD” to “VDD1” and “VDD2”	E09070008	09/27/2007
	Page5,9,12	Change pin “VSS” to “VSS1” and “VSS2”		
	Page 47	SGS Select→ADC Select CMS Select→SHL Select		
	Page 62	Add example of IST3020 ITO connection		
006	Page 45	Change Standby current 10uA to 30uA	E10070008	10/09/2007
	Page 52	Modify OTP write flow, add programming wait tome 1ms		
007	Page 9	Power VPP voltage 6.5 +/- 0.25	E10070012	10/16/2007
	Page 11	DB5~0 must be fix Vdd or Vss in serial mode		
	Page 18	Modify Figure.6 when SHL=1,COM direction reverse		
	Page 41,42	The data is written must be waiting for 100ms after power save completed		
	Page 43	Add new command “extern capacitor”		

		discharge”		
	Page 47	Modify the flow-chart of power save mode, insert wait time 100ms and discharge function		
	Page 34,42	Add note of re-write display ram data before display on or power save		

INTRODUCTION

The IST3020 is a single chip driver & controller LSI for graphic dot-matrix liquid crystal display systems. This chip can be connected directly to a microprocessor, accepts serial or 8-bit parallel display data from the microprocessor, stores the display data in an on-chip display data RAM of 65 x 256 bits and generates a liquid crystal display drive signal independent of the microprocessor. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. It contains 65 common driver circuits and 224 segment driver circuits, so that a single chip can drive a 65 x 224 dot display. And the capacity of the display can be increased through the use of master/slave multi-chip structures.
The chip is able to minimize power consumption because it performs display data RAM read / write operation with no external operation clock. In addition, because it contains power supply circuits necessary to drive liquid crystal, which is a display clock oscillator circuit, high performance voltage converter circuit, high-accuracy voltage regulator circuit, low power consumption voltage divider resistors and OP-Amp for liquid crystal driver power voltage, it is possible to make the lowest power consumption display system with the fewest components for high performance portable systems.

FEATURES

Display Driver Output Circuits

- 65 common outputs / 224 segment outputs

On-chip Display Data RAM

- Capacity : 65 x 256 = 16,640 bits
- RAM bit data “1”: a dot of display is illuminated.
- RAM bit data “0”: a dot of display is not illuminated.

Microprocessor Interface

- High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series
- Serial interface (only write operation) available

Various Function Set

- Display ON / OFF, set initial display line, set page address, set column address, read status, write / read display data, select segment driver output, reverse display ON / OFF, entire display ON / OFF, select LCD bias, set/reset modify-read, select common driver output, control display power circuit, select internal regulator resistor ratio for V0 voltage regulation, electronic volume, set static indicator state, power save, n-line reversal driver, built-in oscillator circuit ON / OFF.
- H/W and S/W reset available
- Static drive circuit equipped internally for indicators with 4 flashing modes

Built-in Analog Circuit

- On-chip oscillator circuit for display clock (external clock can also be used)
- High performance voltage converter (with booster ratios of x2, x3, and x4, where the step-up reference voltage can be used externally)
- High accuracy voltage regulator (temperature coefficient : -0.05% / ℃ or external input)
- Electronic contrast control function (64 steps)
- High performance voltage follower (V1 to V4 voltage divider resistors and OP-Amp for increasing drive capacity)

On-chip Display Data RAM

- Supply voltage (V_{DD}) : 2.4 to 3.6 V
- LCD driving voltage (V_{LCD} = V0 – V_{SS}) : 4.5 to 15.0 V

Low Power Consumption

- Operating power : 40µA typical. (condition : V_{DD} = 3V, x4 boosting (VCI is V_{DD}), V0 = 11V, internal power supply ON, display OFF and normal mode is selected)
- Standby power : 10µA maximum. (during power save[standby] mode)

Operating Temperatures

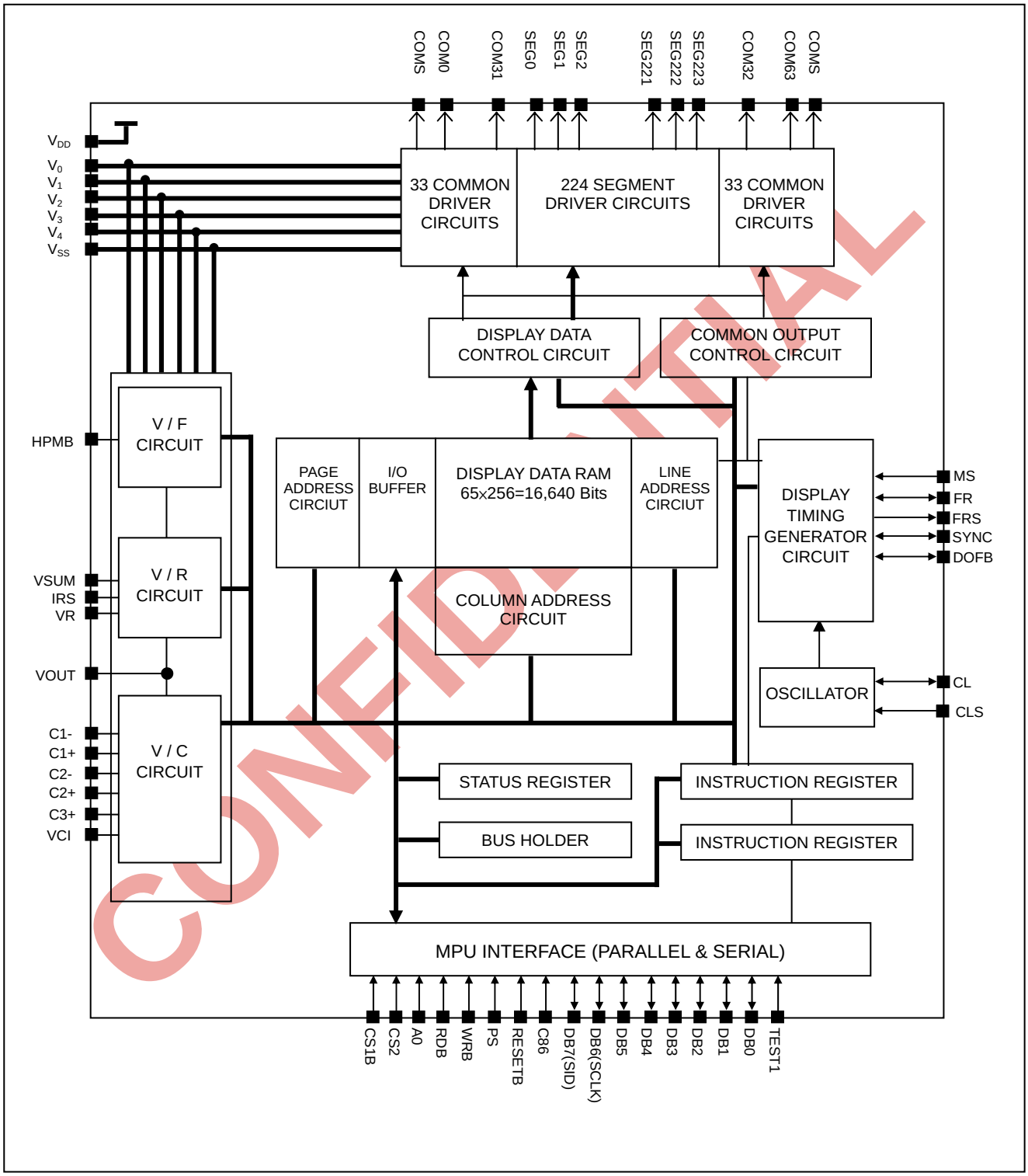
- Wide range of operating temperatures : -40 to 85℃

CMOS Process

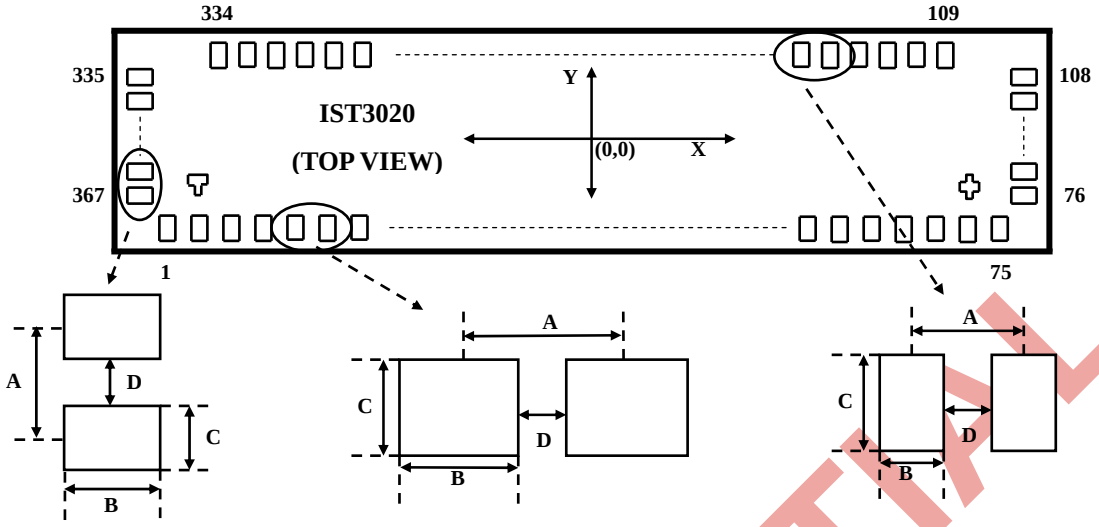
Package Type

- Gold bumped chip

BLOCK DIAGRAM



PAD CONFIGURATION



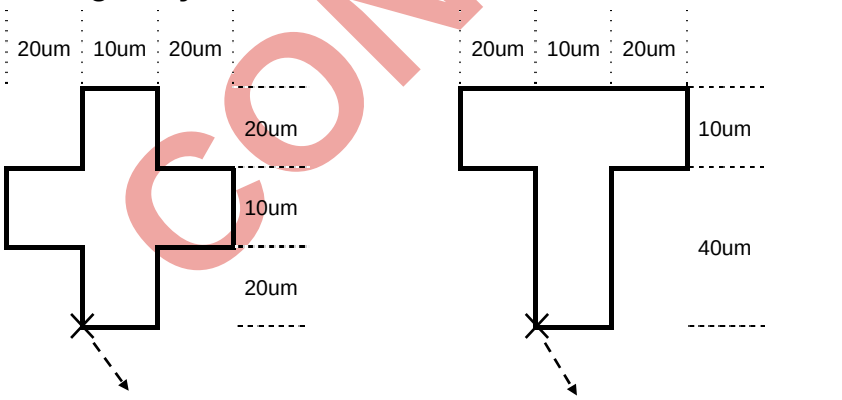
■ Chip Size

Item	X	Y	Unit
Chip size	7970	1098	um

■ Pad Dimensions

Item	Pad No.	A(Min.)	B	C	D(Min.)	Unit
Bumped Pad size	1 ~ 75	100	80	40	20	um
	76 ~ 108, 335 ~ 367	33	105	18	15	um
	109 ~ 334	33	18	105	15	um
Bumped pad height	All pad	15 (Typical)				um

■ Align Key Coordinate



X	Y	Unit
3402	-283	um

X	Y	Unit
-3386	-283	um

PAD CERTER COORDINATES

Unit : um

Pad No	Pad Name	X	Y	Note	Pad No	Pad Name	X	Y	Note
1	DUMMY	-3699.500	-472.425		51	FRS	1300.500	-472.425	
2	DUMMY	-3599.500	-472.425		52	FR	1400.500	-472.425	
3	DUMMY	-3499.500	-472.425		53	DOFB	1500.500	-472.425	
4	DUMMY	-3399.500	-472.425		54	V0	1600.500	-472.425	
5	VSS1	-3299.500	-472.425		55	V0	1700.500	-472.425	
6	VSS1	-3199.500	-472.425		56	V1	1800.500	-472.425	
7	VSS1	-3099.500	-472.425		57	V1	1900.500	-472.425	
8	VSS1	-2999.500	-472.425		58	V2	2000.500	-472.425	
9	VDD1	-2899.500	-472.425		59	V2	2100.500	-472.425	
10	VDD1	-2799.500	-472.425		60	V3	2200.500	-472.425	
11	VDD1	-2699.500	-472.425		61	V3	2300.500	-472.425	
12	VDD1	-2599.500	-472.425		62	V4	2400.500	-472.425	
13	CS2	-2499.500	-472.425		63	V4	2500.500	-472.425	
14	CL	-2399.500	-472.425		64	IRS	2600.500	-472.425	
15	CS1B	-2299.500	-472.425		65	VSUM	2700.500	-472.425	open
16	RESB	-2199.500	-472.425		66	VR	2800.500	-472.425	
17	A0	-2099.500	-472.425		67	DMYVDD	2900.500	-472.425	
18	WRB	-1999.500	-472.425		68	DMYVSS	3000.500	-472.425	
19	RDB	-1899.500	-472.425		69	CLS	3100.500	-472.425	
20	DB0	-1799.500	-472.425		70	C86	3200.500	-472.425	
21	DB1	-1699.500	-472.425		71	HPMB	3300.500	-472.425	
22	DB2	-1599.500	-472.425		72	DUMMY	3400.500	-472.425	
23	DB3	-1499.500	-472.425		73	DUMMY	3500.500	-472.425	
24	DB4	-1399.500	-472.425		74	DUMMY	3600.500	-472.425	
25	DB5	-1299.500	-472.425		75	DUMMY	3700.500	-472.425	
26	DB6	-1199.500	-472.425		76	COM31	3928.750	-528.450	
27	DB7	-1099.500	-472.425		77	COM30	3928.750	-495.450	
28	MS	-999.500	-472.425		78	COM29	3928.750	-462.450	
29	PS	-899.500	-472.425		79	COM28	3928.750	-429.450	
30	VDD2	-799.500	-472.425		80	COM27	3928.750	-396.450	
31	VDD2	-699.500	-472.425		81	COM26	3928.750	-363.450	
32	VDD2	-599.500	-472.425		82	COM25	3928.750	-330.450	
33	VDD2	-499.500	-472.425		83	COM24	3928.750	-297.450	
34	VCI	-399.500	-472.425		84	COM23	3928.750	-264.450	
35	VCI	-299.500	-472.425		85	COM22	3928.750	-231.450	
36	VSS2	-199.500	-472.425		86	COM21	3928.750	-198.450	
37	VSS2	-99.500	-472.425		87	COM20	3928.750	-165.450	
38	VSS2	0.500	-472.425		88	COM19	3928.750	-132.450	
39	VSS2	100.500	-472.425		89	COM18	3928.750	-99.450	
40	VOUT	200.500	-472.425		90	COM17	3928.750	-66.450	
41	VOUT	300.500	-472.425		91	COM16	3928.750	-33.450	
42	VPP	400.500	-472.425		92	COM15	3928.750	-0.450	
43	C3+	500.500	-472.425		93	COM14	3928.750	32.550	
44	C1-	600.500	-472.425		94	COM13	3928.750	65.550	
45	C1+	700.500	-472.425		95	COM12	3928.750	98.550	
46	C2+	800.500	-472.425		96	COM11	3928.750	131.550	
47	C2-	900.500	-472.425		97	COM10	3928.750	164.550	
48	TEST1	1000.500	-472.425	open	98	COM9	3928.750	197.550	
49	DMYVSS	1100.500	-472.425		99	COM8	3928.750	230.550	
50	SYNC	1200.500	-472.425		100	COM7	3928.750	263.550	

Pad No	Pad Name	X	Y	Note	Pad No	Pad Name	X	Y	Note
101	COM6	3928.750	296.550		151	SEG41	2397.900	492.500	
102	COM5	3928.750	329.550		152	SEG42	2341.100	492.500	
103	COM4	3928.750	362.550		153	SEG43	2308.100	492.500	
104	COM3	3928.750	395.550		154	SEG44	2275.100	492.500	
105	COM2	3928.750	428.550		155	SEG45	2242.100	492.500	
106	COM1	3928.750	461.550		156	SEG46	2209.100	492.500	
107	COM0	3928.750	494.550		157	SEG47	2176.100	492.500	
108	COMS	3928.750	527.550		158	SEG48	2143.100	492.500	
109	DUMMY	3807.700	492.500		159	SEG49	2110.100	492.500	
110	SEG0	3774.700	492.500		160	SEG50	2077.100	492.500	
111	SEG1	3741.700	492.500		161	SEG51	2044.100	492.500	
112	SEG2	3708.700	492.500		162	SEG52	2011.100	492.500	
113	SEG3	3675.700	492.500		163	SEG53	1978.100	492.500	
114	SEG4	3642.700	492.500		164	SEG54	1945.100	492.500	
115	SEG5	3609.700	492.500		165	SEG55	1912.100	492.500	
116	SEG6	3576.700	492.500		166	SEG56	1879.100	492.500	
117	SEG7	3543.700	492.500		167	SEG57	1846.100	492.500	
118	SEG8	3510.700	492.500		168	SEG58	1813.100	492.500	
119	SEG9	3477.700	492.500		169	SEG59	1780.100	492.500	
120	SEG10	3444.700	492.500		170	SEG60	1747.100	492.500	
121	SEG11	3411.700	492.500		171	SEG61	1714.100	492.500	
122	SEG12	3378.700	492.500		172	SEG62	1681.100	492.500	
123	SEG13	3345.700	492.500		173	SEG63	1648.100	492.500	
124	SEG14	3288.900	492.500		174	SEG64	1615.100	492.500	
125	SEG15	3255.900	492.500		175	SEG65	1582.100	492.500	
126	SEG16	3222.900	492.500		176	SEG66	1549.100	492.500	
127	SEG17	3189.900	492.500		177	SEG67	1516.100	492.500	
128	SEG18	3156.900	492.500		178	SEG68	1483.100	492.500	
129	SEG19	3123.900	492.500		179	SEG69	1450.100	492.500	
130	SEG20	3090.900	492.500		180	SEG70	1393.300	492.500	
131	SEG21	3057.900	492.500		181	SEG71	1360.300	492.500	
132	SEG22	3024.900	492.500		182	SEG72	1327.300	492.500	
133	SEG23	2991.900	492.500		183	SEG73	1294.300	492.500	
134	SEG24	2958.900	492.500		184	SEG74	1261.300	492.500	
135	SEG25	2925.900	492.500		185	SEG75	1228.300	492.500	
136	SEG26	2892.900	492.500		186	SEG76	1195.300	492.500	
137	SEG27	2859.900	492.500		187	SEG77	1162.300	492.500	
138	SEG28	2826.900	492.500		188	SEG78	1129.300	492.500	
139	SEG29	2793.900	492.500		189	SEG79	1096.300	492.500	
140	SEG30	2760.900	492.500		190	SEG80	1063.300	492.500	
141	SEG31	2727.900	492.500		191	SEG81	1030.300	492.500	
142	SEG32	2694.900	492.500		192	SEG82	997.300	492.500	
143	SEG33	2661.900	492.500		193	SEG83	964.300	492.500	
144	SEG34	2628.900	492.500		194	SEG84	931.300	492.500	
145	SEG35	2595.900	492.500		195	SEG85	898.300	492.500	
146	SEG36	2562.900	492.500		196	SEG86	865.300	492.500	
147	SEG37	2529.900	492.500		197	SEG87	832.300	492.500	
148	SEG38	2496.900	492.500		198	SEG88	799.300	492.500	
149	SEG39	2463.900	492.500		199	SEG89	766.300	492.500	
150	SEG40	2430.900	492.500		200	SEG90	733.300	492.500	

Pad No	Pad Name	X	Y	Note	Pad No	Pad Name	X	Y	Note
201	SEG91	700.300	492.500		251	SEG141	-997.300	492.500	
202	SEG92	667.300	492.500		252	SEG142	-1030.300	492.500	
203	SEG93	634.300	492.500		253	SEG143	-1063.300	492.500	
204	SEG94	601.300	492.500		254	SEG144	-1096.300	492.500	
205	SEG95	568.300	492.500		255	SEG145	-1129.300	492.500	
206	SEG96	535.300	492.500		256	SEG146	-1162.300	492.500	
207	SEG97	502.300	492.500		257	SEG147	-1195.300	492.500	
208	SEG98	445.500	492.500		258	SEG148	-1228.300	492.500	
209	SEG99	412.500	492.500		259	SEG149	-1261.300	492.500	
210	SEG100	379.500	492.500		260	SEG150	-1294.300	492.500	
211	SEG101	346.500	492.500		261	SEG151	-1327.300	492.500	
212	SEG102	313.500	492.500		262	SEG152	-1360.300	492.500	
213	SEG103	280.500	492.500		263	SEG153	-1393.300	492.500	
214	SEG104	247.500	492.500		264	SEG154	-1450.100	492.500	
215	SEG105	214.500	492.500		265	SEG155	-1483.100	492.500	
216	SEG106	181.500	492.500		266	SEG156	-1516.100	492.500	
217	SEG107	148.500	492.500		267	SEG157	-1549.100	492.500	
218	SEG108	115.500	492.500		268	SEG158	-1582.100	492.500	
219	SEG109	82.500	492.500		269	SEG159	-1615.100	492.500	
220	SEG110	49.500	492.500		270	SEG160	-1648.100	492.500	
221	SEG111	16.500	492.500		271	SEG161	-1681.100	492.500	
222	SEG112	-16.500	492.500		272	SEG162	-1714.100	492.500	
223	SEG113	-49.500	492.500		273	SEG163	-1747.100	492.500	
224	SEG114	-82.500	492.500		274	SEG164	-1780.100	492.500	
225	SEG115	-115.500	492.500		275	SEG165	-1813.100	492.500	
226	SEG116	-148.500	492.500		276	SEG166	-1846.100	492.500	
227	SEG117	-181.500	492.500		277	SEG167	-1879.100	492.500	
228	SEG118	-214.500	492.500		278	SEG168	-1912.100	492.500	
229	SEG119	-247.500	492.500		279	SEG169	-1945.100	492.500	
230	SEG120	-280.500	492.500		280	SEG170	-1978.100	492.500	
231	SEG121	-313.500	492.500		281	SEG171	-2011.100	492.500	
232	SEG122	-346.500	492.500		282	SEG172	-2044.100	492.500	
233	SEG123	-379.500	492.500		283	SEG173	-2077.100	492.500	
234	SEG124	-412.500	492.500		284	SEG174	-2110.100	492.500	
235	SEG125	-445.500	492.500		285	SEG175	-2143.100	492.500	
236	SEG126	-502.300	492.500		286	SEG176	-2176.100	492.500	
237	SEG127	-535.300	492.500		287	SEG177	-2209.100	492.500	
238	SEG128	-568.300	492.500		288	SEG178	-2242.100	492.500	
239	SEG129	-601.300	492.500		289	SEG179	-2275.100	492.500	
240	SEG130	-634.300	492.500		290	SEG180	-2308.100	492.500	
241	SEG131	-667.300	492.500		291	SEG181	-2341.100	492.500	
242	SEG132	-700.300	492.500		292	SEG182	-2397.900	492.500	
243	SEG133	-733.300	492.500		293	SEG183	-2430.900	492.500	
244	SEG134	-766.300	492.500		294	SEG184	-2463.900	492.500	
245	SEG135	-799.300	492.500		295	SEG185	-2496.900	492.500	
246	SEG136	-832.300	492.500		296	SEG186	-2529.900	492.500	
247	SEG137	-865.300	492.500		297	SEG187	-2562.900	492.500	
248	SEG138	-898.300	492.500		298	SEG188	-2595.900	492.500	
249	SEG139	-931.300	492.500		299	SEG189	-2628.900	492.500	
250	SEG140	-964.300	492.500		300	SEG190	-2661.900	492.500	

Pad No	Pad Name	X	Y	Note
301	SEG191	-2694.9	492.5	
302	SEG192	-2727.9	492.5	
303	SEG193	-2760.9	492.5	
304	SEG194	-2793.9	492.5	
305	SEG195	-2826.9	492.5	
306	SEG196	-2859.9	492.5	
307	SEG197	-2892.9	492.5	
308	SEG198	-2925.9	492.5	
309	SEG199	-2958.9	492.5	
310	SEG200	-2991.9	492.5	
311	SEG201	-3024.9	492.5	
312	SEG202	-3057.9	492.5	
313	SEG203	-3090.9	492.5	
314	SEG204	-3123.9	492.5	
315	SEG205	-3156.9	492.5	
316	SEG206	-3189.9	492.5	
317	SEG207	-3222.9	492.5	
318	SEG208	-3255.9	492.5	
319	SEG209	-3288.9	492.5	
320	SEG210	-3345.7	492.5	
321	SEG211	-3378.7	492.5	
322	SEG212	-3411.7	492.5	
323	SEG213	-3444.7	492.5	
324	SEG214	-3477.7	492.5	
325	SEG215	-3510.7	492.5	
326	SEG216	-3543.7	492.5	
327	SEG217	-3576.7	492.5	
328	SEG218	-3609.7	492.5	
329	SEG219	-3642.7	492.5	
330	SEG220	-3675.7	492.5	
331	SEG221	-3708.7	492.5	
332	SEG222	-3741.7	492.5	
333	SEG223	-3774.7	492.5	
334	DUMMY	-3807.7	492.5	

Pad No	Pad Name	X	Y	Note
335	COM32	-3928.75	527.55	
336	COM33	-3928.75	494.55	
337	COM34	-3928.75	461.55	
338	COM35	-3928.75	428.55	
339	COM36	-3928.75	395.55	
340	COM37	-3928.75	362.55	
341	COM38	-3928.75	329.55	
342	COM39	-3928.75	296.55	
343	COM40	-3928.75	263.55	
344	COM41	-3928.75	230.55	
345	COM42	-3928.75	197.55	
346	COM43	-3928.75	164.55	
347	COM44	-3928.75	131.55	
348	COM45	-3928.75	98.55	
349	COM46	-3928.75	65.55	
350	COM47	-3928.75	32.55	
351	COM48	-3928.75	-0.45	
352	COM49	-3928.75	-33.45	
353	COM50	-3928.75	-66.45	
354	COM51	-3928.75	-99.45	
355	COM52	-3928.75	-132.45	
356	COM53	-3928.75	-165.45	
357	COM54	-3928.75	-198.45	
358	COM55	-3928.75	-231.45	
359	COM56	-3928.75	-264.45	
360	COM57	-3928.75	-297.45	
361	COM58	-3928.75	-330.45	
362	COM59	-3928.75	-363.45	
363	COM60	-3928.75	-396.45	
364	COM61	-3928.75	-429.45	
365	COM62	-3928.75	-462.45	
366	COM63	-3928.75	-495.45	
367	COMS	-3928.75	-528.45	

PIN DESCRIPTION

POWER SUPPLY

Table 1. Power Supply Pins Description

Name	I/O	Description
VDD1 VDD2	Supply	Power supply
VSS1 VSS2	Supply	Ground
DMYVDD DMYVSS	Supply	Dummy power pin
VPP	Supply	VPP is the power pin of embedded OTP (One-Time Programming) non-volatile memory circuit. Only during OTP programming cycle VPP should connect to an external power source (about 6.5V ± 0.25V). On the other cases, just keep this pin open.
V0 V1 V2 V3 V4	I/O	LCD driver supply voltages The voltage determined by LCD pixel is impedance- converted by an operational amplifier for application. Voltages should have the following relationship; V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS When the internal power circuit is active, these voltages are generated as following as following table according to the state of LCD bias.

LCD bias	V1	V2	V3	V4
1/9 bias	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0
1/7 bias	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0

LCD DRIVER SUPPLY

Table 2. LCD Driver Supply Pins Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input / output pin Connect this pin to Vss through capacitor.
VR	I	V0 voltage adjustment pin It is valid only when internal voltage regulator resistors are not used (IRS = “L”).
VCI	I	This is the reference voltage for the voltage converter circuit for the LCD drive. Whether internal voltage converter use or not use, this pin should be fixed. The voltage should have the following range : 2.4V ≤ VCI ≤ 3.6V
VSUM	I/O	Temperature coefficient adjustment pin Keep open.

SYSTEM CONTROL

Table 3. System Control Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MS</td><td>I</td><td>Master / slave mode select input
Master makes some signals for display, and slave gets them. This is for display synchronization.
- MS = “H” : master mode
- MS = “L” : slave mode
The following table depends on the MS status.
<table>
<tr><th>MS</th><th>CLS</th><th>OSC circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>SYNC</th><th>FRS</th><th>DOF</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>-</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin
- CLS = “H” : enable
- CLS = “L” : disable (external display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin
When the IST3020 is used in master / slave mode (multi-chip), the CL pins must be connected each other.</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC Signal input / output pin
When the IST3020 is used in master / slave mode (multi-chip), the FR pins must be connected each other.
- MS = “H” : output
- MS = “L” : input</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>LCD synchronizing current signal input / output pin
When the IST3020 is used in master / slave mode (multi-chip), the SYNC pins must be connected each other.</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin
This pin is used together with the SYNC pin.</td></tr>
<tr><td>DOFB</td><td>I/O</td><td>LCD display blanking control input / output
When the IST3020 is used in master / slave mode (multi-chip), the DOFB pins must be connected each other.
- DOFB = “H” : output
- DOFB = “L” : input</td></tr>
<tr><td>IRS</td><td>I</td><td>Internal resistor select pin
This pin selects the resistors for adjusting V0 voltage level and is valid only in master operation.
- IRS = “H” : use the internal resistors
- IRS = “L” : use the external resistors
V0 voltage is controlled by VR pin and external resistive divider.</td></tr>
<tr><td>HPMB</td><td>I</td><td>Power supply control pin of the power supply circuit for LCD driver
- HPMB = “H” : Normal mode
- HPMB = “L” : High power supply mode
Valid only at master operation. The pin fixed to HIGH or LOW at slave operation.</td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 4. Microprocessor Interface Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin
When RESB is “L”, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / serial data input select input
<table>
<tr><td>PS</td><td>Interface mode</td><td>Chip select</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>A0</td><td>DB0 to DB7</td><td>RDB
WRB</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>A0</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
</table>
*NOTE : In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5, RDB and WRB must be fixed to either “H” or “L”.</td></tr>
<tr><td>C86</td><td>I</td><td>Microprocessor Interface Select input pin in parallel mode
- C86 = “H” : 6800-series MPU interface
- C86 = “L” : 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. when chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
- A0 = “H” : DB0 to DB7 are display data
- A0 = “L” : DB0 to DB7 are control data</td></tr>
<tr><td>WRB
(RW)</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><td>C86</td><td>MPU Type</td><td>RW_WRB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
- RW = “H” : read
- RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>WRB</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the WRB signal.</td></tr>
</table></td></tr>
<tr><td>RDB
(E)</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><td>C86</td><td>MPU Type</td><td>E_RDB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
- RW = “H” : When E is “H”, DB0 to DB7 are in an output status.
- RW = “L” : The data on DB0 to DB7 are latched at the falling edge the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>RDB</td><td>Read enable clock input pin
When / RDB is “L”, DB0 to DB7 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = “L”);
- DB0 to DB5 : Keep V_{DD} or V_{SS}
- DB6 : serial input clock (SCLK)
- DB7 : serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>TEST1</td><td>I/O</td><td>These are pins for IC chip testing.
They are set to Open.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 5. LCD Driver Outputs Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="8">SEG0
to
SEG223</td><td rowspan="8">O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td><table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
</table></td></tr>
<tr><td></td></tr>
<tr><td rowspan="8">COM0
to
COM63</td><td rowspan="8">O</td><td>LCD common driver outputs
The internal scanning data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td><table>
<tr><td>Scan data</td><td>M</td><td>Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td>Vss</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td></tr>
</table></td></tr>
<tr><td></td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, these pins should be left Open.
In multi-chip (master / slave) mode, all COMS pin on both master and slave units are the same signal.</td></tr>
</table>

IST3020 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
VSS1,VSS2	< 30Ω
VDD1,VDD2,VCI	< 50Ω
VOUT,V0 ~ V4,C1+/- ~ C3+	< 100Ω
CS1B,WRB,RDB,A0,DB0 ~ DB7,PS,C86	< 1KΩ
RESB	< 10KΩ

NOTE : **DUMMY – These pins should be opened (floated).**

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The IST3020 can inter face with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, A0, RDB, and WRB inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

IST3020 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 6.

Table 6. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	C86	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*× : Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C86 as shown in table 7. The type of data transfer is determined by signals at A0, RDB(E) and WRB(RW) as shown in Table 8.

Table 7. Microprocessor Selection for Parallel Interface

C86	CS1B	CS2	A0	RDB	WRB	DB0 to DB7	MPU bus
H	CS1B	CS2	A0	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	A0	RDB	WRB	DB0 to DB7	8080-series

Table 8. Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E	RW	RDB	WRB	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (PS = "L")

When the IST3020 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when A0 is high and control data when A0 is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

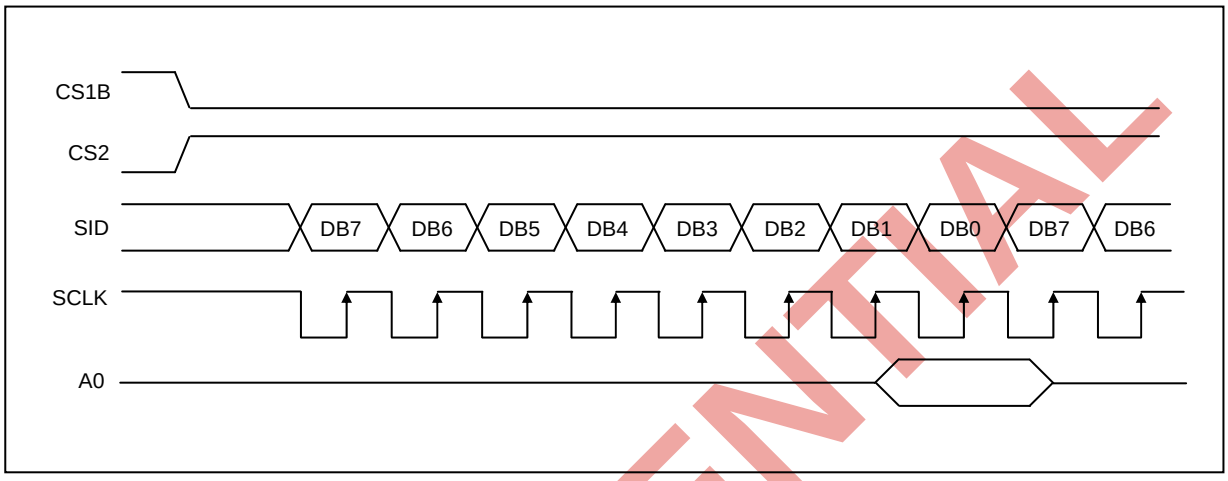


Figure 1. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the IST3020 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The IST3020 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 2. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 3. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

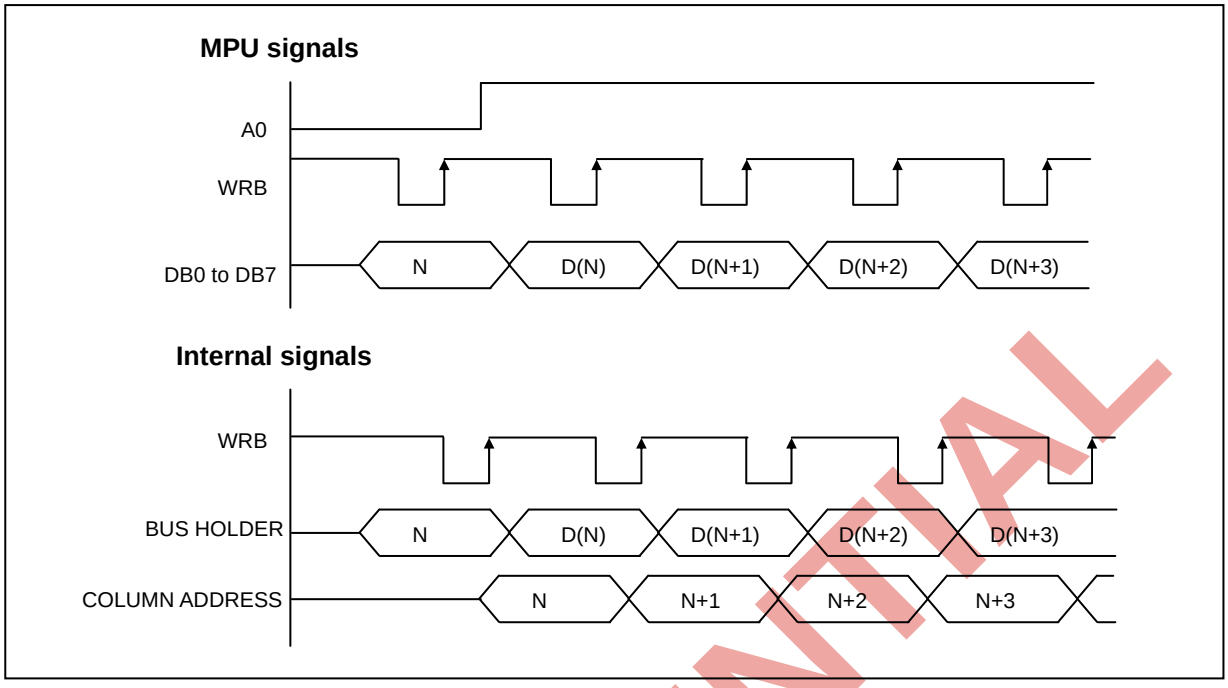


Figure 2. Write Timing

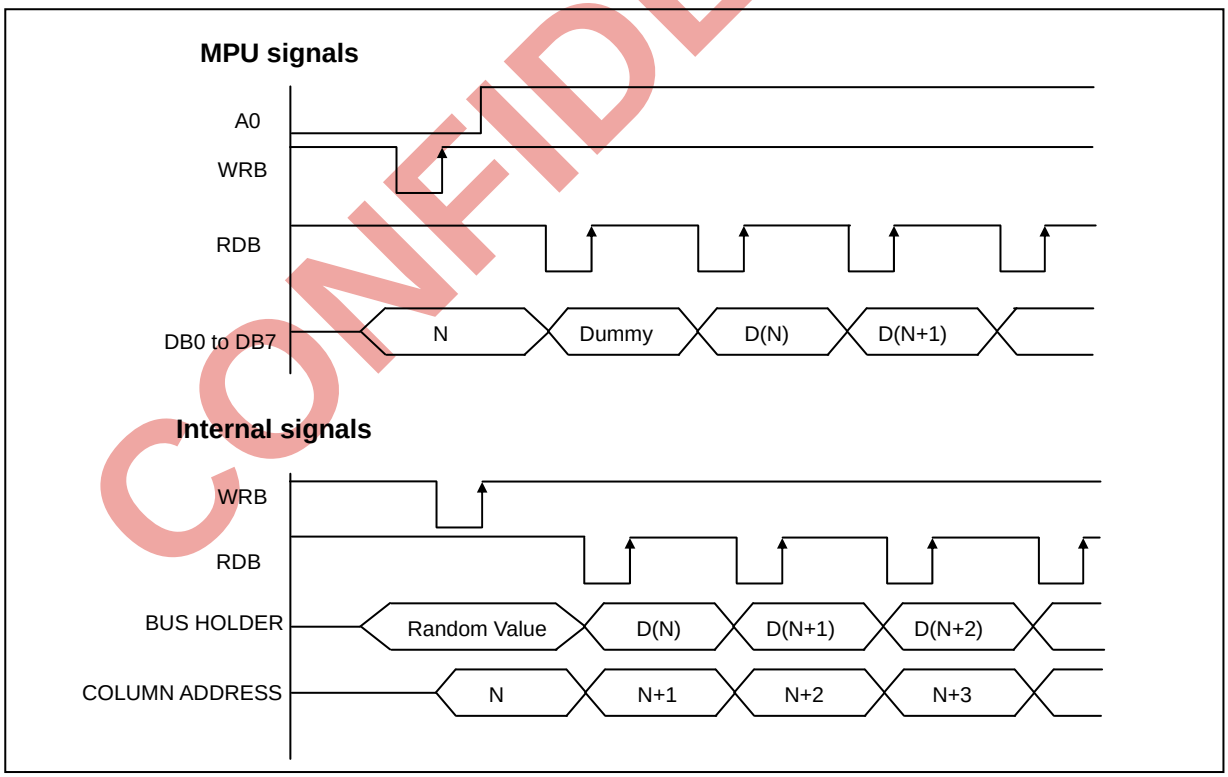


Figure 3. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 224-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 4. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

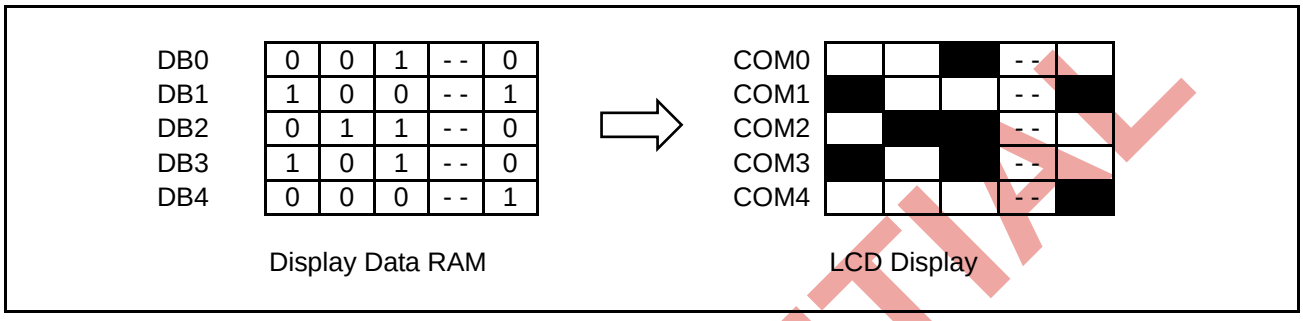


Figure 4. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to DISPLAY-DATA-RAM shown in figure 6. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 8(DB3 is “H”, but DB2, DB1 and DB0 are “L”) is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 6. It incorporates 6-bit line address register changed by only the initial display line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 224-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column Address circuit has 8-bit preset counter that provides column address to the Display Data RAM as shown in figure 6. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. Increment of the column address is stopped by FFH. When display data is accessed continuously, the column address continues to specify the FFH after access of the FFH. It should be noted that the column address FFH display data is accessed repeatedly. The column address and page address are independent of each other. Therefore, when shifting from the column of page 0 to column of page 1, for example, it is necessary to specify each of the page address and column address again.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following figure 5.

SEG output		SEG 0	SEG 1	SEG 2	SEG 3	… …	SEG 220	SEG 221	SEG 222	SEG 223
Column Address [Y7:Y0]	ADC = 0	00H	01H	02H	03H	… …	DCH	DDH	DEH	DFH
	ADC = 1	FFH	FEH	FDH	FCH	… …	23H	22H	21H	20H

Figure 5. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

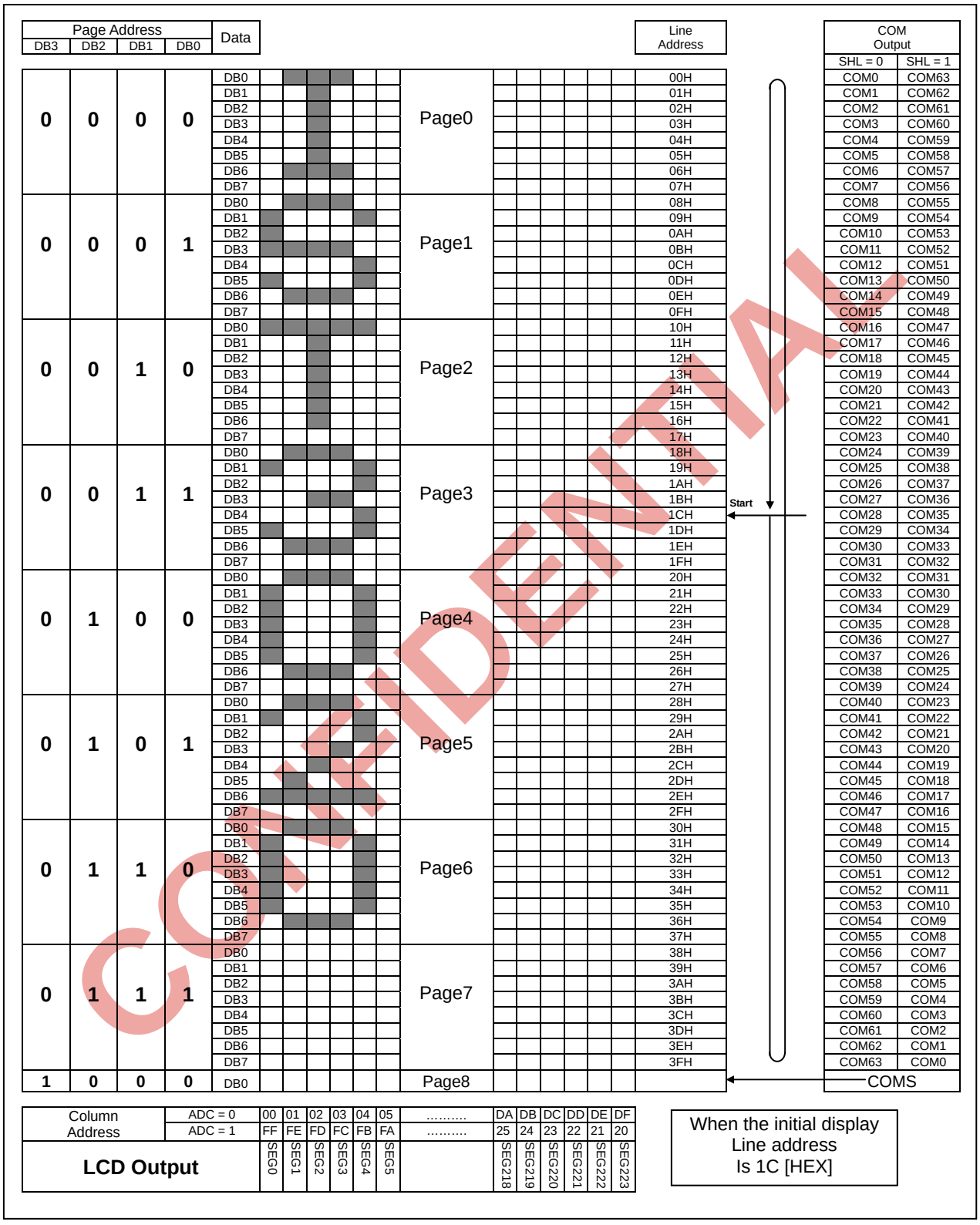


Figure 6. Display Data RAM Map

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit. The oscillator circuit is only enabled when MS = “H” and CLS = “H”. When on-chip oscillator is not used, CLS pin must be “L” condition. In this time, external clock must be input from CL pin.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL generated by oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 224-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The LCD AC signal, FR is generated from the display clock. 2-frame AC driver waveforms with internal timing signal are shown in figure 7. It can generate n-line reversal alternating drive waveforms by setting data (n-1) to the n-line reversal drive register, the timing signal are shown in figure 8.

In a multiple chip configuration, the slave chip requires the M, CL and DISP signals from the master. Table 9 shows the FR, SYNC, CL, and DOFB status.

Table 9. Master and Slave Timing Signal Status

Operation mode	Oscillator	SYNC	FR	CL	DOFB
Master	ON (internal clock used)	Output	Output	Output	Output
	OFF (external clock used)	Output	Output	Input	Output
Slave	-	Input	Input	Input	Input

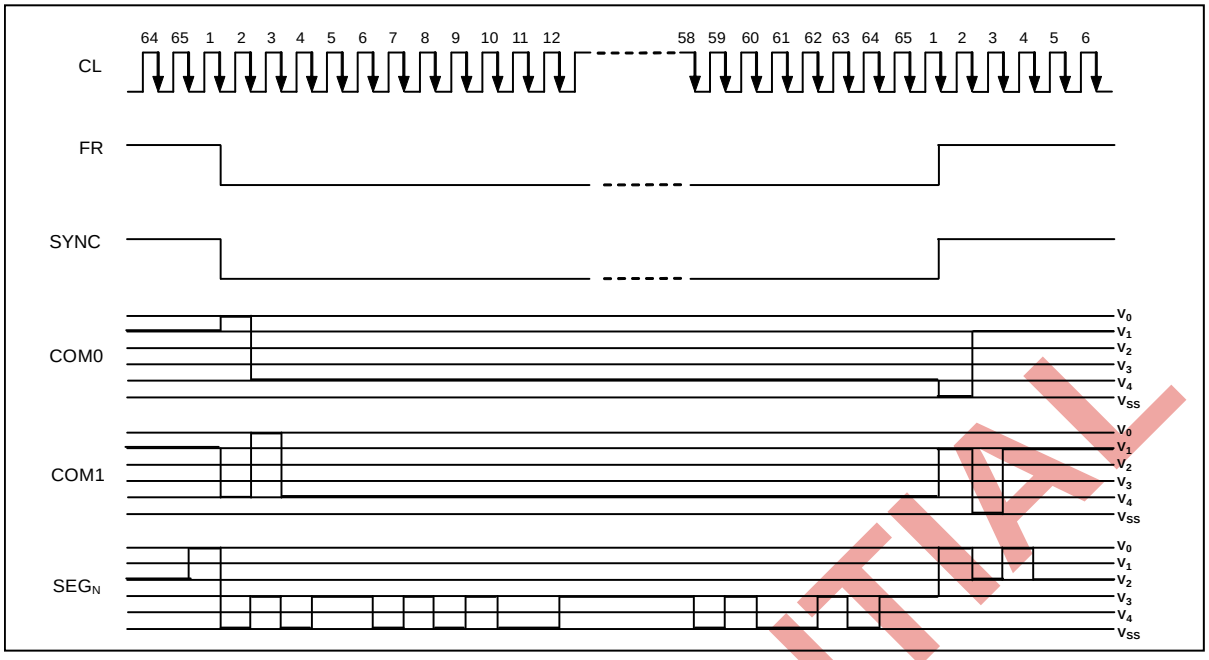


Figure 7. 2-frame Alternating Driving Waveform

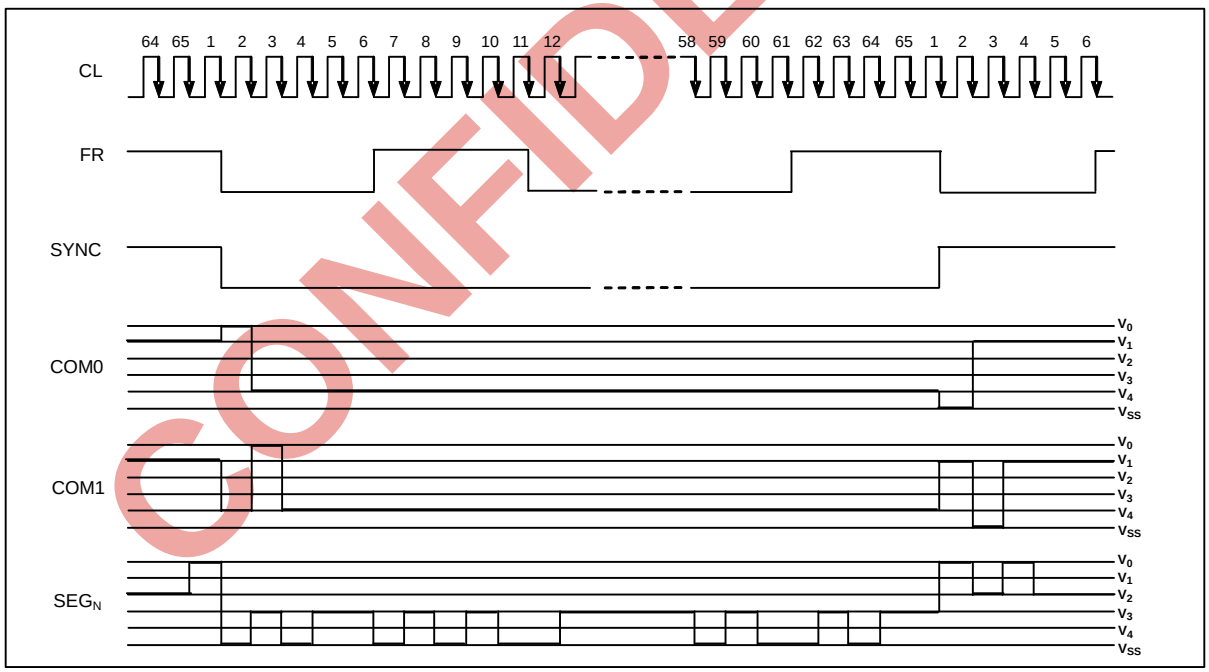


Figure 8. n-line Reversal Alternating Driving Waveform
(Example of n = 5, when the line reversal register is set to 4)

LCD DRIVER CIRCUIT

This driver circuit is configured by 66-channel (including 2 COMS channels) common driver and 224-channel segment driver. This LCD panel driver voltage Depends on the combination of display data and FR signal.

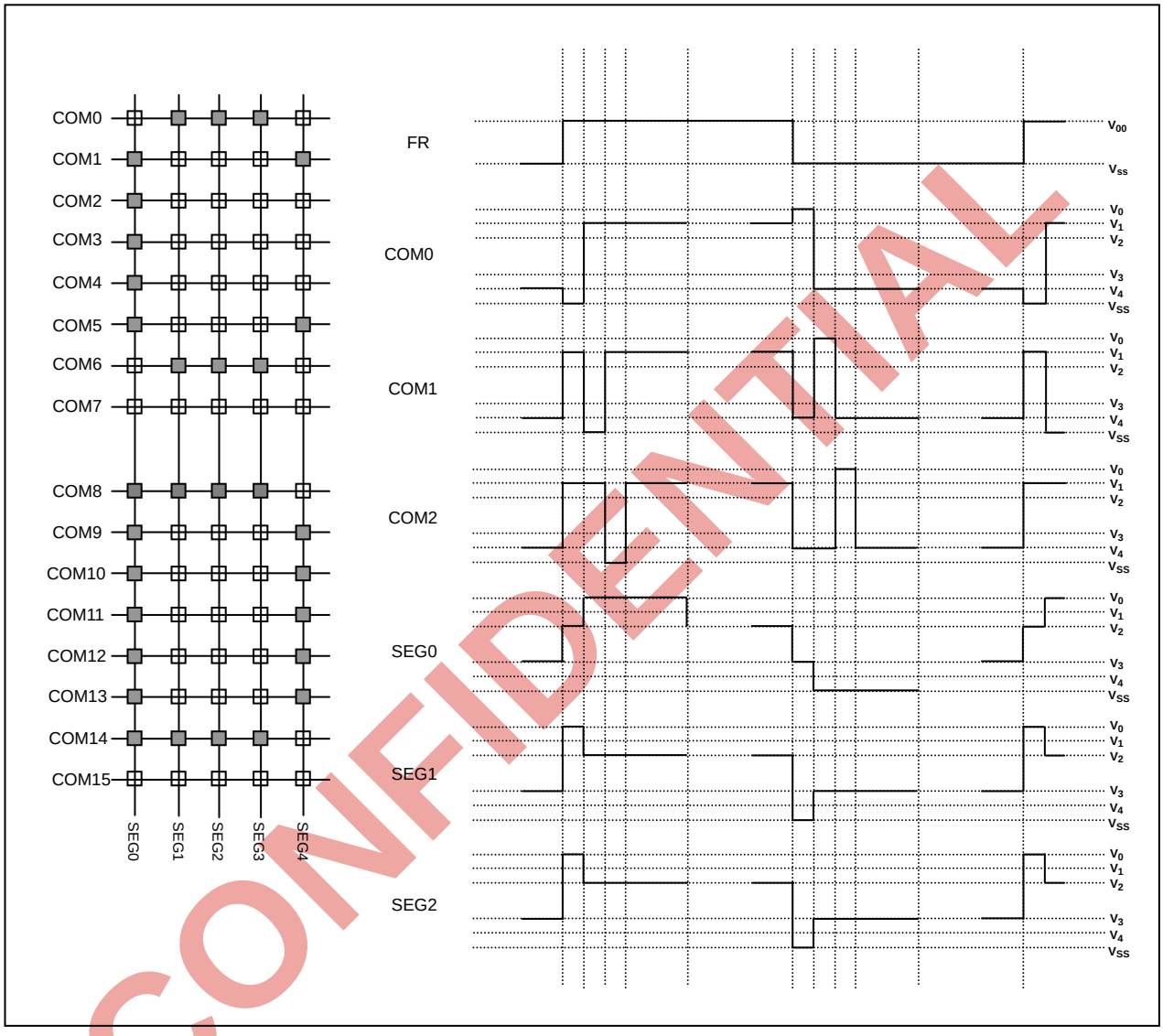


Figure 9. Segment and Common Timing

POWRE SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to “Instruction Description”. Table 10 shows the referenced combinations in using Power Supply circuits.

Table 10. Recommended Power Supply Combinations

User setup	Power Control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	111	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	011	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	001	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	000	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and Vss to 2, 3 or 4 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7 µF]

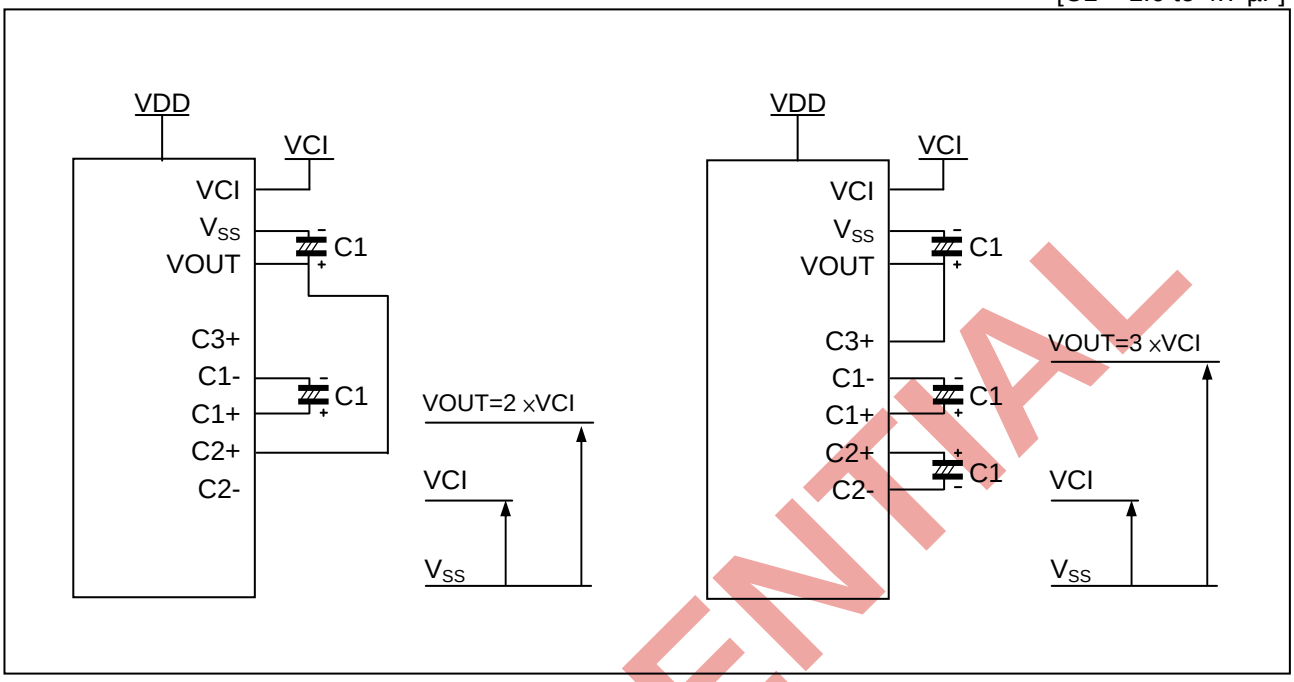


Figure 10. Two Times Boosting Circuit **Figure 11. Three Timing Boosting Circuit**

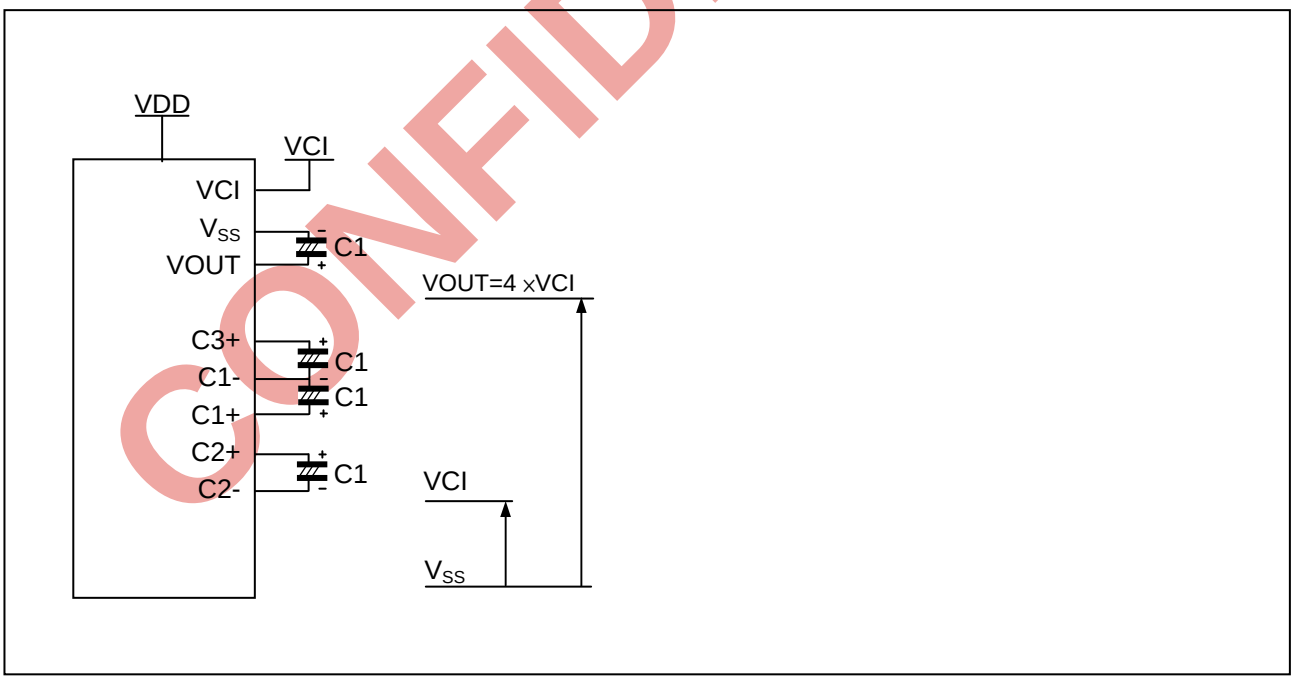


Figure 12. Four Times Boosting Circuit

*The VCI voltage range must be set so that the VOUT voltage does not exceed the absolute maximum rated value

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating Voltage of operational-amplifier circuits shown in figure 13, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally ty IRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, “Set Reference Voltage Register”, within the range 0 to 63. V_{REF} voltage at Ta=25℃ is shown in table 11-1.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \ [V] \text{ ---- (Eq. 1)}$$

$$Vev = \left(1 - \frac{(63-\alpha)}{162}\right) \times V_{REF} \ [V] \text{ ---- (Eq. 2)}$$

Table 11-1. Vref Voltage at Ta = 25℃

Device	Temp. coefficient	V_{REF} [V]
Internal power supply	-0.05%/℃	2.1

Table 11-2. Electronic Contrast Control Register (64 Steps)

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage Parameter (α)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62		
1	1	1	1	1	1	63	Maximum	High

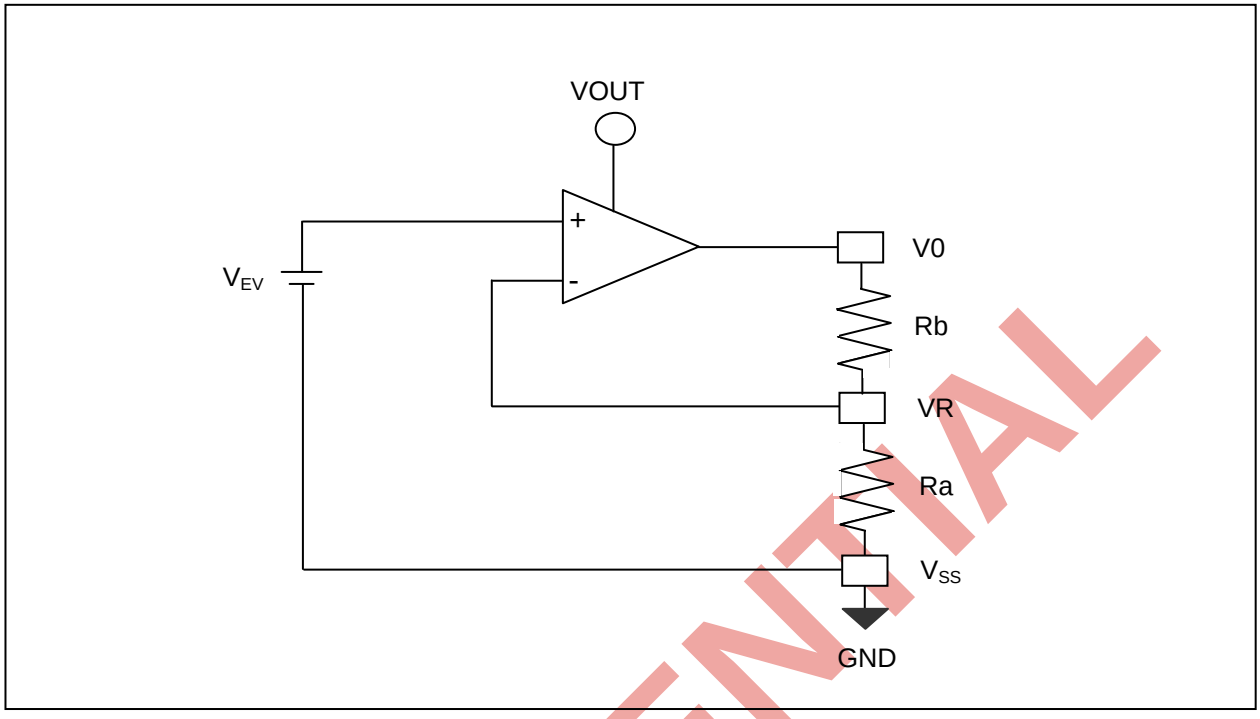


Figure 13. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb. (IRS = "H")

When IRS pin is "H", resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 12. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1+(Rb / Ra)	4.5	5	5.5	6	6.5	7	7.5	8

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25℃.

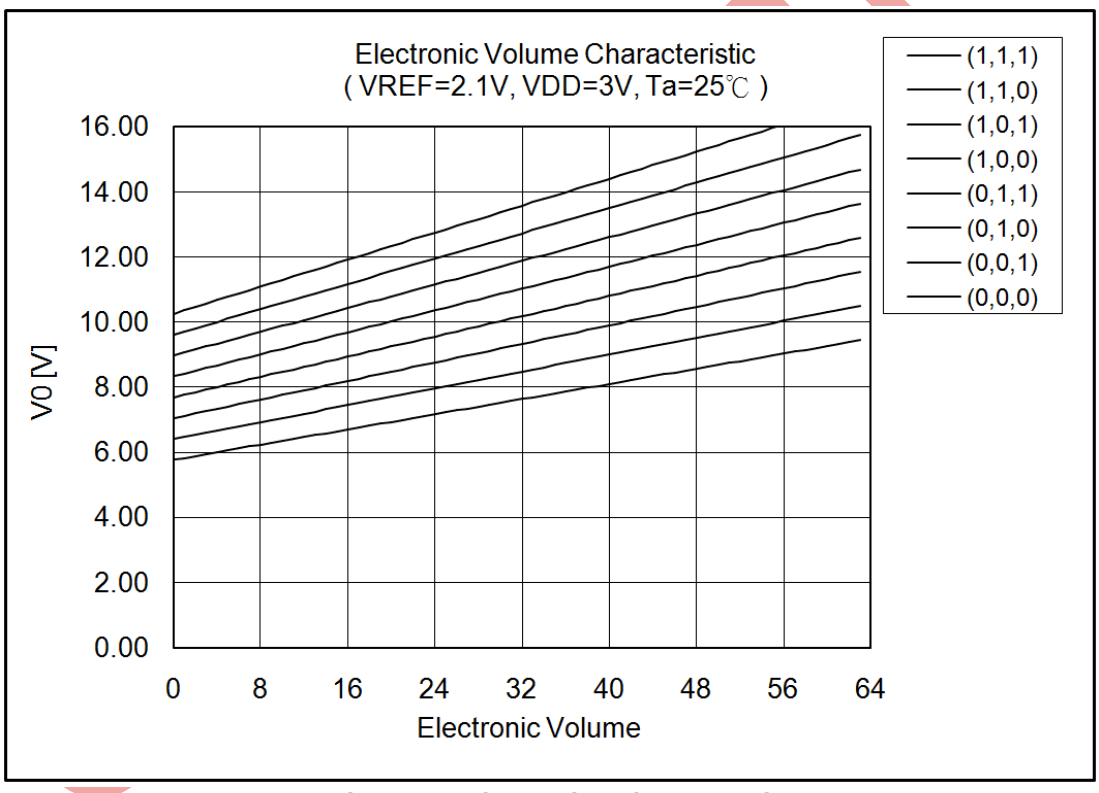


Figure 14. Electronic Volume Level

In Case of Using External Resistors, Ra and Rb. (IRS = "L")
When IRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and Vss, and Rb between V0 and VR.

Example : For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 µA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ---- (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(63-32)}{162}\right) \times 2.1 \cong 1.7 \quad [V] \text{ ---- (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1\ [\mu A] \text{ ---- (Eq. 5)}$$

From equations Eq. 3, 4 and 5
Ra 1.7 [MΩ]
Rb 8.3 [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 13. V0 Depending on Electronic Volume Level

	Electronic volume level				
	0	**……**	**32**	**……**	**63**
V0	7.55	……	10.00	……	12.35

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the Voltage Follower for increasing are capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 14. The Relationship between V1 to V4 Level and Duty Ratio

LCD bias	V1	V2	V3	V4
1/7	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0

REFERENCE CIRCUIT EXAMPLES

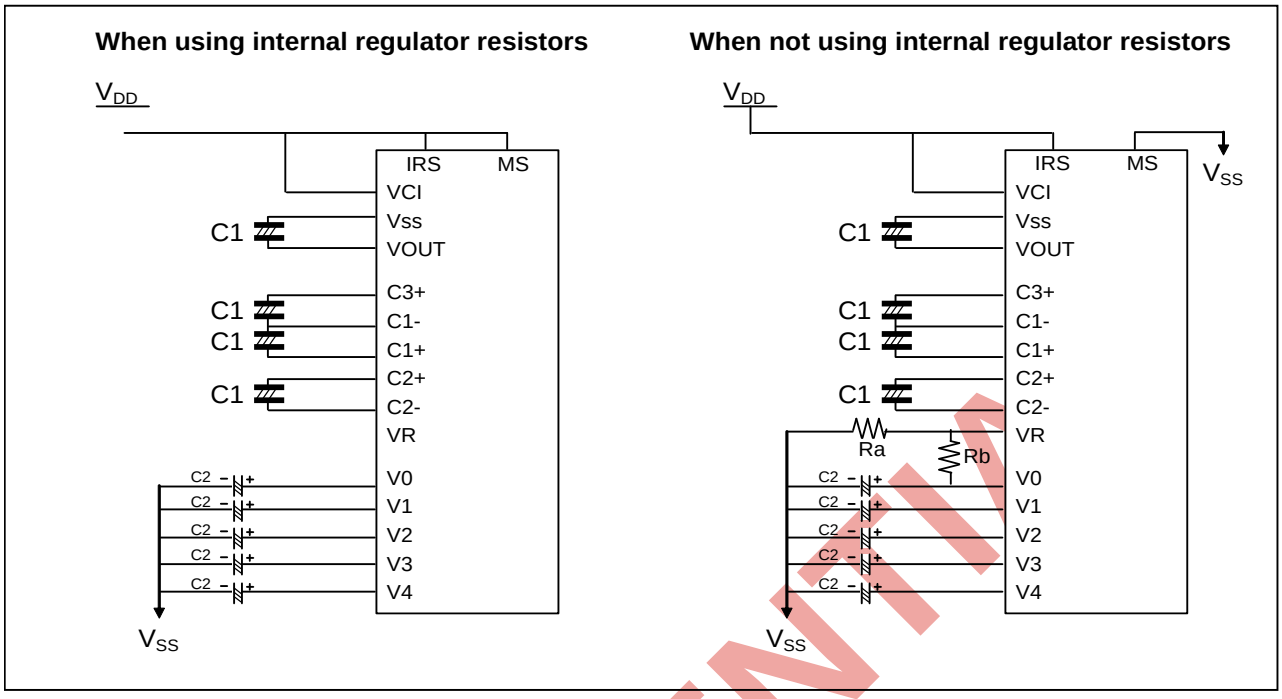


Figure 15. When Using all Internal LCD Power Circuits (VCI = VDD, 4-time V/C : ON, V/R : ON, V/F : ON)

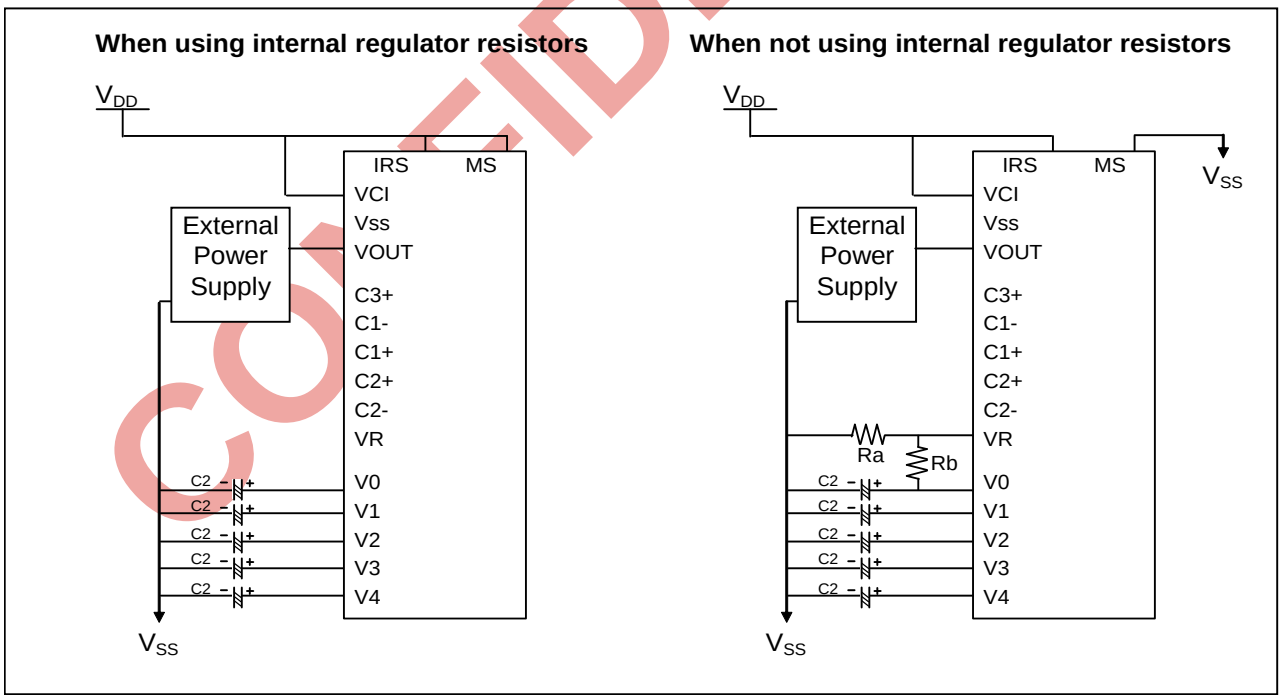
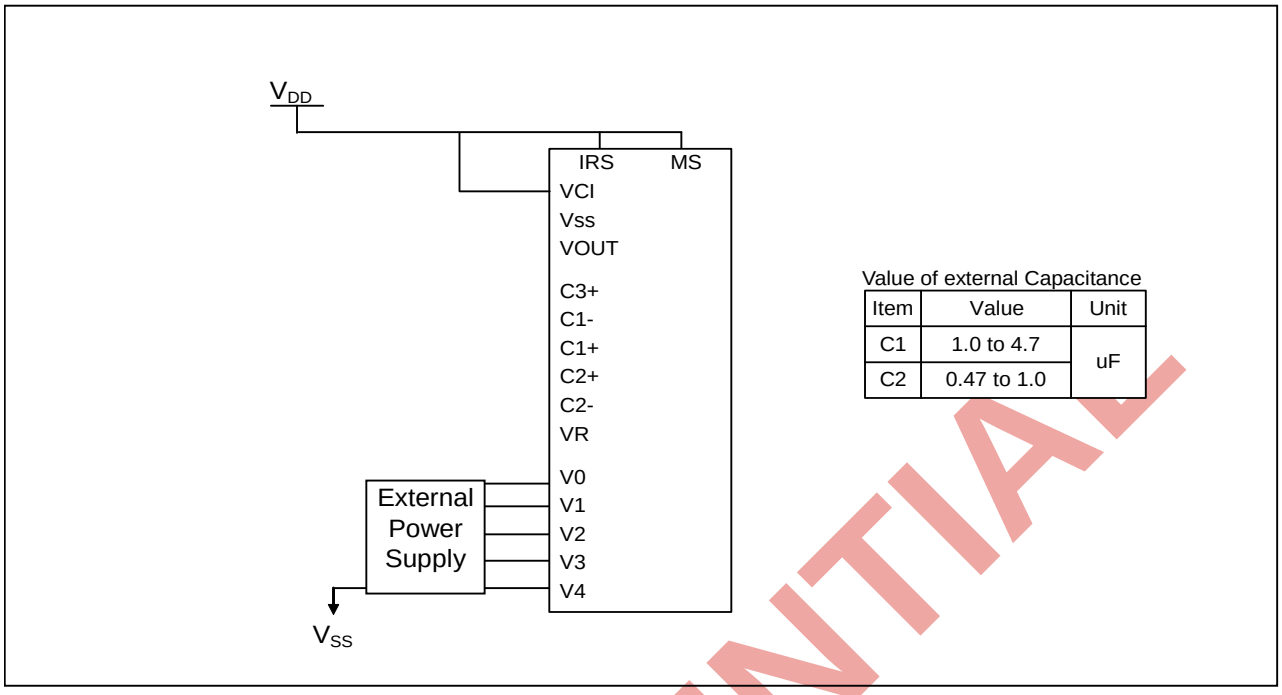


Figure 16. When Using some Internal LCD Power Circuits (VCI = VDD, V/C : OFF, V/R : ON, V/F : ON)



Value of external Capacitance

Item	Value	Unit
C1	1.0 to 4.7	uF
C2	0.47 to 1.0	

Figure 17. When Not Using any Internal LCD Power Circuits (VCI = VDD, V/C : OFF, V/R : OFF, V/F : OFF)

*C1 and C2 are determined by the size of the LCD being driven.
Select a value that will stabilize the liquid crystal drive voltage.

RESET CIRCUIT

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L”, following procedure is occurred.

Display ON / OFF : OFF
Entire display ON / OFF : OFF (normal)
ADC select : OFF (normal)
Reverse display ON / OFF : OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
Serial interface internal register data clear
On-chip oscillator OFF
Power save release
Read-modify-write : OFF
SHL select : OFF (normal)
Static indicator mode : OFF
Static indicator register : (S1, S0) = (0, 0)
Display start line : 0 (first)
Column address : 0
Page address : 0
Regulator resistor select register : (R2, R1, R0) = (0, 0, 0)
LCD power supply bias ratio : 1/9 bias
Reference voltage control register : (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release
n-Line alternating current reversal drive reset
n-Line alternating current reversal register : (NL3, NL2, NL1, NL0) = (0, 0 ,0, 0)
OTP program control : (OTPADJ,OTPPON) = (1, 0)
External capacitor discharge function enable

When RESET instruction is issued, following procedure is occurred.

Read-modify-write : OFF
Static indicator mode : OFF
Static indicator register : (S1, S0) = (0, 0)
SHL select : OFF (normal)
Display start line : 0 (first)
Column address : 0
Rage address : 0
Regulator resistor select register : (R2, R1, R0) = (0, 0, 0)
Reference voltage control register : (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

While RESETB is “L” or Reset instruction is executed, no instruction except read status could be accepted. Reset status appears at DB4 becomes “L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 15. Instruction Table

× : Don't care

INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn on/off LCD panel When DON = 0 : display OFF When DON = 1 : display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADC	ON/OFF	RESETB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into DDRAM
Read display data	1	1	Read data								Read data from DDRAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0 : normal direction (SEG0 → SEG223) when ADC = 1 : reverse direction (SEG223 → SEG0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0 : normal display When REV = 1 : reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal / entire display ON When EON = 0 : normal display When EON = 1 : entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0 : normal direction (COM0 → COM63) When SHL = 1 : reverse direction (COM63 → COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	0	0	1	0	1	0	1	0	0	SAV	Select power save mode When SAV = 0 : Stand-by When SAV = 1 : Sleep
Power save reset	0	0	1	1	1	0	0	0	0	1	Reset power save
Set n-Line reversal drive register	0	0	0	0	1	1	NL3	NL2	NL1	NL0	Set the number of line reversal drive line

n-Line reversal drive reset	0	0	1	1	1	0	0	1	0	0	Reset the line reversal drive
Built-in oscillator ON	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator circuit
External capacitor discharge	0	0	0	1	1	1	0	DISC			DISC = 000 (enable) DISC = 111 (disable)
NOP	0	0	1	1	1	0	0	0	1	1	Non-Operation command
Test	0	0	1	1	1	1	×	×	×	×	Don't use this instruction
Set OTP program	0	0	1	0	0	1	0	0	0	0	Set OTP program mode
OTP program control	0	0	OTPADJ	OTPPON	x	x	x	x	x	x	OTP control option OTPADJ = 1:OTP use OTPADJ = 0:OTP ignore OTPPON =1:OTP program enable OTPPON = 0:OTP program disable
Set contrast offset mode (1)	0	0	1	0	0	1	0	0	0	1	Set contrast offset mode (1)
Set contrast offset (1)	0	0	×	×	CTA5	CTA4	CTA3	CTA2	CTA1	CTA0	Set contrast offset register (1)
Set contrast offset mode (2)	0	0	1	0	0	1	0	0	1	0	Set contrast offset mode (2)
Set contrast offset (2)	0	0	×	×	×	CTB4	CTB3	CTB2	CTB1	CTB0	Set contrast offset register (2)
Set contrast offset mode (3)	0	0	1	0	0	1	0	0	1	1	Set contrast offset mode (3)
Set contrast offset (3)	0	0	×	×	×	CTC4	CTC3	CTC2	CTC1	CTC0	Set contrast offset register (3)

Display ON / OFF

Tums the Display ON or OFF

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1 : display ON
DON = 0 : display OFF

※ To avoid display data loss in display off , please re-write display ram data before display on execute.

Initial Display Line

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM63 when SHL = H) of LCD panel.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set Column Address LSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Read Status

Indicates the internal status of the IST3020

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	RESETB	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0 : chip is active, 1 : chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver 0 : reverse direction (SEG223 to SEG0), 1 : normal direction (SEG0 to SEG223)
ON/OFF	Indicates display ON/OFF status 0 : display ON, 1 : display OFF
RESETB	Indicates the initialization is in progress by RESETB signal 0 : chip is active, 1 : chip is being reset

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

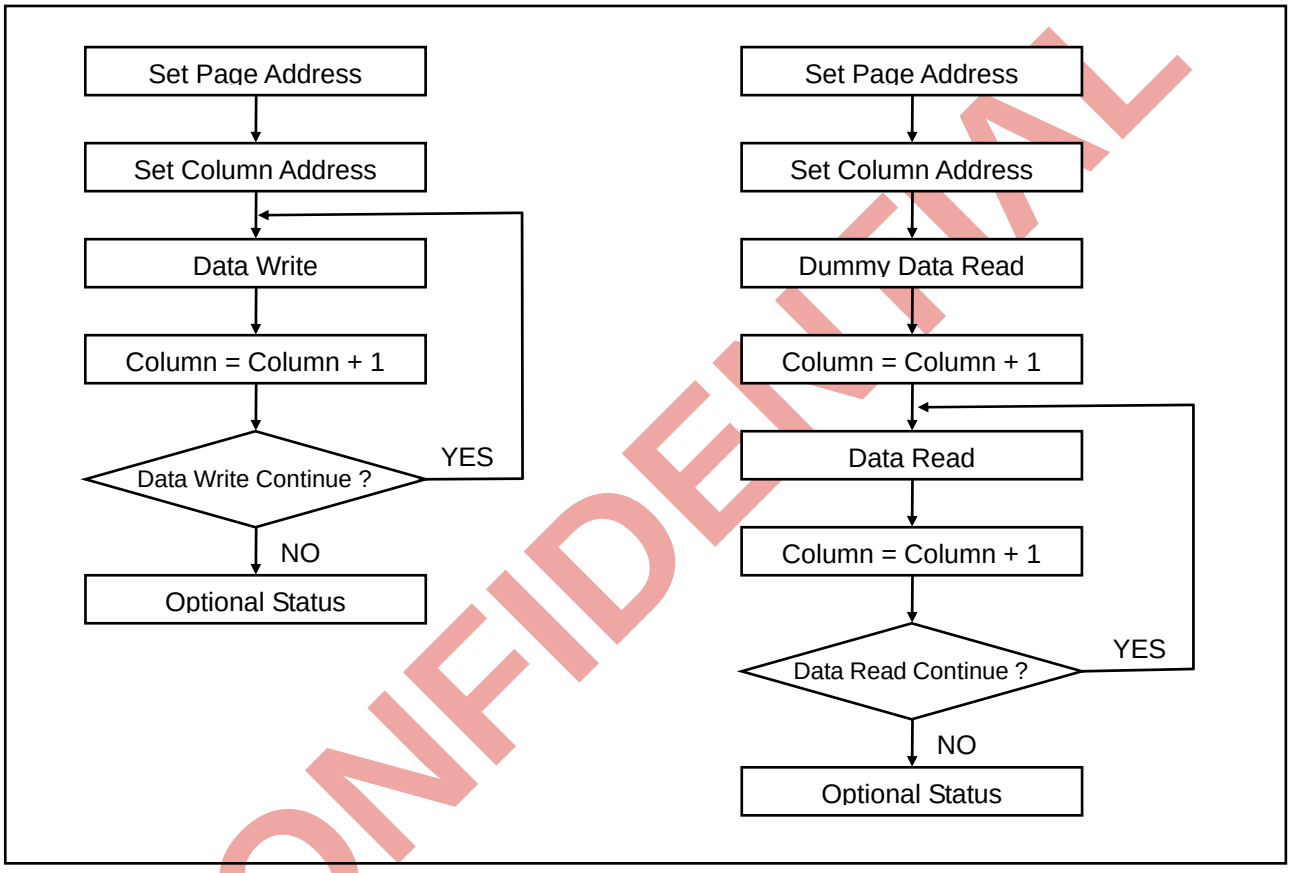


Figure 18. Sequence for Writing Display Data

Figure 19. Sequence for Reading Display Data

Data Read Display Data

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

ADC Select (Segment Driver Direction Select)

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0 : normal direction (SEG0 to SEG223)
ADC = 1 : reverse direction (SEG223 to SEG0)

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = “1”	RAM bit data = “0”
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0 : normal display
EON = 1 : entire display ON

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	BIAS

BIAS = 0 : 1/9
BIAS = 1 : 1/7

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

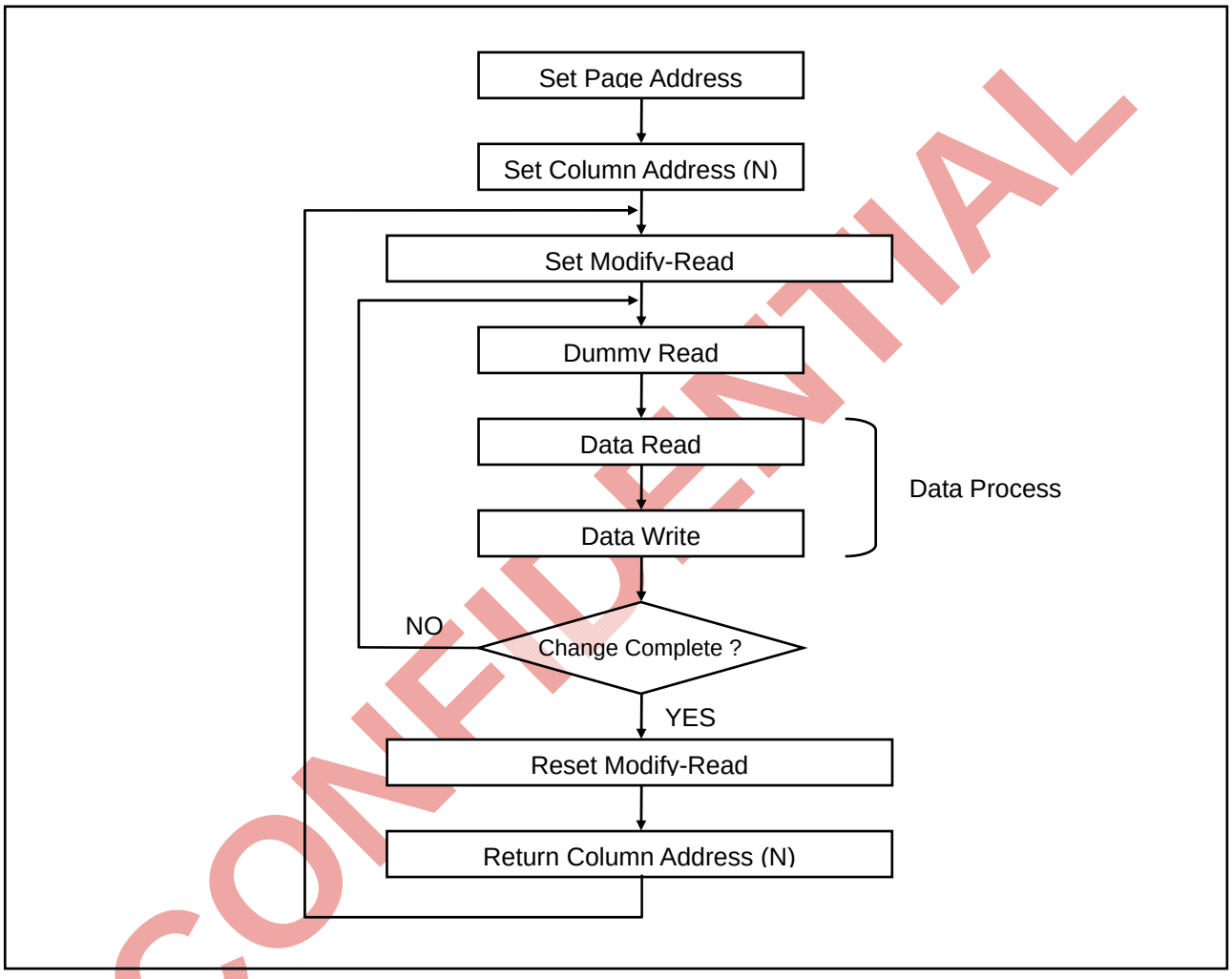


Figure 20. Sequence for Cursor Display

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SHL Select (Common Output Mode Select)

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

× : Don't care

SHL = 0 : normal direction (COM0 to COM63)
SHL = 1 : reverse direction (COM63 to COM0)

Power Control

Selects on of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
		0 1	Internal voltage converter circuit is OFF Internal voltage converter circuit is ON

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 12.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	(1 + Rb / Ra) ratio
0	0	0	4.5 (default)
0	0	1	5.0
0	1	0	5.5
0	1	1	6.0
1	0	0	6.5
1	0	1	7.0
1	1	0	7.5
1	1	1	8.0

Reference Voltage Select

Consists of 2-byte instruction. The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st instruction : Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd instruction : Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage Parameter (α)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62		
1	1	1	1	1	1	63	Maximum	High

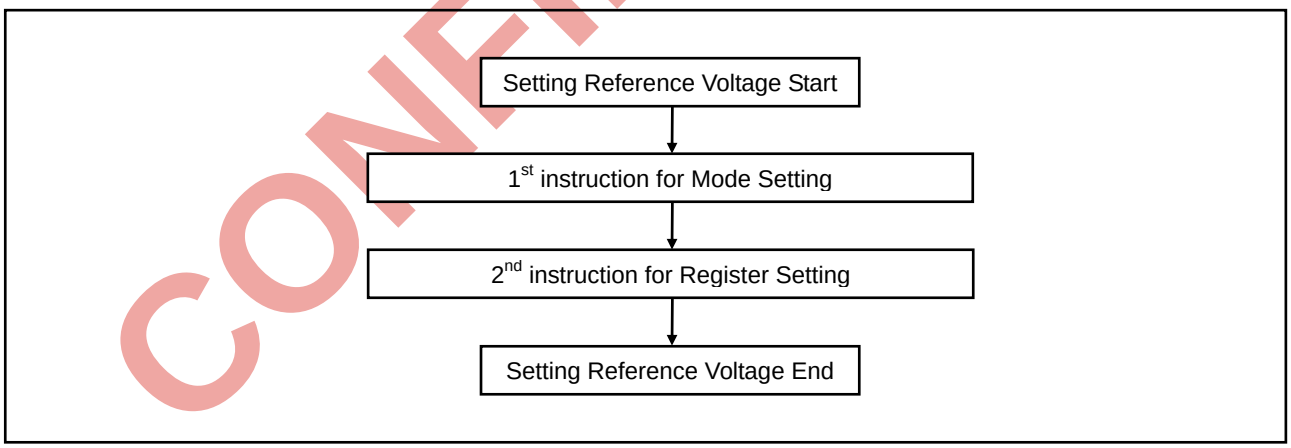


Figure 21. Sequence for Setting the Reference Voltage

Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator mode) enables the second byte instruction (set Static Indicator register) to be valid. The first byte sets the Static Indicator ON / OFF. When it is ON, the second byte updates the contents of Static Indicator register without issuing any other instruction and this Static Indicator state is released after setting the data of indicator register.

The 1st instruction : Set Static Indicator Mode (NO / OFF)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0 : static indicator OFF
SM = 1 : static indicator ON

The 2nd instruction : Set Static Indicator Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 0.5 second blinking)
1	0	ON (about 1.0 second blinking)
1	1	ON (always ON)

Power Save

This command makes the static indicator enter the power save mode and can greatly reduce the power consumption. The power save mode consists of the sleep and stand-by mode. The operating mode before the display data and power save activation is held in the sleep and stand-by modes, and the display data RAM can also be accessed from the MPU.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	SAV

SAV = 0 : stand-by mode
SAV = 1 : sleep mode

- Stand-by mode

This command stops the operation of the duty LCD display system and operations only the static drive system for indicators. Consequently the minimum current consumption required for the static drive is obtained. The internal state in the stand-by mode is as follows:

(1) The LCD power supply circuit is stopped. The oscillator circuit is operated.
(2) The duty drive system liquid crystal drive circuit is stopped and the segment and common drivers output the Vss level. The static drive system is operated.

- Sleep mode

This command stops all the operations of LCD display systems, and can reduce the power consumption approximate to the static current when they are not accessed from MPU. The internal state in the sleep mode is as follows:

(3) The oscillator circuit and the LCD power supply circuit are stopped.
(4) All liquid crystal drive circuit is stopped and the segment and common drivers output the Vss level.

※ The instruction or data is written must be waiting for 100ms after power save completed.

Power Save Reset

This command resets the power save mode and returns the state before power save activation.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

※ The instruction or data is written must be waiting for 100ms after power save reset completed.
※ To avoid display data loss in power save mode, please re-write display ram data before power save reset execute.

n-Line Reversal Drive Register Set

This command sets the number of reversal lines of the liquid crystal drive in the register. 2 to 16 lines can be set.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	PL3	PL2	PL1	PL0

PL3	PL2	PL1	PL0	Line of reversal lines
0	0	0	0	–
0	0	0	1	2
0	0	1	0	3
-	-	-	-	↓
0	1	1	1	15
1	1	1	1	16

n-Line Reversal Drive Reset

This command resets the n-line reversal alternating current drive and returns to the normal 2-frame reversal alternating current drive system. The value of the n-line reversal alternating current drive register is not changed.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Built-in Oscillator Circuit ON / OFF

This command starts the operation of the built-in oscillator circuit. This command is valid only for the master operation (MS=HIGH) and built-in oscillator circuit valid (CLS=HIGH)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

External Capacitor discharge

This command turn on/off the discharge function for external capacitor (V0 ~ V5) of power follower, the function can prevent the residual display line after power off or sleep/stand-by mode. (The procedure for discharge function, please refer Figure 23 on page 47)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	DISC		

DISC = 000 : discharge function enable
DISC = 111 : discharge function disable

NOP

Non Operation Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

These are the instruction for IC chip testing. Please do not use it. If the Test Instruction is used by accident, it can be cleared by applying “0” signal to the RESB input pin or the reset instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

One Time Programming (OTP) control

The IST3020 provides OTP functions for contrast (3 times) offset adjustment. When these OTP bits have been programmed after the next reset, the previous programmed values will be restored. The programmed values will be kept at the embedded NVM (Non-Volatile Memory) and the values will be restored even the power be turned off.

The OTP program mode setting is consists of 2-bytes instruction, the 1st instruction enter OTP program mode, the 2nd one set the contents of OTP control register. When OTPADJ is set to “0” (default = “1”), the contrast offset adjustment function will be disable and only the original command (Set reference voltage instruction, page 39) setting will be effected. Before OTP program beginning, OTPPON must set to “1” (default = “0”), then program section start, after program has been finished, and set OTPON =”0”.

The 1st instruction : Set OTP Program Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	0

The 2nd instruction : Set OTP Program Mode Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	OTPADJ	OTPPON	x	x	x	x	x	x

OTPADJ = 0 : Contrast offset value is invalid
OTPADJ = 1 : Contrast offset value is valid
OTPPON = 0 : OTP programming disable
OTPPON = 1 : OTP programming enable

The contrast offset setting is consists of 2-bytes instruction, the 1st instruction sets contrast offset mode, the 2nd one updates the contents of contrast offset register. When OTPADJ set to “1”, the final contrast adjustment is calculation by this equation “Contrast = SV + CTA + CTB + CTC”, before OTP programming,

the default value of CTA, CTB and CTC are “0”, the contrast within the range 0 to 63, please don’t let the calculated output be overflow and cause some expected results.

The 1st instruction : Set OTP Contrast offset Mode (1)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	1

The 2nd instruction : Set OTP Contrast offset Register (1)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	CTA5	CTA4	CTA3	CTA2	CTA1	CTA0

The 1st instruction : Set OTP Contrast offset Mode (2)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	0

The 2nd instruction : Set OTP Contrast offset Register (2)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	CTB4	CTB3	CTB2	CTB1	CTB0

The 1st instruction : Set OTP Contrast offset Mode (3)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	1

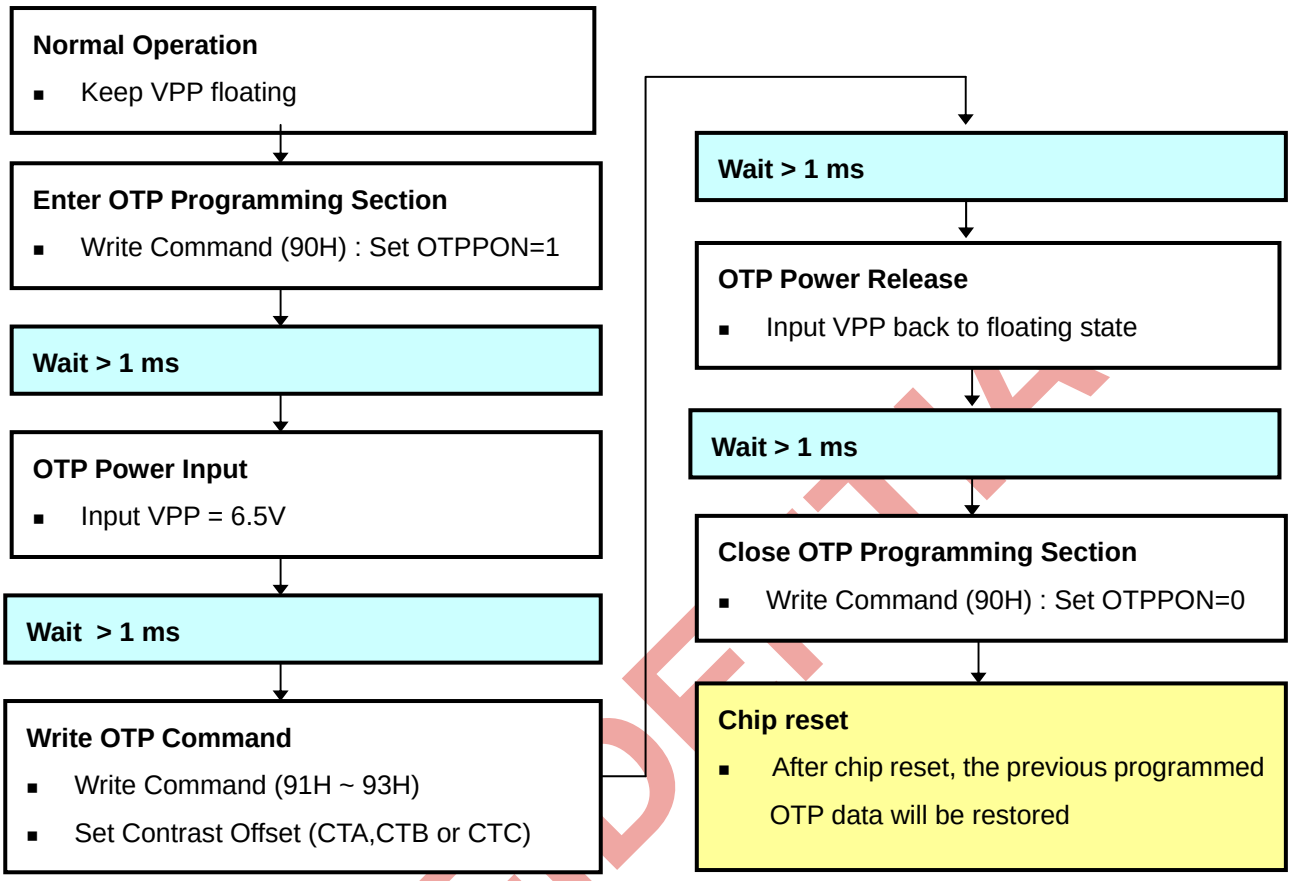
The 2nd instruction : Set OTP Contrast offset Register (3)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	CTC4	CTC3	CTC2	CTC1	CTC0

CTA5	CTA4	CTA3	CTA2	CTA1	CTA0	Offset Value
0	1	1	1	1	1	+31
0	1	1	1	1	0	+30
-	-	-	-	-	-	↓
0	0	0	0	0	0	0
-	-	-	-	-	-	↓
1	0	0	0	0	1	-31
1	0	0	0	0	0	-32

CTB4 CTC4	CTB3 CTC3	CTB2 CTC2	CTB1 CTC1	CTB0 CTC0	Offset Value
0	1	1	1	1	+15
-	-	-	-	-	↓
0	0	0	0	0	0
-	-	-	-	-	↓
1	0	0	0	0	-16

OTP Programming Flow



NOTICE

- The 1st CT adjustment MUST program 91h, the 2nd CT adjustment MUST program 92h, and the 3rd CT adjustment MUST program 93h.
- If the 1st time CT adjustment is not satisfied, user can try the 2nd or 3rd time CT adjustment by programming 92h/93h, and then the CT offset value will be accumulated automatically.
- The 2nd or 3rd time CT adjustment MUST after 1st time CT adjustment, otherwise the 2nd or 3rd time CT adjustment will be ignore.

Referential Instruction Setup Flow (1)

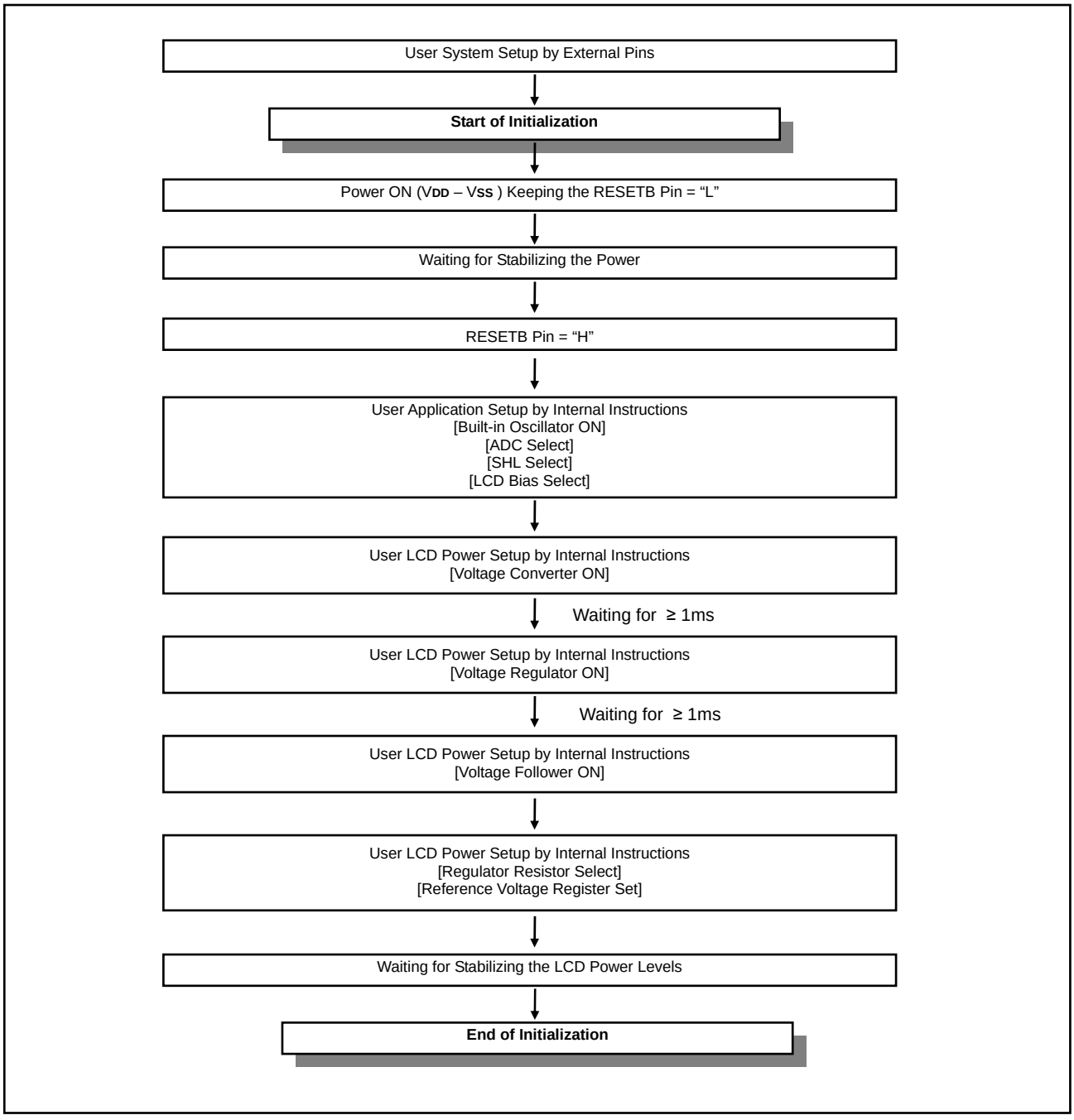


Figure 22. Initializing with the Built-in Power Supply Circuits (Normal mode)

Referential Instruction Setup Flow (2)

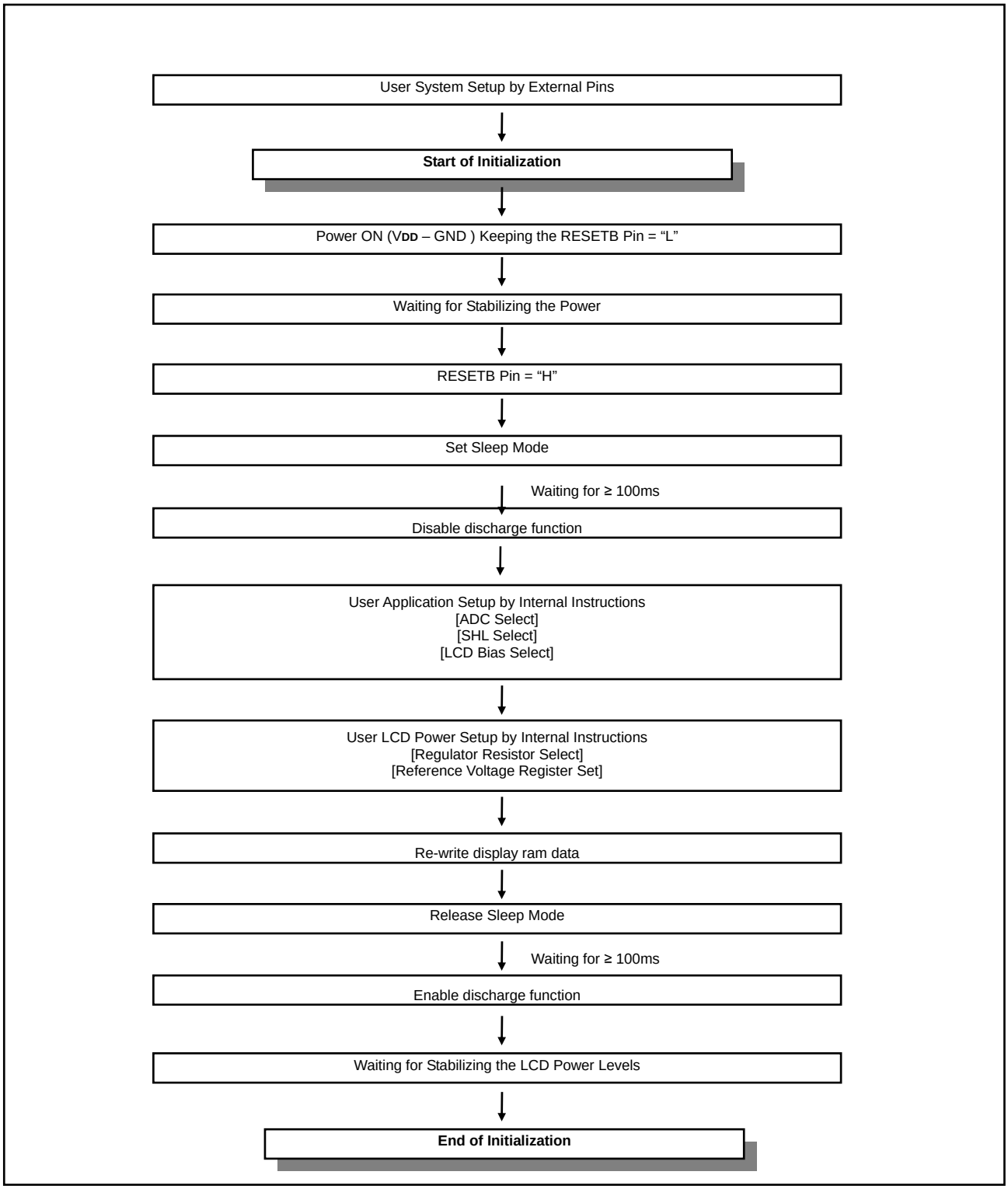


Figure 23. Initializing with the Built-in Power Supply Circuits (Power save mode)

Referential Instruction Setup Flow (3)

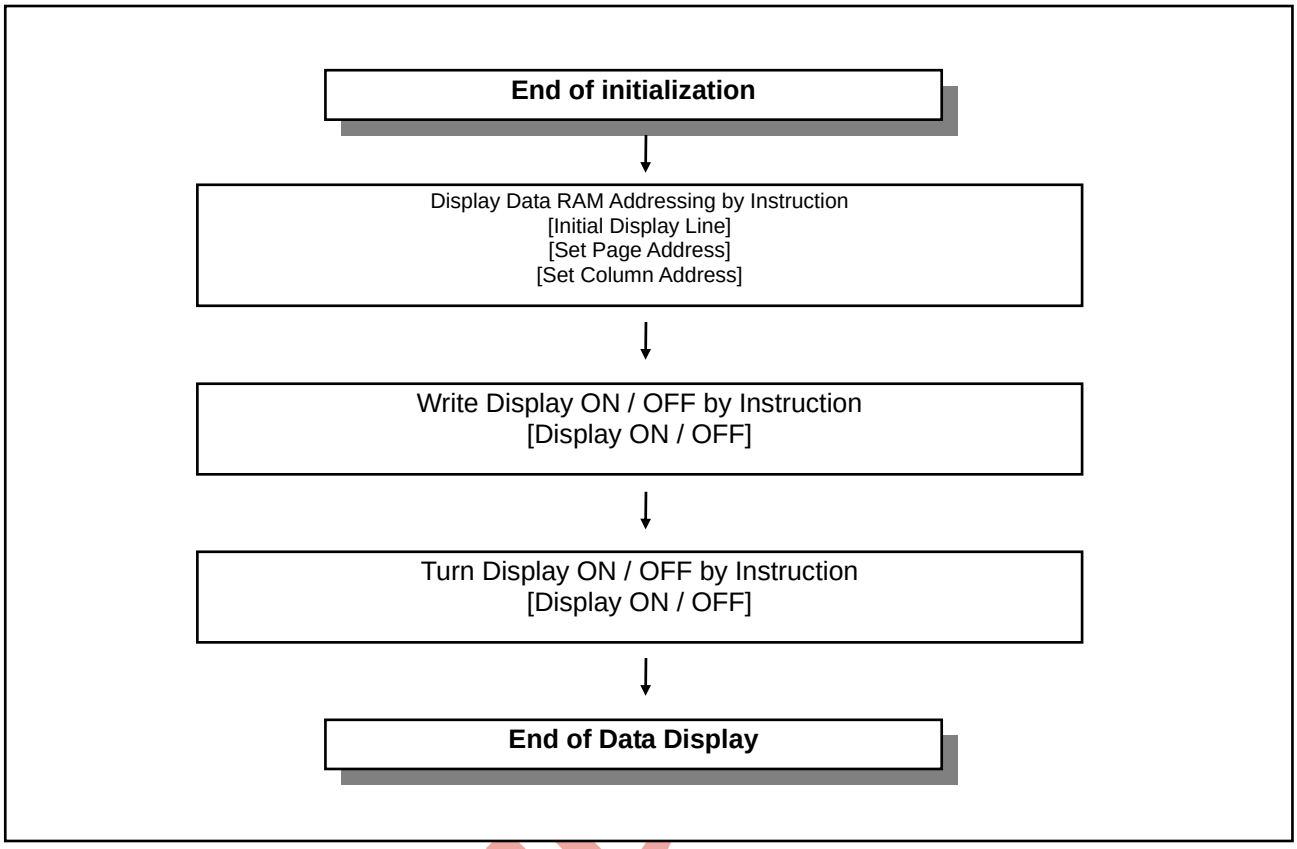


Figure 24. Data Displaying

Referential Instruction Setup Flow (4)

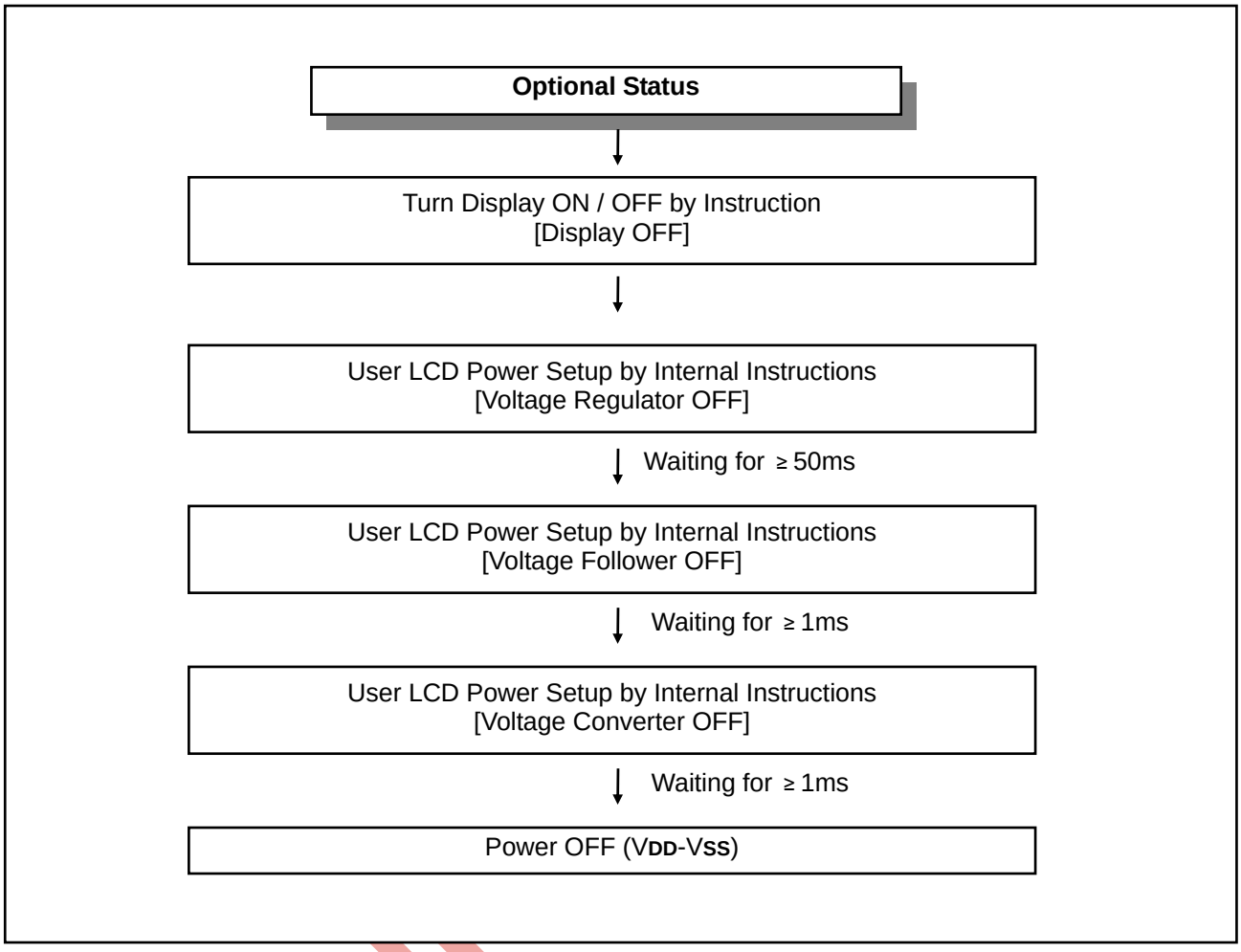


Figure 25. Power OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 16. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD1} V_{DD2}	- 0.3 to +7.0	V
	V_{LCD}	-0.3 to +17.0	V
Input voltage range	V_{IN}	-0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	-40 to +85	℃
Storage temperature range	T_{STR}	-55 to +125	℃

NOTES:

1. VDD and VLCD are based on VSS = 0V
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied. (VLCD = V0 – VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 17. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 3.6V, Ta = -40 to 85℃)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage(1)		V_{DD1} V_{DD2}		2.4	-	3.6	V	VDD *1
Operating Voltage(2)		V0		4.5	-	15.0	V	V0 *2
Input voltage	High	V_{IH}		0.8 V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2 V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8 V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2 V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	-1.0	-	+1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	-3.0	-	+3.0	µA	*6
LCD driver ON Resistance		R_{ON}	Ta = 25℃, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Fosc	f_{OSC}	Ta = 25℃	17.6	22.0	26.4	kHz	CL
	External	f_{CL}		17.6	22.0	26.4		
Voltage converter input voltage		VCI	×2	2.4	-	3.6	V	VCI
			×3	2.4	-	3.6		
			×4	2.4	-	3.6		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT		6.0	-	15.0	V	VOUT
Voltage follower operating voltage		V0		4.5	-	14.0	V	V0 *8
Reference voltage		V_{REF}	Ta = 25℃ -0.05%/℃	2.03	2.1	2.17	V	*9

Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)

(Ta = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V_{DD} = 3.0V V0 – V_{SS} = 11.0V Display pattern OFF	-	15	23	μA	*10

Dynamic Current Consumption (2) when the Built-in Power Circuit is ON (At Operate Mode)

(Ta = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V (VCI = Vdd, 4 times boosting) V0 – V_{SS} = 11.0V Display pattern OFF Normal power mode	-	40	60	μA	*11
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V (VCI = Vdd, 4 times boosting) V0 – V_{SS} = 11.0V Display pattern checker Normal power mode	-	150	200	μA	*12

Current Consumption during Power Save Mode

(Ta = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DD1}	During sleep	-	-	2.0	μA	
Standby mode current	I_{DD2}	During standby	-	-	30.0	μA	

[* Remark Solves]

*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.

*2. In case of external power supply is applied.

*3. CS1B, CS2, A0, DB0 to DB7, RDB, WRB, RESETB, MS, C86, PS, IRS, CLS, CL, FR, SYNC, DOFB pins.

*4. DB[7:0], FR, FRS, DOFB, CL pins.

*5. CS1B, CS2, A0, DB [7:0], RDB, WRB, RESETB, MS, C86, PS, IRS, CLS, CL, FR, SYNC, DOFB pins.

*6. Applies when the DB [7:0], FR, FRS, DOFB, and CL pins are in high impedance.

*7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON= ΔV / 0.1 [KΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)

*8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range

*9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.

*10,11. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.

The current consumption, when the built-in power supply circuit is ON or OFF.

The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

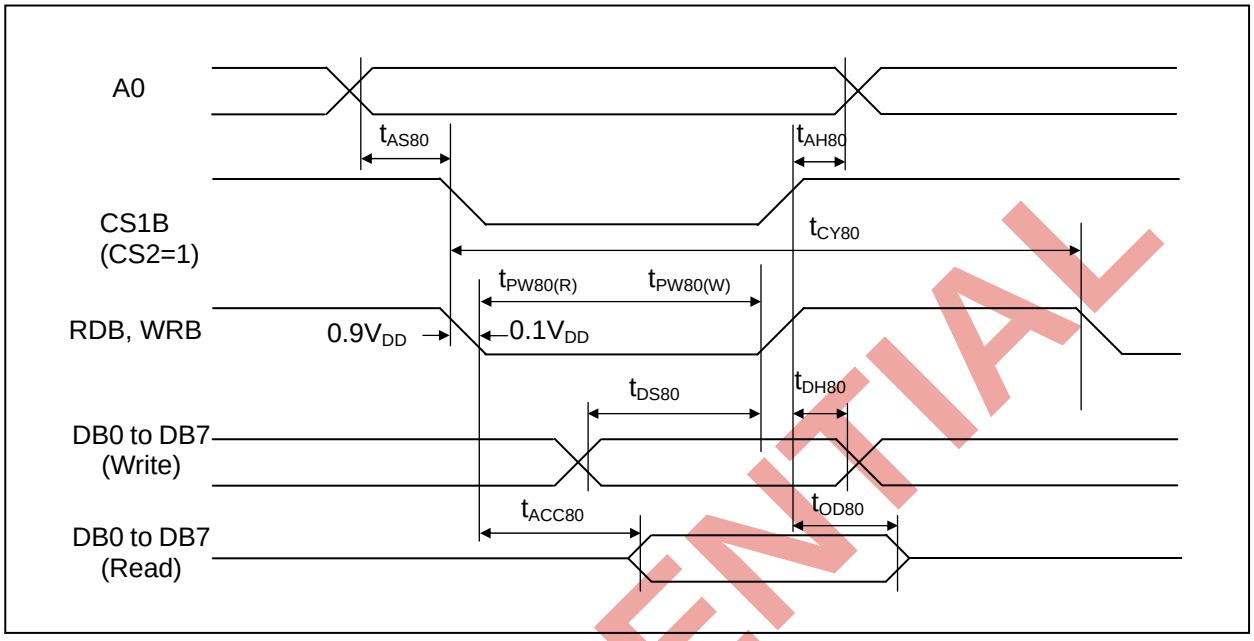


Figure 26. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time	A0	t_{CY80}	300	-	-	ns	
Pulse width (WRB)	WRB	t_{PW80}(W)	60	-	-	ns	
Pulse width (RDB)	RDB	t_{PW80}(R)	60	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	40 15	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	- 10	-	140 100	ns	C_L = 100pF

Read / Write Characteristics (6800-series Microprocessor)

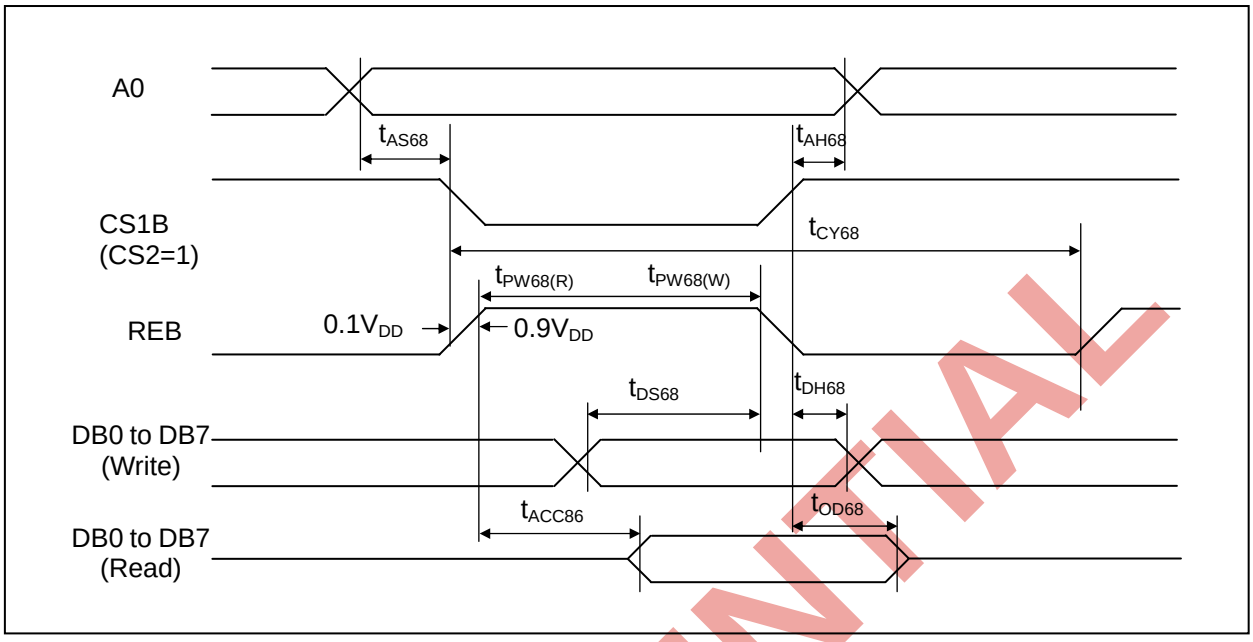


Figure 27. Read / Write Characteristics (6800-series Microprocessor)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85℃)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		A0	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle time		A0	t_{CY68}	300	-	-	ns	
Data setup time Data hold time		DB7 to DB0	t_{DS68} t_{DH68}	40 15	-	-	ns	
Access time Output disable time			t_{ACC86} t_{OD68}	- 10	-	140 100	ns	C_L = 100pF
Enable pulse width	Read Write	RDB	t_{PW68}(R) t_{PW68}(W)	60	-	-	-	

Serial Interface Characteristics

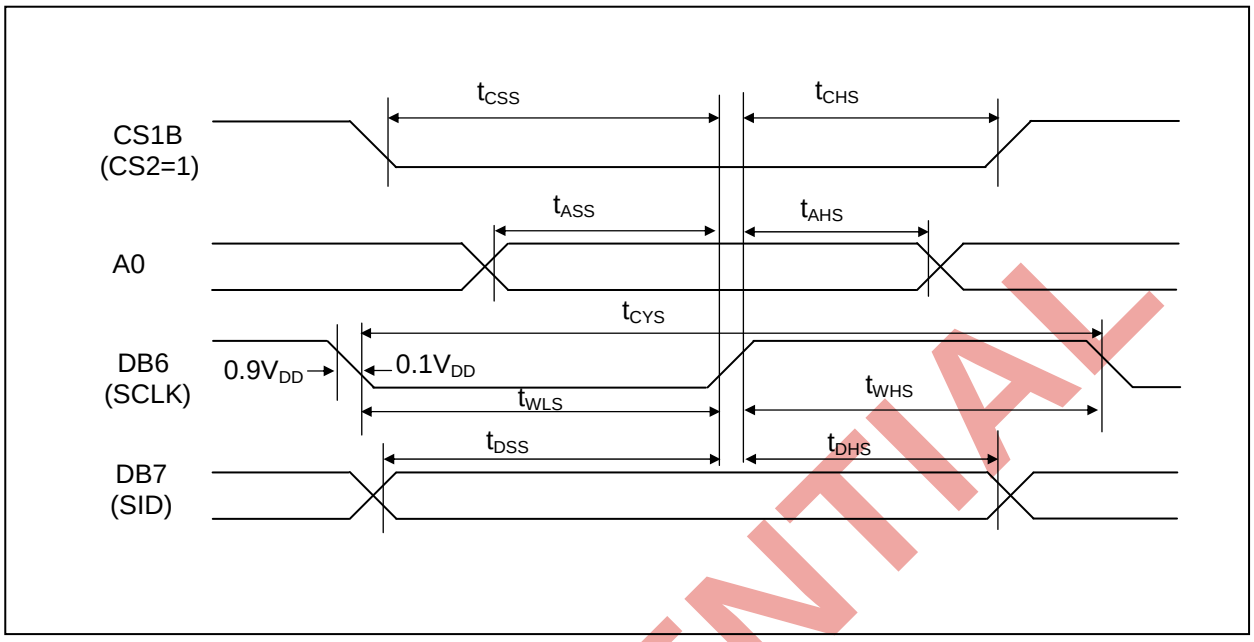


Figure 28. Serial Interface Characteristics

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	tCYS tWHS tWLS	250 100 100	- - -	- - -	ns	
Address setup time Address hold time	A0	tASS tAHS	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	tDSS tDHS	100 100	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	150 150	- -	- -	ns	

Reset Input Timing

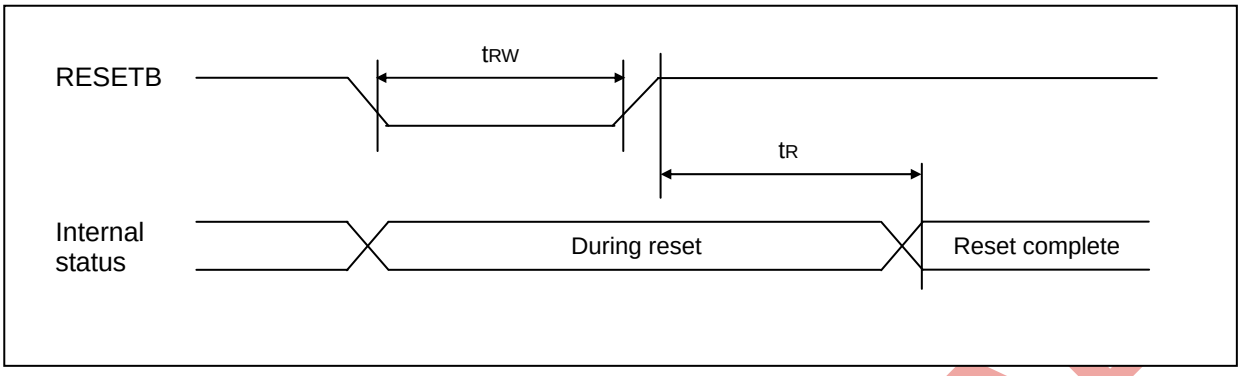


Figure 29. Reset Input Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	1.0	-	-	ns	
Reset time	-	t_R	-	-	1.0	ns	

Display Control Output Timing

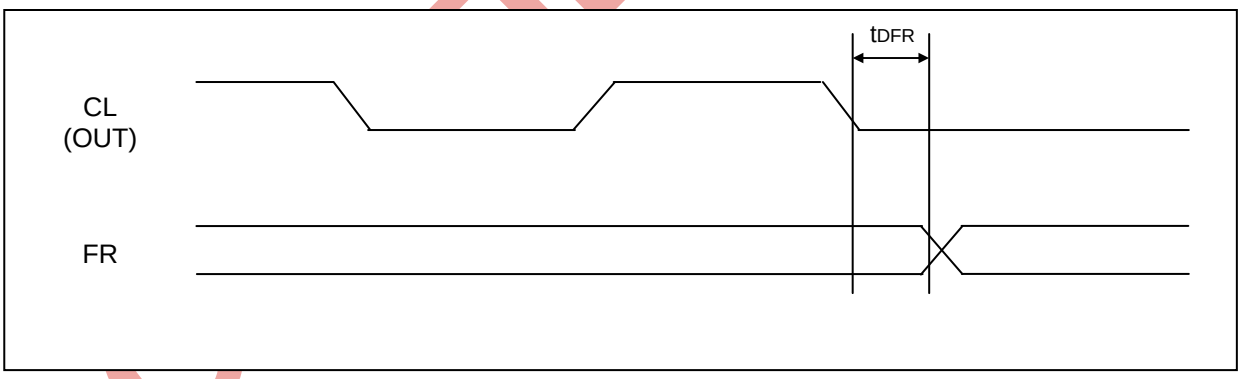


Figure 30. Display Control Output Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	20	80	ns	C_L = 50 pF

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = "H", C86 = "H")

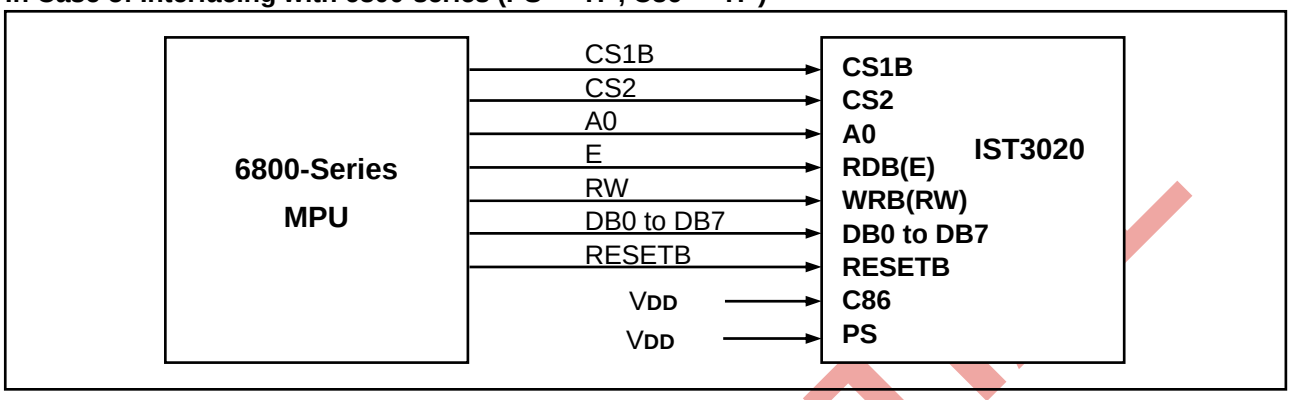


Figure 31. Interfacing with 6800-series (PS = "H", C86 = "H")

In Case of Interfacing with 8080-series (PS = "H", C86 = "L")

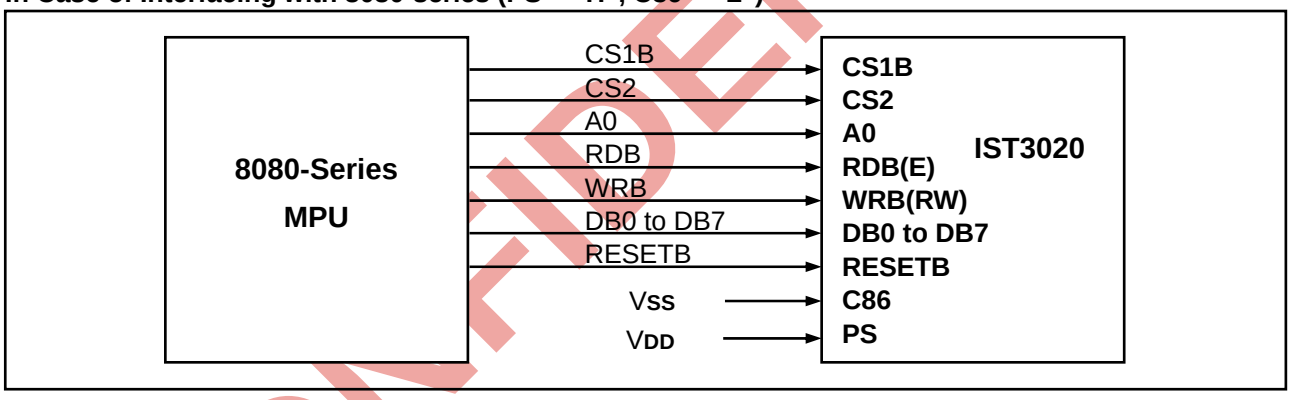


Figure 32. Interfacing with 8080-series (PS = "H", C86 = "H")

In Case of Serial Interface (PS = "L", C86 = "L")

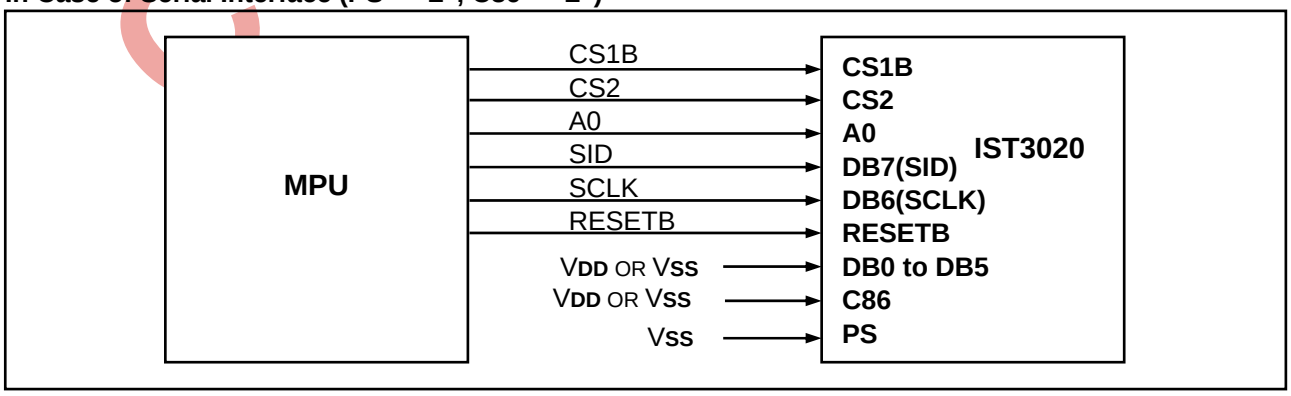


Figure 33. Serial Interface (PS = "L", C86 = "L")

Connections between IST3020 and LCD Panel

Single Chip Structure

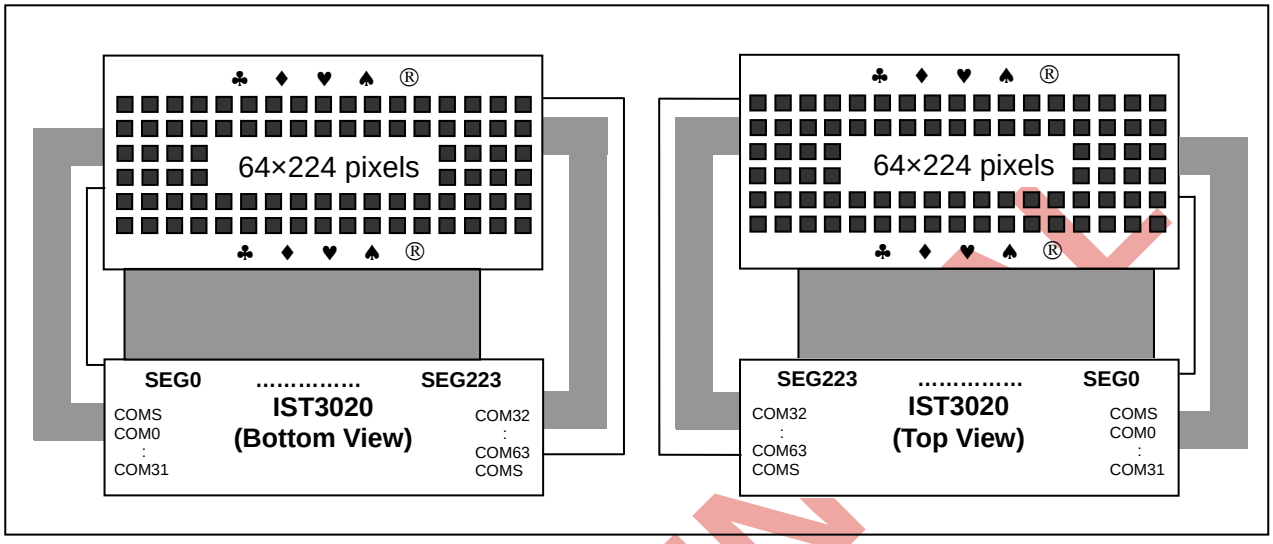


Figure 34. SHL = 1, ADC = 0

Figure 35. SHL = 1, ADC = 1

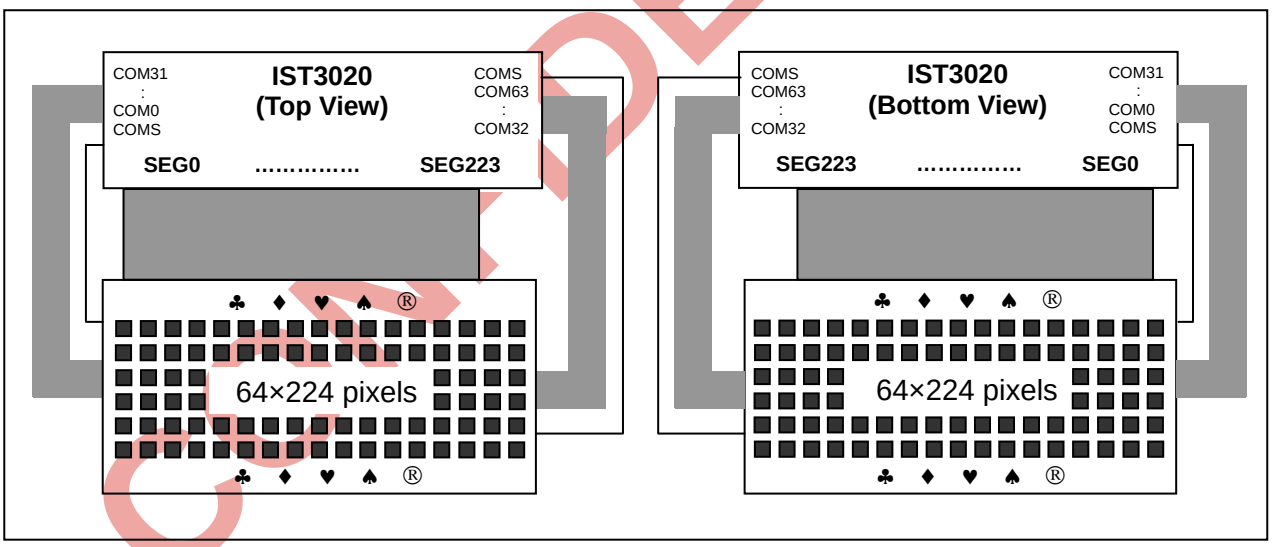


Figure 36. SHL = 0, ADC = 0

Figure 37. SHL = 0, ADC = 1

Multiple Chip Structure

- 65COM (64COM + 1COMS) x 448SEG (224SEG x 2)

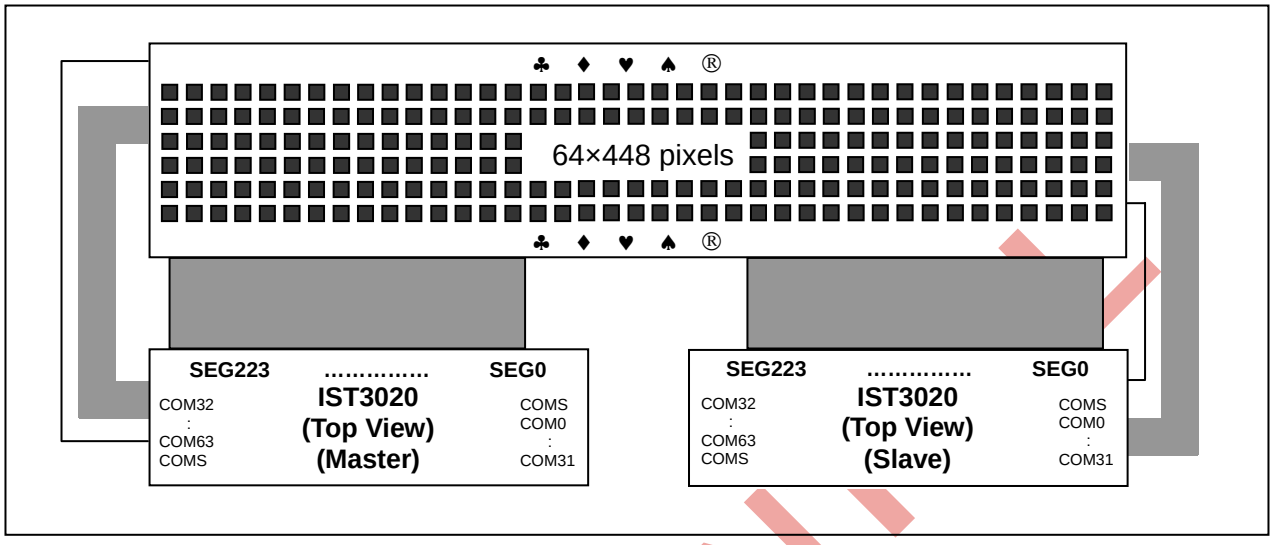


Figure 38. SHL = 1, ADC = 1

- Connect the following pins of two chips each other:
  - Display clock pins: CL, FR
  - Display control pin: DOFB
  - LCD power pins: V0, V1, V2, V3, V4

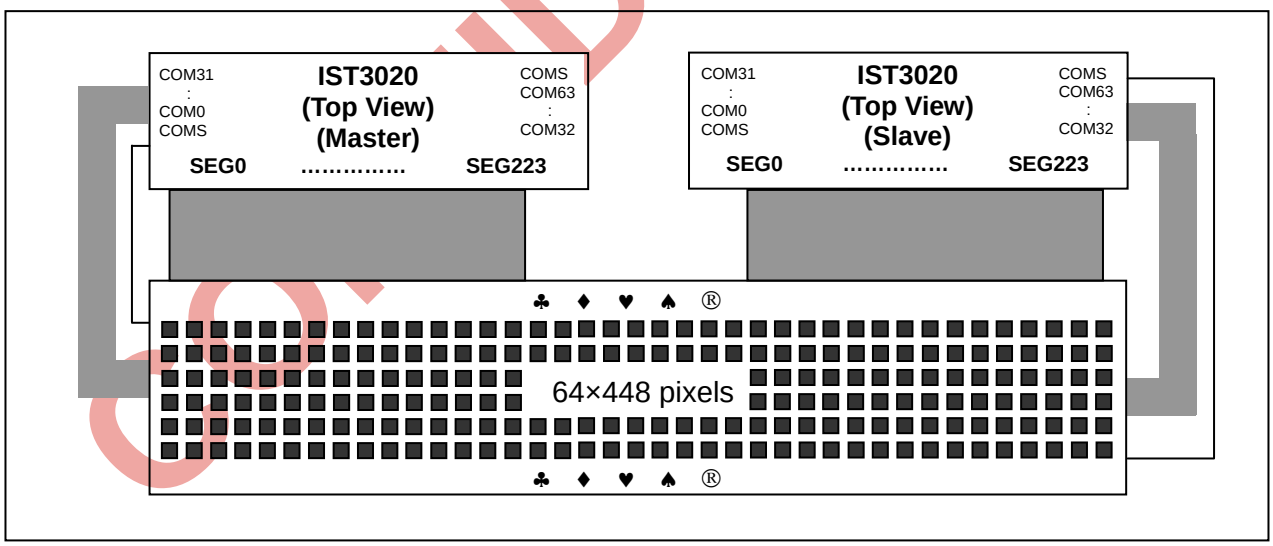


Figure 39. SHL = 0, ADC = 0

- Connect the following pins of two chips each other:
  - Display clock pins: CL, FR
  - Display control pin: DOFB
  - LCD power pins: V0, V1, V2, V3, V4

- 130COM (128COM + 2COMS) x 224SEG

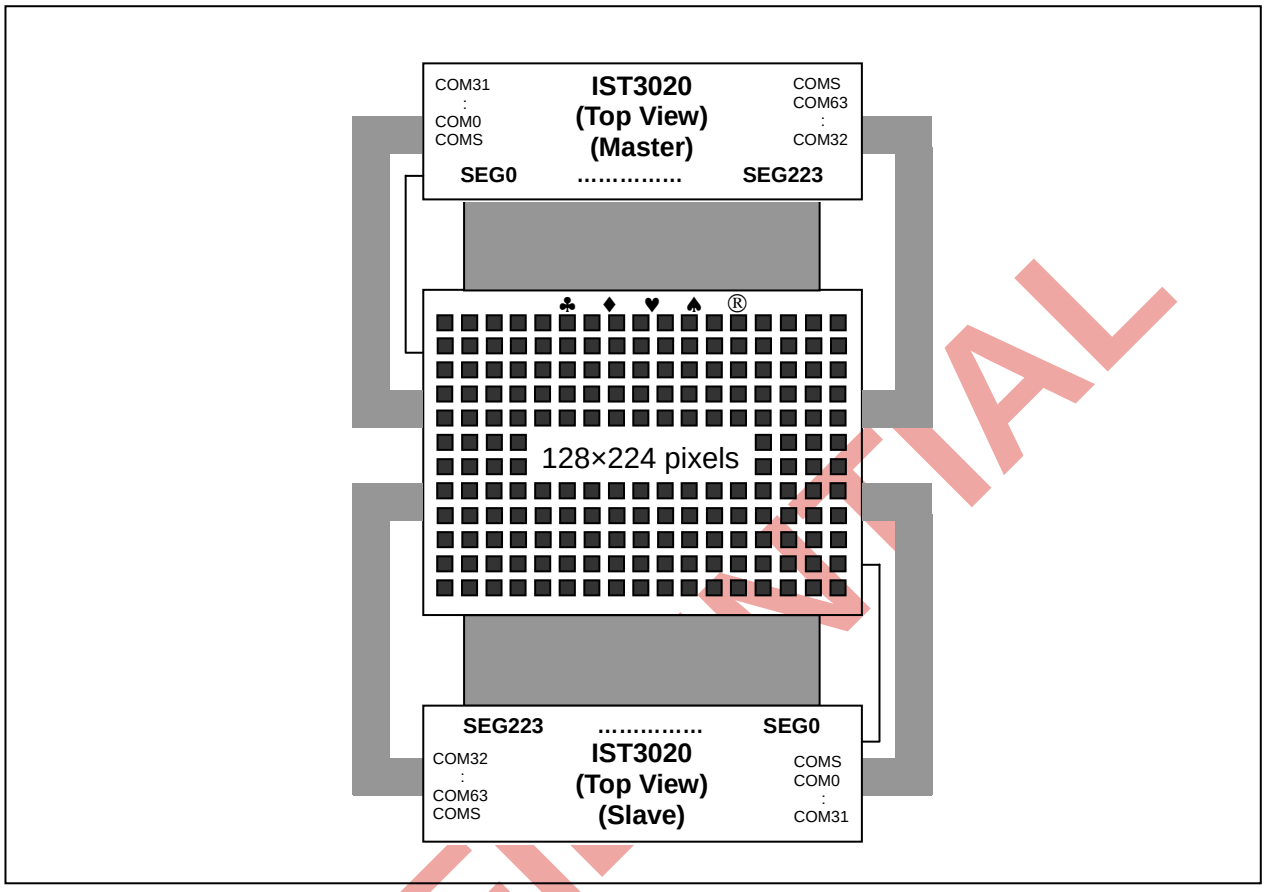
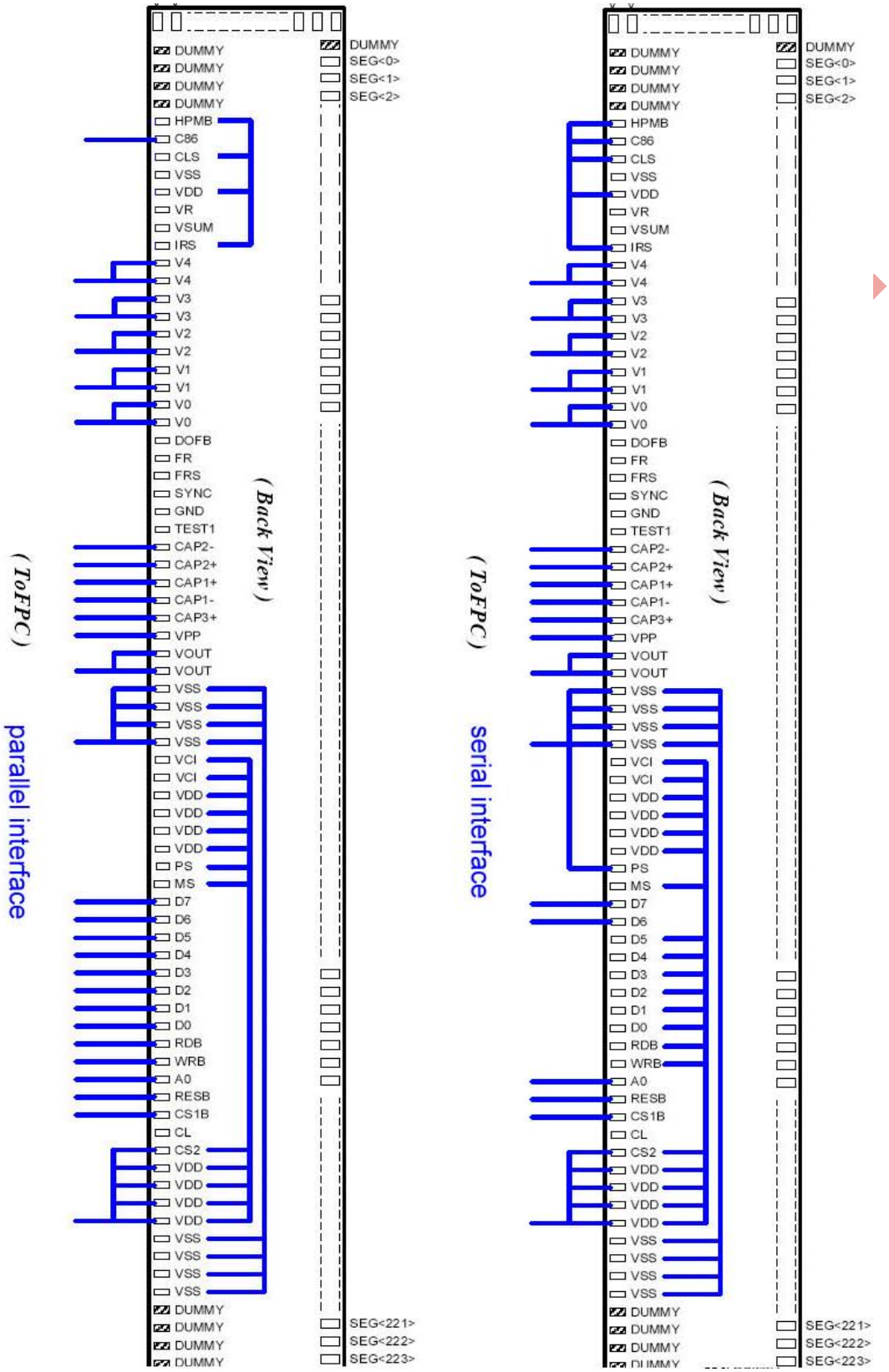


Figure 40. 130COM (128COM + 2COMS) x 224SEG

- Connect the following pins of two chips each other:
  - Display clock pins: CL, FR
  - Display control pin: DOFB
  - LCD power pins: V0, V1, V2, V3, V4

- Common / Segment output direction select
  - Master chip: SHL = 0, ADC = 0
  - Slave chip: SHL = 1, ADC = 1

IST3020 ITO connection example



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