

**a-Si TFT LCD Single Chip Driver  
240RGBx320 Resolution and 262K color  
Datasheet**

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## 1. Introduction

ILI9335 is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes RAM for graphic data of 240RGBx320 dots, and power supply circuit.

ILI9335 has four kinds of system interfaces which are i80-system MPU interface (8-/9-/16-/18-bit bus width), VSYNC interface (system interface + VSYNC, internal clock, DB[17:0]), serial data transfer interface (SPI), RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

ILI9335 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9335 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9335 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

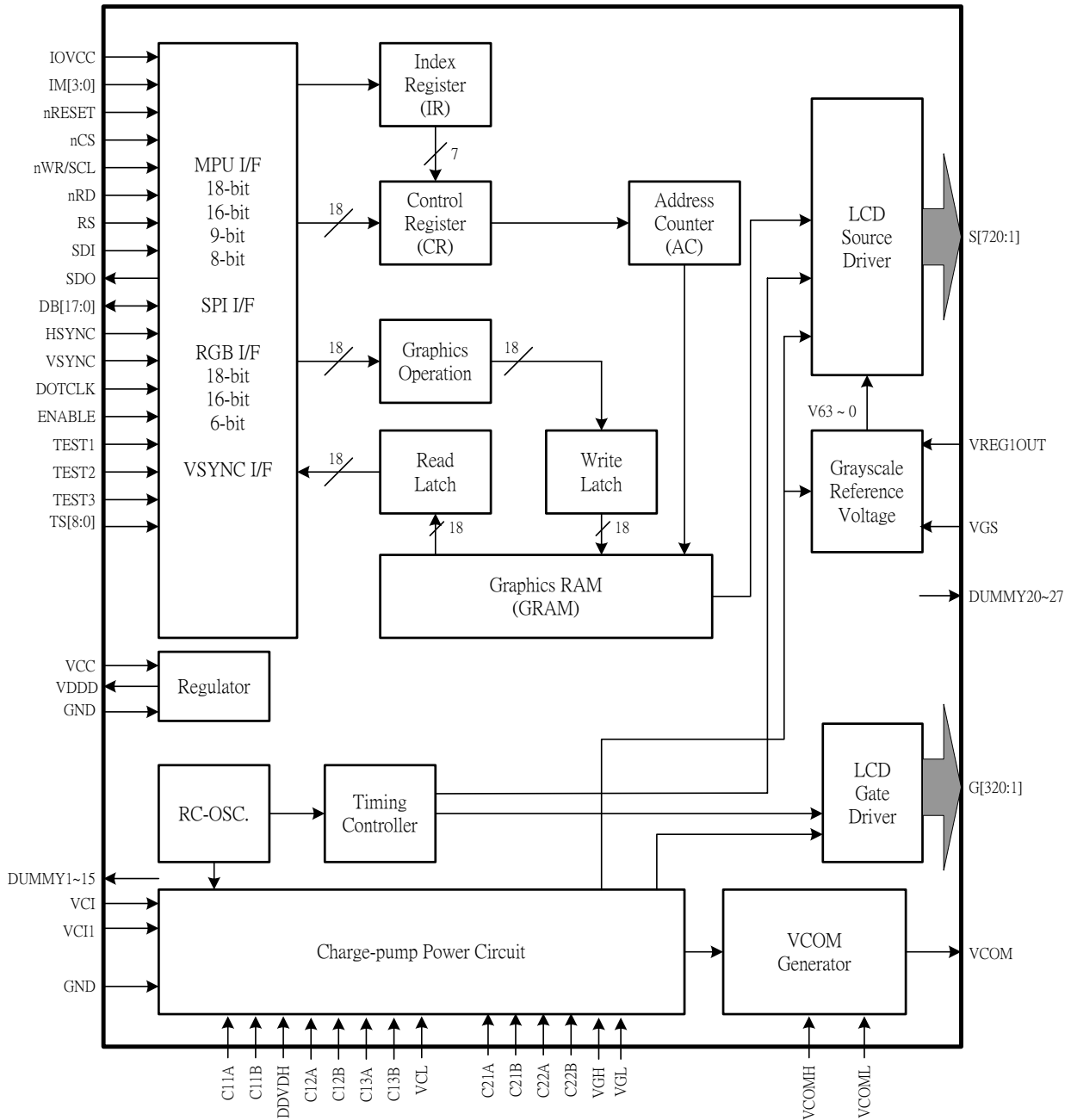
## 2. Features

- ◆ Single chip solution for a liquid crystal QVGA TFT LCD display
- ◆ 240RGBx320-dot resolution capable with real 262,144 display color
- ◆ Support MVA (Multi-domain Vertical Alignment) wide view display
- ◆ Incorporate 720-channel source driver and 320-channel gate driver
- ◆ Internal 172,800 bytes graphic RAM
- ◆ System interfaces
  - i80 system interface with 8-/9-/16-/18-bit bus width
  - Serial Peripheral Interface (SPI)
  - RGB interface with 6-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - VSYNC interface (System interface + VSYNC)
- ◆ Internal oscillator and hardware reset
- ◆ Reversible source/gate driver shift direction
- ◆ Window address function to specify a rectangular area for internal GRAM access
- ◆ Bit operation function for facilitating graphics data processing
  - Bit-unit write data mask function
  - Pixel-unit logical/conditional write function
- ◆ Abundant functions for color display control
  - $\gamma$ -correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function
- ◆ Partial drive function, enabling partially driving an LCD panel at positions specified by user
- ◆ Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- ◆ Power saving functions
  - 8-color mode
  - standby mode
  - sleep mode
  - deep stand by mode
- ◆ Low -power consumption architecture
  - Low operating power supplies:
    - IOVcc = 1.65V ~ 3.6 V (interface I/O)
    - VCI = 2.5V ~ 3.6 V (analog)
- ◆ LCD Voltage drive:
  - Source/VCOM power supply voltage
    - DDVDH - GND = 4.5V ~ 6.0
    - VCL - GND = -2.0V ~ -3.0V
    - VCI - VCL  $\leq$  6.0V
  - Gate driver output voltage
    - VGH - GND = 10V ~ 20V
    - VGL - GND = -5V ~ -15V



- $V_{GH} - V_{GL} \leq 30V$
- VCOM driver output voltage
  - $V_{COMH} = (V_{CI} + 0.2)V \sim (DDVDH - 0.2)V$
  - $V_{COML} = (V_{CL} + 0.2)V \sim 0V$
  - $V_{COMH} - V_{COML} \leq 6.0V$
- ◆ a-TFT LCD storage capacitor: Cst only

### 3. Block Diagram



## 4. Pin Descriptions

Pin Name	I/O	Type	Descriptions																																																																								
Input Interface																																																																											
IM3, IM2, IM1, IM0/ID	I	IOVcc	Select the MPU system interface mode																																																																								
			<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>MPU-Interface Mode</th> <th>DB Pin in use</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>i80-system 16-bit interface</td> <td>DB[17:10], DB[8:1]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>i80-system 8-bit interface</td> <td>DB[17:10]</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>ID</td> <td>Serial Peripheral Interface (SPI)</td> <td>SDI, SDO</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>*</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>i80-system 18-bit interface</td> <td>DB[17:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>i80-system 9-bit interface</td> <td>DB[17:9]</td> </tr> <tr> <td>1</td> <td>1</td> <td>*</td> <td>*</td> <td>Setting invalid</td> <td></td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	0	0	0	0	Setting invalid		0	0	0	1	Setting invalid		0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]	0	0	1	1	i80-system 8-bit interface	DB[17:10]	0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO	0	1	1	*	Setting invalid		1	0	0	0	Setting invalid		1	0	0	1	Setting invalid		1	0	1	0	i80-system 18-bit interface	DB[17:0]	1	0	1	1	i80-system 9-bit interface	DB[17:9]	1	1	*	*	Setting invalid	
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1	0	1	1	i80-system 9-bit interface	DB[17:9]																																																																						
1	1	*	*	Setting invalid																																																																							
			When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.																																																																								
nCS	I	MPU IOVcc	A chip select signal. Low: the ILI9335 is selected and accessible High: the ILI9335 is not selected and not accessible Fix to the GND level when not in use.																																																																								
RS	I	MPU IOVcc	A register select signal. Low: select an index or status register High: select a control register Fix to either IOVcc or GND level when not in use.																																																																								
nWR/SCL	I	MPU IOVcc	A write strobe signal and enables an operation to write data when the signal is low. Fix to either IOVcc or GND level when not in use. SPI Mode: Synchronizing clock signal in SPI mode.																																																																								
nRD	I	MPU IOVcc	A read strobe signal and enables an operation to read out data when the signal is low. Fix to either IOVcc or GND level when not in use.																																																																								
nRESET	I	MPU IOVcc	A reset pin. Initializes the ILI9335 with a low input. Be sure to execute a power-on reset after supplying power.																																																																								
SDI	I	MPU IOVcc	SPI interface input pin. The data is latched on the rising edge of the SCL signal.																																																																								
SDO	O	MPU IOVcc	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. Let SDO as floating when not used.																																																																								
DB[17:0]	I/O	MPU IOVcc	An 18-bit parallel bi-directional data bus for MPU system interface mode 8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. 18-bit parallel bi-directional data bus for RGB interface operation 6-bit RGB I/F: DB[17:12] are used. 16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. Unused pins must be fixed to GND level.																																																																								
ENABLE	I	MPU IOVcc	Data ENEABLE signal for RGB interface operation. Low: Select (access enabled)																																																																								

Pin Name	I/O	Type	Descriptions
			High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVcc or GND level when not in use.
DOTCLK	I	MPU IOVcc	Dot clock signal for RGB interface operation. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK Fix to the GND level when not in use
VSYNC	I	MPU IOVcc	Frame synchronizing signal for RGB interface operation. VSPL = "0": Active low. VSPL = "1": Active high. Fix to the GND level when not in use.
HSYNC	I	MPU IOVcc	Line synchronizing signal for RGB interface operation. HSPL = "0": Active low. HSPL = "1": Active high. Fix to the GND level when not in use
FMARK	O	MPU IOVcc	Output a frame head pulse signal. The FMARK signal is used when writing RAM data in synchronization with frame. Leave the pin open when not in use.
<b>LCD Driving signals</b>			
S720~S1	O	LCD	Source output voltage signals applied to liquid crystal. To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "h00000" is output from S1. SS = "1", the data in the RAM address "h00000" is output from S720. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G320~G1	O	LCD	Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines
VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.
VCOMH	O	Stabilizing capacitor	The high level of VCOM AC voltage. Connect to a stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The low level of VCOM AC voltage. Adjust the VCOML level with the VDV bits. Connect to a stabilizing capacitor.
VGS	I	GND or external resistor	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
<b>Charge-pump and Regulator Circuit</b>			
VCI	I	Power supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.6V.
VCC	I	Power supply	A supply voltage to the digital circuit. Connect to an external power supply of 2.5 ~ 3.6V.
VCI1	O	Stabilizing capacitor	An internal reference voltage for the step-up circuit1. The amplitude between VCI and GND is determined by the VC[2:0] bits. Make sure to set the VCI1 voltage so that the DDVDH, VGH and VGL voltages are set within the respective specification.
DDVDH	O	Stabilizing capacitor	Power supply for the source driver and Vcom drive.
VGH	O	Stabilizing capacitor	Power supply for the gate driver.
VGL	O	Stabilizing capacitor	Power supply for the gate driver.
VCL	O	Stabilizing capacitor	VCOML driver power supply. VCL = 0.5 ~ -VCI. Place a stabilizing capacitor between GND
C11A, C11B	I/O	Step-up	Capacitor connection pins for the step-up circuit 1.

Pin Name	I/O	Type	Descriptions
C12A, C12B		capacitor	
C13A, C13B C21A, C21B C22A, C22B	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.
VREG1OUT	I/O	Stabilizing capacitor	Output voltage generated from the reference voltage.  The voltage level is set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage, (2) VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor. $VREG1OUT = 3.0 \sim (DDVDH - 0.5)V$ .
<b>Power Pads</b>			
IOVCC	I	Power supply	A supply voltage to the interface pins: IM[3:0], nRESET, nCS, nWR, nRD, RS, DB[17:0], VSYNC, HSYNC, DOTCLK, ENABLE, SCL, SDI, SDO. IOVcc = 1.65 ~ 3.6V. In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.
VDD	O	Power	Digital circuit power pad. Connect these pins with the 1uF capacitor.
DGND	I	Power supply	DGND for the digital side: DGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	I	Power supply	AGND for the analog side: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VGMMMA1, 62	O	-	Test pad. Leave these pins as open
VGLDMY1~4	O	Unused gate lines	Connect unused gate lines to fix the level at VGL
<b>Test Pads</b>			
DUMMY3, 5~27,30, 31.	-	-	Dummy pad. Leave these pins as open
DUMMYR1,2, 28, 29.	-	-	Short circuited within the chip for COG contact resistance measurement. DUMMYR pins are short circuited as below: DUMMYR1 and DUMMYR29 DUMMYR2 and DUMMYR28
DUMMY	-	-	Dummy pad and no output (no gold bump)
IOVCCDUM	O		Connect unused interface and test pins to these pins on the glass to fix voltage levels. Leave open when not used.
AGNDDUM1~6	O	-	
DGNDDUM1~7	O	-	
TESTO1~16	O	Open	Test pins. Leave them open.
TEST1, 2, 3	I	IOGND	Test pins (internal pull low). Connect to GND or leave these pins as open.
TS0~8	I	OPEN	Test pins (internal pull low). Leave them open.
TSO	O	OPEN	Test pins. Leave it open or short to ground.
TEST_EN	I	OPEN	Test pins. Leave it open or short to ground.

**Liquid crystal power supply specifications Table 1**

No.	Item	Description
1	TFT Source Driver	720 pins (240 x RGB)
2	TFT Gate Driver	320 pins
3	TFT Display's Capacitor Structure	Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S720
		G1 ~ G320
		VCOM
5	Input Voltage	V0 ~ V63 grayscales
		VGH - VGL
		VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVcc
		VCI
6	Liquid Crystal Drive Voltages	1.65 ~ 3.60V
		2.50 ~ 3.60V
		DDVDH
		4.5V ~ 6.0V
		VGH
		10V ~ 20V
		VGL
-5V ~ -15V		
6	Liquid Crystal Drive Voltages	VCL
		-1.9V ~ -3.0V
		VGH - VGL
		Max. 30V
		VCI - VCL
		Max. 6.0V
		7
VCI1 x2		
VGH		
VCI1 x4, x5, x6		
7	Internal Step-up Circuits	VGL
		VCI1 x-3, x-4, x-5
		VCL
		VCI1 x-1

## 5. Pad Arrangement and Coordination

Chip Size: 18800 um x 680 um

Chip thickness : 280 um (typ.)

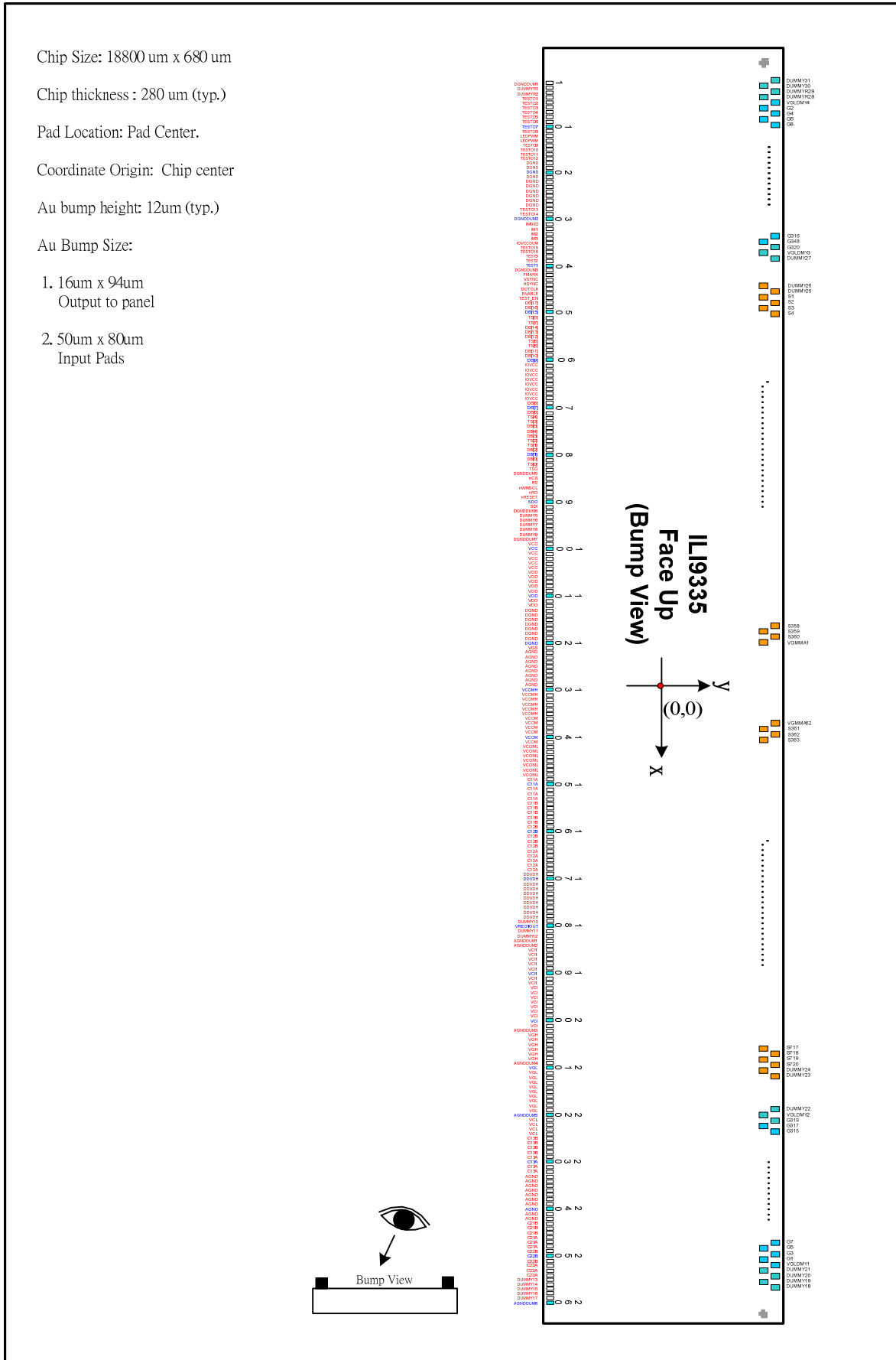
Pad Location: Pad Center.

Coordinate Origin: Chip center

Au bump height: 12um (typ.)

Au Bump Size:

1. 16um x 94um  
Output to panel
2. 50um x 80um  
Input Pads



NO.	Pad Name	X	Y	NO.	Pad Name	X	Y	NO.	Pad Name	X	Y
1	DGND	-9065	-239	61	IOVCC	-4865	-239	121	VGS	-665	-239
2	DUMMYR1	-8995	-239	62	IOVCC	-4795	-239	122	AGND	-595	-239
3	DUMMYR2	-8925	-239	63	IOVCC	-4725	-239	123	AGND	-525	-239
4	TESTO[1]	-8855	-239	64	IOVCC	-4655	-239	124	AGND	-455	-239
5	TESTO[2]	-8785	-239	65	IOVCC	-4585	-239	125	AGND	-385	-239
6	TESTO[3]	-8715	-239	66	IOVCC	-4515	-239	126	AGND	-315	-239
7	TESTO[4]	-8645	-239	67	IOVCC	-4445	-239	127	AGND	-245	-239
8	TESTO[5]	-8575	-239	68	IOVCC	-4375	-239	128	AGND	-175	-239
9	TESTO[6]	-8505	-239	69	DB[8]	-4305	-239	129	AGND	-105	-239
10	TESTO[7]	-8435	-239	70	DB[7]	-4235	-239	120	VCOMH	-35	-239
11	TESTO[8]	-8365	-239	71	DB[6]	-4165	-239	131	VCOMH	35	-239
12	DUMMY	-8295	-239	72	TS[4]	-4095	-239	132	VCOMH	105	-239
13	DUMMY	-8225	-239	73	TS[3]	-4025	-239	133	VCOMH	175	-239
14	TESTO[9]	-8155	-239	74	DB[5]	-3955	-239	134	VCOMH	245	-239
15	TESTO[10]	-8085	-239	75	DB[4]	-3885	-239	135	VCOMH	315	-239
16	TESTO[11]	-8015	-239	76	DB[3]	-3815	-239	136	VCOM	385	-239
17	TESTO[12]	-7945	-239	77	TS[2]	-3745	-239	137	VCOM	455	-239
18	DGND	-7875	-239	78	TS[1]	-3675	-239	138	VCOM	525	-239
19	DGND	-7805	-239	79	DB[2]	-3605	-239	139	VCOM	595	-239
20	DGND	-7735	-239	80	DB[1]	-3535	-239	140	VCOM	665	-239
21	DGND	-7665	-239	81	DB[0]	-3465	-239	141	VCOM	735	-239
22	DGND	-7595	-239	82	TS[0]	-3395	-239	142	VCOML	805	-239
23	DGND	-7525	-239	83	TSO	-3325	-239	143	VCOML	875	-239
24	DGND	-7455	-239	84	DGND	-3255	-239	144	VCOML	945	-239
25	DGND	-7385	-239	85	nCS	-3185	-239	145	VCOML	1015	-239
26	DGND	-7315	-239	86	RS	-3115	-239	146	VCOML	1085	-239
27	DGND	-7245	-239	87	nWR/SCL	-3045	-239	147	VCOML	1155	-239
28	TESTO[13]	-7175	-239	88	nRD	-2975	-239	148	VCOML	1225	-239
29	TESTO[14]	-7105	-239	89	nRESET	-2905	-239	149	C11A	1295	-239
30	DGND	-7035	-239	90	SDO	-2835	-239	150	C11A	1365	-239
31	IMO/ID	-6965	-239	91	SDI	-2765	-239	151	C11A	1435	-239
32	IM1	-6895	-239	92	DGND	-2695	-239	152	C11A	1505	-239
33	IM2	-6825	-239	93	DUMMY5	-2625	-239	153	C11A	1575	-239
34	IM3	-6755	-239	94	DUMMY6	-2555	-239	154	C11B	1645	-239
35	IOVCC	-6685	-239	95	DUMMY7	-2485	-239	155	C11B	1715	-239
36	TESTO[15]	-6615	-239	96	DUMMY8	-2415	-239	156	C11B	1785	-239
37	TESTO[16]	-6545	-239	97	DUMMY9	-2345	-239	157	C11B	1855	-239
38	TEST3	-6475	-239	98	DGND	-2275	-239	158	C11B	1925	-239
39	TEST2	-6405	-239	99	VCC	-2205	-239	159	C12B	1995	-239
40	TEST1	-6335	-239	100	VCC	-2135	-239	160	C12B	2065	-239
41	DGND	-6265	-239	101	VCC	-2065	-239	161	C12B	2135	-239
42	FMARK	-6195	-239	102	VCC	-1995	-239	162	C12B	2205	-239
43	VSYNC	-6125	-239	103	VCC	-1925	-239	163	C12B	2275	-239
44	HSYNC	-6055	-239	104	VCC	-1855	-239	164	C12A	2345	-239
45	DOTCLK	-5985	-239	105	VDD	-1785	-239	165	C12A	2415	-239
46	ENABLE	-5915	-239	106	VDD	-1715	-239	120	C12A	2485	-239
47	TEST_EN	-5845	-239	107	VDD	-1645	-239	167	C12A	2555	-239
48	DB[17]	-5775	-239	108	VDD	-1575	-239	168	C12A	2625	-239
49	DB[16]	-5705	-239	109	VDD	-1505	-239	169	DDVDH	2695	-239
50	DB[15]	-5635	-239	110	VDD	-1435	-239	170	DDVDH	2765	-239
51	TS[8]	-5565	-239	111	VDD	-1365	-239	171	DDVDH	2835	-239
52	TS[7]	-5495	-239	112	VDD	-1295	-239	172	DDVDH	2905	-239
53	DB[14]	-5425	-239	113	DGND	-1225	-239	173	DDVDH	2975	-239
54	DB[13]	-5355	-239	114	DGND	-1155	-239	174	DDVDH	3045	-239
55	DB[12]	-5285	-239	115	DGND	-1085	-239	175	DDVDH	3115	-239
56	TS[6]	-5215	-239	116	DGND	-1015	-239	176	DDVDH	3185	-239
57	TS[5]	-5145	-239	117	DGND	-945	-239	177	DDVDH	3255	-239
58	DB[11]	-5075	-239	118	DGND	-875	-239	178	DDVDH	3325	-239
59	DB[10]	-5005	-239	119	DGND	-805	-239	179	DUMMY10	3395	-239
60	DB[9]	-4935	-239	120	DGND	-735	-239	180	VREG1OUT	3465	-239



NO.	Pad Name	X	Y	NO.	Pad Name	X	Y	NO.	Pad Name	X	Y
181	DUMMY11	3535	-239	241	AGND	7735	-239	301	G[71]	8576	233
182	DUMMY12	3605	-239	242	AGND	7805	-239	302	G[73]	8560	120
183	AGNDDUM1	3675	-239	233	C21B	7875	-239	303	G[75]	8544	233
184	AGNDDUM2	3745	-239	244	C21B	7945	-239	304	G[77]	8528	120
185	VCI1	3815	-239	245	C21B	8015	-239	305	G[79]	8512	233
186	VCI1	3885	-239	246	C21A	8085	-239	306	G[81]	8496	120
187	VCI1	3955	-239	247	C21A	8155	-239	307	G[83]	8480	233
188	VCI1	4025	-239	248	C21A	8225	-239	308	G[85]	8464	120
189	VCI1	4095	-239	249	C22B	8295	-239	309	G[87]	8448	233
190	VCI1	4165	-239	250	C22B	8365	-239	310	G[89]	8432	120
191	VCI1	4235	-239	251	C22B	8435	-239	311	G[91]	8416	233
192	VCI1	4305	-239	252	C22A	8505	-239	312	G[93]	8400	120
193	VCI	4375	-239	253	C22A	8575	-239	313	G[95]	8384	233
194	VCI	4445	-239	254	C22A	8645	-239	314	G[97]	8368	120
195	VCI	4515	-239	255	DUMMY13	8715	-239	315	G[99]	8352	233
196	VCI	4585	-239	256	DUMMY14	8785	-239	316	G[101]	8336	120
197	VCI	4655	-239	257	DUMMY15	8855	-239	317	G[103]	8320	233
198	VCI	4725	-239	258	DUMMY16	8925	-239	318	G[105]	8304	120
199	VCI	4795	-239	259	DUMMY17	8995	-239	319	G[107]	8288	233
200	VCI	4865	-239	260	AGNDDUM6	9065	-239	320	G[109]	8272	120
201	VCI	4935	-239	261	DUMMY18	9216	233	321	G[111]	8256	233
202	AGNDDUM3	5005	-239	262	DUMMY19	9200	120	322	G[113]	8240	120
203	VGH	5075	-239	263	DUMMY20	9184	233	323	G[115]	8224	233
204	VGH	5145	-239	264	DUMMY21	9168	120	324	G[117]	8208	120
205	VGH	5215	-239	265	VGLDMY1	9152	233	325	G[119]	8192	233
206	VGH	5285	-239	266	G[1]	9136	120	326	G[121]	8176	120
207	VGH	5355	-239	267	G[3]	9120	233	327	G[123]	8160	233
208	VGH	5425	-239	268	G[5]	9104	120	328	G[125]	8144	120
209	AGNDDUM4	5495	-239	269	G[7]	9088	233	329	G[127]	8128	233
210	VGL	5565	-239	270	G[9]	9072	120	330	G[129]	8112	120
211	VGL	5635	-239	271	G[11]	9056	233	331	G[131]	8096	233
212	VGL	5705	-239	272	G[13]	9040	120	332	G[133]	8080	120
213	VGL	5775	-239	273	G[15]	9024	233	333	G[135]	8064	233
214	VGL	5845	-239	274	G[17]	9008	120	334	G[137]	8048	120
215	VGL	5915	-239	275	G[19]	8992	233	335	G[139]	8032	233
216	VGL	5985	-239	276	G[21]	8976	120	336	G[141]	8016	120
217	VGL	6055	-239	277	G[23]	8960	233	337	G[143]	8000	233
218	VGL	6125	-239	278	G[25]	8944	120	338	G[145]	7984	120
219	VGL	6195	-239	233	G[27]	8928	233	339	G[147]	7968	233
220	AGNDDUM5	6265	-239	280	G[29]	8912	120	340	G[149]	7952	120
221	VCL	6335	-239	281	G[31]	8896	233	341	G[151]	7936	233
222	VCL	6405	-239	282	G[33]	8880	120	342	G[153]	7920	120
223	VCL	6475	-239	283	G[35]	8864	233	343	G[155]	7904	233
224	VCL	6545	-239	284	G[37]	8848	120	344	G[157]	7888	120
225	C13B	6615	-239	285	G[39]	8832	233	345	G[159]	7872	233
226	C13B	6685	-239	286	G[41]	8816	120	346	G[161]	7856	120
227	C13B	6755	-239	287	G[43]	8800	233	347	G[163]	7840	233
228	C13B	6825	-239	288	G[45]	8784	120	348	G[165]	7824	120
229	C13A	6895	-239	289	G[47]	8768	233	349	G[167]	7808	233
230	C13A	6965	-239	290	G[49]	8752	120	350	G[169]	7792	120
231	C13A	7035	-239	291	G[51]	8736	233	351	G[171]	7776	233
232	C13A	7105	-239	292	G[53]	8720	120	352	G[173]	7760	120
233	AGND	7175	-239	293	G[55]	8704	233	353	G[175]	7744	233
234	AGND	7245	-239	294	G[57]	8688	120	354	G[177]	7728	120
235	AGND	7315	-239	295	G[59]	8672	233	355	G[179]	7712	233
236	AGND	7385	-239	296	G[61]	8656	120	356	G[181]	7696	120
237	AGND	7455	-239	297	G[63]	8640	233	357	G[183]	7680	233
238	AGND	7525	-239	298	G[65]	8624	120	358	G[185]	7664	120
239	AGND	7595	-239	299	G[67]	8608	233	359	G[187]	7648	233
240	AGND	7665	-239	300	G[69]	8592	120	360	G[189]	7632	120

NO.	Pad Name	X	Y	NO.	Pad Name	X	Y	NO.	Pad Name	X	Y
361	G[191]	7616	233	421	G[311]	6656	233	481	S[669]	5520	120
362	G[193]	7600	120	422	G[313]	6640	120	482	S[668]	5504	233
363	G[195]	7584	233	423	G[315]	6624	233	483	S[667]	5488	120
364	G[197]	7568	120	424	G[317]	6608	120	484	S[666]	5472	233
365	G[199]	7552	233	425	G[319]	6592	233	485	S[665]	5456	120
366	G[201]	7536	120	426	VGLDMY2	6576	120	486	S[664]	5440	233
367	G[203]	7520	233	427	DUMMY22	6560	233	487	S[663]	5424	120
368	G[205]	7504	120	428	DUMMY23	6368	233	488	S[662]	5408	233
369	G[207]	7488	233	429	DUMMY24	6352	120	489	S[661]	5392	120
370	G[209]	7472	120	430	S[720]	6336	233	490	S[660]	5376	233
371	G[211]	7456	233	431	S[719]	6320	120	491	S[659]	5360	120
372	G[213]	7440	120	432	S[718]	6304	233	492	S[658]	5344	233
373	G[215]	7424	233	433	S[717]	6288	120	493	S[657]	5328	120
374	G[217]	7408	120	434	S[716]	6272	233	494	S[656]	5312	233
375	G[219]	7392	233	435	S[715]	6256	120	495	S[655]	5296	120
376	G[221]	7376	120	436	S[714]	6240	233	496	S[654]	5280	233
377	G[223]	7360	233	437	S[713]	6224	120	497	S[653]	5264	120
378	G[225]	7344	120	438	S[712]	6208	233	498	S[652]	5248	233
379	G[227]	7328	233	439	S[711]	6192	120	499	S[651]	5232	120
380	G[229]	7312	120	440	S[710]	6176	233	500	S[650]	5216	233
381	G[231]	7296	233	441	S[709]	6160	120	501	S[649]	5200	120
382	G[233]	7280	120	442	S[708]	6144	233	502	S[648]	5184	233
383	G[235]	7264	233	443	S[707]	6128	120	503	S[647]	5168	120
384	G[237]	7248	120	444	S[706]	6112	233	504	S[646]	5152	233
385	G[239]	7232	233	445	S[705]	6096	120	505	S[645]	5136	120
386	G[241]	7216	120	446	S[704]	6080	233	506	S[644]	5120	233
387	G[233]	7200	233	447	S[703]	6064	120	507	S[643]	5104	120
388	G[245]	7184	120	448	S[702]	6048	233	508	S[642]	5088	233
389	G[247]	7168	233	449	S[701]	6032	120	509	S[641]	5072	120
390	G[249]	7152	120	450	S[700]	6016	233	510	S[640]	5056	233
391	G[251]	7136	233	451	S[699]	6000	120	511	S[639]	5040	120
392	G[253]	7120	120	452	S[698]	5984	233	512	S[638]	5024	233
393	G[255]	7104	233	453	S[697]	5968	120	513	S[637]	5008	120
394	G[257]	7088	120	454	S[696]	5952	233	514	S[636]	4992	233
395	G[259]	7072	233	455	S[695]	5936	120	515	S[635]	4976	120
396	G[261]	7056	120	456	S[694]	5920	233	516	S[634]	4960	233
397	G[263]	7040	233	457	S[693]	5904	120	517	S[633]	4944	120
398	G[265]	7024	120	458	S[692]	5888	233	518	S[632]	4928	233
399	G[267]	7008	233	459	S[691]	5872	120	519	S[631]	4912	120
400	G[269]	6992	120	460	S[690]	5856	233	520	S[630]	4896	233
401	G[271]	6976	233	461	S[689]	5840	120	521	S[629]	4880	120
402	G[273]	6960	120	462	S[688]	5824	233	522	S[628]	4864	233
403	G[275]	6944	233	463	S[687]	5808	120	523	S[627]	4848	120
404	G[277]	6928	120	464	S[686]	5792	233	524	S[626]	4832	233
405	G[233]	6912	233	465	S[685]	5776	120	525	S[625]	4816	120
406	G[281]	6896	120	466	S[684]	5760	233	526	S[624]	4800	233
407	G[283]	6880	233	467	S[683]	5744	120	527	S[623]	4784	120
408	G[285]	6864	120	468	S[682]	5728	233	528	S[622]	4768	233
409	G[287]	6848	233	469	S[681]	5712	120	529	S[621]	4752	120
410	G[289]	6832	120	470	S[680]	5696	233	530	S[620]	4736	233
411	G[291]	6816	233	471	S[679]	5680	120	531	S[619]	4720	120
412	G[293]	6800	120	472	S[678]	5664	233	532	S[618]	4704	233
413	G[295]	6784	233	473	S[677]	5648	120	533	S[617]	4688	120
414	G[297]	6768	120	474	S[676]	5632	233	534	S[616]	4672	233
415	G[299]	6752	233	475	S[675]	5616	120	535	S[615]	4656	120
416	G[301]	6736	120	476	S[674]	5600	233	536	S[614]	4640	233
417	G[303]	6720	233	477	S[673]	5584	120	537	S[613]	4624	120
418	G[305]	6704	120	478	S[672]	5568	233	538	S[612]	4608	233
419	G[307]	6688	233	479	S[671]	5552	120	539	S[611]	4592	120
420	G[309]	6672	120	480	S[670]	5536	233	540	S[610]	4576	233

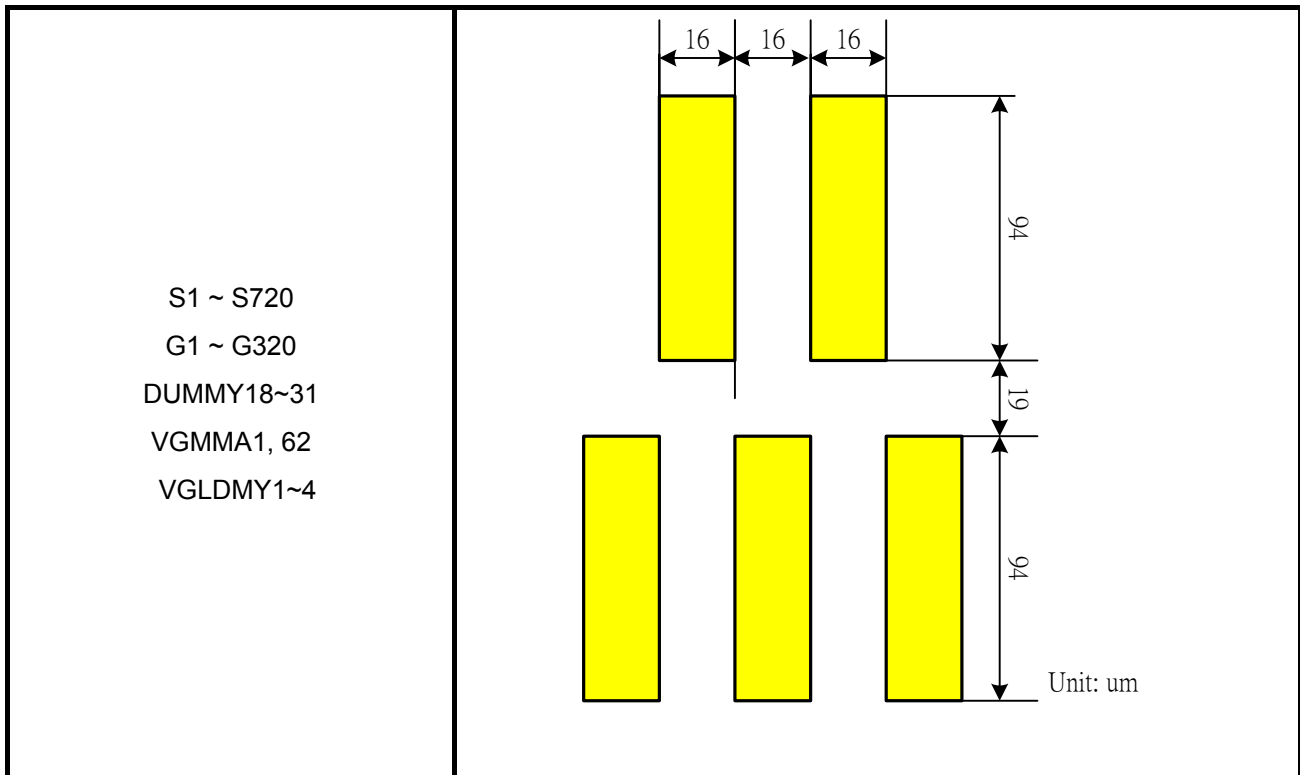
NO.	Pad Name	X	Y	NO.	Pad Name	X	Y	NO.	Pad Name	X	Y
541	S[609]	4560	120	601	S[549]	3600	120	661	S[489]	2640	120
542	S[608]	4544	233	602	S[548]	3584	233	662	S[488]	2624	233
543	S[607]	4528	120	603	S[547]	3568	120	663	S[487]	2608	120
544	S[606]	4512	233	604	S[546]	3552	233	664	S[486]	2592	233
545	S[605]	4496	120	605	S[545]	3536	120	665	S[485]	2576	120
546	S[604]	4480	233	606	S[544]	3520	233	666	S[484]	2560	233
547	S[603]	4464	120	607	S[543]	3504	120	667	S[483]	2544	120
548	S[602]	4448	233	608	S[542]	3488	233	668	S[482]	2528	233
549	S[601]	4432	120	609	S[541]	3472	120	669	S[481]	2512	120
550	S[600]	4416	233	610	S[540]	3456	233	670	S[480]	2496	233
551	S[599]	4400	120	611	S[539]	3440	120	671	S[479]	2480	120
552	S[598]	4384	233	612	S[538]	3424	233	672	S[478]	2464	233
553	S[597]	4368	120	613	S[537]	3408	120	673	S[477]	2448	120
554	S[596]	4352	233	614	S[536]	3392	233	674	S[476]	2432	233
555	S[595]	4336	120	615	S[535]	3376	120	675	S[475]	2416	120
556	S[594]	4320	233	616	S[534]	3360	233	676	S[474]	2400	233
557	S[593]	4304	120	617	S[533]	3344	120	677	S[473]	2384	120
558	S[592]	4288	233	618	S[532]	3328	233	678	S[472]	2368	233
559	S[591]	4272	120	619	S[531]	3312	120	679	S[471]	2352	120
560	S[590]	4256	233	620	S[530]	3296	233	680	S[470]	2336	233
561	S[589]	4240	120	621	S[529]	3280	120	681	S[469]	2320	120
562	S[588]	4224	233	622	S[528]	3264	233	682	S[468]	2304	233
563	S[587]	4208	120	623	S[527]	3248	120	683	S[467]	2288	120
564	S[586]	4192	233	624	S[526]	3232	233	684	S[466]	2272	233
565	S[585]	4176	120	625	S[525]	3216	120	685	S[465]	2256	120
566	S[584]	4160	233	626	S[524]	3200	233	686	S[464]	2240	233
567	S[583]	4144	120	627	S[523]	3184	120	687	S[463]	2224	120
568	S[582]	4128	233	628	S[522]	3168	233	688	S[462]	2208	233
569	S[581]	4112	120	629	S[521]	3152	120	689	S[461]	2192	120
570	S[580]	4096	233	630	S[520]	3136	233	690	S[460]	2176	233
571	S[579]	4080	120	631	S[519]	3120	120	691	S[459]	2160	120
572	S[578]	4064	233	632	S[518]	3104	233	692	S[458]	2144	233
573	S[577]	4048	120	633	S[517]	3088	120	693	S[457]	2128	120
574	S[576]	4032	233	634	S[516]	3072	233	694	S[456]	2112	233
575	S[575]	4016	120	635	S[515]	3056	120	695	S[455]	2096	120
576	S[574]	4000	233	636	S[514]	3040	233	696	S[454]	2080	233
577	S[573]	3984	120	637	S[513]	3024	120	697	S[453]	2064	120
578	S[572]	3968	233	638	S[512]	3008	233	698	S[452]	2048	233
579	S[571]	3952	120	639	S[511]	2992	120	699	S[451]	2032	120
580	S[570]	3936	233	640	S[510]	2976	233	700	S[450]	2016	233
581	S[569]	3920	120	641	S[509]	2960	120	701	S[449]	2000	120
582	S[568]	3904	233	642	S[508]	2944	233	702	S[448]	1984	233
583	S[567]	3888	120	643	S[507]	2928	120	703	S[447]	1968	120
584	S[566]	3872	233	644	S[506]	2912	233	704	S[446]	1952	233
585	S[565]	3856	120	645	S[505]	2896	120	705	S[445]	1936	120
586	S[564]	3840	233	646	S[504]	2880	233	706	S[444]	1920	233
587	S[563]	3824	120	647	S[503]	2864	120	707	S[443]	1904	120
588	S[562]	3808	233	648	S[502]	2848	233	708	S[442]	1888	233
589	S[561]	3792	120	649	S[501]	2832	120	709	S[441]	1872	120
590	S[560]	3776	233	650	S[500]	2816	233	710	S[440]	1856	233
591	S[559]	3760	120	651	S[499]	2800	120	711	S[439]	1840	120
592	S[558]	3744	233	652	S[498]	2784	233	712	S[438]	1824	233
593	S[557]	3728	120	653	S[497]	2768	120	713	S[437]	1808	120
594	S[556]	3712	233	654	S[496]	2752	233	714	S[436]	1792	233
595	S[555]	3696	120	655	S[495]	2736	120	715	S[435]	1776	120
596	S[554]	3680	233	656	S[494]	2720	233	716	S[434]	1760	233
597	S[553]	3664	120	657	S[493]	2704	120	717	S[433]	1744	120
598	S[552]	3648	233	658	S[492]	2688	233	718	S[432]	1728	233
599	S[551]	3632	120	659	S[491]	2672	120	719	S[431]	1712	120
600	S[550]	3616	233	660	S[490]	2656	233	720	S[430]	1696	233

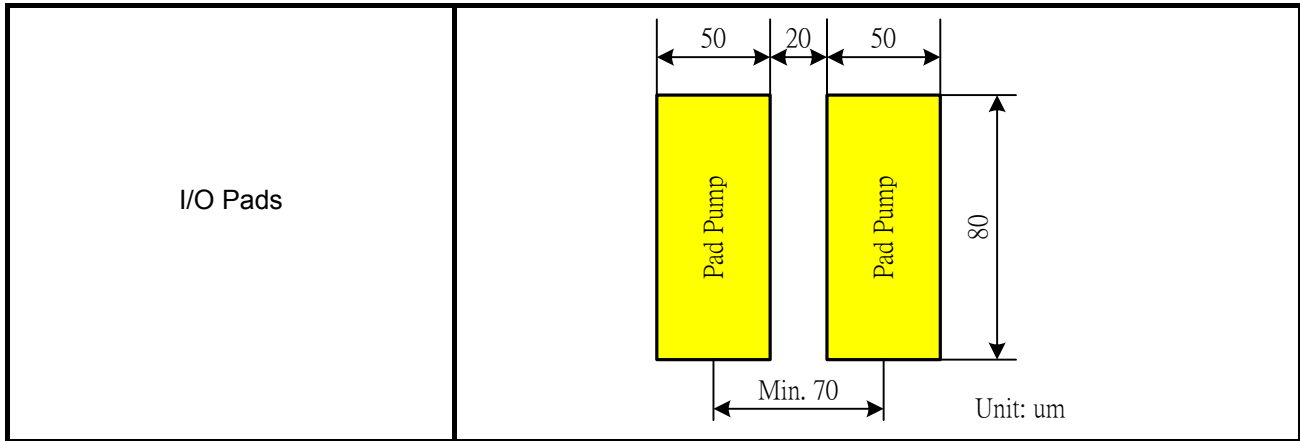
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722	S[428]	1664	233	782	S[368]	704	233	842	S[310]	-1392	233
723	S[427]	1648	120	783	S[367]	688	120	843	S[309]	-1408	120
724	S[426]	1632	233	784	S[366]	672	233	844	S[308]	-1424	233
725	S[425]	1616	120	785	S[365]	656	120	845	S[307]	-1440	120
726	S[424]	1600	233	786	S[364]	640	233	846	S[306]	-1456	233
727	S[423]	1584	120	787	S[363]	624	120	847	S[305]	-1472	120
728	S[422]	1568	233	788	S[362]	608	233	848	S[304]	-1488	233
729	S[421]	1552	120	789	S[361]	592	120	849	S[303]	-1504	120
730	S[420]	1536	233	790	VGMMMA62	576	233	850	S[302]	-1520	233
731	S[419]	1520	120	791	VGMMMA1	-576	120	851	S[301]	-1536	120
732	S[418]	1504	233	792	S[360]	-592	233	852	S[300]	-1552	233
733	S[417]	1488	120	793	S[359]	-608	120	853	S[299]	-1568	120
734	S[416]	1472	233	794	S[358]	-624	233	854	S[298]	-1584	233
735	S[415]	1456	120	795	S[357]	-640	120	855	S[297]	-1600	120
736	S[414]	1440	233	796	S[356]	-656	233	856	S[296]	-1616	233
737	S[413]	1424	120	797	S[355]	-672	120	857	S[295]	-1632	120
738	S[412]	1408	233	798	S[354]	-688	233	858	S[294]	-1648	233
739	S[411]	1392	120	799	S[353]	-704	120	859	S[293]	-1664	120
740	S[410]	1376	233	800	S[352]	-720	233	860	S[292]	-1680	233
741	S[409]	1360	120	801	S[351]	-736	120	861	S[291]	-1696	120
742	S[408]	1344	233	802	S[350]	-752	233	862	S[290]	-1712	233
743	S[407]	1328	120	803	S[349]	-768	120	863	S[289]	-1728	120
744	S[406]	1312	233	804	S[348]	-784	233	864	S[288]	-1744	233
745	S[405]	1296	120	805	S[347]	-800	120	865	S[287]	-1760	120
746	S[404]	1280	233	806	S[346]	-816	233	866	S[286]	-1776	233
747	S[403]	1264	120	807	S[345]	-832	120	867	S[285]	-1792	120
748	S[402]	1248	233	808	S[344]	-848	233	868	S[284]	-1808	233
749	S[401]	1232	120	809	S[343]	-864	120	869	S[283]	-1824	120
750	S[400]	1216	233	810	S[342]	-880	233	870	S[282]	-1840	233
751	S[399]	1200	120	811	S[341]	-896	120	871	S[281]	-1856	120
752	S[398]	1184	233	812	S[340]	-912	233	872	S[280]	-1872	233
753	S[397]	1168	120	813	S[339]	-928	120	873	S[233]	-1888	120
754	S[396]	1152	233	814	S[338]	-944	233	874	S[278]	-1904	233
755	S[395]	1136	120	815	S[337]	-960	120	875	S[277]	-1920	120
756	S[394]	1120	233	816	S[336]	-976	233	876	S[276]	-1936	233
757	S[393]	1104	120	817	S[335]	-992	120	877	S[275]	-1952	120
758	S[392]	1088	233	818	S[334]	-1008	233	878	S[274]	-1968	233
759	S[391]	1072	120	819	S[333]	-1024	120	879	S[273]	-1984	120
760	S[390]	1056	233	820	S[332]	-1040	233	880	S[272]	-2000	233
761	S[389]	1040	120	821	S[331]	-1056	120	881	S[271]	-2016	120
762	S[388]	1024	233	822	S[330]	-1072	233	882	S[270]	-2032	233
763	S[387]	1008	120	823	S[329]	-1088	120	883	S[269]	-2048	120
764	S[386]	992	233	824	S[328]	-1104	233	884	S[268]	-2064	233
765	S[385]	976	120	825	S[327]	-1120	120	885	S[267]	-2080	120
766	S[384]	960	233	826	S[326]	-1136	233	886	S[266]	-2096	233
767	S[383]	944	120	827	S[325]	-1152	120	887	S[265]	-2112	120
768	S[382]	928	233	828	S[324]	-1168	233	888	S[264]	-2128	233
769	S[381]	912	120	829	S[323]	-1184	120	889	S[263]	-2144	120
770	S[380]	896	233	830	S[322]	-1200	233	890	S[262]	-2160	233
771	S[379]	880	120	831	S[321]	-1216	120	891	S[261]	-2176	120
772	S[378]	864	233	832	S[320]	-1232	233	892	S[260]	-2192	233
773	S[377]	848	120	833	S[319]	-1248	120	893	S[259]	-2208	120
774	S[376]	832	233	834	S[318]	-1264	233	894	S[258]	-2224	233
775	S[375]	816	120	835	S[317]	-1280	120	895	S[257]	-2240	120
776	S[374]	800	233	836	S[316]	-1296	233	896	S[256]	-2256	233
777	S[373]	784	120	837	S[315]	-1312	120	897	S[255]	-2272	120
778	S[372]	768	233	838	S[314]	-1328	233	898	S[254]	-2288	233
779	S[371]	752	120	839	S[313]	-1344	120	899	S[253]	-2304	120
780	S[370]	736	233	840	S[312]	-1360	233	900	S[252]	-2320	233

NO.	Pad Name	X	Y	NO.	Pad Name	X	Y	NO.	Pad Name	X	Y
901	S[251]	-2336	120	961	S[191]	-3296	120	1021	S[131]	-4256	120
902	S[250]	-2352	233	962	S[190]	-3312	233	1022	S[120]	-4272	233
903	S[249]	-2368	120	963	S[189]	-3328	120	1023	S[129]	-4288	120
904	S[248]	-2384	233	964	S[188]	-3344	233	1024	S[128]	-4304	233
905	S[247]	-2400	120	965	S[187]	-3360	120	1025	S[127]	-4320	120
906	S[246]	-2416	233	966	S[186]	-3376	233	1026	S[126]	-4336	233
907	S[245]	-2432	120	967	S[185]	-3392	120	1027	S[125]	-4352	120
908	S[244]	-2448	233	968	S[184]	-3408	233	1028	S[124]	-4368	233
909	S[233]	-2464	120	969	S[183]	-3424	120	1029	S[123]	-4384	120
910	S[242]	-2480	233	970	S[182]	-3440	233	1030	S[122]	-4400	233
911	S[241]	-2496	120	971	S[181]	-3456	120	1031	S[121]	-4416	120
912	S[240]	-2512	233	972	S[180]	-3472	233	1032	S[120]	-4432	233
913	S[239]	-2528	120	973	S[179]	-3488	120	1033	S[119]	-4448	120
914	S[238]	-2544	233	974	S[178]	-3504	233	1034	S[118]	-4464	233
915	S[237]	-2560	120	975	S[177]	-3520	120	1035	S[117]	-4480	120
916	S[236]	-2576	233	976	S[176]	-3536	233	1036	S[116]	-4496	233
917	S[235]	-2592	120	977	S[175]	-3552	120	1037	S[115]	-4512	120
918	S[234]	-2608	233	978	S[174]	-3568	233	1038	S[114]	-4528	233
919	S[233]	-2624	120	979	S[173]	-3584	120	1039	S[113]	-4544	120
920	S[232]	-2640	233	980	S[172]	-3600	233	1040	S[112]	-4560	233
921	S[231]	-2656	120	981	S[171]	-3616	120	1041	S[111]	-4576	120
922	S[230]	-2672	233	982	S[170]	-3632	233	1042	S[110]	-4592	233
923	S[229]	-2688	120	983	S[169]	-3648	120	1043	S[109]	-4608	120
924	S[228]	-2704	233	984	S[168]	-3664	233	1044	S[108]	-4624	233
925	S[227]	-2720	120	985	S[167]	-3680	120	1045	S[107]	-4640	120
926	S[226]	-2736	233	986	S[120]	-3696	233	1046	S[106]	-4656	233
927	S[225]	-2752	120	987	S[165]	-3712	120	1047	S[105]	-4672	120
928	S[224]	-2768	233	988	S[164]	-3728	233	1048	S[104]	-4688	233
929	S[223]	-2784	120	989	S[163]	-3744	120	1049	S[103]	-4704	120
930	S[222]	-2800	233	990	S[162]	-3760	233	1050	S[102]	-4720	233
931	S[221]	-2816	120	991	S[161]	-3776	120	1051	S[101]	-4736	120
932	S[220]	-2832	233	992	S[160]	-3792	233	1052	S[100]	-4752	233
933	S[219]	-2848	120	993	S[159]	-3808	120	1053	S[99]	-4768	120
934	S[218]	-2864	233	994	S[158]	-3824	233	1054	S[98]	-4784	233
935	S[217]	-2880	120	995	S[157]	-3840	120	1055	S[97]	-4800	120
936	S[216]	-2896	233	996	S[156]	-3856	233	1056	S[96]	-4816	233
937	S[215]	-2912	120	997	S[155]	-3872	120	1057	S[95]	-4832	120
938	S[214]	-2928	233	998	S[154]	-3888	233	1058	S[94]	-4848	233
939	S[213]	-2944	120	999	S[153]	-3904	120	1059	S[93]	-4864	120
940	S[212]	-2960	233	1000	S[152]	-3920	233	1060	S[92]	-4880	233
941	S[211]	-2976	120	1001	S[151]	-3936	120	1061	S[91]	-4896	120
942	S[210]	-2992	233	1002	S[150]	-3952	233	1062	S[90]	-4912	233
943	S[209]	-3008	120	1003	S[149]	-3968	120	1063	S[89]	-4928	120
944	S[208]	-3024	233	1004	S[148]	-3984	233	1064	S[88]	-4944	233
945	S[207]	-3040	120	1005	S[147]	-4000	120	1065	S[87]	-4960	120
946	S[206]	-3056	233	1006	S[146]	-4016	233	1066	S[86]	-4976	233
947	S[205]	-3072	120	1007	S[145]	-4032	120	1067	S[85]	-4992	120
948	S[204]	-3088	233	1008	S[144]	-4048	233	1068	S[84]	-5008	233
949	S[203]	-3104	120	1009	S[143]	-4064	120	1069	S[83]	-5024	120
950	S[202]	-3120	233	1010	S[142]	-4080	233	1070	S[82]	-5040	233
951	S[201]	-3136	120	1011	S[141]	-4096	120	1071	S[81]	-5056	120
952	S[200]	-3152	233	1012	S[140]	-4112	233	1072	S[80]	-5072	233
953	S[199]	-3168	120	1013	S[139]	-4128	120	1073	S[79]	-5088	120
954	S[198]	-3184	233	1014	S[138]	-4144	233	1074	S[78]	-5104	233
955	S[197]	-3200	120	1015	S[137]	-4160	120	1075	S[77]	-5120	120
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957	S[195]	-3232	120	1017	S[135]	-4192	120	1077	S[75]	-5152	120
958	S[194]	-3248	233	1018	S[134]	-4208	233	1078	S[74]	-5168	233
959	S[193]	-3264	120	1019	S[133]	-4224	120	1079	S[73]	-5184	120
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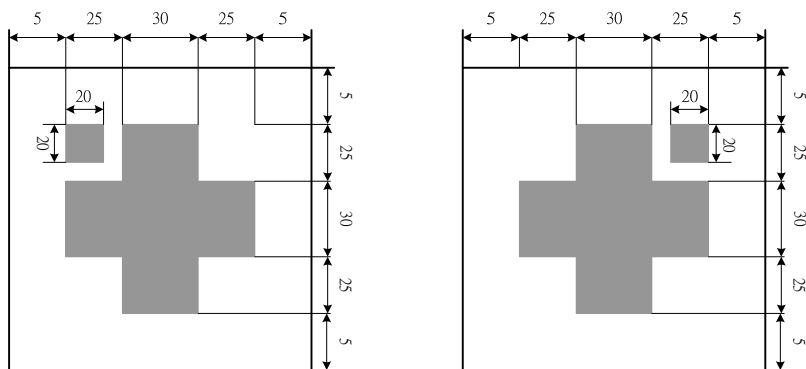
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1082	S[70]	-5232	233	1142	S[10]	-6192	233	1202	G[228]	-7328	233
1083	S[69]	-5248	120	1143	S[9]	-6208	120	1203	G[226]	-7344	120
1084	S[68]	-5264	233	1144	S[8]	-6224	233	1204	G[224]	-7360	233
1085	S[67]	-5280	120	1145	S[7]	-6240	120	1205	G[222]	-7376	120
1086	S[66]	-5296	233	1146	S[6]	-6256	233	1206	G[220]	-7392	233
1087	S[65]	-5312	120	1147	S[5]	-6272	120	1207	G[218]	-7408	120
1088	S[64]	-5328	233	1148	S[4]	-6288	233	1208	G[216]	-7424	233
1089	S[63]	-5344	120	1149	S[3]	-6304	120	1209	G[214]	-7440	120
1090	S[62]	-5360	233	1150	S[2]	-6320	233	1210	G[212]	-7456	233
1091	S[61]	-5376	120	1151	S[1]	-6336	120	1211	G[210]	-7472	120
1092	S[60]	-5392	233	1152	DUMMY25	-6352	233	1212	G[208]	-7488	233
1093	S[59]	-5408	120	1153	DUMMY26	-6368	120	1213	G[206]	-7504	120
1094	S[58]	-5424	233	1154	DUMMY27	-6560	233	1214	G[204]	-7520	233
1095	S[57]	-5440	120	1155	VGLDMY3	-6576	120	1215	G[202]	-7536	120
1096	S[56]	-5456	233	1156	G[320]	-6592	233	1216	G[200]	-7552	233
1097	S[55]	-5472	120	1157	G[318]	-6608	120	1217	G[198]	-7568	120
1098	S[54]	-5488	233	1158	G[316]	-6624	233	1218	G[196]	-7584	233
1099	S[53]	-5504	120	1159	G[314]	-6640	120	1219	G[194]	-7600	120
1100	S[52]	-5520	233	1160	G[312]	-6656	233	1220	G[192]	-7616	233
1101	S[51]	-5536	120	1161	G[310]	-6672	120	1221	G[190]	-7632	120
1102	S[50]	-5552	233	1162	G[308]	-6688	233	1222	G[188]	-7648	233
1103	S[49]	-5568	120	1163	G[306]	-6704	120	1223	G[186]	-7664	120
1104	S[48]	-5584	233	1164	G[304]	-6720	233	1224	G[184]	-7680	233
1105	S[47]	-5600	120	1165	G[302]	-6736	120	1225	G[182]	-7696	120
1106	S[46]	-5616	233	1120	G[300]	-6752	233	1226	G[180]	-7712	233
1107	S[45]	-5632	120	1167	G[298]	-6768	120	1227	G[178]	-7728	120
1108	S[44]	-5648	233	1168	G[296]	-6784	233	1228	G[176]	-7744	233
1109	S[43]	-5664	120	1169	G[294]	-6800	120	1229	G[174]	-7760	120
1110	S[42]	-5680	233	1170	G[292]	-6816	233	1230	G[172]	-7776	233
1111	S[41]	-5696	120	1171	G[290]	-6832	120	1231	G[170]	-7792	120
1112	S[40]	-5712	233	1172	G[288]	-6848	233	1232	G[168]	-7808	233
1113	S[39]	-5728	120	1173	G[286]	-6864	120	1233	G[120]	-7824	120
1114	S[38]	-5744	233	1174	G[284]	-6880	233	1234	G[164]	-7840	233
1115	S[37]	-5760	120	1175	G[282]	-6896	120	1235	G[162]	-7856	120
1116	S[36]	-5776	233	1176	G[280]	-6912	233	1236	G[160]	-7872	233
1117	S[35]	-5792	120	1177	G[278]	-6928	120	1237	G[158]	-7888	120
1118	S[34]	-5808	233	1178	G[276]	-6944	233	1238	G[156]	-7904	233
1119	S[33]	-5824	120	1179	G[274]	-6960	120	1239	G[154]	-7920	120
1120	S[32]	-5840	233	1180	G[272]	-6976	233	1240	G[152]	-7936	233
1121	S[31]	-5856	120	1181	G[270]	-6992	120	1241	G[150]	-7952	120
1122	S[30]	-5872	233	1182	G[268]	-7008	233	1242	G[148]	-7968	233
1123	S[29]	-5888	120	1183	G[266]	-7024	120	1233	G[146]	-7984	120
1124	S[28]	-5904	233	1184	G[264]	-7040	233	1244	G[144]	-8000	233
1125	S[27]	-5920	120	1185	G[262]	-7056	120	1245	G[142]	-8016	120
1126	S[26]	-5936	233	1186	G[260]	-7072	233	1246	G[140]	-8032	233
1127	S[25]	-5952	120	1187	G[258]	-7088	120	1247	G[138]	-8048	120
1128	S[24]	-5968	233	1188	G[256]	-7104	233	1248	G[136]	-8064	233
1129	S[23]	-5984	120	1189	G[254]	-7120	120	1249	G[134]	-8080	120
1120	S[22]	-6000	233	1190	G[252]	-7136	233	1250	G[132]	-8096	233
1131	S[21]	-6016	120	1191	G[250]	-7152	120	1251	G[120]	-8112	120
1132	S[20]	-6032	233	1192	G[248]	-7168	233	1252	G[128]	-8128	233
1133	S[19]	-6048	120	1193	G[246]	-7184	120	1253	G[126]	-8144	120
1134	S[18]	-6064	233	1194	G[244]	-7200	233	1254	G[124]	-8160	233
1135	S[17]	-6080	120	1195	G[242]	-7216	120	1255	G[122]	-8176	120
1136	S[16]	-6096	233	1196	G[240]	-7232	233	1256	G[120]	-8192	233
1137	S[15]	-6112	120	1197	G[238]	-7248	120	1257	G[118]	-8208	120
1138	S[14]	-6128	233	1198	G[236]	-7264	233	1258	G[116]	-8224	233
1139	S[13]	-6144	120	1199	G[234]	-7280	120	1259	G[114]	-8240	120
1140	S[12]	-6160	233	1200	G[232]	-7296	233	1260	G[112]	-8256	233

NO.	Pad Name	X	Y	NO.	Pad Name	X	Y	NO.	Pad Name	X	Y
1261	G[110]	-8272	120	1281	G[70]	-8592	120	1201	G[30]	-8912	120
1262	G[108]	-8288	233	1282	G[68]	-8608	233	1202	G[28]	-8928	233
1263	G[106]	-8304	120	1283	G[66]	-8624	120	1203	G[26]	-8944	120
1264	G[104]	-8320	233	1284	G[64]	-8640	233	1204	G[24]	-8960	233
1265	G[102]	-8336	120	1285	G[62]	-8656	120	1205	G[22]	-8976	120
1266	G[100]	-8352	233	1286	G[60]	-8672	233	1206	G[20]	-8992	233
1267	G[98]	-8368	120	1287	G[58]	-8688	120	1207	G[18]	-9008	120
1268	G[96]	-8384	233	1288	G[56]	-8704	233	1208	G[16]	-9024	233
1269	G[94]	-8400	120	1289	G[54]	-8720	120	1209	G[14]	-9040	120
1270	G[92]	-8416	233	1290	G[52]	-8736	233	1310	G[12]	-9056	233
1271	G[90]	-8432	120	1291	G[50]	-8752	120	1311	G[10]	-9072	120
1272	G[88]	-8448	233	1292	G[48]	-8768	233	1312	G[8]	-9088	233
1273	G[86]	-8464	120	1293	G[46]	-8784	120	1313	G[6]	-9104	120
1274	G[84]	-8480	233	1294	G[44]	-8800	233	1314	G[4]	-9120	233
1275	G[82]	-8496	120	1295	G[42]	-8816	120	1315	G[2]	-9136	120
1276	G[80]	-8512	233	1296	G[40]	-8832	233	1316	VGLDMY4	-9152	233
1277	G[78]	-8528	120	1297	G[38]	-8848	120	1317	DUMMYR28	-9168	120
1278	G[76]	-8544	233	1298	G[36]	-8864	233	1318	DUMMYR29	-9184	233
1233	G[74]	-8560	120	1299	G[34]	-8880	120	1319	DUMMY30	-9200	120
1280	G[72]	-8576	233	1200	G[32]	-8896	233	1320	DUMMY31	-9216	233





Alignment mark



Alignment Mark: 1 (Left)

Alignment Mark: 2 (Right)

Alignment mark	X	Y
1	-9301	226
2	9301	226



## 6. Block Description

### MPU System Interface

ILI9335 supports three system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9335 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9335 read the first data from the internal GRAM. Valid data are read out after the ILI9335 performs the second read operation.

Registers are written consecutively as the register execution time.

Registers selection by system interface (8-/9-/16-/18-bit bus width)			
Function	I80		
	RS	nWR	nRD
Write an index to IR register	0	0	1
Write to control registers or the internal GRAM by WDR register.	1	0	1
Read from the internal GRAM by RDR register.	1	1	0

Registers selection by the SPI system interface		
Function	R/W	RS
Write an index to IR register	0	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

### Parallel RGB Interface

ILI9335 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section. The ILI9335 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

## Bit Operation

The ILI9335 supports a write data mask function for selectively writing data to the internal RAM in units of bits and a logical/compare operation to write data to the GRAM only when a condition is met as a result of comparing the data and the compare register bits. For details, see “Graphics Operation Functions”.

## Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

## Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 172,800 (240 x 320x 18/8) bytes with 18 bits per pixel.

## Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the  $\gamma$ -correction register to display in 262,144 colors. For details, see the “ $\gamma$ -Correction Register” section.

## Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

## Oscillator (OSC)

ILI9335 generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

## LCD Driver Circuit

The LCD driver circuit of ILI9335 consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). Display pattern data are latched when the 720<sup>th</sup> bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720 source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

## LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD

## 7. System Interface

### 7.1. Interface Specifications

ILI9335 has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9335 also has the RGB interface and VSYNC interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

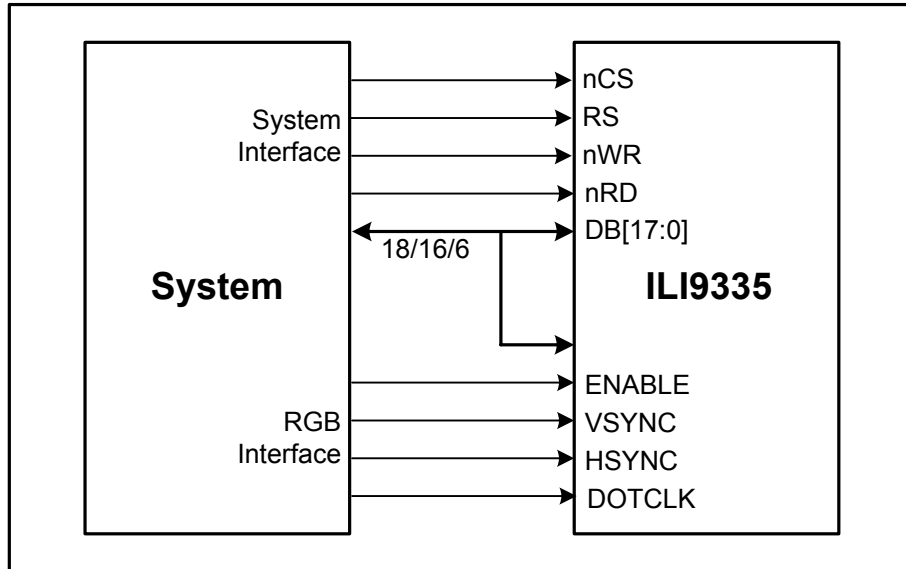
In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

ILI9335 operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM[1:0] = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 01)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available simultaneously.



**Figure1** System Interface and RGB Interface connection

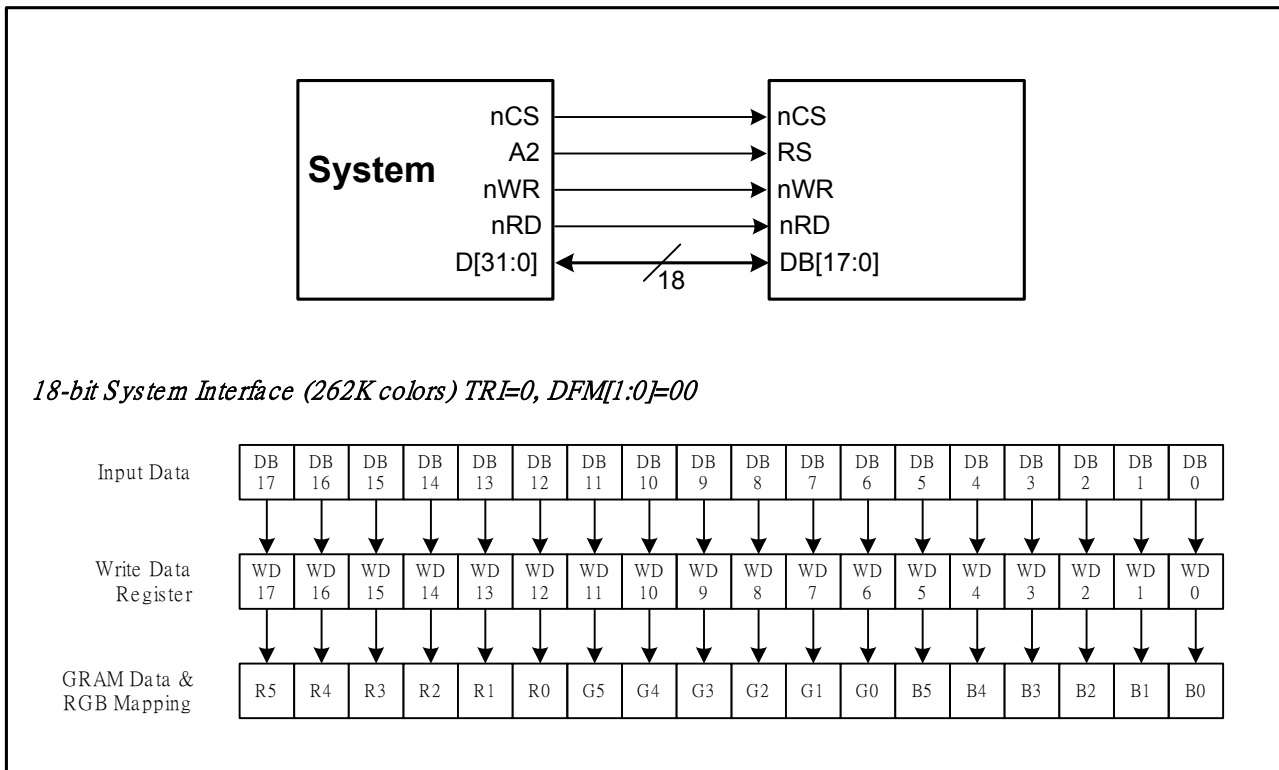
## 7.2. Input Interfaces

The following are the system interfaces available with the ILI9335. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting registers and GRAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO (DB[1:0])
0	1	1	*	Setting invalid	
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	0	1	0	i80-system18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

### 7.2.1. i80/18-bit System Interface

The i80/18-bit system interface is selected by setting the IM[3:0] as "1010" levels.



**Figure2 18-bit System Interface Data Format**

### 7.2.2. i80/16-bit System Interface

The i80/16-bit system interface is selected by setting the IM[3:0] as “0010” levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1<sup>st</sup> transfer: 2 bits, 2<sup>nd</sup> transfer: 16 bits or 1<sup>st</sup> transfer: 16 bits, 2<sup>nd</sup> transfer: 2 bits) are necessary for the 16-bit CPU interface.

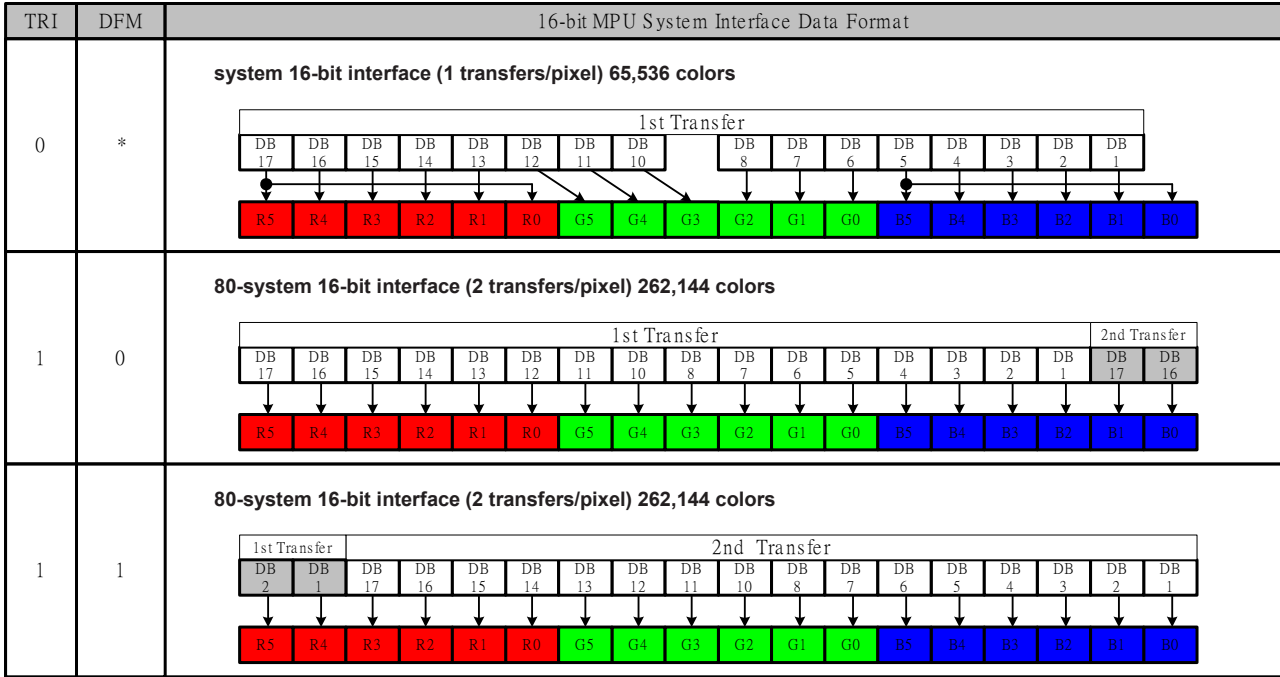
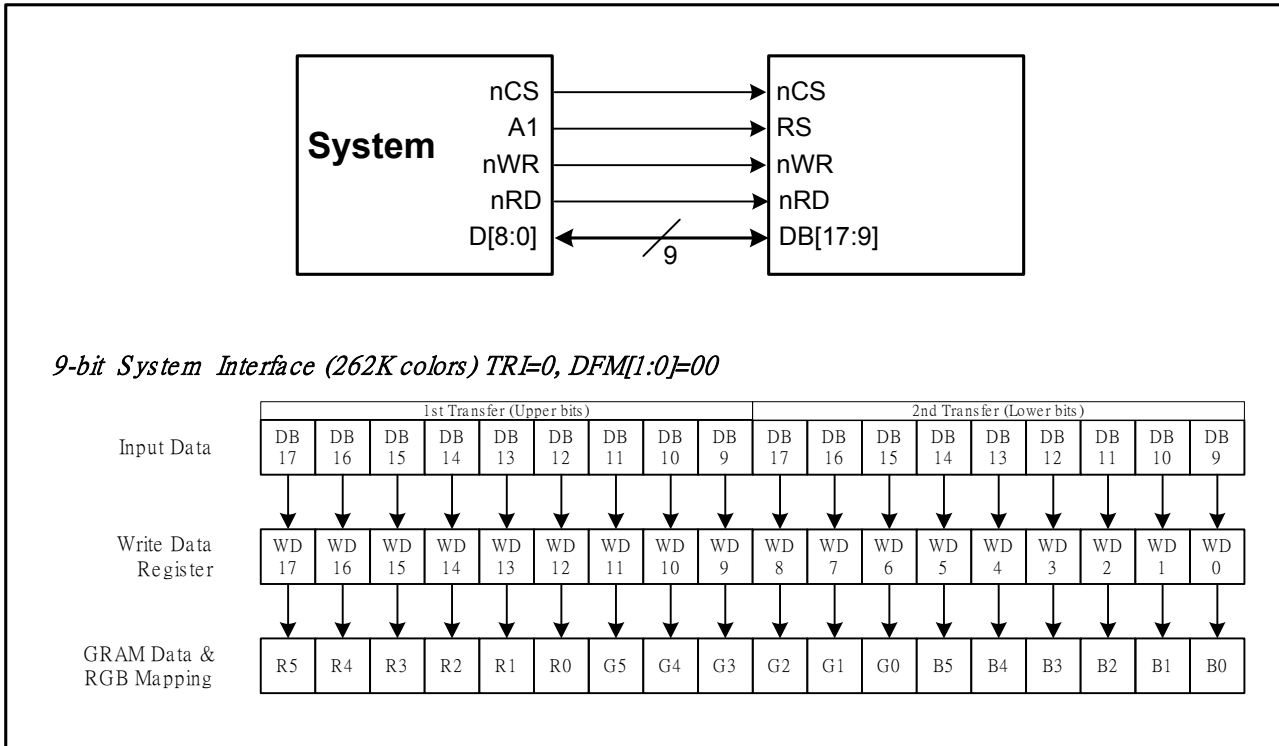


Figure3 16-bit System Interface Data Format

### 7.2.3. i80/9-bit System Interface

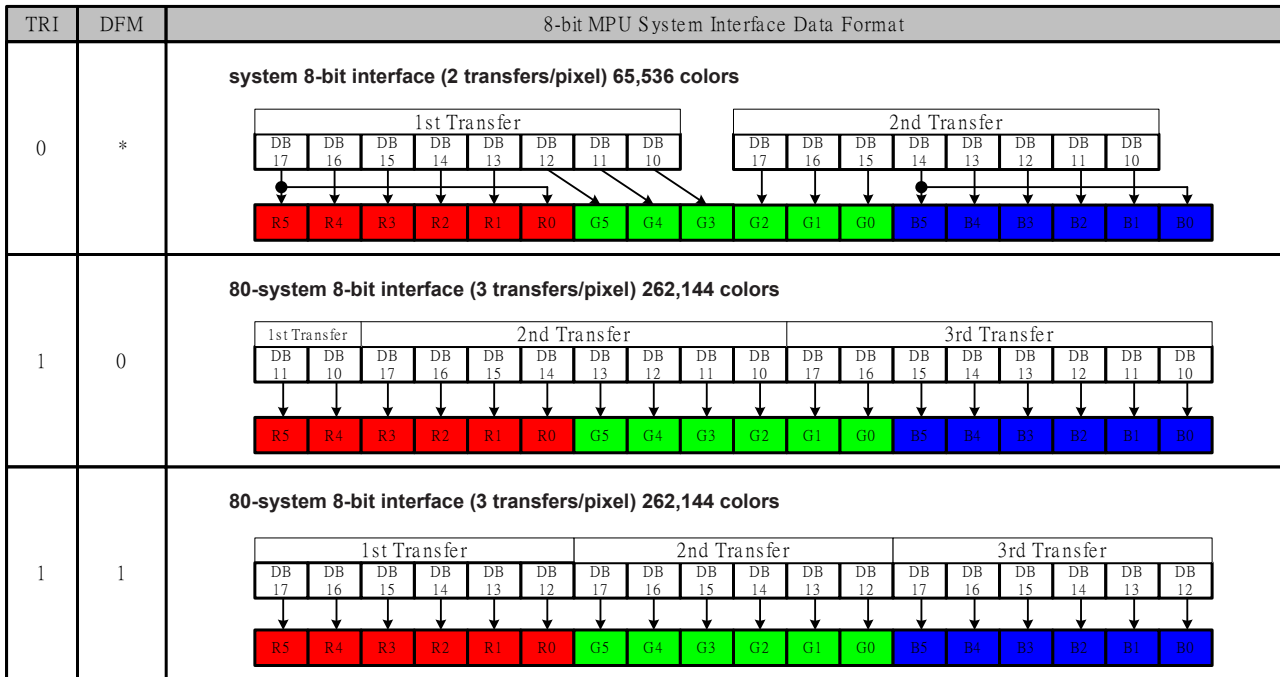
The i80/9-bit system interface is selected by setting the IM[3:0] as “1011” and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to GND.



**Figure4 9-bit System Interface Data Format**

### 7.2.4. i80/8-bit System Interface

The i80/8-bit system interface is selected by setting the IM[3:0] as “0011” and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to GND.



**Figure5 8-bit System Interface Data Format**



### 7.3. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “010x” level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9335.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, ILI9335 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9335 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6<sup>th</sup> byte of read back data.

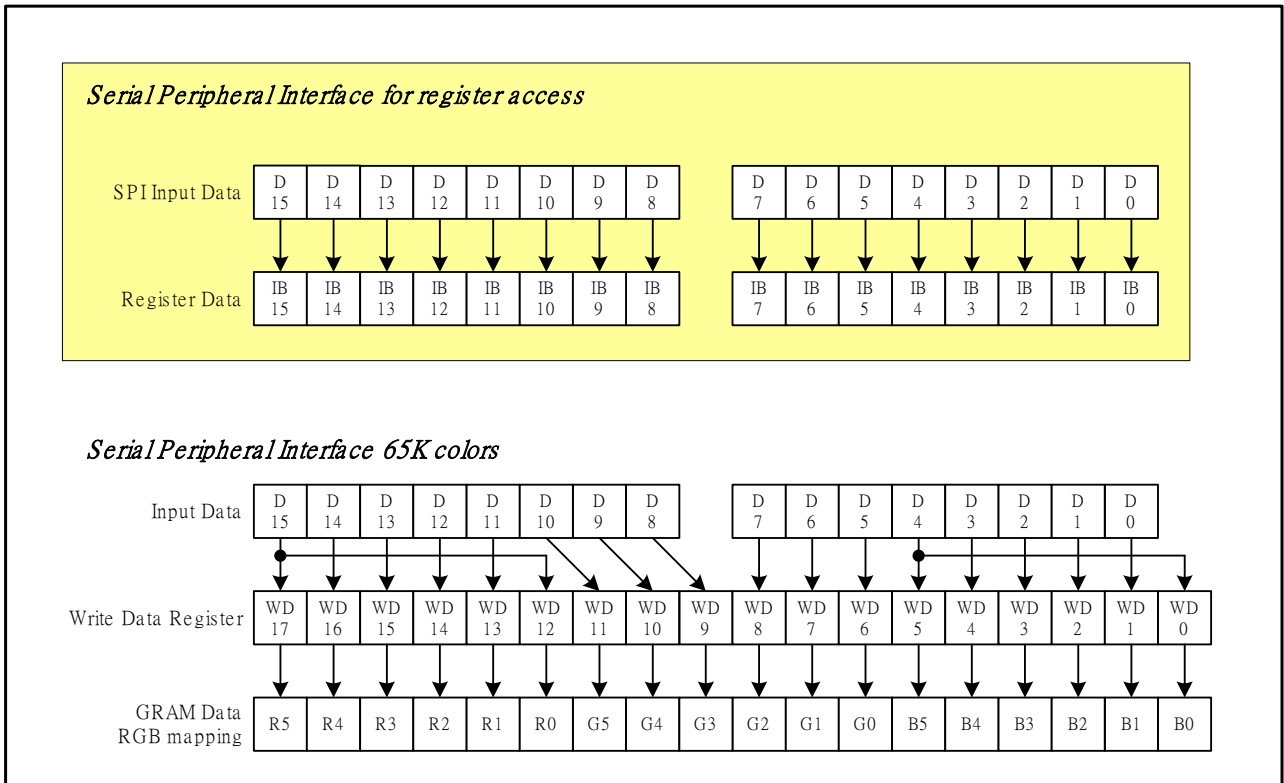
#### Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

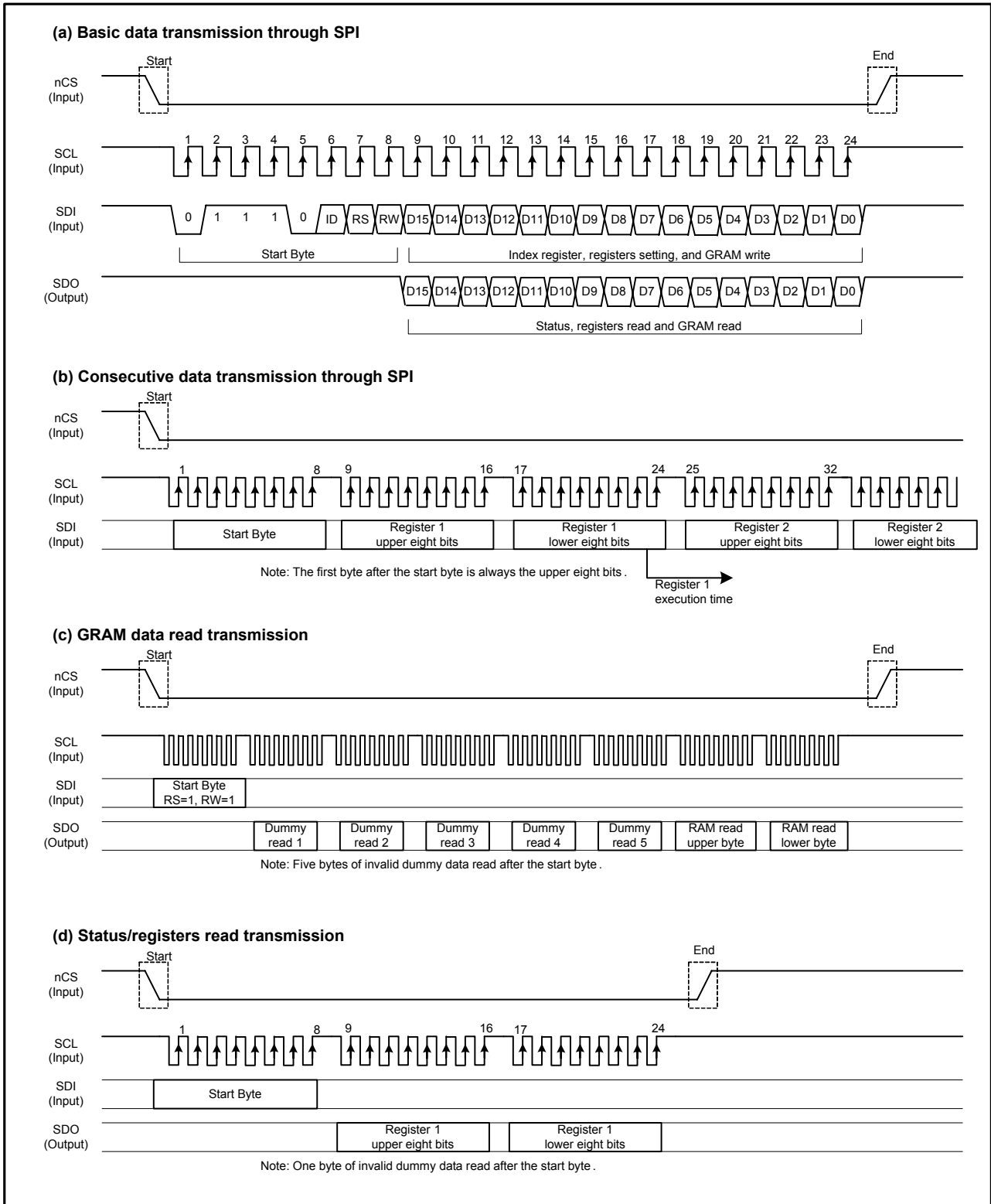
Note: ID bit is selected by setting the IM0/ID pin.

#### RS and R/W Bit Function

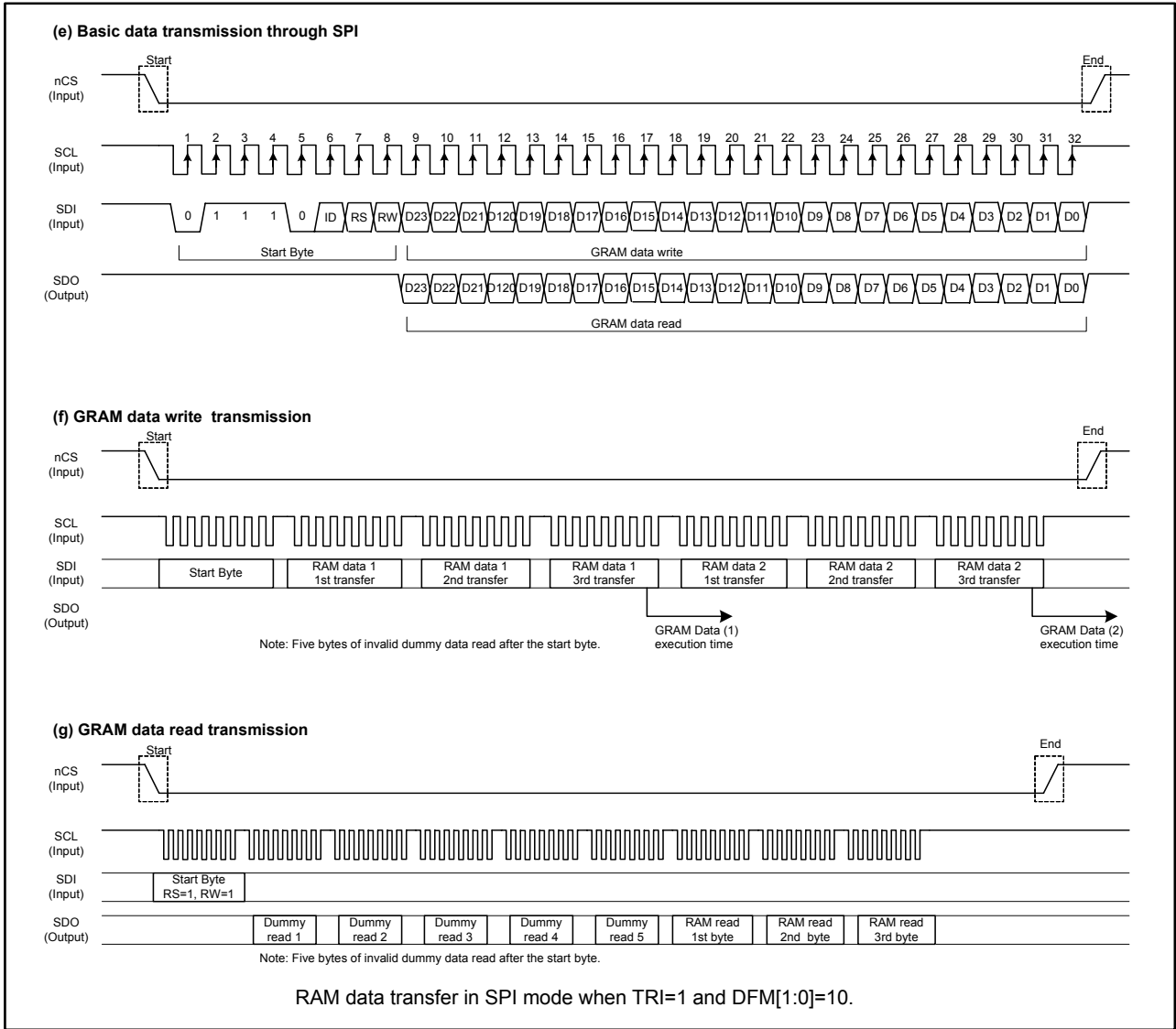
RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data



**Figure 6 Data Format of SPI Interface**



**Figure7 Data transmission through serial peripheral interface (SPI)**



**Figure8 Data transmission through serial peripheral interface (SPI), TRI="1" and DFM="10"**

## 7.4. VSYNC Interface

ILI9335 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the i80 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

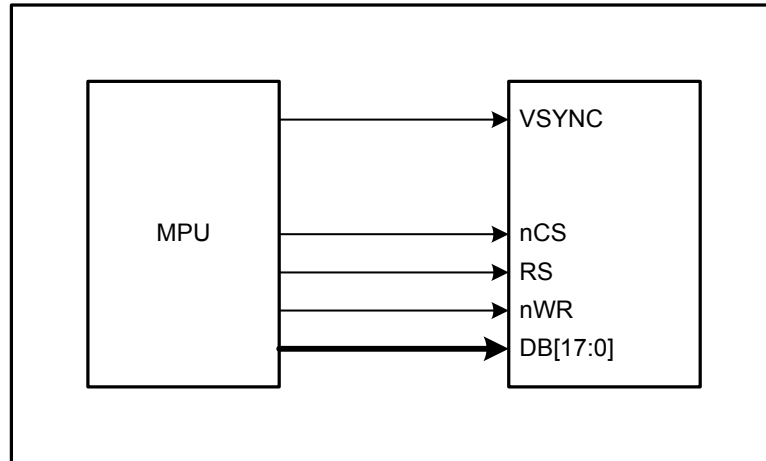


Figure9 Data transmission through VSYNC interface)

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

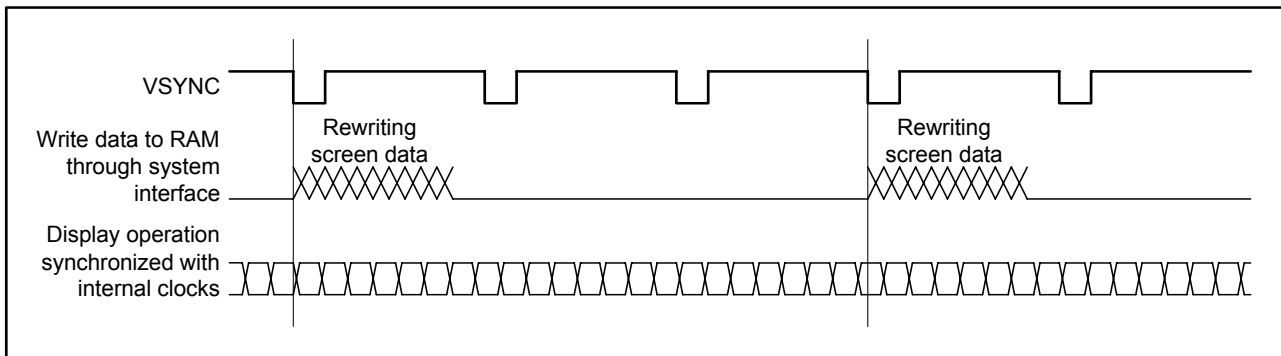
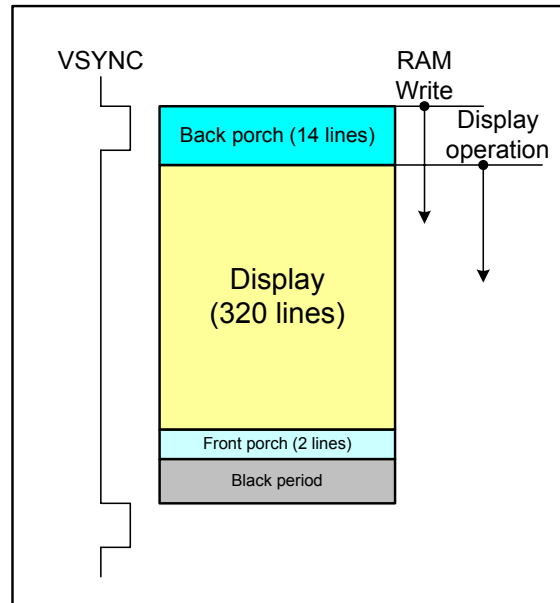


Figure10 Moving picture data transmission through VSYNC interface



**Figure11 Operation through VSYNC Interface**

The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

*Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (FP) + BackPorch (BP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.*

$$\text{Minimum RAM write speed (HZ)} > \frac{240 \times \text{DisplayLines (NL)}}{[(\text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times 16 \text{ (clocks)} \times 1/\text{fosc}]}$$

*Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.*

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

**[Example]**

- Display size: 240 RGB × 320 lines
- Lines: 320 lines (NL = 1000111)
- Back porch: 14 lines (BP = 1110)
- Front porch: 2 lines (FP = 0010)
- Frame frequency: 60 Hz
- Frequency fluctuation: 10%

$$\text{Internal oscillator clock (fosc.) [Hz]} = 60 \times [320 + 2 + 14] \times 16 \text{ clocks} \times (1.1/0.9) \doteq 394\text{KHz}$$

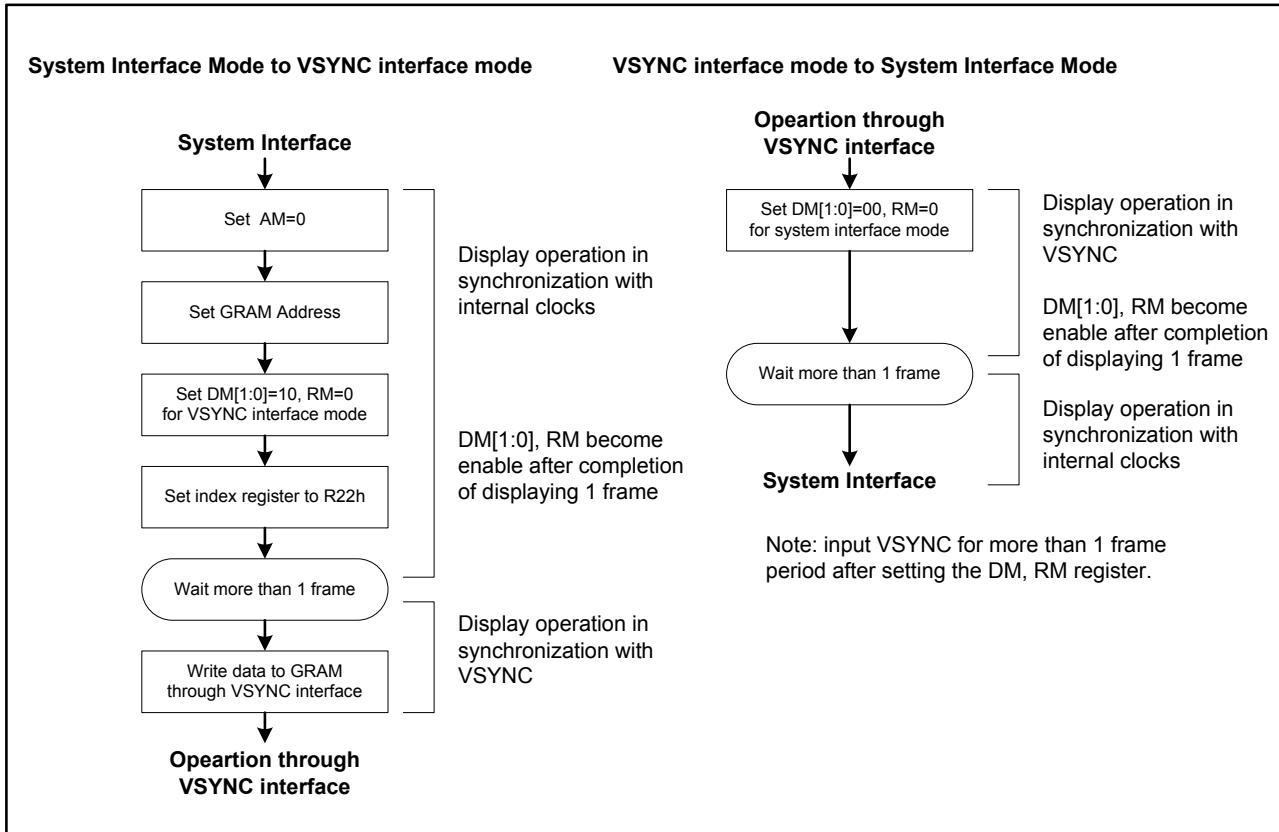
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with  $\pm 10\%$  margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

$$\text{Minimum speed for RAM writing [Hz]} > 240 \times 320 \times 394K / [(14 + 320 - 2)\text{lines} \times 16\text{clocks}] \doteq 5.7 \text{ MHz}$$

The above theoretical value is calculated based on the premise that the ILI9335 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the ILI9335 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

#### **Notes in using the VSYNC interface**

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.



**Figure12 Transition flow between VSYNC and internal clock operation modes**

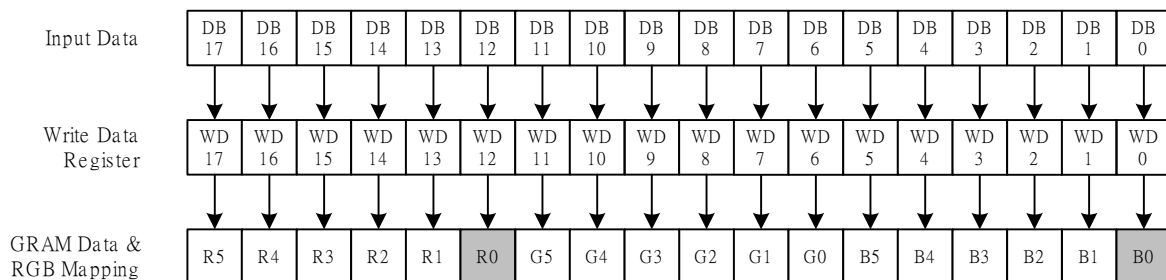


## 7.5. RGB Input Interface

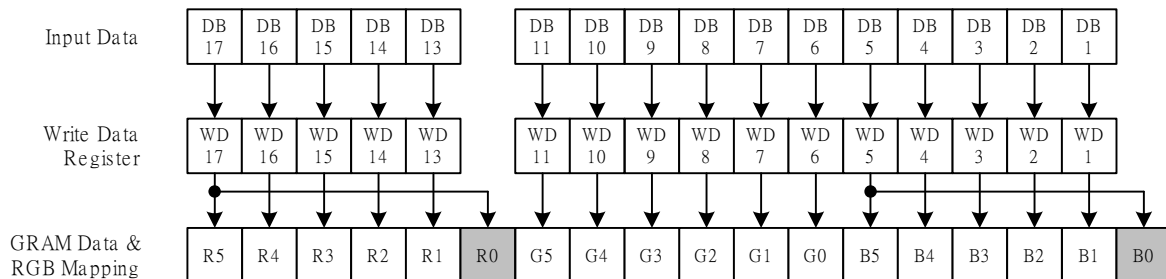
The RGB Interface mode is available for ILI9335 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

### 18-bit RGB Interface (262K colors)



### 16-bit RGB Interface (65K colors)



### 6-bit RGB Interface (262K colors)

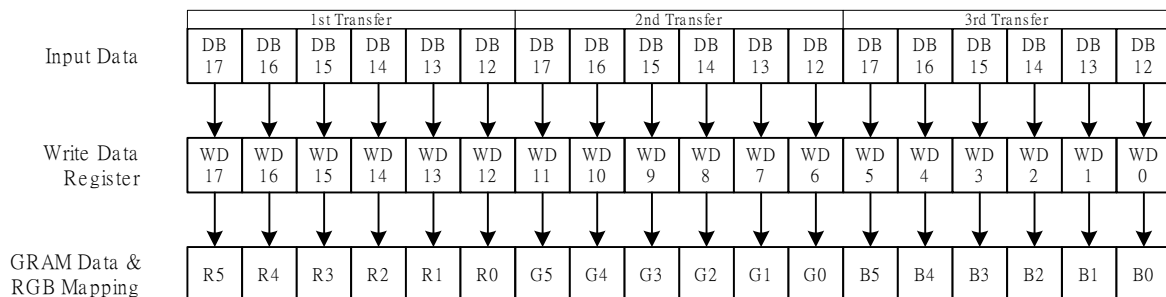


Figure13 RGB Interface Data Format

### 7.5.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

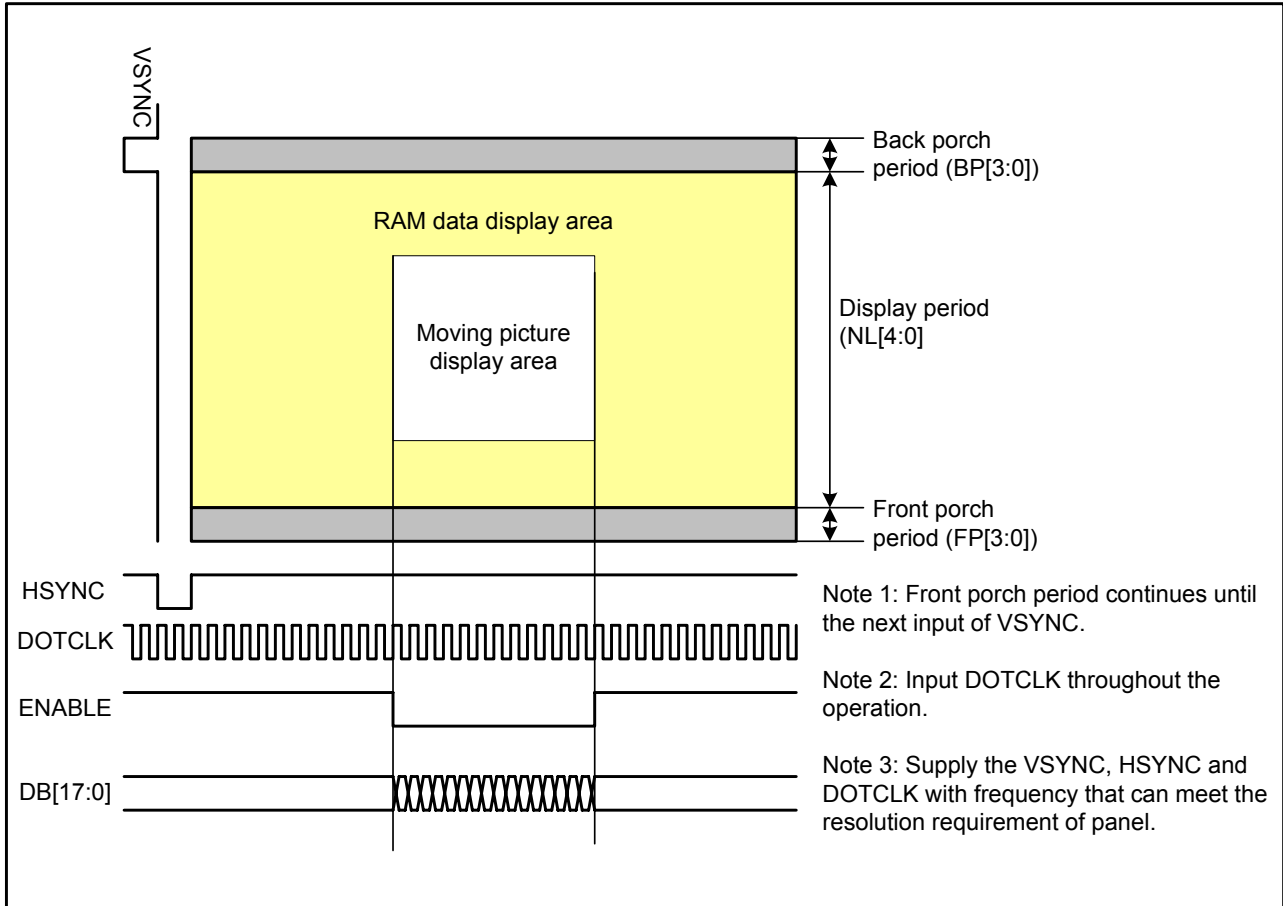
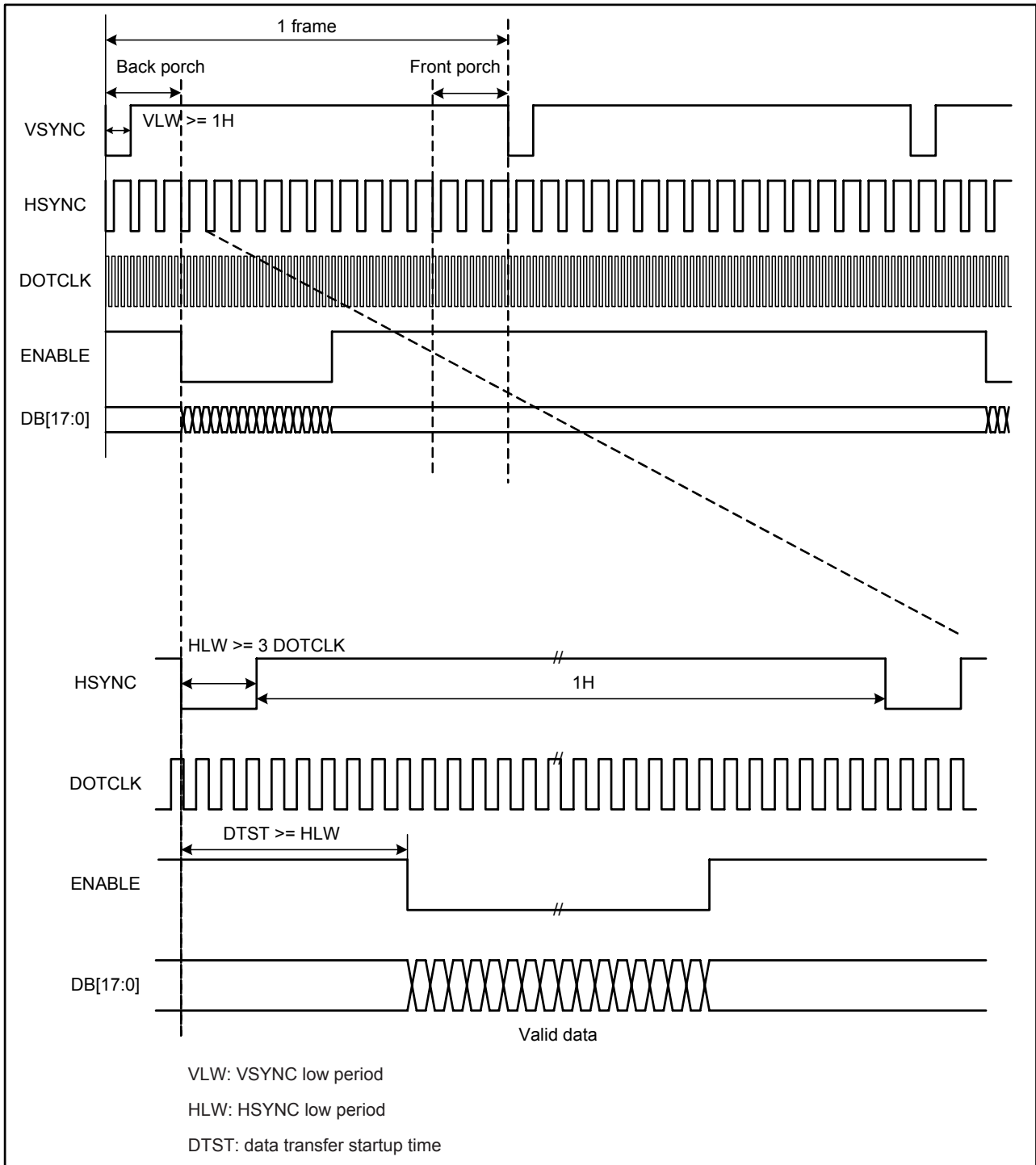


Figure14 GRAM Access Area by RGB Interface

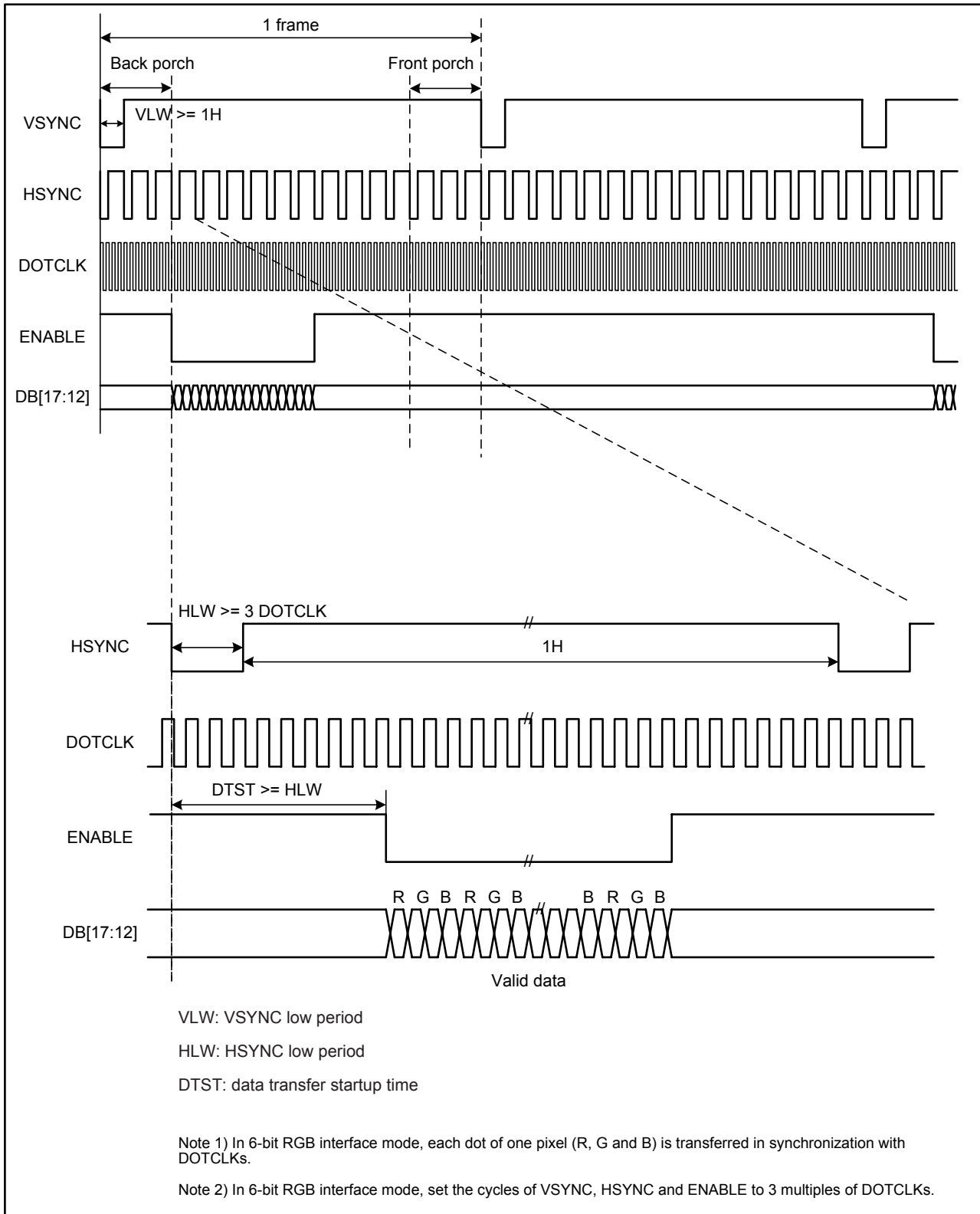
### 7.5.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.



**Figure15 Timing Chart of Signals in 18-/16-bit RGB Interface Mode**

The timing chart of 6-bit RGB interface mode is shown as follows.



**Figure16 Timing chart of signals in 6-bit RGB interface mode**

### 7.5.3. Moving Picture Mode

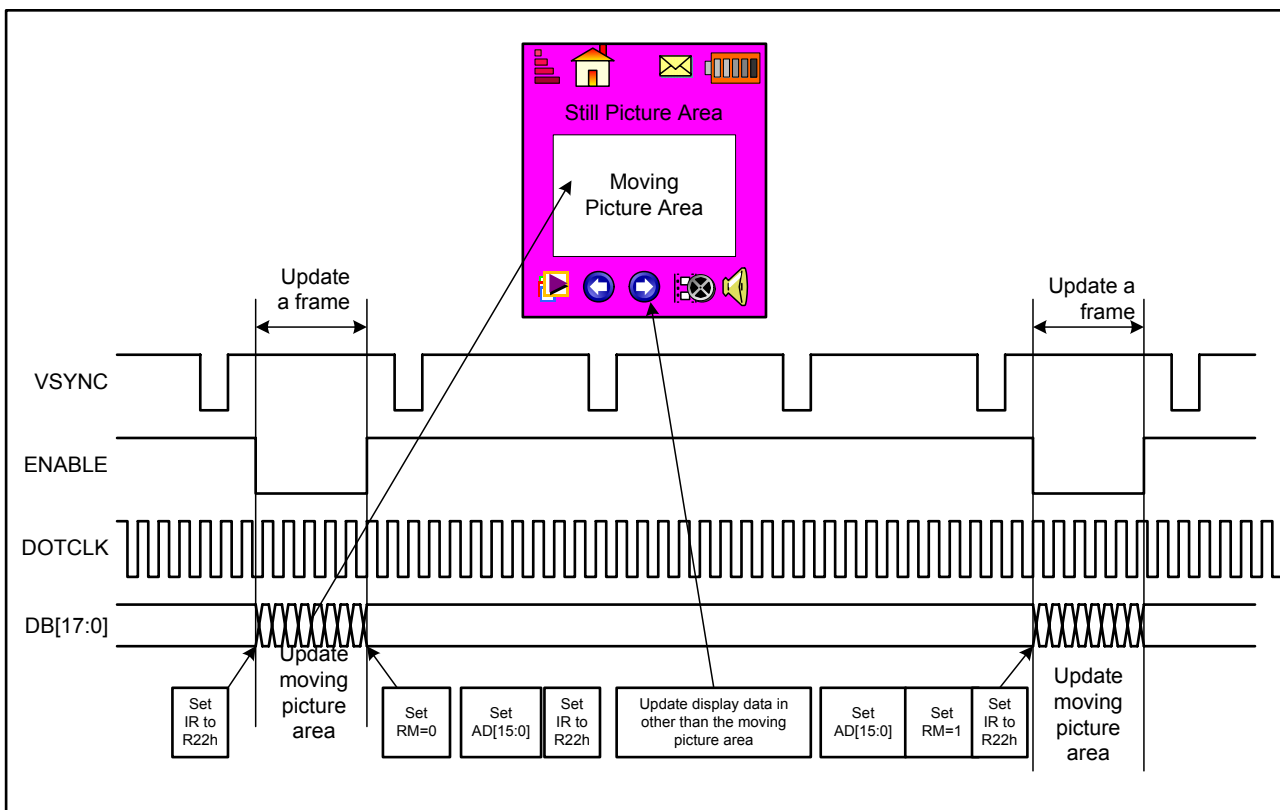
ILI9335 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

#### RAM access via a system interface in RGB-I/F mode

ILI9335 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

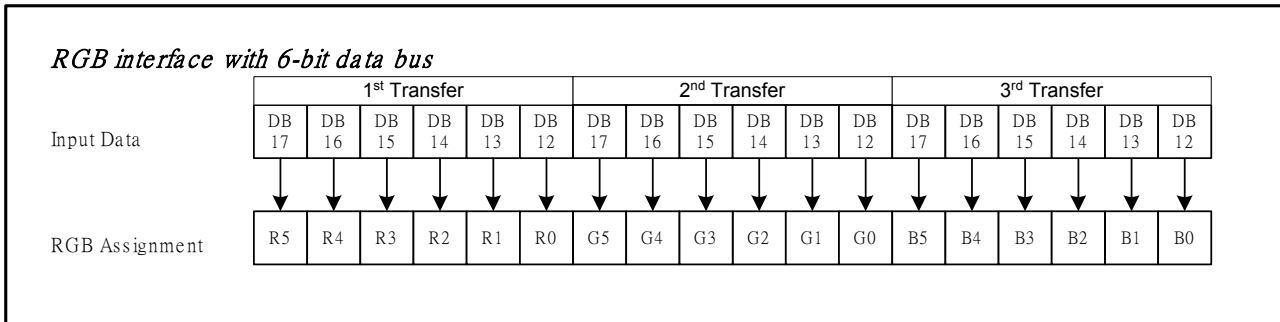
The following figure illustrates the operation of the ILI9335 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.



**Figure17 Example of update the still and moving picture**

### 7.5.4. 6-bit RGB Interface

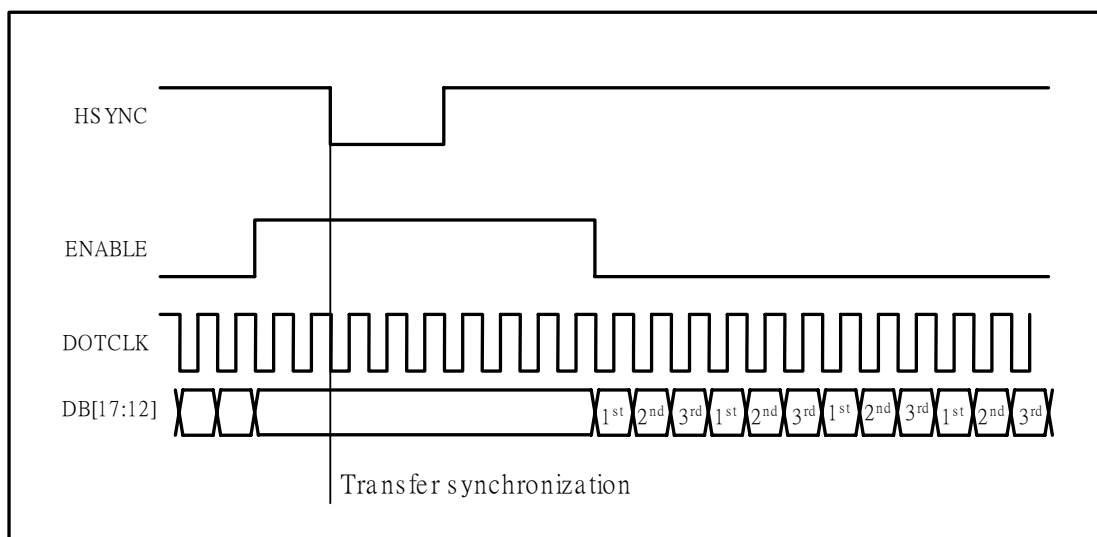
The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at GND level. Registers can be set by the system interface (i80/SPI).



#### Data transfer synchronization in 6-bit RGB interface mode

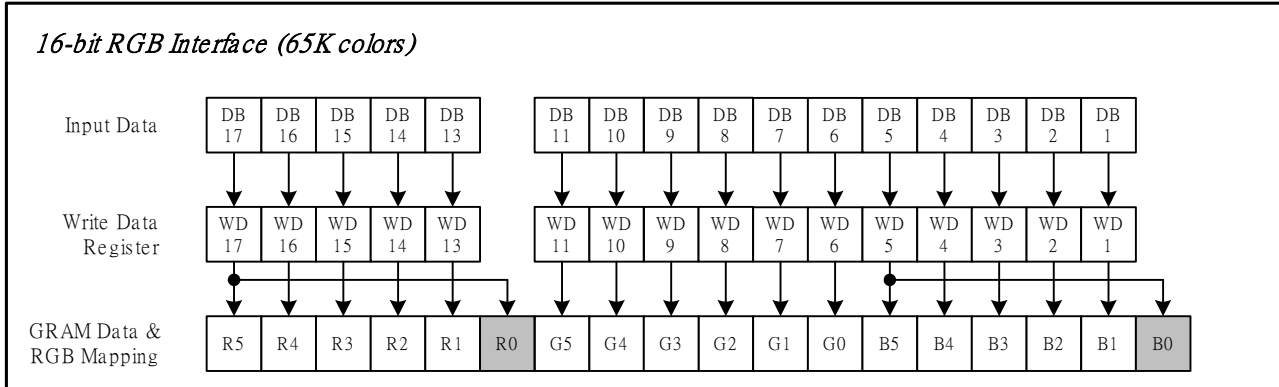
ILI9335 has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



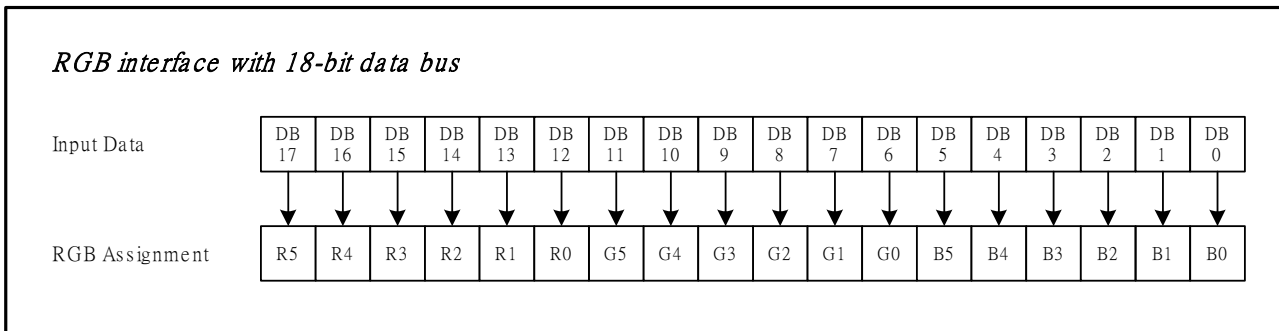
### 7.5.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



### 7.5.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



### Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

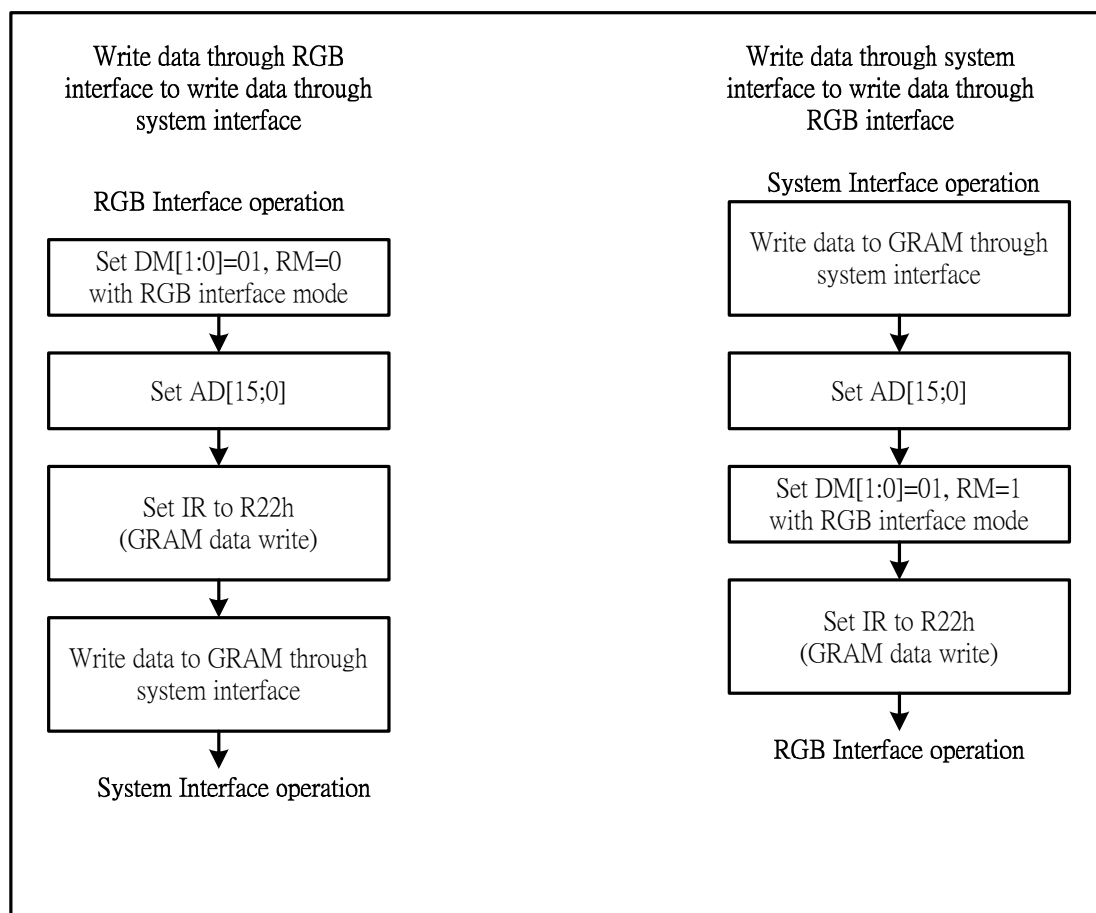
Function	RGB interface	I80 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in

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- RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
  5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
  6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
  7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
  8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

**Figure18 Internal clock operation/RGB interface mode switching**

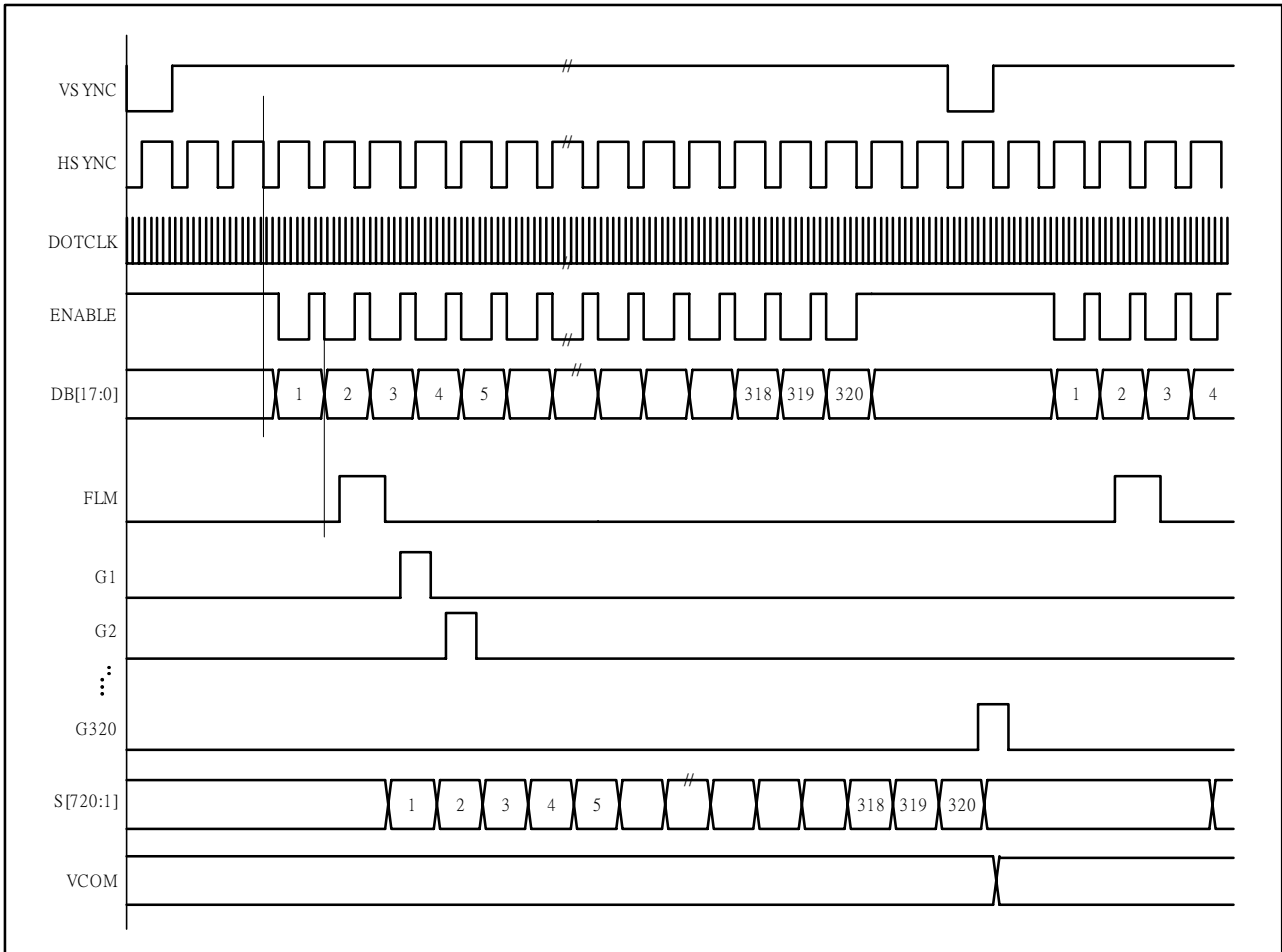


**Figure19 GRAM access between system interface and RGB interface**



## 7.6. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.



**Figure20 Relationship between RGB I/F signals and LCD Driving Signals for Panel**

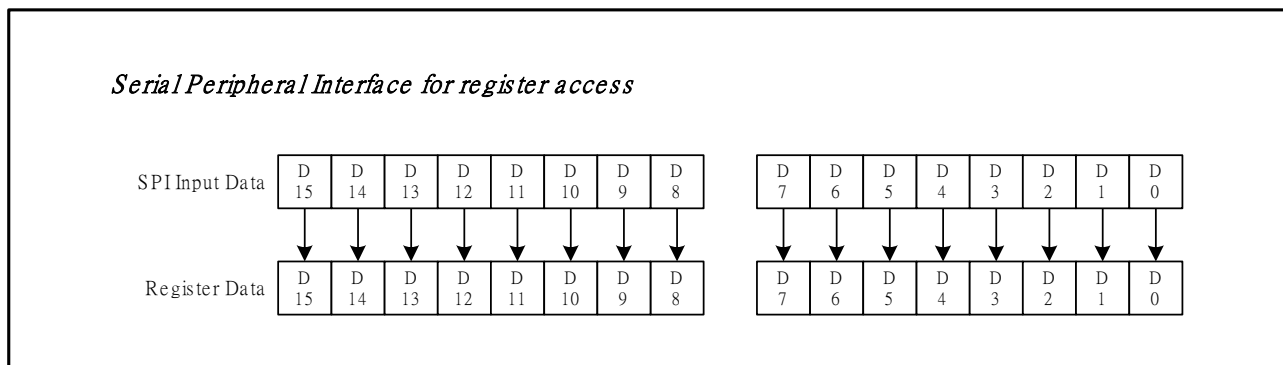
## 8. Register Descriptions

### 8.1. Registers Access

ILI9335 adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9335 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9335. The registers of the ILI9335 are categorized into the following groups.

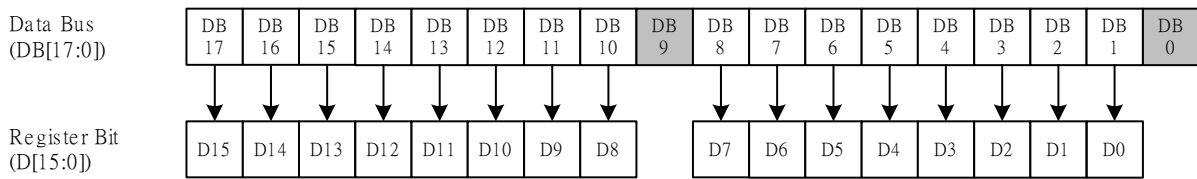
1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale  $\gamma$ -correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9335 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

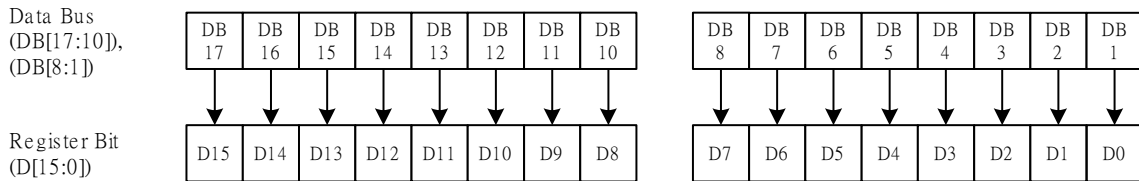


**Figure21 Register Setting with Serial Peripheral Interface (SPI)**

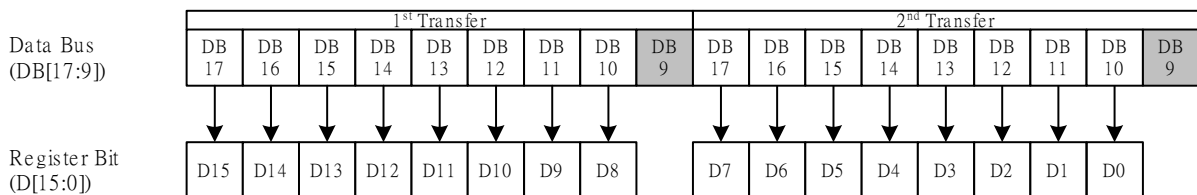
i80/M68 system 18-bit data bus interface



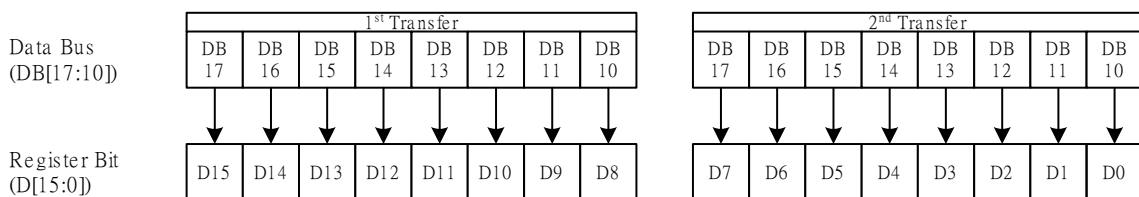
i80/M68 system 16-bit data bus interface



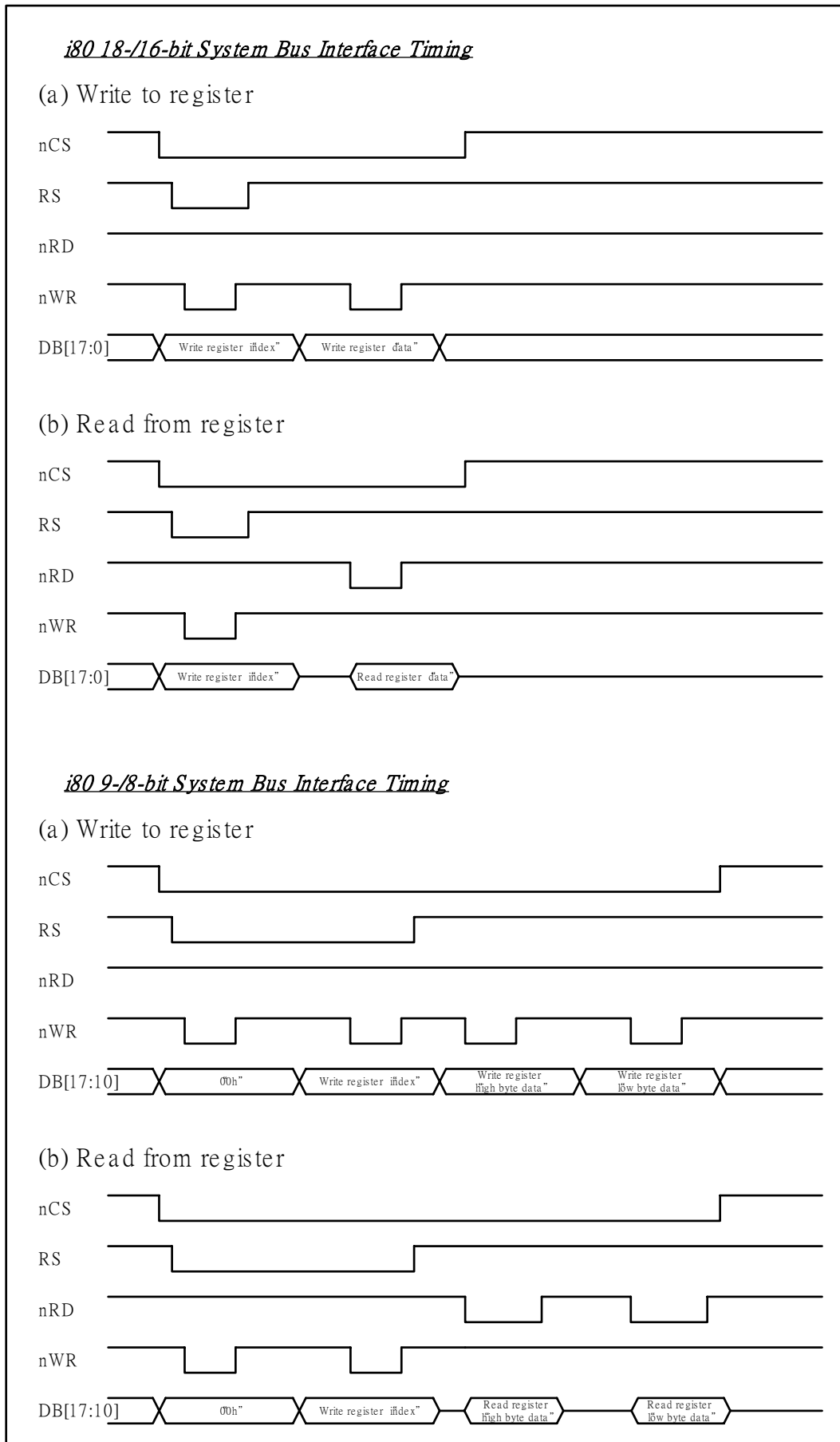
i80/M68 system 9-bit data bus interface



i80/M68 system 8-bit data bus interface/Serial peripheral interface (2/3 transmission)



**Figure22 Register setting with i80 System Interface**



**Figure 23 Register Read/Write Timing of i80 System Interface**

## 8.2. Instruction Descriptions

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	1	1	0	0	1	0	0	1	1	0	0	1	1	0	1	0	1
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
05h	16 bits data format control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS[3]	FRS[2]	FRS[1]	FRS[0]
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

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No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Position																		
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIV11	DIV10	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOW12	NOW11	NOW10	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
A1h	OTP VCM Programming Control	W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
A2h	OTP VCM Status and Enable	W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
A5h	OTP Programming ID Key	W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
E6h	Deep stand by mode control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB

### 8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ RFFh) or RAM which will be accessed.

### 8.2.2. ID code (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RO	1	1	0	0	1	0	0	1	1	0	0	1	1	0	1	0	1

The device code "9335" is read out when read this register.

### 8.2.3. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**SS:** Select the shift direction of outputs from the source driver.

When SS = 0, the shift direction of outputs is from S1 to S720

When SS = 1, the shift direction of outputs is from S720 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

**When changing SS or BGR bits, RAM data must be rewritten.**

**SM:** Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.



SM	GS	Scan Direction	Gate Output Sequence
0	0		<p>G1, G2, G3, G4, ..., G316 G317, G318, G319, G320</p>
0	1		<p>G320, G319, G318, ..., G6, G5, G4, G3, G2, G1</p>
1	0		<p>G1, G3, G5, G7, ..., G311 G313, G315, G317, G319</p> <p>G2, G4, G6, G8, ..., G312 G314, G316, G318, G320</p>
1	1		<p>G320, G318, G316, ..., G10, G8, G6, G4, G2</p> <p>G319, G317, G315, ..., G9, G78, G5, G3, G1</p>

### 8.2.4. LCD Driving Wave Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**.B/C** 0 : Frame/Field inversion  
1 : Line inversion

### 8.2.5. Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

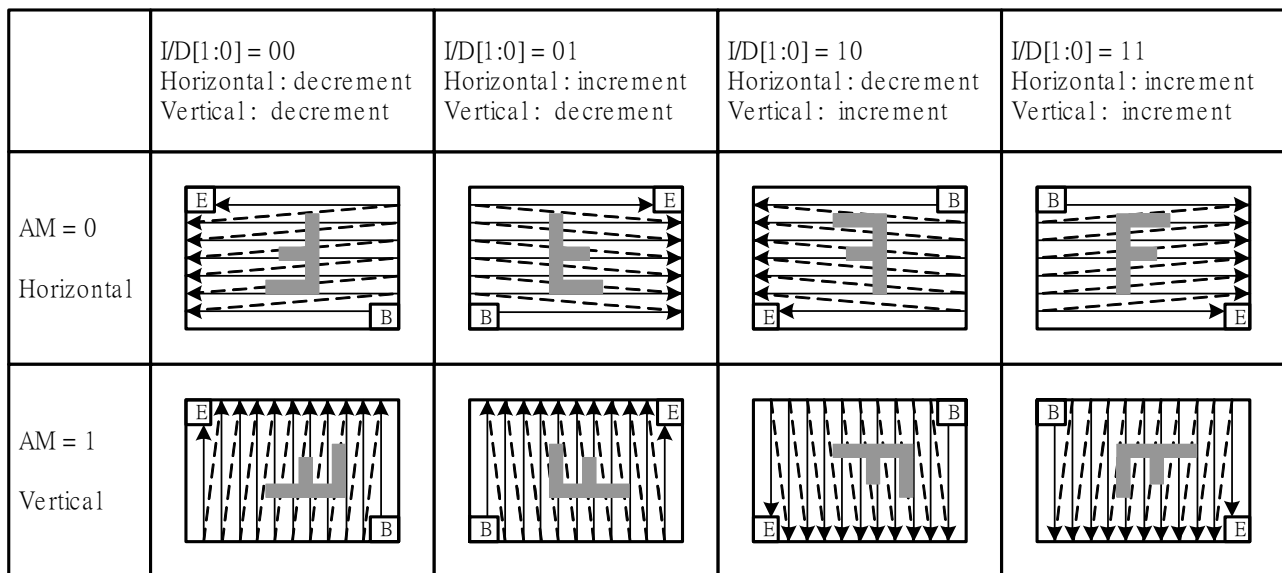
**AM** Control the GRAM update direction.

When AM = "0", the address is updated in horizontal writing direction.

When AM = "1", the address is updated in vertical writing direction.

When a window area is set by registers R50h ~R53h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

**I/D[1:0]** Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.



**Figure24 GRAM Access Direction Setting**

**ORG** Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = "0": The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.

ORG = "1": The original address "00000h" moves according to the I/D[1:0] setting.

**Notes:** 1. When ORG=1, only the origin address address"00000h" can be set in the RAM address set registers R20h, and R21h.

2. In RAM read operation, make sure to set ORG=0.

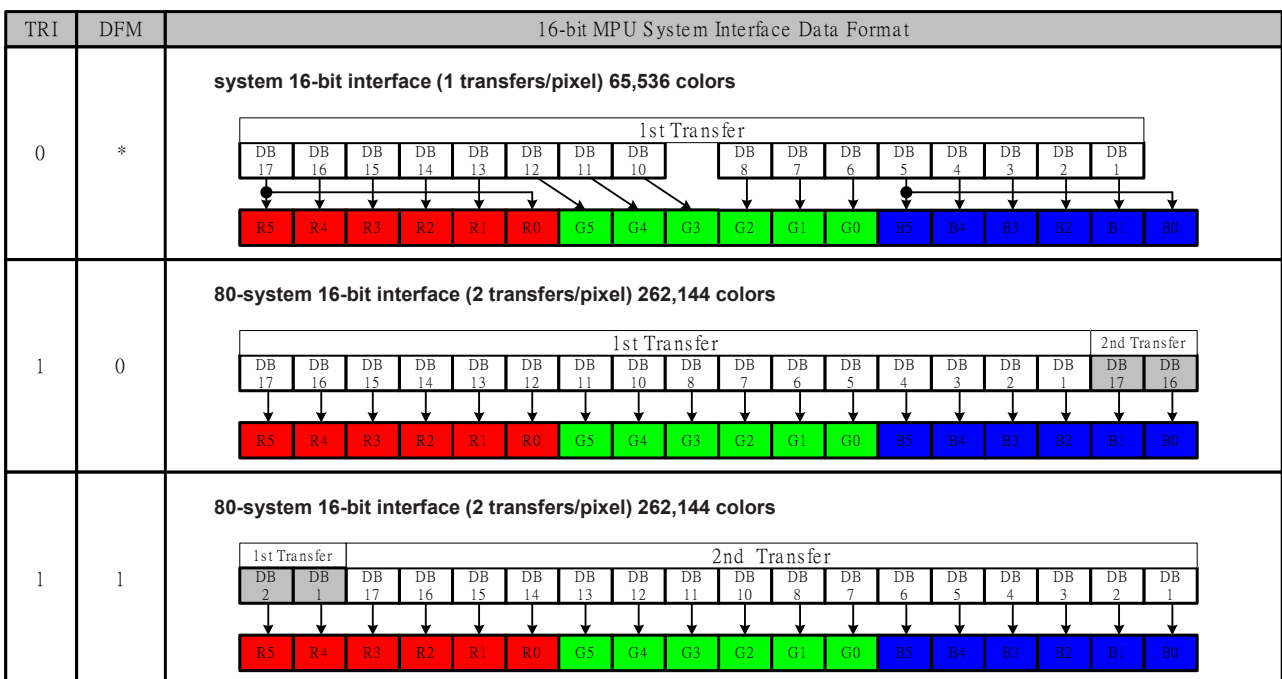
**BGR** Swap the R and B order of written data.

BGR="0": Follow the RGB order to write the pixel data.

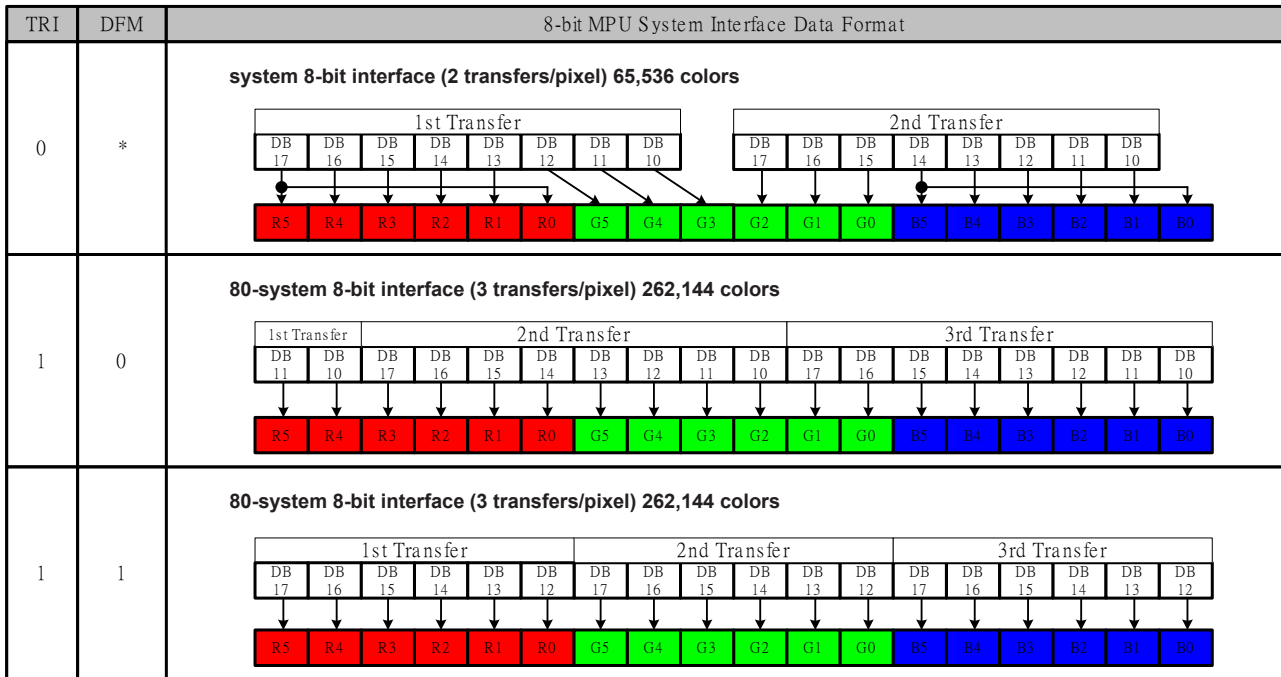
BGR="1": Swap the RGB data to BGR in writing into GRAM.

**TRI** When TRI = "1", data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = "0".

**DFM** Set the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.



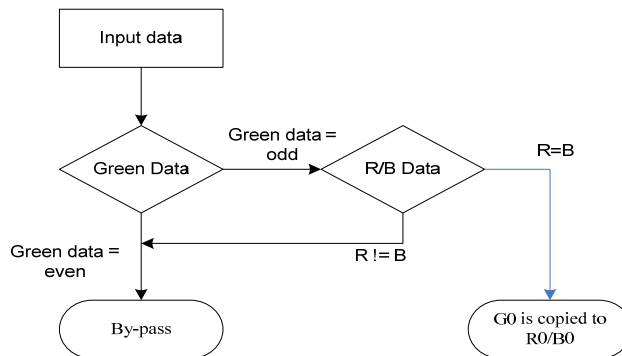
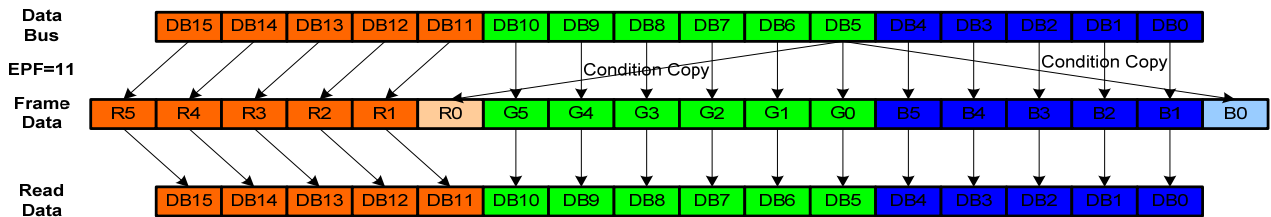
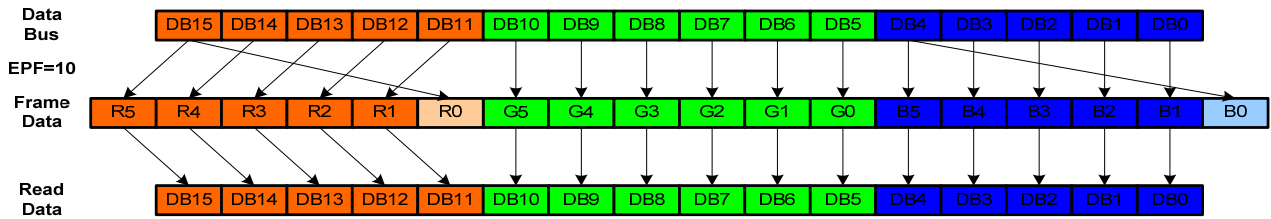
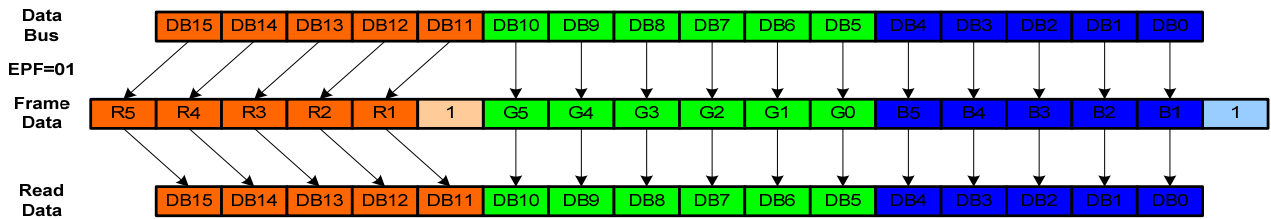
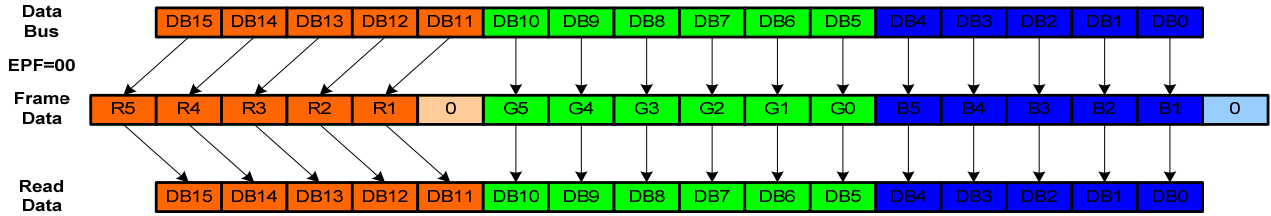
**Figure25 16-bit MPU System Interface Data Format**



**Figure26 8-bit MPU System Interface Data Format**

**8.2.6. 16bits Data Format Selection (R05h)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FPF1	EPF0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



### 8.2.7. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**D[1:0]** Set D[1:0]="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0".

When writing D1 = "0", the graphics display data is retained in the internal GRAM and the ILI9335 displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1:0] = "01", the ILI9335 continues internal display operation. When the display is turned off by setting D[1:0] = "00", the ILI9335 internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D1	D0	BASEE	Source, VCOM Output	ILI9335 internal operation
0	0	0	GND	Halt
0	1	1	GND	Operate
1	0	0	Non-lit display	Operate
1	1	0	Non-lit display	Operate
1	1	1	Base image display	Operate

*Note:* 1. data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

- The D[1:0] setting is valid on both 1<sup>st</sup> and 2<sup>nd</sup> displays.
- The non-lit display level from the source output pins is determined by instruction (PTS).

**CL** When CL = "1", the 8-color display mode is selected.

CL	Colors
0	262,144
1	8

**GON and DTE** Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1 ~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal Display

#### BASEE

Base image display enable bit. When BASEE = "0", no base image is displayed. The ILI9335 drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed. The D[1:0] setting has higher priority over the BASEE setting.

#### PTDE[1:0]

Partial image 2 and Partial image 1 enable bits

PTDE1/0 = 0: turns off partial image. Only base image is displayed.

PTDE1/0 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

### 8.2.8. Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

#### FP[7:0]/BP[7:0]

The FP[7:0] and BP[7:0] bits specify the line number of front and back porch periods respectively.

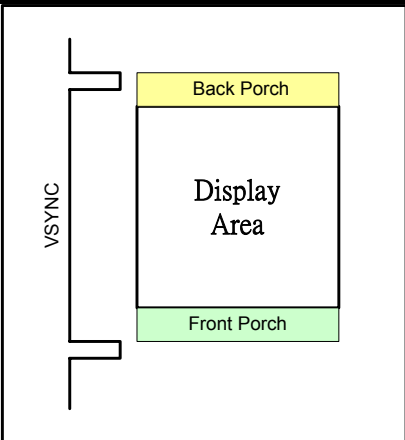
When setting the FP[7:0] and BP[7:0] value, the following conditions shall be met:

$$BP + FP \leq 256 \text{ lines}$$

$$FP \geq 2 \text{ lines}$$

$$BP \geq 2 \text{ lines}$$

FP[7:0] /BP[7:0]	Number of lines for Front Porch	Number of lines for Back Porch
00h	Setting Prohibited	Setting Prohibited
01h	Setting Prohibited	Setting Prohibited
02h	2 lines	2 lines
03h	3 lines	3 lines
04h	4 lines	4 lines
05h	5 lines	5 lines
06h	6 lines	6 lines
07h	7 lines	7 lines
08h	8 lines	8 lines
09h	9 lines	9 lines
0Ah	10 lines	10 lines
:	:	:
7Fh	127 lines	127 lines
80h	128 lines	128 lines
81h	Setting Prohibited	Setting Prohibited
:	:	:
FFh	Setting Prohibited	Setting Prohibited



Note: The output timing to the LCD is delayed by 2 lines period from the input of synchronizing signal.

### 8.2.9. Display Control 3 (R09h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**ISC[3:0]:** Specify the scan cycle interval of gate driver in non-display area when PTG[1:0]="10" to select interval scan. Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f <sub>FLM</sub> =60 Hz
0	0	0	0	0 frame	-
0	0	0	1	0 frame	-
0	0	1	0	3 frame	50ms
0	0	1	1	5 frame	84ms
0	1	0	0	7 frame	117ms
0	1	0	1	9 frame	150ms
0	1	1	0	11 frame	184ms
0	1	1	1	13 frame	217ms
1	0	0	0	15 frame	251ms
1	0	0	1	17 frame	284ms
1	0	1	0	19 frame	317ms
1	0	1	1	21 frame	351ms
1	1	0	0	23 frame	384ms
1	1	0	1	25 frame	418ms
1	1	1	0	27 frame	451ms
1	1	1	1	29 frame	484ms

**PTG[1:0]** Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	0	Normal scan	Set with the PTS[2:0] bits	VcomH/VcomL
0	1	Setting Prohibited	-	-
1	0	Interval scan	Set with the PTS[2:0] bits	VcomH/VcomL
1	1	Setting Prohibited	-	-

**PTS[2:0]**

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted.

PTS[2:0]	Source output level		Grayscale amplifier in operation
	Positive polarity	Negative polarity	
000	V63	V0	V63 to V0
001	Setting Prohibited	Setting Prohibited	-
010	GND	GND	V63 to V0
011	Hi-Z	Hi-Z	V63 to V0
100	V63	V0	V63 and V0
101	Setting Prohibited	Setting Prohibited	-
110	GND	GND	V63 and V0
111	Hi-Z	Hi-Z	V63 and V0

- Notes: 1. The power efficiency can be improved by halting grayscale amplifiers only in non-display drive period.  
2. The gate output level in non-lit display area drive period is determined by PTG[1:0].



### 8.2.10. Display Control 4 (R0Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**FMI[2:0]** Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

**FMARKOE** When FMARKOE=1, ILI9335 starts to output FMARK signal in the output interval set by FMI[2:0] bits.

FMI[2:0]	Output Interval
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Setting disabled

### 8.2.11. RGB Display Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**RIM[1:0]** Select the RGB interface data width.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (1 transfer/pixel), DB[17:0]
0	1	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1]
1	0	6-bit RGB interface (3 transfers/pixel), DB[17:12]
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

**DM[1:0]** Select the display operation mode.

DM1	DM0	Display Interface
0	0	Internal system clock
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

**RM** Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0])
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
Rewrite still picture area while RGB interface Displaying moving pictures.		System interface (RM = 0)	RGB interface (DM[1:0] = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1: Registers are set only via the system interface or SPI interface.

Note 2: Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

**ENC[2:0]** Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

### 8.2.12. Frame Marker Position (R0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**EMP[8:0]** Sets the output position of frame cycle (frame marker).

When FMP[8:0]=0, a high-active pulse FMARK is output at the start of back porch period for one display line period (1H).

Make sure the  $9'h000 \leq FMP \leq BP+NL+FP$

FMP[8:0]	FMARK Output Position
9'h000	0 <sup>th</sup> line
9'h001	1 <sup>st</sup> line
9'h002	2 <sup>nd</sup> line
9'h003	3 <sup>rd</sup> line
.	.
.	.
.	.
9'h175	373 <sup>rd</sup> line
9'h176	374 <sup>th</sup> line
9'h177	375 <sup>th</sup> line

### 8.2.13. RGB Display Interface Control 2 (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**DPL:** Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the rising edge of DOTCLK

DPL = "1" The data is input on the falling edge of DOTCLK

**EPL:** Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".

EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

**HSPL:** Sets the signal polarity of the HSYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

**VSPL:** Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

### 8.2.14. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**SLP:** When SLP = 1, ILI9335 enters the sleep mode and the display operation stops except the RC oscillator to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following instruction.

- a. Exit sleep mode (SLP = "0")

**STB:** When STB = 1, ILI9335 enters the standby mode and the display operation stops except the GRAM power supply to reduce the power consumption. In the STB mode, the GRAM data and instructions cannot be updated except the following instruction.

- a. Exit standby mode (STB = "0")

**AP[2:0]:** Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = "000" to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Gamma driver amplifiers	Source driver amplifiers
000	Halt	Halt
001	1.00	1.00
010	1.00	0.75
011	1.00	0.50
100	0.75	1.00
101	0.75	0.75
110	0.75	0.50
111	0.50	0.50

**SAP:** Source Driver output control

SAP=0, Source driver is disabled.

SAP=1, Source driver is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

**APE:** Power supply enable bit.

Set APE = "1" to start the generation of power supply according to the power supply startup sequence.

**BT[3:0]:** Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	VCI1 x 2	- VCI1	VCI1 x 6	- VCI1 x 5
3'h1	VCI1 x 2	- VCI1		- VCI1 x 4
3'h2				- VCI1 x 3
3'h3	VCI1 x 2	- VCI1	VCI1 x 5	- VCI1 x 5
3'h4				- VCI1 x 4
3'h5			- VCI1 x 3	
3'h6	VCI1 x 2	- VCI1	VCI1 x 4	- VCI1 x 4
3'h7				- VCI1 x 3

Notes: 1. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL and VCL levels.

2. Make sure DDVDH = 6.0V (max.).

### 8.2.15. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

**VC[2:0]** Sets the ratio factor of VCI to generate the reference voltages VCI1.

VC2	VC1	VC0	VCI1 voltage
0	0	0	0.95 x VCI
0	0	1	0.90 x VCI
0	1	0	0.85 x VCI
0	1	1	0.80 x VCI
1	0	0	0.75 x VCI
1	0	1	0.70 x VCI
1	1	0	Disabled
1	1	1	1.0 x VCI

**DC0[2:0]:** Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency

enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

**DC1[2:0]:** Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC02	DC01	DC00	Step-up circuit1 step-up frequency ( $f_{DCDC1}$ )	DC12	DC11	DC10	Step-up circuit2 step-up frequency ( $f_{DCDC2}$ )
0	0	0	Fosc	0	0	0	Fosc / 4
0	0	1	Fosc / 2	0	0	1	Fosc / 8
0	1	0	Fosc / 4	0	1	0	Fosc / 16
0	1	1	Fosc / 8	0	1	1	Fosc / 32
1	0	0	Fosc / 16	1	0	0	Fosc / 64
1	0	1	Fosc / 32	1	0	1	Fosc / 128
1	1	0	Fosc / 64	1	1	0	Fosc / 256
1	1	1	Halt step-up circuit 1	1	1	1	Halt step-up circuit 2

Note: Be sure  $f_{DCDC1} \geq f_{DCDC2}$  when setting DC0[2:0] and DC1[2:0].

### 8.2.16. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**VRH[3:0]** Set the amplifying rate (1.6 ~ 1.9) of VCI applied to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

**VCIRE:** Select the external reference voltage VCI or internal reference voltage VCIR.

VCIRE=0	External reference voltage VCI (default)
VCIRE =1	Internal reference voltage 2.5V

VCIRE =0					VCIRE =1				
VRH3	VRH2	VRH1	VRH0	VREG1OUT	VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt	0	0	0	0	Halt
0	0	0	1	VCI x 2.00	0	0	0	1	2.5V x 2.00 = 5.000V
0	0	1	0	VCI x 2.05	0	0	1	0	2.5V x 2.05 = 5.125V
0	0	1	1	VCI x 2.10	0	0	1	1	2.5V x 2.10 = 5.250V
0	1	0	0	VCI x 2.20	0	1	0	0	2.5V x 2.20 = 5.500V
0	1	0	1	VCI x 2.30	0	1	0	1	2.5V x 2.30 = 5.750V
0	1	1	0	VCI x 2.40	0	1	1	0	2.5V x 2.40 = 6.000V
0	1	1	1	VCI x 2.40	0	1	1	1	2.5V x 2.40 = 6.000V
1	0	0	0	VCI x 1.60	1	0	0	0	2.5V x 1.60 = 4.000V
1	0	0	1	VCI x 1.65	1	0	0	1	2.5V x 1.65 = 4.125V
1	0	1	0	VCI x 1.70	1	0	1	0	2.5V x 1.70 = 4.250V
1	0	1	1	VCI x 1.75	1	0	1	1	2.5V x 1.75 = 4.375V
1	1	0	0	VCI x 1.80	1	1	0	0	2.5V x 1.80 = 4.500V
1	1	0	1	VCI x 1.85	1	1	0	1	2.5V x 1.85 = 4.625V
1	1	1	0	VCI x 1.90	1	1	1	0	2.5V x 1.90 = 4.750V
1	1	1	1	VCI x 1.95	1	1	1	1	2.5V x 1.95 = 4.875V

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When  $VCI < 2.5V$ , Internal reference voltage will be same as  $VCI$ .

Make sure that  $VC$  and  $VRH$  setting restriction:  $VREG1OUT \leq (DDVDH - 0.2)V$ .

### 8.2.17. Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**VDV[4:0]** Select the factor of  $VREG1OUT$  to set the amplitude of  $Vcom$  alternating voltage from 0.70 to 1.24 x  $VREG1OUT$ .

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	$VREG1OUT \times 0.70$
0	0	0	0	1	$VREG1OUT \times 0.72$
0	0	0	1	0	$VREG1OUT \times 0.74$
0	0	0	1	1	$VREG1OUT \times 0.76$
0	0	1	0	0	$VREG1OUT \times 0.78$
0	0	1	0	1	$VREG1OUT \times 0.80$
0	0	1	1	0	$VREG1OUT \times 0.82$
0	0	1	1	1	$VREG1OUT \times 0.84$
0	1	0	0	0	$VREG1OUT \times 0.86$
0	1	0	0	1	$VREG1OUT \times 0.88$
0	1	0	1	0	$VREG1OUT \times 0.90$
0	1	0	1	1	$VREG1OUT \times 0.92$
0	1	1	0	0	$VREG1OUT \times 0.94$
0	1	1	0	1	$VREG1OUT \times 0.96$
0	1	1	1	0	$VREG1OUT \times 0.98$
0	1	1	1	1	$VREG1OUT \times 1.00$

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
1	0	0	0	0	$VREG1OUT \times 0.94$
1	0	0	0	1	$VREG1OUT \times 0.96$
1	0	0	1	0	$VREG1OUT \times 0.98$
1	0	0	1	1	$VREG1OUT \times 1.00$
1	0	1	0	0	$VREG1OUT \times 1.02$
1	0	1	0	1	$VREG1OUT \times 1.04$
1	0	1	1	0	$VREG1OUT \times 1.06$
1	0	1	1	1	$VREG1OUT \times 1.08$
1	1	0	0	0	$VREG1OUT \times 1.10$
1	1	0	0	1	$VREG1OUT \times 1.12$
1	1	0	1	0	$VREG1OUT \times 1.14$
1	1	0	1	1	$VREG1OUT \times 1.16$
1	1	1	0	0	$VREG1OUT \times 1.18$
1	1	1	0	1	$VREG1OUT \times 1.20$
1	1	1	1	0	$VREG1OUT \times 1.22$
1	1	1	1	1	$VREG1OUT \times 1.24$

**Set VDV[4:0] to let  $Vcom$  amplitude less than 6V.**

### 8.2.18. GRAM Horizontal/Vertical Address Set (R20h, R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**AD[16:0]** Set the initial value of address counter (AC).

The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

AD[16:0]	GRAM Data Map
17'h00000 ~ 17'h000EF	1 <sup>st</sup> line GRAM Data
17'h00100 ~ 17'h001EF	2 <sup>nd</sup> line GRAM Data

17'h00200 ~ 17'h002EF	3 <sup>rd</sup> line GRAM Data
17'h00300 ~ 17'h003EF	4 <sup>th</sup> line GRAM Data
17'h13D00 ~ 17' h13DEF	318 <sup>th</sup> line GRAM Data
17'h13E00 ~ 17' h13EEF	319 <sup>th</sup> line GRAM Data
17'h13F00 ~ 17'h13FEF	320 <sup>th</sup> line GRAM Data

Note1: When the RGB interface is selected (RM = "1"), the address AD[16:0] is set to the address counter every frame on the falling edge of VSYNC.

### 8.2.19. Write Data to GRAM (R22h)

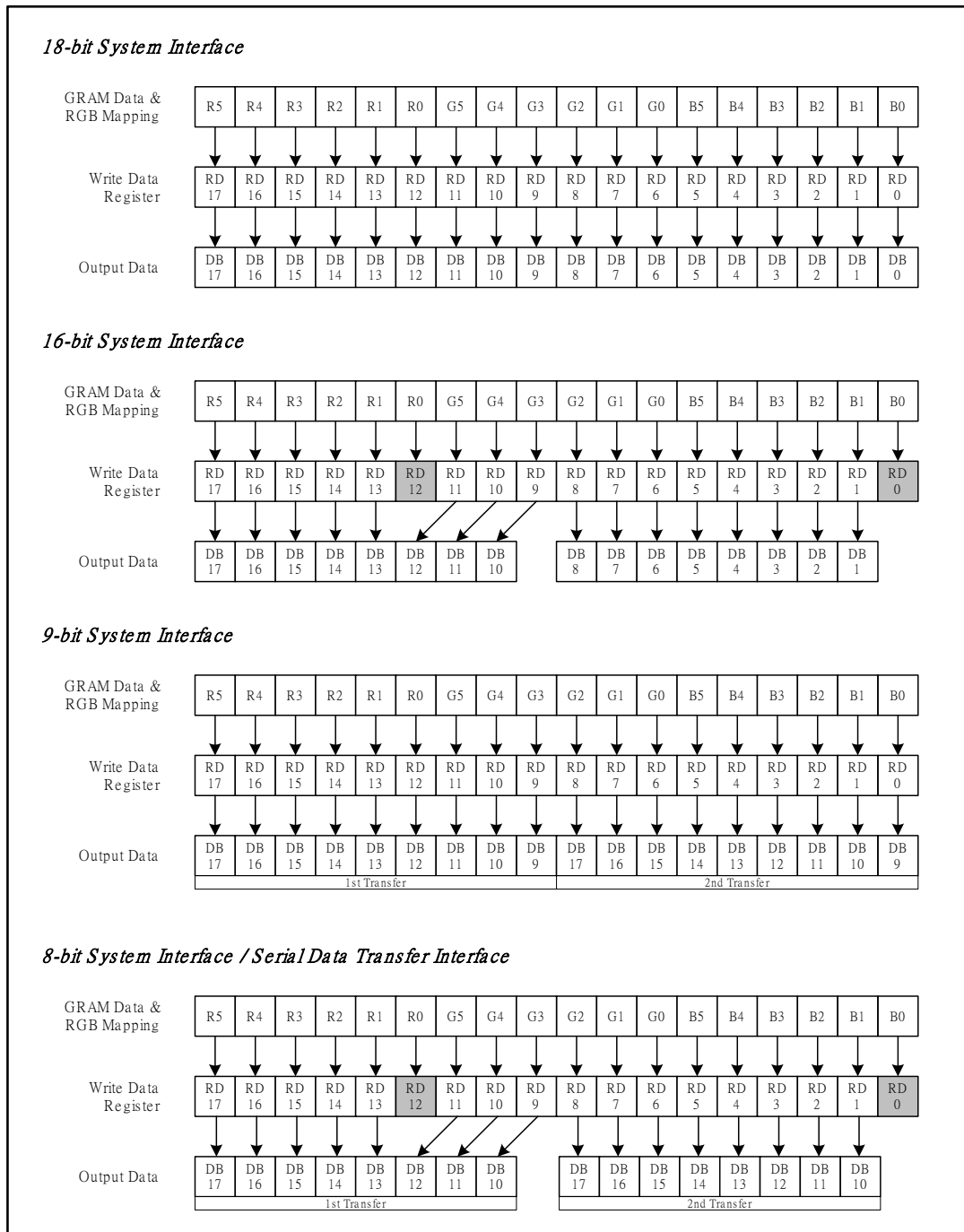
R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																	

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

### 8.2.20. Read Data from GRAM (R22h)

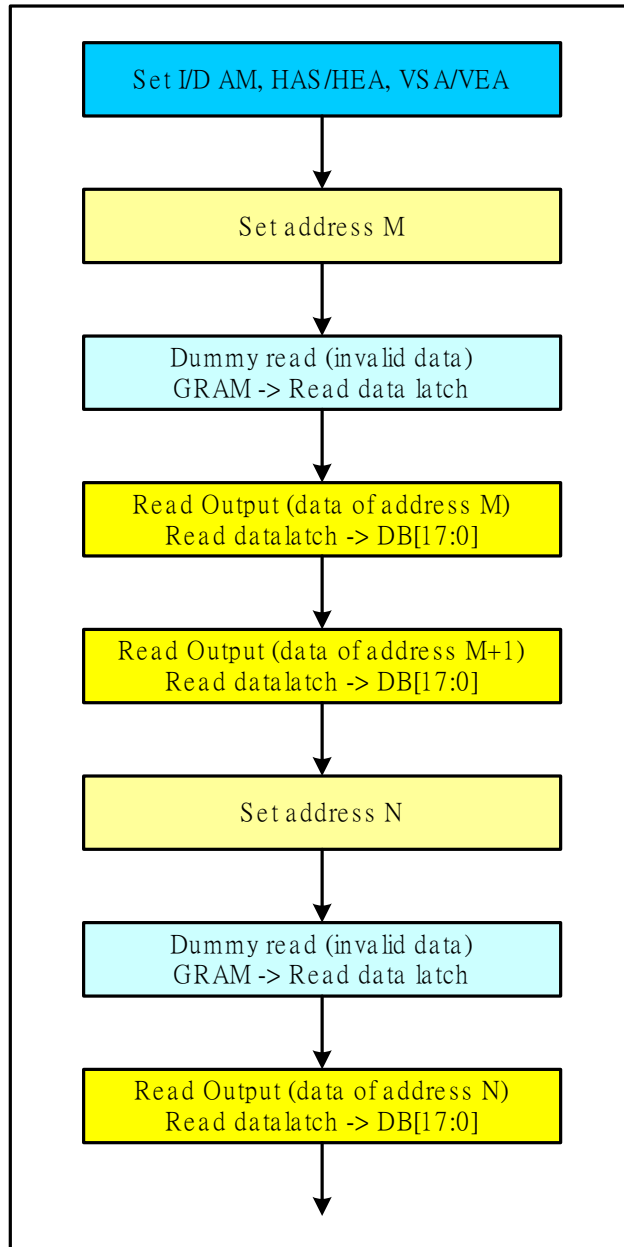
R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																	

**RD[17:0]** Read 18-bit data from GRAM through the read data register (RDR).



**Figure 27 Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit Interface Mode**





**Figure 28 GRAM Data Read Back Flow Chart**

**8.2.21. Power Control 7 (R29h)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

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Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
---------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

**VCM[5:0]** Set the internal VcomH voltage.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	VREG1OUT x 0.685
0	0	0	0	0	1	VREG1OUT x 0.690
0	0	0	0	1	0	VREG1OUT x 0.695
0	0	0	0	1	1	VREG1OUT x 0.700
0	0	0	1	0	0	VREG1OUT x 0.705
0	0	0	1	0	1	VREG1OUT x 0.710
0	0	0	1	1	0	VREG1OUT x 0.715
0	0	0	1	1	1	VREG1OUT x 0.720
0	0	1	0	0	0	VREG1OUT x 0.725
0	0	1	0	0	1	VREG1OUT x 0.730
0	0	1	0	1	0	VREG1OUT x 0.735
0	0	1	0	1	1	VREG1OUT x 0.740
0	0	1	1	0	0	VREG1OUT x 0.745
0	0	1	1	0	1	VREG1OUT x 0.750
0	0	1	1	1	0	VREG1OUT x 0.755
0	0	1	1	1	1	VREG1OUT x 0.760
0	1	0	0	0	0	VREG1OUT x 0.765
0	1	0	0	0	1	VREG1OUT x 0.770
0	1	0	0	1	0	VREG1OUT x 0.775
0	1	0	0	1	1	VREG1OUT x 0.780
0	1	0	1	0	0	VREG1OUT x 0.785
0	1	0	1	0	1	VREG1OUT x 0.790
0	1	0	1	1	0	VREG1OUT x 0.795
0	1	0	1	1	1	VREG1OUT x 0.800
0	1	1	0	0	0	VREG1OUT x 0.805
0	1	1	0	0	1	VREG1OUT x 0.810
0	1	1	0	1	0	VREG1OUT x 0.815
0	1	1	0	1	1	VREG1OUT x 0.820
0	1	1	1	0	0	VREG1OUT x 0.825
0	1	1	1	0	1	VREG1OUT x 0.830
0	1	1	1	1	0	VREG1OUT x 0.835
0	1	1	1	1	1	VREG1OUT x 0.840

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
1	0	0	0	0	0	VREG1OUT x 0.845
1	0	0	0	0	1	VREG1OUT x 0.850
1	0	0	0	1	0	VREG1OUT x 0.855
1	0	0	0	1	1	VREG1OUT x 0.860
1	0	0	1	0	0	VREG1OUT x 0.865
1	0	0	1	0	1	VREG1OUT x 0.870
1	0	0	1	1	0	VREG1OUT x 0.875
1	0	0	1	1	1	VREG1OUT x 0.880
1	0	1	0	0	0	VREG1OUT x 0.885
1	0	1	0	0	1	VREG1OUT x 0.890
1	0	1	0	1	0	VREG1OUT x 0.895
1	0	1	0	1	1	VREG1OUT x 0.900
1	0	1	1	0	0	VREG1OUT x 0.905
1	0	1	1	0	1	VREG1OUT x 0.910
1	0	1	1	1	0	VREG1OUT x 0.915
1	0	1	1	1	1	VREG1OUT x 0.920
1	1	0	0	0	0	VREG1OUT x 0.925
1	1	0	0	0	1	VREG1OUT x 0.930
1	1	0	0	1	0	VREG1OUT x 0.935
1	1	0	0	1	1	VREG1OUT x 0.940
1	1	0	1	0	0	VREG1OUT x 0.945
1	1	0	1	0	1	VREG1OUT x 0.950
1	1	0	1	1	0	VREG1OUT x 0.955
1	1	0	1	1	1	VREG1OUT x 0.960
1	1	1	0	0	0	VREG1OUT x 0.965
1	1	1	0	0	1	VREG1OUT x 0.970
1	1	1	0	1	0	VREG1OUT x 0.975
1	1	1	0	1	1	VREG1OUT x 0.980
1	1	1	1	0	0	VREG1OUT x 0.985
1	1	1	1	0	1	VREG1OUT x 0.990
1	1	1	1	1	0	VREG1OUT x 0.995
1	1	1	1	1	1	VREG1OUT x 1.000

**8.2.22. Frame Rate and Color Control (R2Bh)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0
Default		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

**FRS[4:0]** Set the frame rate when the internal resistor is used for oscillator circuit.

FRS[3:0]	FRS[3:0]	Frame Rate
0000	4'h0	31
0001	4'h1	33
0010	4'h2	34
0011	4'h3	36
0100	4'h4	39
0101	4'h5	41
0110	4'h6	44
0111	4'h7	48
1000	4'h8	52
1001	4'h9	57
1010	4'hA	62
1011	4'hB	69
1100	4'hC	78
1101	4'hD	89
1110	4'hE	Setting Prohibited
1111	4'hF	Setting Prohibited

**8.2.23. Gamma Control (R30h ~ R3Dh)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	----	-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

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R30h	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31h	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32h	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35h	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R36h	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37h	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38h	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39h	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3Ch	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3Dh	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

- KP5-0[2:0] :  $\gamma$  fine adjustment register for positive polarity
- RP1-0[2:0] :  $\gamma$  gradient adjustment register for positive polarity
- VRP1-0[4:0] :  $\gamma$  amplitude adjustment register for positive polarity
- KN5-0[2:0] :  $\gamma$  fine adjustment register for negative polarity
- RN1-0[2:0] :  $\gamma$  gradient adjustment register for negative polarity
- VRN1-0[4:0] :  $\gamma$  amplitude adjustment register for negative polarity

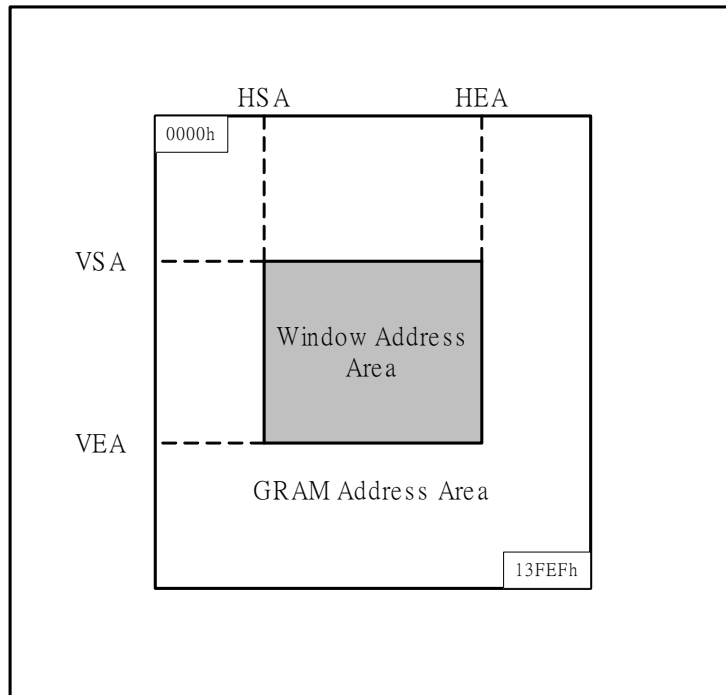
For details “ $\gamma$ -Correction Function” section.

### 8.2.24. Horizontal and Vertical RAM Address Position (R50h, R51h, R52h, R53h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R51h	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
R52h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R53h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
R50h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51h	Default		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R52h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53h	Default		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

**HSA[7:0]/HEA[7:0]** HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00”h ≤ HSA[7:0] < HEA[7:0] ≤ “EF”h. and “01”h ≤ HEA-HAS.

**VSA[8:0]/VEA[8:0]** VSA[8:0] and VEA[8:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure “000”h ≤ VSA[8:0] < VEA[8:0] ≤ “13F”h.



**Figure 29 GRAM Access Range Configuration**

$$"00"h \leq HSA[7:0] \leq HEA[7:0] \leq "EF"h$$

$$"00"h \leq VSA[8:0] \leq VEA[8:0] \leq "13F"h$$

*Note1. The window address range must be within the GRAM address space.*

*Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.*

**8.2.25. Gate Scan Control (R60h, R61h, R6Ah)**

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R60h	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R61h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
R6Ah	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R60h	Default		0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
R61h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6Ah	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**SCN[5:0]** The ILI9335 allows to specify the gate line from which the gate driver starts to scan by setting the SCN[5:0] bits.

SCN[5:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G320	G1	G320
01h	G9	G312	G17	G304
02h	G17	G304	G33	G288
03h	G25	G296	G49	G272
04h	G33	G288	G65	G256
05h	G41	G280	G81	G240
06h	G49	G272	G97	G224
07h	G57	G264	G113	G208
08h	G65	G256	G129	G192
09h	G73	G248	G145	G176
0Ah	G81	G240	G161	G160
0Bh	G89	G232	G177	G144
0Ch	G97	G224	G193	G128
0Dh	G105	G216	G209	G112
0Eh	G113	G208	G2	G96
0Fh	G121	G200	G18	G80
10h	G129	G192	G34	G64
11h	G137	G184	G50	G48
12h	G145	G176	G66	G32
13h	G153	G168	G82	G16
14h	G161	G160	G98	G319
15h	G169	G152	G114	G303
16h	G177	G144	G130	G287
17h	G185	G136	G146	G271
18h	G193	G128	G162	G255
19h	G201	G120	G178	G239
1Ah	G209	G112	G194	G223
1Bh	G217	G104	G114	G207
1Ch	G225	G96	G130	G191
1Dh	G233	G88	G146	G175
1Eh	G241	G80	G162	G159
1Fh	G249	G72	G178	G143
20h	G257	G64	G194	G127
21h	G265	G56	G210	G111
22h	G273	G48	G226	G95
23h	G281	G40	G242	G79
24h	G289	G32	G258	G63
25h	G297	G24	G274	G47
26h	G305	G16	G290	G31
27h	G313	G8	G306	G15
28h ~ 3Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Note: When SM=1, it is a interlacing scanning. Please reference page 72!

**NL[5:0]:** Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00	8 lines
6'h01	16 lines
6'h02	24lines
...	...
6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 line
6'h27	320 line
Others	Setting inhibited

**NDL:** Sets the source driver output level in the non-display area.

NDL	Non-Display Area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

**GS:** Sets the direction of scan by the gate driver in the range determined by SCN[4:0] and NL[4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G320.

When GS = 1, the scan direction is from G320 to G1

**REV:** Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	.	.	.
	.	.	.
	18'h3FFFF	V63	V0

**VLE:** Vertical scroll display enable bit. When VLE = 1, the ILI9335 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the

number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image Display
0	Fixed
1	Enable Scrolling

**VL[8:0]:** Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0] ≤ 320.

### 8.2.26. Partial Image 1 Display Position (R80h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTD P0[8]	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PTDP0[8:0]:** Sets the display start position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.

### 8.2.27. Partial Image 1 RAM Start/End Address (R81h, R82h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A0[8]	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
W	1	0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PTSA0[8:0] PTEA0[8:0]:** Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0].

### 8.2.28. Partial Image 2 Display Position (R83h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTD P1[8]	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PTDP1[8:0]:** Sets the display start position of partial image 2. The display areas of the partial images 1 and 2 must not overlap each another.

### 8.2.29. Partial Image 2 RAM Start/End Address (R84h, R85h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A1[8]	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PTSA1[8:0] PTEA1[8:0]:** Sets the start line address and the end line address of the RAM area storing the data of partial image 2. Make sure PTSA1[8:0] ≤ PTEA1[8:0].

### 8.2.30. Panel Interface Control 1 (R90h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIV11	DIV10	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

**RTNI[4:0]:** Sets 1H (line) clock number of internal clock operating mode. In this mode, ILI9335 display operation is synchronized with internal clock signal.

RTNI[4:0]	Clocks/Line	RTNI[4:0]	Clocks/Line
00000~01111	Setting Disabled	11000	24 clocks
10000	16 clocks	11001	25 clocks
10001	17 clocks	11010	26 clocks
10010	18 clocks	11011	27 clocks
10011	19 clocks	11100	28 clocks
10100	20 clocks	11101	29 clocks
10101	21 clocks	11110	30 clocks
10110	22 clocks	11111	31 clocks
10111	23 clocks		

**DIVI[1:0]:** Sets the division ratio of internal clock frequency.

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

### 8.2.31. Panel Interface Control 2 (R92h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

**NOWI[2:0]:** Sets the gate output non-overlap period when ILI9335 display operation is synchronized with internal clock signal.

NOWI[2:0]	Gate Non-overlap Period
000	Setting inhibited
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	Setting inhibited

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

### 8.2.32. Panel Interface Control 4 (R95h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

**DIVE[1:0]:** Sets the division ratio of DOTCLK when ILI9335 display operation is synchronized with RGB interface signals.



DIVE[1:0]	Division Ratio	18/16-bit RGB Interface	DOTCLK=5MHz	6-bit x 3 Transfers RGB Interface	DOTCLK=5MHz
00	Setting Prohibited	Setting Prohibited	-	Setting Prohibited	-
01	1/4	4 DOTCLKS	0.8 $\mu$ s	12 DOTCLKS	0.8 $\mu$ s
10	1/8	8 DOTCLKS	1.6 $\mu$ s	24 DOTCLKS	1.6 $\mu$ s
11	1/16	16 DOTCLKS	3.2 $\mu$ s	48 DOTCLKS	3.2 $\mu$ s

### 8.2.33. Panel Interface Control 5 (R97h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

**NOWE[3:0]:** Sets the gate output non-overlap period when the ILI9335 display operation is synchronized with RGB interface signals.

NOWE[3:0]	Gate Non-overlap Period	NOWE[3:0]	Gate Non-overlap Period
0000	Setting inhibited	1000	8 clocks
0001	1 clocks	1001	9 clocks
0010	2 clocks	1010	10 clocks
0011	3 clocks	1011	Setting inhibited
0100	4 clocks	1100	Setting inhibited
0101	5 clocks	1101	Setting inhibited
0110	6 clocks	1110	Setting inhibited
0111	7 clocks	1111	Setting inhibited

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

### 8.2.34. OTP VCM Programming Control (RA1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**OTP\_PGM\_EN:** OTP programming enable. When program OTP, must set this bit. OTP data can be programmed 3 times.

**VCM\_OTP[5:0]:** OTP programming data for VCOMH voltage, the voltage refer to VCM[5:0] value.

### 8.2.35. OTP VCM Status and Enable (RA2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PGM\_CNT[1:0]:** OTP programmed record. These bits are read only.

OTP_PGM_CNT[1:0]	Description
00	OTP clean
01	OTP programmed 1 time
10	OTP programmed 2 times
11	OTP programmed 3 times

**VCM\_D[5:0]:** OTP VCM data read value. These bits are read only.

**VCM\_EN:** OTP VCM data enable.

'1': Set this bit to enable OTP VCM data to replace R29h VCM value.

'0': Default value, use R29h VCM value.

**8.2.36. OTP Programming ID Key (RA5h)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**KEY[15:0]:** OTP Programming ID key protection. Before writing OTP programming data RA1h, it must write RA5h with 0xAA55 value first to make OTP programming successfully. If RA5h is not written with 0xAA55, OTP programming will be fail. See OTP Programming flow.

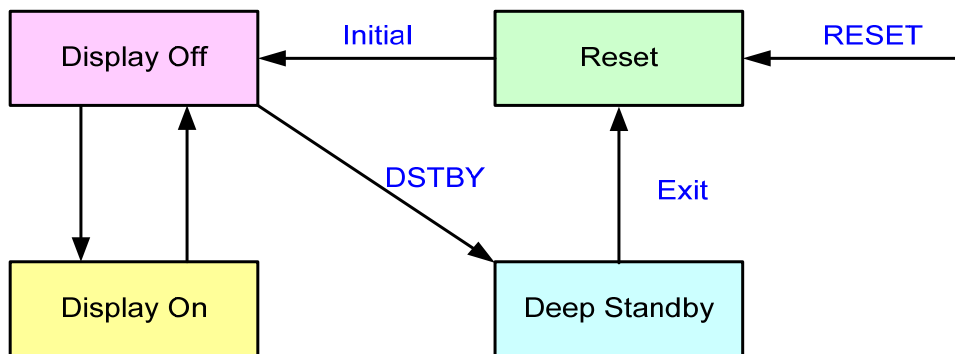
**8.2.37. Deep stand by control (RE6h)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

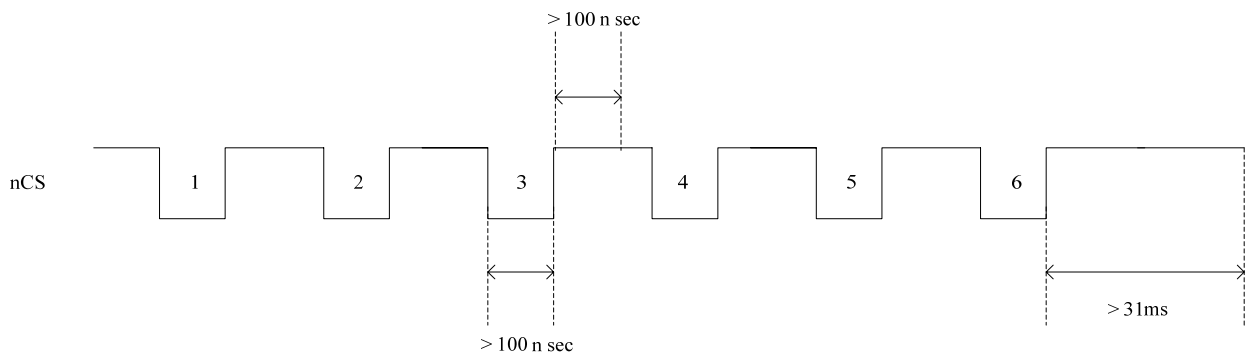
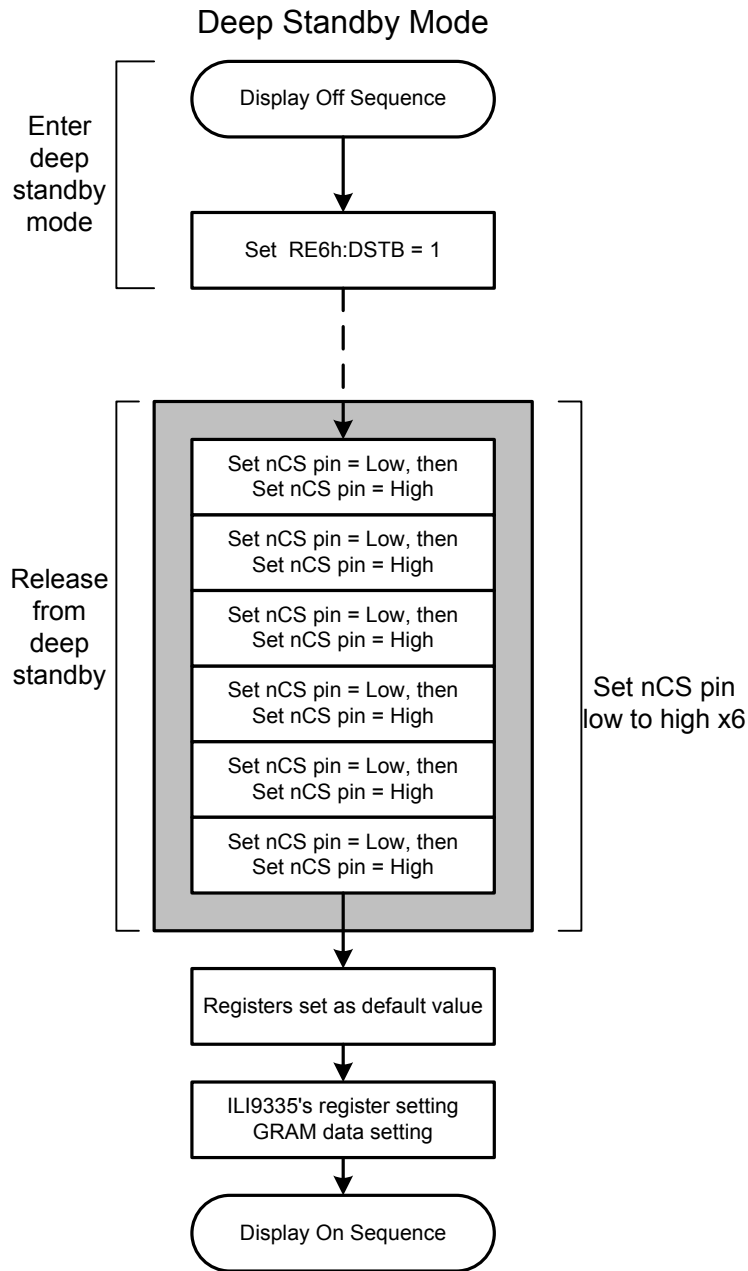
**DSTB:** When DSTB = 1, the ILI9335 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the ILI9335 enters the deep standby mode, and they must be reset after exiting deep standby mode.

**Basic operation**

The basic operation modes of 9335 are as shown in the following diagram.

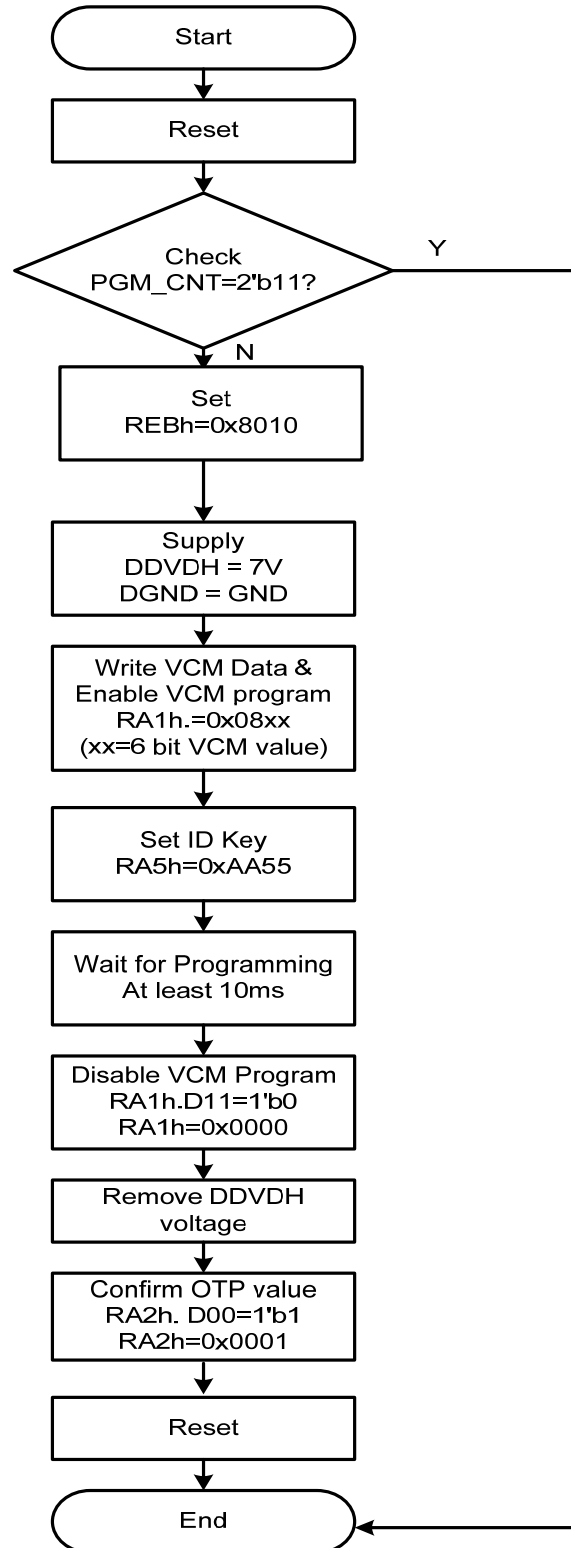


**CPU interface transition setting sequences**



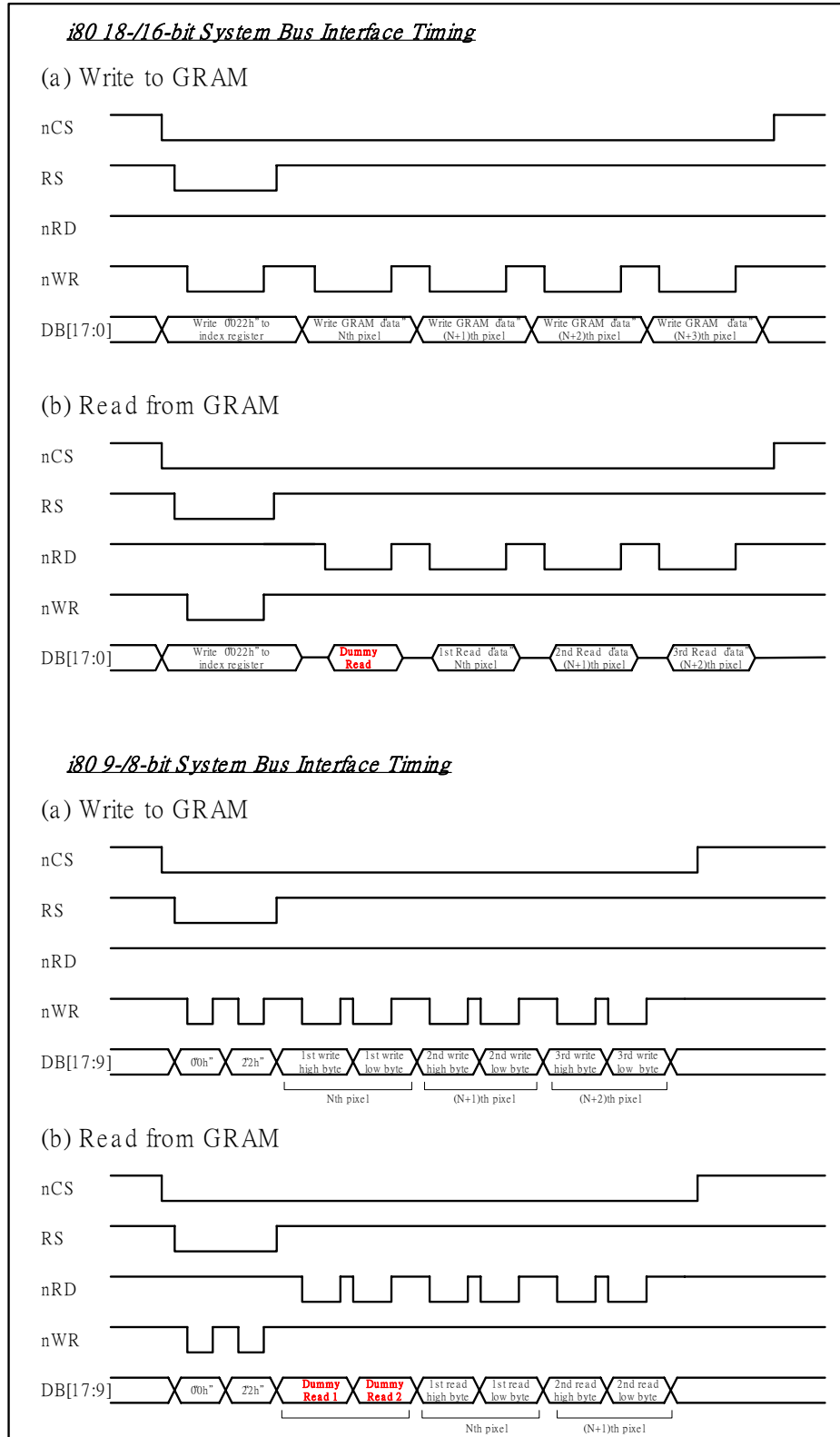
## 9. OTP Programming Flow

VCOMH OTP programming Flow



## 10. GRAM Address Map & Read/Write

ILI9335 has an internal graphics RAM (GRAM) of 172,800 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.

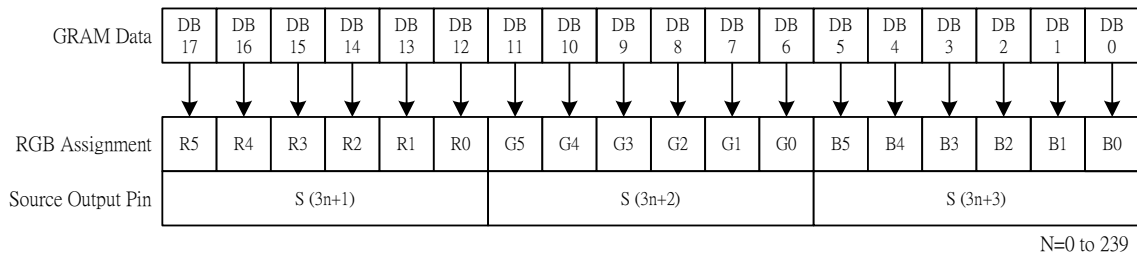


**Figure30 GRAM Read/Write Timing of i80-System Interface**

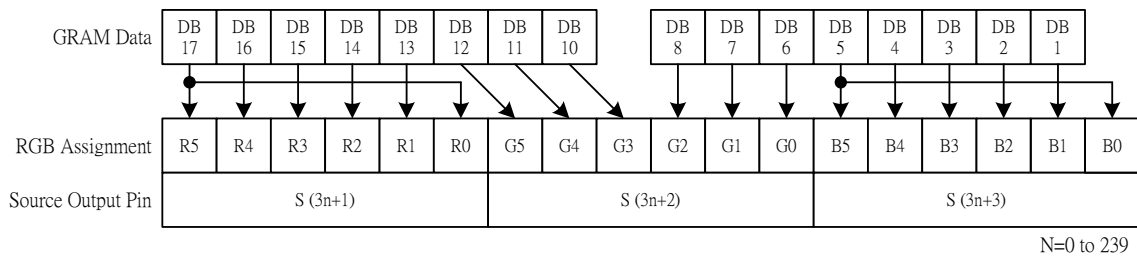
GRAM address map table of SS=0, BGR=0

SS=0, BGR=0	S1...S3	S4...S6	S7...S9	S10...S12	...	S517...S519	S520...S522	S523...S525	S526...S720	
GS=0	GS=1	DB17...0	DB17...0	DB17...0	DB17...0	...	DB17...0	DB17...0	DB17...0	DB17...0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	...	"000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	...	"001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	...	"002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	...	"003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	...	"004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	...	"005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	...	"006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	...	"007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	...	"008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	...	"009ECh"	"009EDh"	"009EEh"	"009EFh"
.	.	.	.	.	.	...	.	.	.	.
.	.	.	.	.	.	...	.	.	.	.
.	.	.	.	.	.	...	.	.	.	.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	...	"136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	...	"137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	...	"138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	...	"139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	...	"13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	...	"13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	...	"13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	...	"13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	...	"13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	...	"13FECh"	"13FEDh"	"13FEEh"	"13FEFh"

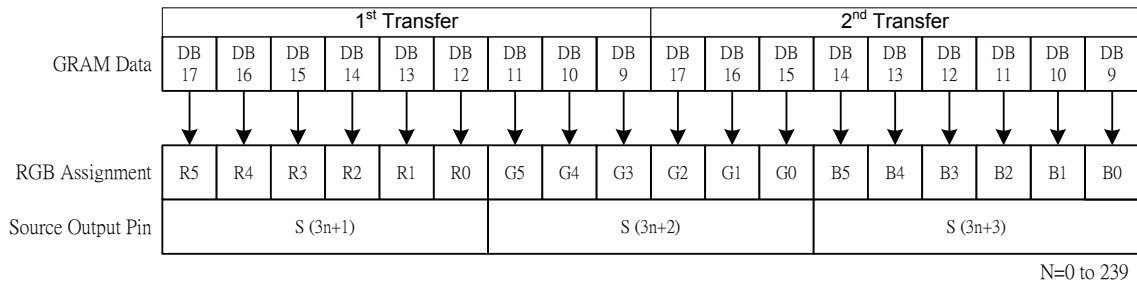
*i80/M68 system 18-bit data bus interface*



*i80/M68 system 16-bit data bus interface*



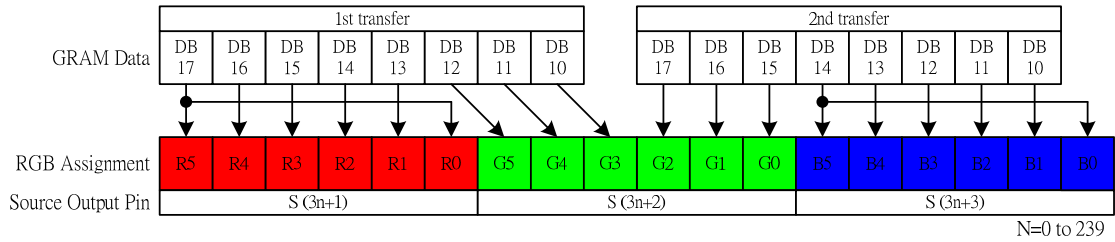
*i80/M68 system 9-bit data bus interface*



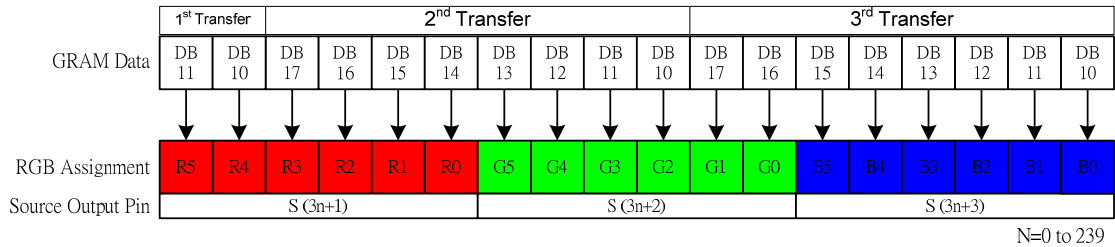
GRAM Data and display data of 18-/16-/9-bit system interface (SS=" 0", BGR=" 0")

**Figure31 i80-System Interface with 18-/16-/9-bit Data Bus (SS="0", BGR="0")**

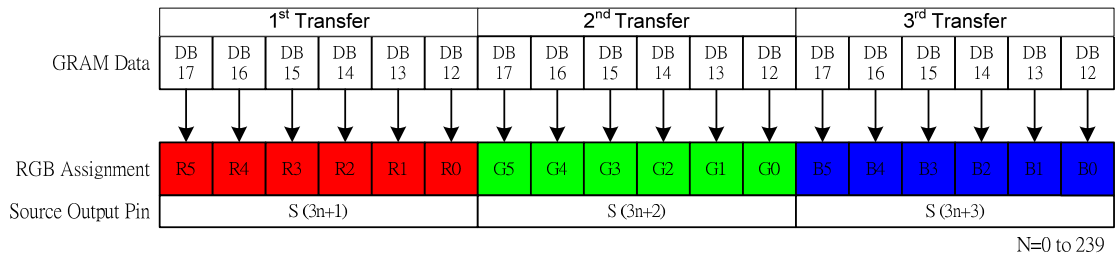
*i80M68 system 8-bit interface / SPI Interface (2 transfers/pixel)*



*i80M68 system 8-bit interface (3 transfers/pixel, TRI=" 1", DFM[1:0]=" 00")*



*i80M68 system 8-bit interface (3 transfers/pixel, TRI=" 1", DFM[1:0]=" 10")*



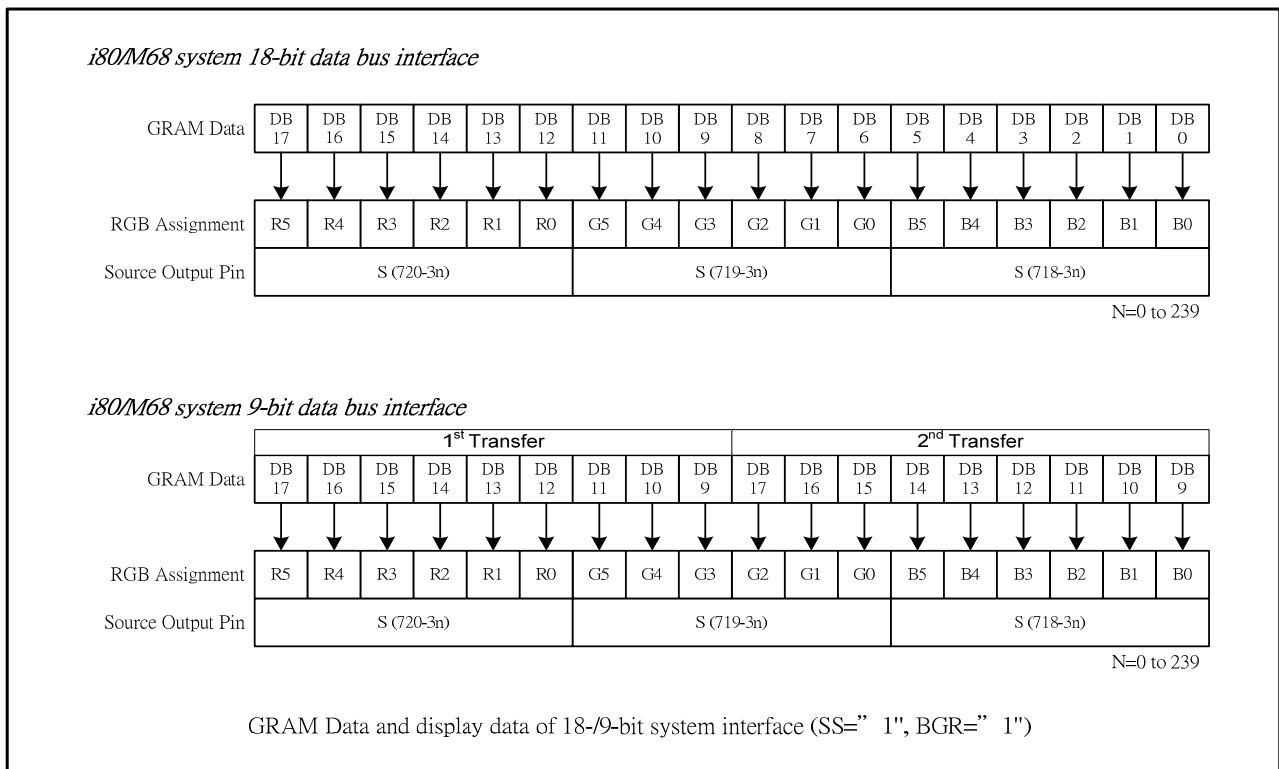
*i80M68 system 8-bit interface (SS=" 0", BGR=" 0")*

**Figure32 i80-System Interface with 8-bit Data Bus (SS="0", BGR="0")**



GRAM address map table of SS=1, BGR=1

SS=1, BGR=1	S720...S718	S717...S715	S714...S712	S711...S709	...	S12...S10	S9...S7	S6...S4	S3...S1
GS=0	GS=1	DB17...0	DB17...0	DB17...0	DB17...0	...	DB17...0	DB17...0	DB17...0
G1	G320	"0000h"	"00001h"	"00002h"	"00003h"	...	"000ECh"	"000EDh"	"000EEh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	...	"001ECh"	"001EDh"	"001EEh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	...	"002ECh"	"002EDh"	"002EEh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	...	"003ECh"	"003EDh"	"003EEh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	...	"004ECh"	"004EDh"	"004EEh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	...	"005ECh"	"005EDh"	"005EEh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	...	"006ECh"	"006EDh"	"006EEh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	...	"007ECh"	"007EDh"	"007EEh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	...	"008ECh"	"008EDh"	"008EEh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	...	"009ECh"	"009EDh"	"009EEh"
.	.	.	.	.	.	...	.	.	.
.	.	.	.	.	.	...	.	.	.
.	.	.	.	.	.	...	.	.	.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	...	"136ECh"	"136EDh"	"136EEh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	...	"137ECh"	"137EDh"	"137EEh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	...	"138ECh"	"138EDh"	"138EEh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	...	"139ECh"	"139EDh"	"139EEh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	...	"13AECh"	"13AEDh"	"13AEEh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	...	"13BECh"	"13BEDh"	"13BEEh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	...	"13CECh"	"13CEDh"	"13CEEh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	...	"13DECh"	"13DEDh"	"13DEEh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	...	"13EECh"	"13EEDh"	"13EEEh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	...	"13FECh"	"13FEDh"	"13FEEh"



**Figure 33 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")**

## 11. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[8:0], end: VEA[8:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9335 to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the GRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

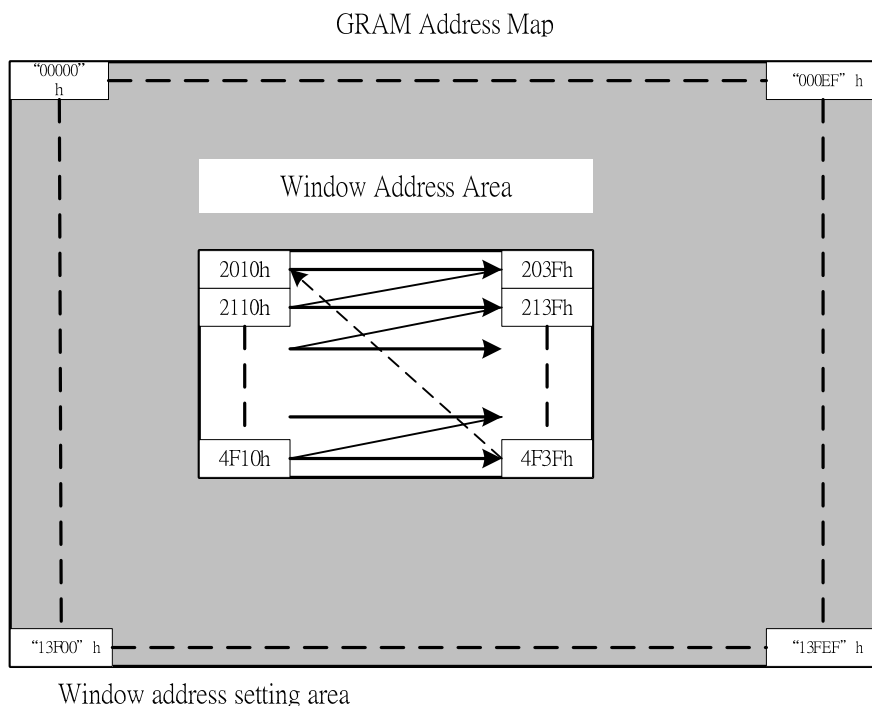
(Horizontal direction)  $00H \leq HSA[7:0] \leq HEA[7:0] \leq "EF"H$

(Vertical direction)  $00H \leq VSA[8:0] \leq VEA[8:0] \leq "13F"H$

[RAM address, AD (an address within a window address area)]

(RAM address)  $HSA[7:0] \leq AD[7:0] \leq HEA[7:0]$

$VSA[8:0] \leq AD[15:8] \leq VEA[8:0]$



HSA[7:0] = 10h, HEA[7:0] = 3Fh, I/D = 1 (increment)  
VSA[8:0] = 20h, VEA[8:0] = 4Fh, AM = 0 (horizontal writing)

**Figure 34 GRAM Access Window Map**

## 12. Gamma Correction

ILI9335 incorporates the  $\gamma$ -correction function to display 262,144 colors for the LCD panel. The  $\gamma$ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9335 available with liquid crystal panels of various characteristics.

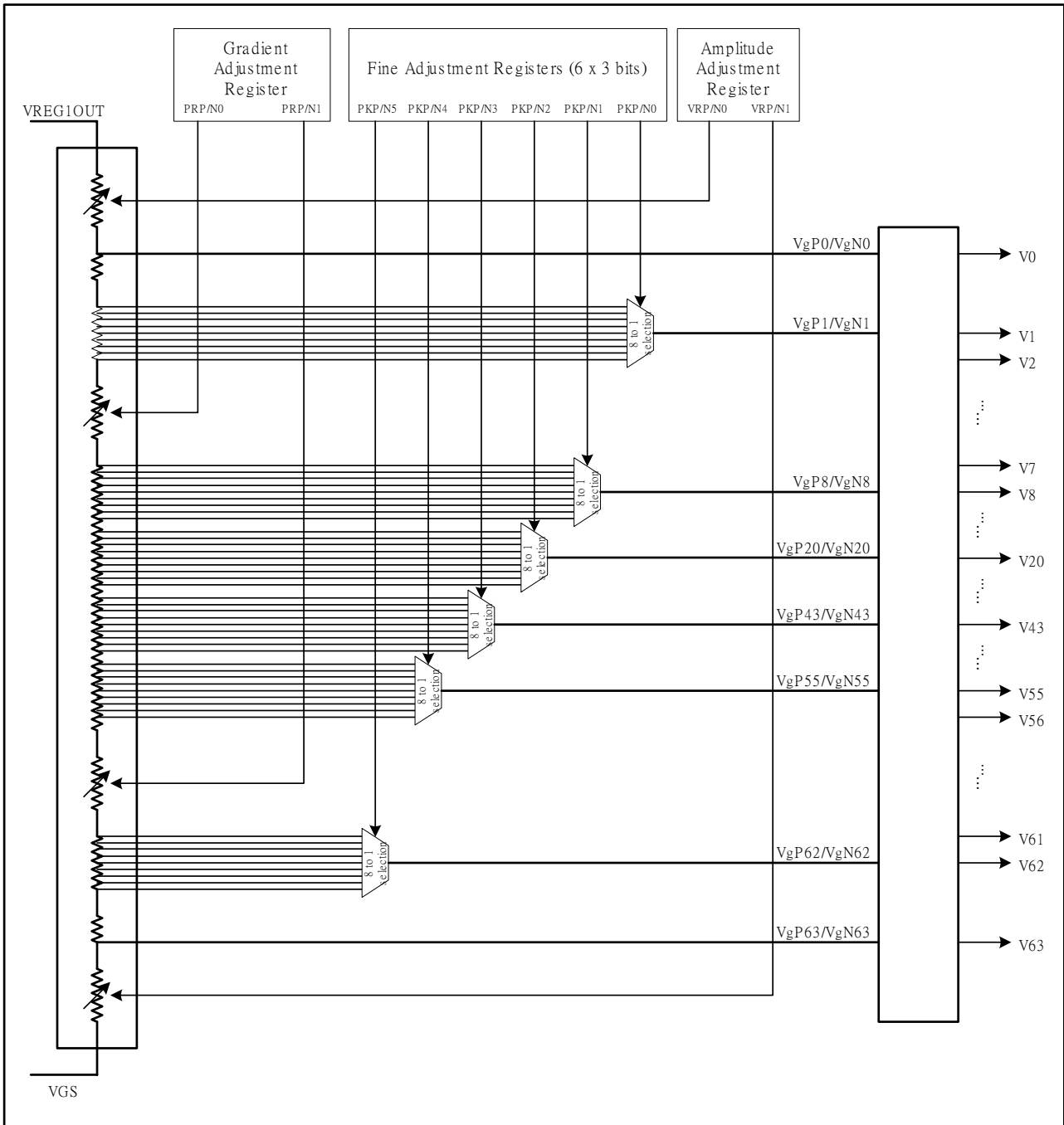
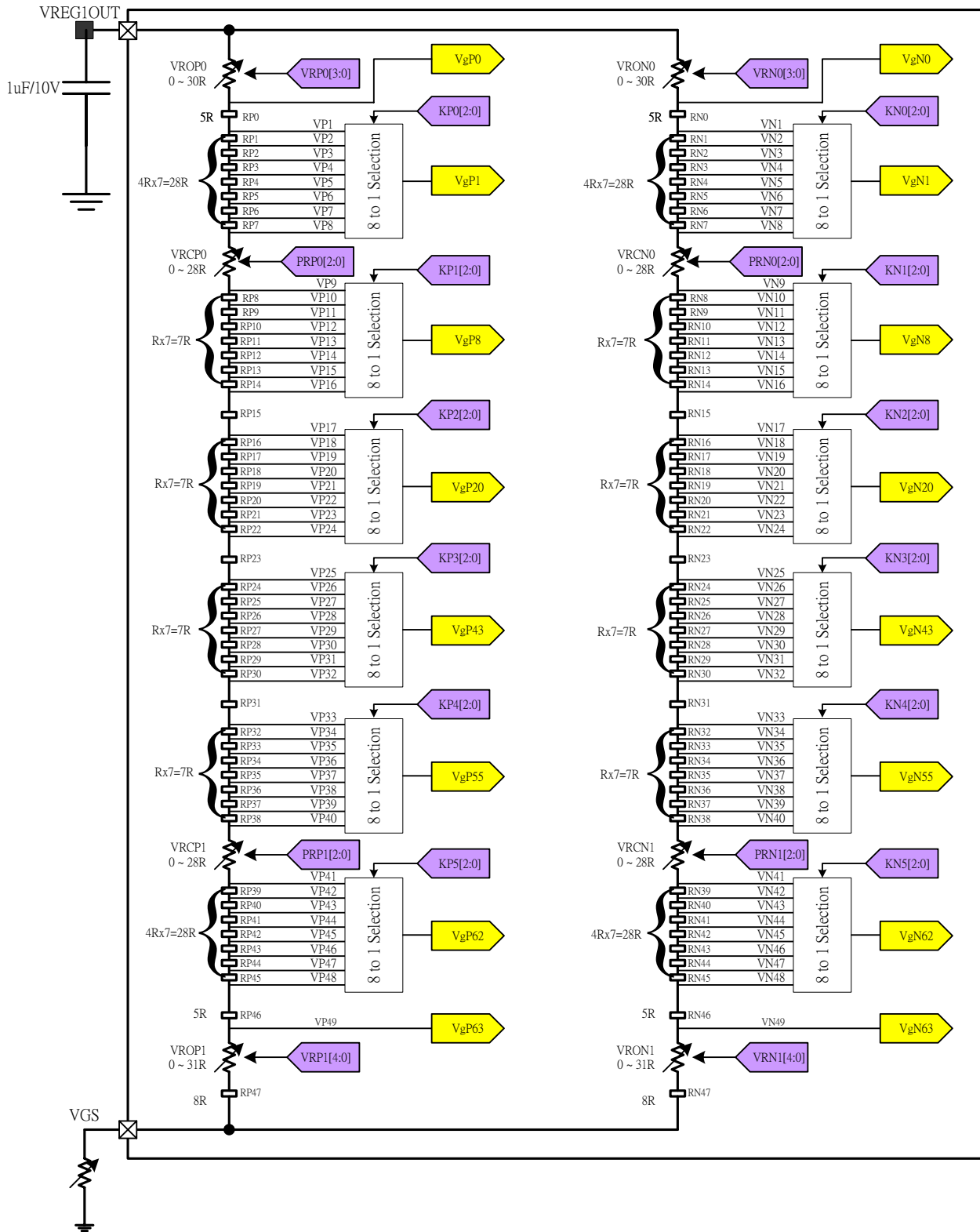


Figure 35 Grayscale Voltage Generation



**Figure 36 Grayscale Voltage Adjustment**

1. Gradient adjustment registers

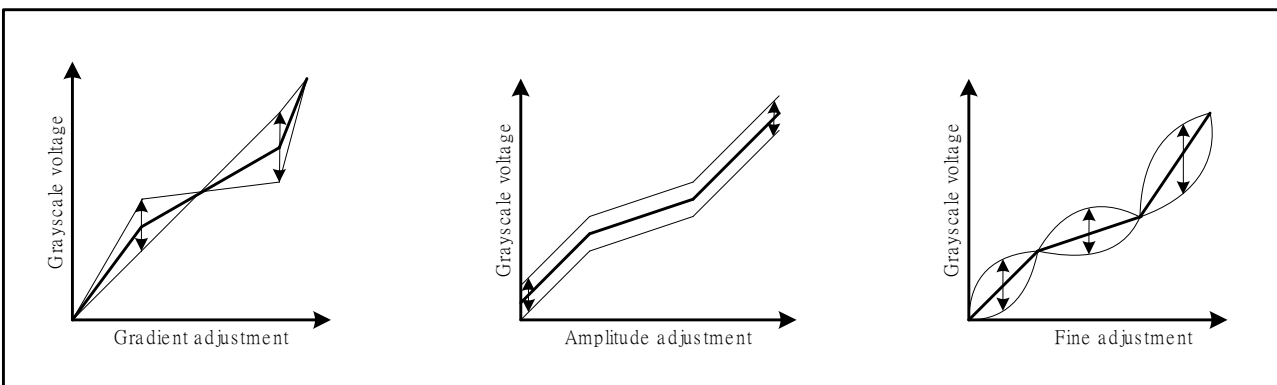
The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.



**Figure 37 Gamma Curve Adjustment**

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRCP0, VRCN0
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VROP0, VRON0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

**Ladder resistors and 8-to-1 selector Block configuration**

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the  $\gamma$ -correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

**Variable resistors**

ILI9335 uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment	
PRP(N)0/1[2:0] Register	VRCP(N)0/1 Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Amplitude adjustment (1)	
VRP(N)0[3:0] Register	VROP(N)0 Resistance
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1111	28R
1111	30R

Amplitude adjustment (2)	
VRP(N)1[4:0] Register	VROP(N)1 Resistance
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

**8-to-1 selectors**

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	Selected Voltage					
KP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Fine adjustment registers and selected resistor						
Register	Selected Resistor					
KP(N)[2:0]	RMP(N)0	RMP(N)1	RMP(N)2	RMP(N)3	RMP(N)4	RMP(N)5
000	0R	0R	0R	0R	0R	0R
001	4R	1R	1R	1R	1R	4R
010	8R	2R	2R	2R	2R	8R
011	12R	3R	3R	3R	3R	12R
100	16R	4R	4R	4R	4R	16R
101	20R	5R	5R	5R	5R	20R
110	24R	6R	6R	6R	6R	24R
111	28R	7R	7R	7R	7R	28R

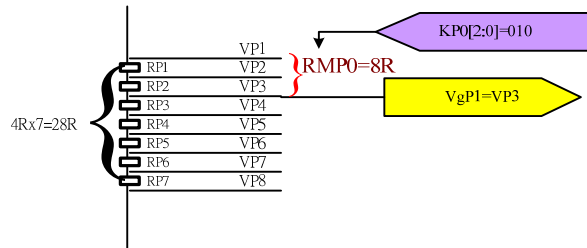


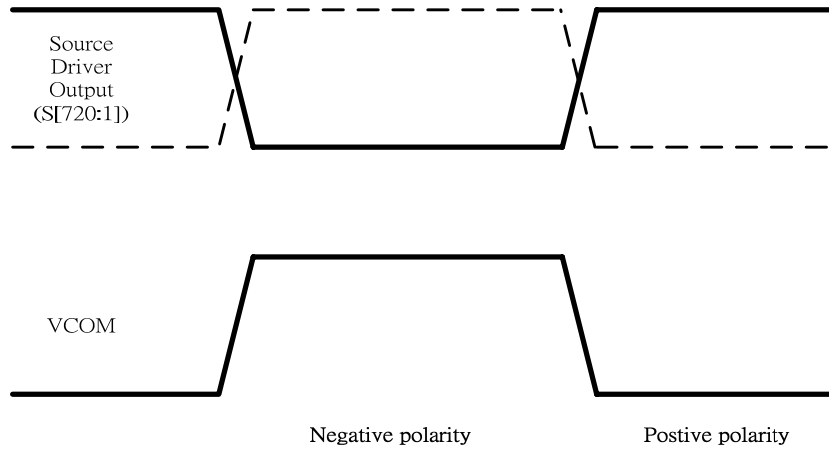
Figure 38 Example of RMP(N)0~5 definition

**Gamma correction resistor ratio**

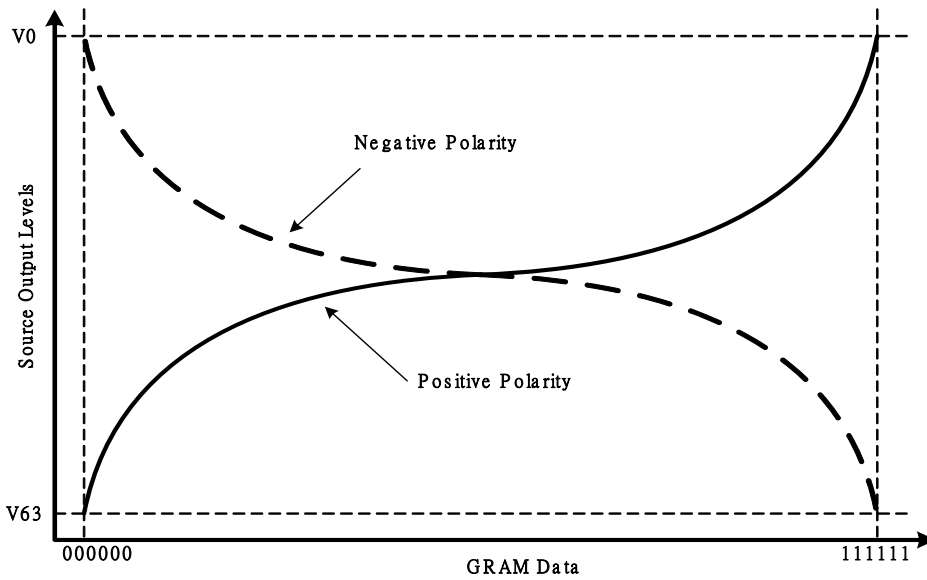
Data	Positive polarity output voltage		Negative polarity output voltage	
00h	VP0	(VgP0)	VN0	(VgN0)
01h	VP1	(VgP1)	VN1	(VgN1)
02h	VP2	$(VP8+(VP1-VP8)*(30/48))$	VN2	$(VN8+(VN1-VN8)*(30/48))$
03h	VP3	$(VP8+(VP1-VP8)*(23/48))$	VN3	$(VN8+(VN1-VN8)*(23/48))$
04h	VP4	$(VP8+(VP1-VP8)*(16/48))$	VN4	$(VN8+(VN1-VN8)*(16/48))$
05h	VP5	$(VP8+(VP1-VP8)*(12/48))$	VN5	$(VN8+(VN1-VN8)*(12/48))$
06h	VP6	$(VP8+(VP1-VP8)*(8/48))$	VN6	$(VN8+(VN1-VN8)*(8/48))$
07h	VP7	$(VP8+(VP1-VP8)*(4/48))$	VN7	$(VN8+(VN1-VN8)*(4/48))$
08h	VP8	(VgP8)	VN8	(VgN8)
09h	VP9	$VP20+(VP8-VP20)*(22/24)$	VN9	$VN20+(VN8-VN20)*(22/24)$
0Ah	VP10	$VP20+(VP8-VP20)*(20/24)$	VN10	$VN20+(VN8-VN20)*(20/24)$
0Bh	VP11	$VP20+(VP8-VP20)*(18/24)$	VN11	$VN20+(VN8-VN20)*(18/24)$
0Ch	VP12	$VP20+(VP8-VP20)*(16/24)$	VN12	$VN20+(VN8-VN20)*(16/24)$
0Dh	VP13	$VP20+(VP8-VP20)*(14/24)$	VN13	$VN20+(VN8-VN20)*(14/24)$
0Eh	VP14	$VP20+(VP8-VP20)*(12/24)$	VN14	$VN20+(VN8-VN20)*(12/24)$
0Fh	VP15	$VP20+(VP8-VP20)*(10/24)$	VN15	$VN20+(VN8-VN20)*(10/24)$
10h	VP16	$VP20+(VP8-VP20)*(8/24)$	VN16	$VN20+(VN8-VN20)*(8/24)$
11h	VP17	$VP20+(VP8-VP20)*(6/24)$	VN17	$VN20+(VN8-VN20)*(6/24)$
12h	VP18	$VP20+(VP8-VP20)*(4/24)$	VN18	$VN20+(VN8-VN20)*(4/24)$
13h	VP19	$VP20+(VP8-VP20)*(2/24)$	VN19	$VN20+(VN8-VN20)*(2/24)$
14h	VP20	(VgP20)	VN20	(VgN20)
15h	VP21	$(VP43+(VP20-VP43)*(22/23))$	VN21	$(VN43+(VN20-VN43)*(22/23))$
16h	VP22	$(VP43+(VP20-VP43)*(21/23))$	VN22	$(VN43+(VN20-VN43)*(21/23))$
17h	VP23	$(VP43+(VP20-VP43)*(20/23))$	VN23	$(VN43+(VN20-VN43)*(20/23))$
18h	VP24	$(VP43+(VP20-VP43)*(19/23))$	VN24	$(VN43+(VN20-VN43)*(19/23))$
19h	VP25	$(VP43+(VP20-VP43)*(18/23))$	VN25	$(VN43+(VN20-VN43)*(18/23))$
1Ah	VP26	$(VP43+(VP20-VP43)*(17/23))$	VN26	$(VN43+(VN20-VN43)*(17/23))$
1Bh	VP27	$(VP43+(VP20-VP43)*(16/23))$	VN27	$(VN43+(VN20-VN43)*(16/23))$
1Ch	VP28	$(VP43+(VP20-VP43)*(15/23))$	VN28	$(VN43+(VN20-VN43)*(15/23))$
1Dh	VP29	$(VP43+(VP20-VP43)*(14/23))$	VN29	$(VN43+(VN20-VN43)*(14/23))$
1Eh	VP30	$(VP43+(VP20-VP43)*(13/23))$	VN30	$(VN43+(VN20-VN43)*(13/23))$
1Fh	VP31	$(VP43+(VP20-VP43)*(12/23))$	VN31	$(VN43+(VN20-VN43)*(12/23))$



Data	Positive polarity output voltage		Negative polarity output voltage	
20h	VP32	$(VP43+(VP20-VP43)*(11/23))$	VN32	$(VN43+(VN20-VN43)*(11/23))$
21h	VP33	$(VP43+(VP20-VP43)*(10/23))$	VN33	$(VN43+(VN20-VN43)*(10/23))$
22h	VP34	$(VP43+(VP20-VP43)*(9/23))$	VN34	$(VN43+(VN20-VN43)*(9/23))$
23h	VP35	$(VP43+(VP20-VP43)*(8/23))$	VN35	$(VN43+(VN20-VN43)*(8/23))$
24h	VP36	$(VP43+(VP20-VP43)*(7/23))$	VN36	$(VN43+(VN20-VN43)*(7/23))$
25h	VP37	$(VP43+(VP20-VP43)*(6/23))$	VN37	$(VN43+(VN20-VN43)*(6/23))$
26h	VP38	$(VP43+(VP20-VP43)*(5/23))$	VN38	$(VN43+(VN20-VN43)*(5/23))$
27h	VP39	$(VP43+(VP20-VP43)*(4/23))$	VN39	$(VN43+(VN20-VN43)*(4/23))$
28h	VP40	$(VP43+(VP20-VP43)*(3/23))$	VN40	$(VN43+(VN20-VN43)*(3/23))$
29h	VP41	$(VP43+(VP20-VP43)*(2/23))$	VN41	$(VN43+(VN20-VN43)*(2/23))$
2Ah	VP42	$(VP43+(VP20-VP43)*(1/23))$	VN42	$(VN43+(VN20-VN43)*(1/23))$
2Bh	VP43	(VgP43)	VN43	(VgN43)
2Ch	VP44	$(VP55+(VP43-VP55)*(22/24))$	VN44	$(VN55+(VN43-VN55)*(22/24))$
2Dh	VP45	$(VP55+(VP43-VP55)*(20/24))$	VN45	$(VN55+(VN43-VN55)*(20/24))$
2Eh	VP46	$(VP55+(VP43-VP55)*(18/24))$	VN46	$(VN55+(VN43-VN55)*(18/24))$
2Fh	VP47	$(VP55+(VP43-VP55)*(16/24))$	VN47	$(VN55+(VN43-VN55)*(16/24))$
30h	VP48	$(VP55+(VP43-VP55)*(14/24))$	VN48	$(VN55+(VN43-VN55)*(14/24))$
31h	VP49	$(VP55+(VP43-VP55)*(12/24))$	VN49	$(VN55+(VN43-VN55)*(12/24))$
32h	VP50	$(VP55+(VP43-VP55)*(10/24))$	VN50	$(VN55+(VN43-VN55)*(10/24))$
33h	VP51	$(VP55+(VP43-VP55)*(8/24))$	VN51	$(VN55+(VN43-VN55)*(8/24))$
34h	VP52	$(VP55+(VP43-VP55)*(6/24))$	VN52	$(VN55+(VN43-VN55)*(6/24))$
35h	VP53	$(VP55+(VP43-VP55)*(4/24))$	VN53	$(VN55+(VN43-VN55)*(4/24))$
36h	VP54	$(VP55+(VP43-VP55)*(2/24))$	VN54	$(VN55+(VN43-VN55)*(2/24))$
37h	VP55	(VgP55)	VN55	(VgN55)
38h	VP56	$(VP62+(VP55-VP62)*(44/48))$	VN56	$(VN62+(VN55-VN62)*(44/48))$
39h	VP57	$(VP62+(VP55-VP62)*(40/48))$	VN57	$(VN62+(VN55-VN62)*(40/48))$
3Ah	VP58	$(VP62+(VP55-VP62)*(36/48))$	VN58	$(VN62+(VN55-VN62)*(36/48))$
3Bh	VP59	$(VP62+(VP55-VP62)*(32/48))$	VN59	$(VN62+(VN55-VN62)*(32/48))$
3Ch	VP60	$(VP62+(VP55-VP62)*(25/48))$	VN60	$(VN62+(VN55-VN62)*(25/48))$
3Dh	VP61	$(VP62+(VP55-VP62)*(18/48))$	VN61	$(VN62+(VN55-VN62)*(18/48))$
3Eh	VP62	(VgP62)	VN62	(VgN62)
3Fh	VP63	(VgP63)	VN63	(VgN63)



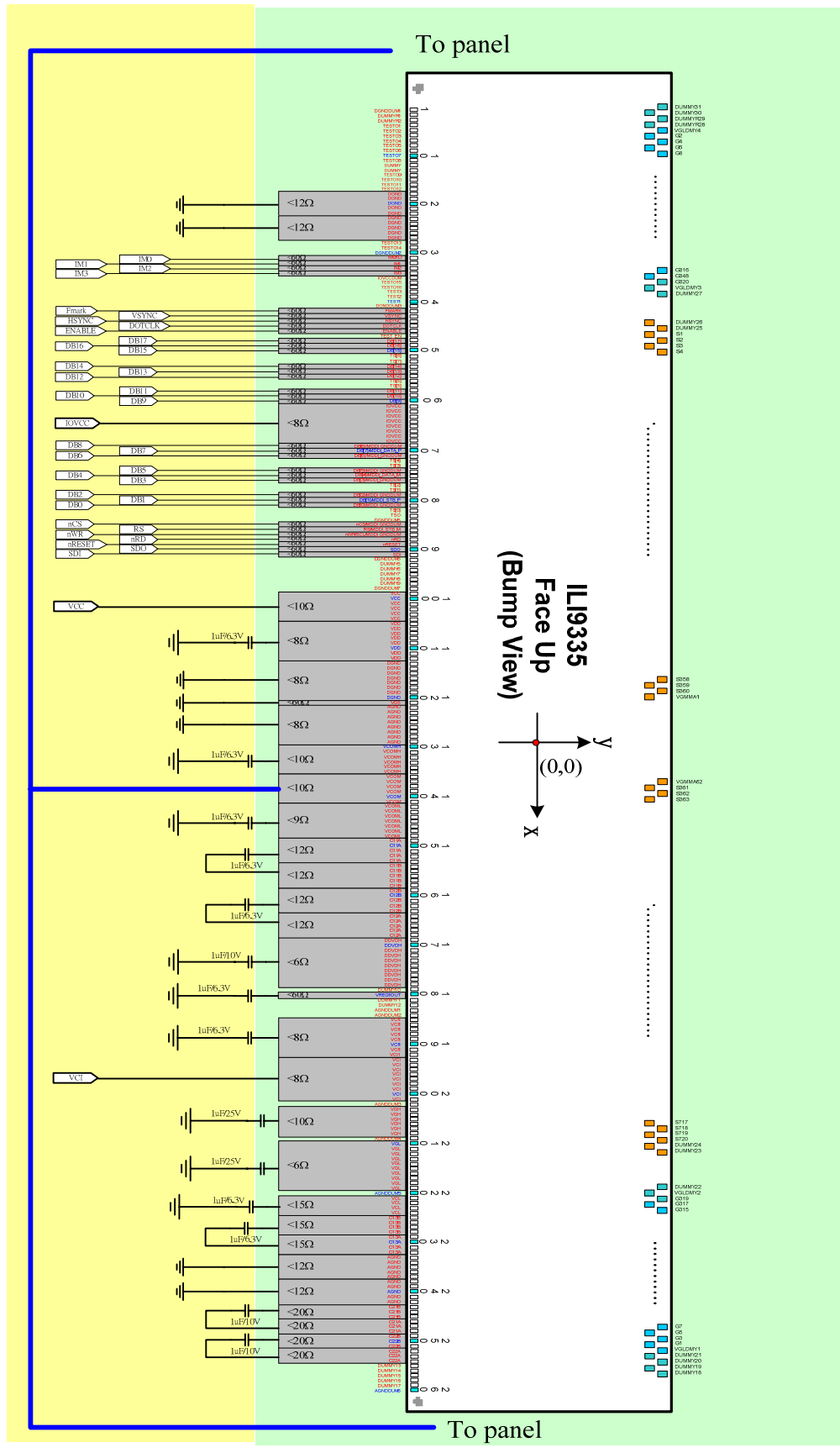
**Figure 39 Relationship between Source Output and VCOM**



**Figure 40 Relationship between GRAM Data and Output Level**

# 13. Application

## 13.1. Configuration of Power Supply Circuit



**Figure 41 Power Supply Circuit Block**

The following table shows specifications of external elements connected to the ILI9335's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 $\mu$ F (B characteristics)	6.3V	VREG1OUT, VCI1, VDD, VCL, VCOMH, VCOML, C11A/B, C12 A/B, C13 A/B,
	10V	DDVDH, C21 A/B, C22 A/B
	25V	VGH, VGL

### 13.2. Display ON/OFF Sequence

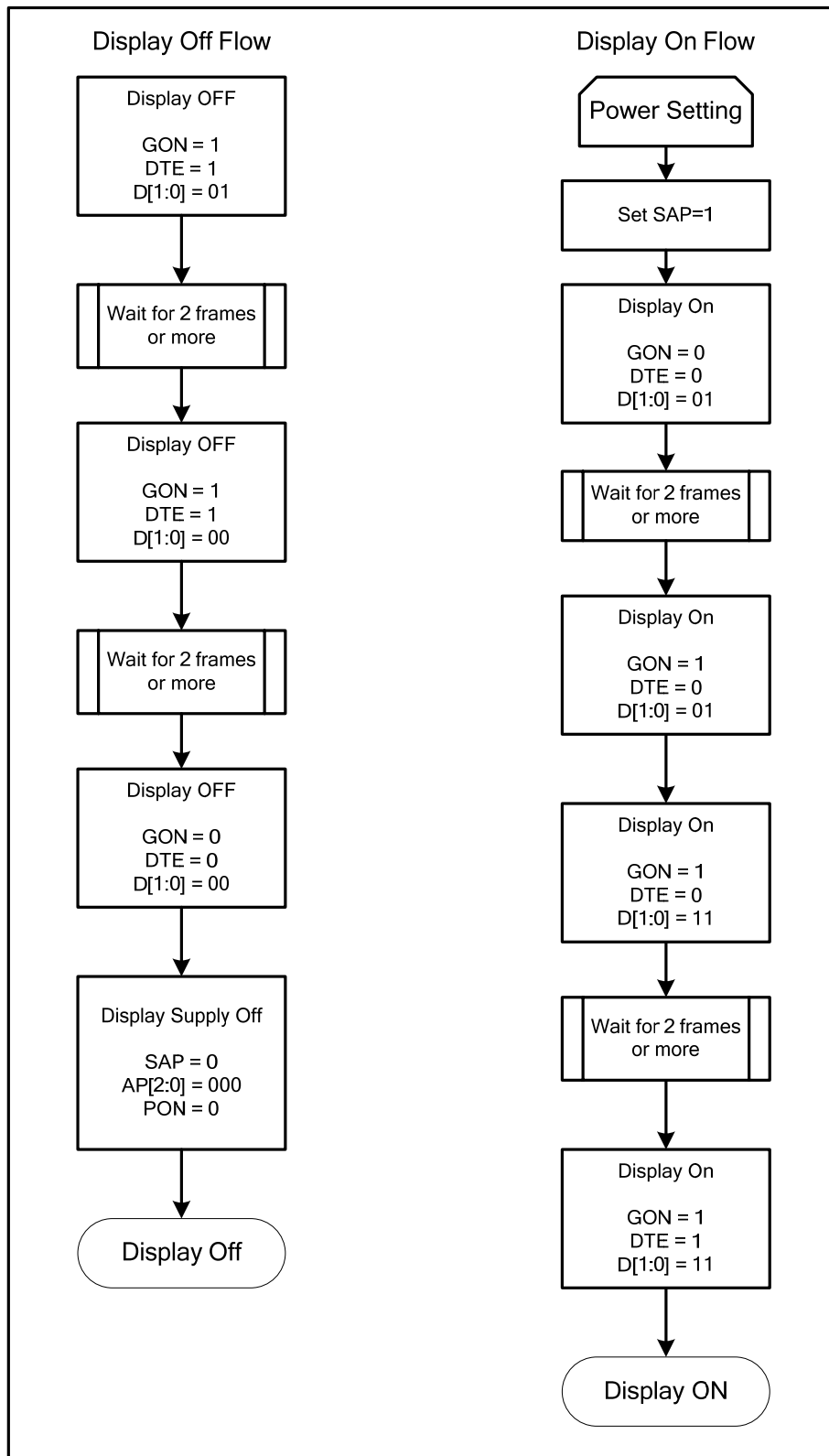
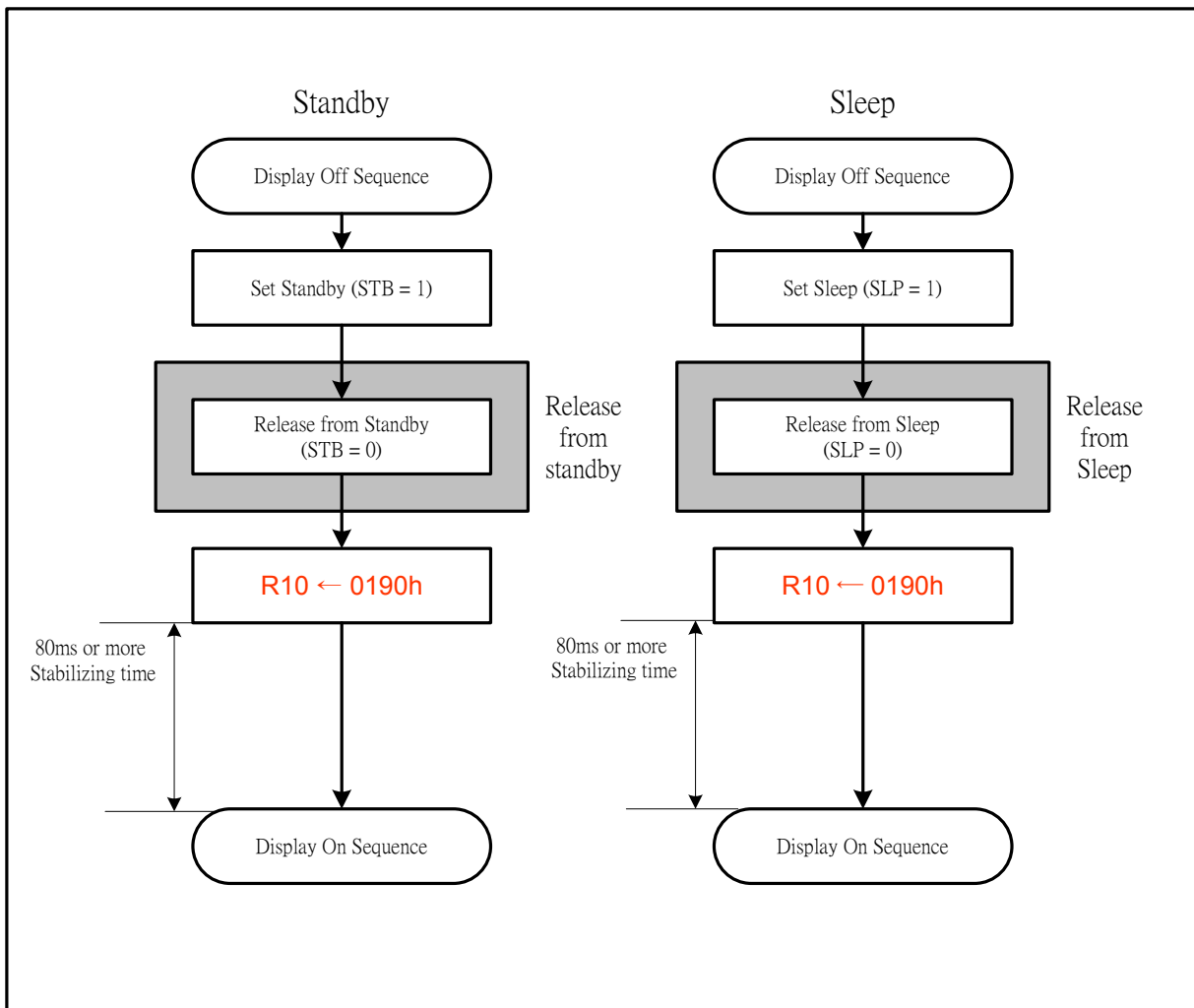


Figure 42 Display On/Off Register Setting Sequence

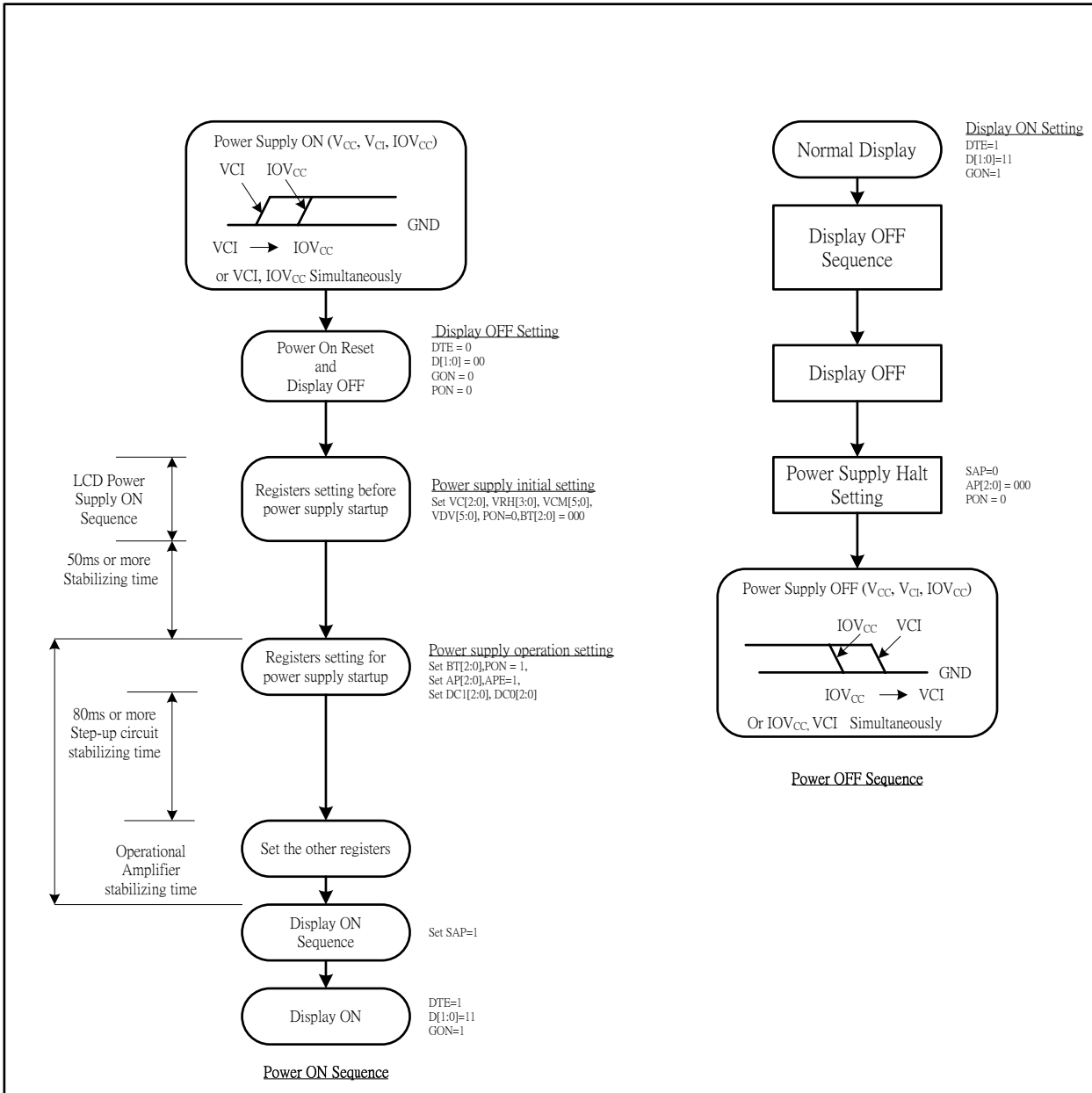
### 13.3. Standby and Sleep Mode



**Figure 43 Standby/Sleep Mode Register Setting Sequence**

### 13.4. Power Supply Configuration

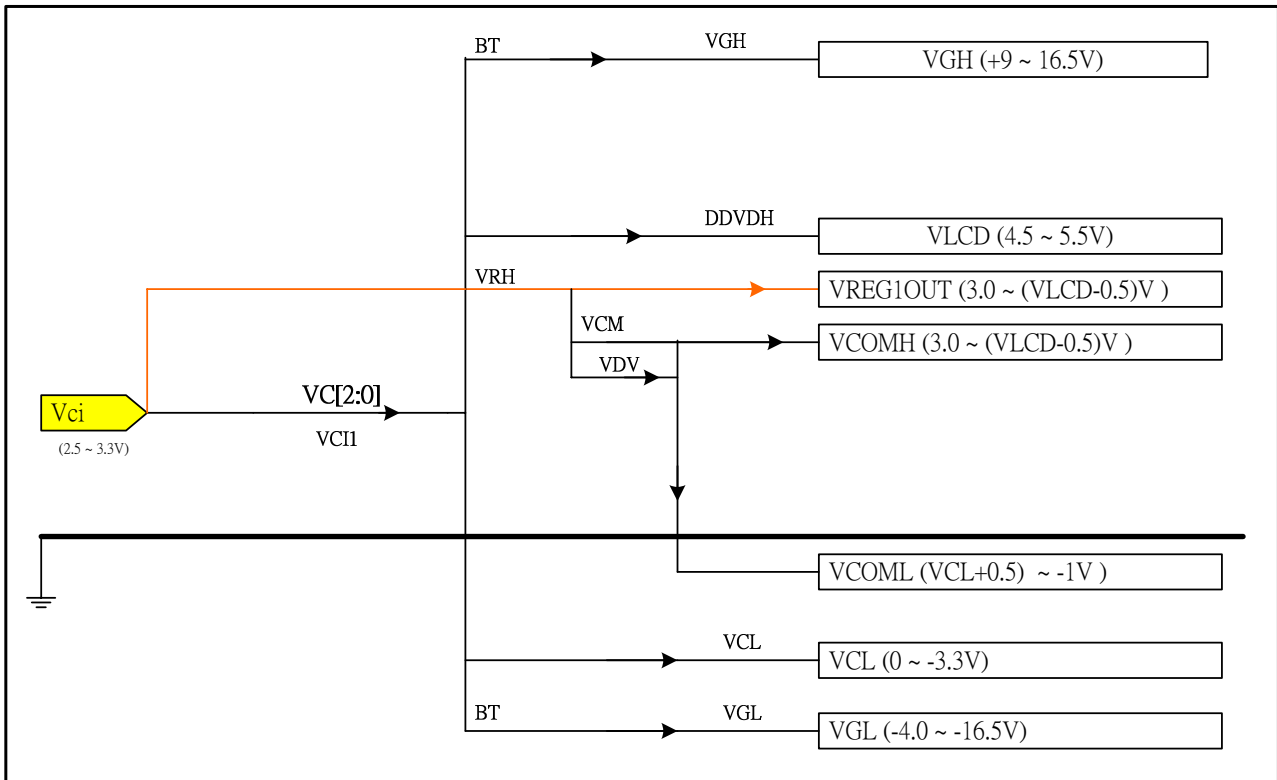
When supplying and cutting off power, follow the sequence below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.



**Figure 44 Power Supply ON/OFF Sequence**

### 13.5. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9335 are as follows.



**Figure 45 Voltage Configuration Diagram**

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships  $(DDVDH - VREG1OUT) > 0.2V$  and  $(VCOML - VCL) > 0.5V$  are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.



### 13.6. Applied Voltage to the TFT panel

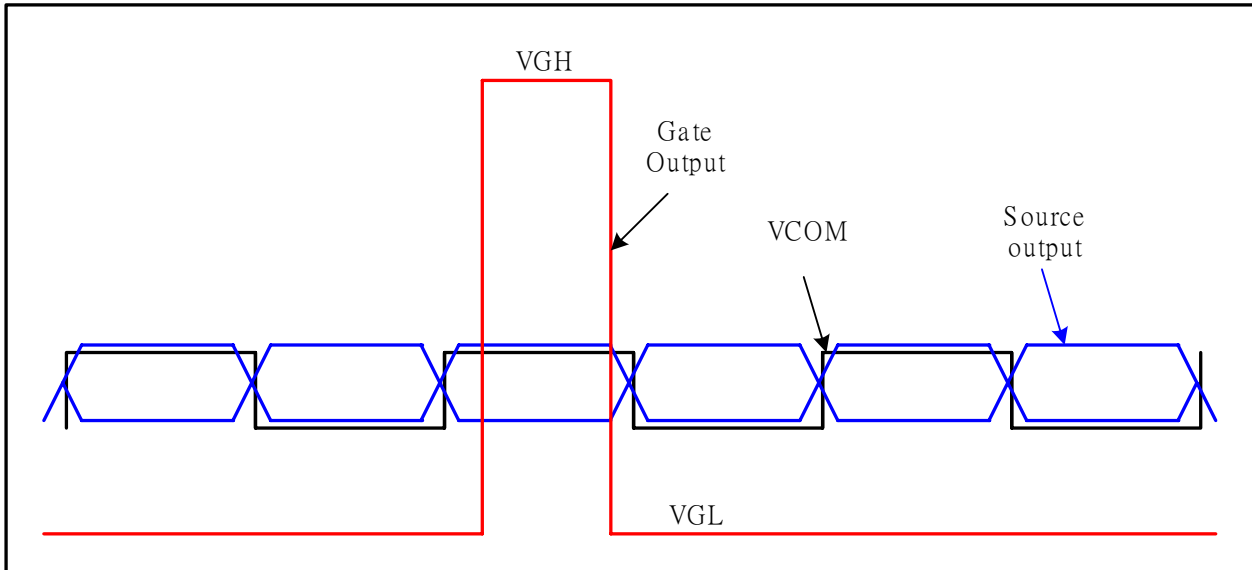


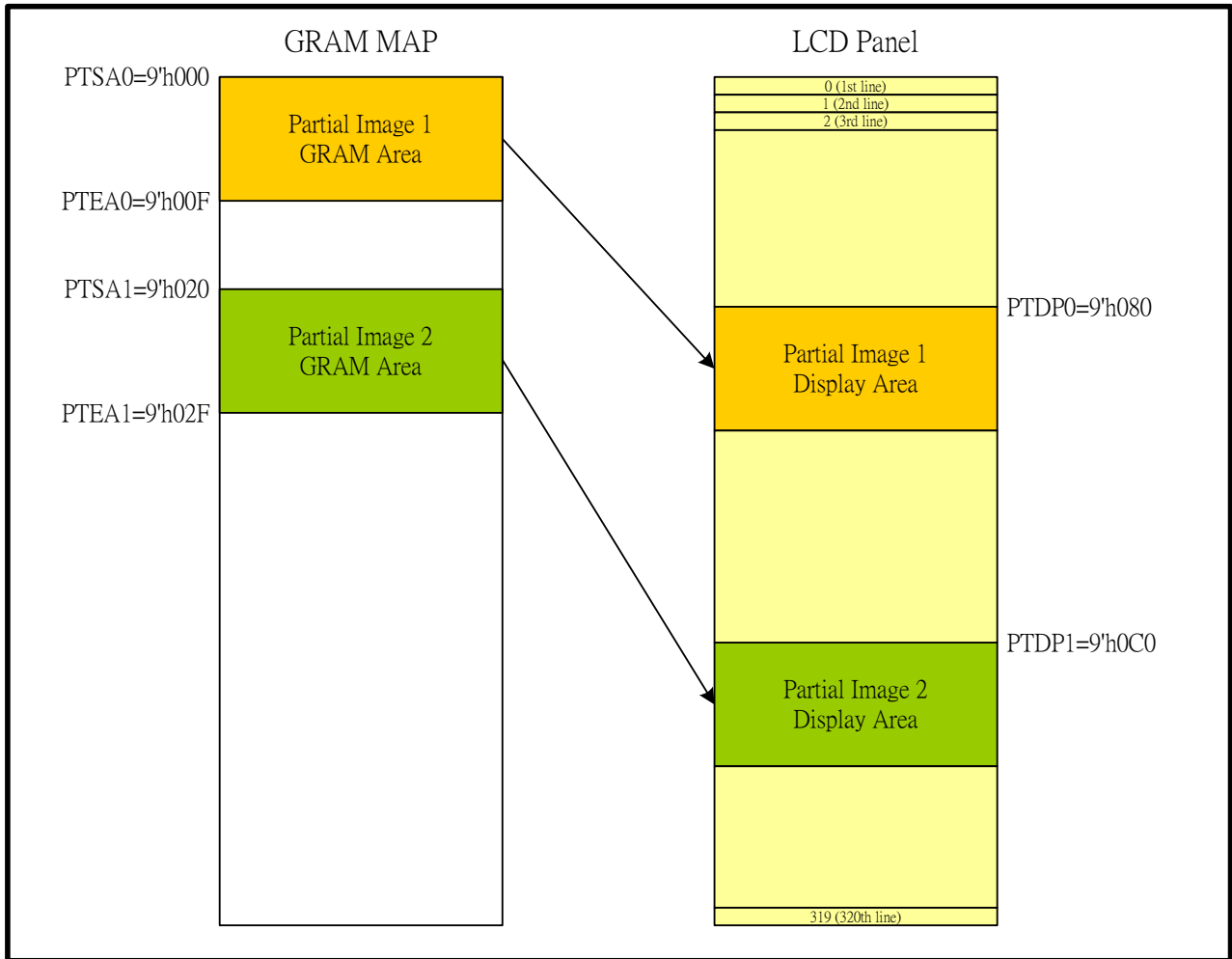
Figure 46 Voltage Output to TFT LCD Panel

### 13.7. Partial Display Function

The ILI9335 allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Base Image Display Setting	
BASEE	0
NL[5:0]	6'h27
Partial Image 1 Display Setting	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080
Partial Image 2 Display Setting	
PTDE1	1
PTSA1[8:0]	9'h020
PTEA1[8:0]	9'h02F
PTDP1[8:0]	9'h0C0



**Figure 47 Partial Display Example**

## 14. Electrical Characteristics

### 14.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9335 is used out of the absolute maximum ratings, the ILI9335 may be permanently damaged. To use the ILI9335 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9335 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	IOVCC	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI - GND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	DDVDH - GND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	GND -VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	DDVDH - VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH - VGL	V	0.3 ~ + 30	1, 5
Input voltage	Vt	V	-0.3 ~ VCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:

1. GND must be maintained
2. (High) (VCC = VCC) ≥ GND (Low), (High) IOVCC ≥ GND (Low).
3. Make sure (High) VCI ≥ GND (Low).
4. Make sure (High) DDVDH ≥ GND (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) VGH ≥ GND (Low).
7. Make sure (High) GND ≥ VGL (Low).
8. For die and wafer products, specified up to 85°C.
9. This temperature specifications apply to the TCP package

## 14.2. DC Characteristics

(VCC = VCI=2.50 ~ 3.6V, IOVCC = 1.65 ~ 3.60V, Ta= -40 ~ 85 °C)

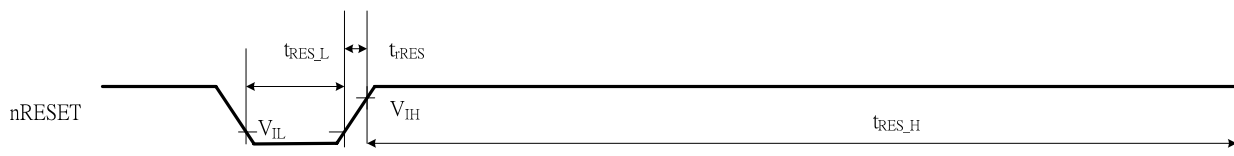
Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V <sub>IH</sub>	V	IOVCC= 1.65 ~ 3.6V	0.8*IOVCC	-	IOVCC	-
Input low voltage	V <sub>IL</sub>	V	IOVCC= 1.65 ~ 3.6V	-0.3	-	0.2*IOVCC	-
Output high voltage(1) (DB0-17 Pins)	V <sub>OH1</sub>	V	IOH = -0.1 mA	0.8*IOVCC	-	-	-
Output low voltage (DB0-17 Pins)	V <sub>OL1</sub>	V	IOVCC=1.65~3.6V	-	-	0.2*IOVCC	-
I/O leakage current	I <sub>LI</sub>	μA	Vin = 0 ~ VCC	-0.1	-	0.1	-
Current consumption during normal operation (VCC - GND)+ (IOVCC - GND)	I <sub>OP</sub>	μA	VCC=IOVCC=2.8V , Ta=25°C , fOSC = 512KHz ( Line) GRAM data = 0000h	-	TBD	-	-
Current consumption during standby mode (VCC - GND)+ (IOVCC - GND)	I <sub>ST</sub>	μA	VCC=IOVCC=2.8V , Ta=25°C	-	30	50	-
LCD Drive Power Supply Current (DDVDH-GND)	ILCD	mA	VCI=2.8V , VREG1OUT =4.8V DDVDH=5.2V , Frame Rate: 70Hz, line-inversion, Ta=25°C, GRAM data = 0000h,	-	5.5	-	-
LCD Driving Voltage (DDVDH-GND)	DDVDH	V	-	4.5	-	6	-
Output deviation voltage	V <sub>DEV</sub>	mV	-	-	-	20	-
Output offset voltage	V <sub>OFFSET</sub>	mV	Note1	-	-	35	-

Note1: The Max. value is between with measure point and Gamma setting value.

## 14.3. Reset Timing Characteristics

Reset Timing Characteristics (IOVCC = 1.65 ~ 3.6 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t <sub>RES L</sub>	ms	1	-	-
Reset rise time	t <sub>RES</sub>	μs	-	-	10
Reset high-level width	t <sub>RES H</sub>	ms	50	-	-



## 14.4. AC Characteristics

### 14.4.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.6V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	$t_{CYCW}$	ns	(75)	-	-
	Read	$t_{CYCR}$	ns	300	-	-
Write low-level pulse width	$PW_{LW}$	ns	(40)	-	500	-
Write high-level pulse width	$PW_{HW}$	ns	(30)	-	-	-
Read low-level pulse width	$PW_{LR}$	ns	150	-	-	-
Read high-level pulse width	$PW_{HR}$	ns	150	-	-	-
Write / Read rise / fall time	$t_{WRr}/t_{WRf}$	ns	-	-	25	-
Setup time	Write ( RS to nCS, E/nWR )	$t_{AS}$	ns	10	-	-
	Read ( RS to nCS, RW/nRD )			5	-	-
Address hold time	$t_{AH}$	ns	5	-	-	-
Write data set up time	$t_{DSW}$	ns	10	-	-	-
Write data hold time	$t_H$	ns	15	-	-	-
Read data delay time	$t_{DDR}$	ns	-	-	100	-
Read data hold time	$t_{DHR}$	ns	5	-	-	-

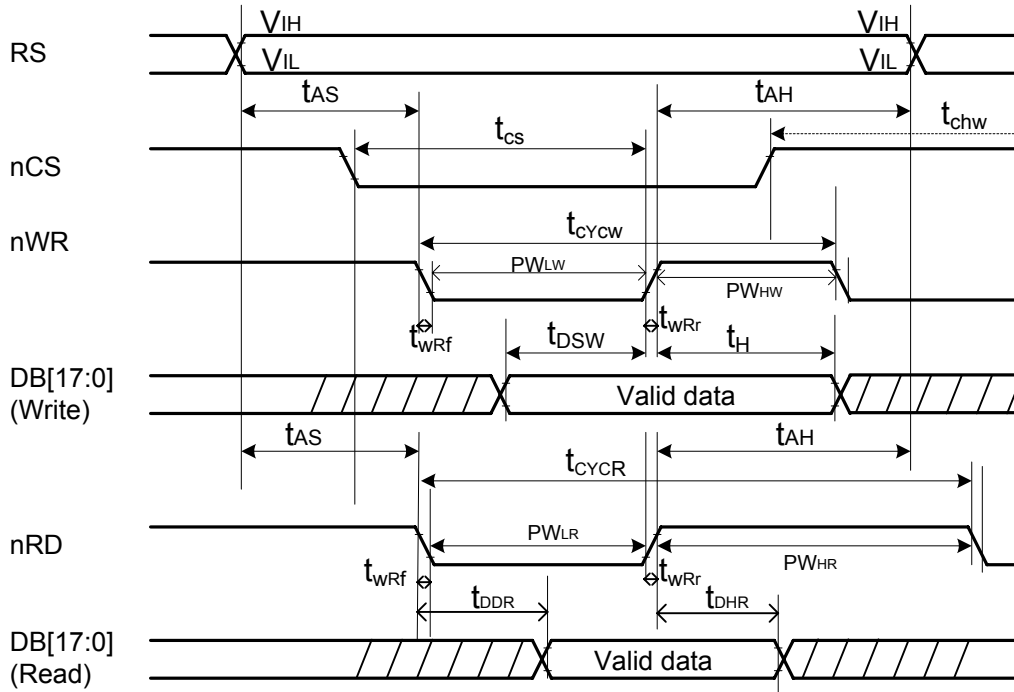
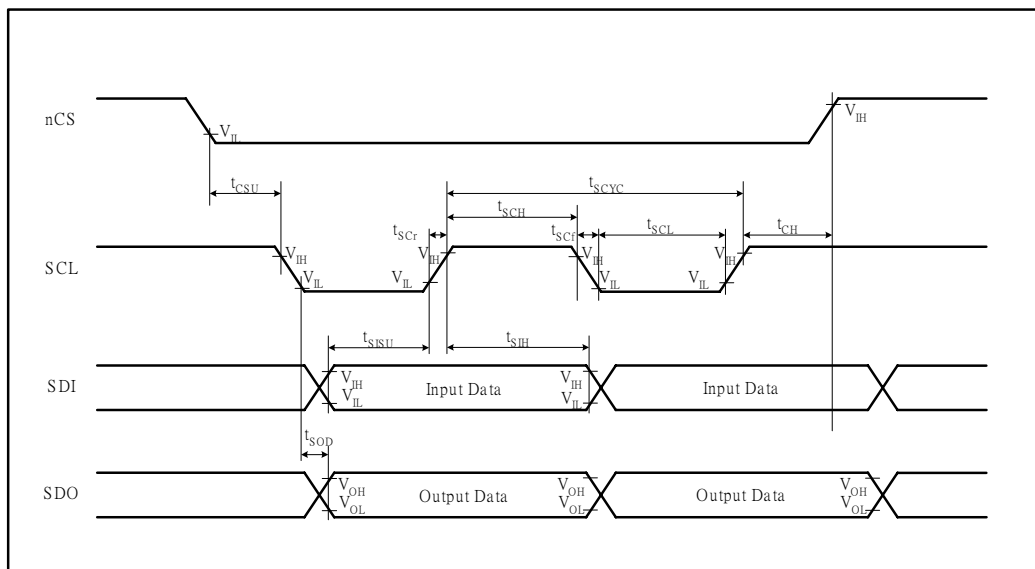


Figure 48 i80-System Bus Timing

**14.4.2. Serial Data Transfer Interface Timing Characteristics**  
(IOVCC= 1.65 ~ 3.6V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write ( received )	$t_{SCYC}$	$\mu s$	(100)	-	-
	Read ( transmitted )	$t_{SCYC}$	$\mu s$	200	-	-
Serial clock high – level pulse width	Write ( received )	$t_{SCH}$	ns	40	-	-
	Read ( transmitted )	$t_{SCH}$	ns	100	-	-
Serial clock low – level pulse width	Write ( received )	$t_{SCL}$	ns	40	-	-
	Read ( transmitted )	$t_{SCL}$	ns	100	-	-
Serial clock rise / fall time	$t_{SCr}, t_{SCf}$	ns	-	-	5	
Chip select set up time	$t_{CSU}$	ns	10	-	-	
Chip select hold time	$t_{CH}$	ns	50	-	-	
Serial input data set up time	$t_{SISU}$	ns	20	-	-	
Serial input data hold time	$t_{SIH}$	ns	20	-	-	
Serial output data set up time	$t_{SOD}$	ns	-	-	100	
Serial output data hold time	$t_{SOH}$	ns	5	-	-	



**Figure 49 SPI System Bus Timing**

**14.4.3. RGB Interface Timing Characteristics**

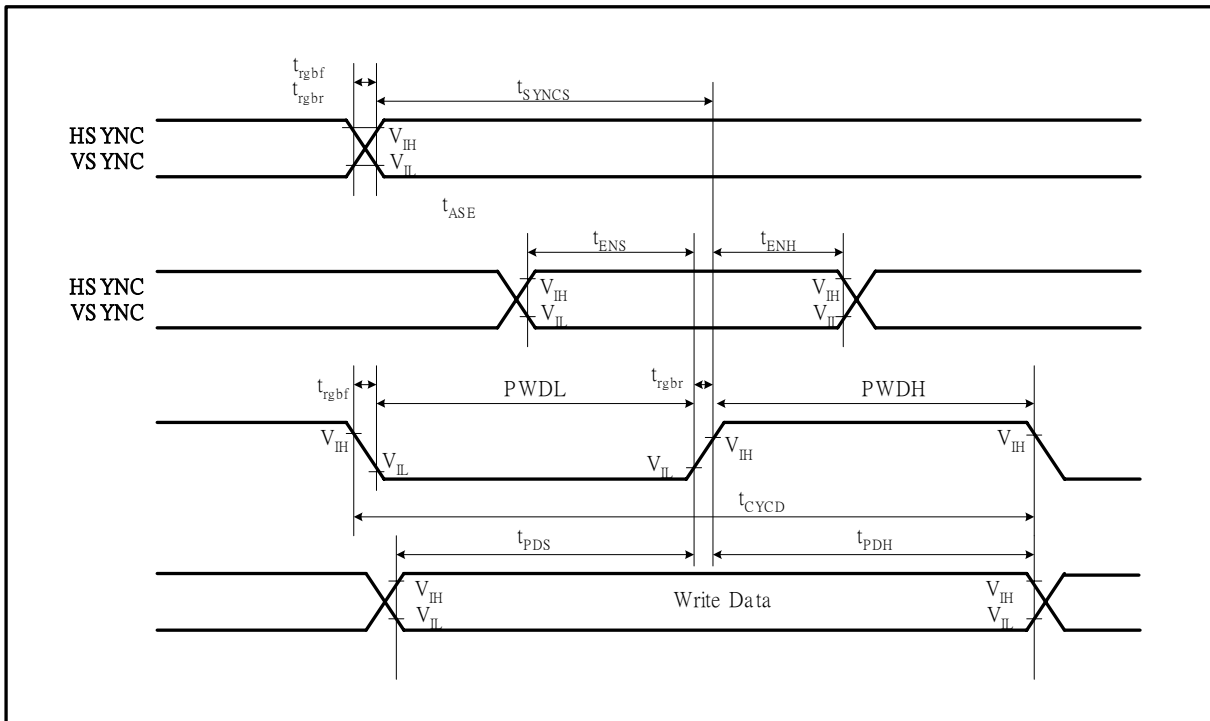
**18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.6V)**

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	$t_{SYNCS}$	ns	0	-	-	-
ENABLE setup time	$t_{ENS}$	ns	10	-	-	-
ENABLE hold time	$t_{ENH}$	ns	10	-	-	-
PD Data setup time	$t_{PDS}$	ns	10	-	-	-
PD Data hold time	$t_{PDH}$	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	$t_{CYCD}$	ns	(150)	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	$t_{rgr}, t_{rgh}$	ns	-	-	25	-

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**6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.6V)**

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	$t_{SYNCS}$	ns	0	-	-	-
ENABLE setup time	$t_{ENS}$	ns	10	-	-	-
ENABLE hold time	$t_{ENH}$	ns	10	-	-	-
PD Data setup time	$t_{PDS}$	ns	10	-	-	-
PD Data hold time	$t_{PDH}$	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	$t_{CYCD}$	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	$t_{rgr}$ , $t_{rgrf}$	ns	-	-	25	-



**Figure50 RGB Interface Timing**

## 15. Revision History

Version No.	Date	Page	Description
V0.00	2008/08/06	all	new built
V0,01	2008/08/14	104	Change condition of stand by and normal mode.
	2008/10/08	15~24	Modify IC height and relative pad and alignment mark coordinate!
		72	Frame rate modified
		96	Schottky diode VCL-VGL → GND-VGL
		73	"04"h ≤ HEA-HAS → "01"h ≤ HEA-HAS.
		100	Modify figure 45
	2008/11/3	19,20,21	Modify pad coordinate of number 674,722, 859, 907 and 931
V0,02	2008/11/03	82, 83	Add deep stand by mode
		61	Add 16 bit data format
		99	Add application circuit
		100	Modify Schottky diode number and capacitor number
V0,03	2008/11/14	84	Modify OTP flow
V0,04	2008/11/24	24	Modify alignment mark coordinate
V0,05	2008/12/22	99,100	Modify component number
V0,06	2008/12/30	8,12,13, 108~111	Modify IOVCC, VCI, VCC range to 3.6V
V0.07	2009/01/19	83	Add wake up timing
		110	Add timing value
		109	Add timing value
V0.08	2009/02/03	40, 48, 49	Delete HWM description
		13	Delete MDDI description in IOVCC