DATA SHEET

(DOC No. HX8367-A-DS)

HX8367-A

240RGB x 320 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Version 01 Januaryr, 2011

Himax Technologies, Inc.
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1. General Description

This document describes HX8367-A 240RGBx320 dots resolution driving controller. The HX8367-A is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx320 dots at maximum.

The HX8367-A can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8367-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8367-A is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

- Single chip solution to drive a TFT LCD panel
- Display Resolution: 240(H) x RGB(H) x 320(V)
- Display Color modes
  - Normal Display Mode On
    - System Interface Circuit
      1. 4096(R (4), G (4), B (4)) colors
      2. 65, 536(R (5), G (6), B (5)) colors
      3. 262, 144(R (6), G (6), B (6)) colors
    - RGB Interface Circuit
      1. 65,536(R(5),G(6),B(5)) colors
      2. 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    - 8 (R (1), G (1), B (1)) colors.

- Outputs
  - Source outputs: 720 source lines.
  - Selectable gate line control signal for glass 320 gate lines
  - Adjusted source voltages (V0p ~V63p, V0n ~V63n)

- Display interface:
  - System interface:
    - 8-/9-/16-/18-bit parallel bus system interface
    - 3-/4-wire serial bus system interface
  - RGB interface:
    - 6-/16-/18-bit RGB interface

- Internal graphics RAM capacity: 240 x18x320 bit = 1382400bits

- Display features
  - The vertical scroll display function in line units
  - Partial area display mode.
  - Software programmable color depth mode

- On chip
  - OTP memory to store initialization register settings
  - Automatic malfunction recovery for default values
  - Internal oscillator and hardware reset function
  - DC/DC converter and charge bump circuit for source, glass gate driving voltage
  - Adjust AC VCOM generation

- LCD Driving Inversion Algorithm

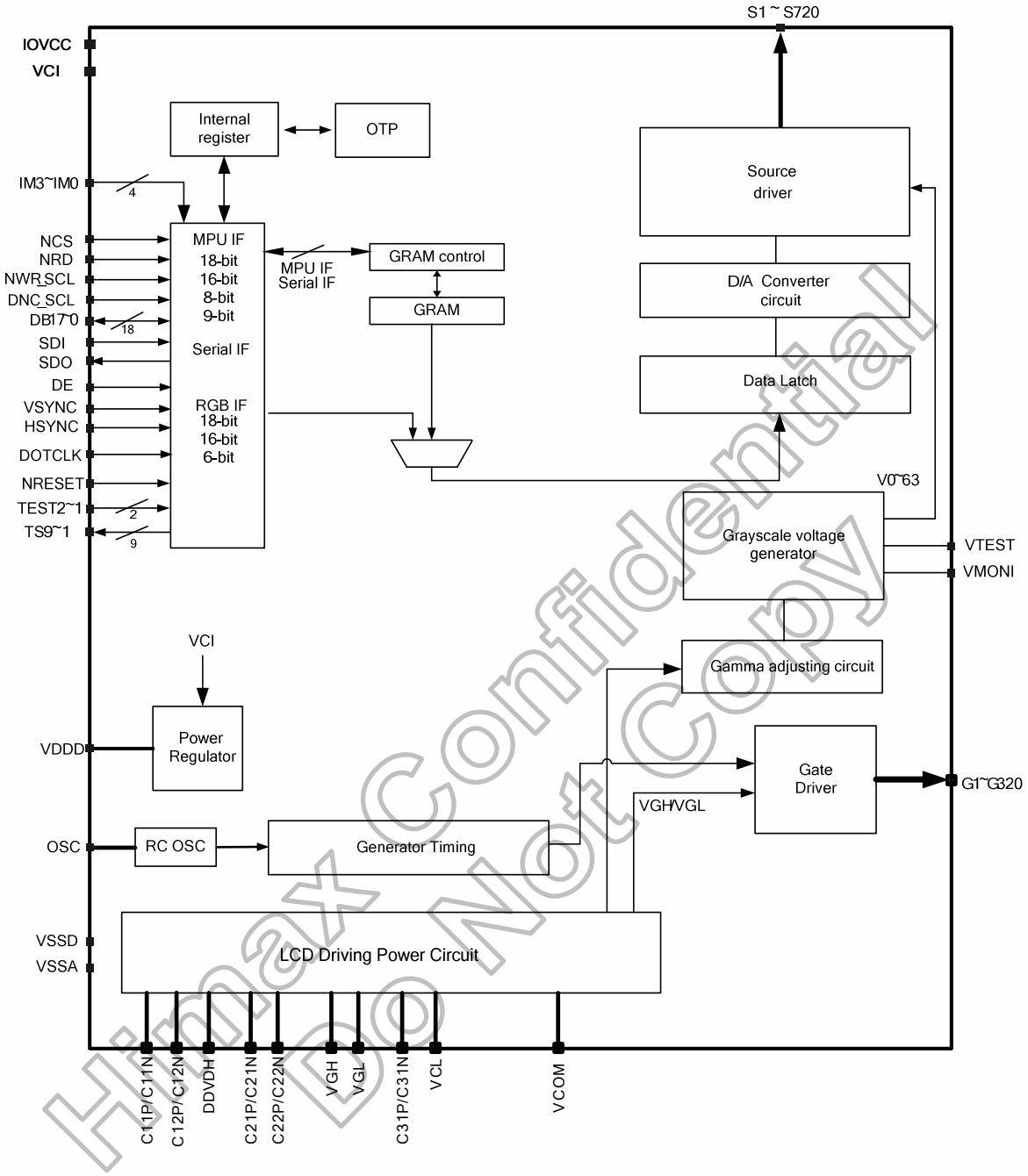
- Frame inversion AC liquid-crystal drive
- 1~7 line inversion AC liquid-crystal drive

- Input power supply
  - IOVCC = 1.65 to 3.3V (Logic IO power supply voltage range)
  - VCI = 2.5 to 3.3V (Driver power supply voltage range)

- Output voltage levels
  - DDVDH = 5.0 V for two time pump (Power supply for driver circuit range)
  - DDVDH = 6.1 V for three time pump (Power supply for driver circuit range)
  - VREG1 = 3.3V to 5.8V (Source output voltage range)
  - VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - VGL = -6.0 to -13.5V (Negative Gate output voltage range)
  - VCOMH = 2.5V to 5.8V, 15mV/step(Common electrode output high voltage)
  - VCOML = -2.5V to 0.0V, 15mV/step (Common electrode output low voltage)

- Digital 3-seperated RGB Gamma
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Chip on Glass
- Operating temperature range : -40℃~ 85℃

3. Block Diagram



4. Pin Description

4.1 Pin description

Interface Logic Pin				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IM3, IM2,IM1,IM0	I	4	VSSD/ IOVCC	System interface select. IM3 IM2 IM1 IM0 Interface 0 0 0 0 8080 MCU 16-bits Parallel type I 0 0 0 1 8080 MCU 8-bits Parallel type I 0 0 1 0 8080 MCU 16-bits Parallel type II 0 0 1 1 8080 MCU 8-bits Parallel type II 0 1 0 ID 3-wire Serial interface 0 1 1 - 4-wire Serial interface 1 0 0 0 8080 MCU 18-bits Parallel type I 1 0 0 1 8080 MCU 9-bits Parallel type I 1 0 1 0 8080 MCU 18-bits Parallel type II 1 0 1 1 8080 MCU 9-bits Parallel type II If not used, please fix this pin to IOVCC or VSSD level.
NCS	I	1	MPU	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.
NWR_SCL	I	1	MPU	(NWR) Write enable pin I80 parallel bus system interface. (SCL) server as serial data clock in serial bus system interface. If not used, connected to IOVCC.
NRD	I	1	MPU	(NRD) Read enable pin I80 parallel bus system interface. If not used, connected to IOVCC.
SDI	I	1	MPU	Serial data input pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. If not used, please connect to VSSD.
DNC_SCL	I	1	MPU	(DNC) Command / parameter or display data selection pin. If not used, please fix this pin at IOVCC or VSSD level.
VSYNC	I	1	MPU	Vertical synchronizing signal in RGB interface. Must be fixed to VSSD level if it is not used.
HSYNC	I	1	MPU	Horizontal synchronizing signal in RGB interface. Must be fixed to VSSD level if it is not used.
DE	I	1	MPU	A data ENABLE signal in RGB I/F mode. Must be fixed to VSSD level if it is not used.
DOTCLK	I	1	MPU	Data enable signal in RGB interface. Must be fixed to VSSD level if it is not used.
NRESET	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
DB17~0	I/O	18	MPU	18-bit bi-directional data bus. The unused pins let to open or connect to IOVCC or VSSD level.

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S720	O	720	LCD	Output voltages applied to the liquid crystal.
G1~G320	O	320	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	6	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
SDO	O	1	MPU	Serial data output pin in serial bus system interface. If not used, please let it open.
TE	O	1	MPU or open	Tearing effect output. If not used, please let it open.

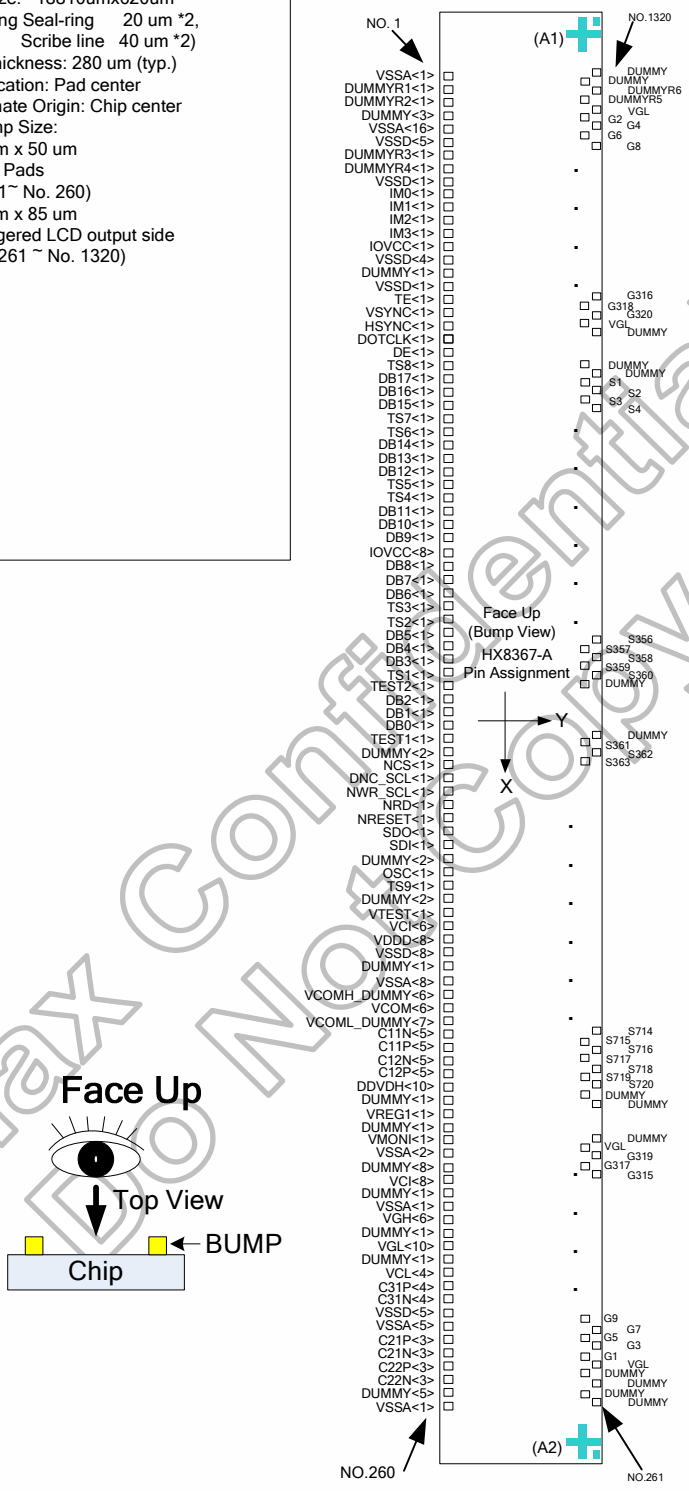
Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11P,C11N C12P, C12N	I/O	5,5 5,5	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C31P,C31N	I/O	4,4	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.
C21P,C21N C22P,C22N	I/O	3,3 3,3	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	9	Power Supply	Digital IO Pad power supply.
VCI	P	14	Power Supply	Analog power supply.
VSSD	P	24	Ground	Digital ground.
VSSA	P	34	Ground	Analog ground.
VDDD	O	8	Stabilizing capacitor	Output from internal logic voltage (1.4V). Connect to a stabilizing capacitor between VSSD and VDDD
VREG1	O	1	Open	Internal generated stable power for source driver unit. Leave it open.
VCL	O	4	Stabilizing capacitor	An output from the step-up circuit3. A negative voltage for VCOML circuit, VCL= -VCI. Connect to a stabilizing capacitor between VSSA and VCL.
DDVDH	O	10	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH.
VGH	O	6	Stabilizing capacitor	A positive power output from the step-up circuit 2 for the gate line drive circuit. The step-up rate is determined by BT[2:0] bits. Connect to a stabilizing capacitor between GND and VGH.
VGL	O	14	Stabilizing capacitor	A negative power output from the step-up circuit 2 for the gate line drive circuit. The step-up rate is determined by BT[2:0] bits. Connect to a stabilizing capacitor between GND and VGL.

Test pin and others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST2-1	I	2	GND	Test pin input (Internal pull low). Disconnect it.
TS9-1	O	9	Open	A test pin. Disconnect it.
VMONI	O	1	Open	A test pin. Disconnect it.
OSC	I	1	Open or Connect to VSSD	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.
VTEST	O	1	Open	Gamma voltage of Panel test pin output. Must left it open.
VCOMH_DUMMY	-	6	Open	Dummy pads. Leave it open.
VCOML_DUMMY	-	7	Open	Dummy pads. Leave it open.
DUMMYR6-1	-	6	Open	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR6 short within the chip. DUMMYR2 and DUMMYR5 short within the chip. DUMMYR3 and DUMMYR4 short within the chip.
DUMMY	-	43	Open	Dummy pads. Leave it open.

4.2 Pin assignment

Chip Size: 18810umx620um
(Including Seal-ring 20 um *2,
Scribe line 40 um *2)
Chip Thickness: 280 um (typ.)
Pad Location: Pad center
Coordinate Origin: Chip center
Au Bump Size:
1. 50 um x 50 um
   Input Pads
   (No. 1~ No. 260)
2. 16 um x 85 um
   Staggered LCD output side
   (No. 261 ~ No. 1320)



4.3 PAD coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	VSSA	-9065	-226.2	61	IOVCC	-4865	-226.2	121	DUMMY	-665	-226.2	181	DUMMY	3535	-226.2
2	DUMMYR1	-8995	-226.2	62	IOVCC	-4795	-226.2	122	VSSA	-595	-226.2	182	VMONI	3605	-226.2
3	DUMMYR2	-8925	-226.2	63	IOVCC	-4725	-226.2	123	VSSA	-525	-226.2	183	VSSA	3675	-226.2
4	DUMMY	-8855	-226.2	64	IOVCC	-4655	-226.2	124	VSSA	-455	-226.2	184	VSSA	3745	-226.2
5	DUMMY	-8785	-226.2	65	IOVCC	-4585	-226.2	125	VSSA	-385	-226.2	185	DUMMY	3815	-226.2
6	DUMMY	-8715	-226.2	66	IOVCC	-4515	-226.2	126	VSSA	-315	-226.2	186	DUMMY	3885	-226.2
7	VSSA	-8645	-226.2	67	IOVCC	-4445	-226.2	127	VSSA	-245	-226.2	187	DUMMY	3955	-226.2
8	VSSA	-8575	-226.2	68	IOVCC	-4375	-226.2	128	VSSA	-175	-226.2	188	DUMMY	4025	-226.2
9	VSSA	-8505	-226.2	69	DB8	-4305	-226.2	129	VSSA	-105	-226.2	189	DUMMY	4095	-226.2
10	VSSA	-8435	-226.2	70	DB7	-4235	-226.2	130	VCOMH_DUMMY	-35	-226.2	190	DUMMY	4165	-226.2
11	VSSA	-8365	-226.2	71	DB6	-4165	-226.2	131	VCOMH_DUMMY	35	-226.2	191	DUMMY	4235	-226.2
12	VSSA	-8295	-226.2	72	TS3	-4095	-226.2	132	VCOMH_DUMMY	105	-226.2	192	DUMMY	4305	-226.2
13	VSSA	-8225	-226.2	73	TS2	-4025	-226.2	133	VCOMH_DUMMY	175	-226.2	193	VCI	4375	-226.2
14	VSSA	-8155	-226.2	74	DB5	-3955	-226.2	134	VCOMH_DUMMY	245	-226.2	194	VCI	4445	-226.2
15	VSSA	-8085	-226.2	75	DB4	-3885	-226.2	135	VCOMH_DUMMY	315	-226.2	195	VCI	4515	-226.2
16	VSSA	-8015	-226.2	76	DB3	-3815	-226.2	136	VCOM	385	-226.2	196	VCI	4585	-226.2
17	VSSA	-7945	-226.2	77	TS1	-3745	-226.2	137	VCOM	455	-226.2	197	VCI	4655	-226.2
18	VSSA	-7875	-226.2	78	TEST2	-3675	-226.2	138	VCOM	525	-226.2	198	VCI	4725	-226.2
19	VSSA	-7805	-226.2	79	DB2	-3605	-226.2	139	VCOM	595	-226.2	199	VCI	4795	-226.2
20	VSSA	-7735	-226.2	80	DB1	-3535	-226.2	140	VCOM	665	-226.2	200	VCI	4865	-226.2
21	VSSA	-7665	-226.2	81	DB0	-3465	-226.2	141	VCOM	735	-226.2	201	DUMMY	4935	-226.2
22	VSSA	-7595	-226.2	82	TEST1	-3395	-226.2	142	VCOML_DUMMY	805	-226.2	202	VSSA	5005	-226.2
23	VSSD	-7525	-226.2	83	DUMMY	-3325	-226.2	143	VCOML_DUMMY	875	-226.2	203	VGH	5075	-226.2
24	VSSD	-7455	-226.2	84	DUMMY	-3255	-226.2	144	VCOML_DUMMY	945	-226.2	204	VGH	5145	-226.2
25	VSSD	-7385	-226.2	85	NCS	-3185	-226.2	145	VCOML_DUMMY	1015	-226.2	205	VGH	5215	-226.2
26	VSSD	-7315	-226.2	86	DNC_SCL	-3115	-226.2	146	VCOML_DUMMY	1085	-226.2	206	VGH	5285	-226.2
27	VSSD	-7245	-226.2	87	NWR_SCL	-3045	-226.2	147	VCOML_DUMMY	1155	-226.2	207	VGH	5355	-226.2
28	DUMMYR3	-7175	-226.2	88	NRD	-2975	-226.2	148	VCOML_DUMMY	1225	-226.2	208	VGH	5425	-226.2
29	DUMMYR4	-7105	-226.2	89	NRESET	-2905	-226.2	149	C11N	1295	-226.2	209	DUMMY	5495	-226.2
30	VSSD	-7035	-226.2	90	SDO	-2835	-226.2	150	C11N	1365	-226.2	210	VGL	5565	-226.2
31	IM0	-6965	-226.2	91	SDI	-2765	-226.2	151	C11N	1435	-226.2	211	VGL	5635	-226.2
32	IM1	-6895	-226.2	92	DUMMY	-2695	-226.2	152	C11N	1505	-226.2	212	VGL	5705	-226.2
33	IM2	-6825	-226.2	93	DUMMY	-2625	-226.2	153	C11N	1575	-226.2	213	VGL	5775	-226.2
34	IM3	-6755	-226.2	94	OSC	-2555	-226.2	154	C11P	1645	-226.2	214	VGL	5845	-226.2
35	IOVCC	-6685	-226.2	95	TS9	-2485	-226.2	155	C11P	1715	-226.2	215	VGL	5915	-226.2
36	VSSD	-6615	-226.2	96	DUMMY	-2415	-226.2	156	C11P	1785	-226.2	216	VGL	5985	-226.2
37	VSSD	-6545	-226.2	97	DUMMY	-2345	-226.2	157	C11P	1855	-226.2	217	VGL	6055	-226.2
38	VSSD	-6475	-226.2	98	VTEST	-2275	-226.2	158	C11P	1925	-226.2	218	VGL	6125	-226.2
39	VSSD	-6405	-226.2	99	VCI	-2205	-226.2	159	C12N	1995	-226.2	219	VGL	6195	-226.2
40	DUMMY	-6335	-226.2	100	VCI	-2135	-226.2	160	C12N	2065	-226.2	220	DUMMY	6265	-226.2
41	VSSD	-6265	-226.2	101	VCI	-2065	-226.2	161	C12N	2135	-226.2	221	VCL	6335	-226.2
42	TE	-6195	-226.2	102	VCI	-1995	-226.2	162	C12N	2205	-226.2	222	VCL	6405	-226.2
43	VSYNC	-6125	-226.2	103	VCI	-1925	-226.2	163	C12N	2275	-226.2	223	VCL	6475	-226.2
44	HSYNC	-6055	-226.2	104	VCI	-1855	-226.2	164	C12P	2345	-226.2	224	VCL	6545	-226.2
45	DOTCLK	-5985	-226.2	105	VDDD	-1785	-226.2	165	C12P	2415	-226.2	225	C31P	6615	-226.2
46	DE	-5915	-226.2	106	VDDD	-1715	-226.2	166	C12P	2485	-226.2	226	C31P	6685	-226.2
47	TS8	-5845	-226.2	107	VDDD	-1645	-226.2	167	C12P	2555	-226.2	227	C31P	6755	-226.2
48	DB17	-5775	-226.2	108	VDDD	-1575	-226.2	168	C12P	2625	-226.2	228	C31P	6825	-226.2
49	DB16	-5705	-226.2	109	VDDD	-1505	-226.2	169	DDVDH	2695	-226.2	229	C31N	6895	-226.2
50	DB15	-5635	-226.2	110	VDDD	-1435	-226.2	170	DDVDH	2765	-226.2	230	C31N	6965	-226.2
51	TS7	-5565	-226.2	111	VDDD	-1365	-226.2	171	DDVDH	2835	-226.2	231	C31N	7035	-226.2
52	TS6	-5495	-226.2	112	VDDD	-1295	-226.2	172	DDVDH	2905	-226.2	232	C31N	7105	-226.2
53	DB14	-5425	-226.2	113	VSSD	-1225	-226.2	173	DDVDH	2975	-226.2	233	VSSD	7175	-226.2
54	DB13	-5355	-226.2	114	VSSD	-1155	-226.2	174	DDVDH	3045	-226.2	234	VSSD	7245	-226.2
55	DB12	-5285	-226.2	115	VSSD	-1085	-226.2	175	DDVDH	3115	-226.2	235	VSSD	7315	-226.2
56	TS5	-5215	-226.2	116	VSSD	-1015	-226.2	176	DDVDH	3185	-226.2	236	VSSD	7385	-226.2
57	TS4	-5145	-226.2	117	VSSD	-945	-226.2	177	DDVDH	3255	-226.2	237	VSSD	7455	-226.2
58	DB11	-5075	-226.2	118	VSSD	-875	-226.2	178	DDVDH	3325	-226.2	238	VSSA	7525	-226.2
59	DB10	-5005	-226.2	119	VSSD	-805	-226.2	179	DUMMY	3395	-226.2	239	VSSA	7595	-226.2
60	DB9	-4935	-226.2	120	VSSD	-735	-226.2	180	VREG1	3465	-226.2	240	VSSA	7665	-226.2

No.	Name	X	Y
241	VSSA	7735	-226.2
242	VSSA	7805	-226.2
243	C21P	7875	-226.2
244	C21P	7945	-226.2
245	C21P	8015	-226.2
246	C21N	8085	-226.2
247	C21N	8155	-226.2
248	C21N	8225	-226.2
249	C22P	8295	-226.2
250	C22P	8365	-226.2
251	C22P	8435	-226.2
252	C22N	8505	-226.2
253	C22N	8575	-226.2
254	C22N	8645	-226.2
255	DUMMY	8715	-226.2
256	DUMMY	8785	-226.2
257	DUMMY	8855	-226.2
258	DUMMY	8925	-226.2
259	DUMMY	8995	-226.2
260	VSSA	9065	-226.2
261	DUMMY	9216	213.5
262	DUMMY	9200	109.5
263	DUMMY	9184	213.5
264	DUMMY	9168	109.5
265	VGL	9152	213.5
266	G1	9136	109.5
267	G3	9120	213.5
268	G5	9104	109.5
269	G7	9088	213.5
270	G9	9072	109.5
271	G11	9056	213.5
272	G13	9040	109.5
273	G15	9024	213.5
274	G17	9008	109.5
275	G19	8992	213.5
276	G21	8976	109.5
277	G23	8960	213.5
278	G25	8944	109.5
279	G27	8928	213.5
280	G29	8912	109.5
281	G31	8896	213.5
282	G33	8880	109.5
283	G35	8864	213.5
284	G37	8848	109.5
285	G39	8832	213.5
286	G41	8816	109.5
287	G43	8800	213.5
288	G45	8784	109.5
289	G47	8768	213.5
290	G49	8752	109.5
291	G51	8736	213.5
292	G53	8720	109.5
293	G55	8704	213.5
294	G57	8688	109.5
295	G59	8672	213.5
296	G61	8656	109.5
297	G63	8640	213.5
298	G65	8624	109.5
299	G67	8608	213.5
300	G69	8592	109.5
301	G71	8576	213.5
302	G73	8560	109.5
303	G75	8544	213.5
304	G77	8528	109.5
305	G79	8512	213.5
306	G81	8496	109.5
307	G83	8480	213.5
308	G85	8464	109.5
309	G87	8448	213.5
310	G89	8432	109.5
311	G91	8416	213.5
312	G93	8400	109.5
313	G95	8384	213.5
314	G97	8368	109.5
315	G99	8352	213.5
316	G101	8336	109.5
317	G103	8320	213.5
318	G105	8304	109.5
319	G107	8288	213.5
320	G109	8272	109.5
321	G111	8256	213.5
322	G113	8240	109.5
323	G115	8224	213.5
324	G117	8208	109.5
325	G119	8192	213.5
326	G121	8176	109.5
327	G123	8160	213.5
328	G125	8144	109.5
329	G127	8128	213.5
330	G129	8112	109.5
331	G131	8096	213.5
332	G133	8080	109.5
333	G135	8064	213.5
334	G137	8048	109.5
335	G139	8032	213.5
336	G141	8016	109.5
337	G143	8000	213.5
338	G145	7984	109.5
339	G147	7968	213.5
340	G149	7952	109.5
341	G151	7936	213.5
342	G153	7920	109.5
343	G155	7904	213.5
344	G157	7888	109.5
345	G159	7872	213.5
346	G161	7856	109.5
347	G163	7840	213.5
348	G165	7824	109.5
349	G167	7808	213.5
350	G169	7792	109.5
351	G171	7776	213.5
352	G173	7760	109.5
353	G175	7744	213.5
354	G177	7728	109.5
355	G179	7712	213.5
356	G181	7696	109.5
357	G183	7680	213.5
358	G185	7664	109.5
359	G187	7648	213.5
360	G189	7632	109.5
361	G191	7616	213.5
362	G193	7600	109.5
363	G195	7584	213.5
364	G197	7568	109.5
365	G199	7552	213.5
366	G201	7536	109.5
367	G203	7520	213.5
368	G205	7504	109.5
369	G207	7488	213.5
370	G209	7472	109.5
371	G211	7456	213.5
372	G213	7440	109.5
373	G215	7424	213.5
374	G217	7408	109.5
375	G219	7392	213.5
376	G221	7376	109.5
377	G223	7360	213.5
378	G225	7344	109.5
379	G227	7328	213.5
380	G229	7312	109.5
381	G231	7296	213.5
382	G233	7280	109.5
383	G235	7264	213.5
384	G237	7248	109.5
385	G239	7232	213.5
386	G241	7216	109.5
387	G243	7200	213.5
388	G245	7184	109.5
389	G247	7168	213.5
390	G249	7152	109.5
391	G251	7136	213.5
392	G253	7120	109.5
393	G255	7104	213.5
394	G257	7088	109.5
395	G259	7072	213.5
396	G261	7056	109.5
397	G263	7040	213.5
398	G265	7024	109.5
399	G267	7008	213.5
400	G269	6992	109.5
401	G271	6976	213.5
402	G273	6960	109.5
403	G275	6944	213.5
404	G277	6928	109.5
405	G279	6912	213.5
406	G281	6896	109.5
407	G283	6880	213.5
408	G285	6864	109.5
409	G287	6848	213.5
410	G289	6832	109.5
411	G291	6816	213.5
412	G293	6800	109.5
413	G295	6784	213.5
414	G297	6768	109.5
415	G299	6752	213.5
416	G301	6736	109.5
417	G303	6720	213.5
418	G305	6704	109.5
419	G307	6688	213.5
420	G309	6672	109.5
421	G311	6656	213.5
422	G313	6640	109.5
423	G315	6624	213.5
424	G317	6608	109.5
425	G319	6592	213.5
426	VGL	6576	109.5
427	DUMMY	6560	213.5
428	DUMMY	6368	213.5
429	DUMMY	6352	109.5
430	S720	6336	213.5
431	S719	6320	109.5
432	S718	6304	213.5
433	S717	6288	109.5
434	S716	6272	213.5
435	S715	6256	109.5
436	S714	6240	213.5
437	S713	6224	109.5
438	S712	6208	213.5
439	S711	6192	109.5
440	S710	6176	213.5
441	S709	6160	109.5
442	S708	6144	213.5
443	S707	6128	109.5
444	S706	6112	213.5
445	S705	6096	109.5
446	S704	6080	213.5
447	S703	6064	109.5
448	S702	6048	213.5
449	S701	6032	109.5
450	S700	6016	213.5
451	S699	6000	109.5
452	S698	5984	213.5
453	S697	5968	109.5
454	S696	5952	213.5
455	S695	5936	109.5
456	S694	5920	213.5
457	S693	5904	109.5
458	S692	5888	213.5
459	S691	5872	109.5
460	S690	5856	213.5
461	S689	5840	109.5
462	S688	5824	213.5
463	S687	5808	109.5
464	S686	5792	213.5
465	S685	5776	109.5
466	S684	5760	213.5
467	S683	5744	109.5
468	S682	5728	213.5
469	S681	5712	109.5
470	S680	5696	213.5
471	S679	5680	109.5
472	S678	5664	213.5
473	S677	5648	109.5
474	S676	5632	213.5
475	S675	5616	109.5
476	S674	5600	213.5
477	S673	5584	109.5
478	S672	5568	213.5
479	S671	5552	109.5
480	S670	5536	213.5

No.	Name	X	Y
481	S669	5520	109.5
482	S668	5504	213.5
483	S667	5488	109.5
484	S666	5472	213.5
485	S665	5456	109.5
486	S664	5440	213.5
487	S663	5424	109.5
488	S662	5408	213.5
489	S661	5392	109.5
490	S660	5376	213.5
491	S659	5360	109.5
492	S658	5344	213.5
493	S657	5328	109.5
494	S656	5312	213.5
495	S655	5296	109.5
496	S654	5280	213.5
497	S653	5264	109.5
498	S652	5248	213.5
499	S651	5232	109.5
500	S650	5216	213.5
501	S649	5200	109.5
502	S648	5184	213.5
503	S647	5168	109.5
504	S646	5152	213.5
505	S645	5136	109.5
506	S644	5120	213.5
507	S643	5104	109.5
508	S642	5088	213.5
509	S641	5072	109.5
510	S640	5056	213.5
511	S639	5040	109.5
512	S638	5024	213.5
513	S637	5008	109.5
514	S636	4992	213.5
515	S635	4976	109.5
516	S634	4960	213.5
517	S633	4944	109.5
518	S632	4928	213.5
519	S631	4912	109.5
520	S630	4896	213.5
521	S629	4880	109.5
522	S628	4864	213.5
523	S627	4848	109.5
524	S626	4832	213.5
525	S625	4816	109.5
526	S624	4800	213.5
527	S623	4784	109.5
528	S622	4768	213.5
529	S621	4752	109.5
530	S620	4736	213.5
531	S619	4720	109.5
532	S618	4704	213.5
533	S617	4688	109.5
534	S616	4672	213.5
535	S615	4656	109.5
536	S614	4640	213.5
537	S613	4624	109.5
538	S612	4608	213.5
539	S611	4592	109.5
540	S610	4576	213.5

No.	Name	X	Y
541	S609	4560	109.5
542	S608	4544	213.5
543	S607	4528	109.5
544	S606	4512	213.5
545	S605	4496	109.5
546	S604	4480	213.5
547	S603	4464	109.5
548	S602	4448	213.5
549	S601	4432	109.5
550	S600	4416	213.5
551	S599	4400	109.5
552	S598	4384	213.5
553	S597	4368	109.5
554	S596	4352	213.5
555	S595	4336	109.5
556	S594	4320	213.5
557	S593	4304	109.5
558	S592	4288	213.5
559	S591	4272	109.5
560	S590	4256	213.5
561	S589	4240	109.5
562	S588	4224	213.5
563	S587	4208	109.5
564	S586	4192	213.5
565	S585	4176	109.5
566	S584	4160	213.5
567	S583	4144	109.5
568	S582	4128	213.5
569	S581	4112	109.5
570	S580	4096	213.5
571	S579	4080	109.5
572	S578	4064	213.5
573	S577	4048	109.5
574	S576	4032	213.5
575	S575	4016	109.5
576	S574	4000	213.5
577	S573	3984	109.5
578	S572	3968	213.5
579	S571	3952	109.5
580	S570	3936	213.5
581	S569	3920	109.5
582	S568	3904	213.5
583	S567	3888	109.5
584	S566	3872	213.5
585	S565	3856	109.5
586	S564	3840	213.5
587	S563	3824	109.5
588	S562	3808	213.5
589	S561	3792	109.5
590	S560	3776	213.5
591	S559	3760	109.5
592	S558	3744	213.5
593	S557	3728	109.5
594	S556	3712	213.5
595	S555	3696	109.5
596	S554	3680	213.5
597	S553	3664	109.5
598	S552	3648	213.5
599	S551	3632	109.5
600	S550	3616	213.5

No.	Name	X	Y
601	S549	3600	109.5
602	S548	3584	213.5
603	S547	3568	109.5
604	S546	3552	213.5
605	S545	3536	109.5
606	S544	3520	213.5
607	S543	3504	109.5
608	S542	3488	213.5
609	S541	3472	109.5
610	S540	3456	213.5
611	S539	3440	109.5
612	S538	3424	213.5
613	S537	3408	109.5
614	S536	3392	213.5
615	S535	3376	109.5
616	S534	3360	213.5
617	S533	3344	109.5
618	S532	3328	213.5
619	S531	3312	109.5
620	S530	3296	213.5
621	S529	3280	109.5
622	S528	3264	213.5
623	S527	3248	109.5
624	S526	3232	213.5
625	S525	3216	109.5
626	S524	3200	213.5
627	S523	3184	109.5
628	S522	3168	213.5
629	S521	3152	109.5
630	S520	3136	213.5
631	S519	3120	109.5
632	S518	3104	213.5
633	S517	3088	109.5
634	S516	3072	213.5
635	S515	3056	109.5
636	S514	3040	213.5
637	S513	3024	109.5
638	S512	3008	213.5
639	S511	2992	109.5
640	S510	2976	213.5
641	S509	2960	109.5
642	S508	2944	213.5
643	S507	2928	109.5
644	S506	2912	213.5
645	S505	2896	109.5
646	S504	2880	213.5
647	S503	2864	109.5
648	S502	2848	213.5
649	S501	2832	109.5
650	S500	2816	213.5
651	S499	2800	109.5
652	S498	2784	213.5
653	S497	2768	109.5
654	S496	2752	213.5
655	S495	2736	109.5
656	S494	2720	213.5
657	S493	2704	109.5
658	S492	2688	213.5
659	S491	2672	109.5
660	S490	2656	213.5

No.	Name	X	Y
661	S489	2640	109.5
662	S488	2624	213.5
663	S487	2608	109.5
664	S486	2592	213.5
665	S485	2576	109.5
666	S484	2560	213.5
667	S483	2544	109.5
668	S482	2528	213.5
669	S481	2512	109.5
670	S480	2496	213.5
671	S479	2480	109.5
672	S478	2464	213.5
673	S477	2448	109.5
674	S476	2432	213.5
675	S475	2416	109.5
676	S474	2400	213.5
677	S473	2384	109.5
678	S472	2368	213.5
679	S471	2352	109.5
680	S470	2336	213.5
681	S469	2320	109.5
682	S468	2304	213.5
683	S467	2288	109.5
684	S466	2272	213.5
685	S465	2256	109.5
686	S464	2240	213.5
687	S463	2224	109.5
688	S462	2208	213.5
689	S461	2192	109.5
690	S460	2176	213.5
691	S459	2160	109.5
692	S458	2144	213.5
693	S457	2128	109.5
694	S456	2112	213.5
695	S455	2096	109.5
696	S454	2080	213.5
697	S453	2064	109.5
698	S452	2048	213.5
699	S451	2032	109.5
700	S450	2016	213.5
701	S449	2000	109.5
702	S448	1984	213.5
703	S447	1968	109.5
704	S446	1952	213.5
705	S445	1936	109.5
706	S444	1920	213.5
707	S443	1904	109.5
708	S442	1888	213.5
709	S441	1872	109.5
710	S440	1856	213.5
711	S439	1840	109.5
712	S438	1824	213.5
713	S437	1808	109.5
714	S436	1792	213.5
715	S435	1776	109.5
716	S434	1760	213.5
717	S433	1744	109.5
718	S432	1728	213.5
719	S431	1712	109.5
720	S430	1696	213.5

No.	Name	X	Y
721	S429	1680	109.5
722	S428	1664	213.5
723	S427	1648	109.5
724	S426	1632	213.5
725	S425	1616	109.5
726	S424	1600	213.5
727	S423	1584	109.5
728	S422	1568	213.5
729	S421	1552	109.5
730	S420	1536	213.5
731	S419	1520	109.5
732	S418	1504	213.5
733	S417	1488	109.5
734	S416	1472	213.5
735	S415	1456	109.5
736	S414	1440	213.5
737	S413	1424	109.5
738	S412	1408	213.5
739	S411	1392	109.5
740	S410	1376	213.5
741	S409	1360	109.5
742	S408	1344	213.5
743	S407	1328	109.5
744	S406	1312	213.5
745	S405	1296	109.5
746	S404	1280	213.5
747	S403	1264	109.5
748	S402	1248	213.5
749	S401	1232	109.5
750	S400	1216	213.5
751	S399	1200	109.5
752	S398	1184	213.5
753	S397	1168	109.5
754	S396	1152	213.5
755	S395	1136	109.5
756	S394	1120	213.5
757	S393	1104	109.5
758	S392	1088	213.5
759	S391	1072	109.5
760	S390	1056	213.5
761	S389	1040	109.5
762	S388	1024	213.5
763	S387	1008	109.5
764	S386	992	213.5
765	S385	976	109.5
766	S384	960	213.5
767	S383	944	109.5
768	S382	928	213.5
769	S381	912	109.5
770	S380	896	213.5
771	S379	880	109.5
772	S378	864	213.5
773	S377	848	109.5
774	S376	832	213.5
775	S375	816	109.5
776	S374	800	213.5
777	S373	784	109.5
778	S372	768	213.5
779	S371	752	109.5
780	S370	736	213.5

No.	Name	X	Y
781	S369	720	109.5
782	S368	704	213.5
783	S367	688	109.5
784	S366	672	213.5
785	S365	656	109.5
786	S364	640	213.5
787	S363	624	109.5
788	S362	608	213.5
789	S361	592	109.5
790	DUMMY	576	213.5
791	DUMMY	-576	109.5
792	S360	-592	213.5
793	S359	-608	109.5
794	S358	-624	213.5
795	S357	-640	109.5
796	S356	-656	213.5
797	S355	-672	109.5
798	S354	-688	213.5
799	S353	-704	109.5
800	S352	-720	213.5
801	S351	-736	109.5
802	S350	-752	213.5
803	S349	-768	109.5
804	S348	-784	213.5
805	S347	-800	109.5
806	S346	-816	213.5
807	S345	-832	109.5
808	S344	-848	213.5
809	S343	-864	109.5
810	S342	-880	213.5
811	S341	-896	109.5
812	S340	-912	213.5
813	S339	-928	109.5
814	S338	-944	213.5
815	S337	-960	109.5
816	S336	-976	213.5
817	S335	-992	109.5
818	S334	-1008	213.5
819	S333	-1024	109.5
820	S332	-1040	213.5
821	S331	-1056	109.5
822	S330	-1072	213.5
823	S329	-1088	109.5
824	S328	-1104	213.5
825	S327	-1120	109.5
826	S326	-1136	213.5
827	S325	-1152	109.5
828	S324	-1168	213.5
829	S323	-1184	109.5
830	S322	-1200	213.5
831	S321	-1216	109.5
832	S320	-1232	213.5
833	S319	-1248	109.5
834	S318	-1264	213.5
835	S317	-1280	109.5
836	S316	-1296	213.5
837	S315	-1312	109.5
838	S314	-1328	213.5
839	S313	-1344	109.5
840	S312	-1360	213.5

No.	Name	X	Y
841	S311	-1376	109.5
842	S310	-1392	213.5
843	S309	-1408	109.5
844	S308	-1424	213.5
845	S307	-1440	109.5
846	S306	-1456	213.5
847	S305	-1472	109.5
848	S304	-1488	213.5
849	S303	-1504	109.5
850	S302	-1520	213.5
851	S301	-1536	109.5
852	S300	-1552	213.5
853	S299	-1568	109.5
854	S298	-1584	213.5
855	S297	-1600	109.5
856	S296	-1616	213.5
857	S295	-1632	109.5
858	S294	-1648	213.5
859	S293	-1664	109.5
860	S292	-1680	213.5
861	S291	-1696	109.5
862	S290	-1712	213.5
863	S289	-1728	109.5
864	S288	-1744	213.5
865	S287	-1760	109.5
866	S286	-1776	213.5
867	S285	-1792	109.5
868	S284	-1808	213.5
869	S283	-1824	109.5
870	S282	-1840	213.5
871	S281	-1856	109.5
872	S280	-1872	213.5
873	S279	-1888	109.5
874	S278	-1904	213.5
875	S277	-1920	109.5
876	S276	-1936	213.5
877	S275	-1952	109.5
878	S274	-1968	213.5
879	S273	-1984	109.5
880	S272	-2000	213.5
881	S271	-2016	109.5
882	S270	-2032	213.5
883	S269	-2048	109.5
884	S268	-2064	213.5
885	S267	-2080	109.5
886	S266	-2096	213.5
887	S265	-2112	109.5
888	S264	-2128	213.5
889	S263	-2144	109.5
890	S262	-2160	213.5
891	S261	-2176	109.5
892	S260	-2192	213.5
893	S259	-2208	109.5
894	S258	-2224	213.5
895	S257	-2240	109.5
896	S256	-2256	213.5
897	S255	-2272	109.5
898	S254	-2288	213.5
899	S253	-2304	109.5
900	S252	-2320	213.5

No.	Name	X	Y
901	S251	-2336	109.5
902	S250	-2352	213.5
903	S249	-2368	109.5
904	S248	-2384	213.5
905	S247	-2400	109.5
906	S246	-2416	213.5
907	S245	-2432	109.5
908	S244	-2448	213.5
909	S243	-2464	109.5
910	S242	-2480	213.5
911	S241	-2496	109.5
912	S240	-2512	213.5
913	S239	-2528	109.5
914	S238	-2544	213.5
915	S237	-2560	109.5
916	S236	-2576	213.5
917	S235	-2592	109.5
918	S234	-2608	213.5
919	S233	-2624	109.5
920	S232	-2640	213.5
921	S231	-2656	109.5
922	S230	-2672	213.5
923	S229	-2688	109.5
924	S228	-2704	213.5
925	S227	-2720	109.5
926	S226	-2736	213.5
927	S225	-2752	109.5
928	S224	-2768	213.5
929	S223	-2784	109.5
930	S222	-2800	213.5
931	S221	-2816	109.5
932	S220	-2832	213.5
933	S219	-2848	109.5
934	S218	-2864	213.5
935	S217	-2880	109.5
936	S216	-2896	213.5
937	S215	-2912	109.5
938	S214	-2928	213.5
939	S213	-2944	109.5
940	S212	-2960	213.5
941	S211	-2976	109.5
942	S210	-2992	213.5
943	S209	-3008	109.5
944	S208	-3024	213.5
945	S207	-3040	109.5
946	S206	-3056	213.5
947	S205	-3072	109.5
948	S204	-3088	213.5
949	S203	-3104	109.5
950	S202	-3120	213.5
951	S201	-3136	109.5
952	S200	-3152	213.5
953	S199	-3168	109.5
954	S198	-3184	213.5
955	S197	-3200	109.5
956	S196	-3216	213.5
957	S195	-3232	109.5
958	S194	-3248	213.5
959	S193	-3264	109.5
960	S192	-3280	213.5

No.	Name	X	Y
961	S191	-3296	109.5
962	S190	-3312	213.5
963	S189	-3328	109.5
964	S188	-3344	213.5
965	S187	-3360	109.5
966	S186	-3376	213.5
967	S185	-3392	109.5
968	S184	-3408	213.5
969	S183	-3424	109.5
970	S182	-3440	213.5
971	S181	-3456	109.5
972	S180	-3472	213.5
973	S179	-3488	109.5
974	S178	-3504	213.5
975	S177	-3520	109.5
976	S176	-3536	213.5
977	S175	-3552	109.5
978	S174	-3568	213.5
979	S173	-3584	109.5
980	S172	-3600	213.5
981	S171	-3616	109.5
982	S170	-3632	213.5
983	S169	-3648	109.5
984	S168	-3664	213.5
985	S167	-3680	109.5
986	S166	-3696	213.5
987	S165	-3712	109.5
988	S164	-3728	213.5
989	S163	-3744	109.5
990	S162	-3760	213.5
991	S161	-3776	109.5
992	S160	-3792	213.5
993	S159	-3808	109.5
994	S158	-3824	213.5
995	S157	-3840	109.5
996	S156	-3856	213.5
997	S155	-3872	109.5
998	S154	-3888	213.5
999	S153	-3904	109.5
1000	S152	-3920	213.5
1001	S151	-3936	109.5
1002	S150	-3952	213.5
1003	S149	-3968	109.5
1004	S148	-3984	213.5
1005	S147	-4000	109.5
1006	S146	-4016	213.5
1007	S145	-4032	109.5
1008	S144	-4048	213.5
1009	S143	-4064	109.5
1010	S142	-4080	213.5
1011	S141	-4096	109.5
1012	S140	-4112	213.5
1013	S139	-4128	109.5
1014	S138	-4144	213.5
1015	S137	-4160	109.5
1016	S136	-4176	213.5
1017	S135	-4192	109.5
1018	S134	-4208	213.5
1019	S133	-4224	109.5
1020	S132	-4240	213.5

No.	Name	X	Y
1021	S131	-4256	109.5
1022	S130	-4272	213.5
1023	S129	-4288	109.5
1024	S128	-4304	213.5
1025	S127	-4320	109.5
1026	S126	-4336	213.5
1027	S125	-4352	109.5
1028	S124	-4368	213.5
1029	S123	-4384	109.5
1030	S122	-4400	213.5
1031	S121	-4416	109.5
1032	S120	-4432	213.5
1033	S119	-4448	109.5
1034	S118	-4464	213.5
1035	S117	-4480	109.5
1036	S116	-4496	213.5
1037	S115	-4512	109.5
1038	S114	-4528	213.5
1039	S113	-4544	109.5
1040	S112	-4560	213.5
1041	S111	-4576	109.5
1042	S110	-4592	213.5
1043	S109	-4608	109.5
1044	S108	-4624	213.5
1045	S107	-4640	109.5
1046	S106	-4656	213.5
1047	S105	-4672	109.5
1048	S104	-4688	213.5
1049	S103	-4704	109.5
1050	S102	-4720	213.5
1051	S101	-4736	109.5
1052	S100	-4752	213.5
1053	S99	-4768	109.5
1054	S98	-4784	213.5
1055	S97	-4800	109.5
1056	S96	-4816	213.5
1057	S95	-4832	109.5
1058	S94	-4848	213.5
1059	S93	-4864	109.5
1060	S92	-4880	213.5
1061	S91	-4896	109.5
1062	S90	-4912	213.5
1063	S89	-4928	109.5
1064	S88	-4944	213.5
1065	S87	-4960	109.5
1066	S86	-4976	213.5
1067	S85	-4992	109.5
1068	S84	-5008	213.5
1069	S83	-5024	109.5
1070	S82	-5040	213.5
1071	S81	-5056	109.5
1072	S80	-5072	213.5
1073	S79	-5088	109.5
1074	S78	-5104	213.5
1075	S77	-5120	109.5
1076	S76	-5136	213.5
1077	S75	-5152	109.5
1078	S74	-5168	213.5
1079	S73	-5184	109.5
1080	S72	-5200	213.5

No.	Name	X	Y
1081	S71	-5216	109.5
1082	S70	-5232	213.5
1083	S69	-5248	109.5
1084	S68	-5264	213.5
1085	S67	-5280	109.5
1086	S66	-5296	213.5
1087	S65	-5312	109.5
1088	S64	-5328	213.5
1089	S63	-5344	109.5
1090	S62	-5360	213.5
1091	S61	-5376	109.5
1092	S60	-5392	213.5
1093	S59	-5408	109.5
1094	S58	-5424	213.5
1095	S57	-5440	109.5
1096	S56	-5456	213.5
1097	S55	-5472	109.5
1098	S54	-5488	213.5
1099	S53	-5504	109.5
1100	S52	-5520	213.5
1101	S51	-5536	109.5
1102	S50	-5552	213.5
1103	S49	-5568	109.5
1104	S48	-5584	213.5
1105	S47	-5600	109.5
1106	S46	-5616	213.5
1107	S45	-5632	109.5
1108	S44	-5648	213.5
1109	S43	-5664	109.5
1110	S42	-5680	213.5
1111	S41	-5696	109.5
1112	S40	-5712	213.5
1113	S39	-5728	109.5
1114	S38	-5744	213.5
1115	S37	-5760	109.5
1116	S36	-5776	213.5
1117	S35	-5792	109.5
1118	S34	-5808	213.5
1119	S33	-5824	109.5
1120	S32	-5840	213.5
1121	S31	-5856	109.5
1122	S30	-5872	213.5
1123	S29	-5888	109.5
1124	S28	-5904	213.5
1125	S27	-5920	109.5
1126	S26	-5936	213.5
1127	S25	-5952	109.5
1128	S24	-5968	213.5
1129	S23	-5984	109.5
1130	S22	-6000	213.5
1131	S21	-6016	109.5
1132	S20	-6032	213.5
1133	S19	-6048	109.5
1134	S18	-6064	213.5
1135	S17	-6080	109.5
1136	S16	-6096	213.5
1137	S15	-6112	109.5
1138	S14	-6128	213.5
1139	S13	-6144	109.5
1140	S12	-6160	213.5

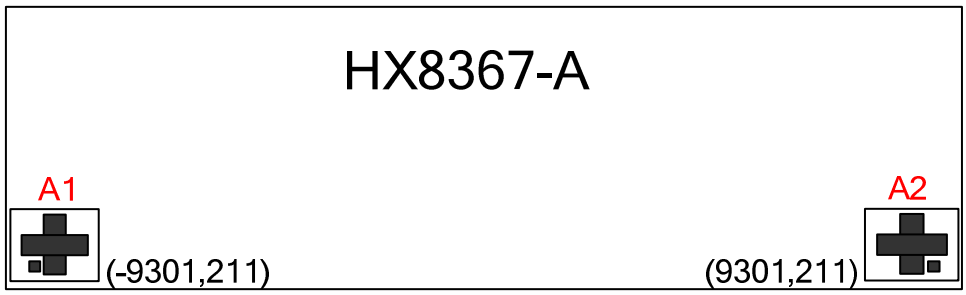
No.	Name	X	Y
1141	S11	-6176	109.5
1142	S10	-6192	213.5
1143	S9	-6208	109.5
1144	S8	-6224	213.5
1145	S7	-6240	109.5
1146	S6	-6256	213.5
1147	S5	-6272	109.5
1148	S4	-6288	213.5
1149	S3	-6304	109.5
1150	S2	-6320	213.5
1151	S1	-6336	109.5
1152	DUMMY	-6352	213.5
1153	DUMMY	-6368	109.5
1154	DUMMY	-6560	213.5
1155	VGL	-6576	109.5
1156	G320	-6592	213.5
1157	G318	-6608	109.5
1158	G316	-6624	213.5
1159	G314	-6640	109.5
1160	G312	-6656	213.5
1161	G310	-6672	109.5
1162	G308	-6688	213.5
1163	G306	-6704	109.5
1164	G304	-6720	213.5
1165	G302	-6736	109.5
1166	G300	-6752	213.5
1167	G298	-6768	109.5
1168	G296	-6784	213.5
1169	G294	-6800	109.5
1170	G292	-6816	213.5
1171	G290	-6832	109.5
1172	G288	-6848	213.5
1173	G286	-6864	109.5
1174	G284	-6880	213.5
1175	G282	-6896	109.5
1176	G280	-6912	213.5
1177	G278	-6928	109.5
1178	G276	-6944	213.5
1179	G274	-6960	109.5
1180	G272	-6976	213.5
1181	G270	-6992	109.5
1182	G268	-7008	213.5
1183	G266	-7024	109.5
1184	G264	-7040	213.5
1185	G262	-7056	109.5
1186	G260	-7072	213.5
1187	G258	-7088	109.5
1188	G256	-7104	213.5
1189	G254	-7120	109.5
1190	G252	-7136	213.5
1191	G250	-7152	109.5
1192	G248	-7168	213.5
1193	G246	-7184	109.5
1194	G244	-7200	213.5
1195	G242	-7216	109.5
1196	G240	-7232	213.5
1197	G238	-7248	109.5
1198	G236	-7264	213.5
1199	G234	-7280	109.5
1200	G232	-7296	213.5

No.	Name	X	Y
1201	G230	-7312	109.5
1202	G228	-7328	213.5
1203	G226	-7344	109.5
1204	G224	-7360	213.5
1205	G222	-7376	109.5
1206	G220	-7392	213.5
1207	G218	-7408	109.5
1208	G216	-7424	213.5
1209	G214	-7440	109.5
1210	G212	-7456	213.5
1211	G210	-7472	109.5
1212	G208	-7488	213.5
1213	G206	-7504	109.5
1214	G204	-7520	213.5
1215	G202	-7536	109.5
1216	G200	-7552	213.5
1217	G198	-7568	109.5
1218	G196	-7584	213.5
1219	G194	-7600	109.5
1220	G192	-7616	213.5
1221	G190	-7632	109.5
1222	G188	-7648	213.5
1223	G186	-7664	109.5
1224	G184	-7680	213.5
1225	G182	-7696	109.5
1226	G180	-7712	213.5
1227	G178	-7728	109.5
1228	G176	-7744	213.5
1229	G174	-7760	109.5
1230	G172	-7776	213.5
1231	G170	-7792	109.5
1232	G168	-7808	213.5
1233	G166	-7824	109.5
1234	G164	-7840	213.5
1235	G162	-7856	109.5
1236	G160	-7872	213.5
1237	G158	-7888	109.5
1238	G156	-7904	213.5
1239	G154	-7920	109.5
1240	G152	-7936	213.5
1241	G150	-7952	109.5
1242	G148	-7968	213.5
1243	G146	-7984	109.5
1244	G144	-8000	213.5
1245	G142	-8016	109.5
1246	G140	-8032	213.5
1247	G138	-8048	109.5
1248	G136	-8064	213.5
1249	G134	-8080	109.5
1250	G132	-8096	213.5
1251	G130	-8112	109.5
1252	G128	-8128	213.5
1253	G126	-8144	109.5
1254	G124	-8160	213.5
1255	G122	-8176	109.5
1256	G120	-8192	213.5
1257	G118	-8208	109.5
1258	G116	-8224	213.5
1259	G114	-8240	109.5
1260	G112	-8256	213.5

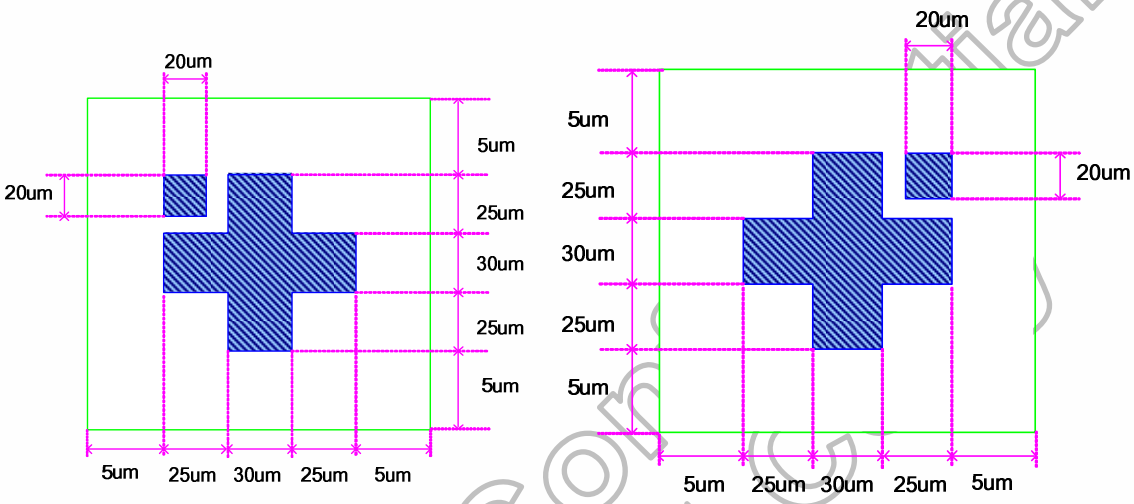
No.	Name	X	Y
1261	G110	-8272	109.5
1262	G108	-8288	213.5
1263	G106	-8304	109.5
1264	G104	-8320	213.5
1265	G102	-8336	109.5
1266	G100	-8352	213.5
1267	G98	-8368	109.5
1268	G96	-8384	213.5
1269	G94	-8400	109.5
1270	G92	-8416	213.5
1271	G90	-8432	109.5
1272	G88	-8448	213.5
1273	G86	-8464	109.5
1274	G84	-8480	213.5
1275	G82	-8496	109.5
1276	G80	-8512	213.5
1277	G78	-8528	109.5
1278	G76	-8544	213.5
1279	G74	-8560	109.5
1280	G72	-8576	213.5
1281	G70	-8592	109.5
1282	G68	-8608	213.5
1283	G66	-8624	109.5
1284	G64	-8640	213.5
1285	G62	-8656	109.5
1286	G60	-8672	213.5
1287	G58	-8688	109.5
1288	G56	-8704	213.5
1289	G54	-8720	109.5
1290	G52	-8736	213.5
1291	G50	-8752	109.5
1292	G48	-8768	213.5
1293	G46	-8784	109.5
1294	G44	-8800	213.5
1295	G42	-8816	109.5
1296	G40	-8832	213.5
1297	G38	-8848	109.5
1298	G36	-8864	213.5
1299	G34	-8880	109.5
1300	G32	-8896	213.5
1301	G30	-8912	109.5
1302	G28	-8928	213.5
1303	G26	-8944	109.5
1304	G24	-8960	213.5
1305	G22	-8976	109.5
1306	G20	-8992	213.5
1307	G18	-9008	109.5
1308	G16	-9024	213.5
1309	G14	-9040	109.5
1310	G12	-9056	213.5
1311	G10	-9072	109.5
1312	G8	-9088	213.5
1313	G6	-9104	109.5
1314	G4	-9120	213.5
1315	G2	-9136	109.5
1316	VGL	-9152	213.5
1317	DUMMYR5	-9168	109.5
1318	DUMMYR6	-9184	213.5
1319	DUMMY	-9200	109.5
1320	DUMMY	-9216	213.5

Alignment mark	X	Y
A1	-9301	211
A2	9301	211

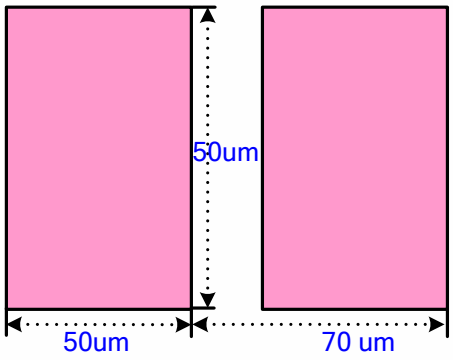
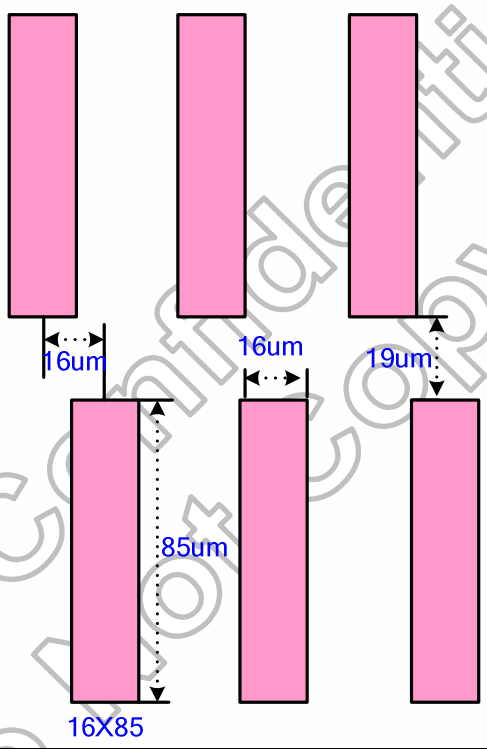
4.4 Alignment mark



A_MARK (A1) A_MARK (A2)



4.5 Bump size

Input PAD	
Output PAD	

5. Interface

The HX8367-A has a system interface circuit for register command/GRAM data transferring, and a RGB interface circuit for display data transferring during animated display. The system interface circuit uses data bus pins (DB17-0). Since the data bus pins (DB17-0) can be used as input in RGB interface circuit, the HX8367-A shows animated display with less wiring.

System interface can be used to access internal command and internal 18-bit/pixel GRAM. The RGB interface is only used to access display data. Please make sure that in RGB interface mode, the input display data is not written to GRAM and is displayed directly.

5.1 System interface circuit

The system interface circuit in HX8367-A supports 18-/16-/9-/8-bit bus width parallel bus system interface for I80 series CPU, and 4-/3-wire serial bus system interface for serial data input. When NCS = "L", the parallel and serial bus system interface of the HX8367-A become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the display data RAM. The input bus format of system interface circuit is selected by external pins setting. For selecting the input bus format, please refer to Table 5.1.

IM3	IM2	IM1	IM0	Interface	DNC_SCL	NWR_SCL	Data Bus use	
							Register/Content	GRAM
0	0	0	0	8080 MCU 16-bits Parallel type I	DNC	NWR	D7-D0	D15-D0: 16-bit data
0	0	0	1	8080 MCU 8-bits Parallel type I	DNC	NWR	D7-D0	D7-D0: 8-bits Data
0	0	1	0	8080 MCU 16-bits Parallel type II	DNC	NWR	D8-D1	D17-10, D8-D1: 16-bit data
0	0	1	1	8080 MCU 8-bits Parallel type II	DNC	NWR	D17-D10	D17-D10: 8-bits Data
0	1	0	ID	3-wire Serial interface	-	SCL	SDI, SDO	
0	1	1	-	4-wire Serial interface	DNC	SCL	SDI, SDO	
1	0	0	0	8080 MCU 18-bits Parallel type I	DNC	NWR	D7-D0	D17-D0: 18-bits Data
1	0	0	1	8080 MCU 9-bits Parallel type I	DNC	NWR	D7-D0	D8-D0: 9-bits Data
1	0	1	0	8080 MCU 18-bits Parallel type II	DNC	NWR	D8-D1	D17-D0: 18-bits Data
1	0	1	1	8080 MCU 9-bits Parallel type II	DNC	NWR	D17-D10	D17-D9: 9-bits Data
Other Setting				Setting Invalid				

Table 5.1 Input bus format selection of system interface circuit

It has an Index Register (IR) in HX8367-A to store index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

5.1.1 Parallel bus system interface

The input / output data from data pins (DB17-0) and signal operation of the I80 series parallel bus interface are listed in Table 5.2.

Operations	NWR_SCL	NRD	DNC_SCL
Writes Indexes into IR	0	1	0
Reads internal status	1	0	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 5.2 Data pin function for I80 series CPU

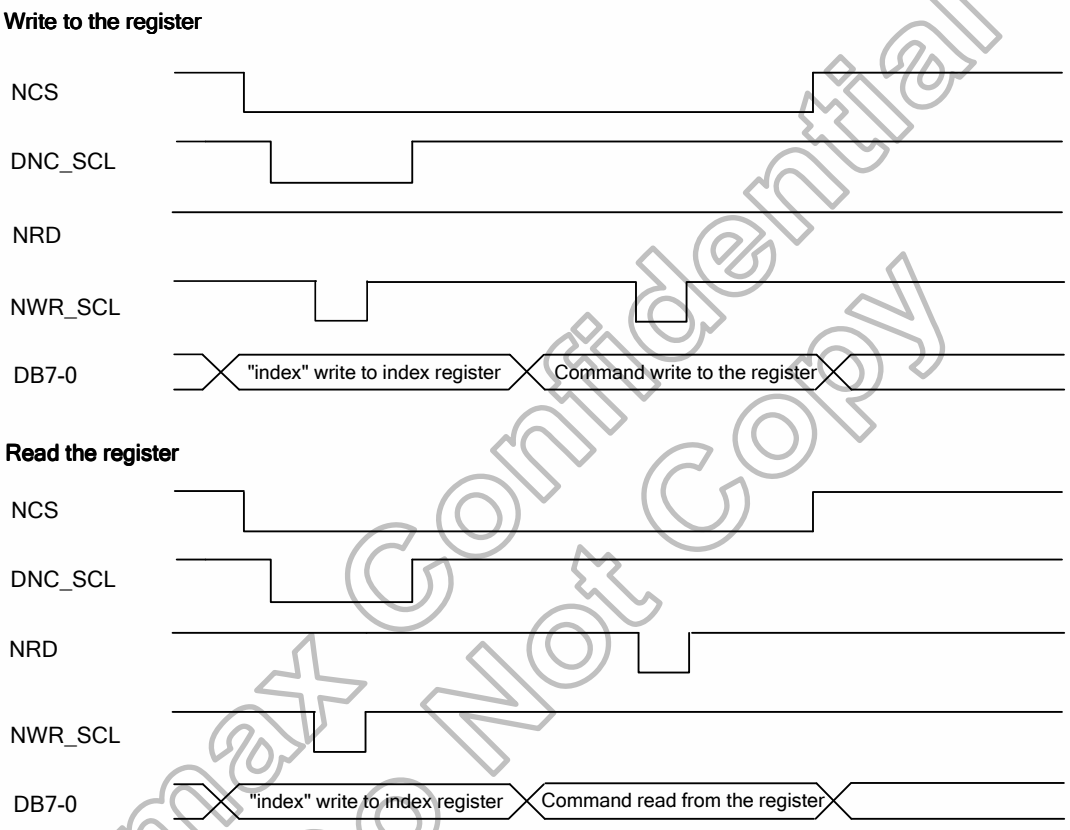


Figure 5.1 Register read/write timing in parallel bus system interface (for I80 series MPU)

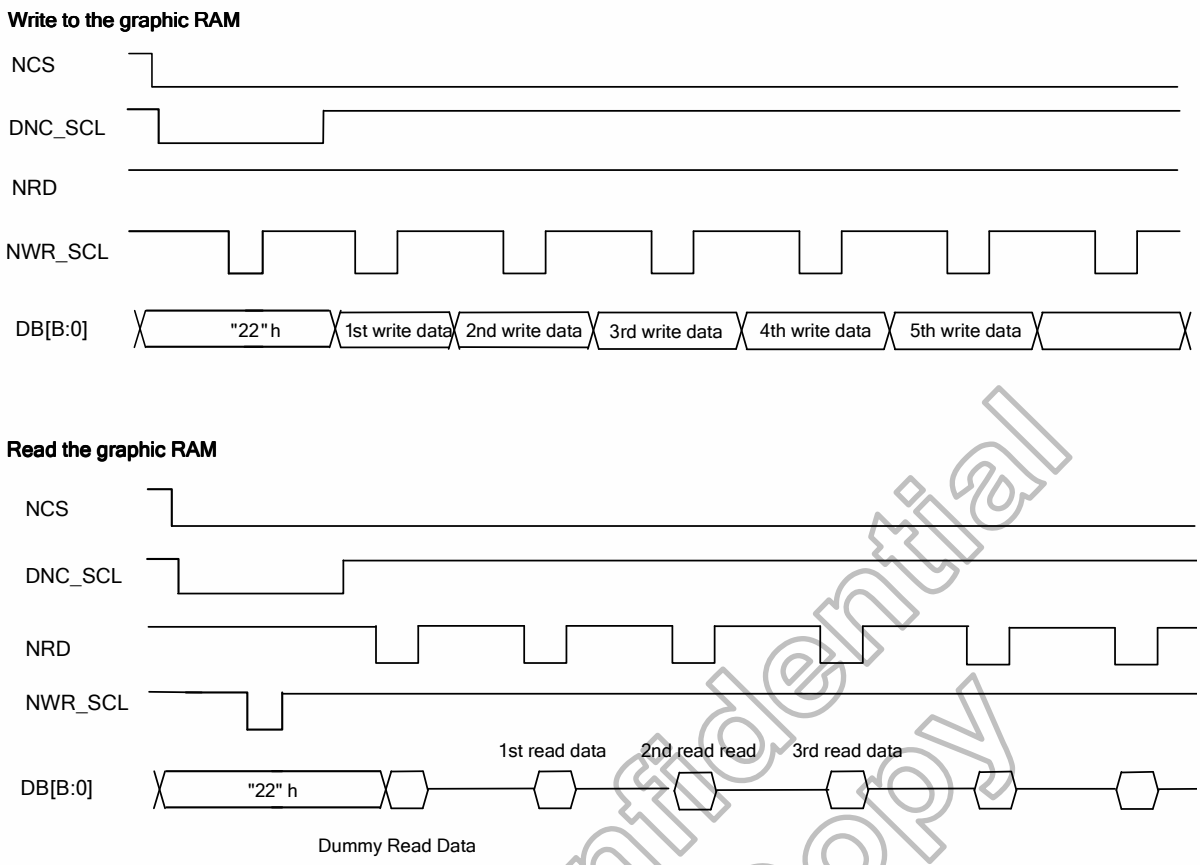


Figure 5.2 GRAM read/write timing in parallel bus system interface (for I80 series MPU)

5.1.2 MCU data color coding

MCU Data Color Coding for RAM data ***Write***

- Parallel 8-bit bus interface typeI (IM3,IM2,IM1,IM0="0001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	4K-Color (2-pixel/ 3-byte)
	x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	
05h	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-byte)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (6+6+6)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	
07	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	262K-Color (2+8+8)
	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G5	G4	G3	G2	
	x	x	x	x	x	x	x	x	x	x	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.3 8-bit parallel interface type I GRAM write table

- Parallel 16-bit bus interface typeI (IM3,IM2,IM1,IM0="0000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Color
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	65K-Color
06h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixel/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
07h	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	262K-Color (16+2)
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B1	B0	
04h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	262K-Color (2+16)
	x	x	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.4 16-bit parallel interface type I GRAM write table

- Parallel 9-bit bus interface typeI (IM3,IM2,IM1,IM0="1001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2byte)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.5 9-bit parallel interface type I GRAM write table

- Parallel 18-bit bus interface typeI (IM3,IM2,IM1,IM0="1000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.6 18-bit parallel interface type I GRAM write table

- Parallel 8-bit bus interface typeII (IM3,IM2,IM1,IM0="0011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	R3	R2	R1	R0	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	4K-Color (2-pixel/ 3-byte)
	B3	B2	B1	B0	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	
	G3	G2	G1	G0	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color (1-pixel/ 2-byte)
	G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
06h	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (6+6+6)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	
07h	x	x	x	x	x	x	R5	R4	x	x	x	x	x	x	x	x	x	x	262K-Color (2+8+8)
	R3	R2	R1	R0	G5	G4	G3	G2	x	x	x	x	x	x	x	x	x	x	
	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	

Table 5.7 8-bit parallel interface type II GRAM write table

- Parallel 16-bit bus interface typeII (IM3,IM2,IM1,IM0="0010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
									x	0	0	1	0	0	0	1	0	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	R3	R2	R1	R0	x	G3	G2	G1	G0	B3	B2	B1	B0	x	4K-Color
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	65K-Color
06h	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixel/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	
07h	R5	R4	R3	R2	R1	R0	G5	G4	x	G3	G2	G1	G0	B5	B4	B3	B2	x	262K-Color (16+2)
	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
04h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	x	262K-Color (2+16)
	R3	R2	R1	R0	G5	G4	G3	G2	x	G1	G0	B5	B4	B3	B2	B1	B0	x	

Table 5.8 16-bit parallel interface type II GRAM write set table

- Parallel 9-bit bus interface typeII (IM3,IM2,IM1,IM0="1011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
17H	D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 2byte)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5.9 9-bit parallel interface set type II GRAM write table

- Parallel 18-bit bus interface typeII (IM3,IM2,IM1,IM0="1010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.10 18-bit parallel interface type II GRAM write set table

18-bit parallel bus system interface

The I80-system 18-bit parallel bus interface **type I** used by setting external pins “IM3, IM2, IM1, IM0” pins to “1000”. And the I80-system 18-bit parallel bus interface **type II** used by setting ““IM3, IM2, IM1, IM0” pins to “1010”. Figure 5.3 is the example of interface with I80 microcomputer system interface.

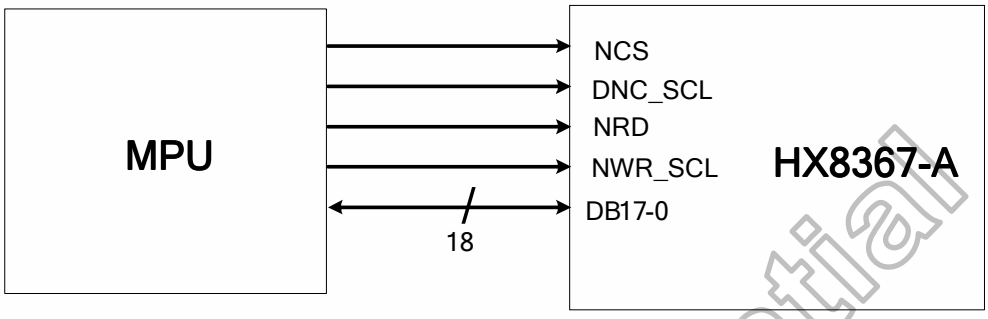


Figure 5.3 Example of I80-system 18-bit parallel bus interface

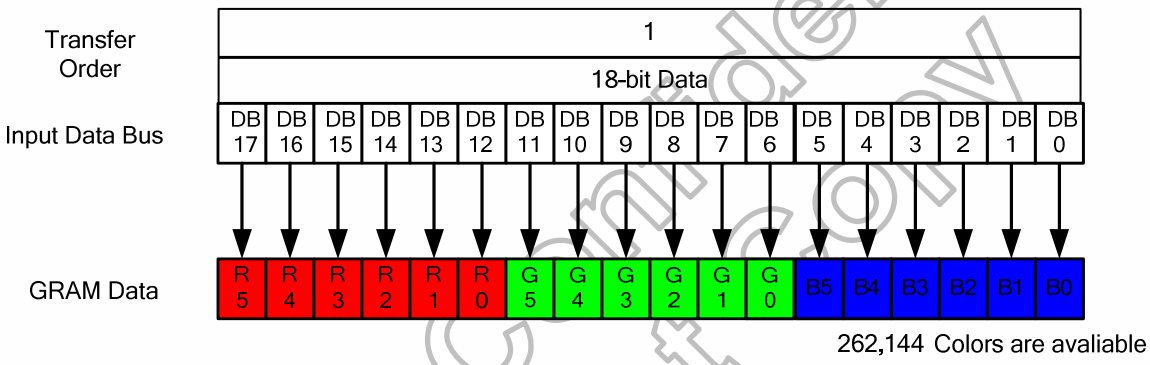


Figure 5.4 Input data bus and GRAM data mapping in 18-bit bus system interface with 18 bit-data input (“IM3, IM2, IM1, IM”=”1010” or “1000”)

16-bit parallel bus system interface

The I80-system 16-bit parallel bus interface **type I** used by setting external pins ““IM3, IM2, IM1, IM0” pins to “0000”. And I80-system 16-bit parallel bus interface **type II** used by setting ““IM3, IM2, IM1, IM0” pins to “0010”. Figure 5.5 is the example of type I interface with I80 microcomputer system interface. And Figure 5.6 is the example of type II interface with I80 microcomputer system interface.

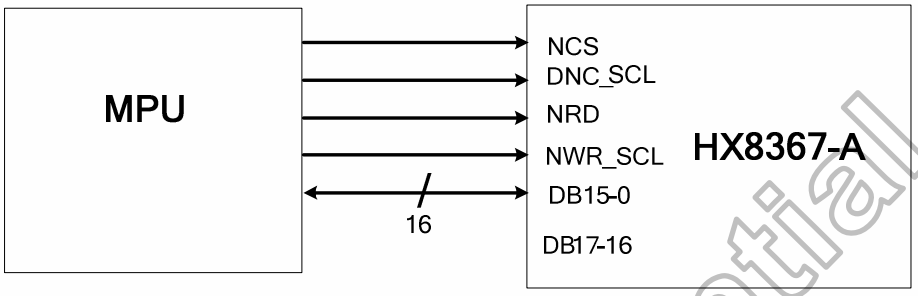


Figure 5.5 Example of I80 system 16-bit parallel bus interface type I

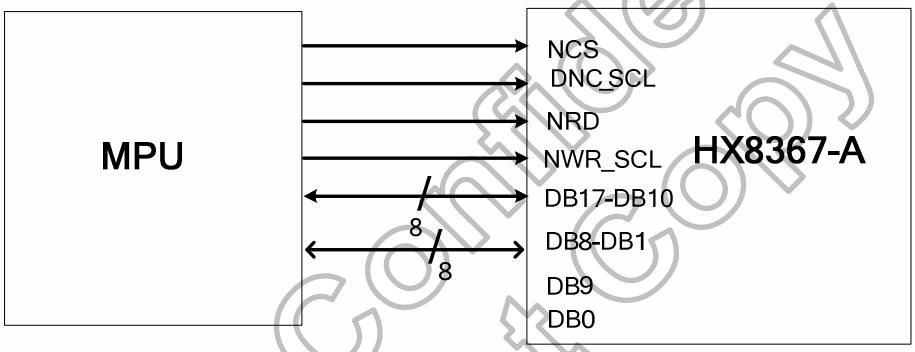


Figure 5.6 Example of I80 system 16-bit parallel bus interface type II

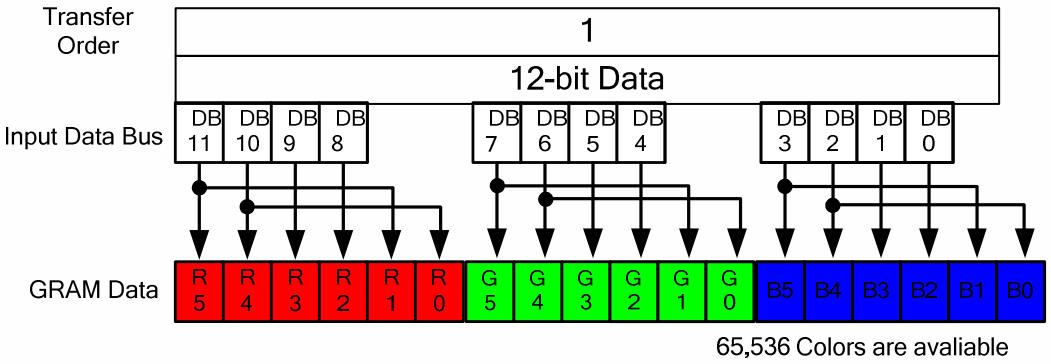


Figure 5.7 Input data bus and GRAM data mapping in 16-bit bus system interface with 12 bit-data input (R17H=03h and "IM3, IM2, IM1, IM0"="0000")

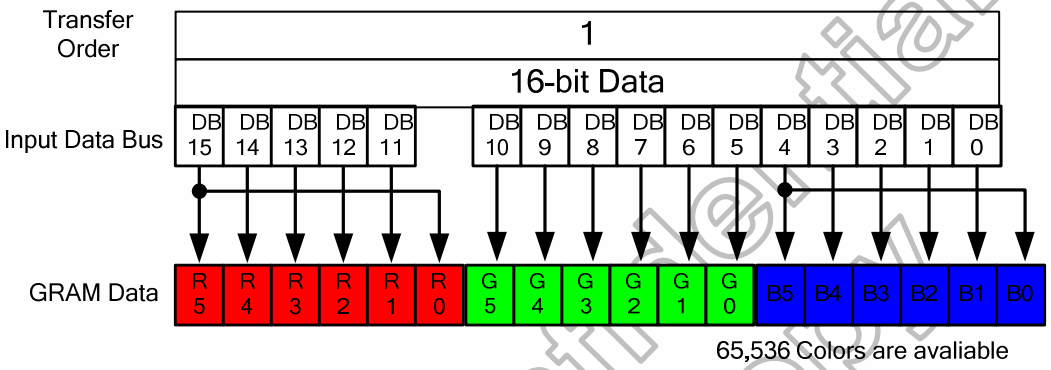


Figure 5.8 Input data bus and GRAM data mapping in 16-bit bus system interface with 16 bit-data input (R17H=05h and "IM3, IM2, IM1, IM0"="0000")

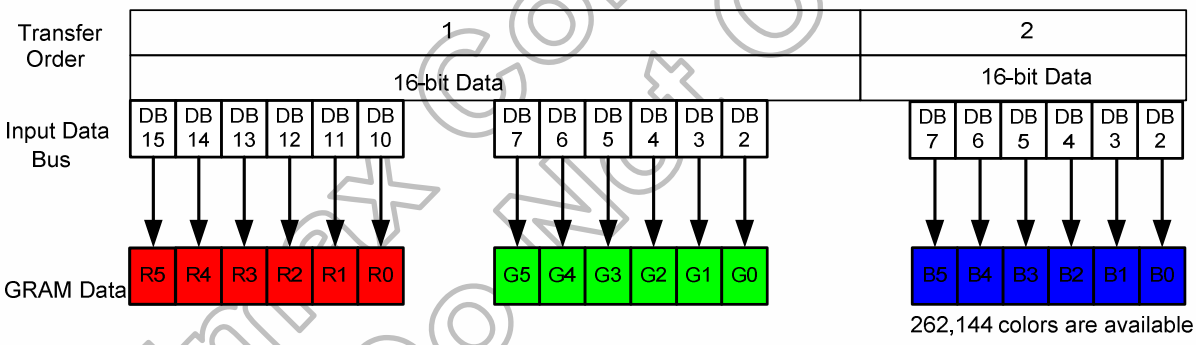


Figure 5.9 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(12+6) bit-data input (R17H=06h and "IM3, IM2, IM1, IM0"="0000")

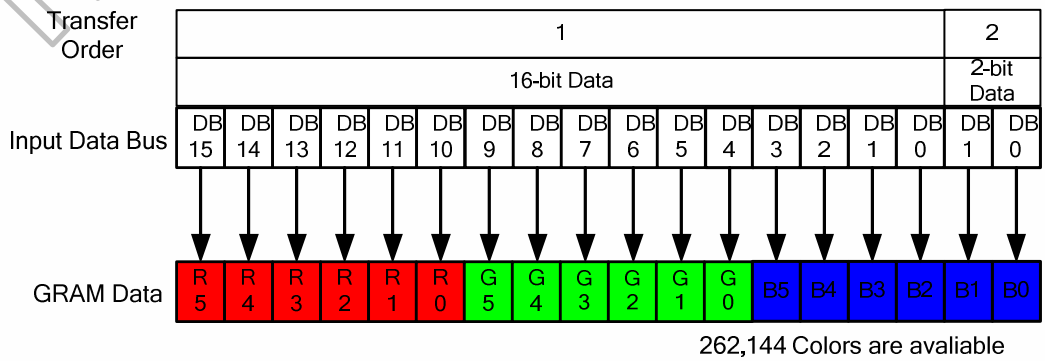


Figure 5.10 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (R17H=07h and "IM3, IM2, IM1, IM0"="0000")

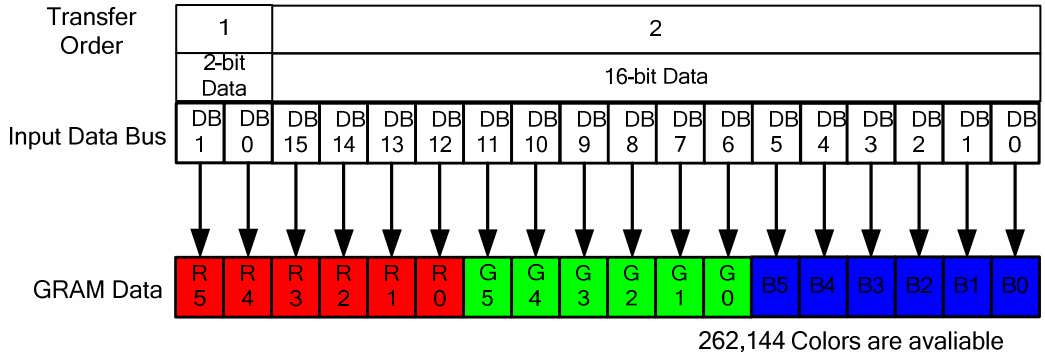


Figure 5.11 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(2+16) bit-data input (R17H=04h and "IM3, IM2, IM1, IM0"="0000")

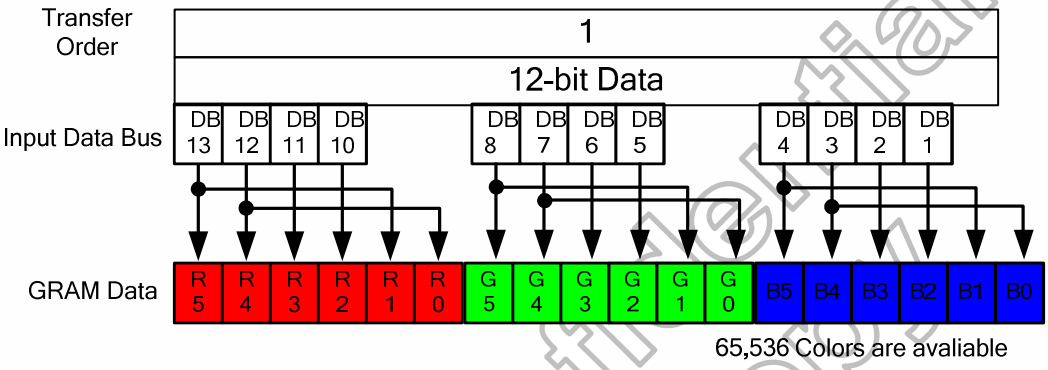


Figure 5.12 Input data bus and GRAM data mapping in 16-bit bus system interface with 12 bit-data input (R17H=03h and "IM3, IM2, IM1, IM0"="0010")

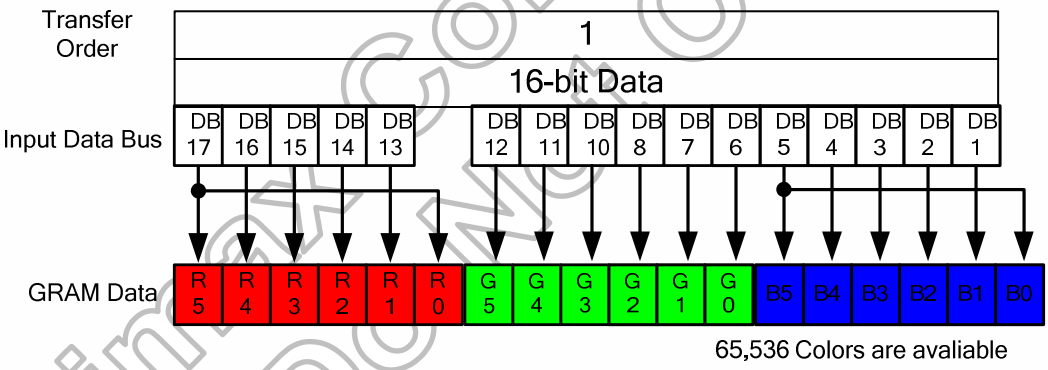


Figure 5.13 Input data bus and GRAM data mapping in 16-bit bus system interface with 16 bit-data input (R17H=05h and "IM3, IM2, IM1, IM0"="0010")

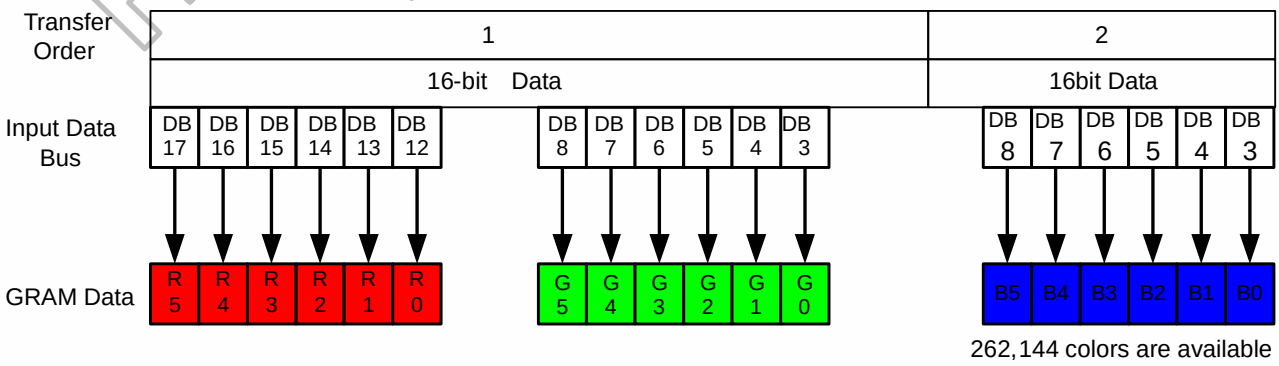


Figure 5.14 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(12+6) bit-data input (R17H=06h and "IM3, IM2, IM1, IM0"="0010")

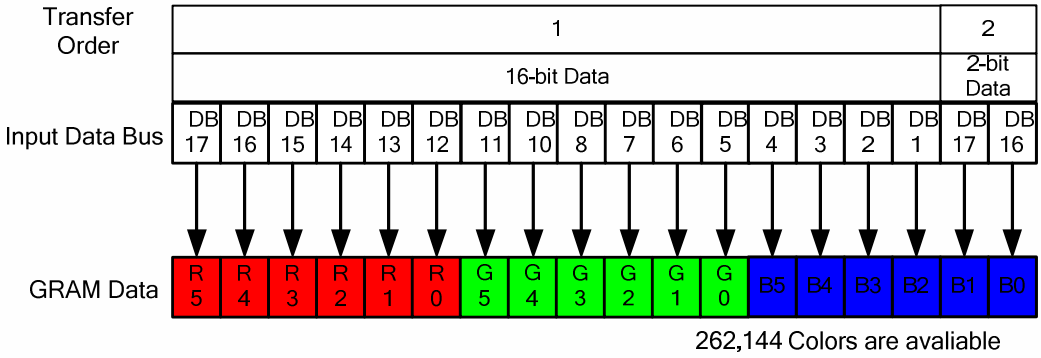


Figure 5.15 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (R17H=07h and "IM3, IM2, IM1, IM0"="0010")

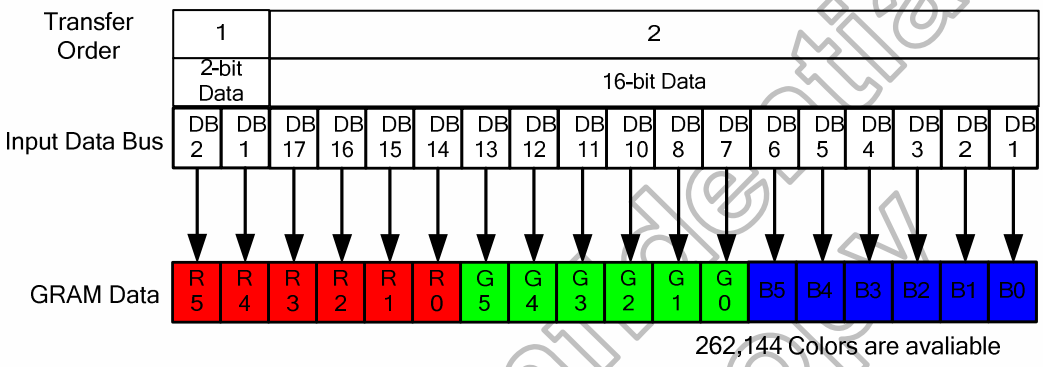


Figure 5.16 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(2+16) bit-data input (R17H=04h and "IM3, IM2, IM1, IM0"="0010")

9-bit parallel bus system interface

The I80-system 9-bit parallel bus interface **type I** used by setting external pins ““IM3, IM2, IM1, IM0” pins to “1001”. And I80-system 9-bit parallel bus interface **type II** used by setting ““IM3, IM2, IM1, IM0” pins to “1011”. Figure 5.17 is the example of type I interface with I80 microcomputer system interface. And Figure 5.18 is the example of type II interface with I80 microcomputer system interface.

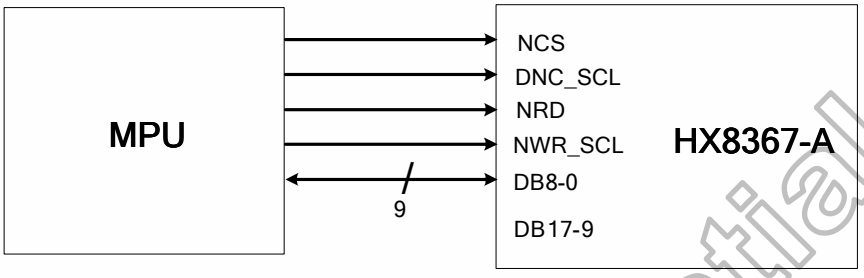


Figure 5.17 Example of I80 system 9-bit parallel bus interface type I

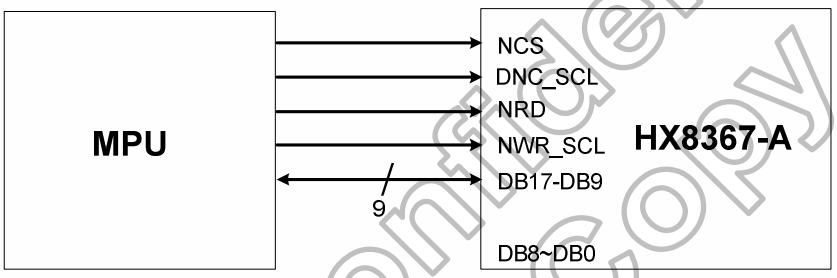


Figure 5.18 Example of I80 system 9-bit parallel bus interface type II

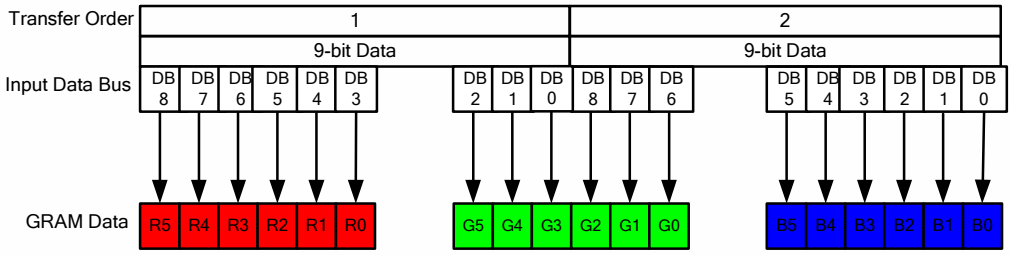


Figure 5.19 Input data bus and GRAM data mapping in 9-bit bus system interface with 18 bit-data input (R17H=06h and "IM3, IM2, IM1, IM0"="1001")

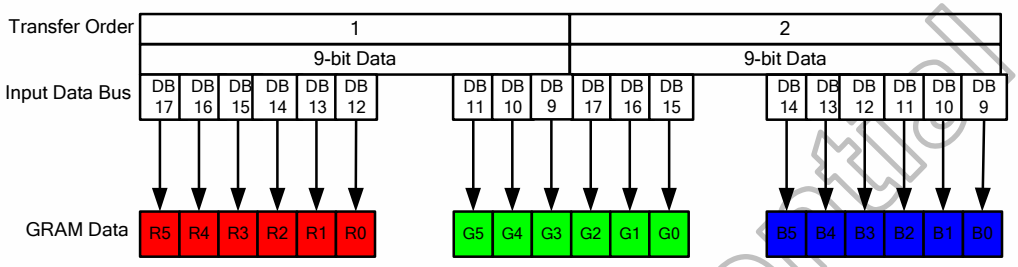


Figure 5.20 Input data bus and GRAM data mapping in 9-bit bus system interface with 18 bit-data input (R17H=06h and "IM3, IM2, IM1, IM0"="1011")

8-bit parallel bus system interface

The I80-system 8-bit parallel bus interface **type I** used by setting external pins ““IM3, IM2, IM1, IM0” pins to “0001”. And I80-system 8-bit parallel bus interface **type II** used by setting ““IM3, IM2, IM1, IM0” pins to “0011”. Figure 5.21 is the example of type I interface with I80 microcomputer system interface. And Figure 5.22 is the example of type II interface with I80 microcomputer system interface.

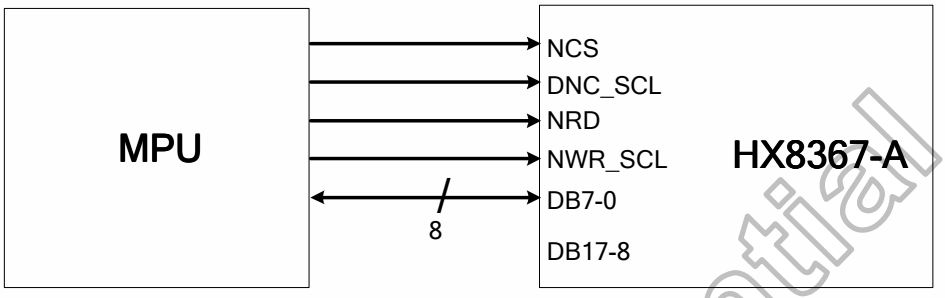


Figure 5.21 Example of I80-system 8-bit parallel bus interface type I

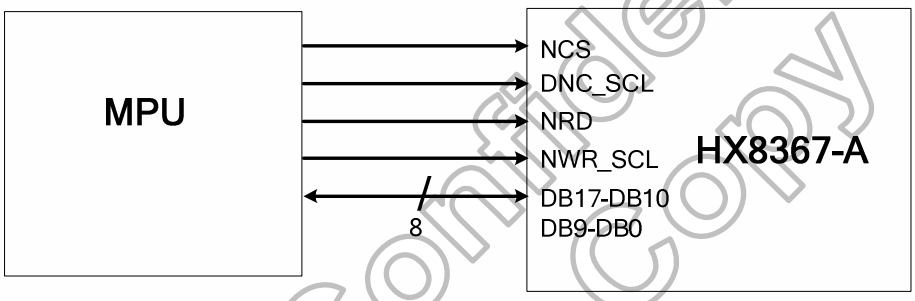


Figure 5.22 Example of I80-system 8-bit parallel bus interface type II

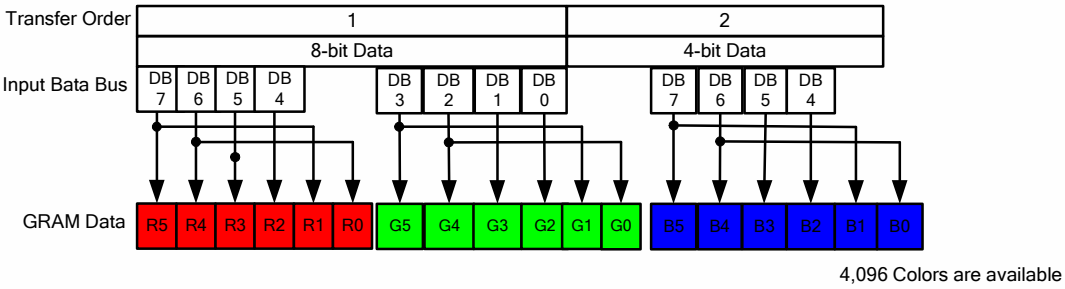


Figure 5.23 Input data bus and GRAM data mapping in 8-bit bus system interface with 12 bit-data input (R17H=03h and“IM3, IM2, IM1, IM0”=”0001”)

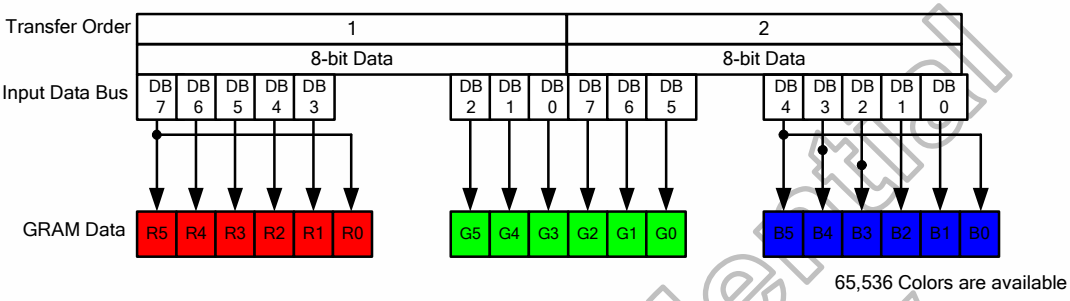


Figure 5.24 Input data bus and GRAM data mapping in 8-bit bus system interface with 16 bit-data input (R17H=05h and “IM3, IM2, IM1, IM0”=”0001”)

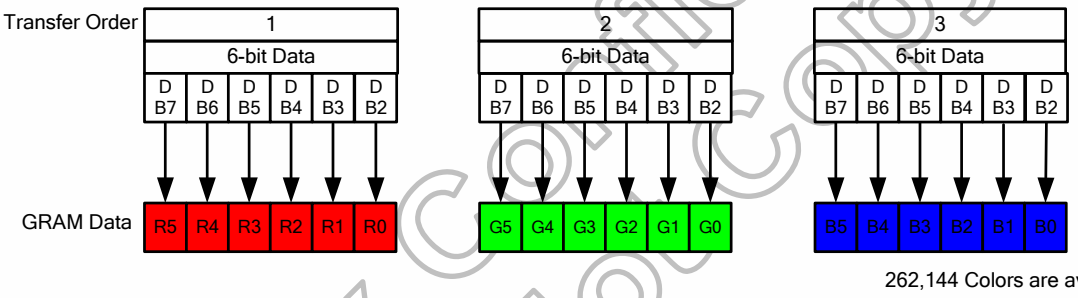


Figure 5.25 Input data bus and GRAM data mapping in 8-bit bus system interface with 18 bit-data input (R17H=06h and “IM3, IM2, IM1, IM0”=”0001”)

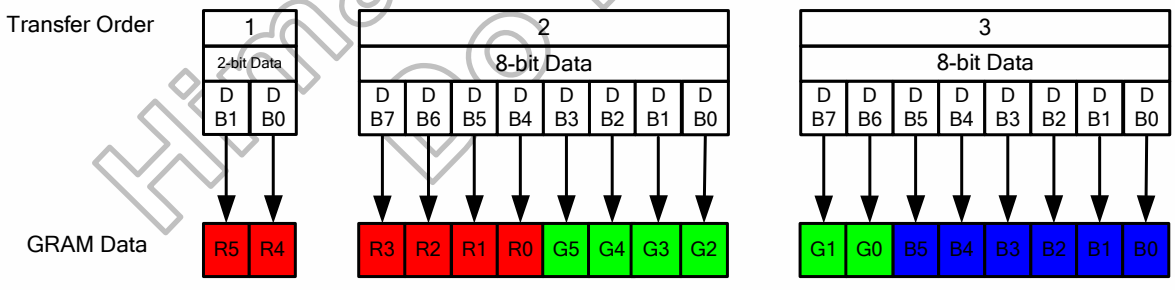


Figure 5.26 Input data bus and GRAM data mapping in 8-bit bus system interface with 18(2+8+8) bit-data input (R17H=07h and “IM3, IM2, IM1, IM0”=”0001”)

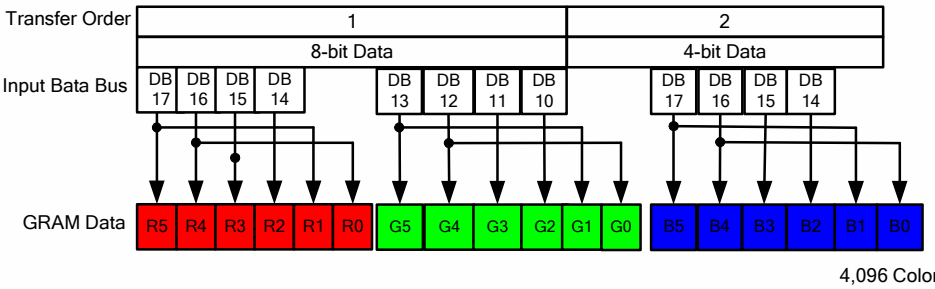


Figure 5.27 Input data bus and GRAM data mapping in 8-bit bus system interface with 12 bit-data input (R17H=03h and"IM3, IM2, IM1, IM0"="0011")

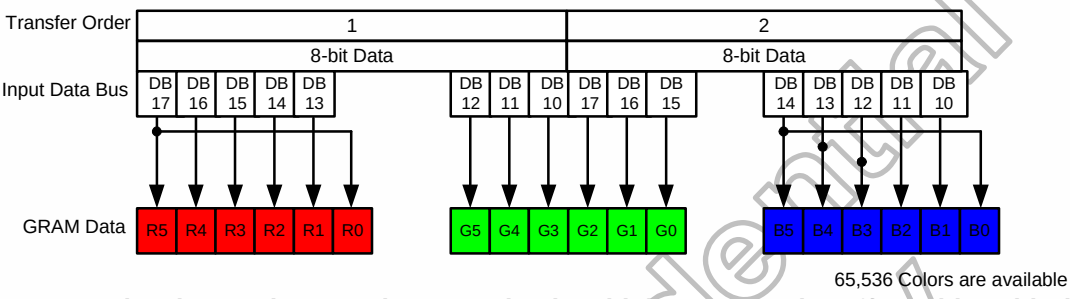


Figure 5.28 Input data bus and GRAM data mapping in 8-bit bus system interface with 16 bit-data input (R17H=05h and "IM3, IM2, IM1, IM0"="0011")

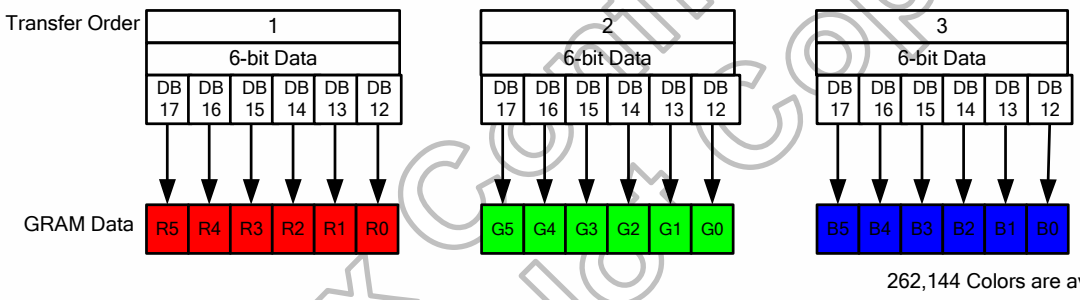


Figure 5.29 Input data bus and GRAM data mapping in 8-bit bus system interface with 18 bit-data input (R17H=06h and "IM3, IM2, IM1, IM0"="0011")

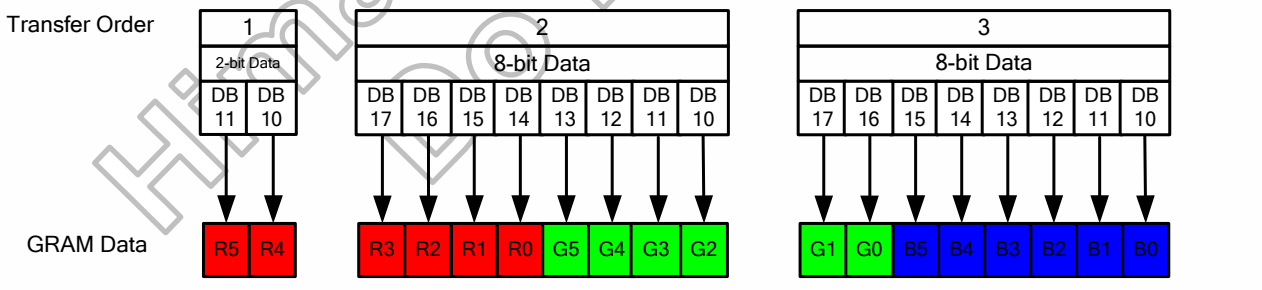


Figure 5.30 Input data bus and GRAM data mapping in 8-bit bus system interface with 18(2+8+8) bit-data input (R17H=07h and "IM3, IM2, IM1, IM0"="0011")

MCU Data Color Coding for RAM data ***Read***

- Parallel 8-bit bus interface type I (IM3,IM2,IM1,IM0="0001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.11 8-bits parallel interface type I GRAM read table

- Parallel 16-bit bus interface type I (IM3,IM2,IM1,IM0="0000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixel/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.12 16-bit parallel interface type I GRAM read table

- Parallel 9-bit bus interface type I (IM3,IM2,IM1,IM0="1001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.13 9-bit parallel interface type I GRAM read table

- Parallel 18-bit bus interface type I (IM3,IM2,IM1,IM0="1000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.14 18-bit parallel interface type I GRAM read table

- Parallel 8-bit bus interface type II (IM3,IM2,IM1,IM0=”0011”)

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 3byte)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5.15 8-bit parallel interface type II GRAM read table

- Parallel 16-bit bus interface type II (IM3,IM2,IM1,IM0=”0010”)

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixel/ 3byte)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	

Table 5.16 16-bit parallel interface type II GRAM read table

- Parallel 9-Bits Bus Interface type II (IM3,IM2,IM1,IM0=”1011”)

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	X	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 2byte)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5.17 9-bit parallel interface type II GRAM read table

- Parallel 18-Bits Bus Interface type II (IM3,IM2,IM1,IM0=”1010”)

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.18 18-bit parallel interface type II GRAM read table

5.1.3 Serial bus system interface

The HX8367-A supports two kinds' serial bus interface in register-content mode by setting external pins "IM2, IM1" pins to "10" 3-wire serial interface and "IM2, IM1" pins to "11" 4-wire serial interface. The serial bus system interface mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI), and the serial transfer clock signal (NWR_SCL).

5.1.3.1 3-wire serial interface

As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to "01110", and the least significant bit of the identification code must be set as the external pin IM0 input as "ID".

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to "0" when writing data to the index register or reading the status and it must be set to "1" when writing or reading a command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

RS	R/W	Function
0	0	Set index register
1	0	Writes Instruction or GRAM data
1	1	Reads command (Not support GRAM read)

Table 5.19 Function of RS and R/W bit bus

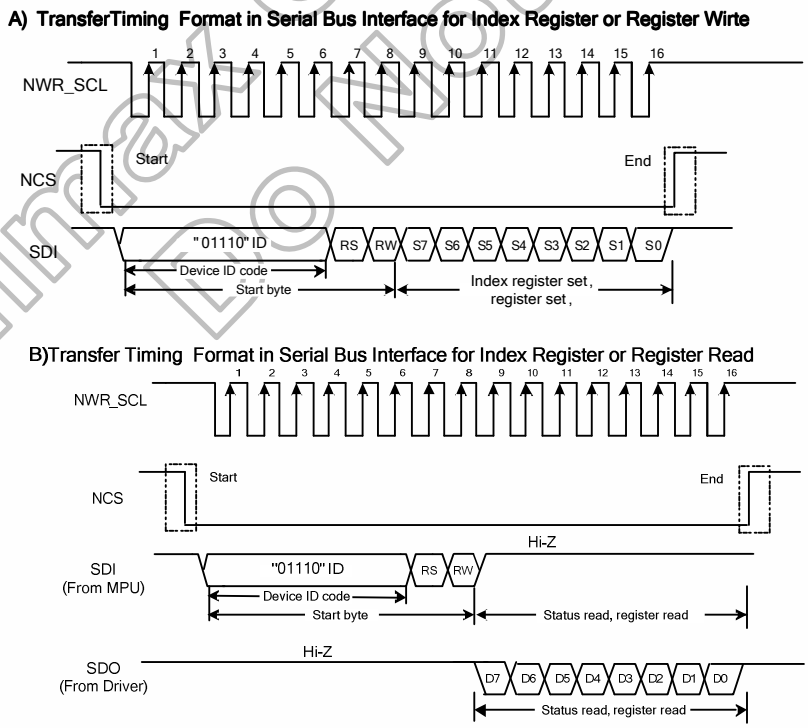


Figure 5.31 Index register read/write timing in 3-wire serial bus system interface

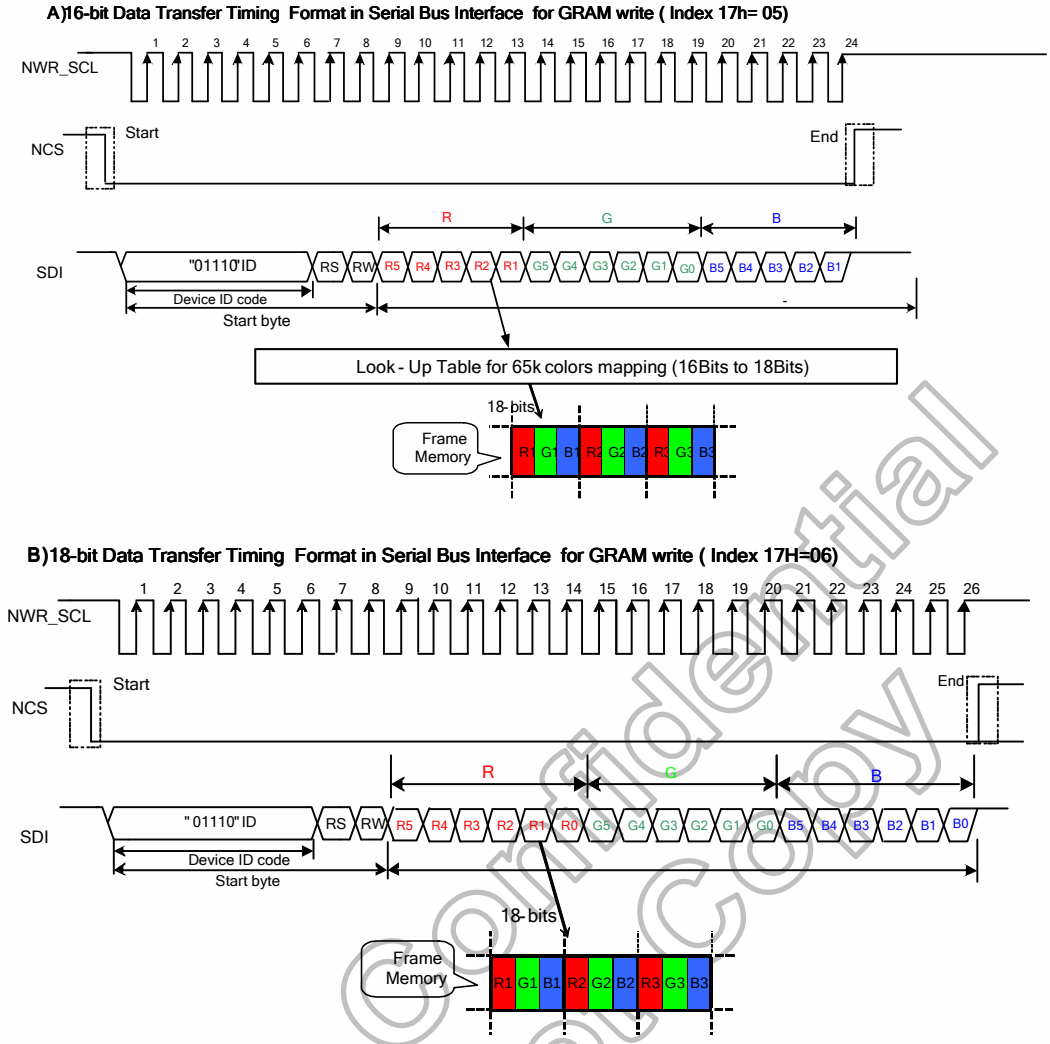


Figure 5.32 Data write timing in 3-wire serial bus system interface

5.1.3.2 4-wire serial interface

4-pin serial case, data packet contains just transmission byte and control bit DNC is transferred by DNC_SCL pin. If DNC_SCL is low, the transmission byte is command byte. If DNC_SCL is high, the transmission byte is stored to index register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, NWR_SCL clock pulse or SDI data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

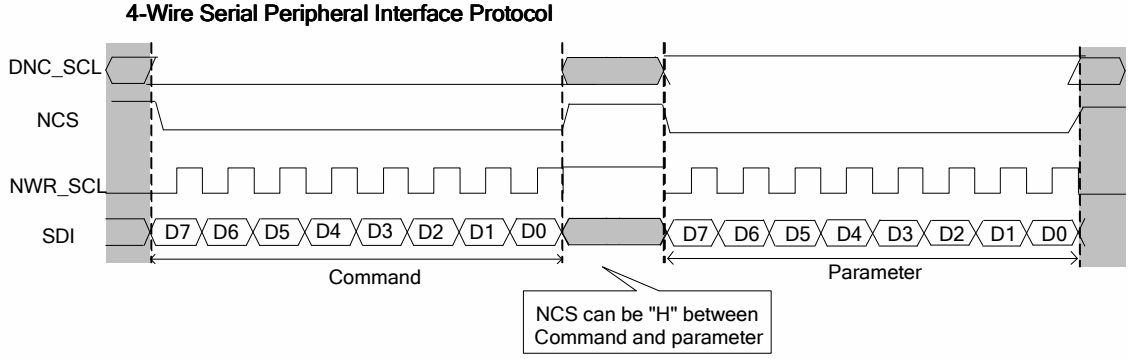


Figure 5.33 Index register write timing in 4-wire serial bus system interface

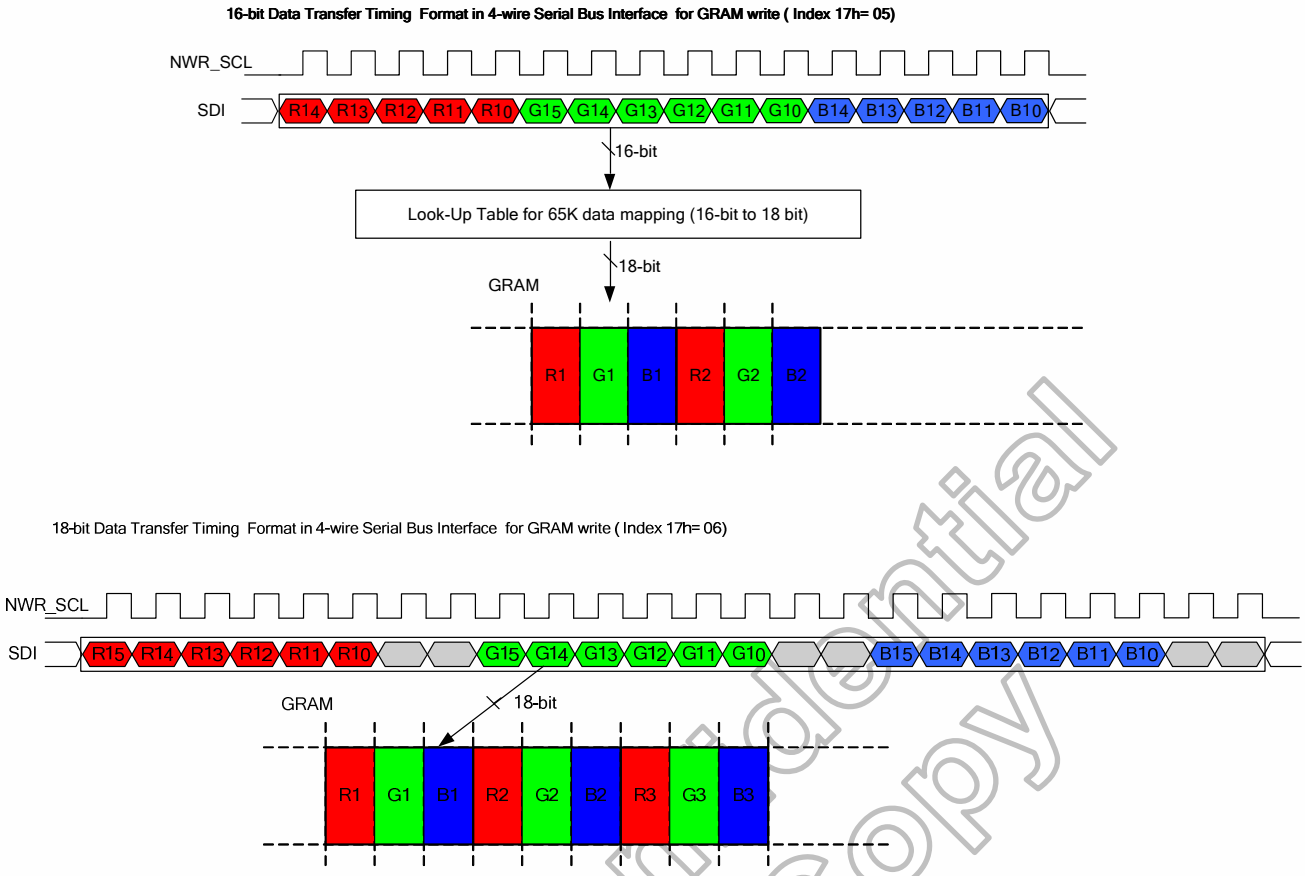


Figure 5.34 Data write timing in 4-wire serial bus system interface

5.2 RGB interface

The HX8367-A uses **RCM [1:0] =’10’ or ‘11’ software setting to select RGB interface.** When after Power on Sequence, the RGB interface is activated. When RCM [1:0] =’10’ use VSYNC, HSYNC, DE, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 1). When RCM [1:0] =’11’ use VSYNC, HSYNC, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 2)

Pixel clock (DOTCLK) must be running all the time without stopping and it is used to entering VSYNC, HSYNC, DE and DB17-0 lines states when there is a rising edge of the DOTCLK.

In RGB interface mode 1, the valid display data is inputted in pixel unit via DB17-0 according to the high-level(‘H’) of DE signal, and display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and pixel clock (DOTCLK). In RGB interface mode 2, the valid display data is inputted in pixel unit via DB17-0 according to the HBP setting of HSYNC signal, and the VBP setting of VSYNC. In these two RGB interface mode, the input display data is not written to GRAM and is displayed directly.

Vertical synchronization (VSYNC) signal is used to tell when there is received a new frame of the display, and this is negative (‘-‘, ‘0’, low) active. Horizontal synchronization signal (HSYNC) is used to tell when there is received a new line of the frame, and this is negative (‘-‘, ‘0’, low) active. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display, and this is positive (‘+’, ‘1’, high) active. DB17-0 are used to tell what is the information of the image that is transferred on the display when DE=’H’.

The pixel clock cycle is described in the following figure.

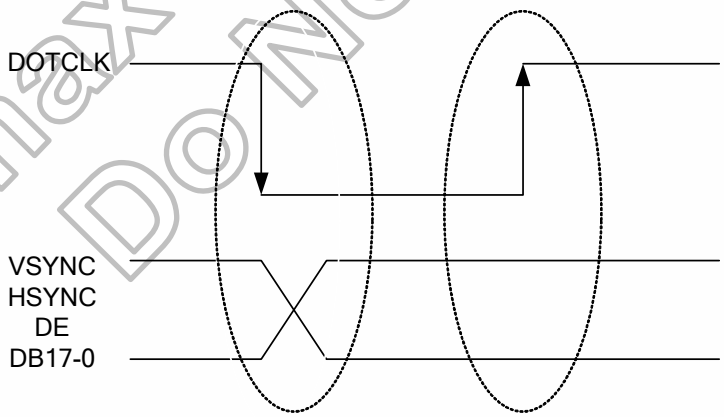


Figure 5.35 DOTCLK cycle

General timing diagram in RGB interface is as follow

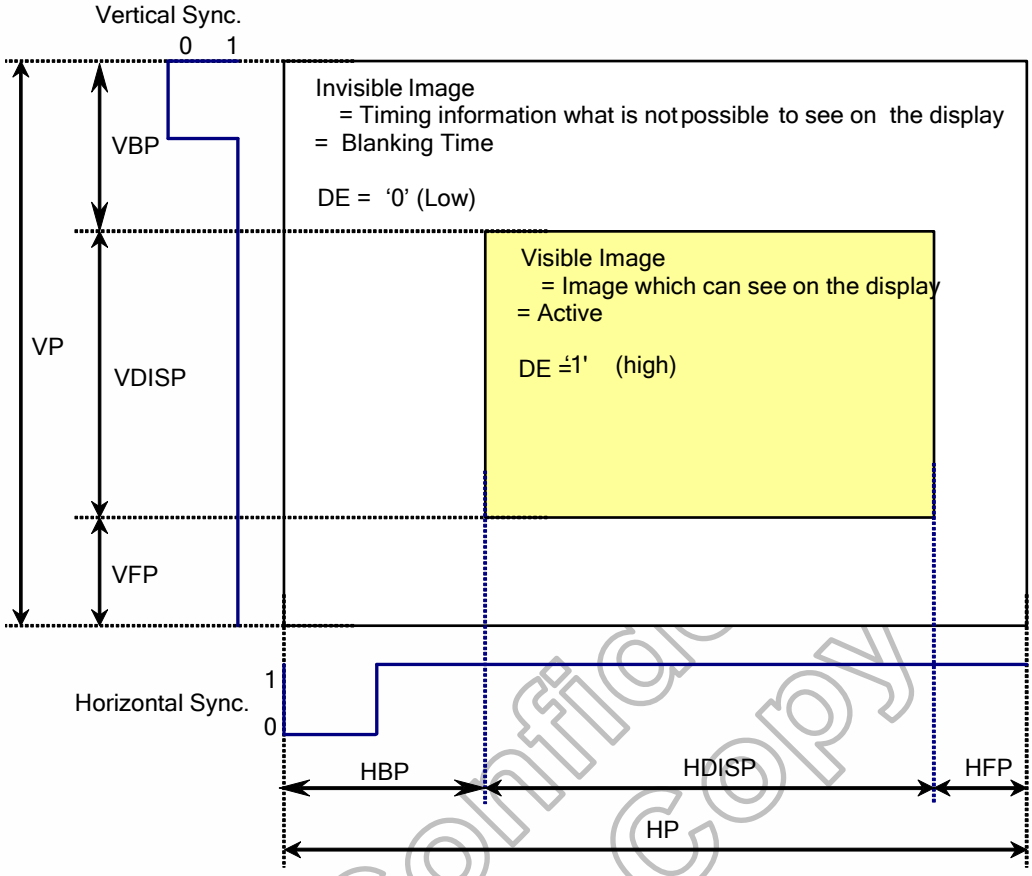
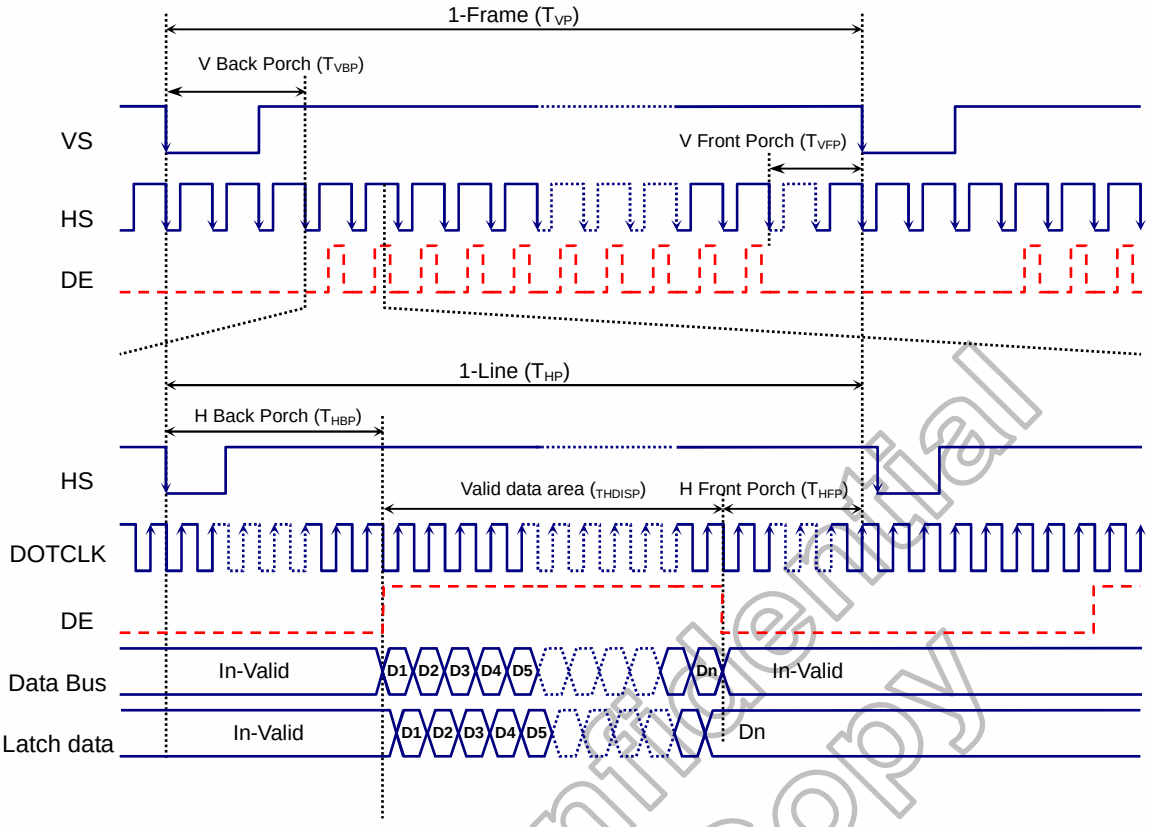


Figure 5.36 RGB interface circuit input timing diagram

The image information is correct on the display when the timings are in range on the interface. However, the image information will be incorrect on the display, when timings are out of the range on the RGB interface and the correct image information will be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range RGB interface timings.



Note: (1) RGB mode 2 doesn't need DE signal
(2) EPL='0', VSPL='0', HSPL='0' and DPL='0' of SETRGBIF (32H) command.

Figure 5.37 RGB mode timing diagram

All 3 kinds of bus width can be available during RGB interface mode (selected by COLMOD (17H) command for 6-bit, 16-bit and 18-bit data width)

17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
50h	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bit data
60h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit data
17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
E0h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bit data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note: (1) When 17H=”E0h”, 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color Depth information.
(2) Only 17H= “50h”,”60h”, “E0h” are valid on RGB I/F, Others are invalid.
(3) ‘X’ don’t care, but need to set IOVCC or VSSD level.

Table 5.20 RGB interface bus width set table

RGB interface mode

RGB I/F Mode	DOTCLK	DE	VS	HS	Video Data bus DB [B: 0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

There are 2 kinds of RGB mode which is selected by RCM1 & RCM0 software setting.

In RGB Mode 1 (RCM1, RCM0 = “10”), writing data to display is done by DOTCLK and Video Data Bus (DB [17:0]), when DE is high state. The external synchronization signals (DOTCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer DOTCLK, VS, HS and DE signals to driver.

In RGB Mode 2 (RCM1, RCM0 = “11”), blanking porch setting of VS and HS signals are defined by R33h and R34h command. DE pin is not used.

5.2.1 Color order on RGB interface

The meaning of the pixel information, when there are used 3 components/pixel (Red, Green and Blue) on RGB interface, is describing on the following table:

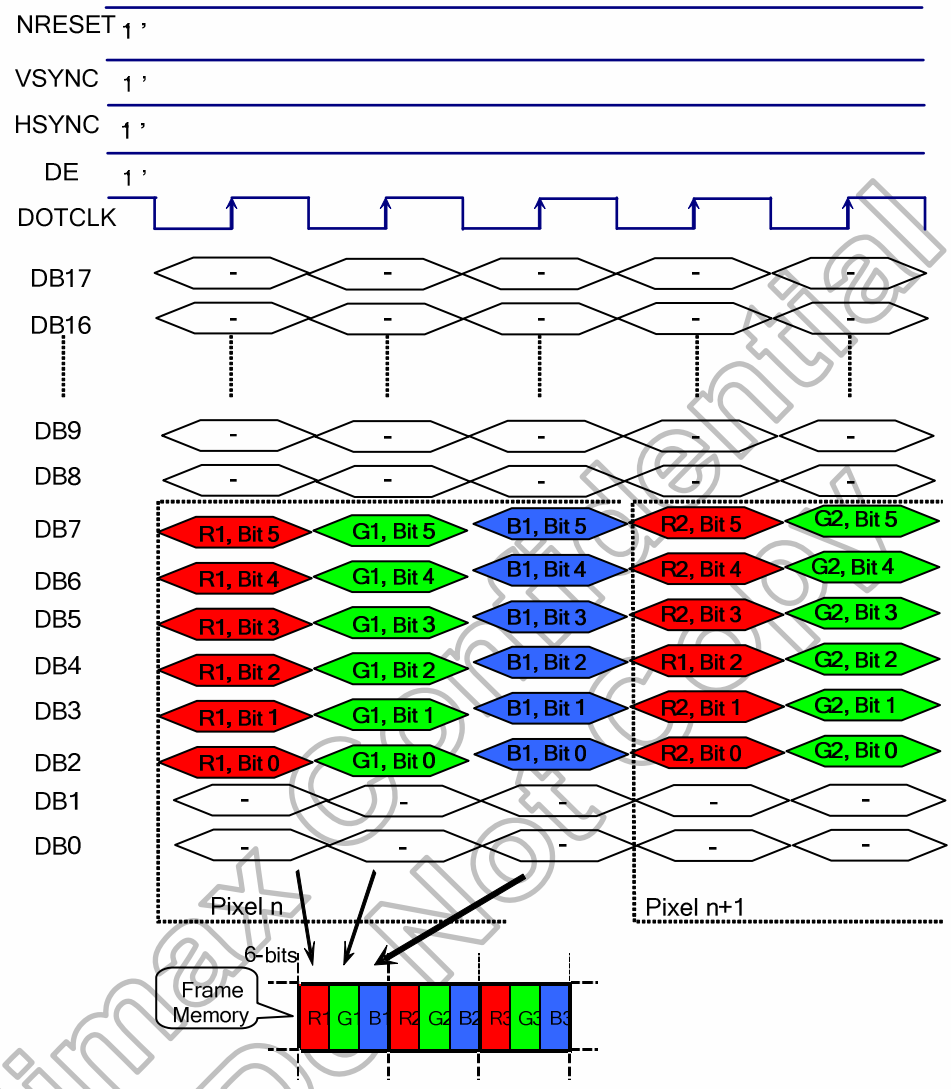
Pixel Color	R Component	G Component	B Component
Black	All bits are 0	All bits are 0	All bits are 0
Blue	All bits are 0	All bits are 0	All bits are 1
Green	All bits are 0	All bits are 1	All bits are 0
Cyan	All bits are 0	All bits are 1	All bits are 1
Red	All bits are 1	All bits are 0	All bits are 0
Magenta	All bits are 1	All bits are 0	All bits are 1
Yellow	All bits are 1	All bits are 1	All bits are 0
White	All bits are 1	All bits are 1	All bits are 1

Note: There are only defined main colors on this table - Not all gray levels of colors.

Table 5.21 Meaning of pixel information for main colors on RGB interface

5.2.2 RGB data color coding

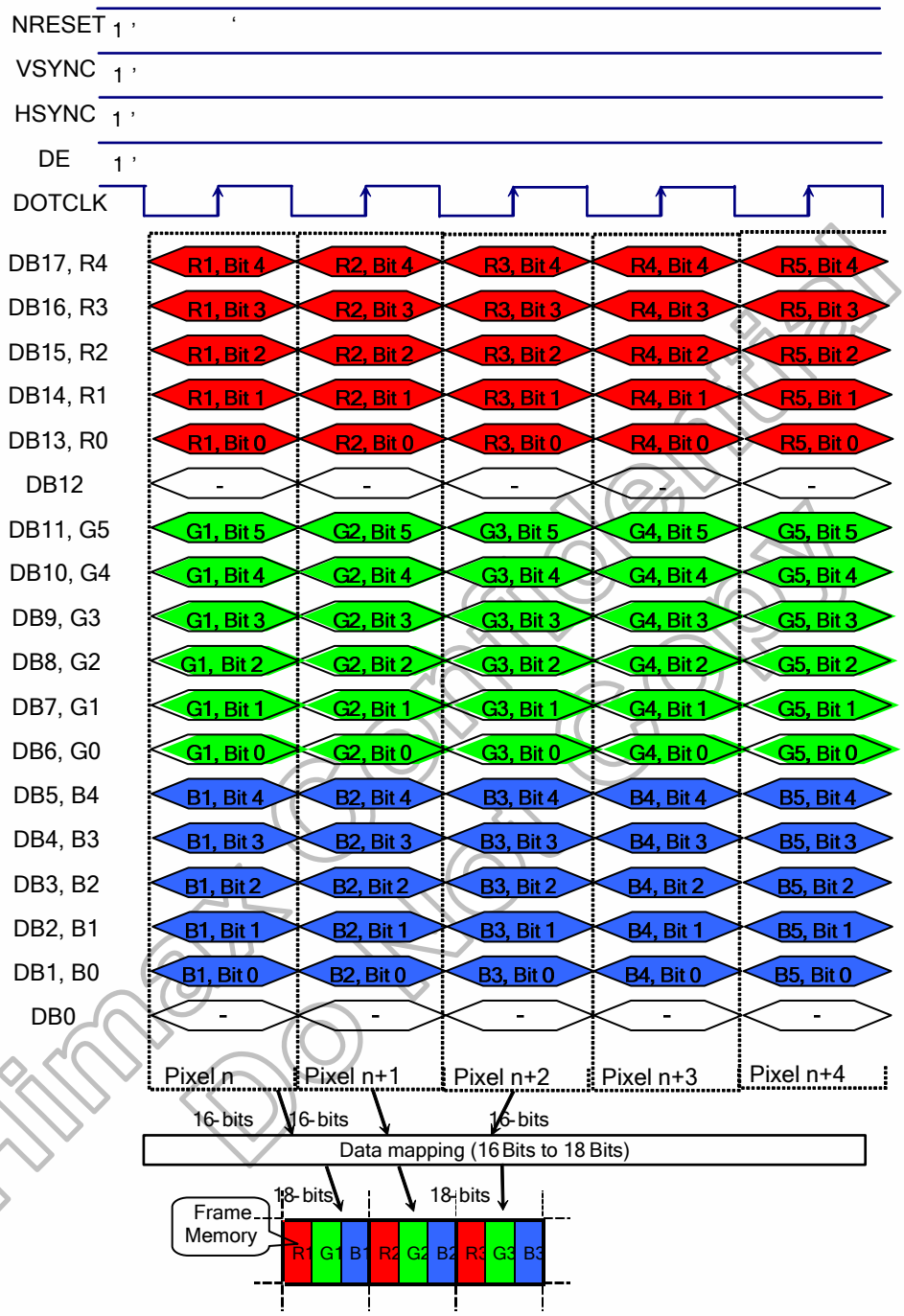
18-bit/pixel Colors Order on 6-bit Data width RGB Interface (RGB 6-6-6-bits input).
There are 1 pixel (3 sub-pixels) per 3 bytes, 262K-colors, 17H="E0h"



Note: (1) The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit7, LSB=Bit0 for Red, Green and Blue data. (3-trandfer data one pixel)
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5.38 RGB 18-bit/pixel on 6-bit Data width

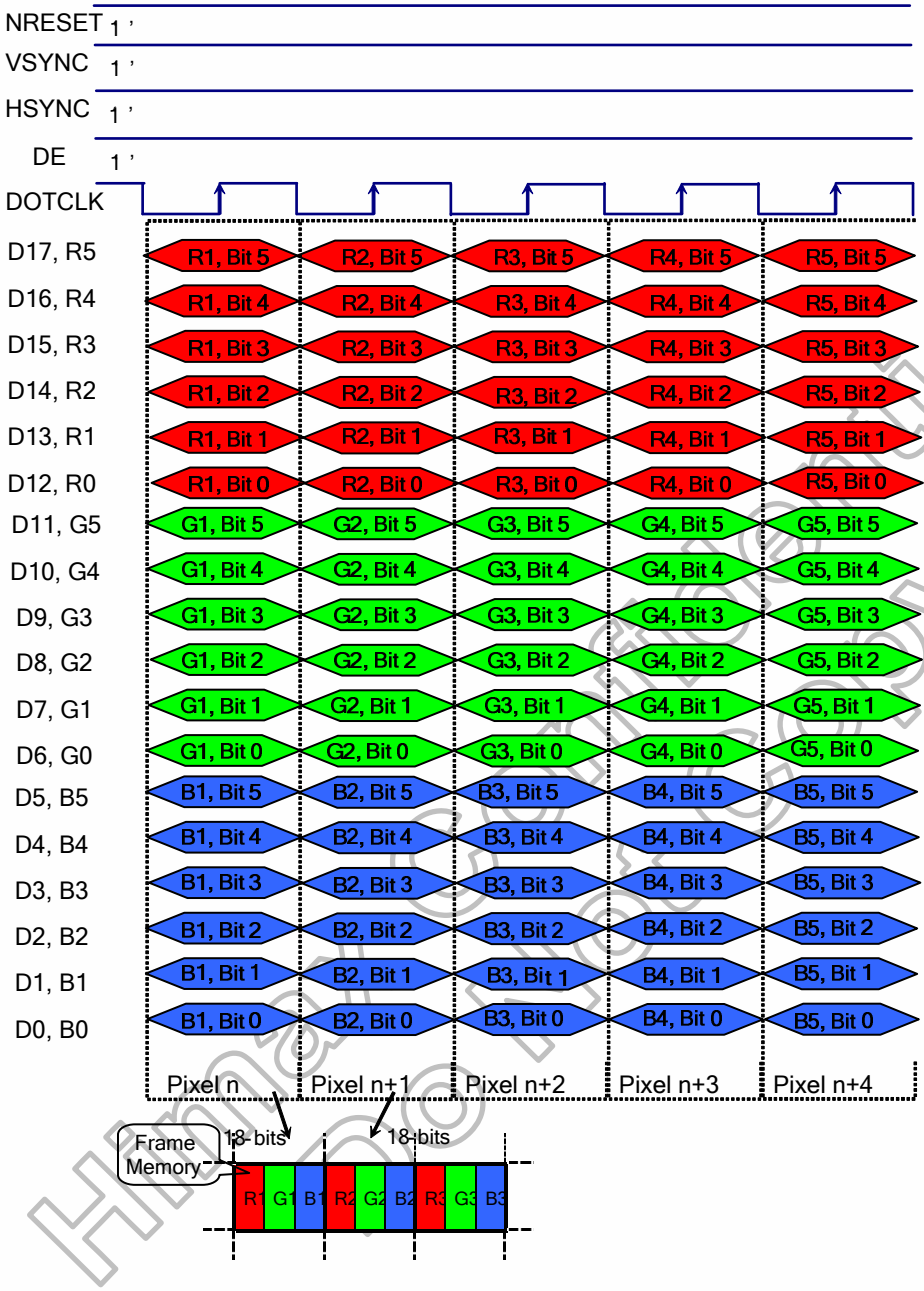
16-bits/pixel Colors Order on the 16-bits Data width RGB Interface (RGB 5-6-5-bits input). There are 1 pixel (3 sub-pixels) per 1 bytes, 65K-colors, 17H="50h"



Note: (1) The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5.39 RGB 16-bit/pixel on 16-bit data width

18-bit/pixel Colors Order on the 18-bit Data width RGB Interface (RGB 6-6-6-bit input). There are 1 pixel (3 sub-pixels) per 1 bytes, 262K-colors, 17H="60h"

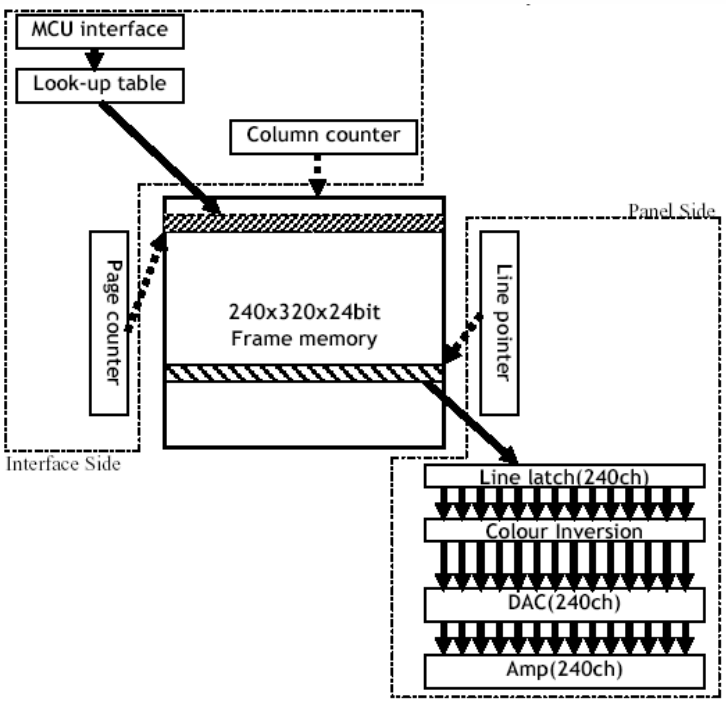


Note: (1) The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5.40 RGB 18-bit/pixel on 18-bit data width

6. Display Data GRAM

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



6.1 Display data GRAM mapping

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD command from start positions of the window address.

(00,00)H	(00,01)H	(00,02)H	---------	(00,EC)H	(00,ED)H	(00,EE)H	(00,EF)H
(01,00)H	(01,01)H	(01,02)H	---------	(01,EC)H	(01,ED)H	(01,EE)H	(01,EF)H
(02,00)H	(02,01)H	(02,02)H	---------	(02,EC)H	(02,ED)H	(02,EE)H	(02,EF)H
(03,00)H	(03,01)H	(03,02)H	---------	(03,EC)H	(03,ED)H	(03,EE)H	(03,EF)H
(04,00)H	(04,01)H	(04,02)H	---------	(04,EC)H	(04,ED)H	(04,EE)H	(04,EF)H
(05,00)H	(05,01)H	(05,02)H	---------	(05,EC)H	(05,ED)H	(05,EE)H	(05,EF)H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(13A,00)H	(13A,01)H	(13A,02)H	---------	(13A,EC)H	(13A,ED)H	(13A,EE)H	(13A,EF)H
(13B,00)H	(13B,01)H	(13B,02)H	---------	(13B,EC)H	(13B,ED)H	(13B,EE)H	(13B,EF)H
(13C,00)H	(13C,01)H	(13C,02)H	---------	(13C,EC)H	(13C,ED)H	(13C,EE)H	(13C,EF)H
(13D,00)H	(13D,01)H	(13D,02)H	---------	(13D,EC)H	(13DED)H	(13D17E)H	(13D,EF)H
(13E,00)H	(13E,01)H	(13E,02)H	---------	(13E,EC)H	(13E,ED)H	(13E,EE)H	(13E,EF)H
(13F,00)H	(13F,01)H	(13F,02)H	---------	(13F,EC)H	(13F,ED)H	(13F,EE)H	(13F,EF)H

Table 6.1 GRAM address for display panel position

6.2 Address counter (AC) of GRAM

The HX8367-A contains an address counter (AC) which assigns address for writing/reading pixel data to GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

6.2.1 System interface to GRAM write direction

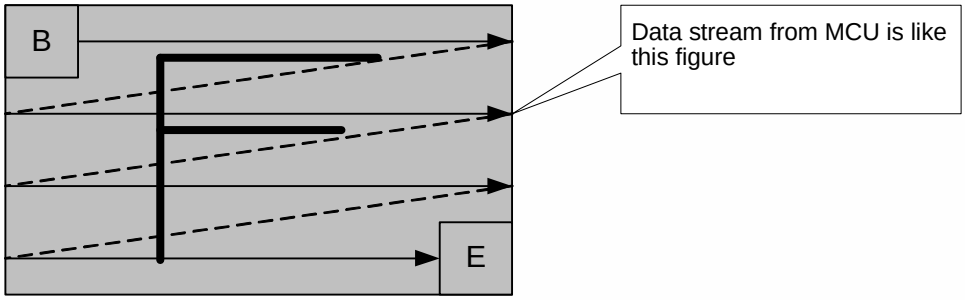


Figure 6.1 Image data sending order from host

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting

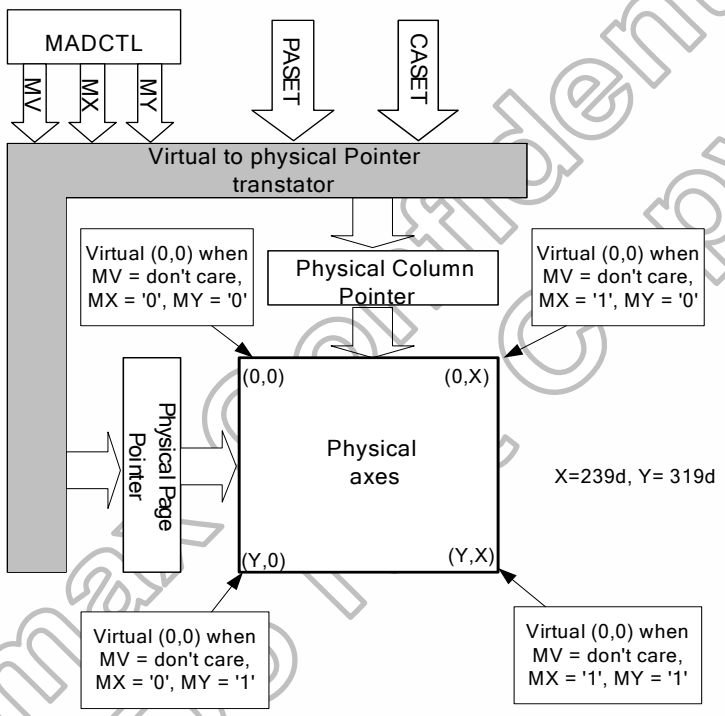


Figure 6.2 Image data writing control

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (Y - Physical Page Pointer)
0	1	0	Direct to (X-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (X - Physical Column Pointer)	Direct to (Y - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (Y - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (X-Physical Column Pointer)
1	1	1	Direct to (Y - Physical Page Pointer)	Direct to (X - Physical Column Pointer)

Table 6.2 CASET and PASET control for physical column/page pointers

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start Column"	Return to "Start Page"

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MX, MY, MV.

Table 6.3 Rules for updating GRAM order

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

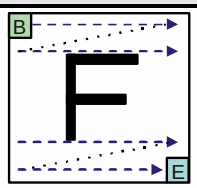
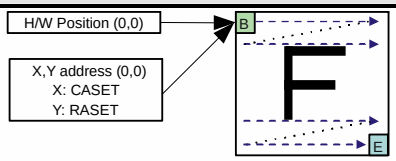
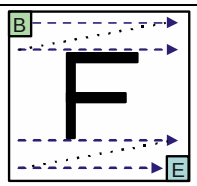
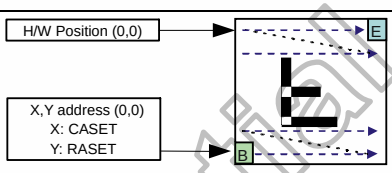
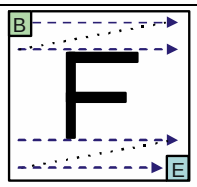
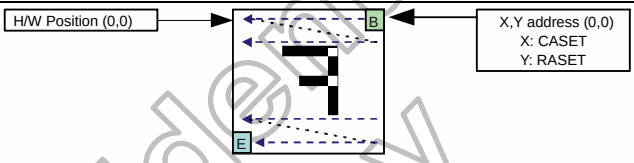
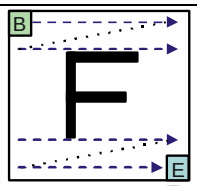
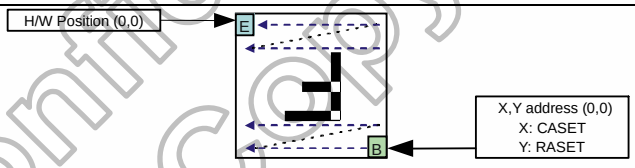
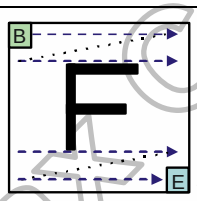
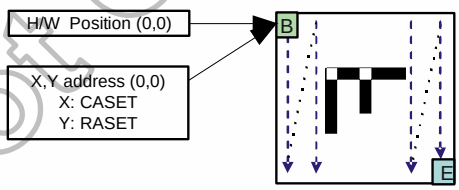
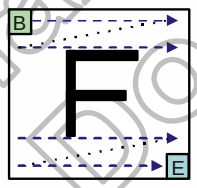
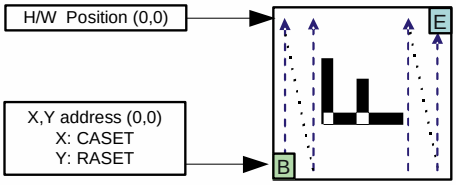
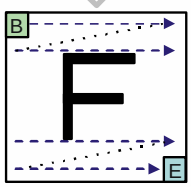
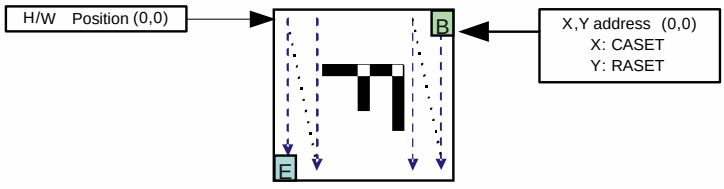
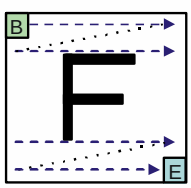
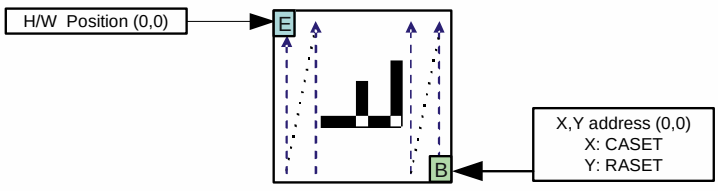
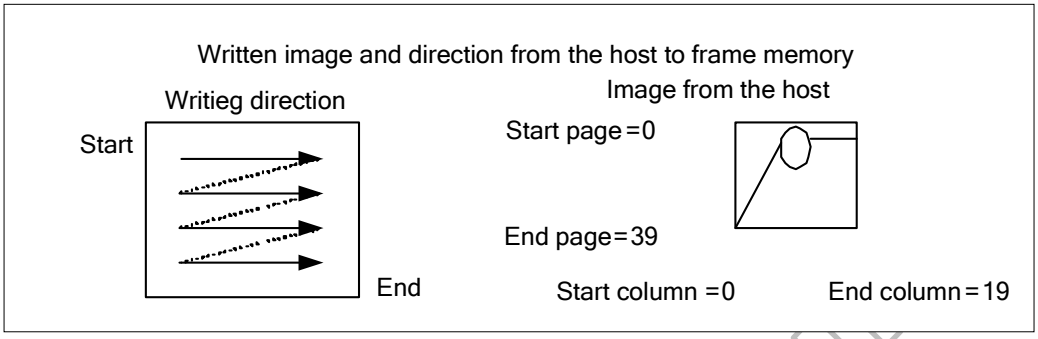
Display Data Direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange X-invert	1	0	1		
X-Y Exchange Y-invert	1	1	0		
X-Y Exchange X-invert Y-invert	1	1	1		

Table 6.4 Address direction settings

Example for rotation with MY, MX and MV

This example is using following values: start page = 0, end page = 39, start column = 0 and end column = 19 => commands: page address set (0, 39) and column address set (0, 19). The sent figure is as follows and its sending order is as follows.



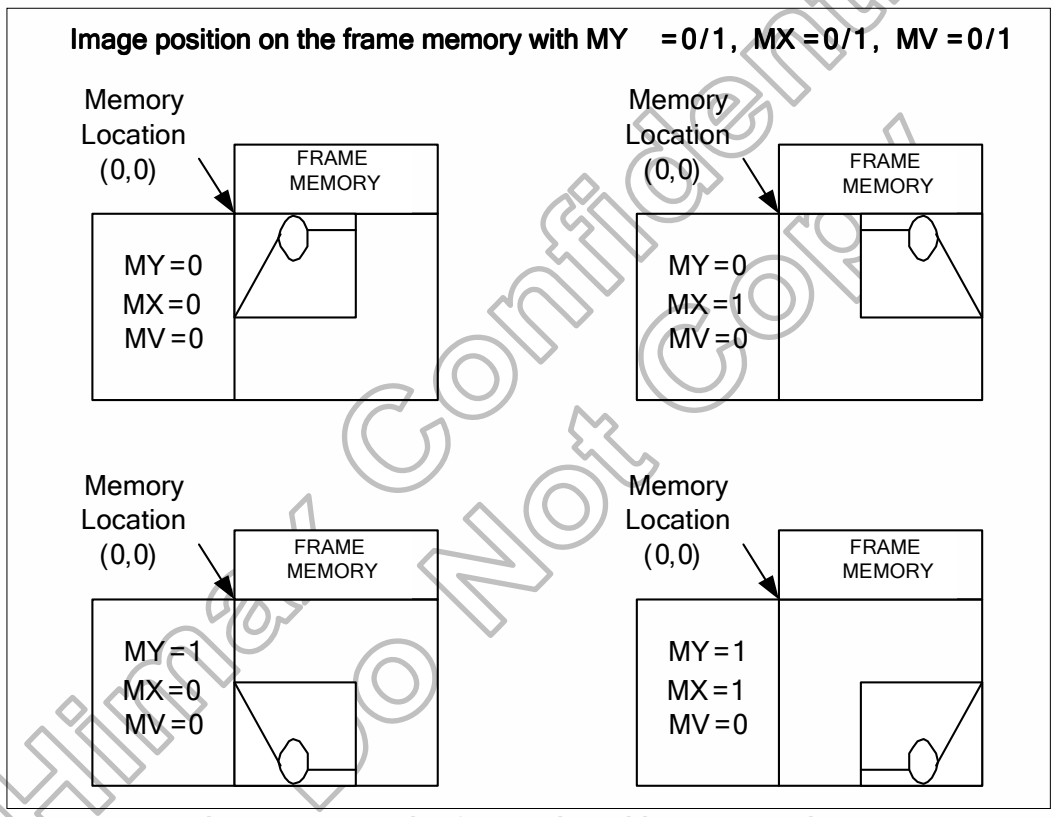


Figure 6.3 Example1 for rotation with MY, MX and MV

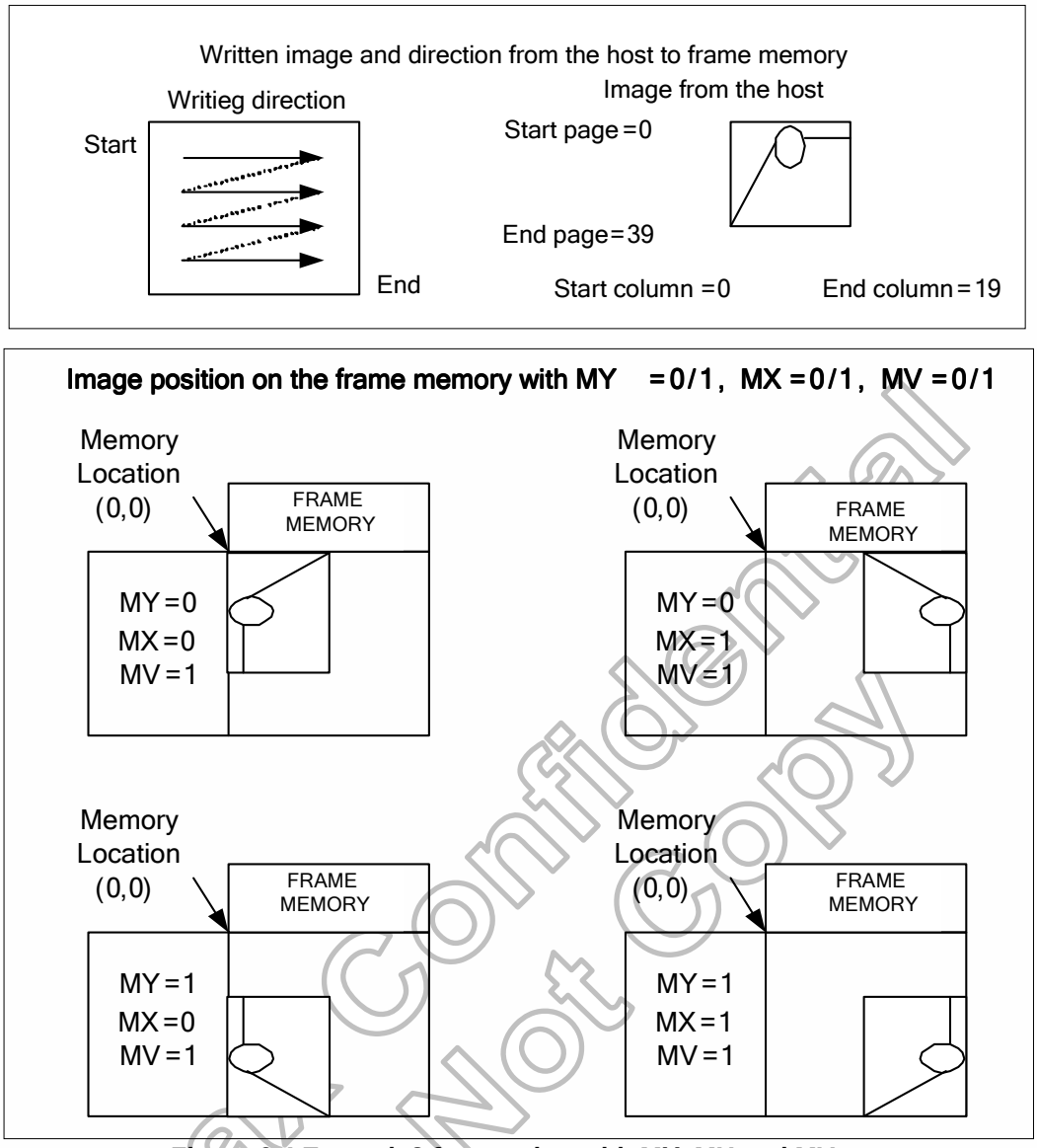


Figure 6.4 Example2 for rotation with MY, MX and MV

6.3 GRAM to display address mapping

By setting the **SS** bit, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** bit, the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR** bit, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement. Table 6.5, Table 6.6 and Table 6.7 show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

BGR = 0														
Source	**SS = 0**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**-------**	**S715**	**S716**	**S717**	**S718**	**S719**	**S720**
Output	**SS= 1**	**S718**	**S719**	**S720**	**S715**	**S716**	**S717**	**-------**	**S4**	**S5**	**S6**	**S1**	**S2**	**S3**
X Address		“00”h			“01”h			-------	“EE”h			“EF”h		
RGB data		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

BGR = 1														
Source	**SS = 0**	**S3**	**S2**	**S1**	**S6**	**S5**	**S4**	**-------**	**S717**	**S716**	**S715**	**S720**	**S719**	**S718**
Output	**SS= 1**	**S720**	**S719**	**S718**	**S717**	**S716**	**S715**	**-------**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**
X Address		“00”h			“01”h			-------	“EE”h			“EF”h		
Bit Allocation		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

Table 6.5 GRAM X address and display panel position

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
G1	0000h			0001h			0002h			---	00ECh			00EDh			00EEh			00EFh		
G2	0100h			0101h			0102h			---	01ECh			01EDh			01EEh			01EFh		
G3	0200h			0201h			0202h			---	02ECh			02EDh			02EEh			02EFh		
G4	0300h			0301h			0302h			---	03ECh			03EDh			03EEh			03EFh		
G5	0400h			0401h			0402h			---	04ECh			04EDh			04EEh			04EFh		
G6	0500h			0501h			0502h			---	05ECh			05EDh			05EEh			05EFh		
G7	0600h			0601h			0602h			---	06ECh			06EDh			06EEh			06EFh		
G8	0700h			0701h			0702h			---	07ECh			07EDh			07EEh			07EFh		
G9	0800h			0801h			0802h			---	08ECh			08EDh			08EEh			08EFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G311	13600h			13601h			13602h			---	136ECh			136EDh			136EEh			136EFh		
G312	13700h			13701h			13702h			---	137ECh			137EDh			137EEh			137EFh		
G313	13800h			13801h			13802h			---	138ECh			138EDh			138EEh			138EFh		
G314	13900h			13901h			13902h			---	139ECh			139EDh			139EEh			139EFh		
G315	13A00h			13A01h			13A02h			---	13AECh			13AEDh			13AEEh			13AEFh		
G316	13B00h			13B01h			13B02h			---	13BECh			13BEDh			13BEEh			13BEFh		
G317	13C00h			13C01h			13C02h			---	13CECh			13CEDh			13CEEh			13CEFh		
G318	13D00h			13D01h			13D02h			---	13DECh			13DEDh			13DEEh			13DEFh		
G319	13E00h			13E01h			13E02h			---	13EECh			13EEDh			13EEEh			13EEFh		
G320	13F00h			13F01h			13F02h			---	13FECh			13FEDh			13FEEh			13FEFh		

Table 6.6 GRAM address and display panel position (GS =’0’)

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
G320	0000h			0001h			0002h			---	00ECh			00EDh			00EEh			00EFh		
G319	0100h			0101h			0102h			---	01ECh			01EDh			01EEh			01EFh		
G318	0200h			0201h			0202h			---	02ECh			02EDh			02EEh			02EFh		
G317	0300h			0301h			0302h			---	03ECh			03EDh			03EEh			03EFh		
G316	0400h			0401h			0402h			---	04ECh			04EDh			04EEh			04EFh		
G315	0500h			0501h			0502h			---	05ECh			05EDh			05EEh			05EFh		
G314	0600h			0601h			0602h			---	06ECh			06EDh			06EEh			06EFh		
G313	0700h			0701h			0702h			---	07ECh			07EDh			07EEh			07EFh		
G312	0800h			0801h			0802h			---	08ECh			08EDh			08EEh			08EFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G10	13600h			13601h			13602h			---	136ECh			136EDh			136EEh			136EFh		
G9	13700h			13701h			13702h			---	137ECh			137EDh			137EEh			137EFh		
G8	13800h			13801h			13802h			---	138ECh			138EDh			138EEh			138EFh		
G7	13900h			13901h			13902h			---	139ECh			139EDh			139EEh			139EFh		
G6	13A00h			13A01h			13A02h			---	13AECh			13AEDh			13AEEh			13AEFh		
G5	13B00h			13B01h			13B02h			---	13BECh			13BEDh			13BEEh			13BEFh		
G4	13C00h			13C01h			13C02h			---	13CECh			13CEDh			13CEEh			13CEFh		
G3	13D00h			13D01h			13D02h			---	13DECh			13DEDh			13DEEh			13DEFh		
G2	13E00h			13E01h			13E02h			---	13EECh			13EEDh			13EEEh			13EEFh		
G1	13F00h			13F01h			13F02h			---	13FECh			13FEDh			13FEEh			13FEFh		

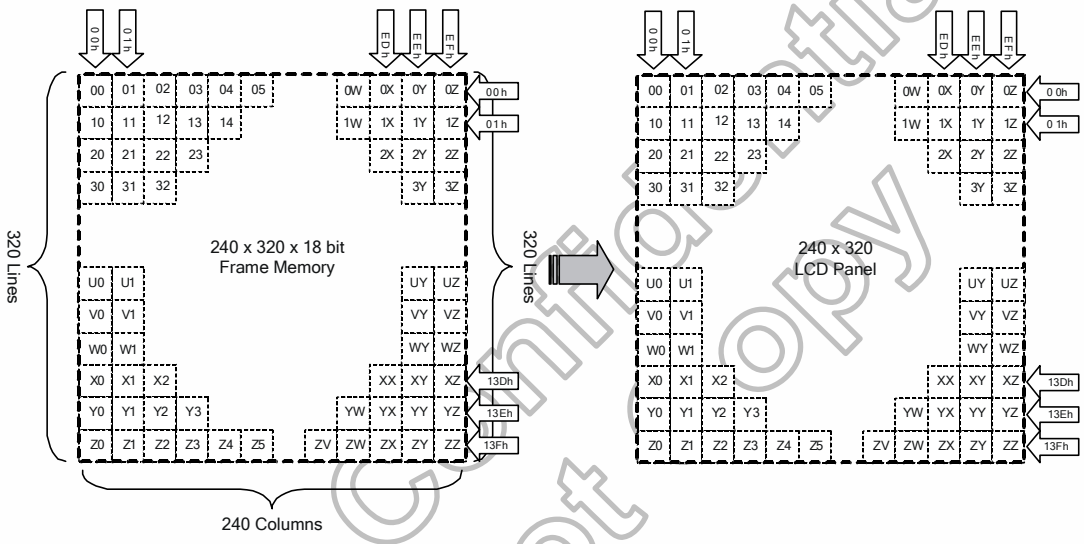
Table 6.7 GRAM address and display panel position (GS =’1’)

The HX8367-A supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

When the **PLTON** = '0' is set, HX8367-A will be into Normal Display Mode. When the **PLTON** = '1' is set, HX8367-A will be into Partial Display Mode. When the **SCROLL_ON** = '1' is set, HX8367-A will be into Scrolling Display Mode.

6.3.1 Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0) (**SS**='0',**GS**='0').



Example:

(1) **PLTON** = '1',

(2) PSL [15:0] =11_{DEC}, PEL [15:0] =130_{DEC}, ML=0, (**GS = 0**).

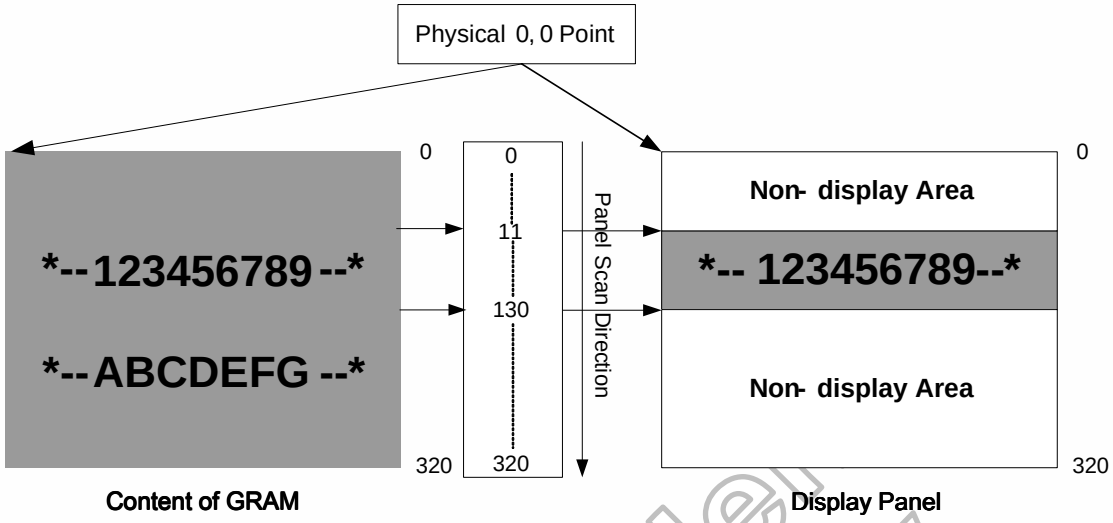


Figure 6.5 Partial display when ML= '0'

Example:

(1) **PLTON** = '1',

(2) PSL [15:0] =11_{DEC}, PEL [15:0] =130_{DEC}, ML=1, (**GS = 0**).

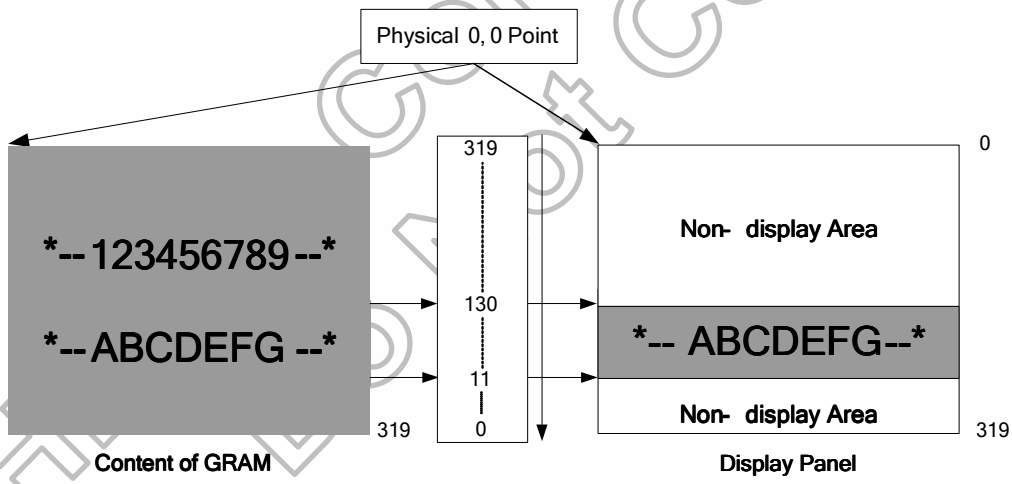


Figure 6.6 Partial display when ML= '1'

6.3.2 Vertical scroll display mode

When **SCROLL_ON** bit is set to '1', the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA, BFA** bits (R0Eh ~R13h) and **VSP** bits (R14~R15h).

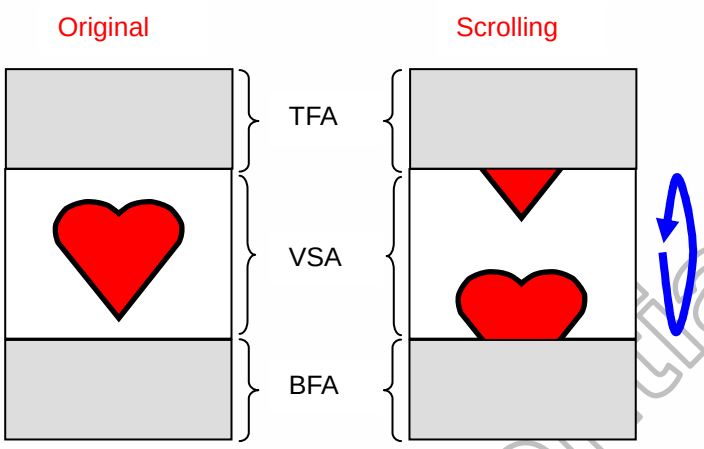


Figure 6.7 Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =320. In this case, scrolling is applied as shown below.

Example (1) TFA='2d', VSA='318d', BFA='0d', VSP='3d' (**SS**='0', **GS**='0')

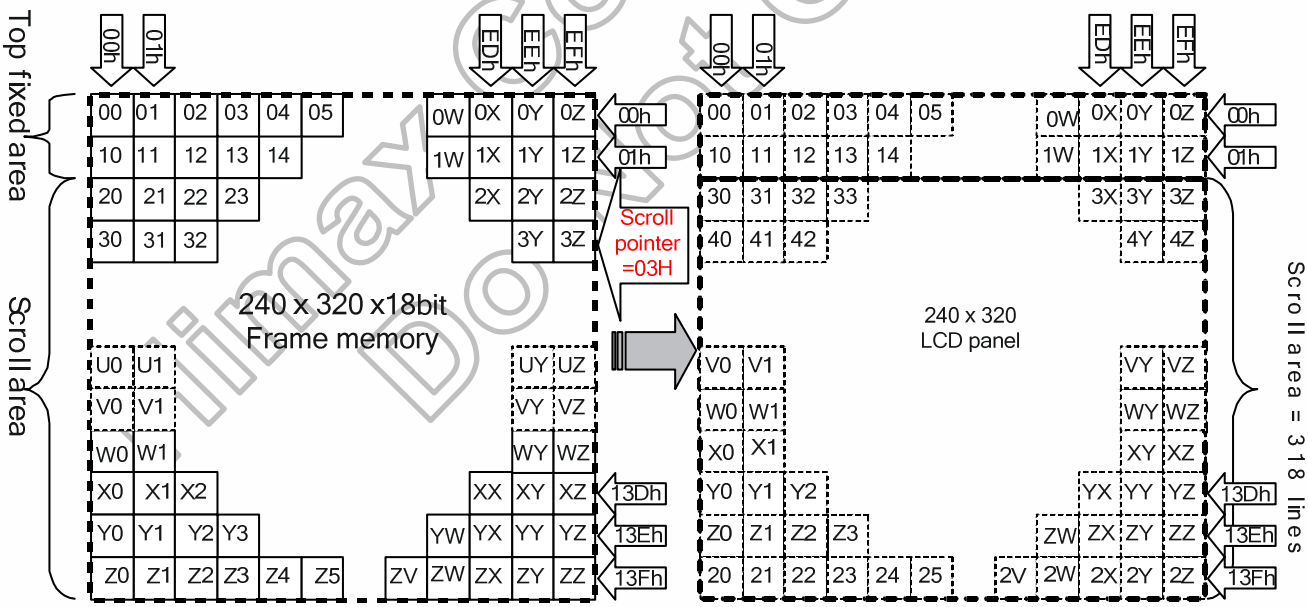


Figure 6.8 Memory map of vertical scrolling 1

Example (2) TFA=’2d’, VSA=’316d’, BFA=’2d’, VSP=’3d’ (**SS**=’0’, **GS**=’0’)

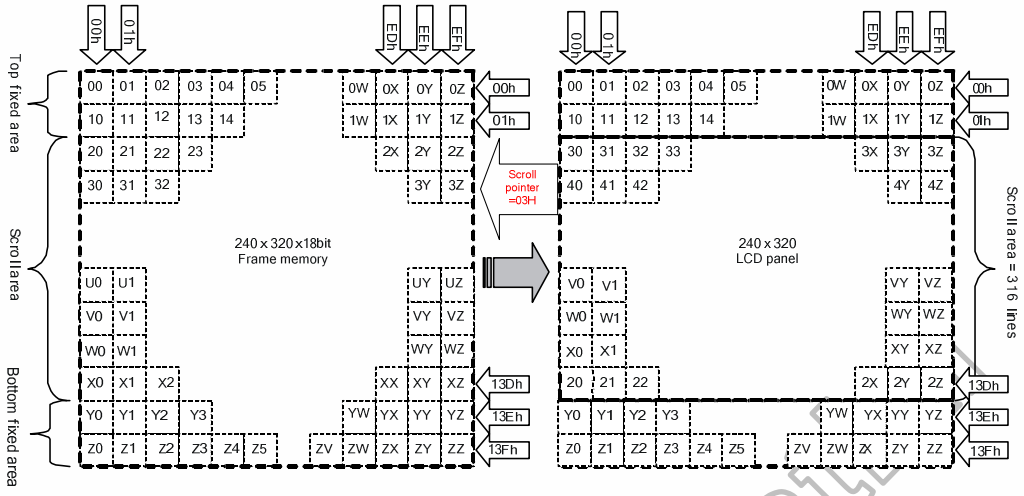


Figure 6.9 Memory map of vertical scrolling 2

Example (3) TFA=’2d’, VSA=’316d’, BFA=’2d’, VSP=’5d’ (**SS**=’0’, **GS**=’0’).

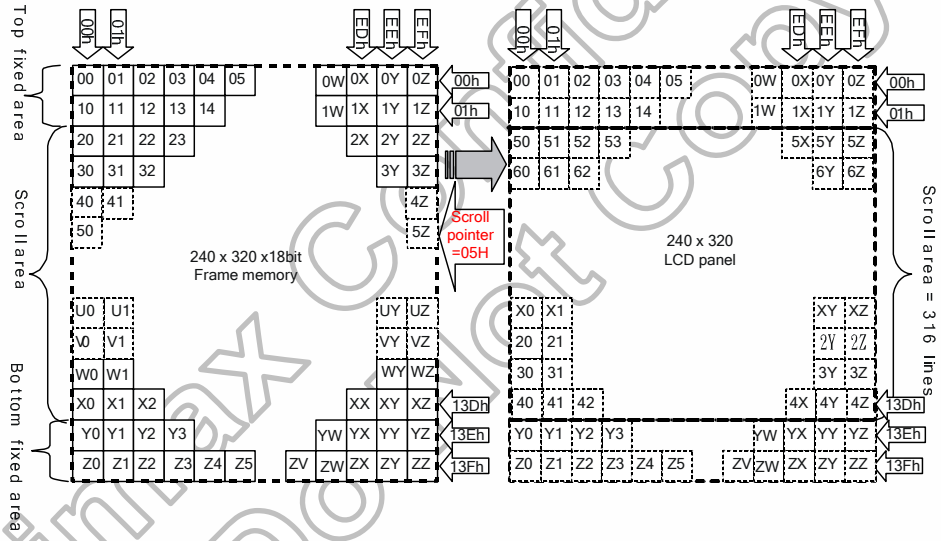


Figure 6.10 Memory map of vertical scrolling 3

Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits (R0Eh ~R13h) and **VSP** bits (R14~R15h).

Case 1: TFA + VSA + BFA ≠ '320d'
N/A. Do not set TFA + VSA + BFA ≠ '320d'. In that case, unexpected picture will be shown.
Case 2: TFA + VSA + BFA = '320d' (Scrolling)
Example (1) When TFA='0d', VSA='320d', BFA='0d' and VSP='40d' (**SS**='0', **GS**='0')

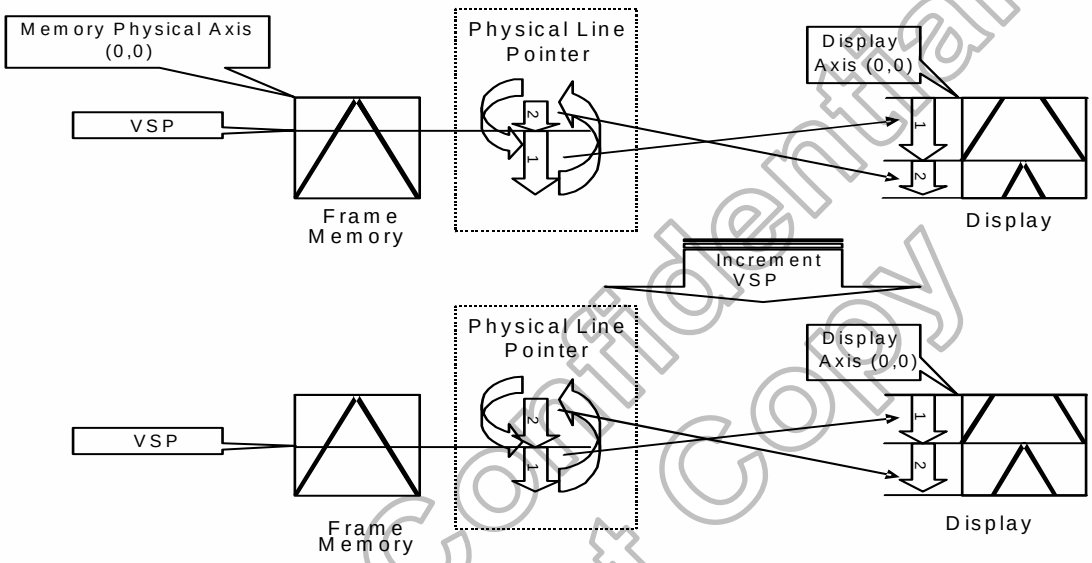


Figure 6.11 Vertical scrolling example

6.3.3 Updating order on display active area in RGB interface mode

There is defined different kind of updating orders for display in RGB interface mode (**RCM [1:0]** =’1x’). These updating are controlled by **MY** and **MX** bits.

Data streaming direction from the host to the display is described in the following figure.

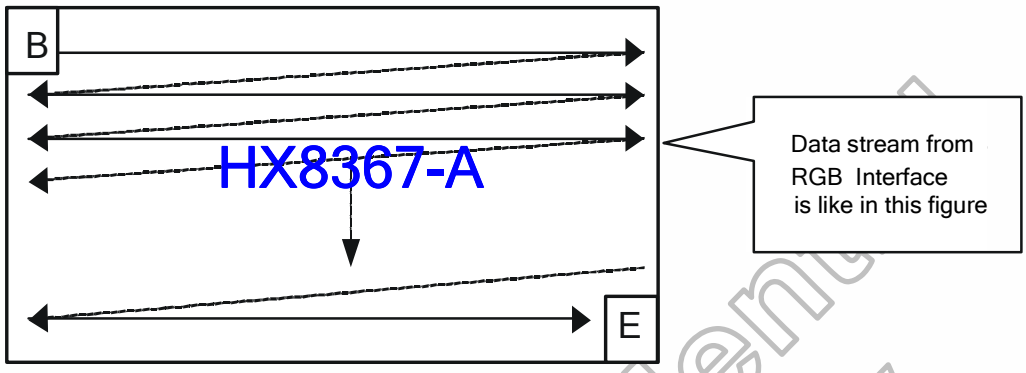


Figure 6.12 Data streaming order in RGB I/F

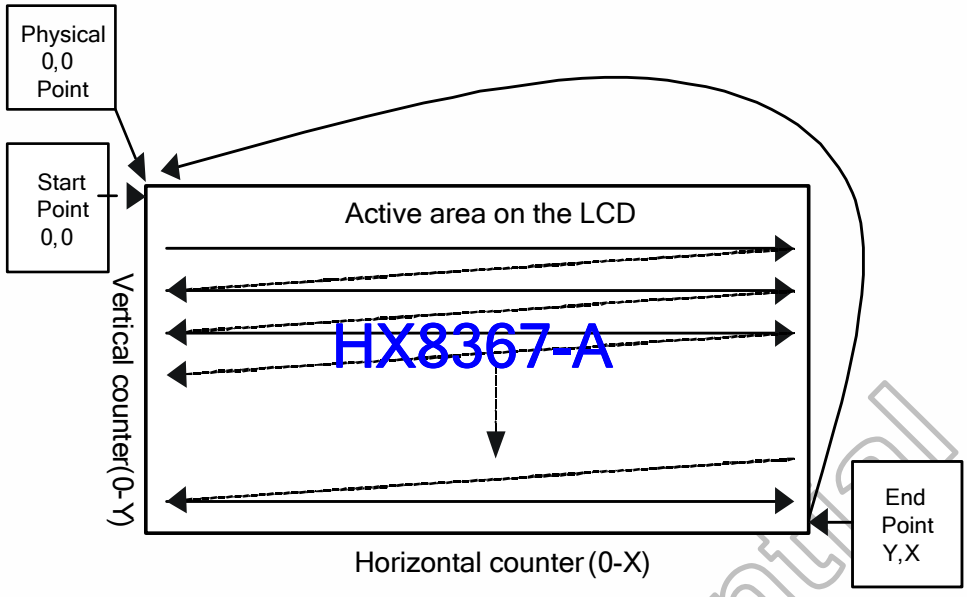


Figure 6.13 Updating order when MY = '0' and MX = '0'

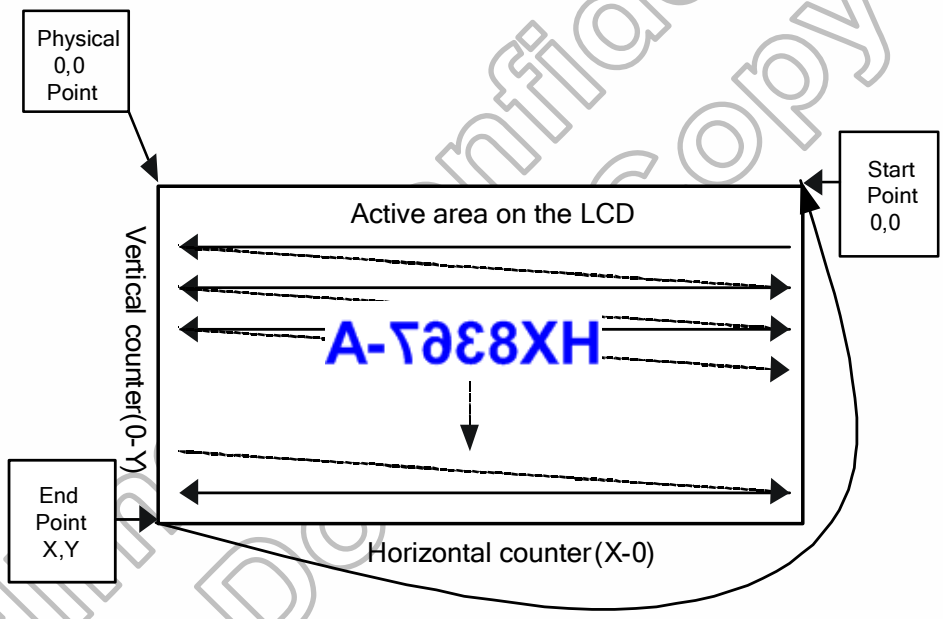


Figure 6.14 Updating order when MY = '0' and MX = '1'

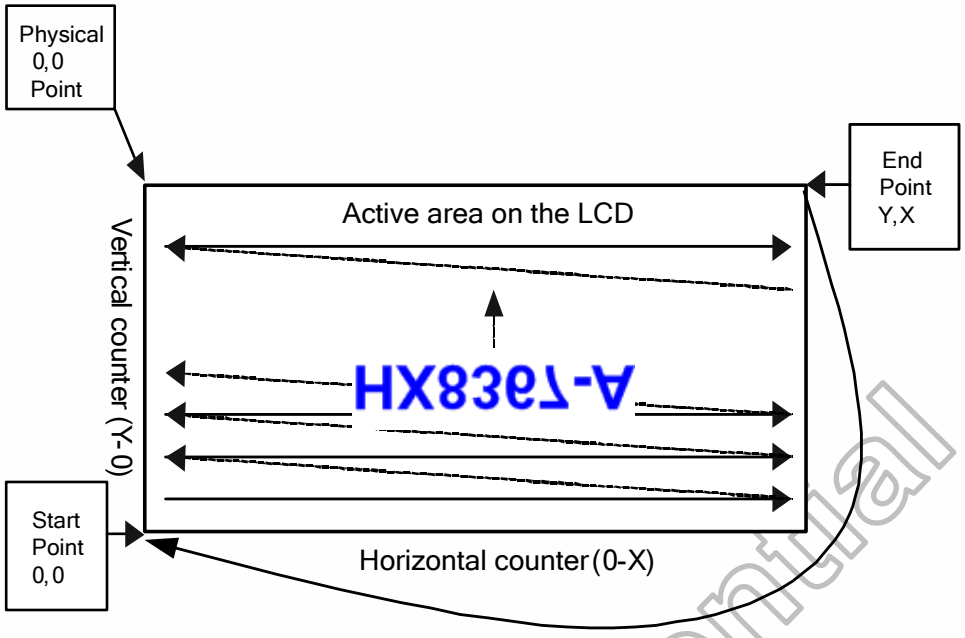


Figure 6.15 Updating order when MY = '1' and MX = '0'

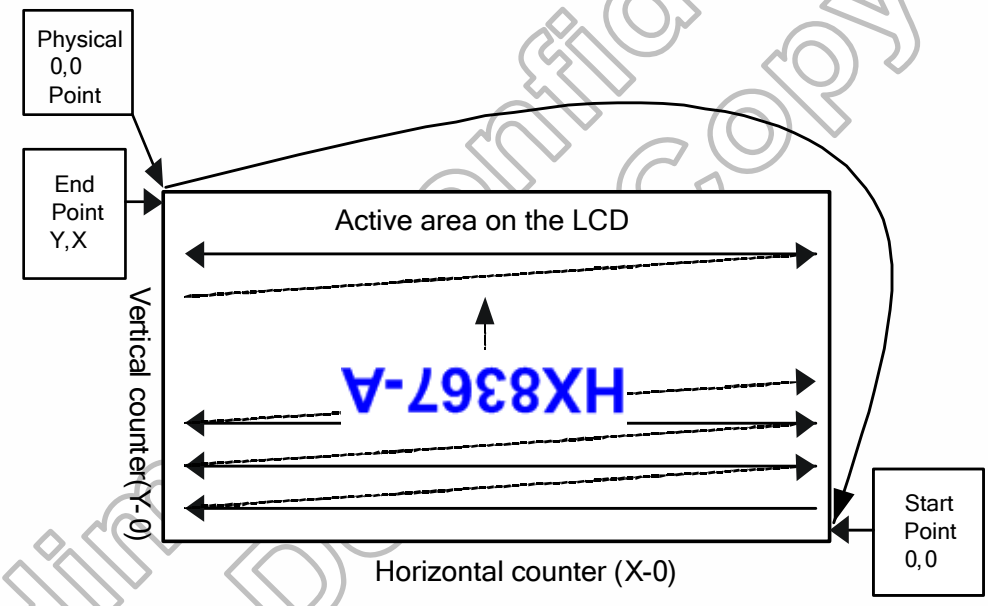


Figure 6.16 Updating order when MY = '1' and MX = '1'

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to "Start Column"	Return to "Start Page"

Note: Pixel order is RGB on the display.

Table 6.8 Rules for updating order on display active area in RGB interface display mode

7. Functional Description

7.1 Internal oscillator

The HX8367-A can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±5%, **RADJ [3:0]** bits for initial 2.63MHz internal clock generation. With other dividers setting, the 2.63MHz internal clock can be used to generate clock for other part of the chip using.

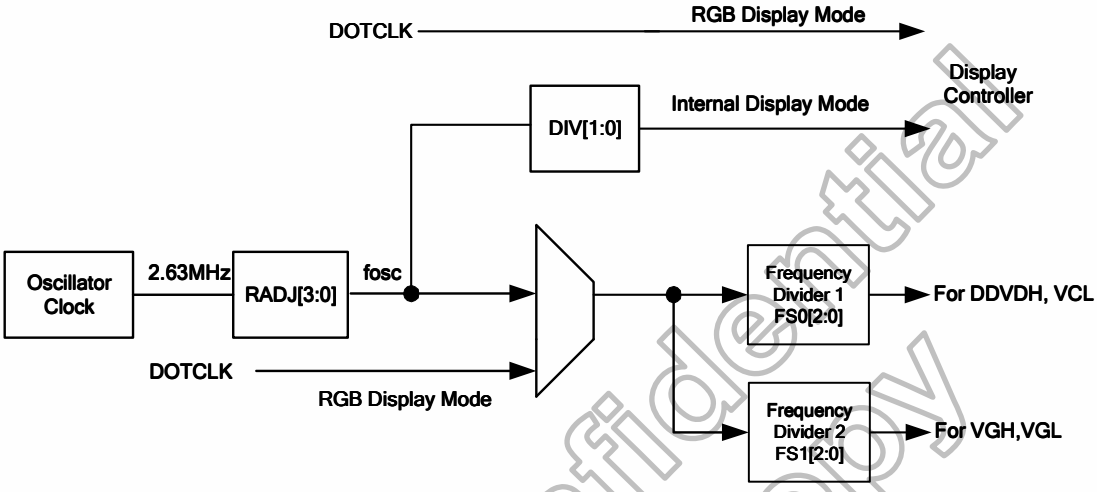
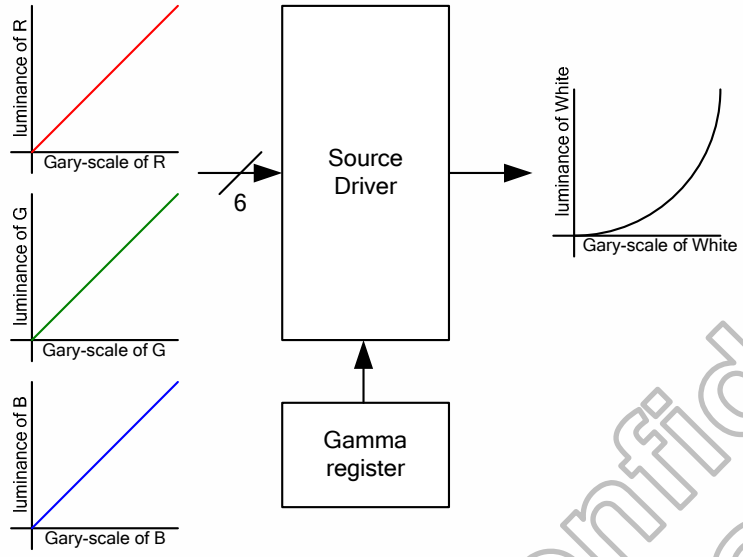


Figure 7.1 HX8367-A internal clock circuit

7.2 Gamma characteristic correction function

The HX8367-A offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction

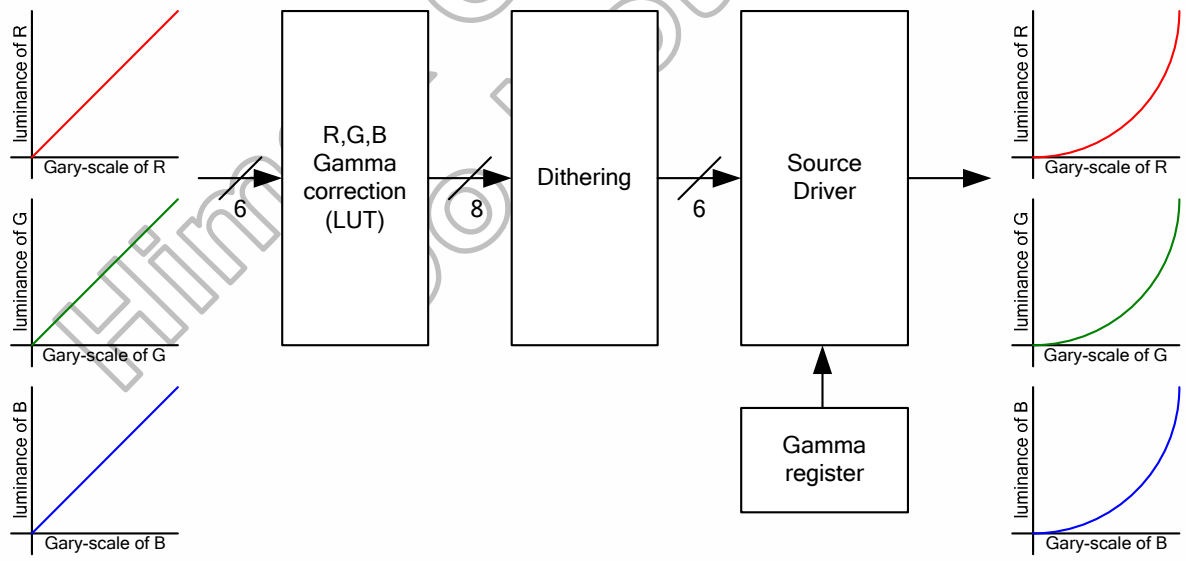


Figure 7.2 Gamma adjustments different of source driver with digital gamma correction

The HX8367-A offers Gamma adjustment ways to come to accord with LC characteristic through Source Driver directly.

7.2.1 Gray voltage generator for source driver

The HX8367-A incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

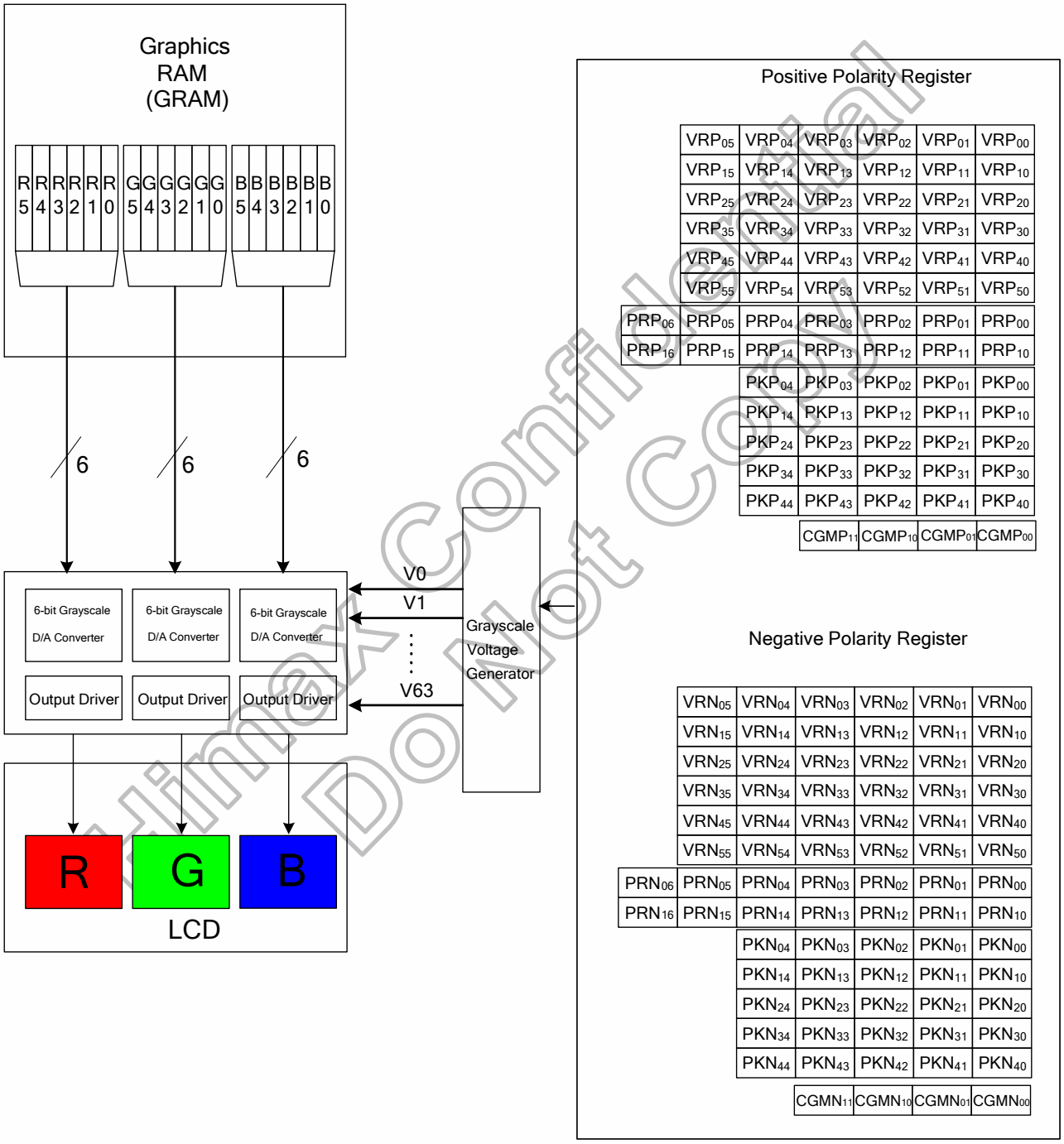


Figure 7.3 Grayscale control

Gamma-characteristics adjustment register

This HX8367-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. his function is implemented by choosing one input of 64-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

Gamma macro adjustment registers

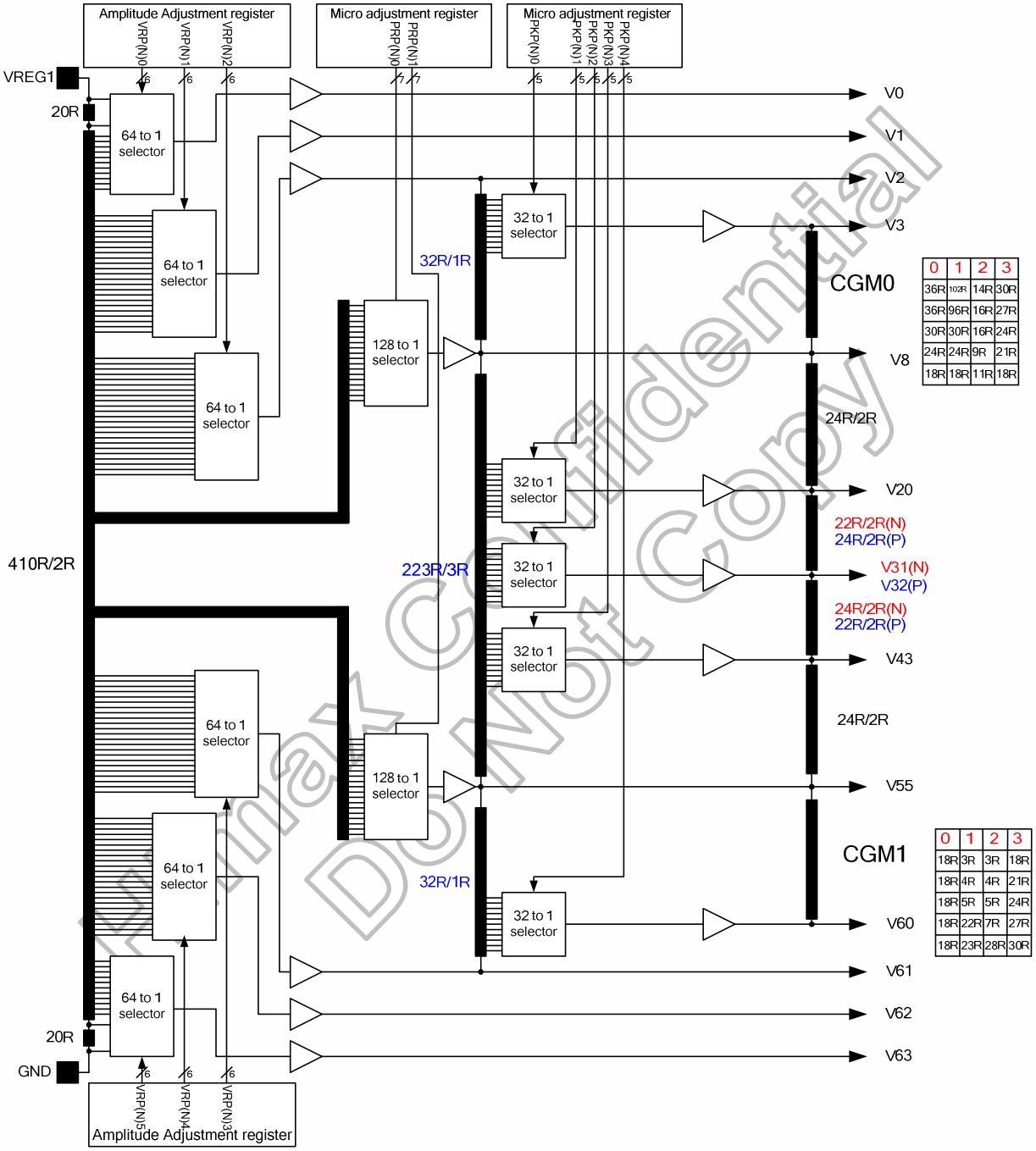
The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (Vg(P/N) 3, 20, 32(31), 43, 60).

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	128-to-1 selector (voltage level of grayscale 8)
	PRP1 6-0	PRN1 6-0	128-to-1 selector (voltage level of grayscale 55)
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 20)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 43)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	VRP0 5-0	VRN0 5-0	64-to-1 selector (voltage level of grayscale 0)
	VRP1 5-0	VRN1 5-0	64-to-1 selector (voltage level of grayscale 1)
	VRP2 5-0	VRN2 5-0	64-to-1 selector (voltage level of grayscale 2)
	VRP3 5-0	VRN3 5-0	64-to-1 selector (voltage level of grayscale 61)
	VRP4 5-0	VRN4 5-0	64-to-1 selector (voltage level of grayscale 62)
	VRP5 5-0	VRN5 5-0	64-to-1 selector (voltage level of grayscale 63)

Table 7.1 Gamma-adjustment registers

Gamma resister stream

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. VgP/N (0, 1, 2, 3, 8 20, 32(31), 43, 55, 60, 61, 62, 63).



0	1	2	3
36R	102R	14R	30R
36R	96R	16R	27R
30R	30R	16R	24R
24R	24R	9R	21R
18R	18R	11R	18R

0	1	2	3
18R	3R	3R	18R
18R	4R	4R	21R
18R	5R	5R	24R
18R	22R	7R	27R
18R	23R	28R	30R

Figure 7.4 Gamma resister stream and gamma reference voltage

Variable Resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0
000000	0R
000001	20R
000010	22R
000011	24R
• •	• •
011101	76R
011110	78R
011111	80R
100000	84R
100001	88R
100010	92R
• •	• •
111101	200R
111110	204R
111111	208R

Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1
000000	0R
000001	2R
000010	4R
000011	6R
• •	• •
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
• •	• •
111101	182R
111110	186R
111111	190R

Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
000011	6R
• •	• •
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
• •	• •
111101	182R
111110	186R
111111	190R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3
000000	0R
000001	4R
000010	8R
• •	• •
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
• •	• •
111100	184R
111101	186R
111110	188R
111111	190R

Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4
000000	0R
000001	4R
000010	8R
• •	• •
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
• •	• •
111100	184R
111101	186R
111110	188R
111111	190R

Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R
000001	4R
000010	8R
• •	• •
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
• •	• •
111100	184R
111101	186R
111110	188R
111111	208R

Table 7.2 Offset adjustment 0 ~ 5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0
0000000	0R
0000001	2R
0000010	4R
• •	• •
1111101	250R
1111110	252R
1111111	254R

Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R
0000001	2R
0000010	4R
• •	• •
1010101	250R
1111110	252R
1111111	254R

Table 7.3 Center adjustment

The grayscale levels are determined by the following formulas:

Reference Voltage	Macro Adjustment Value	VinP/N0 Formula
VinP/N0	VRP/N0 5-0 = 000000	VREG1
	VRP/N0 5-0 = 000001	((450R - 20R) / 450R) * VREG1
	VRP/N0 5-0 = 000010	((450R - 22R) / 450R) * VREG1
	VRP/N0 5-0 = 000011	((450R - 24R) / 450R) * VREG1
	VRP/N0 5-0 = 000100	((450R - 26R) / 450R) * VREG1
	VRP/N0 5-0 = 000101	((450R - 28R) / 450R) * VREG1
	VRP/N0 5-0 = 000110	((450R - 30R) / 450R) * VREG1
	VRP/N0 5-0 = 000111	((450R - 32R) / 450R) * VREG1
	VRP/N0 5-0 = 001000	((450R - 34R) / 450R) * VREG1
	VRP/N0 5-0 = 001001	((450R - 36R) / 450R) * VREG1
	VRP/N0 5-0 = 001010	((450R - 38R) / 450R) * VREG1
	VRP/N0 5-0 = 001011	((450R - 40R) / 450R) * VREG1
	VRP/N0 5-0 = 001100	((450R - 42R) / 450R) * VREG1
	VRP/N0 5-0 = 001101	((450R - 44R) / 450R) * VREG1
	VRP/N0 5-0 = 001110	((450R - 46R) / 450R) * VREG1
	VRP/N0 5-0 = 001111	((450R - 48R) / 450R) * VREG1
	VRP/N0 5-0 = 010000	((450R - 50R) / 450R) * VREG1
	VRP/N0 5-0 = 010001	((450R - 52R) / 450R) * VREG1
	VRP/N0 5-0 = 010010	((450R - 54R) / 450R) * VREG1
	VRP/N0 5-0 = 010011	((450R - 56R) / 450R) * VREG1
	VRP/N0 5-0 = 010100	((450R - 58R) / 450R) * VREG1
	VRP/N0 5-0 = 010101	((450R - 60R) / 450R) * VREG1
	VRP/N0 5-0 = 010110	((450R - 62R) / 450R) * VREG1
	VRP/N0 5-0 = 010111	((450R - 64R) / 450R) * VREG1
	VRP/N0 5-0 = 011000	((450R - 66R) / 450R) * VREG1
	VRP/N0 5-0 = 011001	((450R - 68R) / 450R) * VREG1
	VRP/N0 5-0 = 011010	((450R - 70R) / 450R) * VREG1
	VRP/N0 5-0 = 011011	((450R - 72R) / 450R) * VREG1
	VRP/N0 5-0 = 011100	((450R - 74R) / 450R) * VREG1
	VRP/N0 5-0 = 011101	((450R - 76R) / 450R) * VREG1
	VRP/N0 5-0 = 011110	((450R - 78R) / 450R) * VREG1
	VRP/N0 5-0 = 011111	((450R - 80R) / 450R) * VREG1
	VRP/N0 5-0 = 100000	((450R - 84R) / 450R) * VREG1
	VRP/N0 5-0 = 100001	((450R - 88R) / 450R) * VREG1
	VRP/N0 5-0 = 100010	((450R - 92R) / 450R) * VREG1
	VRP/N0 5-0 = 100011	((450R - 96R) / 450R) * VREG1
	VRP/N0 5-0 = 100100	((450R - 100R) / 450R) * VREG1
	VRP/N0 5-0 = 100101	((450R - 104R) / 450R) * VREG1
	VRP/N0 5-0 = 100110	((450R - 108R) / 450R) * VREG1
	VRP/N0 5-0 = 100111	((450R - 112R) / 450R) * VREG1
	VRP/N0 5-0 = 101000	((450R - 116R) / 450R) * VREG1
	VRP/N0 5-0 = 101001	((450R - 120R) / 450R) * VREG1
	VRP/N0 5-0 = 101010	((450R - 124R) / 450R) * VREG1
	VRP/N0 5-0 = 101011	((450R - 128R) / 450R) * VREG1
	VRP/N0 5-0 = 101100	((450R - 132R) / 450R) * VREG1
	VRP/N0 5-0 = 101101	((450R - 136R) / 450R) * VREG1
	VRP/N0 5-0 = 101110	((450R - 140R) / 450R) * VREG1
	VRP/N0 5-0 = 101111	((450R - 144R) / 450R) * VREG1
	VRP/N0 5-0 = 110000	((450R - 148R) / 450R) * VREG1
	VRP/N0 5-0 = 110001	((450R - 152R) / 450R) * VREG1
	VRP/N0 5-0 = 110010	((450R - 156R) / 450R) * VREG1
	VRP/N0 5-0 = 110011	((450R - 160R) / 450R) * VREG1
	VRP/N0 5-0 = 110100	((450R - 164R) / 450R) * VREG1
	VRP/N0 5-0 = 110101	((450R - 168R) / 450R) * VREG1
	VRP/N0 5-0 = 110110	((450R - 172R) / 450R) * VREG1
	VRP/N0 5-0 = 110111	((450R - 176R) / 450R) * VREG1
	VRP/N0 5-0 = 111000	((450R - 180R) / 450R) * VREG1
	VRP/N0 5-0 = 111001	((450R - 184R) / 450R) * VREG1
	VRP/N0 5-0 = 111010	((450R - 188R) / 450R) * VREG1
	VRP/N0 5-0 = 111011	((450R - 192R) / 450R) * VREG1
	VRP/N0 5-0 = 111100	((450R - 196R) / 450R) * VREG1
	VRP/N0 5-0 = 111101	((450R - 200R) / 450R) * VREG1
	VRP/N0 5-0 = 111110	((450R - 204R) / 450R) * VREG1
	VRP/N0 5-0 = 111111	((450R - 208R) / 450R) * VREG1

Table 7.4 VinP/N 0

Reference Voltage	Macro Adjustment Value	VinP/N1 Formula
VinP/N1	VRP/N1 5-0 = 000000	(430R / 450R) * VREG1
	VRP/N1 5-0 = 000001	((430R - 2R) / 450R) * VREG1
	VRP/N1 5-0 = 000010	((430R - 4R) / 450R) * VREG1
	VRP/N1 5-0 = 000011	((430R - 6R) / 450R) * VREG1
	VRP/N1 5-0 = 000100	((430R - 8R) / 450R) * VREG1
	VRP/N1 5-0 = 000101	((430R - 10R) / 450R) * VREG1
	VRP/N1 5-0 = 000110	((430R - 12R) / 450R) * VREG1
	VRP/N1 5-0 = 000111	((430R - 14R) / 450R) * VREG1
	VRP/N1 5-0 = 001000	((430R - 16R) / 450R) * VREG1
	VRP/N1 5-0 = 001001	((430R - 18R) / 450R) * VREG1
	VRP/N1 5-0 = 001010	((430R - 20R) / 450R) * VREG1
	VRP/N1 5-0 = 001011	((430R - 22R) / 450R) * VREG1
	VRP/N1 5-0 = 001100	((430R - 24R) / 450R) * VREG1
	VRP/N1 5-0 = 001101	((430R - 26R) / 450R) * VREG1
	VRP/N1 5-0 = 001110	((430R - 28R) / 450R) * VREG1
	VRP/N1 5-0 = 001111	((430R - 30R) / 450R) * VREG1
	VRP/N1 5-0 = 010000	((430R - 32R) / 450R) * VREG1
	VRP/N1 5-0 = 010001	((430R - 34R) / 450R) * VREG1
	VRP/N1 5-0 = 010010	((430R - 36R) / 450R) * VREG1
	VRP/N1 5-0 = 010011	((430R - 38R) / 450R) * VREG1
	VRP/N1 5-0 = 010100	((430R - 40R) / 450R) * VREG1
	VRP/N1 5-0 = 010101	((430R - 42R) / 450R) * VREG1
	VRP/N1 5-0 = 010110	((430R - 44R) / 450R) * VREG1
	VRP/N1 5-0 = 010111	((430R - 46R) / 450R) * VREG1
	VRP/N1 5-0 = 011000	((430R - 48R) / 450R) * VREG1
	VRP/N1 5-0 = 011001	((430R - 50R) / 450R) * VREG1
	VRP/N1 5-0 = 011010	((430R - 52R) / 450R) * VREG1
	VRP/N1 5-0 = 011011	((430R - 54R) / 450R) * VREG1
	VRP/N1 5-0 = 011100	((430R - 56R) / 450R) * VREG1
	VRP/N1 5-0 = 011101	((430R - 58R) / 450R) * VREG1
	VRP/N1 5-0 = 011110	((430R - 60R) / 450R) * VREG1
	VRP/N1 5-0 = 011111	((430R - 62R) / 450R) * VREG1
	VRP/N1 5-0 = 100000	((430R - 66R) / 450R) * VREG1
	VRP/N1 5-0 = 100001	((430R - 70R) / 450R) * VREG1
	VRP/N1 5-0 = 100010	((430R - 74R) / 450R) * VREG1
	VRP/N1 5-0 = 100011	((430R - 78R) / 450R) * VREG1
	VRP/N1 5-0 = 100100	((430R - 82R) / 450R) * VREG1
	VRP/N1 5-0 = 100101	((430R - 86R) / 450R) * VREG1
	VRP/N1 5-0 = 100110	((430R - 90R) / 450R) * VREG1
	VRP/N1 5-0 = 100111	((430R - 94R) / 450R) * VREG1
	VRP/N1 5-0 = 101000	((430R - 98R) / 450R) * VREG1
	VRP/N1 5-0 = 101001	((430R - 102R) / 450R) * VREG1
	VRP/N1 5-0 = 101010	((430R - 106R) / 450R) * VREG1
	VRP/N1 5-0 = 101011	((430R - 110R) / 450R) * VREG1
	VRP/N1 5-0 = 101100	((430R - 114R) / 450R) * VREG1
	VRP/N1 5-0 = 101101	((430R - 118R) / 450R) * VREG1
	VRP/N1 5-0 = 101110	((430R - 122R) / 450R) * VREG1
	VRP/N1 5-0 = 101111	((430R - 126R) / 450R) * VREG1
	VRP/N1 5-0 = 110000	((430R - 130R) / 450R) * VREG1
	VRP/N1 5-0 = 110001	((430R - 134R) / 450R) * VREG1
	VRP/N1 5-0 = 110010	((430R - 138R) / 450R) * VREG1
	VRP/N1 5-0 = 110011	((430R - 142R) / 450R) * VREG1
	VRP/N1 5-0 = 110100	((430R - 146R) / 450R) * VREG1
	VRP/N1 5-0 = 110101	((430R - 150R) / 450R) * VREG1
	VRP/N1 5-0 = 110110	((430R - 154R) / 450R) * VREG1
	VRP/N1 5-0 = 110111	((430R - 158R) / 450R) * VREG1
	VRP/N1 5-0 = 111000	((430R - 162R) / 450R) * VREG1
	VRP/N1 5-0 = 111001	((430R - 166R) / 450R) * VREG1
	VRP/N1 5-0 = 111010	((430R - 170R) / 450R) * VREG1
	VRP/N1 5-0 = 111011	((430R - 174R) / 450R) * VREG1
	VRP/N1 5-0 = 111100	((430R - 178R) / 450R) * VREG1
	VRP/N1 5-0 = 111101	((430R - 182R) / 450R) * VREG1
	VRP/N1 5-0 = 111110	((430R - 186R) / 450R) * VREG1
	VRP/N1 5-0 = 111111	((430R - 190R) / 450R) * VREG1

Table 7.5 VinP/N 1

Reference Voltage	Macro Adjustment Value	VinP/N2 Formula
VinP/N2	VRP/N2 5-0 = 000000	(410R / 450R) * VREG1
	VRP/N2 5-0 = 000001	((410R - 2R) / 450R) * VREG1
	VRP/N2 5-0 = 000010	((410R - 4R) / 450R) * VREG1
	VRP/N2 5-0 = 000011	((410R - 6R) / 450R) * VREG1
	VRP/N2 5-0 = 000100	((410R - 8R) / 450R) * VREG1
	VRP/N2 5-0 = 000101	((410R - 10R) / 450R) * VREG1
	VRP/N2 5-0 = 000110	((410R - 12R) / 450R) * VREG1
	VRP/N2 5-0 = 000111	((410R - 14R) / 450R) * VREG1
	VRP/N2 5-0 = 001000	((410R - 16R) / 450R) * VREG1
	VRP/N2 5-0 = 001001	((410R - 18R) / 450R) * VREG1
	VRP/N2 5-0 = 001010	((410R - 20R) / 450R) * VREG1
	VRP/N2 5-0 = 001011	((410R - 22R) / 450R) * VREG1
	VRP/N2 5-0 = 001100	((410R - 24R) / 450R) * VREG1
	VRP/N2 5-0 = 001101	((410R - 26R) / 450R) * VREG1
	VRP/N2 5-0 = 001110	((410R - 28R) / 450R) * VREG1
	VRP/N2 5-0 = 001111	((410R - 30R) / 450R) * VREG1
	VRP/N2 5-0 = 010000	((410R - 32R) / 450R) * VREG1
	VRP/N2 5-0 = 010001	((410R - 34R) / 450R) * VREG1
	VRP/N2 5-0 = 010010	((410R - 36R) / 450R) * VREG1
	VRP/N2 5-0 = 010011	((410R - 38R) / 450R) * VREG1
	VRP/N2 5-0 = 010100	((410R - 40R) / 450R) * VREG1
	VRP/N2 5-0 = 010101	((410R - 42R) / 450R) * VREG1
	VRP/N2 5-0 = 010110	((410R - 44R) / 450R) * VREG1
	VRP/N2 5-0 = 010111	((410R - 46R) / 450R) * VREG1
	VRP/N2 5-0 = 011000	((410R - 48R) / 450R) * VREG1
	VRP/N2 5-0 = 011001	((410R - 50R) / 450R) * VREG1
	VRP/N2 5-0 = 011010	((410R - 52R) / 450R) * VREG1
	VRP/N2 5-0 = 011011	((410R - 54R) / 450R) * VREG1
	VRP/N2 5-0 = 011100	((410R - 56R) / 450R) * VREG1
	VRP/N2 5-0 = 011101	((410R - 58R) / 450R) * VREG1
	VRP/N2 5-0 = 011110	((410R - 60R) / 450R) * VREG1
	VRP/N2 5-0 = 011111	((410R - 62R) / 450R) * VREG1
	VRP/N2 5-0 = 100000	((410R - 66R) / 450R) * VREG1
	VRP/N2 5-0 = 100001	((410R - 70R) / 450R) * VREG1
	VRP/N2 5-0 = 100010	((410R - 74R) / 450R) * VREG1
	VRP/N2 5-0 = 100011	((410R - 78R) / 450R) * VREG1
	VRP/N2 5-0 = 100100	((410R - 82R) / 450R) * VREG1
	VRP/N2 5-0 = 100101	((410R - 86R) / 450R) * VREG1
	VRP/N2 5-0 = 100110	((410R - 90R) / 450R) * VREG1
	VRP/N2 5-0 = 100111	((410R - 94R) / 450R) * VREG1
	VRP/N2 5-0 = 101000	((410R - 98R) / 450R) * VREG1
	VRP/N2 5-0 = 101001	((410R - 102R) / 450R) * VREG1
	VRP/N2 5-0 = 101010	((410R - 106R) / 450R) * VREG1
	VRP/N2 5-0 = 101011	((410R - 110R) / 450R) * VREG1
	VRP/N2 5-0 = 101100	((410R - 114R) / 450R) * VREG1
	VRP/N2 5-0 = 101101	((410R - 118R) / 450R) * VREG1
	VRP/N2 5-0 = 101110	((410R - 122R) / 450R) * VREG1
	VRP/N2 5-0 = 101111	((410R - 126R) / 450R) * VREG1
	VRP/N2 5-0 = 110000	((410R - 130R) / 450R) * VREG1
	VRP/N2 5-0 = 110001	((410R - 134R) / 450R) * VREG1
	VRP/N2 5-0 = 110010	((410R - 138R) / 450R) * VREG1
	VRP/N2 5-0 = 110011	((410R - 142R) / 450R) * VREG1
	VRP/N2 5-0 = 110100	((410R - 146R) / 450R) * VREG1
	VRP/N2 5-0 = 110101	((410R - 150R) / 450R) * VREG1
	VRP/N2 5-0 = 110110	((410R - 154R) / 450R) * VREG1
	VRP/N2 5-0 = 110111	((410R - 158R) / 450R) * VREG1
	VRP/N2 5-0 = 111000	((410R - 162R) / 450R) * VREG1
	VRP/N2 5-0 = 111001	((410R - 166R) / 450R) * VREG1
	VRP/N2 5-0 = 111010	((410R - 170R) / 450R) * VREG1
	VRP/N2 5-0 = 111011	((410R - 174R) / 450R) * VREG1
	VRP/N2 5-0 = 111100	((410R - 178R) / 450R) * VREG1
	VRP/N2 5-0 = 111101	((410R - 182R) / 450R) * VREG1
	VRP/N2 5-0 = 111110	((410R - 186R) / 450R) * VREG1
	VRP/N2 5-0 = 111111	((410R - 190R) / 450R) * VREG1

Table 7.6 VinP/N 2

Reference Voltage	Macro Adjustment Value	VinP/N10 Formula
VinP/N10	VRP/N3 5-0 = 000000	(230R / 450R) * VREG1
	VRP/N3 5-0 = 000001	((230R - 4R) / 450R) * VREG1
	VRP/N3 5-0 = 000010	((230R - 8R) / 450R) * VREG1
	VRP/N3 5-0 = 000011	((230R - 12R) / 450R) * VREG1
	VRP/N3 5-0 = 000100	((230R - 16R) / 450R) * VREG1
	VRP/N3 5-0 = 000101	((230R - 20R) / 450R) * VREG1
	VRP/N3 5-0 = 000110	((230R - 24R) / 450R) * VREG1
	VRP/N3 5-0 = 000111	((230R - 28R) / 450R) * VREG1
	VRP/N3 5-0 = 001000	((230R - 32R) / 450R) * VREG1
	VRP/N3 5-0 = 001001	((230R - 36R) / 450R) * VREG1
	VRP/N3 5-0 = 001010	((230R - 40R) / 450R) * VREG1
	VRP/N3 5-0 = 001011	((230R - 44R) / 450R) * VREG1
	VRP/N3 5-0 = 001100	((230R - 48R) / 450R) * VREG1
	VRP/N3 5-0 = 001101	((230R - 52R) / 450R) * VREG1
	VRP/N3 5-0 = 001110	((230R - 56R) / 450R) * VREG1
	VRP/N3 5-0 = 001111	((230R - 60R) / 450R) * VREG1
	VRP/N3 5-0 = 010000	((230R - 64R) / 450R) * VREG1
	VRP/N3 5-0 = 010001	((230R - 68R) / 450R) * VREG1
	VRP/N3 5-0 = 010010	((230R - 72R) / 450R) * VREG1
	VRP/N3 5-0 = 010011	((230R - 76R) / 450R) * VREG1
	VRP/N3 5-0 = 010100	((230R - 80R) / 450R) * VREG1
	VRP/N3 5-0 = 010101	((230R - 84R) / 450R) * VREG1
	VRP/N3 5-0 = 010110	((230R - 88R) / 450R) * VREG1
	VRP/N3 5-0 = 010111	((230R - 92R) / 450R) * VREG1
	VRP/N3 5-0 = 011000	((230R - 96R) / 450R) * VREG1
	VRP/N3 5-0 = 011001	((230R - 100R) / 450R) * VREG1
	VRP/N3 5-0 = 011010	((230R - 104R) / 450R) * VREG1
	VRP/N3 5-0 = 011011	((230R - 108R) / 450R) * VREG1
	VRP/N3 5-0 = 011100	((230R - 112R) / 450R) * VREG1
	VRP/N3 5-0 = 011101	((230R - 116R) / 450R) * VREG1
	VRP/N3 5-0 = 011110	((230R - 120R) / 450R) * VREG1
	VRP/N3 5-0 = 011111	((230R - 124R) / 450R) * VREG1
	VRP/N3 5-0 = 100000	((230R - 128R) / 450R) * VREG1
	VRP/N3 5-0 = 100001	((230R - 130R) / 450R) * VREG1
	VRP/N3 5-0 = 100010	((230R - 132R) / 450R) * VREG1
	VRP/N3 5-0 = 100011	((230R - 134R) / 450R) * VREG1
	VRP/N3 5-0 = 100100	((230R - 136R) / 450R) * VREG1
	VRP/N3 5-0 = 100101	((230R - 138R) / 450R) * VREG1
	VRP/N3 5-0 = 100110	((230R - 140R) / 450R) * VREG1
	VRP/N3 5-0 = 100111	((230R - 142R) / 450R) * VREG1
	VRP/N3 5-0 = 101000	((230R - 144R) / 450R) * VREG1
	VRP/N3 5-0 = 101001	((230R - 146R) / 450R) * VREG1
	VRP/N3 5-0 = 101010	((230R - 148R) / 450R) * VREG1
	VRP/N3 5-0 = 101011	((230R - 150R) / 450R) * VREG1
	VRP/N3 5-0 = 101100	((230R - 152R) / 450R) * VREG1
	VRP/N3 5-0 = 101101	((230R - 154R) / 450R) * VREG1
	VRP/N3 5-0 = 101110	((230R - 156R) / 450R) * VREG1
	VRP/N3 5-0 = 101111	((230R - 158R) / 450R) * VREG1
	VRP/N3 5-0 = 110000	((230R - 160R) / 450R) * VREG1
	VRP/N3 5-0 = 110001	((230R - 162R) / 450R) * VREG1
	VRP/N3 5-0 = 110010	((230R - 164R) / 450R) * VREG1
	VRP/N3 5-0 = 110011	((230R - 166R) / 450R) * VREG1
	VRP/N3 5-0 = 110100	((230R - 168R) / 450R) * VREG1
	VRP/N3 5-0 = 110101	((230R - 170R) / 450R) * VREG1
	VRP/N3 5-0 = 110110	((230R - 172R) / 450R) * VREG1
	VRP/N3 5-0 = 110111	((230R - 174R) / 450R) * VREG1
	VRP/N3 5-0 = 111000	((230R - 176R) / 450R) * VREG1
	VRP/N3 5-0 = 111001	((230R - 178R) / 450R) * VREG1
	VRP/N3 5-0 = 111010	((230R - 180R) / 450R) * VREG1
	VRP/N3 5-0 = 111011	((230R - 182R) / 450R) * VREG1
	VRP/N3 5-0 = 111100	((230R - 184R) / 450R) * VREG1
	VRP/N3 5-0 = 111101	((230R - 186R) / 450R) * VREG1
	VRP/N3 5-0 = 111110	((230R - 188R) / 450R) * VREG1
	VRP/N3 5-0 = 111111	((230R - 190R) / 450R) * VREG1

Table 7.7 VinP/N 10

Reference Voltage	Macro Adjustment Value	VinP/N11 Formula
VinP/N11	VRP/N4 5-0 = 000000	(210R / 450R) * VREG1
	VRP/N4 5-0 = 000001	((210R - 4R) / 450R) * VREG1
	VRP/N4 5-0 = 000010	((210R - 8R) / 450R) * VREG1
	VRP/N4 5-0 = 000011	((210R - 12R) / 450R) * VREG1
	VRP/N4 5-0 = 000100	((210R - 16R) / 450R) * VREG1
	VRP/N4 5-0 = 000101	((210R - 20R) / 450R) * VREG1
	VRP/N4 5-0 = 000110	((210R - 24R) / 450R) * VREG1
	VRP/N4 5-0 = 000111	((210R - 28R) / 450R) * VREG1
	VRP/N4 5-0 = 001000	((210R - 32R) / 450R) * VREG1
	VRP/N4 5-0 = 001001	((210R - 36R) / 450R) * VREG1
	VRP/N4 5-0 = 001010	((210R - 40R) / 450R) * VREG1
	VRP/N4 5-0 = 001011	((210R - 44R) / 450R) * VREG1
	VRP/N4 5-0 = 001100	((210R - 48R) / 450R) * VREG1
	VRP/N4 5-0 = 001101	((210R - 52R) / 450R) * VREG1
	VRP/N4 5-0 = 001110	((210R - 56R) / 450R) * VREG1
	VRP/N4 5-0 = 001111	((210R - 60R) / 450R) * VREG1
	VRP/N4 5-0 = 010000	((210R - 64R) / 450R) * VREG1
	VRP/N4 5-0 = 010001	((210R - 68R) / 450R) * VREG1
	VRP/N4 5-0 = 010010	((210R - 72R) / 450R) * VREG1
	VRP/N4 5-0 = 010011	((210R - 76R) / 450R) * VREG1
	VRP/N4 5-0 = 010100	((210R - 80R) / 450R) * VREG1
	VRP/N4 5-0 = 010101	((210R - 84R) / 450R) * VREG1
	VRP/N4 5-0 = 010110	((210R - 88R) / 450R) * VREG1
	VRP/N4 5-0 = 010111	((210R - 92R) / 450R) * VREG1
	VRP/N4 5-0 = 011000	((210R - 96R) / 450R) * VREG1
	VRP/N4 5-0 = 011001	((210R - 100R) / 450R) * VREG1
	VRP/N4 5-0 = 011010	((210R - 104R) / 450R) * VREG1
	VRP/N4 5-0 = 011011	((210R - 108R) / 450R) * VREG1
	VRP/N4 5-0 = 011100	((210R - 112R) / 450R) * VREG1
	VRP/N4 5-0 = 011101	((210R - 116R) / 450R) * VREG1
	VRP/N4 5-0 = 011110	((210R - 120R) / 450R) * VREG1
	VRP/N4 5-0 = 011111	((210R - 124R) / 450R) * VREG1
	VRP/N4 5-0 = 100000	((210R - 128R) / 450R) * VREG1
	VRP/N4 5-0 = 100001	((210R - 130R) / 450R) * VREG1
	VRP/N4 5-0 = 100010	((210R - 132R) / 450R) * VREG1
	VRP/N4 5-0 = 100011	((210R - 134R) / 450R) * VREG1
	VRP/N4 5-0 = 100100	((210R - 136R) / 450R) * VREG1
	VRP/N4 5-0 = 100101	((210R - 138R) / 450R) * VREG1
	VRP/N4 5-0 = 100110	((210R - 140R) / 450R) * VREG1
	VRP/N4 5-0 = 100111	((210R - 142R) / 450R) * VREG1
	VRP/N4 5-0 = 101000	((210R - 144R) / 450R) * VREG1
	VRP/N4 5-0 = 101001	((210R - 146R) / 450R) * VREG1
	VRP/N4 5-0 = 101010	((210R - 148R) / 450R) * VREG1
	VRP/N4 5-0 = 101011	((210R - 150R) / 450R) * VREG1
	VRP/N4 5-0 = 101100	((210R - 152R) / 450R) * VREG1
	VRP/N4 5-0 = 101101	((210R - 154R) / 450R) * VREG1
	VRP/N4 5-0 = 101110	((210R - 156R) / 450R) * VREG1
	VRP/N4 5-0 = 101111	((210R - 158R) / 450R) * VREG1
	VRP/N4 5-0 = 110000	((210R - 160R) / 450R) * VREG1
	VRP/N4 5-0 = 110001	((210R - 162R) / 450R) * VREG1
	VRP/N4 5-0 = 110010	((210R - 164R) / 450R) * VREG1
	VRP/N4 5-0 = 110011	((210R - 166R) / 450R) * VREG1
	VRP/N4 5-0 = 110100	((210R - 168R) / 450R) * VREG1
	VRP/N4 5-0 = 110101	((210R - 170R) / 450R) * VREG1
	VRP/N4 5-0 = 110110	((210R - 172R) / 450R) * VREG1
	VRP/N4 5-0 = 110111	((210R - 174R) / 450R) * VREG1
	VRP/N4 5-0 = 111000	((210R - 176R) / 450R) * VREG1
	VRP/N4 5-0 = 111001	((210R - 178R) / 450R) * VREG1
	VRP/N4 5-0 = 111010	((210R - 180R) / 450R) * VREG1
	VRP/N4 5-0 = 111011	((210R - 182R) / 450R) * VREG1
	VRP/N4 5-0 = 111100	((210R - 184R) / 450R) * VREG1
	VRP/N4 5-0 = 111101	((210R - 186R) / 450R) * VREG1
	VRP/N4 5-0 = 111110	((210R - 188R) / 450R) * VREG1
	VRP/N4 5-0 = 111111	((210R - 190R) / 450R) * VREG1

Table 7.8 VinP/N 11

Reference Voltage	Macro Adjustment Value	VinP/N12 Formula
VinP/N12	VRP/N5 5-0 = 000000	(210R / 450R) * VREG1
	VRP/N5 5-0 = 000001	((208R - 4R) / 450R) * VREG1
	VRP/N5 5-0 = 000010	((208R - 8R) / 450R) * VREG1
	VRP/N5 5-0 = 000011	((208R - 12R) / 450R) * VREG1
	VRP/N5 5-0 = 000100	((208R - 16R) / 450R) * VREG1
	VRP/N5 5-0 = 000101	((208R - 20R) / 450R) * VREG1
	VRP/N5 5-0 = 000110	((208R - 24R) / 450R) * VREG1
	VRP/N5 5-0 = 000111	((208R - 28R) / 450R) * VREG1
	VRP/N5 5-0 = 001000	((208R - 32R) / 450R) * VREG1
	VRP/N5 5-0 = 001001	((208R - 36R) / 450R) * VREG1
	VRP/N5 5-0 = 001010	((208R - 40R) / 450R) * VREG1
	VRP/N5 5-0 = 001011	((208R - 44R) / 450R) * VREG1
	VRP/N5 5-0 = 001100	((208R - 48R) / 450R) * VREG1
	VRP/N5 5-0 = 001101	((208R - 52R) / 450R) * VREG1
	VRP/N5 5-0 = 001110	((208R - 56R) / 450R) * VREG1
	VRP/N5 5-0 = 001111	((208R - 60R) / 450R) * VREG1
	VRP/N5 5-0 = 010000	((208R - 64R) / 450R) * VREG1
	VRP/N5 5-0 = 010001	((208R - 68R) / 450R) * VREG1
	VRP/N5 5-0 = 010010	((208R - 72R) / 450R) * VREG1
	VRP/N5 5-0 = 010011	((208R - 76R) / 450R) * VREG1
	VRP/N5 5-0 = 010100	((208R - 80R) / 450R) * VREG1
	VRP/N5 5-0 = 010101	((208R - 84R) / 450R) * VREG1
	VRP/N5 5-0 = 010110	((208R - 88R) / 450R) * VREG1
	VRP/N5 5-0 = 010111	((208R - 92R) / 450R) * VREG1
	VRP/N5 5-0 = 011000	((208R - 96R) / 450R) * VREG1
	VRP/N5 5-0 = 011001	((208R - 100R) / 450R) * VREG1
	VRP/N5 5-0 = 011010	((208R - 104R) / 450R) * VREG1
	VRP/N5 5-0 = 011011	((208R - 108R) / 450R) * VREG1
	VRP/N5 5-0 = 011100	((208R - 112R) / 450R) * VREG1
	VRP/N5 5-0 = 011101	((208R - 116R) / 450R) * VREG1
	VRP/N5 5-0 = 011110	((208R - 120R) / 450R) * VREG1
	VRP/N5 5-0 = 011111	((208R - 124R) / 450R) * VREG1
	VRP/N5 5-0 = 100000	((208R - 128R) / 450R) * VREG1
	VRP/N5 5-0 = 100001	((208R - 130R) / 450R) * VREG1
	VRP/N5 5-0 = 100010	((208R - 132R) / 450R) * VREG1
	VRP/N5 5-0 = 100011	((208R - 134R) / 450R) * VREG1
	VRP/N5 5-0 = 100100	((208R - 136R) / 450R) * VREG1
	VRP/N5 5-0 = 100101	((208R - 138R) / 450R) * VREG1
	VRP/N5 5-0 = 100110	((208R - 140R) / 450R) * VREG1
	VRP/N5 5-0 = 100111	((208R - 142R) / 450R) * VREG1
	VRP/N5 5-0 = 101000	((208R - 144R) / 450R) * VREG1
	VRP/N5 5-0 = 101001	((208R - 146R) / 450R) * VREG1
	VRP/N5 5-0 = 101010	((208R - 148R) / 450R) * VREG1
	VRP/N5 5-0 = 101011	((208R - 150R) / 450R) * VREG1
	VRP/N5 5-0 = 101100	((208R - 152R) / 450R) * VREG1
	VRP/N5 5-0 = 101101	((208R - 154R) / 450R) * VREG1
	VRP/N5 5-0 = 101110	((208R - 156R) / 450R) * VREG1
	VRP/N5 5-0 = 101111	((208R - 158R) / 450R) * VREG1
	VRP/N5 5-0 = 110000	((208R - 160R) / 450R) * VREG1
	VRP/N5 5-0 = 110001	((208R - 162R) / 450R) * VREG1
	VRP/N5 5-0 = 110010	((208R - 164R) / 450R) * VREG1
	VRP/N5 5-0 = 110011	((208R - 166R) / 450R) * VREG1
	VRP/N5 5-0 = 110100	((208R - 168R) / 450R) * VREG1
	VRP/N5 5-0 = 110101	((208R - 170R) / 450R) * VREG1
	VRP/N5 5-0 = 110110	((208R - 172R) / 450R) * VREG1
	VRP/N5 5-0 = 110111	((208R - 174R) / 450R) * VREG1
	VRP/N5 5-0 = 111000	((208R - 176R) / 450R) * VREG1
	VRP/N5 5-0 = 111001	((208R - 178R) / 450R) * VREG1
	VRP/N5 5-0 = 111010	((208R - 180R) / 450R) * VREG1
	VRP/N5 5-0 = 111011	((208R - 182R) / 450R) * VREG1
	VRP/N5 5-0 = 111100	((208R - 184R) / 450R) * VREG1
	VRP/N5 5-0 = 111101	((208R - 186R) / 450R) * VREG1
	VRP/N5 5-0 = 111110	((208R - 188R) / 450R) * VREG1
	VRP/N5 5-0 = 111111	GND

Table 7.9 VinP/N 12

Reference Voltage	Macro Adjustment Value	VinP/N4 Formula
VinP/N4	PRP/N0 6-0 = 0000000	(350R / 450R) * VREG1
	PRP/N0 6-0 = 0000001	((350R - 2R) / 450R) * VREG1
	PRP/N0 6-0 = 0000010	((350R - 4R) / 450R) * VREG1
	PRP/N0 6-0 = 0000011	((350R – 6R) / 450R) * VREG1
	PRP/N0 6-0 = 0000100	((350R – 8R) / 450R) * VREG1
	PRP/N0 6-0 = 0000101	((350R – 10R) / 450R) * VREG1
	PRP/N0 6-0 = 0000110	((350R – 12R) / 450R) * VREG1
	PRP/N0 6-0 = 0000111	((350R - 14R) / 450R) * VREG1
	PRP/N0 6-0 = 0001000	((350R – 16R) / 450R) * VREG1
	PRP/N0 6-0 = 0001001	((350R – 18R) / 450R) * VREG1
	PRP/N0 6-0 = 0001010	((350R – 20R) / 450R) * VREG1
	PRP/N0 6-0 = 0001011	((350R – 22R) / 450R) * VREG1
	PRP/N0 6-0 = 0001100	((350R – 24R) / 450R) * VREG1
	PRP/N0 6-0 = 0001101	((350R – 26R) / 450R) * VREG1
	PRP/N0 6-0 = 0001110	((350R – 28R) / 450R) * VREG1
	PRP/N0 6-0 = 0001111	((350R – 30R) / 450R) * VREG1
	PRP/N0 6-0 = 0010000	((350R – 32R) / 450R) * VREG1
	PRP/N0 6-0 = 0010001	((350R - 34R) / 450R) * VREG1
	PRP/N0 6-0 = 0010010	((350R – 36R) / 450R) * VREG1
	PRP/N0 6-0 = 0010011	((350R – 38R) / 450R) * VREG1
	PRP/N0 6-0 = 0010100	((350R – 40R) / 450R) * VREG1
	PRP/N0 6-0 = 0010101	((350R – 42R) / 450R) * VREG1
	PRP/N0 6-0 = 0010110	((350R – 44R) / 450R) * VREG1
	PRP/N0 6-0 = 0010111	((350R – 46R) / 450R) * VREG1
	PRP/N0 6-0 = 0011000	((350R – 48R) / 450R) * VREG1
	PRP/N0 6-0 = 0011001	((350R – 50R) / 450R) * VREG1
	PRP/N0 6-0 = 0011010	((350R – 52R) / 450R) * VREG1
	PRP/N0 6-0 = 0011011	((350R - 54R) / 450R) * VREG1
	PRP/N0 6-0 = 0011100	((350R – 56R) / 450R) * VREG1
	PRP/N0 6-0 = 0011101	((350R – 58R) / 450R) * VREG1
	PRP/N0 6-0 = 0011110	((350R – 60R) / 450R) * VREG1
	PRP/N0 6-0 = 0011111	((350R – 62R) / 450R) * VREG1
	PRP/N0 6-0 = 0100000	((350R - 64R) / 450R) * VREG1
	PRP/N0 6-0 = 0100001	((350R – 66R) / 450R) * VREG1
	PRP/N0 6-0 = 0100010	((350R – 68R) / 450R) * VREG1
	PRP/N0 6-0 = 0100011	((350R – 70R) / 450R) * VREG1
	PRP/N0 6-0 = 0100100	((350R – 72R) / 450R) * VREG1
	PRP/N0 6-0 = 0100101	((350R – 74R) / 450R) * VREG1
	PRP/N0 6-0 = 0100110	((350R – 76R) / 450R) * VREG1
	PRP/N0 6-0 = 0100111	((350R – 78R) / 450R) * VREG1
	PRP/N0 6-0 = 0101000	((350R – 80R) / 450R) * VREG1
	PRP/N0 6-0 = 0101001	((350R – 82R) / 450R) * VREG1
	PRP/N0 6-0 = 0101010	((350R - 84R) / 450R) * VREG1
	PRP/N0 6-0 = 0101011	((350R – 86R) / 450R) * VREG1
	PRP/N0 6-0 = 0101100	((350R – 88R) / 450R) * VREG1
	PRP/N0 6-0 = 0101101	((350R – 90R) / 450R) * VREG1
	PRP/N0 6-0 = 0101110	((350R – 92R) / 450R) * VREG1
	PRP/N0 6-0 = 0101111	((350R – 94R) / 450R) * VREG1
	PRP/N0 6-0 = 0110000	((350R – 96R) / 450R) * VREG1
	PRP/N0 6-0 = 0110001	((350R – 98R) / 450R) * VREG1
	PRP/N0 6-0 = 0110010	((350R – 100R) / 450R) * VREG1
	PRP/N0 6-0 = 0110011	((350R – 102R) / 450R) * VREG1
	PRP/N0 6-0 = 0110100	((350R – 104R) / 450R) * VREG1
	PRP/N0 6-0 = 0110101	((350R – 106R) / 450R) * VREG1
	PRP/N0 6-0 = 0110110	((350R – 108R) / 450R) * VREG1
	PRP/N0 6-0 = 0110111	((350R – 110R) / 450R) * VREG1
	PRP/N0 6-0 = 0111000	((350R – 112R) / 450R) * VREG1
	PRP/N0 6-0 = 0111001	((350R – 114R) / 450R) * VREG1
	PRP/N0 6-0 = 0111010	((350R – 116R) / 450R) * VREG1
	PRP/N0 6-0 = 0111011	((350R – 118R) / 450R) * VREG1
	PRP/N0 6-0 = 0111100	((350R – 120R) / 450R) * VREG1
	PRP/N0 6-0 = 0111101	((350R – 122R) / 450R) * VREG1
	PRP/N0 6-0 = 0111110	((350R - 124R) / 450R) * VREG1
	PRP/N0 6-0 = 0111111	((350R – 126R) / 450R) * VREG1
	PRP/N0 6-0 = 1000000	((350R – 128R) / 450R) * VREG1
	PRP/N0 6-0 = 1000001	((350R – 130R) / 450R) * VREG1
	PRP/N0 6-0 = 1000010	((350R - 132R) / 450R) * VREG1
	PRP/N0 6-0 = 1000011	((350R – 134R) / 450R) * VREG1
	PRP/N0 6-0 = 1000100	((350R – 136R) / 450R) * VREG1

	PRP/N0 6-0 = 1000101	((350R – 138R) / 450R) * VREG1
	PRP/N0 6-0 = 1000110	((350R – 140R) / 450R) * VREG1
	PRP/N0 6-0 = 1000111	((350R – 142R) / 450R) * VREG1
	PRP/N0 6-0 = 1001000	((350R – 144R) / 450R) * VREG1
	PRP/N0 6-0 = 1001001	((350R – 146R) / 450R) * VREG1
	PRP/N0 6-0 = 1001010	((350R – 148R) / 450R) * VREG1
	PRP/N0 6-0 = 1001011	((350R – 150R) / 450R) * VREG1
	PRP/N0 6-0 = 1001100	((350R - 152R) / 450R) * VREG1
	PRP/N0 6-0 = 1001101	((350R – 154R) / 450R) * VREG1
	PRP/N0 6-0 = 1001110	((350R – 156R) / 450R) * VREG1
	PRP/N0 6-0 = 1001111	((350R – 158R) / 450R) * VREG1
	PRP/N0 6-0 = 1010000	((350R – 160R) / 450R) * VREG1
	PRP/N0 6-0 = 1010001	((350R – 162R) / 450R) * VREG1
	PRP/N0 6-0 = 1010010	((350R – 164R) / 450R) * VREG1
	PRP/N0 6-0 = 1010011	((350R – 166R) / 450R) * VREG1
	PRP/N0 6-0 = 1010100	((350R – 168R) / 450R) * VREG1
	PRP/N0 6-0 = 1010101	((350R – 170R) / 450R) * VREG1
	PRP/N0 6-0 = 1010110	((350R – 172R) / 450R) * VREG1
	PRP/N0 6-0 = 1010111	((350R - 174R) / 450R) * VREG1
	PRP/N0 6-0 = 1011000	((350R – 176R) / 450R) * VREG1
	PRP/N0 6-0 = 1011001	((350R – 178R) / 450R) * VREG1
	PRP/N0 6-0 = 1011010	((350R – 180R) / 450R) * VREG1
	PRP/N0 6-0 = 1011011	((350R – 182R) / 450R) * VREG1
	PRP/N0 6-0 = 1011100	((350R – 184R) / 450R) * VREG1
	PRP/N0 6-0 = 1011101	((350R – 186R) / 450R) * VREG1
	PRP/N0 6-0 = 1011110	((350R – 188R) / 450R) * VREG1
	PRP/N0 6-0 = 1011111	((350R – 190R) / 450R) * VREG1
	PRP/N0 6-0 = 1100000	((350R – 192R) / 450R) * VREG1
	PRP/N0 6-0 = 1100001	((350R – 194R) / 450R) * VREG1
	PRP/N0 6-0 = 1100010	((350R – 196R) / 450R) * VREG1
	PRP/N0 6-0 = 1100011	((350R – 198R) / 450R) * VREG1
	PRP/N0 6-0 = 1100100	((350R – 200R) / 450R) * VREG1
	PRP/N0 6-0 = 1100101	((350R – 202R) / 450R) * VREG1
	PRP/N0 6-0 = 1100110	((350R – 204R) / 450R) * VREG1
	PRP/N0 6-0 = 1100111	((350R – 206R) / 450R) * VREG1
	PRP/N0 6-0 = 1101000	((350R – 208R) / 450R) * VREG1
	PRP/N0 6-0 = 1101001	((350R – 210R) / 450R) * VREG1
	PRP/N0 6-0 = 1101010	((350R – 212R) / 450R) * VREG1
	PRP/N0 6-0 = 1101011	((350R – 214R) / 450R) * VREG1
	PRP/N0 6-0 = 1101100	((350R – 216R) / 450R) * VREG1
	PRP/N0 6-0 = 1101101	((350R – 218R) / 450R) * VREG1
	PRP/N0 6-0 = 1101110	((350R – 220R) / 450R) * VREG1
	PRP/N0 6-0 = 1101111	((350R – 223R) / 450R) * VREG1
	PRP/N0 6-0 = 1110000	((350R – 224R) / 450R) * VREG1
	PRP/N0 6-0 = 1110001	((350R – 226R) / 450R) * VREG1
	PRP/N0 6-0 = 1110010	((350R – 228R) / 450R) * VREG1
	PRP/N0 6-0 = 1110011	((350R – 230R) / 450R) * VREG1
	PRP/N0 6-0 = 1110100	((350R – 232R) / 450R) * VREG1
	PRP/N0 6-0 = 1110101	((350R – 234R) / 450R) * VREG1
	PRP/N0 6-0 = 1110110	((350R – 236R) / 450R) * VREG1
	PRP/N0 6-0 = 1110111	((350R – 238R) / 450R) * VREG1
	PRP/N0 6-0 = 1111000	((350R – 240R) / 450R) * VREG1
	PRP/N0 6-0 = 1111001	((350R – 243R) / 450R) * VREG1
	PRP/N0 6-0 = 1111010	((350R – 244R) / 450R) * VREG1
	PRP/N0 6-0 = 1111011	((350R – 246R) / 450R) * VREG1
	PRP/N0 6-0 = 1111100	((350R – 248R) / 450R) * VREG1
	PRP/N0 6-0 = 1111101	((350R – 250R) / 450R) * VREG1
	PRP/N0 6-0 = 1111110	((350R – 252R) / 450R) * VREG1
	PRP/N0 6-0 = 1111111	((350R – 254R) / 450R) * VREG1

Table 7.10 VinP/N4

Reference Voltage	Macro Adjustment Value	VinP/N8 Formula
VinP/N8	PRP/N1 6-0 = 0000000	(354R / 450R) * VREG1
	PRP/N1 6-0 = 0000001	((354R - 2R) / 450R) * VREG1
	PRP/N1 6-0 = 0000010	((354R - 4R) / 450R) * VREG1
	PRP/N1 6-0 = 0000011	((354R – 6R) / 450R) * VREG1
	PRP/N1 6-0 = 0000100	((354R – 8R) / 450R) * VREG1
	PRP/N1 6-0 = 0000101	((354R – 10R) / 450R) * VREG1
	PRP/N1 6-0 = 0000110	((354R – 12R) / 450R) * VREG1
	PRP/N1 6-0 = 0000111	((354R - 14R) / 450R) * VREG1
	PRP/N1 6-0 = 0001000	((354R – 16R) / 450R) * VREG1
	PRP/N1 6-0 = 0001001	((354R – 18R) / 450R) * VREG1
	PRP/N1 6-0 = 0001010	((354R – 20R) / 450R) * VREG1
	PRP/N1 6-0 = 0001011	((354R – 22R) / 450R) * VREG1
	PRP/N1 6-0 = 0001100	((354R – 24R) / 450R) * VREG1
	PRP/N1 6-0 = 0001101	((354R – 26R) / 450R) * VREG1
	PRP/N1 6-0 = 0001110	((354R – 28R) / 450R) * VREG1
	PRP/N1 6-0 = 0001111	((354R – 30R) / 450R) * VREG1
	PRP/N1 6-0 = 0010000	((354R – 32R) / 450R) * VREG1
	PRP/N1 6-0 = 0010001	((354R - 34R) / 450R) * VREG1
	PRP/N1 6-0 = 0010010	((354R – 36R) / 450R) * VREG1
	PRP/N1 6-0 = 0010011	((354R – 38R) / 450R) * VREG1
	PRP/N1 6-0 = 0010100	((354R – 40R) / 450R) * VREG1
	PRP/N1 6-0 = 0010101	((354R – 42R) / 450R) * VREG1
	PRP/N1 6-0 = 0010110	((354R – 44R) / 450R) * VREG1
	PRP/N1 6-0 = 0010111	((354R – 46R) / 450R) * VREG1
	PRP/N1 6-0 = 0011000	((354R – 48R) / 450R) * VREG1
	PRP/N1 6-0 = 0011001	((354R – 50R) / 450R) * VREG1
	PRP/N1 6-0 = 0011010	((354R – 52R) / 450R) * VREG1
	PRP/N1 6-0 = 0011011	((354R - 54R) / 450R) * VREG1
	PRP/N1 6-0 = 0011100	((354R – 56R) / 450R) * VREG1
	PRP/N1 6-0 = 0011101	((354R – 58R) / 450R) * VREG1
	PRP/N1 6-0 = 0011110	((354R – 60R) / 450R) * VREG1
	PRP/N1 6-0 = 0011111	((354R – 62R) / 450R) * VREG1
	PRP/N1 6-0 = 0100000	((354R - 64R) / 450R) * VREG1
	PRP/N1 6-0 = 0100001	((354R – 66R) / 450R) * VREG1
	PRP/N1 6-0 = 0100010	((354R – 68R) / 450R) * VREG1
	PRP/N1 6-0 = 0100011	((354R – 70R) / 450R) * VREG1
	PRP/N1 6-0 = 0100100	((354R – 72R) / 450R) * VREG1
	PRP/N1 6-0 = 0100101	((354R – 74R) / 450R) * VREG1
	PRP/N1 6-0 = 0100110	((354R – 76R) / 450R) * VREG1
	PRP/N1 6-0 = 0100111	((354R – 78R) / 450R) * VREG1
	PRP/N1 6-0 = 0101000	((354R – 80R) / 450R) * VREG1
	PRP/N1 6-0 = 0101001	((354R – 82R) / 450R) * VREG1
	PRP/N1 6-0 = 0101010	((354R - 84R) / 450R) * VREG1
	PRP/N1 6-0 = 0101011	((354R – 86R) / 450R) * VREG1
	PRP/N1 6-0 = 0101100	((354R – 88R) / 450R) * VREG1
	PRP/N1 6-0 = 0101101	((354R – 90R) / 450R) * VREG1
	PRP/N1 6-0 = 0101110	((354R – 92R) / 450R) * VREG1
	PRP/N1 6-0 = 0101111	((354R – 94R) / 450R) * VREG1
	PRP/N1 6-0 = 0110000	((354R – 96R) / 450R) * VREG1
	PRP/N1 6-0 = 0110001	((354R – 98R) / 450R) * VREG1
	PRP/N1 6-0 = 0110010	((354R – 100R) / 450R) * VREG1
	PRP/N1 6-0 = 0110011	((354R – 102R) / 450R) * VREG1
	PRP/N1 6-0 = 0110100	((354R – 104R) / 450R) * VREG1
	PRP/N1 6-0 = 0110101	((354R – 106R) / 450R) * VREG1
	PRP/N1 6-0 = 0110110	((354R – 108R) / 450R) * VREG1
	PRP/N1 6-0 = 0110111	((354R – 110R) / 450R) * VREG1
	PRP/N1 6-0 = 0111000	((354R – 112R) / 450R) * VREG1
	PRP/N1 6-0 = 0111001	((354R – 114R) / 450R) * VREG1
	PRP/N1 6-0 = 0111010	((354R – 116R) / 450R) * VREG1
	PRP/N1 6-0 = 0111011	((354R – 118R) / 450R) * VREG1
	PRP/N1 6-0 = 0111100	((354R – 120R) / 450R) * VREG1
	PRP/N1 6-0 = 0111101	((354R – 122R) / 450R) * VREG1
	PRP/N1 6-0 = 0111110	((354R - 124R) / 450R) * VREG1
	PRP/N1 6-0 = 0111111	((354R – 126R) / 450R) * VREG1
	PRP/N1 6-0 = 1000000	((354R – 128R) / 450R) * VREG1
	PRP/N1 6-0 = 1000001	((354R – 130R) / 450R) * VREG1
	PRP/N1 6-0 = 1000010	((354R - 132R) / 450R) * VREG1
	PRP/N1 6-0 = 1000011	((354R – 134R) / 450R) * VREG1
	PRP/N1 6-0 = 1000100	((354R – 136R) / 450R) * VREG1

	PRP/N1 6-0 = 1000101	((354R – 138R) / 450R) * VREG1
	PRP/N1 6-0 = 1000110	((354R – 140R) / 450R) * VREG1
	PRP/N1 6-0 = 1000111	((354R – 142R) / 450R) * VREG1
	PRP/N1 6-0 = 1001000	((354R – 144R) / 450R) * VREG1
	PRP/N1 6-0 = 1001001	((354R – 146R) / 450R) * VREG1
	PRP/N1 6-0 = 1001010	((354R – 148R) / 450R) * VREG1
	PRP/N1 6-0 = 1001011	((354R – 150R) / 450R) * VREG1
	PRP/N1 6-0 = 1001100	((354R - 152R) / 450R) * VREG1
	PRP/N1 6-0 = 1001101	((354R – 154R) / 450R) * VREG1
	PRP/N1 6-0 = 1001110	((354R – 156R) / 450R) * VREG1
	PRP/N1 6-0 = 1001111	((354R – 158R) / 450R) * VREG1
	PRP/N1 6-0 = 1010000	((354R – 160R) / 450R) * VREG1
	PRP/N1 6-0 = 1010001	((354R – 162R) / 450R) * VREG1
	PRP/N1 6-0 = 1010010	((354R – 164R) / 450R) * VREG1
	PRP/N1 6-0 = 1010011	((354R – 166R) / 450R) * VREG1
	PRP/N1 6-0 = 1010100	((354R – 168R) / 450R) * VREG1
	PRP/N1 6-0 = 1010101	((354R – 170R) / 450R) * VREG1
	PRP/N1 6-0 = 1010110	((354R – 172R) / 450R) * VREG1
	PRP/N1 6-0 = 1010111	((354R - 174R) / 450R) * VREG1
	PRP/N1 6-0 = 1011000	((354R – 176R) / 450R) * VREG1
	PRP/N1 6-0 = 1011001	((354R - 178R) / 450R) * VREG1
	PRP/N1 6-0 = 1011010	((354R – 180R) / 450R) * VREG1
	PRP/N1 6-0 = 1011011	((354R – 182R) / 450R) * VREG1
	PRP/N1 6-0 = 1011100	((354R - 184R) / 450R) * VREG1
	PRP/N1 6-0 = 1011101	((354R – 186R) / 450R) * VREG1
	PRP/N1 6-0 = 1011110	((354R - 188R) / 450R) * VREG1
	PRP/N1 6-0 = 1011111	((354R – 190R) / 450R) * VREG1
	PRP/N1 6-0 = 1100000	((354R – 192R) / 450R) * VREG1
	PRP/N1 6-0 = 1100001	((354R - 194R) / 450R) * VREG1
	PRP/N1 6-0 = 1100010	((354R – 196R) / 450R) * VREG1
	PRP/N1 6-0 = 1100011	((354R - 198R) / 450R) * VREG1
	PRP/N1 6-0 = 1100100	((354R – 200R) / 450R) * VREG1
	PRP/N1 6-0 = 1100101	((354R – 202R) / 450R) * VREG1
	PRP/N1 6-0 = 1100110	((354R - 204R) / 450R) * VREG1
	PRP/N1 6-0 = 1100111	((354R – 206R) / 450R) * VREG1
	PRP/N1 6-0 = 1101000	((354R - 208R) / 450R) * VREG1
	PRP/N1 6-0 = 1101001	((354R – 210R) / 450R) * VREG1
	PRP/N1 6-0 = 1101010	((354R – 212R) / 450R) * VREG1
	PRP/N1 6-0 = 1101011	((354R - 214R) / 450R) * VREG1
	PRP/N1 6-0 = 1101100	((354R – 216R) / 450R) * VREG1
	PRP/N1 6-0 = 1101101	((354R - 218R) / 450R) * VREG1
	PRP/N1 6-0 = 1101110	((354R – 220R) / 450R) * VREG1
	PRP/N1 6-0 = 1101111	((354R – 222R) / 450R) * VREG1
	PRP/N1 6-0 = 1110000	((354R - 224R) / 450R) * VREG1
	PRP/N1 6-0 = 1110001	((354R – 226R) / 450R) * VREG1
	PRP/N1 6-0 = 1110010	((354R - 228R) / 450R) * VREG1
	PRP/N1 6-0 = 1110011	((354R – 230R) / 450R) * VREG1
	PRP/N1 6-0 = 1110100	((354R – 232R) / 450R) * VREG1
	PRP/N1 6-0 = 1110101	((354R - 234R) / 450R) * VREG1
	PRP/N1 6-0 = 1110110	((354R – 236R) / 450R) * VREG1
	PRP/N1 6-0 = 1110111	((354R - 238R) / 450R) * VREG1
	PRP/N1 6-0 = 1111000	((354R – 240R) / 450R) * VREG1
	PRP/N1 6-0 = 1111001	((354R – 242R) / 450R) * VREG1
	PRP/N1 6-0 = 1111010	((354R - 244R) / 450R) * VREG1
	PRP/N1 6-0 = 1111011	((354R – 246R) / 450R) * VREG1
	PRP/N1 6-0 = 1111100	((354R - 248R) / 450R) * VREG1
	PRP/N1 6-0 = 1111101	((354R – 250R) / 450R) * VREG1
	PRP/N1 6-0 = 1111110	((354R – 252R) / 450R) * VREG1
	PRP/N1 6-0 = 1111111	((354R - 254R) / 450R) * VREG1

Table 7.11 VinP/N 8

Reference Voltage	Macro Adjustment Value	VinP/N3 Formula
VinP/N3	PKP/N0 4-0 = 00000	(31R / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00001	((31R – 1R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00010	((31R – 2R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00011	((31R – 3R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00100	((31R – 4R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00101	((31R – 5R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00110	((31R – 6R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00111	((31R – 7R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01000	((31R – 8R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01001	((31R – 9R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01010	((31R - 10R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01011	((31R - 11R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01100	((31R - 12R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01101	((31R - 13R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01110	((31R - 14R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01111	((31R - 15R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10000	((31R - 16R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10001	((31R - 17R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10010	((31R - 18R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10011	((31R - 19R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10100	((31R - 20R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10101	((31R - 21R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10110	((31R - 22R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10111	((31R - 23R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11000	((31R - 24R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11001	((31R - 25R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11010	((31R - 26R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11011	((31R - 27R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11100	((31R - 28R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11101	((31R - 29R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11110	((31R - 30R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11111	((31R - 31R) / 32R) * (VinP/N2 - VinP/N4) + VinP/N4

Table 7.12 VinP/N 3

Reference Voltage	Macro Adjustment Value	VinP/N5 Formula
VinP/N5	PKP/N1 4-0 = 00000	(193R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00001	((193R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00010	((193R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00011	((193R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N14-0 = 00100	((193R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00101	((193R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00110	((193R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 00111	((193R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01000	((193R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01001	((193R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01010	((193R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01011	((193R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01100	((193R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01101	((193R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01110	((193R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 01111	((193R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10000	((193R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10001	((193R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10010	((193R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10011	((193R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10100	((193R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10101	((193R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10110	((193R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 10111	((193R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11000	((193R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11001	((193R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11010	((193R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11011	((193R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11100	((193R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11101	((193R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11110	((193R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N1 4-0 = 11111	((193R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7.13 VinP/N 5

Reference Voltage	Macro Adjustment Value	VinP/N6 Formula
VinP/N6	PKP/N2 4-0 = 00000	(158R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00001	((158R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00010	((158R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00011	((158R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00100	((158R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00101	((158R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00110	((158R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00111	((158R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01000	((158R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01001	((158R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01010	((158R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01011	((158R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01100	((158R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01101	((158R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01110	((158R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01111	((158R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10000	((158R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10001	((158R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10010	((158R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10011	((158R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10100	((158R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10101	((158R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10110	((158R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10111	((158R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11000	((158R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11001	((158R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11010	((158R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11011	((158R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11100	((158R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11101	((158R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11110	((158R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11111	((158R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7.14 VinP/N 6

Reference Voltage	Macro Adjustment Value	VinP/N7 Formula
VinP/N7	PKP/N3 4-0 = 00000	(123R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00001	((123R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00010	((123R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00011	((123R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00100	((123R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00101	((123R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00110	((123R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00111	((123R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01000	((123R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01001	((123R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01010	((123R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01011	((123R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01100	((123R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01101	((123R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01110	((123R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01111	((123R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10000	((123R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10001	((123R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10010	((123R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10011	((123R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10100	((123R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10101	((123R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10110	((123R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10111	((123R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11000	((123R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11001	((123R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11010	((123R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11011	((123R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11100	((123R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11101	((123R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11110	((123R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11111	((123R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7.15 VinP/N 7

Reference Voltage	Macro Adjustment Value	VinP/N9 Formula
VinP/N9	PKP/N4 4-0 = 00000	(31R / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00001	((31R - 1R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00010	((31R - 2R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00011	((31R - 3R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00100	((31R - 4R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00101	((31R - 5R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00110	((31R - 6R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00111	((31R - 7R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01000	((31R - 8R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01001	((31R - 9R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01010	((31R - 10R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01011	((31R - 11R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01100	((31R - 12R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01101	((31R - 13R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01110	((31R - 14R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01111	((31R - 15R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10000	((31R - 16R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10001	((31R - 17R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10010	((31R - 18R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10011	((31R - 19R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10100	((31R - 20R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10101	((31R - 21R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10110	((31R - 22R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10111	((31R - 23R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11000	((31R - 24R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11001	((31R - 25R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11010	((31R - 26R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11011	((31R - 27R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11100	((31R - 28R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11101	((31R - 29R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11110	((31R - 30R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11111	((31R - 31R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10

Table 7.16 VinP/N 9

Grayscale Voltage	Formula
V0	VinP0
V1	VinP1
V2	VinP2
V3	VinP3
V4	VinP4+ (VinP3 - VinP4)*CT1
V5	VinP4+ (VinP3 - VinP4)*CT2
V6	VinP4+ (VinP3 - VinP4)*CT3
V7	VinP4+ (VinP3 - VinP4)*CT4
V8	VinP4
V9	VinP5+(VinP4- VinP5)*(22R/24R)
V10	VinP5+(VinP4- VinP5)*(20R/24R)
V11	VinP5+(VinP4- VinP5)*(18R/24R)
V12	VinP5+(VinP4- VinP5)*(16R/24R)
V13	VinP5+(VinP4- VinP5)*(14R/24R)
V14	VinP5+(VinP4- VinP5)*(12R/24R)
V15	VinP5+(VinP4- VinP5)*(10R/24R)
V16	VinP5+(VinP4- VinP5)*(8R/24R)
V17	VinP5+(VinP4- VinP5)*(6R/24R)
V18	VinP5+(VinP4- VinP5)*(4R/24R)
V19	VinP5+(VinP4- VinP5)*(2R/24R)
V20	VinP5
V21	VinP6+(VinP5- VinP6)*(22R/24R)
V22	VinP6+(VinP5- VinP6)*(20R/24R)
V23	VinP6+(VinP5- VinP6)*(18R/24R)
V24	VinP6+(VinP5- VinP6)*(16R/24R)
V25	VinP6+(VinP5- VinP6)*(14R/24R)
V26	VinP6+(VinP5- VinP6)*(12R/24R)
V27	VinP6+(VinP5- VinP6)*(10R/24R)
V28	VinP6+(VinP5- VinP6)*(8R/24R)
V29	VinP6+(VinP5- VinP6)*(6R/24R)
V30	VinP6+(VinP5- VinP6)*(4R/24R)
V31	VinP6+(VinP5- VinP6)*(2R/24R)

Grayscale Voltage	Formula
V32	VinP6
V33	VinP7+(VinP6- VinP7)*(20R/22R)
V34	VinP7+(VinP6- VinP7)*(18R/22R)
V35	VinP7+(VinP6- VinP7)*(16R/22R)
V36	VinP7+(VinP6- VinP7)*(14R/22R)
V37	VinP7+(VinP6- VinP7)*(12R/22R)
V38	VinP7+(VinP6- VinP7)*(10R/22R)
V39	VinP7+(VinP6- VinP7)*(8R/22R)
V40	VinP7+(VinP6- VinP7)*(6R/22R)
V41	VinP7+(VinP6- VinP7)*(4R/22R)
V42	VinP7+(VinP6- VinP7)*(2R/22R)
V43	VinP7
V44	VinP8+(VinP7- VinP8)*(22R/24R)
V45	VinP8+(VinP7- VinP8)*(20R/24R)
V46	VinP8+(VinP7- VinP8)*(18R/24R)
V47	VinP8+(VinP7- VinP8)*(16R/24R)
V48	VinP8+(VinP7- VinP8)*(14R/24R)
V49	VinP8+(VinP7- VinP8)*(12R/24R)
V50	VinP8+(VinP7- VinP8)*(10R/24R)
V51	VinP8+(VinP7- VinP8)*(8R/24R)
V52	VinP8+(VinP7- VinP8)*(6R/24R)
V53	VinP8+(VinP7- VinP8)*(4R/24R)
V54	VinP8+(VinP7- VinP8)*(2R/24R)
V55	VinP8
V56	VinP9+ (VinP8 – VinP9)*CB1
V57	VinP9+ (VinP8 – VinP9)*CB2
V58	VinP9+ (VinP8 – VinP9)*CB3
V59	VinP9+ (VinP8 – VinP9)*CB4
V60	VinP9
V61	VinP10
V62	VinP11
V63	VinP12

Table 7.17 Voltage calculation formula of 64-grayscale voltage (positive polarity)

CGMP0[1:0]	“00”	“01”	“10”	“11”
CT1	3/4	28/45	26/33	3/4
CT2	1/2	4/15	6/11	21/40
CT3	7/24	7/45	10/33	13/40
CT4	1/8	1/15	1/6	3/20

CGMP1[1:0]	“00”	“01”	“10”	“11”
CB1	4/5	18/19	44/47	17/20
CB2	3/5	50/57	40/47	27/40
CB3	2/5	15/19	35/47	19/40
CB4	1/5	23/57	28/47	1/4

Table 7.18 Voltage calculation formula of grayscale voltage V4~V7 and V56~V59

Grayscale Voltage	Formula
V63	VinN0
V62	VinN1
V61	VinN2
V60	VinN3
V59	VinN4+ (VinN3 - VinN4)*CT1
V58	VinN4+ (VinN3 - VinN4)*CT2
V57	VinN4+ (VinN3 - VinN4)*CT3
V56	VinN4+ (VinN3 - VinN4)*CT4
V55	VinN4
V54	VinN5+(VinN4- VinN5)*(22R/24R)
V53	VinN5+(VinN4- VinN5)*(20R/24R)
V52	VinN5+(VinN4- VinN5)*(18R/24R)
V51	VinN5+(VinN4- VinN5)*(16R/24R)
V50	VinN5+(VinN4- VinN5)*(14R/24R)
V49	VinN5+(VinN4- VinN5)*(12R/24R)
V48	VinN5+(VinN4- VinN5)*(10R/24R)
V47	VinN5+(VinN4- VinN5)*(8R/24R)
V46	VinN5+(VinN4- VinN5)*(6R/24R)
V45	VinN5+(VinN4- VinN5)*(4R/24R)
V44	VinN5+(VinN4- VinN5)*(2R/24R)
V43	VinN5
V42	VinN6+(VinN5- VinN6)*(20R/22R)
V41	VinN6+(VinN5- VinN6)*(18R/22R)
V40	VinN6+(VinN5- VinN6)*(16R/22R)
V39	VinN6+(VinN5- VinN6)*(14R/22R)
V38	VinN6+(VinN5- VinN6)*(12R/22R)
V37	VinN6+(VinN5- VinN6)*(10R/22R)
V36	VinN6+(VinN5- VinN6)*(8R/22R)
V35	VinN6+(VinN5- VinN6)*(6R/22R)
V34	VinN6+(VinN5- VinN6)*(4R/22R)
V33	VinN6+(VinN5- VinN6)*(2R/22R)
V32	VinN6

Grayscale Voltage	Formula
V31	VinN7+(VinN6- VinN7)*(22R/24R)
V30	VinN7+(VinN6- VinN7)*(20R/24R)
V29	VinN7+(VinN6- VinN7)*(18R/24R)
V28	VinN7+(VinN6- VinN7)*(16R/24R)
V27	VinN7+(VinN6- VinN7)*(14R/24R)
V26	VinN7+(VinN6- VinN7)*(12R/24R)
V25	VinN7+(VinN6- VinN7)*(10R/24R)
V24	VinN7+(VinN6- VinN7)*(8R/24R)
V23	VinN7+(VinN6- VinN7)*(6R/24R)
V22	VinN7+(VinN6- VinN7)*(4R/24R)
V21	VinN7+(VinN6- VinN7)*(2R/24R)
V20	VinN7
V19	VinN8+(VinN7- VinN8)*(22R/24R)
V18	VinN8+(VinN7- VinN8)*(20R/24R)
V17	VinN8+(VinN7- VinN8)*(18R/24R)
V16	VinN8+(VinN7- VinN8)*(16R/24R)
V15	VinN8+(VinN7- VinN8)*(14R/24R)
V14	VinN8+(VinN7- VinN8)*(12R/24R)
V13	VinN8+(VinN7- VinN8)*(10R/24R)
V12	VinN8+(VinN7- VinN8)*(8R/24R)
V11	VinN8+(VinN7- VinN8)*(6R/24R)
V10	VinN8+(VinN7- VinN8)*(4R/24R)
V9	VinN8+(VinN7- VinN8)*(2R/24R)
V8	VinN8
V7	VinN9+ (VinN8 – VinN9)*CB1
V6	VinN9+ (VinN8 – VinN9)*CB2
V5	VinN9+ (VinN8 – VinN9)*CB3
V4	VinN9+ (VinN8 – VinN9)*CB4
V3	VinN9
V2	VinN10
V1	VinN11
V0	VinN12

Table 7.19 Voltage calculation formula of 64-grayscale voltage (negative polarity)

CGMN1[1:0]	“00”	“01”	“10”	“11”
CT1	4/5	34/57	19/47	3/4
CT2	3/5	4/19	12/47	21/40
CT3	2/5	7/57	7/47	13/40
CT4	1/5	1/19	3/47	3/20

CGMN0[1:0]	“00”	“01”	“10”	“11”
CB1	7/8	14/15	5/6	17/20
CB2	17/24	38/45	23/33	27/40
CB3	1/2	11/15	5/11	19/40
CB4	1/4	17/45	7/33	1/4

Table 7.20 Voltage calculation formula of grayscale voltage V59~V56 and V7~V4

Relationship between GRAM data and output Level (“Normally White Panel”, GRAM data=0)

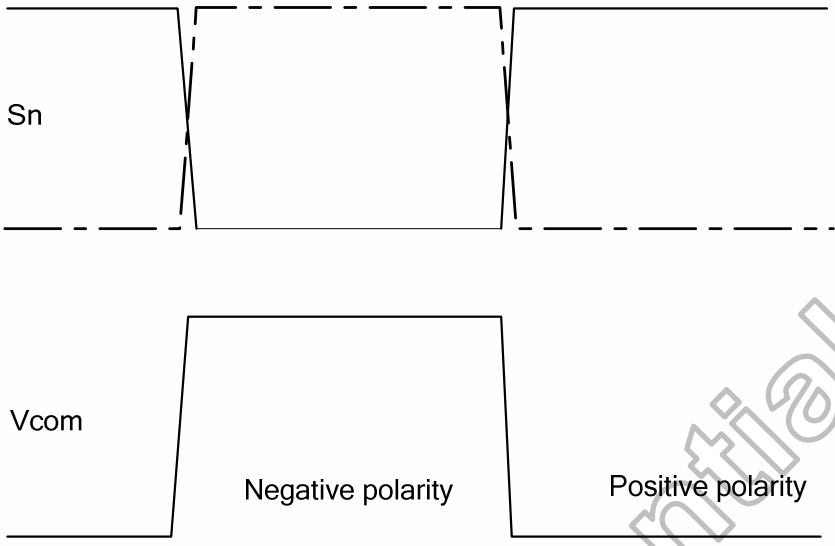
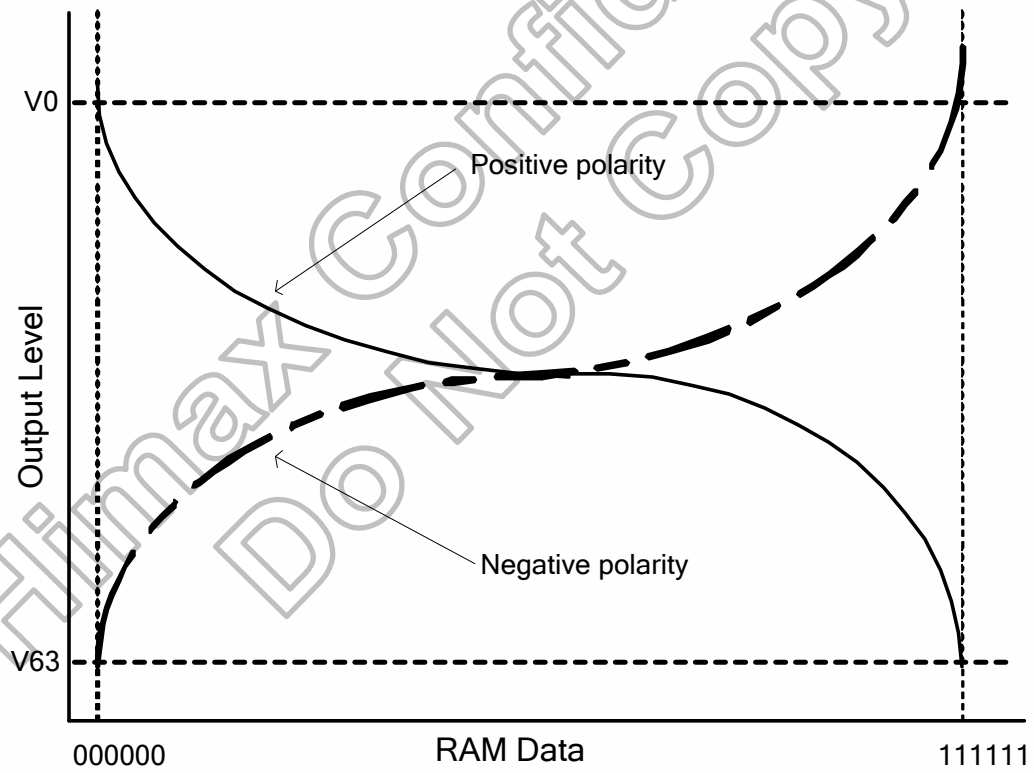


Figure 7.5 Relationship between source output and Vcom



(Same characteristic for each RGB)

Figure 7.6 Relationship between GRAM data and output level (normal white panel REV_Panel=“0”)

7.2.2 Gray voltage generator for digital gamma correction

The HX8367-A digital gamma correction can reach the independent GAMMA curve of RGB. HX8367-A utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 6-bit into 8-bit and sends 8-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the funcion.

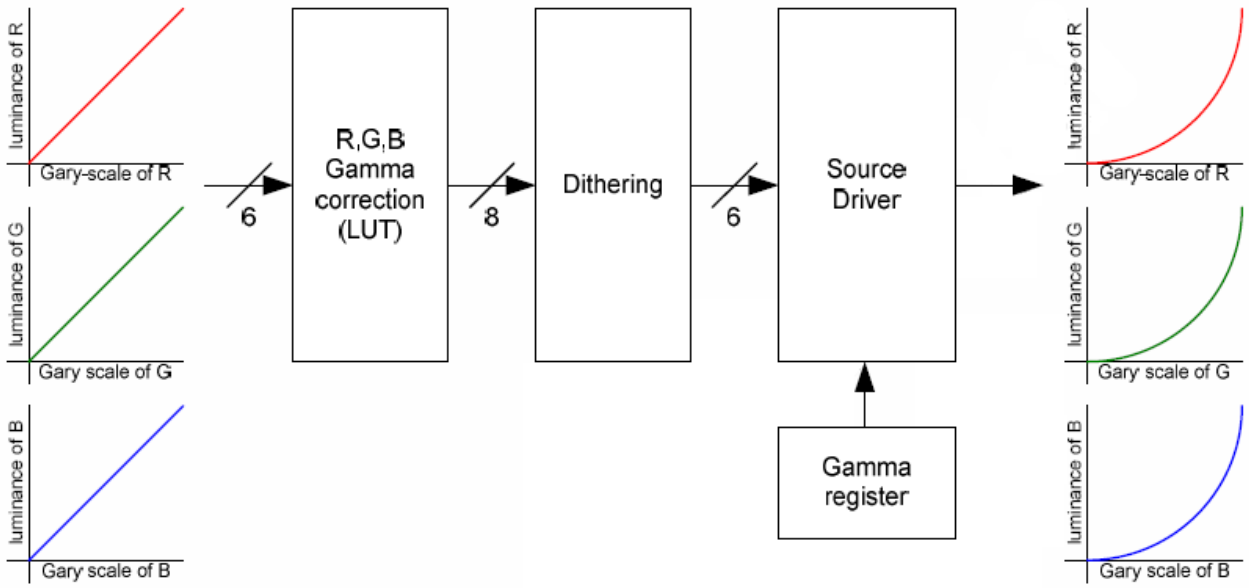


Figure 7.7 Block diagram of digital gamma correction

The HX8367-A builds one 99-bytes LUT (Look up table) to transfer every display data of Dithering circuit input and setting by DGC_LUT registers.

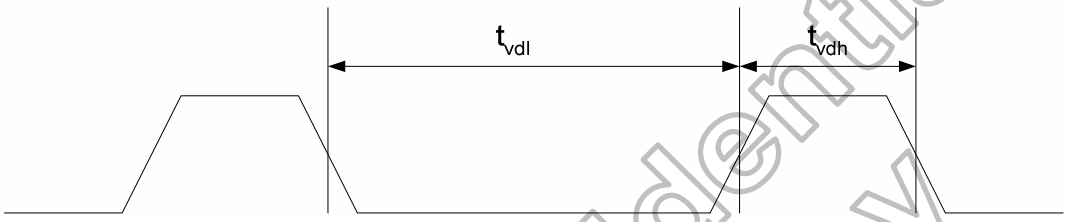
7.3 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing effect function is not support when at RGB interface (RCM[1:0]="1x").

7.3.1 Tearing effect line modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Figure 7.8 TE mode 1 output

Under Mode1, the TE output timing will be defined by TSEL[15:0] setting.
Ex: 1. TSEL[15:0]=0, then TE signal will output after last Line finished.
2. TSEL[15:0]=2, then TE signal will output at second Line start.

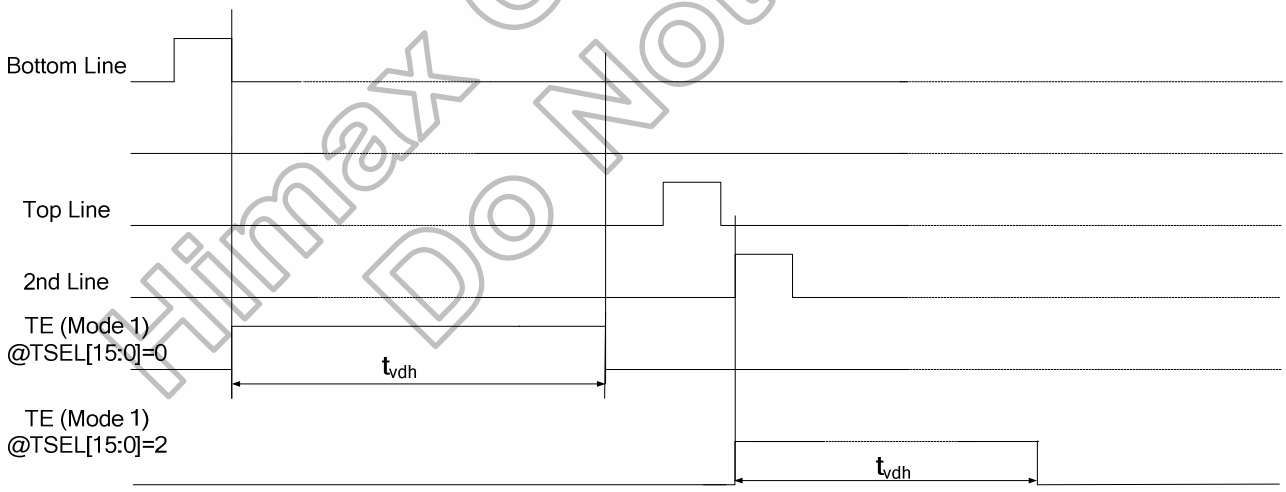
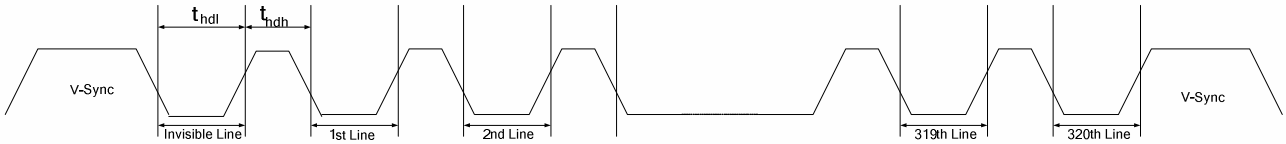


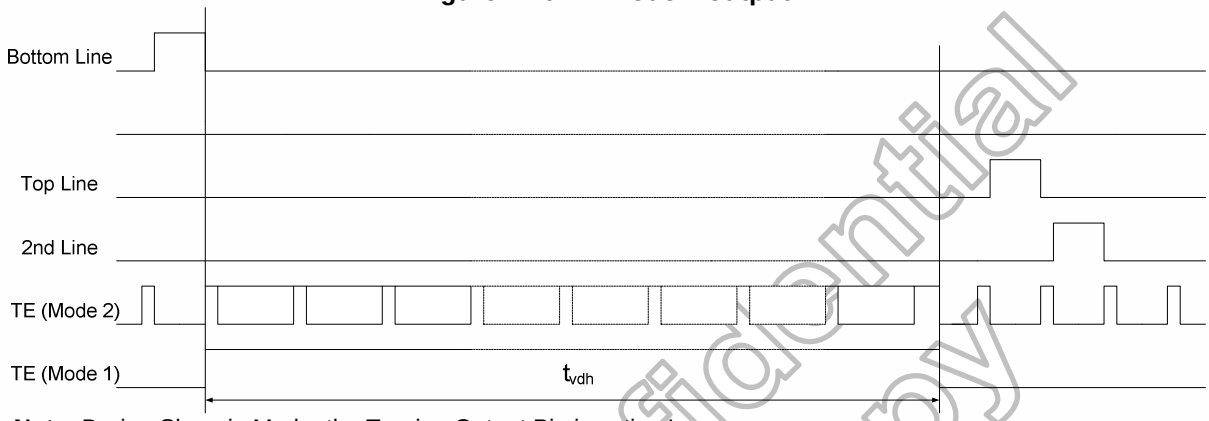
Figure 7.9 TE delay output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Figure 7.10 TE mode 2 output



Note: During Sleep in Mode, the Tearing Output Pin is active Low

Figure 7.11 TE output waveform

7.3.2 Tearing effect line timing

The Tearing Effect signal is described below.

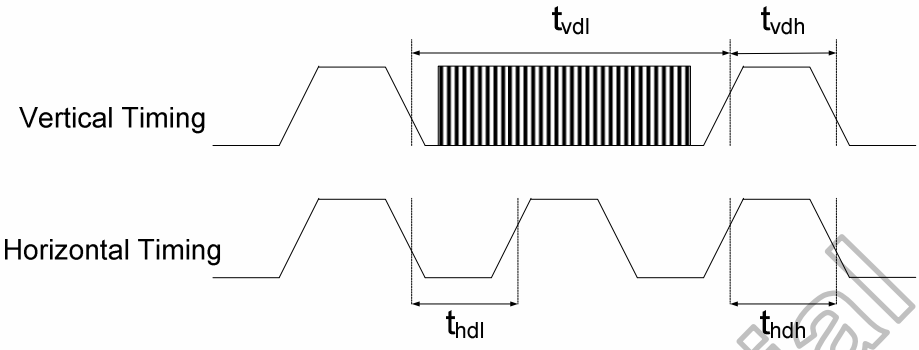


Figure 7.12 Waveform of tearing effect signal

Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Spec.			Unit	Description
		Min.	Typ.	Max.		
tvdl	Vertical Timing Low Duration	14.5	-	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	-	µs	-
thdl	Horizontal Timing Low Duration	43	-	-	µs	-
thdh	Horizontal Timing High Duration	1	-	500	µs	-

Table 7.21 AC characteristics of tearing effect signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

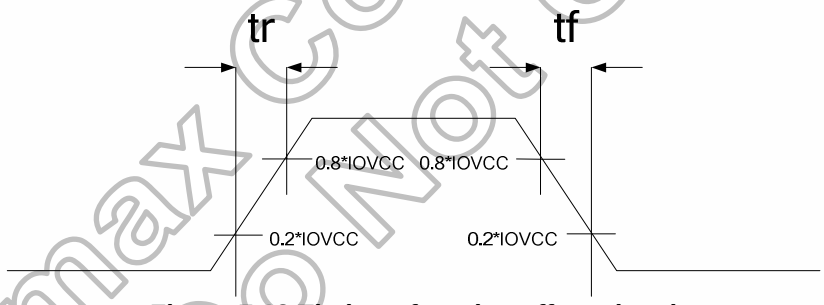


Figure 7.13 Timing of tearing effect signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

7.3.3 Example 1: MPU write is faster than panel read

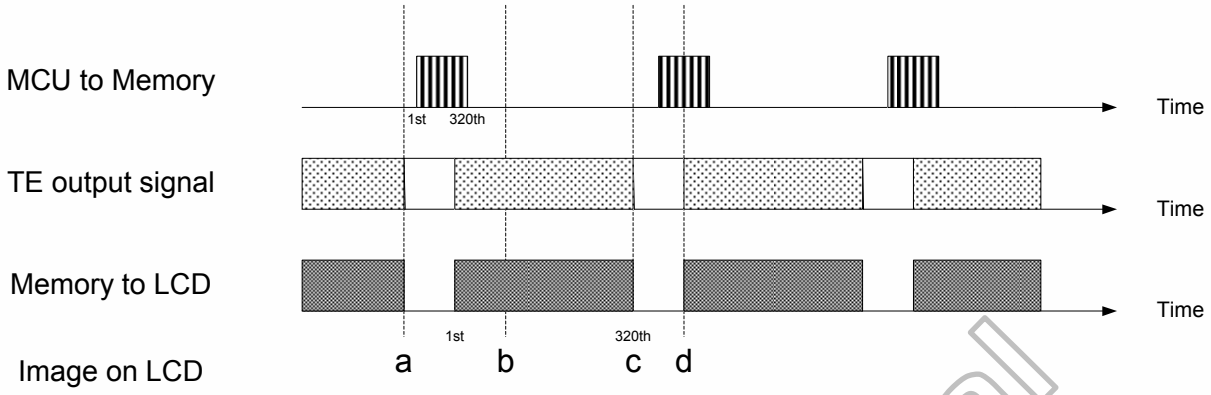


Figure 7.14 Timing of MPU write is faster than panel read

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image.

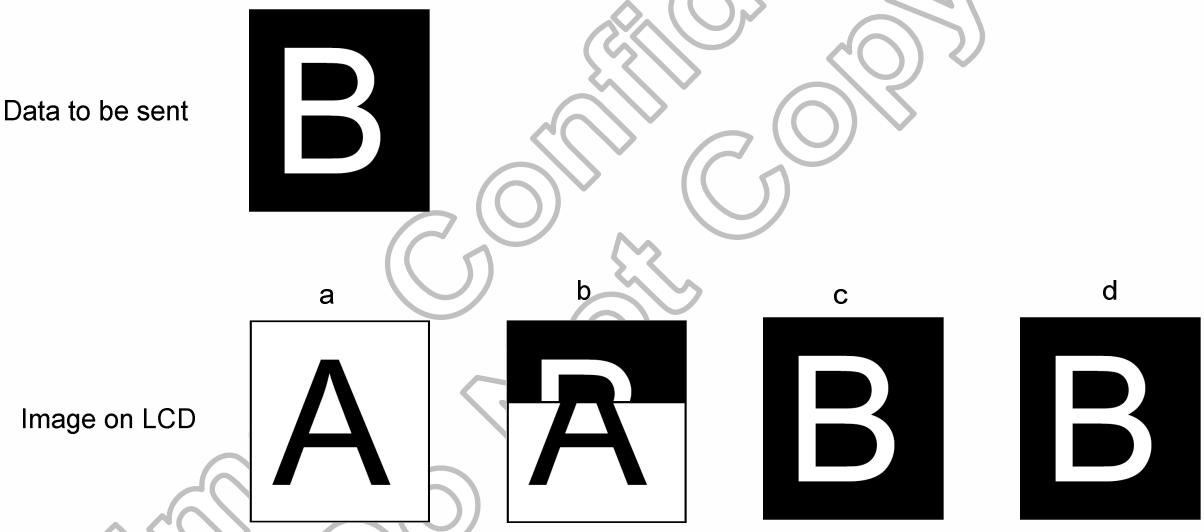


Figure 7.15 Display of MPU write is faster than panel read

7.3.4 Example 2: MPU write is slower than panel read

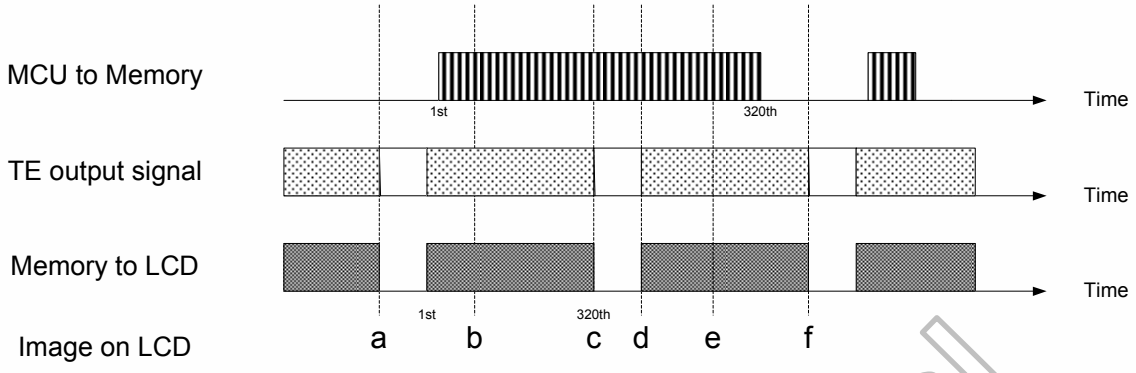


Figure 7.16 Timing of MPU write is slower than panel read

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

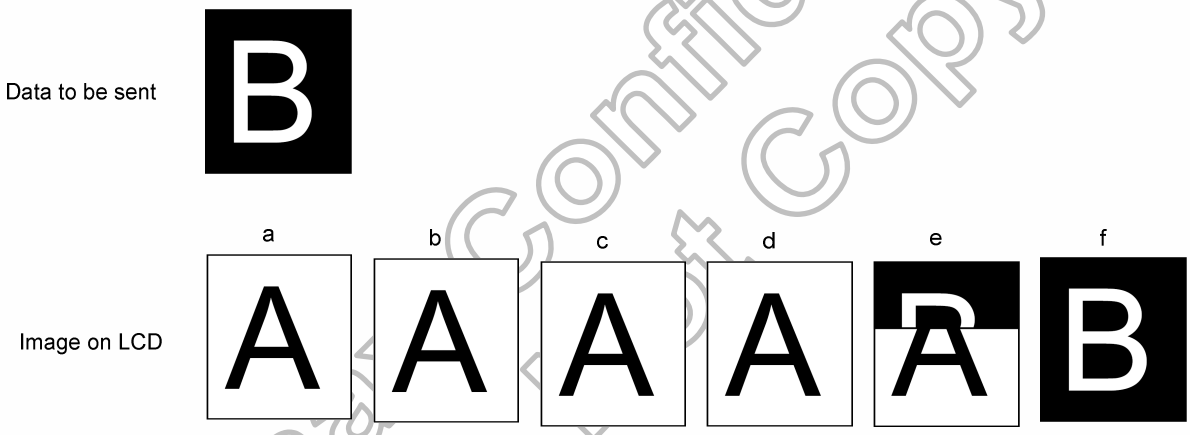


Figure 7.17 Display of MPU write is slower than panel read

7.4 Scan mode setting

The HX8367-A can set internal register GS_PANEL bit to determine the pin assignment of gate. The GS_PANEL setting allows changing the shift direction of gate outputs by connecting LCD panel with the HX8367-A.

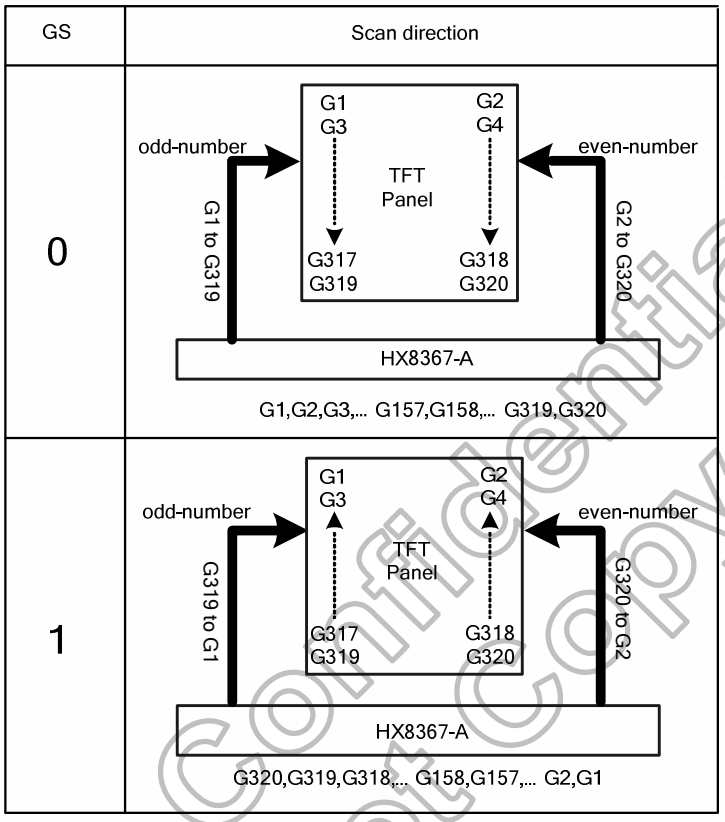


Figure 7.18 Gate scan mode

7.5 LCD power generation circuit

7.5.1 Power supply circuit

The power circuit of HX8367-A is used to generate supply voltages for LCD panel driving.

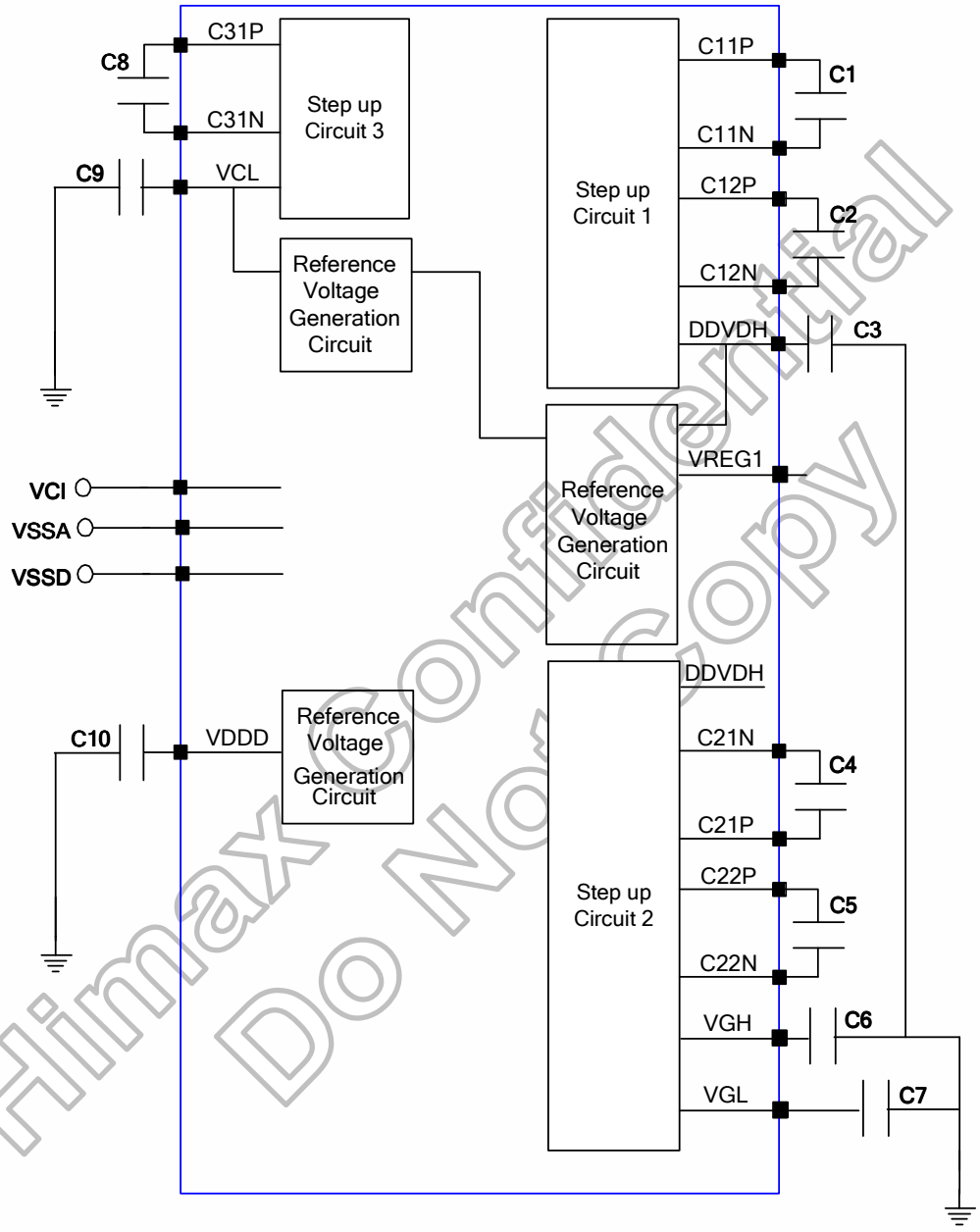


Figure 7.19 Block diagram of HX8367-A power circuit

Specification of connected passive component

Capacitor	Recommended voltage	Capacity
C1 (C11P/N)	6V	1 µF (B characteristics)
C2 (C12P/N)	6V	1 µF (B characteristics)
C3 (DDVDH)	10V	1 µF (B characteristics)
C4 (C21P/N)	10V	1 µF (B characteristics)
C5 (C22P/N)	10V	1 µF (B characteristics)
C6 (VGH)	25V	1 µF (B characteristics)
C7 (VGL)	16V	1 µF (B characteristics)
C8 (C31P/N)	6V	1 µF (B characteristics)
C9 (VCL)	6V	1 µF (B characteristics)
C10 (VDDD)	6V	1 µF (B characteristics)

Table 7.22 Adoptability of capacitor

7.5.2 LCD power generation scheme

The boost voltage generated is shown as below.

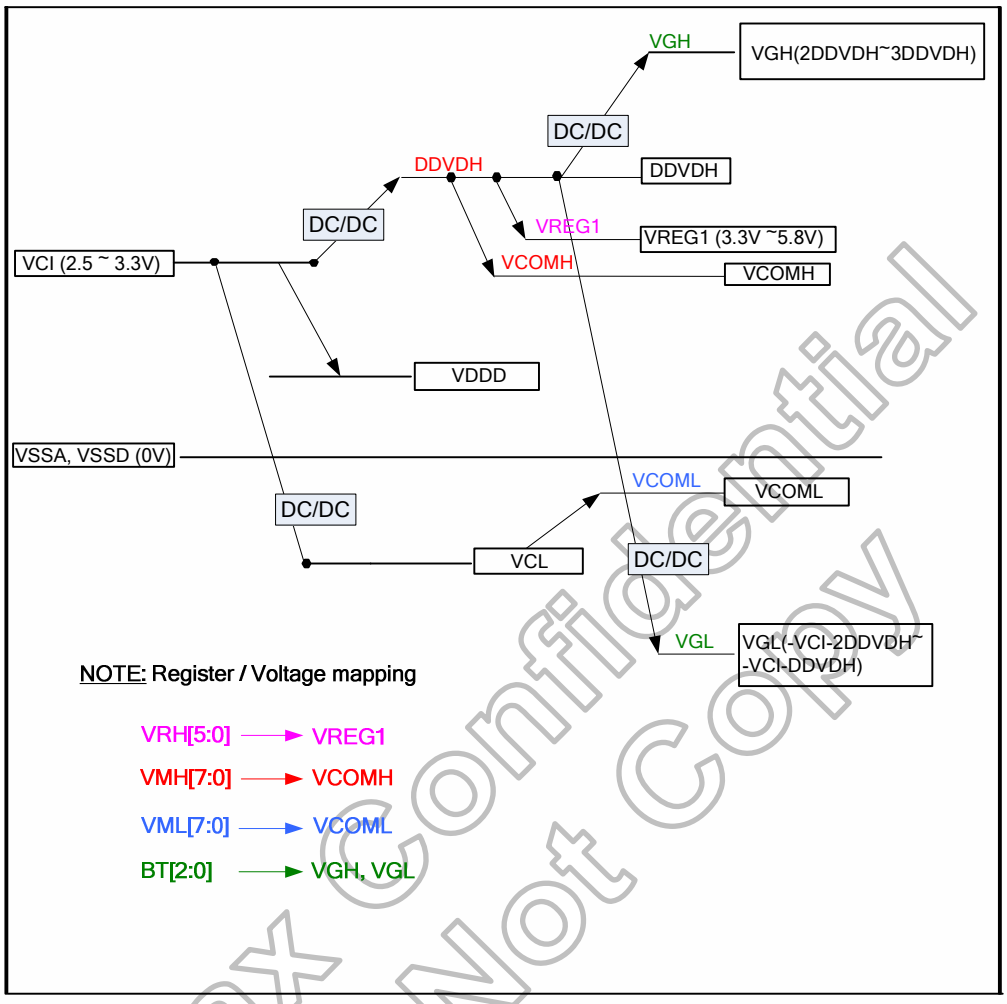


Figure 7.20 LCD power generation scheme

7.6 Power on/off sequence

The following are the sequences of register setting flow that applied to this driver driving the TFT display, when operate in Register-Content interface mode.

Display on/off set flow

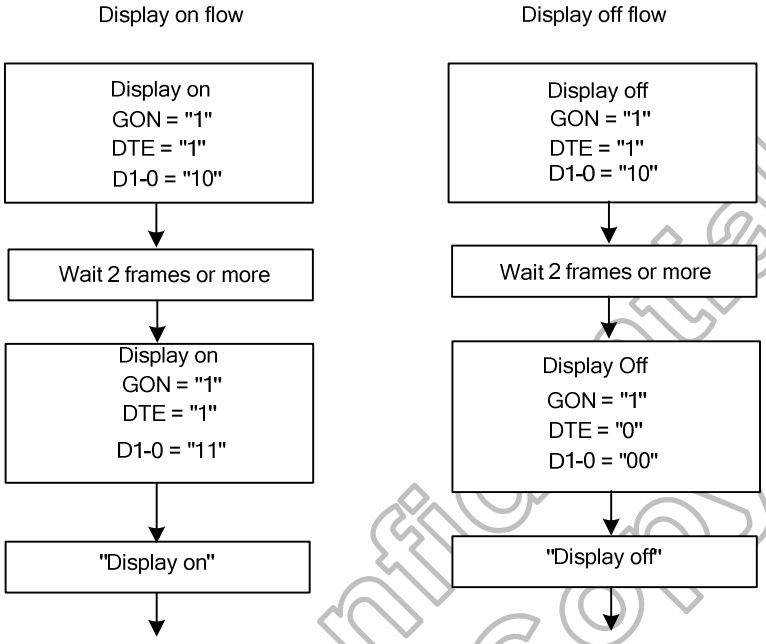


Figure 7.21 Display on/off set flow

Standby mode set up flow

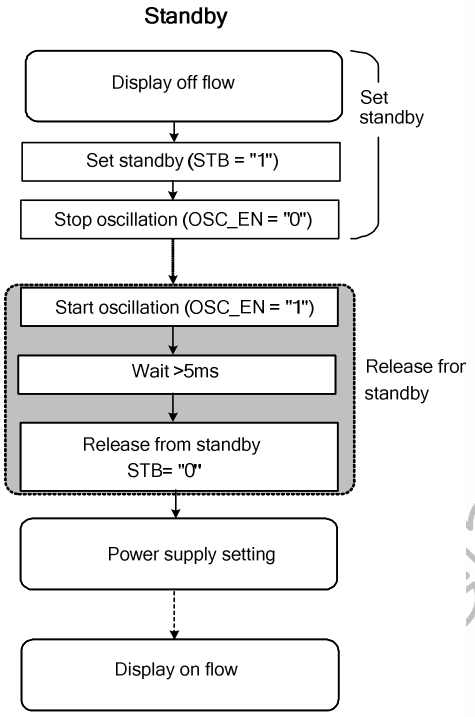


Figure 7.22 Standby mode setting flow

Deep standby mode set up flow

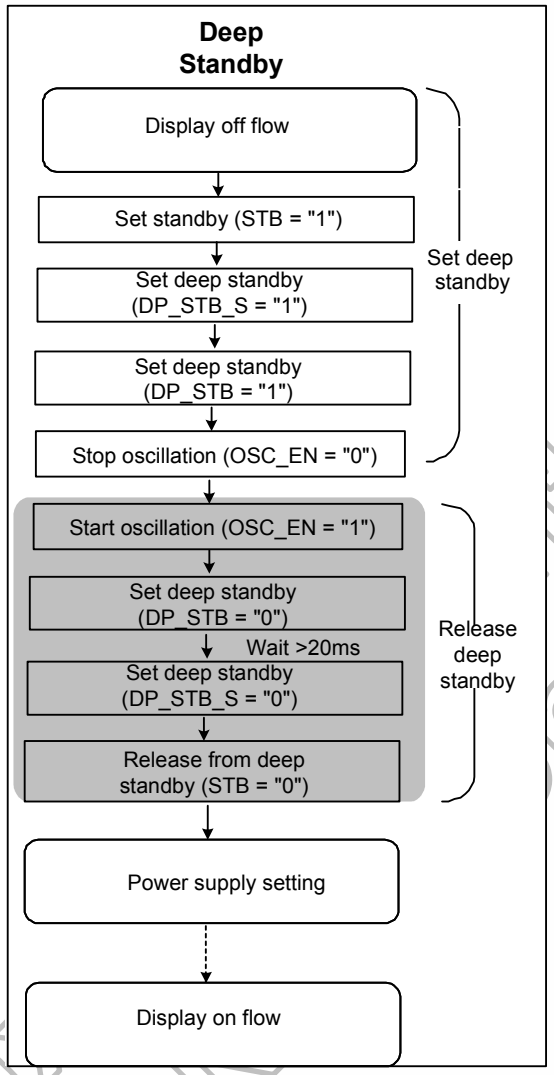


Figure 7.23 Deep standby mode setting flow

Power on/off setting up flow

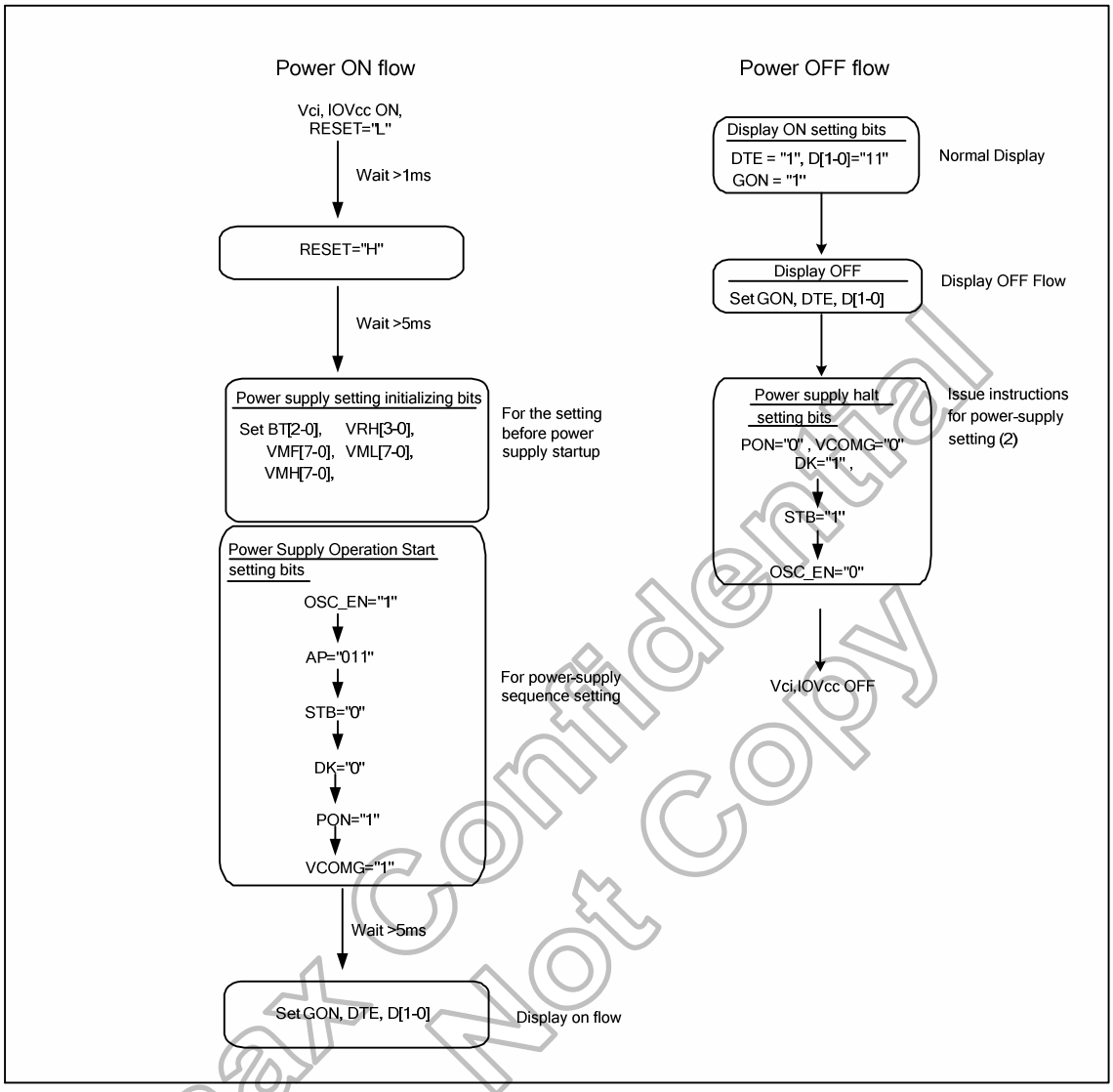


Figure 7.24 Power supply setting flow

7.7 Input/output pin state

7.7.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low

Table 7.23 Characteristics of output pins

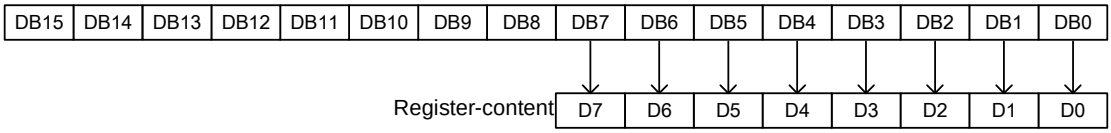
7.7.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
NRESET	Input valid	Input valid	Input valid	Input valid
NCS	Input invalid	Input valid	Input valid	Input invalid
NWR_SCL	Input invalid	Input valid	Input valid	Input invalid
NRD	Input invalid	Input valid	Input valid	Input invalid
DNC_SCL	Input invalid	Input valid	Input valid	Input invalid
SDI	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
DB[17:0]	Input invalid	Input valid	Input valid	Input invalid
OSC, IM3~0	Input invalid	Input valid	Input valid	Input invalid
TEST2-1	Input invalid	Input valid	Input valid	Input invalid

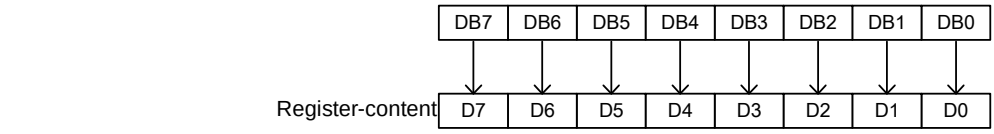
Table 7.24 Characteristics of input pins

8. Command

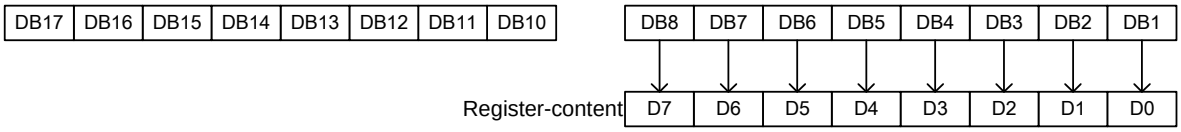
IM3~IM0 = "0000" 8080 MCU 16-bits Parallel type I



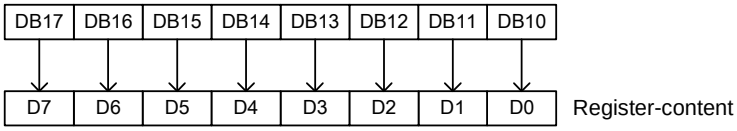
IM3~IM0 = "0001" 8080 MCU 8-bits Parallel type I



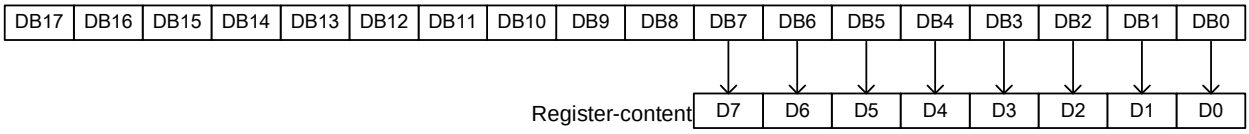
IM3~IM0 = "0010" 8080 MCU 16-bits Parallel type II



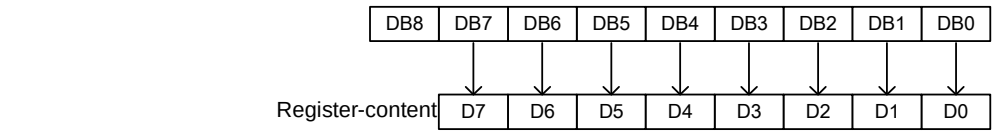
IM3~IM0 = "0011" 8080 MCU 8-bits Parallel type II



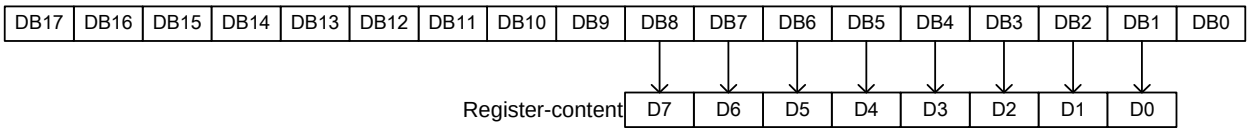
IM3~IM0 = "1000" 8080 MCU 18-bits Parallel type I



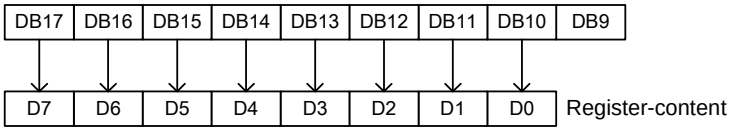
IM3~IM0 = "1001" 8080 MCU 9-bits Parallel type I



IM3~IM0 = "1010" 8080 MCU 18-bits Parallel type II



IM3~IM0 = "1011" 8080 MCU 9-bits Parallel type II



8.1 Command set

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R00h	Himax ID	R	-	0	1	1	0	0	1	1	1	
R01h	Display Mode control	W/R	-	DP_STB(0)	DP_STB_S(0)	-	-	SCROL(0)	IDMON(0)	INVON(0)	PTLON(0)	
R02h	Column address start 2	W/R	-	SC[15:8] (8'b0000_0000)								
R03h	Column address start 1	W/R	-	SC[7:0] (8'b0000_0000)								
R04h	Column address end 2	W/R	-	EC[15:8] (8'b0000_0000)								
R05h	Column address end 1	W/R	-	EC[7:0] (8'b1110_1111)								
R06h	Row address start 2	W/R	-	SP[15:8] (8'b0000_0000)								
R07h	Row address start 1	W/R	-	SP[7:0] (8'b0000_00000)								
R08h	Row address end 2	W/R	-	EP[15:8] (8'b0000_0001)								
R09h	Row address end 1	W/R	-	EP[7:0] (8'b0011_1111)								
R0Ah	Partial area start row 2	W/R	-	PSL[15:8] (8'b0000_0000)								
R0Bh	Partial area start row 1	W/R	-	PSL[7:0] (8'b0000_00000)								
R0Ch	Partial area end row 2	W/R	-	PEL[15:8] (8'b0000_0001)								
R0Dh	Partial area end row 1	W/R	-	PEL[7:0] (8'b0011_1111)								
R0Eh	Vertical Scroll Top fixed area 2	W/R	-	TFA[15:8] (8'b0000_0000)								
R0Fh	Vertical Scroll Top fixed area 1	W/R	-	TFA[7:0] (8'b0000_0000)								
R10h	Vertical Scroll height area 2	W/R	-	VSA[15:8] (8'b0000_0001)								
R11h	Vertical Scroll height area 1	W/R	-	VSA[7:0] (8'b0100_0000)								
R12h	Vertical Scroll Button area 2	W/R	-	BFA[15:8] (8'b0000_0000)								
R13h	Vertical Scroll Button area 1	W/R	-	BFA [7:0] (8'b0000_0000)								
R14h	Vertical Scroll Start address 2	W/R	-	VSP [15:8] (8'b0000_0000)								
R15h	Vertical Scroll Start address 1	W/R	-	VSP [7:0] (8'b0000_0000)								
R16h	Memory Access control	W/R	-	MY(0)	MX(0)	MV(0)	ML(0)	BGR(0)	-	-	-	
R17h	COLMOD	W/R	-	CSEL[3:0] (4b'0110)				-	IFPF[2:0] (3b'110)			
R18h	OSC Control 2	W/R	-	I_RADJ1[3:0] (3b'0011)				N_RADJ0[3:0](4b'0100)				*
R19h	OSC Control 1	W/R	-	-	-	-	-	-	-	-	OSC_EN(0)	
R1Ah	Power Control 1	W/R	-	-	-	-	-	-	BT[2:0] (001)			
R1Bh	Power Control 2	W/R	-	-	-	VRH[5:0] (01_1011)_4.8V						
R1Ch	Power Control 3	W/R	-	-	-	-	-	-	AP[2:0] (011)			
R1Dh	Power Control 4	W/R	-	-	I_FS0[2:0](100)			-	N_FS0[2:0](100)			
R1Eh	Power Control 5	W/R	-	-	I_FS1[2:0](100)			-	N_FS1[2:0](100)			
R1Fh	Power Control 6	W/R	-	GASEN(1)	VCOMG(0)	-	PON(0)	DK(1)	XDK(0)	DDVDH_TRI(0)	STB(1)	
R20h	Power Control 7	W/R	-	BLANK_FS1[3:0](0001)				BLANK_FS0[3:0](0001)				
R22h	SRAM Write Control	W/R	SRAM Write									
R23h	VCOM Control 1	W/R	-	VMF[7:0](1000_0000)								
R24h	VCOM Control 2	W/R	-	VMH[7:0](0010_1111)								
R25h	VCOM Control 3	W/R	-	VML[7:0](0101_0111)								
R26h	Display Control 1	W/R	-	--	-	-	-	ISC[3:0](0001)				

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R27h	Display Control 2	W/R	-	PT[1:0](10)		PTV[1:0](01)		-	-	PTG(1)	REF(1)	-
R28h	Display Control 3	W/R	-	-	-	GON(1)	DTE(0)	D[1:0] (00)		-	-	-
R29h	Frame Rate control 1	W/R	-	RTN[7:0](8'b0000_0010)								-
R2Ah	Frame Rate Control 2	W/R	-	-	-	I_DIV[1:0](00)		-	-	N_DIV[1:0](00)		-
R2Bh	Frame Rate Control 3	W/R	-	N_DUM[7:0] (8b'0001_1100)								-
R2Ch	Frame Rate Control 4	W/R	-	I_DUM[7:0] (8b'0001_1100)								-
R2Dh	Cycle Control 1	W/R	-	GDON[7:0] (8'b0000_1101)								-
R2Eh	Cycle Control 2	W/R	-	GDOF[7:0] (8'b0111_0000)								-
R2Fh	Display inversion	W/R	-	-	I_NW[2:0](3b'001)			-	N_NW[2:0] (3b'001)			-
R31h	RGB interface control 1	W/R	-	-	-	-	-	-	-	RCM[1:0](00)		-
R32h	RGB interface control 2	W/R	-	-	-	-	-	DPL (0)	HSPL (0)	VSPL (0)	EPL (0)	-
R33h	RGB interface control 3	W/R	-	HBP[7:0](8'b0000_1000)								-
R34h	RGB interface control 4	W/R	-	HBP[9:8](2'b00)		VBP[5:0](6'b00_0100)						-
R36h	Panel Characteristic	W/R	-	-	-	-	-	SS_PANEL (0)	GS_PANEL(0)I	REV_PANEL(0)	BGR_PANEL (0)	-
R38h	OTP Control 1	W/R	-	OTP_MASK[7:0] (8'h00)								-
R39h	OTP Control 2	W/R	-	OTP_INDEX[7:0] (8'h00)								-
R3Ah	OTP Control 3	W/R	-	OTP_LOAD_DISABLE(0)	DCCLK_DISABLE (0)	OTP_POR(0)	OTP_PWE(0)	OTP_PTM[1:0] (00)		VPP_SEL (0)	OTP_PROG(0)	-
R3Bh	OTP Control 4	R	-	OTP_DATA[7:0]								-
R40h	r1 Control (1)	W/R	-	-	-	VRP0[5:0] (6'b00_0001)						-
R41h	r1 Control (2)	W/R	-	-	-	VRP1[5:0] (6'b00_1110)						-
R42h	r1 Control (3)	W/R	-	-	-	VRP2[5:0] (6'b01_0001)						-
R43h	r1 Control (4)	W/R	-	-	-	VRP3[5:0] (6'b01_1010)						-
R44h	r1 Control (5)	W/R	-	-	-	VRP4[5:0] (6'b01_1000)						-
R45h	r1 Control (6)	W/R	-	-	-	VRP5[5:0] (6'b10_0100)						-
R46h	r1 Control (7)	W/R	-	-	PRP0[6:0] (7'b001_0101)							-
R47h	r1 Control (8)	W/R	-	-	PRP1[6:0] (7'b110_0101)							-
R48h	r1 Control (9)	W/R	-	-	-	-	PKP0[4:0] (5'b0_1011)					-
R49h	r1 Control (10)	W/R	-	-	-	-	PKP1[4:0] (5'b1_0100)					-
R4Ah	r1 Control (11)	W/R	-	-	-	-	PKP2[4:0] (5'b1_1001)					-
R4Bh	r1 Control (12)	W/R	-	-	-	-	PKP3[4:0] (5'b1_1010)					-
R4Ch	r1 Control (13)	W/R	-	-	-	-	PKP4[4:0] (5'b1_1000)					-
R50h	r1 Control (18)	W/R	-	-	-	VRN0[5:0] (6'b01_1011)						-
R51h	r1 Control (19)	W/R	-	-	-	VRN1[5:0] (6'b10_0111)						-
R52h	r1 Control (20)	W/R	-	-	-	VRN2[5:0] (6'b10_0101)						-
R53h	r1 Control (21)	W/R	-	-	-	VRN3[5:0] (6'b10_1110)						-
R54h	r1 Control (22)	W/R	-	-	-	VRN4[5:0] (6'b11_0001)						-
R55h	r1 Control (23)	W/R	-	-	-	VRN5[5:0] (6'b11_1110)						-
R56h	r1 Control (24)	W/R	-	-	PRN0[6:0] (7'b001_1010)							-
R57h	r1 Control (25)	W/R	-	-	PRN1[6:0] (7'b110_1010)							-
R58h	r1 Control (26)	W/R	-	-	-	PKN0[4:0] (5'b0_0111)						-
R59h	r1 Control (27)	W/R	-	-	-	PKN1[4:0] (5'b0_0101)						-
R5Ah	r1 Control (28)	W/R	-	-	-	PKN2[4:0] (5'b0_0110)						-
R5Bh	r1 Control (29)	W/R	-	-	-	PKN3[4:0] (5'b0_1011)						-
R5Ch	r1 Control (30)	W/R	-	-	-	PKN4[4:0] (5'b1_0100)						-
R5Dh	r1 Control (35)	W/R	-	CGMN1[1:0] (11)		CGMN0[1:0](00)		CGMP1[1:0](11)		CGMP0[1:0](00)		-
R60h	TE Control	W/R	-	-	-		TE_MODE(0)	TEON (0)		-	-	-
R61h	ID1	W/R	-	ID1[7:0](8'h00)								-
R62h	ID2	W/R	-	1	ID2[6:0](7'h00)							-
R63h	ID3	W/R	-	ID3[7:0](8'h00)								-
R84h	TE Output Line 2	W/R	-	TSEL[15:8](8'h00)								-
R85h	TE Output Line 1	W/R	-	TSEL[7:0](8'h00)								-
R87h	OTP Control 5	W/R	-	OTP_KEY[7:0] (8'h55)								-
RE8h	OPON Control 1	W/R	-	N_OPON[8'b0100_0000]								
RE9h	OPON Control 2	W/R	-	I_OPON[8'b0010_0000]								
REAh	PTBA Control 1	W/R	-	PTBA[15:8](8'b0000_0000)								

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
REBh	PTBA Control 2	W/R	-	PTBA[7:0](8'b0000_0000)								
RECh	STBA Control 1	W/R	-	STBA[15:8](8'b0000_0000)								
REDh	STBA Control 2	W/R	-	STBA[7:0](8'b0000_0000)								
RF1h	OTPS1B	W/R	-	-	-	-	-	-	-	-	OTPS1B(0)	
RF2h	GENON	W/R	-	GENON[7:0](8'b0010_0000)								
RFFh	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)		-

Table 8.1 List table of command set page 0

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R00h	DGC Control	W/R	-	-	-	-	-	-	-	-	DGC_EN(0)	-
R01h	DGC LUT1	W/R	-	DGC_LUT_R00(8'h00)								-
R02h	DGC LUT2	W/R	-	DGC_LUT_R01(8'h08)								-
R03h	DGC LUT3	W/R	-	DGC_LUT_R02(8'h10)								-
R04h	DGC LUT4	W/R	-	DGC_LUT_R03(8'h18)								-
R05h	DGC LUT5	W/R	-	DGC_LUT_R04(8'h20)								-
R06h	DGC LUT6	W/R	-	DGC_LUT_R05(8'h28)								-
R07h	DGC LUT7	W/R	-	DGC_LUT_R06(8'h30)								-
R08h	DGC LUT8	W/R	-	DGC_LUT_R07(8'h38)								-
R09h	DGC LUT9	W/R	-	DGC_LUT_R08(8'h40)								-
R0Ah	DGC LUT10	W/R	-	DGC_LUT_R09(8'h48)								-
R0Bh	DGC LUT11	W/R	-	DGC_LUT_R10(8'h50)								-
R0Ch	DGC LUT12	W/R	-	DGC_LUT_R11(8'h58)								-
R0Dh	DGC LUT13	W/R	-	DGC_LUT_R12(8'h60)								-
R0Eh	DGC LUT14	W/R	-	DGC_LUT_R13(8'h68)								-
R0Fh	DGC LUT15	W/R	-	DGC_LUT_R14(8'h70)								-
R10h	DGC LUT16	W/R	-	DGC_LUT_R15(8'h78)								-
R11h	DGC LUT17	W/R	-	DGC_LUT_R16(8'h80)								-
R12h	DGC LUT18	W/R	-	DGC_LUT_R17(8'h88)								-
R13h	DGC LUT19	W/R	-	DGC_LUT_R18(8'h90)								-
R14h	DGC LUT20	W/R	-	DGC_LUT_R19(8'h98)								-
R15h	DGC LUT21	W/R	-	DGC_LUT_R20(8'hA0)								-
R16h	DGC LUT22	W/R	-	DGC_LUT_R21(8'hA8)								-
R17h	DGC LUT23	W/R	-	DGC_LUT_R22(8'hB0)								-
R18h	DGC LUT24	W/R	-	DGC_LUT_R23(8'hB8)								-
R19h	DGC LUT25	W/R	-	DGC_LUT_R24(8'hC0)								-
R1Ah	DGC LUT26	W/R	-	DGC_LUT_R25(8'hC8)								-
R1Bh	DGC LUT27	W/R	-	DGC_LUT_R26(8'hD0)								-
R1Ch	DGC LUT28	W/R	-	DGC_LUT_R27(8'hD8)								-
R1Dh	DGC LUT29	W/R	-	DGC_LUT_R28(8'hE0)								-
R1Eh	DGC LUT30	W/R	-	DGC_LUT_R29(8'hE8)								-
R1Fh	DGC LUT31	W/R	-	DGC_LUT_R30(8'hF0)								-
R20h	DGC LUT32	W/R	-	DGC_LUT_R31(8'hF8)								-
R21h	DGC LUT33	W/R	-	DGC_LUT_R32(8'hFC)								-
R22h	DGC LUT34	W/R	-	DGC_LUT_G00(8'h00)								-
R23h	DGC LUT35	W/R	-	DGC_LUT_G01(8'h08)								-
R24h	DGC LUT36	W/R	-	DGC_LUT_G02(8'h10)								-
R25h	DGC LUT37	W/R	-	DGC_LUT_G03(8'h18)								-
R26h	DGC LUT38	W/R	-	DGC_LUT_G04(8'h20)								-
R27h	DGC LUT39	W/R	-	DGC_LUT_G05(8'h28)								-
R28h	DGC LUT40	W/R	-	DGC_LUT_G06(8'h30)								-
R29h	DGC LUT41	W/R	-	DGC_LUT_G07(8'h38)								-
R2Ah	DGC LUT42	W/R	-	DGC_LUT_G08(8'h40)								-
R2Bh	DGC LUT43	W/R	-	DGC_LUT_G09(8'h48)								-
R2Ch	DGC LUT44	W/R	-	DGC_LUT_G10(8'h50)								-
R2Dh	DGC LUT45	W/R	-	DGC_LUT_G11(8'h58)								-
R2Eh	DGC LUT46	W/R	-	DGC_LUT_G12(8'h60)								-
R2Fh	DGC LUT47	W/R	-	DGC_LUT_G13(8'h68)								-
R30h	DGC LUT48	W/R	-	DGC_LUT_G14(8'h70)								-
R31h	DGC LUT49	W/R	-	DGC_LUT_G15(8'h78)								-
R32h	DGC LUT50	W/R	-	DGC_LUT_G16(8'h80)								-
R33h	DGC LUT51	W/R	-	DGC_LUT_G17(8'h88)								-
R34h	DGC LUT52	W/R	-	DGC_LUT_G18(8'h90)								-
R35h	DGC LUT53	W/R	-	DGC_LUT_G19(8'h98)								-
R36h	DGC LUT54	W/R	-	DGC_LUT_G20(8'hA0)								-
R37h	DGC LUT55	W/R	-	DGC_LUT_G21(8'hA8)								-
R38h	DGC LUT56	W/R	-	DGC_LUT_G22(8'hB0)								-
R39h	DGC LUT57	W/R	-	DGC_LUT_G23(8'hB8)								-
R3Ah	DGC LUT58	W/R	-	DGC_LUT_G24(8'hC0)								-
R3Bh	DGC LUT59	W/R	-	DGC_LUT_G25(8'hC8)								-
R3Ch	DGC LUT60	W/R	-	DGC_LUT_G26(8'hD0)								-
R3Dh	DGC LUT61	W/R	-	DGC_LUT_G27(8'hD8)								-
R3Eh	DGC LUT62	W/R	-	DGC_LUT_G28(8'hE0)								-
R3Fh	DGC LUT63	W/R	-	DGC_LUT_G29(8'hE8)								-
R40h	DGC LUT64	W/R	-	DGC_LUT_G30(8'hF0)								-
R41h	DGC LUT65	W/R	-	DGC_LUT_G31(8'hF8)								-
R42h	DGC LUT66	W/R	-	DGC_LUT_G32(8'hFC)								-

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R43h	DGC LUT67	W/R	-	DGC_LUT_B00(8'h00)								-
R44h	DGC LUT68	W/R	-	DGC_LUT_B01(8'h08)								-
R45h	DGC LUT69	W/R	-	DGC_LUT_B02(8'h10)								-
R46h	DGC LUT70	W/R	-	DGC_LUT_B03(8'h18)								-
R47h	DGC LUT71	W/R	-	DGC_LUT_B04(8'h20)								-
R48h	DGC LUT72	W/R	-	DGC_LUT_B05(8'h28)								-
R49h	DGC LUT73	W/R	-	DGC_LUT_B06(8'h30)								-
R4Ah	DGC LUT74	W/R	-	DGC_LUT_B07(8'h38)								-
R4Bh	DGC LUT75	W/R	-	DGC_LUT_B08(8'h40)								-
R4Ch	DGC LUT76	W/R	-	DGC_LUT_B09(8'h48)								-
R4Dh	DGC LUT77	W/R	-	DGC_LUT_B10(8'h50)								-
R4Eh	DGC LUT78	W/R	-	DGC_LUT_B11(8'h58)								-
R4Fh	DGC LUT79	W/R	-	DGC_LUT_B12(8'h60)								-
R50h	DGC LUT80	W/R	-	DGC_LUT_B13(8'h68)								-
R51h	DGC LUT81	W/R	-	DGC_LUT_B14(8'h70)								-
R52h	DGC LUT82	W/R	-	DGC_LUT_B15(8'h78)								-
R53h	DGC LUT83	W/R	-	DGC_LUT_B16(8'h80)								-
R54h	DGC LUT84	W/R	-	DGC_LUT_B17(8'h88)								-
R55h	DGC LUT85	W/R	-	DGC_LUT_B18(8'h90)								-
R56h	DGC LUT86	W/R	-	DGC_LUT_B19(8'h98)								-
R57h	DGC LUT87	W/R	-	DGC_LUT_B20(8'hA0)								-
R58h	DGC LUT88	W/R	-	DGC_LUT_B21(8'hA8)								-
R59h	DGC LUT89	W/R	-	DGC_LUT_B22(8'hB0)								-
R5Ah	DGC LUT90	W/R	-	DGC_LUT_B23(8'hB8)								-
R5Bh	DGC LUT91	W/R	-	DGC_LUT_B24(8'hC0)								-
R5Ch	DGC LUT92	W/R	-	DGC_LUT_B25(8'hC8)								-
R5Dh	DGC LUT93	W/R	-	DGC_LUT_B26(8'hD0)								-
R5Eh	DGC LUT94	W/R	-	DGC_LUT_B27(8'hD8)								-
R5Fh	DGC LUT95	W/R	-	DGC_LUT_B28(8'hE0)								-
R60h	DGC LUT96	W/R	-	DGC_LUT_B29(8'hE8)								-
R61h	DGC LUT97	W/R	-	DGC_LUT_B30(8'hF0)								-
R62h	DGC LUT98	W/R	-	DGC_LUT_B31(8'hF8)								-
R63h	DGC LUT99	W/R	-	DGC_LUT_B32(8'hFC)								-
RFFh	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0](00)		-

Table 8.2 List table of command set page 1

8.2 Index register

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 8.1 Index register

Index register (IR) specifies the Index of register from R00h to RFFh. It sets the register number (ID7-0) in the range from 00000000b to 11111111b in binary form.

8.3 Himax ID register (PAGE0 -R00h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	1	1	0	0	1	1	1

Figure 8.2 Himax ID register (PAGE0 -00h)

This command is used to read this IC's ID code. The ID code of this IC is 67h.

8.4 Display mode control register (PAGE0 -01h)

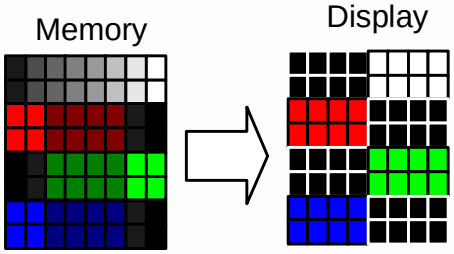
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	DP_STB	DP_STB_S	*	*	SCROLL	IDMON	INVON	PLTON
R	1	DP_STB	DP_STB_S	0	0	SCROLL	IDMON	INVON	PLTON

Figure 8.3 Display mode control register (PAGE0 -01h)

DP_STB, DP_STB_S : These two bits can let the driver into the deep standby mode. And when into deep standby, all display operation stops, including the internal R-C oscillator. In the deep standby mode, the GRAM data and register content are not retained. For details, please refer to "7.7 Power On/Off Sequence" section for detail use.

IDMON: This bit is Idle mode (8-color display mode) enable bit. **IDMON** = '1', chip will be into idle mode, and color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

(Idel Mode On Example)

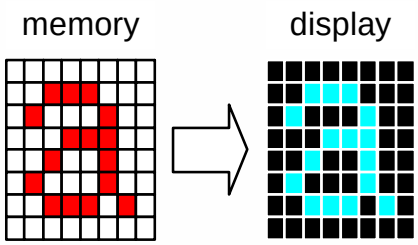


SCROLL : This bit turns on scroll mode by setting SCROLL = '1'. The scroll mode window is described by the Vertical Scroll Area command **TFA[15:0],**

VSA[15:0], BFA[15:0] and the Vertical start address **VSP[15:0]** (R0Eh~R15h). To leave scroll mode to normal mode, the **SCROLL** bit should be set to '0'.

INVON: This bit is display inversion mode enable bit. **INVON** = '1', chip will be into display inversion mode, and makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.

(Example)



PTLON: This command is used for turning on/off SCROLL mode by setting SCROLL=1/0. The scrolling mode window is described by the Partial Area command **PSL[15:0], PEL[15:0]** bits(R0Ah~R0Dh). To leave Partial mode to normal mode, the **PLTON** bit should be set to '0'.

8.5 Column address start register (PAGE0 -02~03h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8
R	1	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8

Figure 8.4 Column address start register upper byte (PAGE0 -02h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R	1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Figure 8.5 Column address start register low byte (PAGE0 -03h)

8.6 Column address end register (PAGE0 -04~05h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8
R	1	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8

Figure 8.6 Column address end register upper byte (PAGE0 -04h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Figure 8.7 Column address end register low byte (PAGE0 -05h)

8.7 Row address start register (PAGE0 -06~07h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8
R	1	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8

Figure 8.8 Row address start register upper byte (PAGE0 -06h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
R	1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Figure 8.9 Row address start register low byte (PAGE0 -07h)

8.8 Row address end register (PAGE0 -08~09h)

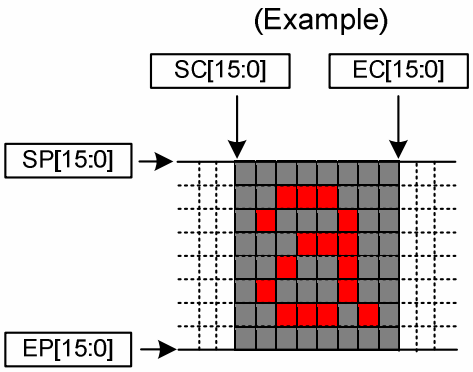
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8
R	1	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8

Figure 8.10 Row address end register upper byte (PAGE0 -08h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
R	1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

Figure 8.11 Row address end register low byte (PAGE0 -09h)

These commands (R02h~R09h) are used to define area of frame memory where MCU can access. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value of SC[15:0], EC[15:0] represents one column line in the Frame Memory. Each value of SP[15:0], EP[15:0] represents one page line in the Frame Memory.



8.9 Partial Area Start Row Register (PAGE0 -0A~0Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8
R	1	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8

Figure 8.12 Partial area start row register upper byte (PAGE0 -0Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0
R	1	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0

Figure 8.13 Partial area start row register low byte (PAGE0 -0Bh)

8.10 Partial Area End Row Register (PAGE0 -0C~0Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8
R	1	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8

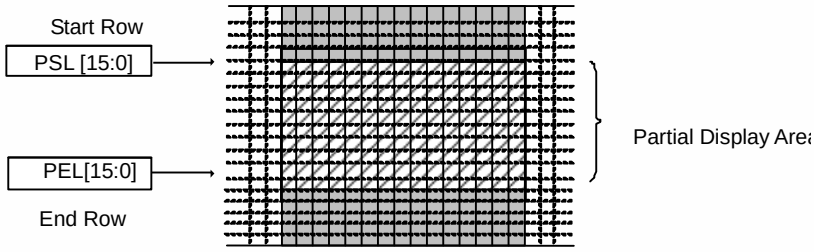
Figure 8.14 Partial area end row register upper byte (PAGE0 -0Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0
R	1	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0

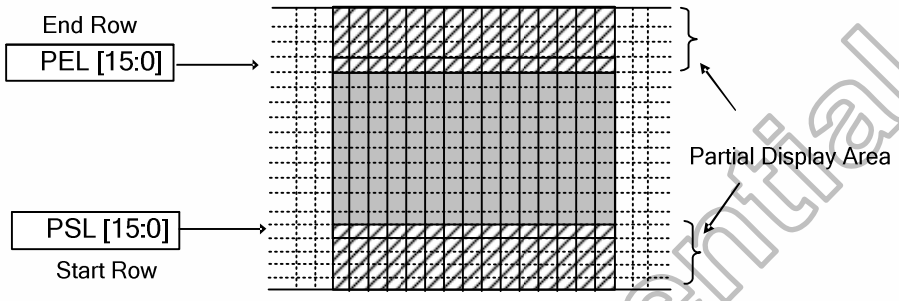
Figure 8.15 Partial area end row register low byte (PAGE0 -0Dh)

These commands (PAGE0 -0Ah~~0Dh) define the partial mode's display area. The Start Row (PSL) and the second the End Row (PEL) are illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

If End Row > Start Row



If End Row < Start Row



If End Row = Start Row then the Partial Area will be one row deep.

8.11 Vertical scroll top fixed area register (PAGE0 -0E~0Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8
R	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8

Figure 8.16 Vertical scroll top fixed area register upper byte (PAGE0 -0Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0
R	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0

Figure 8.17 Vertical scroll top fixed area register low byte (PAGE0 -0Fh)

8.12 Vertical scroll height area register (PAGE0 -10~11h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8
R	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8

Figure 8.18 Vertical scroll height area register upper byte (PAGE0 -10h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
R	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 8.19 Vertical scroll height area register low byte (PAGE0 -11h)

8.13 Vertical scroll button fixed area register (PAGE0 -12~13h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8
R	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8

Figure 8.20 Vertical scroll button fixed area register upper byte (PAGE0 -12h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0
R	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0

Figure 8.21 Vertical scroll button fixed area register low byte (PAGE0 -13h)

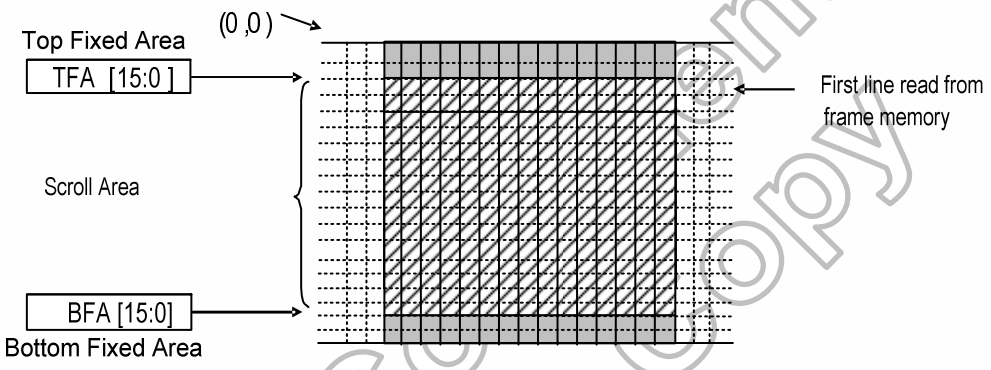
These commands (PAGE0 -0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display.

TFA[15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Please note that (TFA+VSA+BFA) must be set to '320d', otherwise Scrolling mode is undefined. In Vertical Scroll Mode, **MV** bit should be set to '0' – this only affects the Frame Memory Write.

8.14 Vertical scroll start address register (PAGE0 -14~15h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8
R	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8

Figure 8.22 Vertical Scroll Start Address Register Upper Byte (PAGE0 -14h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0
R	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0

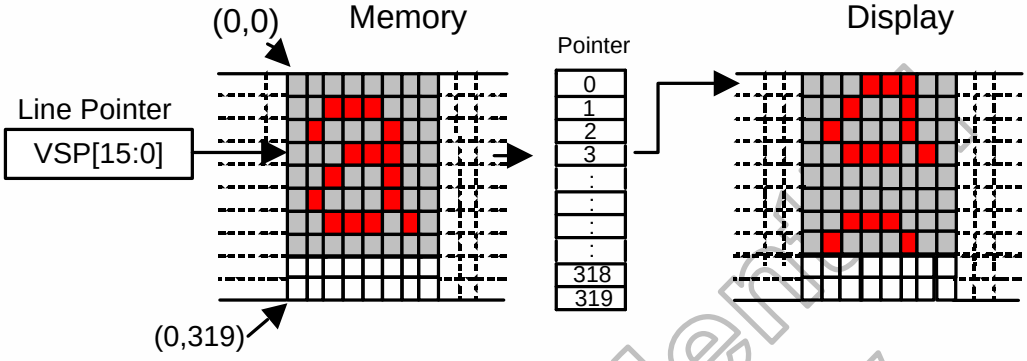
Figure 8.23 Vertical Scroll Start Address Register Low Byte (PAGE0 -15h)

VSP[15:0] is used together with Vertical Scrolling Definition register (PAGE0 -0Eh~R13h), which describe the scrolling area and the scrolling mode.

VSP[15:0] refers to the Frame Memory line Pointer, and describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

Example:
When Top Fixed Area TFA = ‘00d’, Bottom Fixed Area BFA = ‘02’d, Vertical Scrolling Area VSA = ‘318'd’ and VSP = ‘3d’ (**SS**=’0’, **GS**=’0’)

(Example)



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

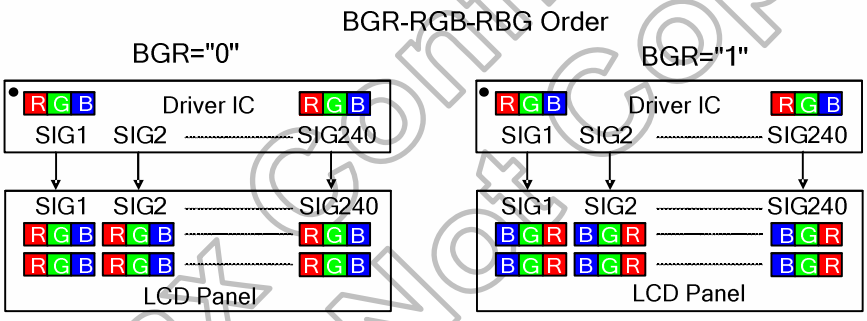
8.15 Memory access control register (PAGE0 -16h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	MY	MX	MV	ML	BGR	*	*	*
R	1	MY	MX	MV	ML	BGR	0	0	0

Figure 8.24 Memory access control register (PAGE0 -16h)

This command defines read/write scanning direction of frame memory. **MX, MY** bits also define the display direction in the RGB interface. This command makes no change on the other driver status. For details, please refer to “6.2.1 System interface to GRAM Write Direction” section.

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write direction. “MCU to memory write direction”
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
ML	Vertical ORDER	LCD vertical refresh direction control
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)



8.16 COLMOD control register (PAGE0 -17h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CSEL3	CSEL2	CSEL1	CSEL0	*	IFPF2	IFPF1	IFPF0
R	1	CSEL3	CSEL2	CSEL1	CSEL0	*	IFPF2	IFPF1	IFPF0

Figure 8.25 COLMOD control register (PAGE0 -17h)

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

System interface

Interface Format	IFPF2	IFPF1	IFPF0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
18 Bit/Pixel at 16-bits data bus interface (16+2)	1	1	1

RGB interface

Interface Format	CSEL3	CSEL2	CSEL1	CSEL0
16 Bit/Pixel	0	1	0	1
18 Bit/Pixel	0	1	1	0
6 Bit/Pixel	1	1	1	0
Not Defined	The Other Setting			

8.17 OSC control register (PAGE0 -18h & R19h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I_RADJ3	I_RADJ2	I_RADJ1	I_RADJ0	N_RADJ3	N_RADJ2	N_RADJ1	N_RADJ0
R	1	I_RADJ3	I_RADJ2	I_RADJ1	I_RADJ0	N_RADJ3	N_RADJ2	N_RADJ1	N_RADJ0

Figure 8.26 OSC control 1 register (PAGE0 -18h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	OSC_EN
R	1	0	0	0	0	0	0	0	OSC_EN

Figure 8.27 OSC control 2 register (PAGE0 -19h)

These commands are used to set internal oscillator related setting
OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop. In RGB interface mode (PAGE0 -RCM[1:0] = '10' or '11'), internal oscillator will be stop to oscillate and OSC_EN bit control is invalid.

N_RADJ[2:0]: Internal oscillator frequency adjusts in Normal / Partial mode.
I_RADJ[2:0]: Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.
For details, please refer to "7.1 Internal Oscillator" section.

RADJ3	RADJ2	RADJ1	RADJ0	Internal Oscillator Frequency	Display Frame rate
0	0	0	0	50% x 2.63MHz	30Hz
0	0	0	1	67% x 2.63MHz	40Hz
0	0	1	0	75% x 2.63MHz	45Hz
0	0	1	1	83% x 2.63MHz	50Hz
0	1	0	0	100% x2.63MHz	60Hz
0	1	0	1	108% x 2.63MHz	65Hz
0	1	1	0	117% x 2.63MHz	70Hz
0	1	1	1	125% x 2.63MHz	75Hz
1	0	0	0	100% x 2.63MHz	60Hz
1	0	0	1	133% x 2.63MHz	80Hz
1	0	1	0	150% x 2.63MHz	90Hz
1	0	1	1	167% x 2.63MHz	100Hz
1	1	0	0	200% x 2.63MHz	120Hz
1	1	0	1	217% x 2.63MHz	130Hz
1	1	1	0	233% x 2.63MHz	140Hz
1	1	1	1	250% x 2.63MHz	150Hz

8.18 Power control 1 register (PAGE0 -1Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	BT2	BT1	BT0
R	1	*	*	*	*	*	BT2	BT0	BT0

Figure 8.28 Power control 1 register (PAGE0 -1Ah)

BT[2:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	5.0V	-VCI	3DDVDH	-VCI-2DDVDH
0	0	1	5.0V	-VCI	3DDVDH	-2DDVDH
0	1	0	5.0V	-VCI	3DDVDH	VCI-2DDVDH
0	1	1	5.0V	-VCI	VCI+2DDVDH	-VCI-2DDVDH
1	0	0	5.0V	-VCI	VCI+2DDVDH	-2DDVDH
1	0	1	5.0V	-VCI	VCI+2DDVDH	VCI-2DDVDH
1	1	0	5.0V	-VCI	2DDVDH	-2DDVDH
1	1	1	5.0V	-VCI	2DDVDH	-VCI-DDVDH

Note: When VCI = 2.8V, DDVDH_TRI=0

BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	6.1V	-VCI	Setting inhabited	Setting inhabited
0	0	1	6.1V	-VCI	3DDVDH	-2DDVDH
0	1	0	6.1V	-VCI	3DDVDH	VCI-2DDVDH
0	1	1	6.1V	-VCI	VCI+2DDVDH	-VCI-2DDVDH
1	0	0	6.1V	-VCI	VCI+2DDVDH	-2DDVDH
1	0	1	6.1V	-VCI	VCI+2DDVDH	VCI-2DDVDH
1	1	0	6.1V	-VCI	2DDVDH	-2DDVDH
1	1	1	6.1V	-VCI	2DDVDH	-VCI-DDVDH

Note: When VCI = 2.8V, DDVDH_TRI=1

8.19 Power control 2 register (PAGE0 -1Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R	1	*	*	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 8.29 Power control 2 register (PAGE0 -1Bh)

VRH[4:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting.VREG1=Decimal(VRH[5:0])x0.05+3.3.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VREG1 (DDVDH_TRI=0)	VREG1 (DDVDH_TRI=1)
0	0	0	0	0	0	3.30	3.30
0	0	0	0	0	1	3.35	3.35
0	0	0	0	1	0	3.40	3.40
0	0	0	0	1	1	3.45	3.45
0	0	0	1	0	0	3.50	3.50
0	0	0	1	0	1	3.55	3.55
0	0	0	1	1	0	3.60	3.60
0	0	0	1	1	1	3.65	3.65
0	0	1	0	0	0	3.70	3.70
:	:	:	:	:	:	:	:
0	1	1	0	1	1	4.65	4.65
0	1	1	1	0	0	4.70	4.70
0	1	1	1	0	1	4.75	4.75
0	1	1	1	1	0	4.80	4.80
0	1	1	1	1	1	4.80	4.85
1	0	0	0	0	0	4.80	4.90
1	0	0	0	0	1	4.80	4.95
:	:	:	:	:	:	:	:
1	1	0	0	0	0	4.80	5.70
1	1	0	0	0	1	4.80	5.75
1	1	0	0	1	0	4.80	5.80
1	1	0	0	1	1	STOP	STOP
1	1	0	1	0	0	STOP	STOP
:	:	:	:	:	:	:	:
1	1	1	1	1	0	STOP	STOP
1	1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VREG1 input.	

Note: Internal VREF can be modified by Custom' s special request. default VREF=4.8 if DDVDH_TRI=0 and VREF=5.8 if DDVDH_TRI=1
VREG1={Decimal(VRH[5:0])x0.05+3.3 **}*(VREF/4.8) if** DDVDH_TRI=0.
VREG1={Decimal(VRH[5:0])x0.05+3.3 **}*(VREF/5.8) if** DDVDH_TRI=1.

8.20 Power control 3 register (PAGE0 -1Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	AP2	AP1	AP0
R	1	*	*	*	*	*	AP2	AP1	AP0

Figure 8.30 Power control 3 register (PAGE0 -1Ch)

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Small
0	1	0	Small
0	1	1	Small
1	0	0	Medium
1	0	1	Medium High
1	1	0	Large
1	1	1	Setting Inhibited

8.21 Power control 4~5 register (PAGE0 -1Dh~1Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I_FS02	I_FS01	I_FS00	*	N_FS02	N_FS01	N_FS00
R	1	*	I_FS02	I_FS01	I_FS00	*	N_FS02	N_FS01	N_FS00

Figure 8.31 Power control 4 register (PAGE0 -1Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I_FS12	I_FS11	I_FS10	*	N_FS12	N_FS11	N_FS10
R	1	*	I_FS12	I_FS11	I_FS10	*	N_FS12	N_FS11	N_FS10

Figure 8.32 Power control 5 register (PAGE0 -1Eh)

FS0[2:0]: Set the operating frequency for DDVDH and VCL voltage generation.
FS1[2:0]: Set the operating frequency for VGH and VGL voltage generation.
For details, please refer to “7.1 Internal Oscillator” section.

FS02	FS01	FS00	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

FS12	FS11	FS10	Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

8.22 Power control 6 register (PAGE0 -1Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GASEN	VCOMG	*	PON	DK	XDK	DDVDH_TRI	STB
R	1	GASEN	VCOMG	*	PON	DK	XDK	DDVDH_TRI	STB

Figure 8.33 Power control 6 register (PAGE0 -1Fh)

PON: Specify on/off control of step-up circuit 2 for VCL, VGL voltage generation. For detail, see the Power On/Off Setting Flow.

PON	Operation of step-up circuit 2
0	OFF
1	ON

DK: Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

STB: When **STB** = '1', the HX8367-A into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

a. Start the oscillation
b. Exit the Standby mode (STB = "0") ,

In the standby mode, the GRAM data and register content are retained.

XDK, DDVDH_TRI: Specify the ratio of step-up circuit for DDVDH voltage generation.

DDVDH_TRI	XDK	Step up circuit 1	Capacitor connection pins used
0	0	2 x VCI	C11P, C11N
0	1	2 x VCI	C11P, C11N, C12P, C12N
1	0	3 x VCI	C11P, C11N, C12P, C12N
1	1	Setting inhabited	Setting inhabited

VCOMG: When **VCOMG** = '1', VCOML voltage can output to negative voltage (1.0V ~ VCL+0.5V). When VCOMG = '0', VCOML outputs GND and **VML[7:0]** setting are invalid. Then, low power consumption is accomplished.

GASEN: This stands for abnormal power-off monitor function when the power is off.

8.23 Power control 7 register (PAGE0 -20h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BLANK_FS13	BLANK_FS12	BLANK_FS11	BLANK_FS10	BLANK_FS03	BLANK_FS02	BLANK_FS01	BLANK_FS00
R	1	BLANK_FS13	BLANK_FS12	BLANK_FS11	BLANK_FS10	BLANK_FS03	BLANK_FS02	BLANK_FS01	BLANK_FS00

Figure 8.34 Power control 7 register (PAGE0 -20h)

BLANK_FS0: Set the blanking frequency for DDVDH and VCL voltage generation.

BLANK_FS1: Set the blanking frequency for VGH and VGL voltage generation.

FS3	FS2	FS1	FS0	Blanking Frequency
0	0	0	0	1 line
0	0	0	1	4 line
0	0	1	0	8 line
0	0	1	1	12 line
:	:	:	:	:
1	1	1	0	56 line
1	1	1	1	60 line

8.24 Read data register (PAGE0 -22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
R	1	RD 17	RD 16	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 8.35 Read data register (PAGE0 -22h)

WD[17:0] : Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

RD[17:0]: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17–0) becomes invalid and the second-word read is normal.

8.25 VCOM control 1~3 register (PAGE0 -23~25h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VMF 7	VMF 6	VMF 5	VMF 4	VMF 3	VMF 2	VMF 1	VMF 0
R	1	VMF 7	VMF 6	VMF 5	VMF 4	VMF 3	VMF 2	VMF 1	VMF 0

Figure 8.36 Vcom control 1 register (PAGE0 -23h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0
R	1	VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0

Figure 8.37 Vcom control 2 register (PAGE0 -24h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VML 7	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0
R	1	VML 7	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0

Figure 8.38 Vcom control 3 register (PAGE0 -25h)

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage

VMH[7:0]: Set the VCOMH voltage (High level voltage of VCOM). VCOM High voltage = Decimal(VMH[7:0])x0.015+2.5.

VMH7	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	VCOMH (DDVDH_TRI=0)	VCOMH (DDVDH_TRI=1)
0	0	0	0	0	0	0	0	2.500	2.500
0	0	0	0	0	0	0	1	2.515	2.515
0	0	0	0	0	0	1	0	2.530	2.530
0	0	0	0	0	0	1	1	2.545	2.545
0	0	0	0	0	1	0	0	2.560	2.560
0	0	0	0	0	1	0	1	2.575	2.575
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
0	0	1	0	1	1	1	1	3.205	3.205
0	0	1	1	0	0	0	0	3.220	3.220
:	:	:	:	:	:	:	:	:	:
1	0	0	1	0	1	1	0	4.750	4.750
1	0	0	1	0	1	1	1	4.765	4.765
1	0	0	1	1	0	0	0	4.780	4.780
1	0	0	1	1	0	0	1	4.795	4.795
1	0	0	1	1	0	1	0	4.800	4.810
1	0	0	1	1	0	1	1	4.800	4.825
1	0	0	1	1	1	0	0	4.800	4.840
1	0	0	1	1	1	0	1	4.800	4.855
:	:	:	:	:	:	:	:	4.800	:
1	1	0	1	1	1	0	0	4.800	5.800
:	:	:	:	:	:	:	:	4.800	5.800

VMH7	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	VCOMH (DDVDH_TRI=0)	VCOMH (DDVDH_TRI=1)
1	1	1	1	1	1	1	0	4.800	5.800
1	1	1	1	1	1	1	1	Setting inhibited	

Note: internal VREF can be modified by customer's request. default VREF=4.8 if DDVDH_TRI=0 and VREF=5.8 if DDVDH_TRI=1
VCOMH= {Decimal(VMH[7:0])x0.015+2.5 **}*(VREF/4.8) if** DDVDH_TRI=0
VCOMH= {Decimal(VMH[7:0])x0.015+2.5 **}*(VREF/5.8) if** DDVDH_TRI=1

VML[7:0]: Set the VCOML voltage (Low level voltage of VCOM). VCOM Low voltage = Decimal(VML[7:0])x0.015-2.5.

VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0	VCOML
0	0	0	0	0	0	0	0	-2.500
0	0	0	0	0	0	0	1	-2.485
0	0	0	0	0	0	1	0	-2.470
0	0	0	0	0	1	0	1	-2.455
:	:	:	:	:	:	:	:	:
0	1	0	1	0	1	1	1	-1.195
0	1	0	1	1	0	0	0	-1.180
:	:	:	:	:	:	:	:	:
1	0	1	0	0	0	1	1	-0.055
1	0	1	0	0	1	0	0	-0.040
1	0	1	0	0	1	0	1	-0.025
1	0	1	0	0	1	1	0	-0.010
1	0	1	0	0	1	1	1	VSSA
	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	VSSA

Note: internal VREF can be modified by customer's request. default VREF=4.8 if DDVDH_TRI=0 and VREF=5.8 if DDVDH_TRI=1
VCOML= { Decimal(VML[7:0])x0.015-2.5 **}*(VREF/4.8) if** DDVDH_TRI=0,
VCOML= { Decimal (VML[7:0])x0.015-2.5 **}*(VREF/5.8) if** DDVDH_TRI=1

VMF[7:0]: Set the VCOM offset voltage. VMH+1d/VML+1d means VMH/VML from original setting move up one step (15mV). VMH-1d/VML-1d means VMH/VML from original setting move down one step (15mV)

VMF[7:0]	VCOMH	VCOML
0	"VMH" – 128d	"VML" – 128d
1	"VMH" – 127d	"VML" – 127d
2	"VMH" – 126d	"VML" – 126d
3	"VMH" – 125d	"VML" – 125d
:	:	:
126	"VMH" – 2d	"VML" – 2d
127	"VMH" – 1d	"VML" – 1d
128	"VMH"	"VML"
129	"VMH" + 1d	"VML" + 1d
130	"VMH" + 2d	"VML" + 2d
:	:	:
254	"VMH" + 126d	"VML" + 126d
255	"VMH" + 127d	"VML" + 127d

Note: VMH[7:0]-128+VMF[7:0]>=0 and VML[7:0]-128+VMF[7:0]>=0

8.26 Display control 1 register (PAGE0 -26h~R28h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	ISC3	ISC2	ISC1	ISC0
R	1	*	*	*	*	ISC3	ISC2	ISC1	ISC0

Figure 8.39 Display control 1 register (PAGE0 -26h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PT1	PT0	PTV 1	PTV 0	*	*	PTG	REF
R	1	PT1	PT0	PTV 1	PTV 0	*	*	PTG	REF

Figure 8.40 Display control 2 register (PAGE0 -27h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	GON	DTE	D1	D0	*	*
R	1	*	*	GON	DTE	D1	D0	0	0

Figure 8.41 Display control 3 register (PAGE0 -28h)

ISC[3:0]: Specify the scan cycle of gate driver when **REF** = '1' in non-display area. Then scan cycle is set to Decimal(ISC[3:0])x4+1 frames.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	5 frames	83ms
0	0	1	0	9 frames	150ms
0	0	1	1	13 frames	217ms
0	1	0	0	17 frames	283ms
0	1	0	1	21 frames	350ms
0	1	1	0	25 frames	417ms
0	1	1	1	29 frames	483ms
1	0	0	0	33 frames	550ms
1	0	0	1	37 frames	616ms
1	0	1	0	41 frames	683ms
1	0	1	1	45 frames	750ms
1	1	0	0	49 frames	816ms
1	1	0	1	53 frames	883ms
1	1	1	0	57 frames	950ms
1	1	1	1	61 frames	1017ms

REF: Refresh display in non-display area in Partial mode enable bit.

REF	Refresh display operation
0	Disanle
1	Enable

PTG: Specify the scan mode of gate driver in non-display area.

PTG	Gate Outputs in Non-display Area
0	Normal Drive
1	Fixed VGL

PTV[1:0]: Specify the scan mode of VCOM in non-display area.

PTV1	PTV0	VCOM Outputs in Non-display Area
0	0	Normal Drive
0	1	Fixed to VCOML
1	0	Fixed to GND
1	1	Setting Inhibited

PT[1:0] : Specify the Non-display area source output in partial display mode.

REV_panel	GRAM Data	Source Output Level							
		Display area		Non-display Area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
1 (Normally Black Panel)	18'h0000 . . 18'h3FFF	V63P . . V0P	V0N . . V63N	V63P	V0N	VSSD	VSSD	Hi-z	Hi-z
0 (Normally White Panel)	18'h0000 . . 18'h3FFF	V0P . . V63P	V63N . . V0N	V63P	V0N	VSSD	VSSD	Hi-z	Hi-z

D[1:0]: When D1='1', display is on; when D1='0', display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = '1'. When D1='0', the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8367-A can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE.
When D[1:0]= '01', the internal display of the HX8367-A is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

D1	D0	Source Output	HX8367-A Internal Display Operations	Gate-Driver Control Signals
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Halt
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

GON, DTE:

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

PT1	PT0	REF	ISC[3:0]	Source Output	VCOM Output	Gate Output
0	x	x	--	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving
1	0	0	--	GND	PTV[1:0]	PTG
		1	Non-refresh cycle	GND	PTV[1:0]	PTG
			Refresh cycle	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving
1	1	0	--	Hi-z	PTV[1:0]	PTG
		1	Non-refresh cycle	Hi-z	PTV[1:0]	PTG
			Refresh cycle	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving

8.27 Frame control register (PAGE0 -29h~R2Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	RTN7	RTN6	RTN5	RTN4	RTN3	RTN2	RTN1	RTN0
R	1	RTN7	RTN6	RTN5	RTN4	RTN3	RTN2	RTN1	RTN0

Figure 8.42 Frame control 1 register (PAGE0 -29h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	I_DIV1	I_DIV0	*	*	N_DIV1	N_DIV0
R	1	*	*	I_DIV1	I_DIV0	*	*	N_DIV1	N_DIV0

Figure 8.43 Frame control 2 register (PAGE0 -2Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	N_DUM7	N_DUM6	N_DUM5	N_DUM4	N_DUM3	N_DUM2	N_DUM1	N_DUM0
R	1	N_DUM7	N_DUM6	N_DUM5	N_DUM4	N_DUM3	N_DUM2	N_DUM1	N_DUM0

Figure 8.44 Frame control 3 register (PAGE0 -2Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I_DUM7	I_DUM6	I_DUM5	I_DUM4	I_DUM3	I_DUM2	I_DUM1	I_DUM0
R	1	I_DUM7	I_DUM6	I_DUM5	I_DUM4	I_DUM3	I_DUM2	I_DUM1	I_DUM0

Figure 8.45 Frame control 4 register (PAGE0 -2Ch)

N_DIV[1:0]: Specify the division ratio of internal clocks in Normal / Partial mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **RTN[7:0]** bits (1H period clock cycle), **N_DIV[1:0]**, and **N_DUM[7:0]** bits.

I_DIV[1:0]: Specify the division ratio of internal clocks in Idle (8-color) / Partial Idle mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **RTN[7:0]** bits(1H period clock cycle), **I_DIV[1:0]**, and **I_DUM[7:0]** bits.

DIV1	DIV0	Division Ratio	Internal Display Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc = R-C oscillation frequency

RTN[7:0]: Specify clock number of one line period for internal operation.

Clock cycles=1/internal operation clock frequency(fosc)

RTN[7:0]	Clock Number Per Line
8'b0000_0000	124
8'b0000_0001	125
8'b0000_0010	126
8'b0000_0011	127
8'b0000_0100	128
:	:
8'b1111_1110	378
8'b1111_1111	379

N_DUM[7:0]: Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.

I_DUM[7:0]: Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

DUM[7:0]	Line Number in Blanking Period
000d	Setting Inhibited
001d	Setting Inhibited
002d	2
003d	3
004d	4
:	:
028d	28
:	:
190d	190
others	Setting Inhibited

Formula for the Frame Frequency during internal display mode:

Frame frequency = fosc/(RTN × DIV × (320+DUM)) [Hz]

fosc: RC oscillation frequency

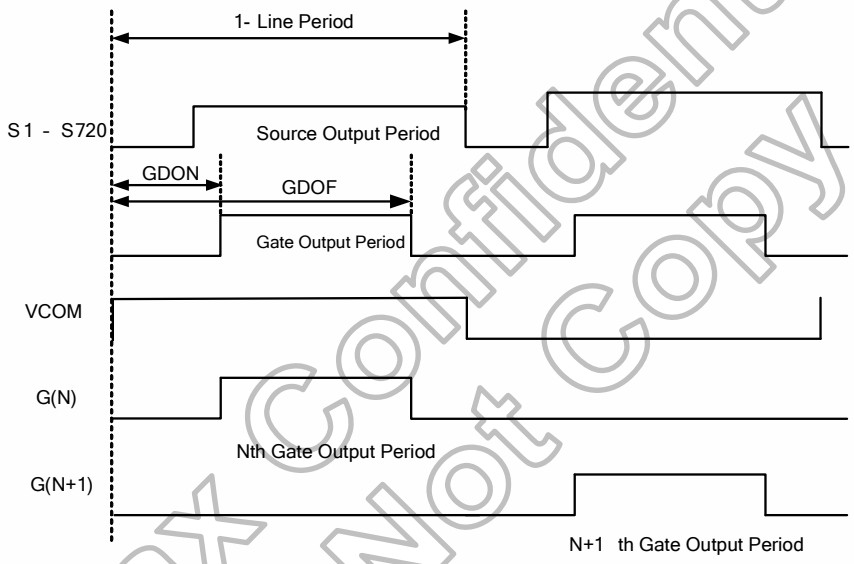
8.28 Cycle control register (PAGE0 -2Dh~R2Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GDON7	GDON6	GDON5	GDON4	GDON3	GDON2	GDON1	GDON0
R	1	GDON7	GDON6	GDON5	GDON4	GDON3	GDON2	GDON1	GDON0

Figure 8.46 Cycle control register 1 (PAGE0 -2Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GDOF7	GDOF6	GDOF5	GDOF4	GDOF3	GDOF2	GDOF1	GDOF0
R	1	GDOF7	GDOF6	GDOF5	GDOF4	GDOF3	GDOF2	GDOF1	GDOF0

Figure 8.47 Cycle control register 2 (PAGE0 -2Eh)



GDON[7:0]: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting “00h”, “01h”, “02h” is inhibited).

GDOF[7:0]: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the GDON[7:0] + 1≤ GDOF[7:0] ≤ RTN-1).

8.29 Display inversion register (PAGE0 -2Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I_NW2	I_NW1	I_NW0	*	N_NW2	N_NW1	N_NW0
R	1	*	I_NW2	I_NW1	I_NW0	*	N_NW2	N_NW1	N_NW0

Figure 8.48 Cycle control register (PAGE0 -2Fh)

N_ NW[2:0]: Specify LCD driving inversion type in Normal/ Partial mode.
I_ NW[2:0]: Specify LCD driving inversion type in Idle / Partial Idle mode.

NW[2:0]	LCD Driving Inversion Type
0d	Frame inversion
1d	1-line inversion
2d	2-line inversion
3d	3-line inversion
:	:
6d	6-line inversion
7d	7-line inversion

8.30 RGB interface control register (PAGE0 -31h~R34h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	RCM 1	RCM 0
R	1	0	0	0	0	0	0	RCM 1	RCM 0

Figure 8.49 RGB interface control register (PAGE0 -31h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	DPL	HSPL	VSPL	EPL
R	1	0	0	0	*	DPL	HSPL	VSPL	EPL

Figure 8.50 RGB interface control register (PAGE0 -32h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
R	1	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

Figure 8.51 RGB interface control register (PAGE0 -33h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HBP9	HBP8	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R	1	HBP9	HBP8	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 8.52 RGB interface control register (PAGE0 -34h)

This command is used to set RGB interface related register

RCM[1:0]: RGB and MCU interface select.

RCM1	RCM0	Interface Select
0	x	System Interface(1)
1	0	RGB Interface(1) (VS+HS+DE)
1	1	RGB Interface(2) (VS+HS)

EPL: Specify the polarity of ENABLE signal in RGB interface mode. EPL='1', the ENABLE signal is High active; EPL=0, the ENABLE signal is Low active.

VSPL: The polarity of VSYNC pin. When VSPL='0', the VSYNC signal is Low active. When VSPL=1, the VSYNC signal is High active.

HSPL: The polarity of HSYNC pin. When HSPL='0', the HSYNC signal is Low active. When HSPL=1, the HSYNC signal is High active.

DPL: The polarity of DOTCLK pin. When DPL='0', the data is latched by the chip on the rising edge of DOTCLK signal. When DPL='1', the data is latched by the chip on the falling edge of DOTCLK signal.

HBP and **VBP** are used to set vertical and horizontal back porch control in RGB I/F mode 2 (RCM[1:0]= '11') (RGB I/F mode 1 is using DE signal as data enable signal)

HBP[9:0]: Set the delay period from falling edge of HSYNC signal to first valid data in RGB I/F mode 2.

HBP[9:0]	No. of Clock Cycle of DOTCLK
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
08d	8
:	:
1021d	1021
1022d	1022
1023d	Setting Inhibited

VBP[5:0]: Set the delay period from falling edge of VSYNC signal to first valid line in RGB I/F mode 2.

VBP[5:0]	No. of Clock Cycle of HSYNC
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
125d	125
126d	126
127d	Setting Inhibited

8.31 Panel characteristic control register (PAGE0 -36h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL
R	1	*	*	*	*	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL

Figure 8.53 Panel characteristic control register (PAGE0 -36h)

This command is internal use for display panel setting.
REV_PANEL: The source output data polarity selected. When REV_PANEL=0, normally white panel is selected. When REV_PANEL = 1, normally black panel is selected.

BGR_PANEL: The color filter order direction selected. When BGR_PANEL=0, RGB-BGR order don't reverse. When BGR_PANEL = 1, the color filter order will be reversed.

GS_PANEL: The gate driver output shift direction selected. When GS_PANEL=0, the shift direction don't reverse. When GS_PANEL = 1, the shift direction will be reversed.

SS_PANEL: The source driver output shift direction selected. When SS_PANEL=0, the shift direction don't reverse. When SS_PANEL = 1, the shift direction will be reversed.

8.32 OTP register (PAGE0 -38h ~ R3Ah, R87h)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_MASK7	OTP_MASK6	OTP_MASK5	OTP_MASK4	OTP_MASK3	OTP_MASK2	OTP_MASK1	OTP_MASK0
R	1	OTP_MASK7	OTP_MASK6	OTP_MASK5	OTP_MASK4	OTP_MASK3	OTP_MASK2	OTP_MASK1	OTP_MASK0

Figure 8.54 OTP command 1 (PAGE0 -38h)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_INDEX7	OTP_INDEX6	OTP_INDEX5	OTP_INDEX4	OTP_INDEX3	OTP_INDEX2	OTP_INDEX1	OTP_INDEX0
R	1	OTP_INDEX7	OTP_INDEX6	OTP_INDEX5	OTP_INDEX4	OTP_INDEX3	OTP_INDEX2	OTP_INDEX1	OTP_INDEX0

Figure 8.55 OTP command 2 (PAGE0 -39h)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG
R	1	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG

Figure 8.56 OTP command 3 (PAGE0 -3Ah)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
R	1	OTP_DATA7	OTP_DATA6	OTP_DATA5	OTP_DATA4	OTP_DATA3	OTP_DATA2	OTP_DATA1	OTP_DATA0

Figure 8.57 OTP command 4 (PAGE0 -3Bh)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_KEY7	OTP_KEY6	OTP_KEY5	OTP_KEY4	OTP_KEY3	OTP_KEY2	OTP_KEY1	OTP_KEY0
R	1	OTP_KEY7	OTP_KEY6	OTP_KEY5	OTP_KEY4	OTP_KEY3	OTP_KEY2	OTP_KEY1	OTP_KEY0

Figure 8.58 OTP command 5 (PAGE0 -87h)

This command is used to set the OTP related setting. Please see OTP flow for detail use.

OTP_MASK[7:0]: OTP bit programming mask, if set to ‘1’, it means the related bit in OTP can not be programmed.

OTP_INDEX[7:0]: Set index location in OTP to be programmed.

OTP_PROG: When this bit is set to ‘1’, LSI writes data to OTP from internal register.

VPP_SEL: When set to ‘1’, VGH input voltage is fed to OTP.

OTP_LOAD_DISABLE: Internal use, not open.

DCCLK_DISABLE: Stop pumping colock.

OTP_PTM[1:0]: Internal use, not open.

OTP_PWE: Internal use, not open.

OTP_POR: When set to ‘1’, OTP data can be read the related OTP Index data at OTP_DATA[7:0]

OTP_DATA[7:0]: Read OTP data.

OTP_KEY[7:0]: Set to “AAh” to enable OTP program.

8.33 Gamma control 1~35 register (PAGE0 -40h~5Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP05	VRP04	VRP03	VRP02	VRP01	VRP00
R	1	0	0	VRP05	VRP04	VRP03	VRP02	VRP01	VRP00

Figure 8.59 Gamma control 1 register (PAGE0 -40h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP15	VRP14	VRP13	VRP12	VRP11	VRP10
R	1	0	0	VRP15	VRP14	VRP13	VRP12	VRP11	VRP10

Figure 8.60 Gamma control 2 register (PAGE0 -41h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP25	VRP24	VRP23	VRP22	VRP21	VRP20
R	1	0	0	VRP25	VRP24	VRP23	VRP22	VRP21	VRP20

Figure 8.61 Gamma control 3 register (PAGE0 -42h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP35	VRP34	VRP33	VRP32	VRP31	VRP30
R	1	0	0	VRP35	VRP34	VRP33	VRP32	VRP31	VRP30

Figure 8.62 Gamma control 4 register (PAGE0 -43h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP45	VRP44	VRP43	VRP42	VRP41	VRP40
R	1	0	0	VRP45	VRP44	VRP43	VRP42	VRP41	VRP40

Figure 8.63 Gamma control 5 register (PAGE0 -44h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP55	VRP54	VRP53	VRP52	VRP51	VRP50
R	1	0	0	VRP55	VRP54	VRP53	VRP52	VRP51	VRP50

Figure 8.64 Gamma control 6 register (PAGE0 -45h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRP 06	PRP 05	PRP 04	PRP 03	PRP 02	PRP 01	PRP 00
R	1	0	PRP 06	PRP 05	PRP 04	PRP 03	PRP 02	PRP 01	PRP 00

Figure 8.65 Gamma control 7 register (PAGE0 -46h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRP 16	PRP 15	PRP 14	PRP 13	PRP 12	PRP 11	PRP 10
R	1	0	PRP 16	PRP 15	PRP 14	PRP 13	PRP 12	PRP 11	PRP 10

Figure 8.66 Gamma control 8 register (PAGE0 -47h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 04	PKP 03	PKP 02	PKP 01	PKP 00
R	1	0	0	0	PKP 04	PKP 03	PKP 02	PKP 01	PKP 00

Figure 8.67 Gamma control 9 register (PAGE0 -48h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 14	PKP 13	PKP 12	PKP 11	PKP 10
R	1	0	0	0	PKP 14	PKP 13	PKP 12	PKP 11	PKP 10

Figure 8.68 Gamma control 10 register (PAGE0 -49h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 24	PKP 23	PKP 22	PKP 21	PKP 20
R	1	0	0	0	PKP 24	PKP 23	PKP 22	PKP 21	PKP 20

Figure 8.69 Gamma control 11 register (PAGE0 -4Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 34	PKP 33	PKP 32	PKP 31	PKP 30
R	1	0	0	0	PKP 34	PKP 33	PKP 32	PKP 31	PKP 30

Figure 8.70 Gamma control 12 register (PAGE0 -4Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 44	PKP 43	PKP 42	PKP 41	PKP 40
R	1	0	0	0	PKP 44	PKP 43	PKP 42	PKP 41	PKP 40

Figure 8.71 Gamma control 13 register (PAGE0 -4Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 05	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00
R	1	0	0	VRN 05	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00

Figure 8.72 Gamma control 14 register (PAGE0 -50h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 15	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10
R	1	0	0	VRN 15	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10

Figure 8.73 Gamma control 15 register (PAGE0 -51h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 25	VRN 24	VRN 23	VRN 22	VRN 21	VRN 20
R	1	0	0	VRN 25	VRN 24	VRN 23	VRN 22	VRN 21	VRN 20

Figure 8.74 Gamma control 16 register (PAGE0 -52h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 35	VRN 34	VRN 33	VRN 32	VRN 31	VRN 30
R	1	0	0	VRN 35	VRN 34	VRN 33	VRN 32	VRN 31	VRN 30

Figure 8.75 Gamma control 17 register (PAGE0 -53h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 45	VRN 44	VRN 43	VRN 42	VRN 41	VRN 40
R	1	0	0	VRN 45	VRN 44	VRN 43	VRN 42	VRN 41	VRN 40

Figure 8.76 Gamma control 18 register (PAGE0 -54h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 55	VRN 54	VRN 53	VRN 52	VRN 51	VRN 50
R	1	0	0	VRN 55	VRN 54	VRN 53	VRN 52	VRN 51	VRN 50

Figure 8.77 Gamma control 19 register (PAGE0 -55h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRN 06	PRN 05	PRN 04	PRN 03	PRN 02	PRN 01	PRN 00
R	1	0	PRN 06	PRN 05	PRN 04	PRN 03	PRN 02	PRN 01	PRN 00

Figure 8.78 Gamma control 20 register (PAGE0 -56h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRN 16	PRN 15	PRN 14	PRN 13	PRN 12	PRN 11	PRN 10
R	1	0	PRN 16	PRN 15	PRN 14	PRN 13	PRN 12	PRN 11	PRN 10

Figure 8.79 Gamma control 21 register (PAGE0 -57h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 04	PKN 03	PKN 02	PKN 01	PKN 00
R	1	0	0	0	PKN 04	PKN 03	PKN 02	PKN 01	PKN 00

Figure 8.80 Gamma control 22 register (PAGE0 -58h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 14	PKN 13	PKN 12	PKN 11	PKN 10
R	1	0	0	0	PKN 14	PKN 13	PKN 12	PKN 11	PKN 10

Figure 8.81 Gamma control 23 register (PAGE0 -59h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 24	PKN 23	PKN 22	PKN 21	PKN 20
R	1	0	0	0	PKN 24	PKN 23	PKN 22	PKN 21	PKN 20

Figure 8.82 Gamma control 24 register (PAGE0 -5Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 34	PKN 33	PKN 32	PKN 31	PKN 30
R	1	0	0	0	PKN 34	PKN 33	PKN 32	PKN 31	PKN 30

Figure 8.83 Gamma control 25 register (PAGE0 -5Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 44	PKN 43	PKN 42	PKN 41	PKN 40
R	1	0	0	0	PKN 44	PKN 43	PKN 42	PKN 41	PKN 40

Figure 8.84 Gamma control 26 register (PAGE0 -5Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CGM N11	CGM N10	CGM N01	CGM N00	CGM P11	CGM P10	CGM P01	CGM P00
R	1	CGM N11	CGM N10	CGM N01	CGM N00	CGM P11	CGM P10	CGM P01	CGM P00

Figure 8.85 Gamma control 27 register (PAGE0 -5Dh)

VRP5-0[5:0]: Gamma Offset adjustment registers for positive polarity output
VRN5-0[5:0]: Gamma Offset adjustment registers for negative polarity output
PRP1-0[6:0]: Gamma Center adjustment registers for positive polarity output
PRN1-0[6:0]: Gamma Center adjustment registers for negative polarity output
PKP8-0[4:0]: Gamma Macro adjustment registers for positive polarity output
PKN8-0[4:0]: Gamma Macro adjustment registers for negative polarity output
For details, please refer to 7.2 Gamma resister stream and 8 to 1 Selector.

8.34 TE control register (PAGE0 -60h, 84h~85h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	TEMODE	TEON	*	*	*
R	1	0	0	0	TEMODE	TEON	0	0	0

Figure 8.86 TE control register (PAGE0 -60h)

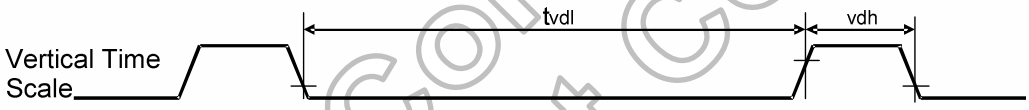
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TSEL15	TSEL14	TSEL13	TSEL12	TSEL11	TSEL10	TSEL9	TSEL8
R	1	TSEL15	TSEL14	TSEL13	TSEL12	TSEL11	TSEL10	TSEL9	TSEL8

Figure 8.87 TE output line2 register (PAGE0 -84h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TSEL7	TSEL6	TSEL5	TSEL4	TSEL3	TSEL2	TSEL1	TSEL0
R	1	TSEL7	TSEL6	TSEL5	TSEL4	TSEL3	TSEL2	TSEL1	TSEL0

Figure 8.88 TE output line1 register (PAGE0 -85h)

TEMODE: Specify the Tearing-Effect mode.
When **TEMODE** = '0': The Tearing Effect Output line (TE) consists of V-Blanking information only.

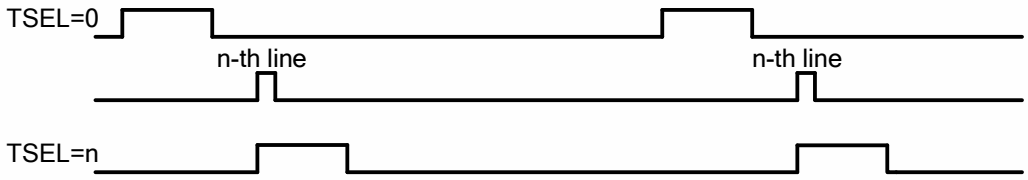


When **TEMODE** ='1': The Tearing Effect Output Line (TE) consists of both V-Blanking and H-Blanking information

Note: During Stand by Mode with Tearing Effect Line On, Tearing Effect Output pin active low

TEON: This command is used to turn ON the Tearing Effect output signal from the TE signal line.

TSEL[15:0]: This command is used to setting TE delay line at TEMODE="0". When TSEL[15:0]=16'h0000, TE output is the same as TEMODE="0". When Decimal(TSEL[15:0])=n, TE output at n-th line starting.



8.35 ID register (PAGE0 -61h~63h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
R	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

Figure 8.89 ID1 register (PAGE0 -61h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	ID26	ID25	ID24	ID23	ID22	ID21	ID20
R	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20

Figure 8.90 ID2 register (PAGE0 -62h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
R	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

Figure 8.91 ID3 register (PAGE0 -63h)

ID1~ID3: ID setting related register.

8.36 PTBA Control 1~2 Register (PAGE0 –REAh~REBh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PTBA 15	PTBA 14	PTBA 13	PTBA 12	PTBA 11	PTBA 10	PTBA 9	PTBA 8
R	1	PTBA 15	PTBA 14	PTBA 13	PTBA 12	PTBA 11	PTBA 10	PTBA 9	PTBA 8

Figure 8.92 PTBA Control 1 Register (PAGE0 –EAh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PTBA 7	PTBA 6	PTBA 5	PTBA 4	PTBA 3	PTBA 2	PTBA 1	PTBA 0
R	1	PTBA 7	PTBA 6	PTBA 5	PTBA 4	PTBA 3	PTBA 2	PTBA 1	PTBA 0

Figure 8.93 PTBA Control 2 Register (PAGE0 –EBh)

PTBA[15:6], PTBA[4:0]: Internal power related setting, not open.
PTBA5: PSRR_POR set '1' to raise OP bias besides Source OP.

8.37 STBA Control 1~2 Register (PAGE0 –RECh~REDh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	STBA 15	STBA 14	STBA 13	STBA 12	STBA 11	STBA 10	STBA 9	STBA 8
R	1	STBA 15	STBA 14	STBA 13	STBA 12	STBA 11	STBA 10	STBA 9	STBA 8

Figure 8.94 STBA Control 1 Register (PAGE0 –ECh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	STBA 7	STBA 6	STBA 5	STBA 4	STBA 3	STBA 2	STBA 1	STBA 0
R	1	STBA 7	STBA 6	STBA 5	STBA 4	STBA 3	STBA 2	STBA 1	STBA 0

Figure 8.95 STBA Control 2 Register (PAGE0 –EDh)

STBA[15:6]: Source Bias current setting.
STBA[4:2]: Gamma Bias current setting.
STBA5, STAB[1:0]: Not used.

8.38 OTPS1B Register (PAGE0 –RF1h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	OTPS 1B
R	1	0	0	0	0	0	0	0	OTPS 1B

Figure 8.96 OTPS1B Register (PAGE0 –F1h)

OTPS1B: Source OP gamma short control.

8.39 GENON Register (PAGE0 –RF2h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GEN ON7	GEN ON6	GEN ON5	GEN ON4	GEN ON3	GEN ON2	GEN ON1	GEN ON0
R	1	GEN ON7	GEN ON6	GEN ON5	GEN ON4	GEN ON3	GEN ON2	GEN ON1	GEN ON0

Figure 8.97 GENON Register (PAGE0 –F2h)

GENON[7:0]: Gamma OP on period control.

8.40 Command page select register (RFFh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	PAGE_SEL1	PAGE_SEL0
R	1	0	0	0	0	0	0	PAGE_SEL1	PAGE_SEL0

Figure 8.98 Command page select register (RFFh)

PAGE_SEL[1:0]: Command set page select.

PAGE_SEL1	PAGE_SEL0	Command Page
0	0	Page 0
0	1	Page 1

8.41 DGC control register (PAGE1 -00h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	DGC_EN
R	1	0	0	0	0	0	0	0	DGC_EN

Figure 8.99 DGC control register (PAGE1 -00h)

DGC_EN: Digital gamma correction enable.
0: Disable
1: Enable

8.42 DGC LUT register (PAGE1 -01h~63h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	D7	D6	D5	D4	D3	D2	D1	D0
R	1	D7	D6	D5	D4	D3	D2	D1	D0

Figure 8.100 DGC LUT register (PAGE1 -01h~63h)

There are 99 bytes DGC LUT to set R, G, B gamma independently. When DGC_EN=1, R, G, B gamma will mapping V0, V2, V4, ..., V60, V62, V63 voltage to the LUT register setting gray level voltage. V(2N+1) = (V(2N) + V(2N+2))/2 (N=0~30).

LUT	D7	D6	D5	D4	D3	D2	D1	D0	Default	Gray Mapping
R01h	R007	R006	R005	R004	R003	R002	R001	R000	00h	R_V0
R02h	R017	R016	R015	R014	R013	R012	R011	R010	08h	R_V2
R03h	R027	R026	R025	R024	R023	R022	R021	R020	10h	R_V4
:	:	:	:	:	:	:	:	:	:	:
R20h	R317	R316	R315	R314	R313	R312	R311	R310	F8h	R_V62
R21h	R327	R326	R325	R324	R323	R322	R321	R320	FCh	R_V63
R22h	G007	G006	G005	G004	G003	G002	G001	G000	00h	G_V0
R23h	G017	G016	G015	G014	G013	G012	G011	G010	08h	G_V2
R24h	G027	G026	G025	G024	G023	G022	G021	G020	10h	G_V4
:	:	:	:	:	:	:	:	:	:	:
R41h	G317	G316	G315	G314	G313	G312	G311	G310	F8h	G_V62
R42h	G327	R326	G325	G324	G323	G322	G321	G320	FCh	G_V63
R43h	B007	B006	B005	B004	B003	B002	B001	B000	00h	B_V0
R44h	B017	B016	B015	B014	B013	B012	B011	B010	08h	B_V2
R45h	B027	B026	B025	B024	B023	B022	B021	B020	10h	B_V4
:	:	:	:	:	:	:	:	:	:	:
R62h	B317	B316	B315	B314	B313	B312	B311	B310	F8h	B_V62
R63h	B327	B326	B325	B324	B323	B322	B321	B320	FCh	B_V63

9. Layout Recommendation

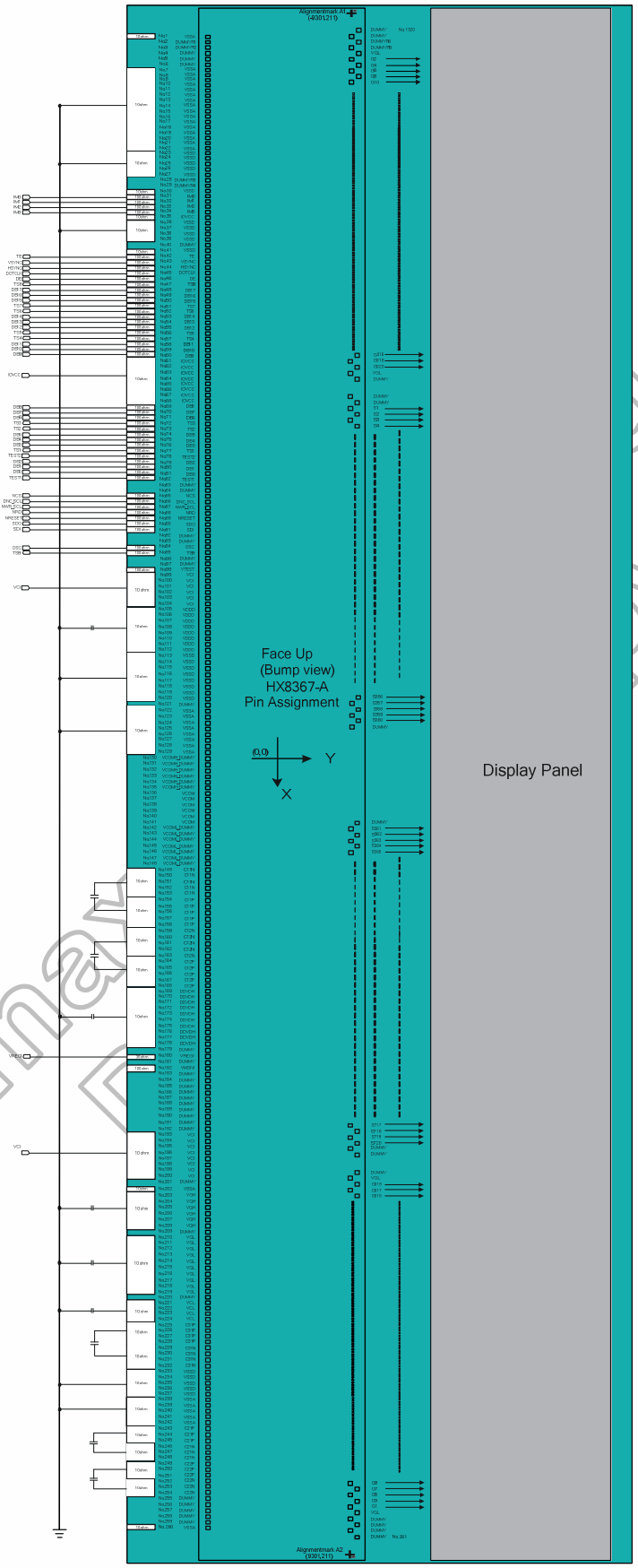


Figure 9.1 Layout recommendation of HX8367-A

Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
OSC	Input	100	Ω
IM[3:0]	Input	100	Ω
NRD, NWR_SCL, DNC_SCL, NCS, SDI	Input	100	Ω
NRESET	Input	100	Ω
TE, SDO	Output	100	Ω
DB[17:0], SDA	I/O	100	Ω
DOTCLK, DE, VSYNC, HSYNC	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
DDVDH	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1	Output	30	Ω
C11P, C11N, C12P, C12N	Open	10	Ω
C31P, C31N	Open	10	Ω
C21P, C21N	Open	10	Ω
C22P, C22N	Open	10	Ω
TEST2~1	Input	100	Ω
TS9~1	Output	100	Ω
VCOMH_DUMMY, VCOML_DUMMY,DUMMY	Dummy	100	Ω
VTEST,VMONI, DUMMYR6~1	Test Pin	100	Ω

Table 9.1 Maximum layout resistance

10. OTP

10.1 OTP programming flow

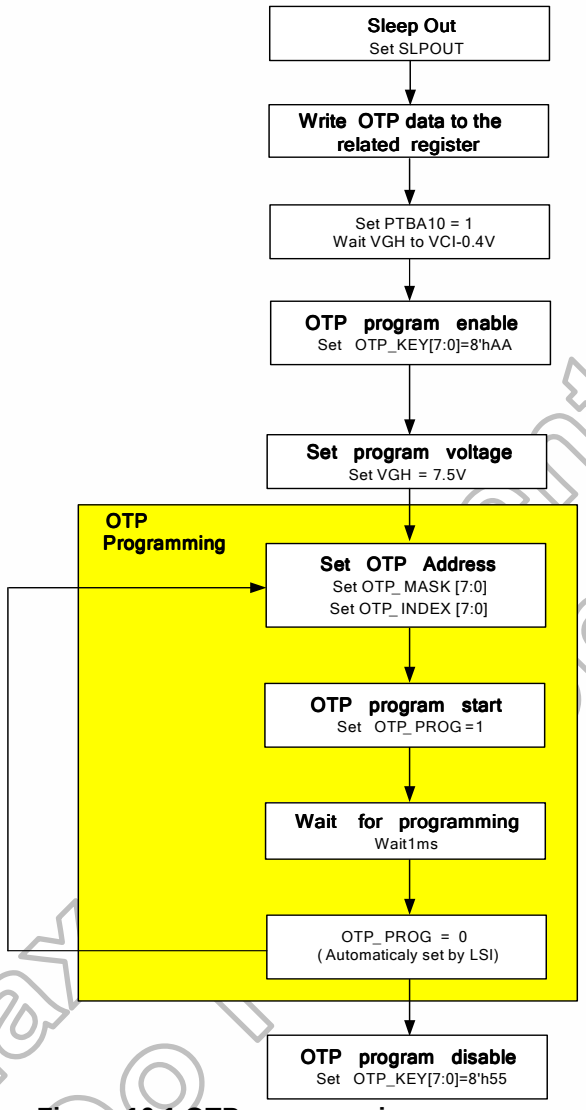
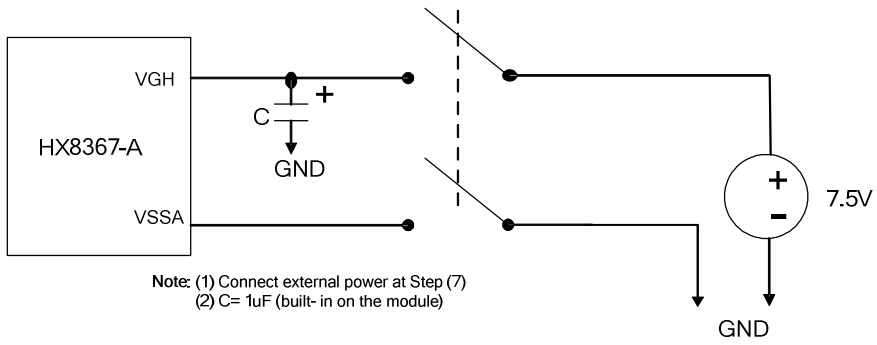


Figure 10.1 OTP programming sequence

Programming circuitry



Note: (1) Connect external power at Step (7)
(2) C= 1uF (built- in on the module)

10.2 OTP table

PA	D7	D6	D5	D4	D3	D2	D1	D0	Command Set
00	ID1[7:0]								-
01	NVALID_ID	ID2[6:0]							-
02	ID3[7:0]								-
03	VMF1[7:0]								-
04	VMF2[7:0]								-
05	VMF3[7:0]								-
06	VMH[7:0]								-
07	VML[7:0]								-
08	(no use)			NVALID_VML	NVALID_VMH	NVALID_VMF3	NVALID_VML2	NVALID_VML1	-
09	NVALID_PANEL	(no use)					DDVDH_TRI	(no use)	-
0A	(no use)				SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	-
0B	NVALID_DGC	(no use)						DGC_EN	-
0C	DGC_LUT_R00[7:0]								-
0D	DGC_LUT_R01[7:0]								-
0E	DGC_LUT_R02[7:0]								-
0F	DGC_LUT_R03[7:0]								-
10	DGC_LUT_R04[7:0]								-
11	DGC_LUT_R05[7:0]								-
12	DGC_LUT_R06[7:0]								-
13	DGC_LUT_R07[7:0]								-
14	DGC_LUT_R08[7:0]								-
15	DGC_LUT_R09[7:0]								-
16	DGC_LUT_R10[7:0]								-
17	DGC_LUT_R11[7:0]								-
18	DGC_LUT_R12[7:0]								-
19	DGC_LUT_R13[7:0]								-
1A	DGC_LUT_R14[7:0]								-
1B	DGC_LUT_R15[7:0]								-
1C	DGC_LUT_R16[7:0]								-
1D	DGC_LUT_R17[7:0]								-
1E	DGC_LUT_R18[7:0]								-
1F	DGC_LUT_R19[7:0]								-
20	DGC_LUT_R20[7:0]								-
21	DGC_LUT_R21[7:0]								-
22	DGC_LUT_R22[7:0]								-
23	DGC_LUT_R23[7:0]								-
24	DGC_LUT_R24[7:0]								-
25	DGC_LUT_R25[7:0]								-
26	DGC_LUT_R26[7:0]								-
27	DGC_LUT_R27[7:0]								-
28	DGC_LUT_R28[7:0]								-
29	DGC_LUT_R29[7:0]								-
2A	DGC_LUT_R30[7:0]								-
2B	DGC_LUT_R31[7:0]								-
2C	DGC_LUT_R32[7:0]								-
2D	DGC_LUT_G00[7:0]								-
2E	DGC_LUT_G01[7:0]								-
2F	DGC_LUT_G02[7:0]								-
30	DGC_LUT_G03[7:0]								-
31	DGC_LUT_G04[7:0]								-
32	DGC_LUT_G05[7:0]								-
33	DGC_LUT_G06[7:0]								-
34	DGC_LUT_G07[7:0]								-
35	DGC_LUT_G08[7:0]								-
36	DGC_LUT_G09[7:0]								-
37	DGC_LUT_G10[7:0]								-
38	DGC_LUT_G11[7:0]								-
39	DGC_LUT_G12[7:0]								-
3A	DGC_LUT_G13[7:0]								-
3B	DGC_LUT_G14[7:0]								-
3C	DGC_LUT_G15[7:0]								-
3D	DGC_LUT_G16[7:0]								-
3E	DGC_LUT_G17[7:0]								-
3F	DGC_LUT_G18[7:0]								-
40	DGC_LUT_G19[7:0]								-

PA	D7	D6	D5	D4	D3	D2	D1	D0	Command Set
41	DGC_LUT_G20[7:0]								-
42	DGC_LUT_G21[7:0]								-
43	DGC_LUT_G22[7:0]								-
44	DGC_LUT_G23[7:0]								-
45	DGC_LUT_G24[7:0]								-
46	DGC_LUT_G25[7:0]								-
47	DGC_LUT_G26[7:0]								-
48	DGC_LUT_G27[7:0]								-
49	DGC_LUT_G28[7:0]								-
4A	DGC_LUT_G29[7:0]								-
4B	DGC_LUT_G30[7:0]								-
4C	DGC_LUT_G31[7:0]								-
4D	DGC_LUT_G32[7:0]								-
4E	DGC_LUT_B00[7:0]								-
4F	DGC_LUT_B01[7:0]								-
50	DGC_LUT_B02[7:0]								-
51	DGC_LUT_B03[7:0]								-
52	DGC_LUT_B04[7:0]								-
53	DGC_LUT_B05[7:0]								-
54	DGC_LUT_B06[7:0]								-
55	DGC_LUT_B07[7:0]								-
56	DGC_LUT_B08[7:0]								-
57	DGC_LUT_B09[7:0]								-
58	DGC_LUT_B10[7:0]								-
59	DGC_LUT_B11[7:0]								-
5A	DGC_LUT_B12[7:0]								-
5B	DGC_LUT_B13[7:0]								-
5C	DGC_LUT_B14[7:0]								-
5D	DGC_LUT_B15[7:0]								-
5E	DGC_LUT_B16[7:0]								-
5F	DGC_LUT_B17[7:0]								-
60	DGC_LUT_B18[7:0]								-
61	DGC_LUT_B19[7:0]								-
62	DGC_LUT_B20[7:0]								-
63	DGC_LUT_B21[7:0]								-
64	DGC_LUT_B22[7:0]								-
65	DGC_LUT_B23[7:0]								-
66	DGC_LUT_B24[7:0]								-
67	DGC_LUT_B25[7:0]								-
68	DGC_LUT_B26[7:0]								-
69	DGC_LUT_B27[7:0]								-
6A	DGC_LUT_B28[7:0]								-
6B	DGC_LUT_B29[7:0]								-
6C	DGC_LUT_B30[7:0]								-
6D	DGC_LUT_B31[7:0]								-
6E	DGC_LUT_B32[7:0]								-

Note: (1) The same color means the same NVALID bit controlled.
(2) VMF can be OTP three times. If Index 03h programmed first time, VMF1(Index 03h) will be OTP. If Index 03h programmed second time, VMF2(Index 04h) will be OTP. If Index 03h programmed third time, VMF3(Index 05h) will be OTP.
(3) If VMF1, VMF2, VMF3, VMH, VML was programmed, the related NVALID bit in Index 08h will be programmed at the same time automatically.
(4) If programming Index 0Bh, DGC group(Index 0Bh~6Eh) will be programmed automatically.

11. Electrical Characteristics

11.1 Absolute maximum ratings

Item	Symbol	Unit	Spec.			Note
			Min.	Typ.	Max.	
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3		+4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3		+4.6	Note(3)
Power Supply Voltage 3	DDVDH ~ VSSA	V	-0.3		+6.6	Note(4)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3		+4.6	Note(5)
Power Supply Voltage 5	DDVDH ~ VCL	V	-0.3		+9	Note(6)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3		+18.5	Note(7)
Power Supply Voltage 7	VSSA ~ VGL	V	0		-16.5	Note(8)
Logic Input Voltage	V_{IN}	V	-0.3		IOVCC+0.5	-
Logic Output Voltage	Vo	V	-0.3		IOVCC+0.5	-
Operating Temperature	Topr	℃	-40		+85	Note(9),(10)
Storage Temperature	Tstg	℃	-55		+110	Note(9),(10)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure DDVDH ≥ VSSA.
(5) To make sure VSSA ≥ VCL.
(6) To make sure DDVDH ≥ VCL.
(7) To make sure VGH ≥ VSSA.
(8) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(9) For die and wafer products, specified up to +85℃.
(10) This temperature specifications apply to the TCP package.

Table 11.1 Absolute maximum ratings

11.2 ESD protection level

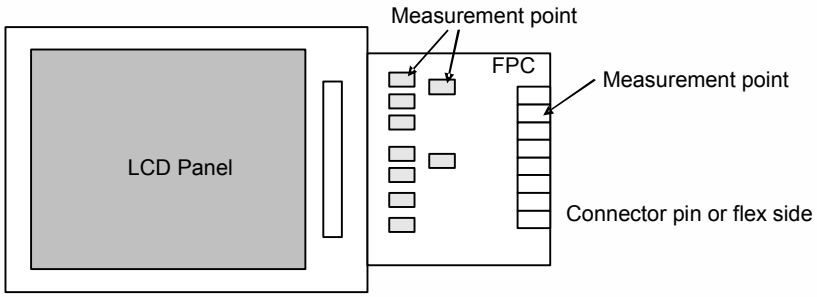
Mode	Test Condition	Protection Level	Unit
Human Body Model	C=100 pF, R=1.5 kΩ	±2.0K	V
Machine Model	C=200 pF, R=0.0 Ω	±200	V

Table 11.2 ESD protection level

11.3 DC characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
IO Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Driver Operating voltage	VCI	Operation voltage	2.5	2.8	3.3	
Source Drive Voltage	VREG1	Triple Pump	3.3	4.65	5.8	
	VREG1	Dual Pump	3.3	4.65	4.8	
Gate Drive High Voltage	VGH	IVGH=30uA (Typ:BT=001) VCI=2.8 Dual Pump	9.5	14.25	-	
		IVGH=30uA (Typ:BT=001) VCI=2.8 Triple Pump	11.6	17.39	-	
Gate Drive Low Voltage	VGL	IVGL=30uA (Typ:BT=001) VCI=2.8 Dual Pump	-6.85	-9.5	-	
		IVGL=30uA (Typ:BT=001) VCI=2.8 Triple Pump	-8.46	-11.59	-	
Drive Supply Voltage	|VGH-VGL|	-	-	-	30	
Input / Output						
High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	µA
Oscillator frequency	fOSC	Frame rate at 60hz,default Vs and Hs setting Ta=25℃	2.50	2.63	2.76	MHz
Booster(VCI=2.8V)						
DDVDH boost voltage1	DDVDH	Dual Pump IDDVDH=300uA	4.8	5.0	5.2	V
		Triple Pump IDDVDH=300uA	5.9	6.1	6.3	
VCL boost voltage	VCL	ICL=-100uA	-2.5	-2.65	-2.75	
VCOM Generator(VCI=2.8V)						
VCOM amplitude	VCOM	No load, Dual Pump	2.5	4.4	7.3	V
		No load Triple Pump	2.5	4.4	8.3	V
VCOM high level	VCOMH	No load Dual Pump	2.5	3.205	4.8	V
		No load Triple Pump	2.5	3.205	5.8	V
VCOM low level	VCOML	No load	-2.5	-1.195	VSSD	V
Source Driver(Typ:Ta=25℃ VCI=2.8V)						
Output voltage deviation (mean value)	DVOS	VSSD+1.0 ~ VREG1-1.0	-	+/- 10	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VREG1-1.0 ~ VREG1-0.1V	-	+/- 30	+/- 50	mV
Output voltage range	VOS	-	0.1	-	DDVDH-0.1	V
Output offset voltage	Voff	-		+/-30	+/-50	mV

Note: VREG1/VCOMH/VCOML conditions: When Internal Voltage VREF=4.8V for dual pump and VREF=5.8V for Triple pump.



11.3.1 Current consumption

Host I/F	Mode of operation	Frame Frequency	Inversion Mode	Image	Memory Data Access Control (MY:MX:MV)	Current consumption			
						Typical		Worst case	
						VCI (mA)	IOVCC(mA)	VCI (mA)	IOVCC (mA)
Host interface NOT active	Normal Mode On	60Hz	1-line	Black	X;X;X	3.33	0.37	3.80	0.43
			1-line	1x1 checker board	X;X;X	2.58	0.37	3.14	0.43
			1-line	2x2 checker board	X;X;X	2.65	0.64	3.21	0.72
			1-line	Gray_Scale Top to Bottom	X;X;X	2.53	0.37	3.15	0.43
			1-line	20B80W	X;X;X	2.45	0.37	2.87	0.43
	Idle Mode On	60Hz	1-line	20B80W	X;X;X	2.24	0.28	2.76	0.34
	Partial Mode On (48 lines)	60Hz	1-line	Black	X;X;X	1.47	0.19	2.11	0.23
	Partial Mode On (48 lines) Idle Mode On	60Hz	1-line	1x1 checker board	X;X;X	1.07	0.17	1.71	0.19
			1-line	Worst pattern	X;X;X	1.17	0.17	1.83	0.19
	Sleep Mode	N/A	N/A	N/A	X;X;X	0.002	0.003	0.002	0.024
Host interface active	Normal Mode On	60Hz	1-line	262k Colors Worst pattern CPU Access @ 15fps	X;X;X	3.33	1.36	3.80	1.42
				262k Colors Worst pattern CPU Access @ 30fps	X;X;X	3.33	1.89	3.80	1.96

Table 11.3 Current consumption

Typical Case:
T_A = 25℃
IOVCC=1.8V
VCI = 2.8V
CMO 2.2” panel

Worst Case:
T_A = -40 to 85℃
IOVCC = 1.65V to 1.95V
VCI = 2.5V to 3.3V
Includes Process Variance.

11.4 AC characteristics

11.4.1 Parallel interface characteristics (8080-series MPU)

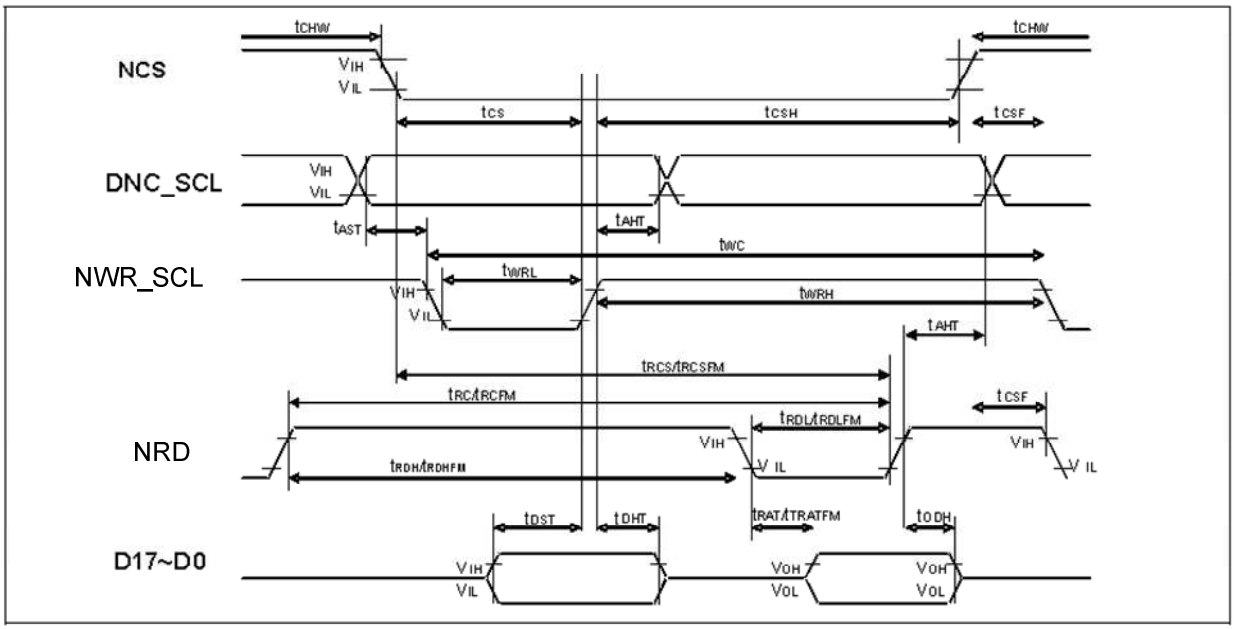


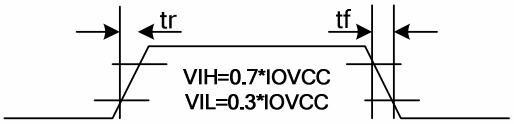
Figure 11.1 Parallel interface characteristics (8080-Series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A=-30 to 70°C)

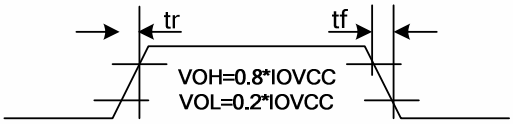
Signal	Symbol	Parameter	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Description
DNC_SCL	t_{AST}	Address setup time	0	-	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	15	-	-		
NCS	t_{CHW}	Chip select "H" pulse width	0	-	-	ns	-
	t_{CS}	Chip select setup time (Write)	15	-	-		
	t_{RCS}	Chip select setup time (Read ID)	45	-	-		
	t_{RCSFM}	Chip select setup time (Read FM)	355	-	-		
	t_{CSF}	Chip select wait time (Write/Read)	10	-	-		
	t_{CSH}	Chip select hold time	10	-	-		
NWR_SCL	t_{WC}	Write cycle	90	-	-	ns	-
	t_{WRH}	Control pulse "H" duration	20	-	-		
	t_{WRL}	Control pulse "L" duration	20	-	-		
NRD(ID)	t_{RC}	Read cycle (ID)	160	-	-	ns	When read ID data
	t_{RDH}	Control pulse "H" duration (ID)	90	-	-		
	t_{RDL}	Control pulse "L" duration (ID)	45	-	-		
NRD(FM)	t_{RCFM}	Read cycle (FM)	550	-	-	ns	When read from frame memory
	t_{RDHFM}	Control pulse "H" duration (FM)	90	-	-		
	t_{RDLFM}	Control pulse "L" duration (FM)	355	-	-		
DB17 to DB0	t_{DST}	Data setup time	10	-	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	10	-	-		
	t_{RAT}	Read access time (ID)	-	-	80		
	t_{RATFM}	Read access time (FM)	-	-	340		
	t_{ODH}	Output disable time	20	-	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



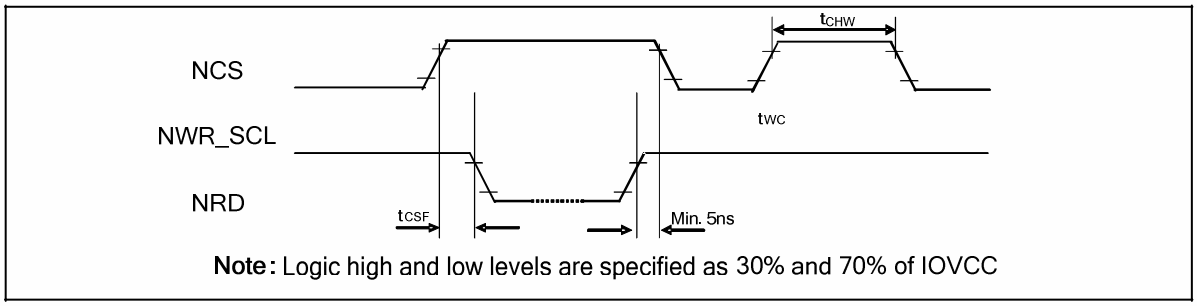


Figure 11.2 Chip select timing

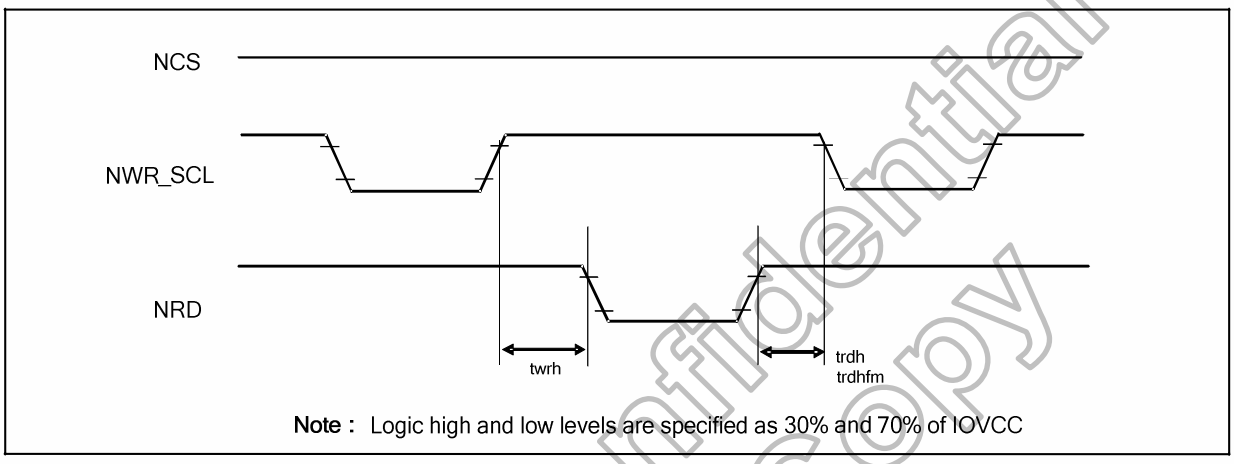


Figure 11.3 Write to read and read to write timing

11.4.2 Serial interface characteristics

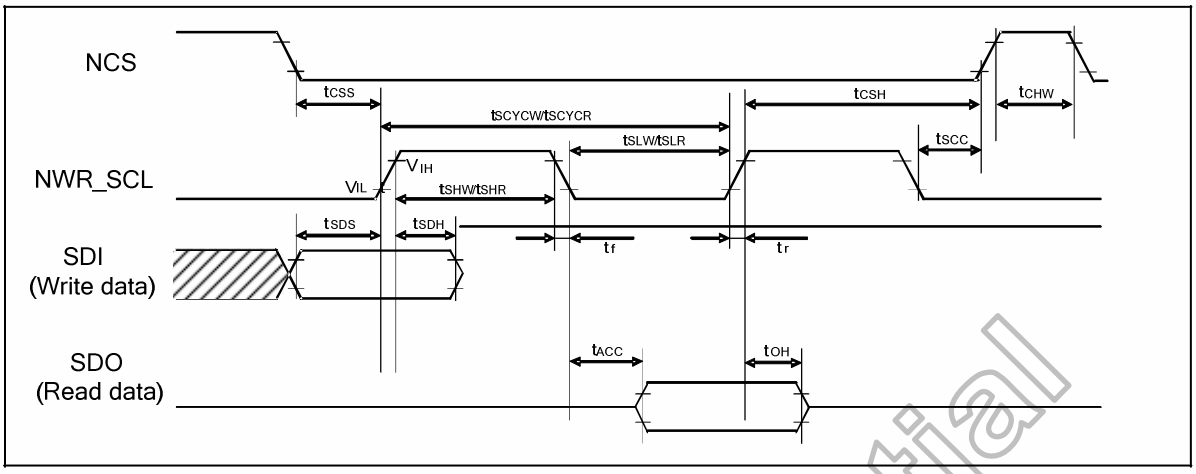


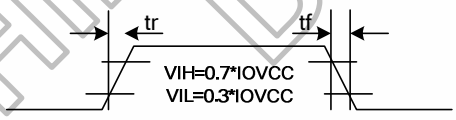
Figure 11.4 Serial interface characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A=-30 to 70°C)

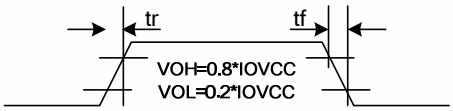
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	SCL	66 15 15	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDI	10 10	- -	- -	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	SCL	150 60 60	- - -	- - -	ns
Access Time	t_{ACC}	SDI for maximum C_L=30pF For minimum C_L=8pF	10	-	80	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For minimum C_L=8pF	15	-	50	ns
SCL to Chip select	t_{SCC}	SCL, NCS	20	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	40	-	-	ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	NCS	60 65	- -	- -	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

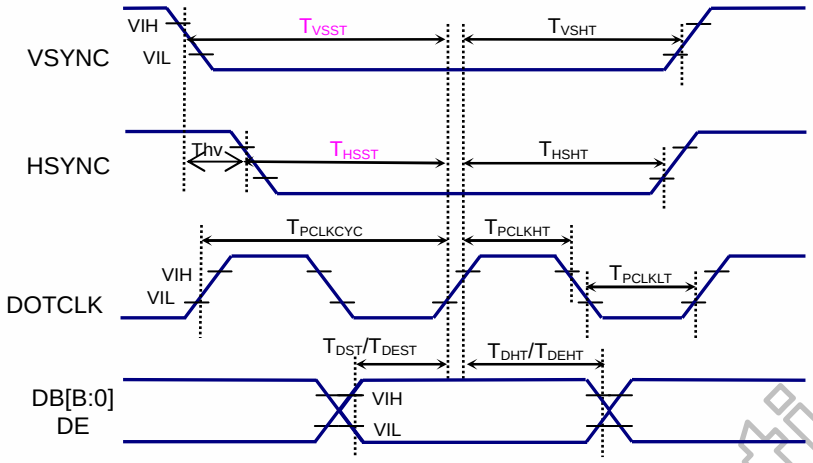
Input Signal Slope



Output Signal Slope



11.4.3 RGB interface characteristics

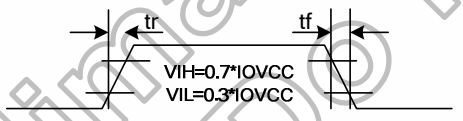


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,T_A=-30 to 70°C)

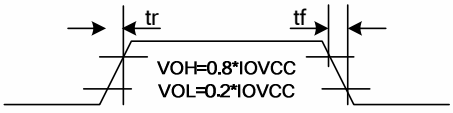
Item	Symbol	Condition	Spec.			Unit
			Min	Type.	Max	
Pixel low pulse width	T_{CLKLT}	-	15	-	-	ns
Pixel high pulse width	T_{CLKHT}	-	15	-	-	ns
Vertical Sync. set-up time	T_{VSST}	-	15	-	-	ns
Vertical Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Horizontal Sync. set-up time	T_{HSST}	-	15	-	-	ns
Horizontal Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Data Enable set-up time	T_{DEST}	-	15	-	-	ns
Data Enable hold time	T_{DEHT}	-	15	-	-	ns
Data set-up time	T_{DST}	-	15	-	-	ns
Data hold time	T_{DHT}	-	15	-	-	ns
Phase difference of sync signal falling edge	Thv	-	0	-	240	Dotclk

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

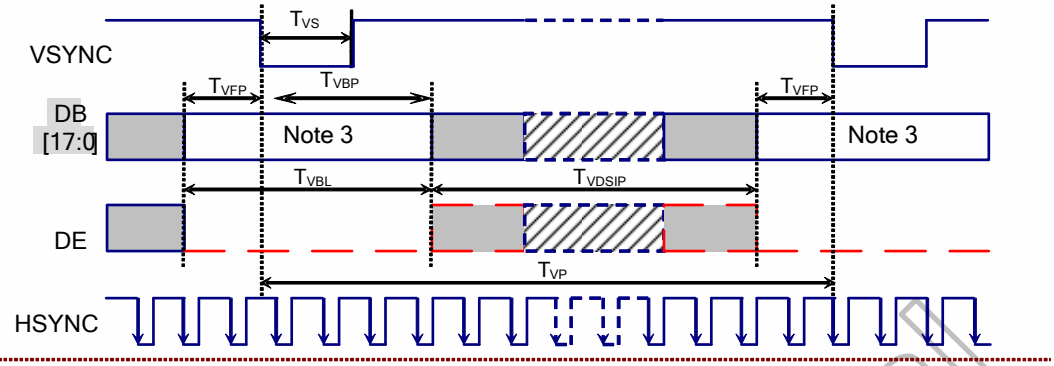
Input Signal Slope



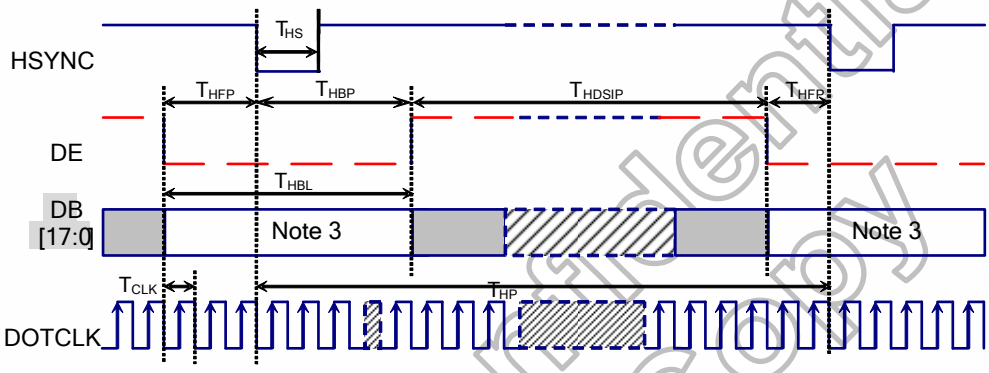
Output Signal Slope



Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F



Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}		324	326	452	HS
Vertical low pulse width	T_{VS}		2	2	-	HS
Vertical front porch	T_{VFP}		2	2	6	HS
Vertical back porch	T_{VBP}		2	4	62	HS
Vertical blanking period	T_{VBL}	$T_{VBP} + T_{VFP}$	4	6	132	HS
Vertical active area	T_{VDISP}			320		HS
						HS
						HS
Vertical refresh rate	TVRR	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}		244	252	1008	DOTCLK
Horizontal low pulse width	T_{HS}		2	2	256	DOTCLK
Horizontal front porch	T_{HFP}		2	4	256	DOTCLK
Horizontal back porch	T_{HBP}		2	8	256	DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP} + T_{HFP}$	4	12	256	DOTCLK
Horizontal active area	T_{HDISP}			240		DOTCLK
Pixel clock cycle TVRR=60Hz	f_{CLKCYC}		3.9		16.6	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, VSSA=VSSD=0V, T_A=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(3) HP is multiples of DOTCLK.

11.4.4 Reset input timing

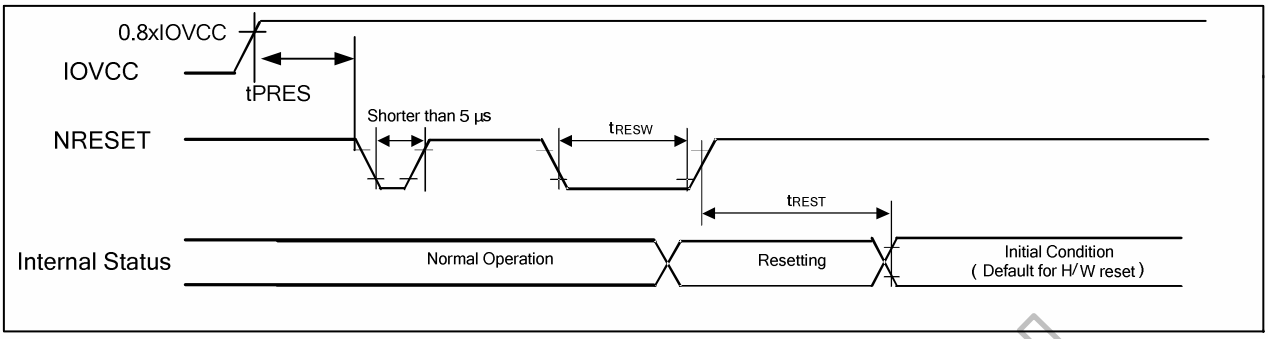


Figure 11.5 Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	5	-	-	After 5ms can set command	ms
		-		-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms

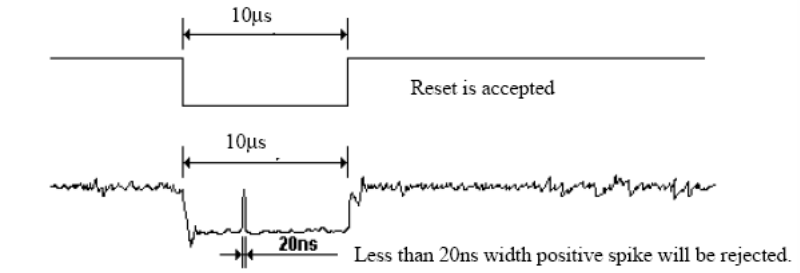
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5 µs and 10µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, VMF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

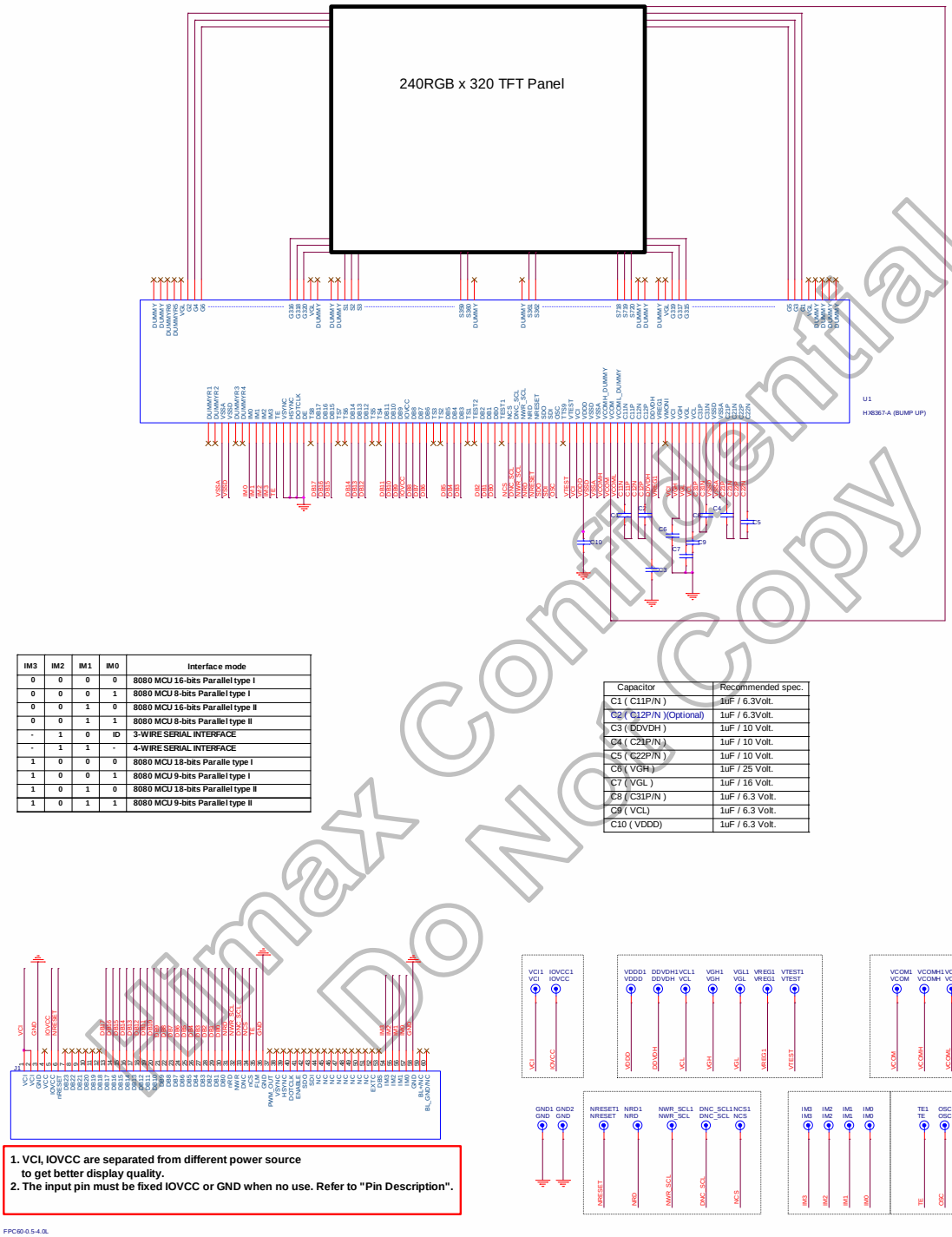
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out

12. Application Circuit

12.1 240RGBx320 MPU application circuit



IM3	IM2	IM1	IM0	Interface mode
0	0	0	0	8080 MCU 16-bits Parallel type I
0	0	0	1	8080 MCU 8-bits Parallel type I
0	0	1	0	8080 MCU 16-bits Parallel type II
0	0	1	1	8080 MCU 8-bits Parallel type II
-	1	0	ID	3-WIRE SERIAL INTERFACE
-	1	1	-	4-WIRE SERIAL INTERFACE
1	0	0	0	8080 MCU 18-bits Paralle type I
1	0	0	1	8080 MCU 9-bits Parallel type I
1	0	1	0	8080 MCU 18-bits Parallel type II
1	0	1	1	8080 MCU 9-bits Parallel type II

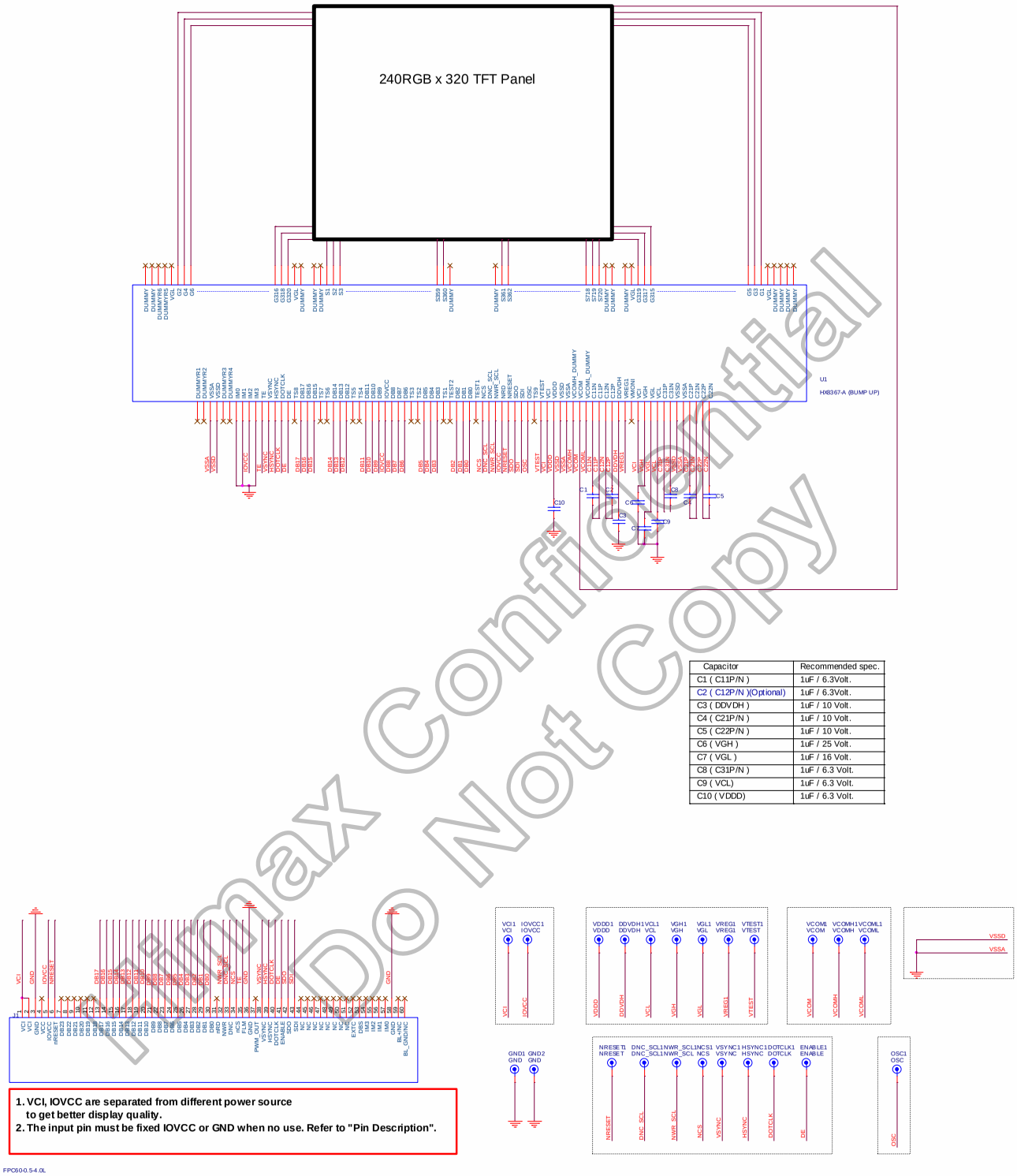
Capacitor	Recommended spec.
C1 (C11P/N)	1uF / 6.3Volt.
C2 (C12P/N)(Optional)	1uF / 6.3Volt.
C3 (DDVDH)	1uF / 10 Volt.
C4 (C21P/N)	1uF / 10 Volt.
C5 (C22P/N)	1uF / 10 Volt.
C6 (VGH)	1uF / 25 Volt.
C7 (VGL)	1uF / 16 Volt.
C8 (C31P/N)	1uF / 6.3 Volt.
C9 (VCL)	1uF / 6.3 Volt.
C10 (VDDD)	1uF / 6.3 Volt.

1. VCI, IOVCC are separated from different power source to get better display quality.
2. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".

FPC60-0.5-4.0L

Figure 12.1 MPU FPC reference circuit

12.2 240RGBx320 SPI+RGB application circuit



Capacitor	Recommended spec.
C1 (C11P/N)	1uF / 6.3Volt.
C2 (C12P/N)(Optional)	1uF / 6.3Volt.
C3 (DDVDH)	1uF / 10 Volt.
C4 (C21P/N)	1uF / 10 Volt.
C5 (C22P/N)	1uF / 10 Volt.
C6 (VGH)	1uF / 25 Volt.
C7 (VGL)	1uF / 16 Volt.
C8 (C31P/N)	1uF / 6.3 Volt.
C9 (VCL)	1uF / 6.3 Volt.
C10 (VDDD)	1uF / 6.3 Volt.

Figure 12.2 SPI+RGB FPC reference circuit

13. Ordering Information

Part No.	Package
HX8367-A000 PDxxx	PD : mean COG xxx : mean chip thickness (μm), (default: 280 μm)

14. Revision History

Version	Date	Description of Changes
01	2009/02/27	New setup
	2009/06/01	1. Modify Figure 10.1 OTP programming sequence in P.153. 2. Modify OSC frequency from 2.85MHz to 2.65MHz. 3. Modify VRH setting table in P.124. 4. Modify RADJ setting table in P.122. 5. Modify D[1:0] setting table in P.133. 6. Modify Figure 7.21 Display On/Off Set Flow in P.102. 7. Modify VMF setting table in P.131. 8. Modify Figure 9.1 Layout Recommendation of HX8367-A in P.151.
	2009/06/05	1. Modify trat max. value to 80ns in P.160.
	2009/06/22	1. Modify VCI voltage from 2.3~3.3V to 2.5~3.3V.
	2009/06/25	1. Modify OSC frequency from 2.65MHz to 2.63MHz.
	2009/06/29	1. Modify T_{VBP} max. from 126 to 62 in P.164.
	2009/07/13	1. Modify t_{AST} min. from 10ns to 0ns in P.160.
	2009/09/14	1. Modify AC characteristic in P.161 and P.163.
	2009/10/22	1. Modify DB17~0 pin description to “The unused pins let to open or connect to IOVCC or VSSD level.” In P.14.
	2009/11/25	1. Remove Figure 8.72 PKP8[4:0] in P.146.
	2011/01/25	1. Add Register RE8h~REDh and RF1h~RF2h description in P.151~P.152.