



» **DATA SHEET**
(DOC No. HX8257-A01-DS)

» **HX8257-A01**
480RGBX272 TFT LCD Single
Chip Digital Driver
Version 01, November 2008

Himax 奇景光電股份有限公司

文件發行及參考文件

TO : 光基

Date : 2008.12.25

DOCUMENT CONTROL CENTER



*Version 01**November 2008*

1. General Description	4
2. Features.....	5
3. Block Diagram	6
4. Pad Assignment.....	7
5. Pad Coordinates	9
6. Pin Description	25
7. Function Description.....	28
7.1 Power relationship.....	28
7.2 VCOM block.....	29
7.3 Gate driver.....	30
7.4 Source driver.....	32
7.5 Gamma adjustment	33
7.5.1 Structure of grayscale amplifier	34
7.5.2 Gamma adjustment register	36
7.5.2.1 Gradient adjusting register.....	36
7.5.2.2 Amplitude adjusting register	36
7.5.2.3 Micro adjusting register	36
7.5.3 Ladder resistor / 8 to 1 selector.....	37
7.6 PWM	41
7.7 TCON.....	42
7.7.1 LR/UD function	43
7.7.2 Aging mode	43
7.7.3 TCON power on/off control.....	43
8. SPI Register	45
9. OTP Programming.....	58
10.DC Characteristics	60
11.AC Characteristics	62
11.1 Timing relationship among DE、Source Output、Gate Output、VCOM.....	62
11.2 Parallel RGB input timing requirement	62
11.3 Serial RGB input timing requirement	65
11.4 Input setup timing requirement	67
12.Application Circuit.....	68
13.Ordering Information.....	69
14.Revision History	69

List of Figures

November 2008

Figure 3.1 Block Diagram	6
Figure 4.1 HX8257-A Die Floor Plan (Bump Face UP)	8
Figure 7.1 Power Block.....	28
Figure 7.2 VGH/VGL External Setting.....	28
Figure 7.3 VCOM Block.....	29
Figure 7.4 Gate Driver.....	30
Figure 7.5 Gate Sequence	31
Figure 7.6 Source Block	32
Figure 7.7 Source Sequence	32
Figure 7.8 Grayscale Control Block	33
Figure 7.9 Grayscale Amplifier.....	34
Figure 7.10 Resistor Ladder for Gamma Voltages Generation.....	35
Figure 7.11 Gamma Adjustment Function	36
Figure 7.12 PWM Block.....	41
Figure 7.13 LR/UD Function	43
Figure 7.14 Power On Sequence	44
Figure 7.15 Power Off Sequence	44
Figure 8.1 Write SPI Timing	45
Figure 8.2 Read SPI Timing	46
Figure 8.3 Vertical Data	54
Figure 8.4 Horizontal Data	55
Figure 9.1 OTP Programming Circuit	59
Figure 10.1 VCIX2 Voltage	61
Figure 11.1 Timing Relationship	62
Figure 12.1 Booster Capacitors (VGH=4VDC/VGL=-2VDC).....	68
Figure 12.2 Voltage Stable Capacitors & Schottky Diode	68

List of Tables

November 2008

Table 7.1 Variable Resistor	37
Table 7.2 PKP and PKN	37
Table 7.3 Grayscale Voltages Formulas	38
Table 7.4 Reference Voltages of Positive Polarity	39
Table 7.5 Reference Voltages of Negative Polarity	40
Table 8.1 Driver Output Control ("x" means default value is set by hardware pin)	47

Himax Confidential
DO NOT COPY

Version 01

November, 2008

1. General Description

The HX8257-A is a single chip digital driver supporting 480RGBX272 or 480RGBX240 resolution. The single chip includes Source, Gate, TCON, and Power circuits. The driver receives 24-bit digital display data with single clock edge and generates corresponding 64 level gray scale voltage outputs with dithering function to realize 16M colors display. Positive and negative polarity voltages can be alternately output from each channel in line (row) inversion driving method.

The HX8257-A can be applied on dual gate TFT LCD panel. Source line is half with 720 channels and gate line is double with 544 or 480-channel outputs.

Himax Confidential
DO NOT COPY

Himax Confidential

This information contained herein is the exclusive property of Himax and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Himax.



November, 2008

2. Features

- Support 480RGBx272 or 480RGBx240 graphics display TFT LCD panel
- 64-gray level with 2 bit dithering function to realize 16M colors
- Support 8-bit serial RGB data and 24-bit parallel RGB data input
- Power supply:
 - VDDIO: 1.8V ~ 3.6V
 - VCI: 3.0V ~ 3.6V
- Built in 1.8V LDO for internal logic circuit
- Maximum gate driving output range: 30Vp-p
- Source output range: 0.1 ~ VLCD - 0.1
- Source and gate scan direction control
- 720-channel source outputs and 544-channel gate outputs
- Programmable gamma correction curve
- Support contrast/brightness adjustment
- Support PAL decimation in 480RGBx240 resolution
- Non-Volatile Memory (OTP) for VCOM calibration
- On-chip DC-DC converter for gate driver VGH/VGL and panel AC VCOM signal
- PWM control function to generate power for backlight
- CABC function is embedded
- COG package

Himax Confidential

3. Block Diagram

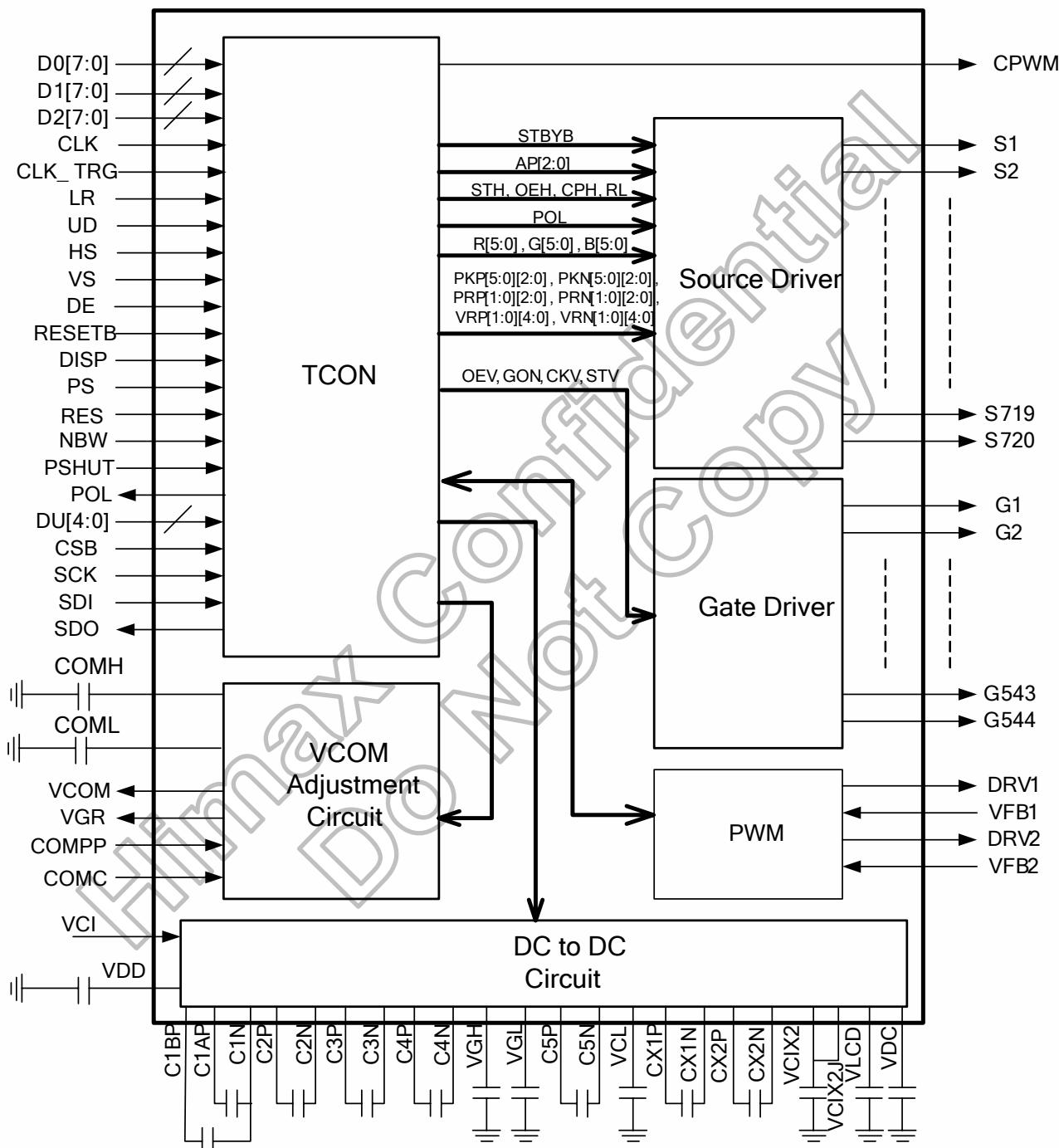
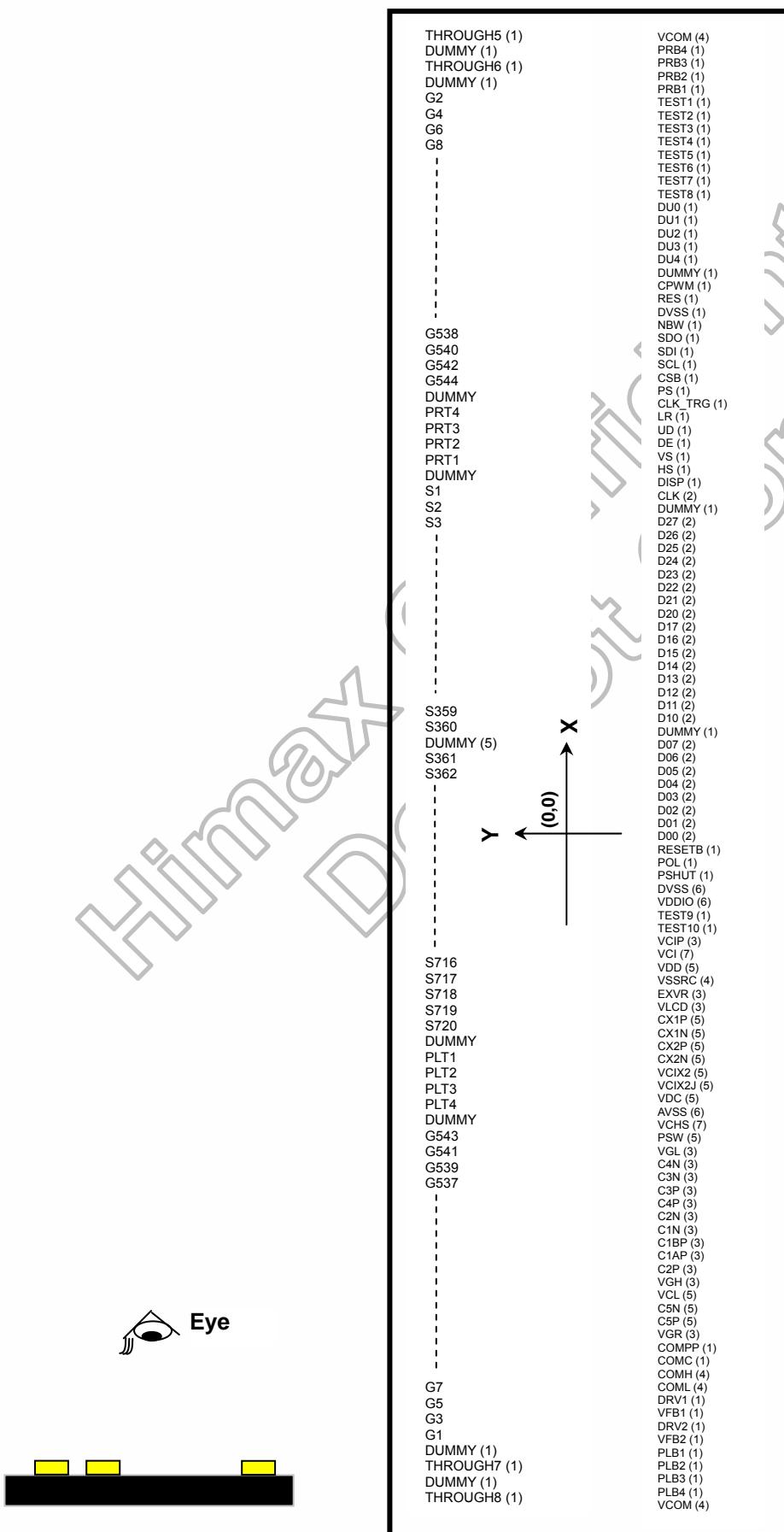


Figure 3.1 Block Diagram

4. Pad Assignment(Gold Bump Face Up)



○ PAD1



DCC文件管制中心

-P7-

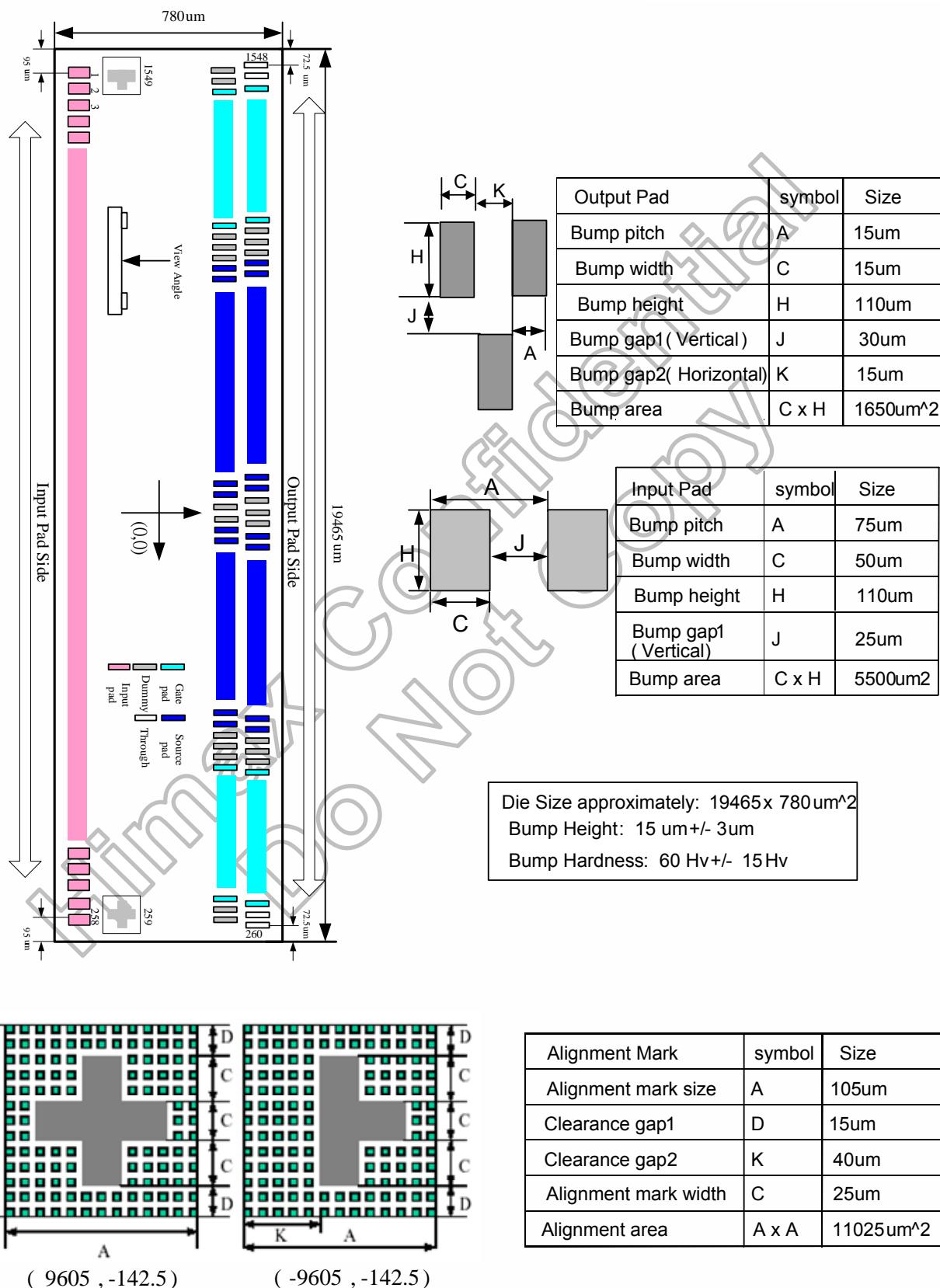


Figure 4.1 HX8257-A Die Floor Plan (Bump Face UP)

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
301	G76	9045	130	15x110	351	G176	8295	130	15x110
302	G78	9030	270	15x110	352	G178	8280	270	15x110
303	G80	9015	130	15x110	353	G180	8265	130	15x110
304	G82	9000	270	15x110	354	G182	8250	270	15x110
305	G84	8985	130	15x110	355	G184	8235	130	15x110
306	G86	8970	270	15x110	356	G186	8220	270	15x110
307	G88	8955	130	15x110	357	G188	8205	130	15x110
308	G90	8940	270	15x110	358	G190	8190	270	15x110
309	G92	8925	130	15x110	359	G192	8175	130	15x110
310	G94	8910	270	15x110	360	G194	8160	270	15x110
311	G96	8895	130	15x110	361	G196	8145	130	15x110
312	G98	8880	270	15x110	362	G198	8130	270	15x110
313	G100	8865	130	15x110	363	G200	8115	130	15x110
314	G102	8850	270	15x110	364	G202	8100	270	15x110
315	G104	8835	130	15x110	365	G204	8085	130	15x110
316	G106	8820	270	15x110	366	G206	8070	270	15x110
317	G108	8805	130	15x110	367	G208	8055	130	15x110
318	G110	8790	270	15x110	368	G210	8040	270	15x110
319	G112	8775	130	15x110	369	G212	8025	130	15x110
320	G114	8760	270	15x110	370	G214	8010	270	15x110
321	G116	8745	130	15x110	371	G216	7995	130	15x110
322	G118	8730	270	15x110	372	G218	7980	270	15x110
323	G120	8715	130	15x110	373	G220	7965	130	15x110
324	G122	8700	270	15x110	374	G222	7950	270	15x110
325	G124	8685	130	15x110	375	G224	7935	130	15x110
326	G126	8670	270	15x110	376	G226	7920	270	15x110
327	G128	8655	130	15x110	377	G228	7905	130	15x110
328	G130	8640	270	15x110	378	G230	7890	270	15x110
329	G132	8625	130	15x110	379	G232	7875	130	15x110
330	G134	8610	270	15x110	380	G234	7860	270	15x110
331	G136	8595	130	15x110	381	G236	7845	130	15x110
332	G138	8580	270	15x110	382	G238	7830	270	15x110
333	G140	8565	130	15x110	383	G240	7815	130	15x110
334	G142	8550	270	15x110	384	G242	7800	270	15x110
335	G144	8535	130	15x110	385	G244	7785	130	15x110
336	G146	8520	270	15x110	386	G246	7770	270	15x110
337	G148	8505	130	15x110	387	G248	7755	130	15x110
338	G150	8490	270	15x110	388	G250	7740	270	15x110
339	G152	8475	130	15x110	389	G252	7725	130	15x110
340	G154	8460	270	15x110	390	G254	7710	270	15x110
341	G156	8445	130	15x110	391	G256	7695	130	15x110
342	G158	8430	270	15x110	392	G258	7680	270	15x110
343	G160	8415	130	15x110	393	G260	7665	130	15x110
344	G162	8400	270	15x110	394	G262	7650	270	15x110
345	G164	8385	130	15x110	395	G264	7635	130	15x110
346	G166	8370	270	15x110	396	G266	7620	270	15x110
347	G168	8355	130	15x110	397	G268	7605	130	15x110
348	G170	8340	270	15x110	398	G270	7590	270	15x110
349	G172	8325	130	15x110	399	G272	7575	130	15x110
350	G174	8310	270	15x110	400	G274	7560	270	15x110

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
401	G276	7545	130	15x110	451	G376	6795	130	15x110
402	G278	7530	270	15x110	452	G378	6780	270	15x110
403	G280	7515	130	15x110	453	G380	6765	130	15x110
404	G282	7500	270	15x110	454	G382	6750	270	15x110
405	G284	7485	130	15x110	455	G384	6735	130	15x110
406	G286	7470	270	15x110	456	G386	6720	270	15x110
407	G288	7455	130	15x110	457	G388	6705	130	15x110
408	G290	7440	270	15x110	458	G390	6690	270	15x110
409	G292	7425	130	15x110	459	G392	6675	130	15x110
410	G294	7410	270	15x110	460	G394	6660	270	15x110
411	G296	7395	130	15x110	461	G396	6645	130	15x110
412	G298	7380	270	15x110	462	G398	6630	270	15x110
413	G300	7365	130	15x110	463	G400	6615	130	15x110
414	G302	7350	270	15x110	464	G402	6600	270	15x110
415	G304	7335	130	15x110	465	G404	6585	130	15x110
416	G306	7320	270	15x110	466	G406	6570	270	15x110
417	G308	7305	130	15x110	467	G408	6555	130	15x110
418	G310	7290	270	15x110	468	G410	6540	270	15x110
419	G312	7275	130	15x110	469	G412	6525	130	15x110
420	G314	7260	270	15x110	470	G414	6510	270	15x110
421	G316	7245	130	15x110	471	G416	6495	130	15x110
422	G318	7230	270	15x110	472	G418	6480	270	15x110
423	G320	7215	130	15x110	473	G420	6465	130	15x110
424	G322	7200	270	15x110	474	G422	6450	270	15x110
425	G324	7185	130	15x110	475	G424	6435	130	15x110
426	G326	7170	270	15x110	476	G426	6420	270	15x110
427	G328	7155	130	15x110	477	G428	6405	130	15x110
428	G330	7140	270	15x110	478	G430	6390	270	15x110
429	G332	7125	130	15x110	479	G432	6375	130	15x110
430	G334	7110	270	15x110	480	G434	6360	270	15x110
431	G336	7095	130	15x110	481	G436	6345	130	15x110
432	G338	7080	270	15x110	482	G438	6330	270	15x110
433	G340	7065	130	15x110	483	G440	6315	130	15x110
434	G342	7050	270	15x110	484	G442	6300	270	15x110
435	G344	7035	130	15x110	485	G444	6285	130	15x110
436	G346	7020	270	15x110	486	G446	6270	270	15x110
437	G348	7005	130	15x110	487	G448	6255	130	15x110
438	G350	6990	270	15x110	488	G450	6240	270	15x110
439	G352	6975	130	15x110	489	G452	6225	130	15x110
440	G354	6960	270	15x110	490	G454	6210	270	15x110
441	G356	6945	130	15x110	491	G456	6195	130	15x110
442	G358	6930	270	15x110	492	G458	6180	270	15x110
443	G360	6915	130	15x110	493	G460	6165	130	15x110
444	G362	6900	270	15x110	494	G462	6150	270	15x110
445	G364	6885	130	15x110	495	G464	6135	130	15x110
446	G366	6870	270	15x110	496	G466	6120	270	15x110
447	G368	6855	130	15x110	497	G468	6105	130	15x110
448	G370	6840	270	15x110	498	G470	6090	270	15x110
449	G372	6825	130	15x110	499	G472	6075	130	15x110
450	G374	6810	270	15x110	500	G474	6060	270	15x110

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
501	G476	6045	130	15x110	551	S10	5295	130	15x110
502	G478	6030	270	15x110	552	S11	5280	270	15x110
503	G480	6015	130	15x110	553	S12	5265	130	15x110
504	G482	6000	270	15x110	554	S13	5250	270	15x110
505	G484	5985	130	15x110	555	S14	5235	130	15x110
506	G486	5970	270	15x110	556	S15	5220	270	15x110
507	G488	5955	130	15x110	557	S16	5205	130	15x110
508	G490	5940	270	15x110	558	S17	5190	270	15x110
509	G492	5925	130	15x110	559	S18	5175	130	15x110
510	G494	5910	270	15x110	560	S19	5160	270	15x110
511	G496	5895	130	15x110	561	S20	5145	130	15x110
512	G498	5880	270	15x110	562	S21	5130	270	15x110
513	G500	5865	130	15x110	563	S22	5115	130	15x110
514	G502	5850	270	15x110	564	S23	5100	270	15x110
515	G504	5835	130	15x110	565	S24	5085	130	15x110
516	G506	5820	270	15x110	566	S25	5070	270	15x110
517	G508	5805	130	15x110	567	S26	5055	130	15x110
518	G510	5790	270	15x110	568	S27	5040	270	15x110
519	G512	5775	130	15x110	569	S28	5025	130	15x110
520	G514	5760	270	15x110	570	S29	5010	270	15x110
521	G516	5745	130	15x110	571	S30	4995	130	15x110
522	G518	5730	270	15x110	572	S31	4980	270	15x110
523	G520	5715	130	15x110	573	S32	4965	130	15x110
524	G522	5700	270	15x110	574	S33	4950	270	15x110
525	G524	5685	130	15x110	575	S34	4935	130	15x110
526	G526	5670	270	15x110	576	S35	4920	270	15x110
527	G528	5655	130	15x110	577	S36	4905	130	15x110
528	G530	5640	270	15x110	578	S37	4890	270	15x110
529	G532	5625	130	15x110	579	S38	4875	130	15x110
530	G534	5610	270	15x110	580	S39	4860	270	15x110
531	G536	5595	130	15x110	581	S40	4845	130	15x110
532	G538	5580	270	15x110	582	S41	4830	270	15x110
533	G540	5565	130	15x110	583	S42	4815	130	15x110
534	G542	5550	270	15x110	584	S43	4800	270	15x110
535	G544	5535	130	15x110	585	S44	4785	130	15x110
536	DUMMY	5520	270	15x110	586	S45	4770	270	15x110
537	PRT4	5505	130	15x110	587	S46	4755	130	15x110
538	PRT3	5490	270	15x110	588	S47	4740	270	15x110
539	PRT2	5475	130	15x110	589	S48	4725	130	15x110
540	PRT1	5460	270	15x110	590	S49	4710	270	15x110
541	DUMMY	5445	130	15x110	591	S50	4695	130	15x110
542	S1	5430	270	15x110	592	S51	4680	270	15x110
543	S2	5415	130	15x110	593	S52	4665	130	15x110
544	S3	5400	270	15x110	594	S53	4650	270	15x110
545	S4	5385	130	15x110	595	S54	4635	130	15x110
546	S5	5370	270	15x110	596	S55	4620	270	15x110
547	S6	5355	130	15x110	597	S56	4605	130	15x110
548	S7	5340	270	15x110	598	S57	4590	270	15x110
549	S8	5325	130	15x110	599	S58	4575	130	15x110
550	S9	5310	270	15x110	600	S59	4560	270	15x110

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
701	S160	3045	130	15x110	751	S210	2295	130	15x110
702	S161	3030	270	15x110	752	S211	2280	270	15x110
703	S162	3015	130	15x110	753	S212	2265	130	15x110
704	S163	3000	270	15x110	754	S213	2250	270	15x110
705	S164	2985	130	15x110	755	S214	2235	130	15x110
706	S165	2970	270	15x110	756	S215	2220	270	15x110
707	S166	2955	130	15x110	757	S216	2205	130	15x110
708	S167	2940	270	15x110	758	S217	2190	270	15x110
709	S168	2925	130	15x110	759	S218	2175	130	15x110
710	S169	2910	270	15x110	760	S219	2160	270	15x110
711	S170	2895	130	15x110	761	S220	2145	130	15x110
712	S171	2880	270	15x110	762	S221	2130	270	15x110
713	S172	2865	130	15x110	763	S222	2115	130	15x110
714	S173	2850	270	15x110	764	S223	2100	270	15x110
715	S174	2835	130	15x110	765	S224	2085	130	15x110
716	S175	2820	270	15x110	766	S225	2070	270	15x110
717	S176	2805	130	15x110	767	S226	2055	130	15x110
718	S177	2790	270	15x110	768	S227	2040	270	15x110
719	S178	2775	130	15x110	769	S228	2025	130	15x110
720	S179	2760	270	15x110	770	S229	2010	270	15x110
721	S180	2745	130	15x110	771	S230	1995	130	15x110
722	S181	2730	270	15x110	772	S231	1980	270	15x110
723	S182	2715	130	15x110	773	S232	1965	130	15x110
724	S183	2700	270	15x110	774	S233	1950	270	15x110
725	S184	2685	130	15x110	775	S234	1935	130	15x110
726	S185	2670	270	15x110	776	S235	1920	270	15x110
727	S186	2655	130	15x110	777	S236	1905	130	15x110
728	S187	2640	270	15x110	778	S237	1890	270	15x110
729	S188	2625	130	15x110	779	S238	1875	130	15x110
730	S189	2610	270	15x110	780	S239	1860	270	15x110
731	S190	2595	130	15x110	781	S240	1845	130	15x110
732	S191	2580	270	15x110	782	S241	1830	270	15x110
733	S192	2565	130	15x110	783	S242	1815	130	15x110
734	S193	2550	270	15x110	784	S243	1800	270	15x110
735	S194	2535	130	15x110	785	S244	1785	130	15x110
736	S195	2520	270	15x110	786	S245	1770	270	15x110
737	S196	2505	130	15x110	787	S246	1755	130	15x110
738	S197	2490	270	15x110	788	S247	1740	270	15x110
739	S198	2475	130	15x110	789	S248	1725	130	15x110
740	S199	2460	270	15x110	790	S249	1710	270	15x110
741	S200	2445	130	15x110	791	S250	1695	130	15x110
742	S201	2430	270	15x110	792	S251	1680	270	15x110
743	S202	2415	130	15x110	793	S252	1665	130	15x110
744	S203	2400	270	15x110	794	S253	1650	270	15x110
745	S204	2385	130	15x110	795	S254	1635	130	15x110
746	S205	2370	270	15x110	796	S255	1620	270	15x110
747	S206	2355	130	15x110	797	S256	1605	130	15x110
748	S207	2340	270	15x110	798	S257	1590	270	15x110
749	S208	2325	130	15x110	799	S258	1575	130	15x110
750	S209	2310	270	15x110	800	S259	1560	270	15x110

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
801	S260	1545	130	15x110	851	S310	795	130	15x110
802	S261	1530	270	15x110	852	S311	780	270	15x110
803	S262	1515	130	15x110	853	S312	765	130	15x110
804	S263	1500	270	15x110	854	S313	750	270	15x110
805	S264	1485	130	15x110	855	S314	735	130	15x110
806	S265	1470	270	15x110	856	S315	720	270	15x110
807	S266	1455	130	15x110	857	S316	705	130	15x110
808	S267	1440	270	15x110	858	S317	690	270	15x110
809	S268	1425	130	15x110	859	S318	675	130	15x110
810	S269	1410	270	15x110	860	S319	660	270	15x110
811	S270	1395	130	15x110	861	S320	645	130	15x110
812	S271	1380	270	15x110	862	S321	630	270	15x110
813	S272	1365	130	15x110	863	S322	615	130	15x110
814	S273	1350	270	15x110	864	S323	600	270	15x110
815	S274	1335	130	15x110	865	S324	585	130	15x110
816	S275	1320	270	15x110	866	S325	570	270	15x110
817	S276	1305	130	15x110	867	S326	555	130	15x110
818	S277	1290	270	15x110	868	S327	540	270	15x110
819	S278	1275	130	15x110	869	S328	525	130	15x110
820	S279	1260	270	15x110	870	S329	510	270	15x110
821	S280	1245	130	15x110	871	S330	495	130	15x110
822	S281	1230	270	15x110	872	S331	480	270	15x110
823	S282	1215	130	15x110	873	S332	465	130	15x110
824	S283	1200	270	15x110	874	S333	450	270	15x110
825	S284	1185	130	15x110	875	S334	435	130	15x110
826	S285	1170	270	15x110	876	S335	420	270	15x110
827	S286	1155	130	15x110	877	S336	405	130	15x110
828	S287	1140	270	15x110	878	S337	390	270	15x110
829	S288	1125	130	15x110	879	S338	375	130	15x110
830	S289	1110	270	15x110	880	S339	360	270	15x110
831	S290	1095	130	15x110	881	S340	345	130	15x110
832	S291	1080	270	15x110	882	S341	330	270	15x110
833	S292	1065	130	15x110	883	S342	315	130	15x110
834	S293	1050	270	15x110	884	S343	300	270	15x110
835	S294	1035	130	15x110	885	S344	285	130	15x110
836	S295	1020	270	15x110	886	S345	270	270	15x110
837	S296	1005	130	15x110	887	S346	255	130	15x110
838	S297	990	270	15x110	888	S347	240	270	15x110
839	S298	975	130	15x110	889	S348	225	130	15x110
840	S299	960	270	15x110	890	S349	210	270	15x110
841	S300	945	130	15x110	891	S350	195	130	15x110
842	S301	930	270	15x110	892	S351	180	270	15x110
843	S302	915	130	15x110	893	S352	165	130	15x110
844	S303	900	270	15x110	894	S353	150	270	15x110
845	S304	885	130	15x110	895	S354	135	130	15x110
846	S305	870	270	15x110	896	S355	120	270	15x110
847	S306	855	130	15x110	897	S356	105	130	15x110
848	S307	840	270	15x110	898	S357	90	270	15x110
849	S308	825	130	15x110	899	S358	75	130	15x110
850	S309	810	270	15x110	900	S359	60	270	15x110

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
1001	S455	-1455	130	15x110	1051	S505	-2205	130	15x110
1002	S456	-1470	270	15x110	1052	S506	-2220	270	15x110
1003	S457	-1485	130	15x110	1053	S507	-2235	130	15x110
1004	S458	-1500	270	15x110	1054	S508	-2250	270	15x110
1005	S459	-1515	130	15x110	1055	S509	-2265	130	15x110
1006	S460	-1530	270	15x110	1056	S510	-2280	270	15x110
1007	S461	-1545	130	15x110	1057	S511	-2295	130	15x110
1008	S462	-1560	270	15x110	1058	S512	-2310	270	15x110
1009	S463	-1575	130	15x110	1059	S513	-2325	130	15x110
1010	S464	-1590	270	15x110	1060	S514	-2340	270	15x110
1011	S465	-1605	130	15x110	1061	S515	-2355	130	15x110
1012	S466	-1620	270	15x110	1062	S516	-2370	270	15x110
1013	S467	-1635	130	15x110	1063	S517	-2385	130	15x110
1014	S468	-1650	270	15x110	1064	S518	-2400	270	15x110
1015	S469	-1665	130	15x110	1065	S519	-2415	130	15x110
1016	S470	-1680	270	15x110	1066	S520	-2430	270	15x110
1017	S471	-1695	130	15x110	1067	S521	-2445	130	15x110
1018	S472	-1710	270	15x110	1068	S522	-2460	270	15x110
1019	S473	-1725	130	15x110	1069	S523	-2475	130	15x110
1020	S474	-1740	270	15x110	1070	S524	-2490	270	15x110
1021	S475	-1755	130	15x110	1071	S525	-2505	130	15x110
1022	S476	-1770	270	15x110	1072	S526	-2520	270	15x110
1023	S477	-1785	130	15x110	1073	S527	-2535	130	15x110
1024	S478	-1800	270	15x110	1074	S528	-2550	270	15x110
1025	S479	-1815	130	15x110	1075	S529	-2565	130	15x110
1026	S480	-1830	270	15x110	1076	S530	-2580	270	15x110
1027	S481	-1845	130	15x110	1077	S531	-2595	130	15x110
1028	S482	-1860	270	15x110	1078	S532	-2610	270	15x110
1029	S483	-1875	130	15x110	1079	S533	-2625	130	15x110
1030	S484	-1890	270	15x110	1080	S534	-2640	270	15x110
1031	S485	-1905	130	15x110	1081	S535	-2655	130	15x110
1032	S486	-1920	270	15x110	1082	S536	-2670	270	15x110
1033	S487	-1935	130	15x110	1083	S537	-2685	130	15x110
1034	S488	-1950	270	15x110	1084	S538	-2700	270	15x110
1035	S489	-1965	130	15x110	1085	S539	-2715	130	15x110
1036	S490	-1980	270	15x110	1086	S540	-2730	270	15x110
1037	S491	-1995	130	15x110	1087	S541	-2745	130	15x110
1038	S492	-2010	270	15x110	1088	S542	-2760	270	15x110
1039	S493	-2025	130	15x110	1089	S543	-2775	130	15x110
1040	S494	-2040	270	15x110	1090	S544	-2790	270	15x110
1041	S495	-2055	130	15x110	1091	S545	-2805	130	15x110
1042	S496	-2070	270	15x110	1092	S546	-2820	270	15x110
1043	S497	-2085	130	15x110	1093	S547	-2835	130	15x110
1044	S498	-2100	270	15x110	1094	S548	-2850	270	15x110
1045	S499	-2115	130	15x110	1095	S549	-2865	130	15x110
1046	S500	-2130	270	15x110	1096	S550	-2880	270	15x110
1047	S501	-2145	130	15x110	1097	S551	-2895	130	15x110
1048	S502	-2160	270	15x110	1098	S552	-2910	270	15x110
1049	S503	-2175	130	15x110	1099	S553	-2925	130	15x110
1050	S504	-2190	270	15x110	1100	S554	-2940	270	15x110

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
1101	S555	-2955	130	15x110	1151	S605	-3705	130	15x110
1102	S556	-2970	270	15x110	1152	S606	-3720	270	15x110
1103	S557	-2985	130	15x110	1153	S607	-3735	130	15x110
1104	S558	-3000	270	15x110	1154	S608	-3750	270	15x110
1105	S559	-3015	130	15x110	1155	S609	-3765	130	15x110
1106	S560	-3030	270	15x110	1156	S610	-3780	270	15x110
1107	S561	-3045	130	15x110	1157	S611	-3795	130	15x110
1108	S562	-3060	270	15x110	1158	S612	-3810	270	15x110
1109	S563	-3075	130	15x110	1159	S613	-3825	130	15x110
1110	S564	-3090	270	15x110	1160	S614	-3840	270	15x110
1111	S565	-3105	130	15x110	1161	S615	-3855	130	15x110
1112	S566	-3120	270	15x110	1162	S616	-3870	270	15x110
1113	S567	-3135	130	15x110	1163	S617	-3885	130	15x110
1114	S568	-3150	270	15x110	1164	S618	-3900	270	15x110
1115	S569	-3165	130	15x110	1165	S619	-3915	130	15x110
1116	S570	-3180	270	15x110	1166	S620	-3930	270	15x110
1117	S571	-3195	130	15x110	1167	S621	-3945	130	15x110
1118	S572	-3210	270	15x110	1168	S622	-3960	270	15x110
1119	S573	-3225	130	15x110	1169	S623	-3975	130	15x110
1120	S574	-3240	270	15x110	1170	S624	-3990	270	15x110
1121	S575	-3255	130	15x110	1171	S625	-4005	130	15x110
1122	S576	-3270	270	15x110	1172	S626	-4020	270	15x110
1123	S577	-3285	130	15x110	1173	S627	-4035	130	15x110
1124	S578	-3300	270	15x110	1174	S628	-4050	270	15x110
1125	S579	-3315	130	15x110	1175	S629	-4065	130	15x110
1126	S580	-3330	270	15x110	1176	S630	-4080	270	15x110
1127	S581	-3345	130	15x110	1177	S631	-4095	130	15x110
1128	S582	-3360	270	15x110	1178	S632	-4110	270	15x110
1129	S583	-3375	130	15x110	1179	S633	-4125	130	15x110
1130	S584	-3390	270	15x110	1180	S634	-4140	270	15x110
1131	S585	-3405	130	15x110	1181	S635	-4155	130	15x110
1132	S586	-3420	270	15x110	1182	S636	-4170	270	15x110
1133	S587	-3435	130	15x110	1183	S637	-4185	130	15x110
1134	S588	-3450	270	15x110	1184	S638	-4200	270	15x110
1135	S589	-3465	130	15x110	1185	S639	-4215	130	15x110
1136	S590	-3480	270	15x110	1186	S640	-4230	270	15x110
1137	S591	-3495	130	15x110	1187	S641	-4245	130	15x110
1138	S592	-3510	270	15x110	1188	S642	-4260	270	15x110
1139	S593	-3525	130	15x110	1189	S643	-4275	130	15x110
1140	S594	-3540	270	15x110	1190	S644	-4290	270	15x110
1141	S595	-3555	130	15x110	1191	S645	-4305	130	15x110
1142	S596	-3570	270	15x110	1192	S646	-4320	270	15x110
1143	S597	-3585	130	15x110	1193	S647	-4335	130	15x110
1144	S598	-3600	270	15x110	1194	S648	-4350	270	15x110
1145	S599	-3615	130	15x110	1195	S649	-4365	130	15x110
1146	S600	-3630	270	15x110	1196	S650	-4380	270	15x110
1147	S601	-3645	130	15x110	1197	S651	-4395	130	15x110
1148	S602	-3660	270	15x110	1198	S652	-4410	270	15x110
1149	S603	-3675	130	15x110	1199	S653	-4425	130	15x110
1150	S604	-3690	270	15x110	1200	S654	-4440	270	15x110

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
1201	S655	-4455	130	15x110	1251	S705	-5205	130	15x110
1202	S656	-4470	270	15x110	1252	S706	-5220	270	15x110
1203	S657	-4485	130	15x110	1253	S707	-5235	130	15x110
1204	S658	-4500	270	15x110	1254	S708	-5250	270	15x110
1205	S659	-4515	130	15x110	1255	S709	-5265	130	15x110
1206	S660	-4530	270	15x110	1256	S710	-5280	270	15x110
1207	S661	-4545	130	15x110	1257	S711	-5295	130	15x110
1208	S662	-4560	270	15x110	1258	S712	-5310	270	15x110
1209	S663	-4575	130	15x110	1259	S713	-5325	130	15x110
1210	S664	-4590	270	15x110	1260	S714	-5340	270	15x110
1211	S665	-4605	130	15x110	1261	S715	-5355	130	15x110
1212	S666	-4620	270	15x110	1262	S716	-5370	270	15x110
1213	S667	-4635	130	15x110	1263	S717	-5385	130	15x110
1214	S668	-4650	270	15x110	1264	S718	-5400	270	15x110
1215	S669	-4665	130	15x110	1265	S719	-5415	130	15x110
1216	S670	-4680	270	15x110	1266	S720	-5430	270	15x110
1217	S671	-4695	130	15x110	1267	DUMMY	-5445	130	15x110
1218	S672	-4710	270	15x110	1268	PLT1	-5460	270	15x110
1219	S673	-4725	130	15x110	1269	PLT2	-5475	130	15x110
1220	S674	-4740	270	15x110	1270	PLT3	-5490	270	15x110
1221	S675	-4755	130	15x110	1271	PLT4	-5505	130	15x110
1222	S676	-4770	270	15x110	1272	DUMMY	-5520	270	15x110
1223	S677	-4785	130	15x110	1273	G543	-5535	130	15x110
1224	S678	-4800	270	15x110	1274	G541	-5550	270	15x110
1225	S679	-4815	130	15x110	1275	G539	-5565	130	15x110
1226	S680	-4830	270	15x110	1276	G537	-5580	270	15x110
1227	S681	-4845	130	15x110	1277	G535	-5595	130	15x110
1228	S682	-4860	270	15x110	1278	G533	-5610	270	15x110
1229	S683	-4875	130	15x110	1279	G531	-5625	130	15x110
1230	S684	-4890	270	15x110	1280	G529	-5640	270	15x110
1231	S685	-4905	130	15x110	1281	G527	-5655	130	15x110
1232	S686	-4920	270	15x110	1282	G525	-5670	270	15x110
1233	S687	-4935	130	15x110	1283	G523	-5685	130	15x110
1234	S688	-4950	270	15x110	1284	G521	-5700	270	15x110
1235	S689	-4965	130	15x110	1285	G519	-5715	130	15x110
1236	S690	-4980	270	15x110	1286	G517	-5730	270	15x110
1237	S691	-4995	130	15x110	1287	G515	-5745	130	15x110
1238	S692	-5010	270	15x110	1288	G513	-5760	270	15x110
1239	S693	-5025	130	15x110	1289	G511	-5775	130	15x110
1240	S694	-5040	270	15x110	1290	G509	-5790	270	15x110
1241	S695	-5055	130	15x110	1291	G507	-5805	130	15x110
1242	S696	-5070	270	15x110	1292	G505	-5820	270	15x110
1243	S697	-5085	130	15x110	1293	G503	-5835	130	15x110
1244	S698	-5100	270	15x110	1294	G501	-5850	270	15x110
1245	S699	-5115	130	15x110	1295	G499	-5865	130	15x110
1246	S700	-5130	270	15x110	1296	G497	-5880	270	15x110
1247	S701	-5145	130	15x110	1297	G495	-5895	130	15x110
1248	S702	-5160	270	15x110	1298	G493	-5910	270	15x110
1249	S703	-5175	130	15x110	1299	G491	-5925	130	15x110
1250	S704	-5190	270	15x110	1300	G489	-5940	270	15x110

No.	Name	X	Y	Bump Size	No.	Name	X	Y	Bump Size
1401	G287	-7455	130	15x110	1451	G187	-8205	130	15x110
1402	G285	-7470	270	15x110	1452	G185	-8220	270	15x110
1403	G283	-7485	130	15x110	1453	G183	-8235	130	15x110
1404	G281	-7500	270	15x110	1454	G181	-8250	270	15x110
1405	G279	-7515	130	15x110	1455	G179	-8265	130	15x110
1406	G277	-7530	270	15x110	1456	G177	-8280	270	15x110
1407	G275	-7545	130	15x110	1457	G175	-8295	130	15x110
1408	G273	-7560	270	15x110	1458	G173	-8310	270	15x110
1409	G271	-7575	130	15x110	1459	G171	-8325	130	15x110
1410	G269	-7590	270	15x110	1460	G169	-8340	270	15x110
1411	G267	-7605	130	15x110	1461	G167	-8355	130	15x110
1412	G265	-7620	270	15x110	1462	G165	-8370	270	15x110
1413	G263	-7635	130	15x110	1463	G163	-8385	130	15x110
1414	G261	-7650	270	15x110	1464	G161	-8400	270	15x110
1415	G259	-7665	130	15x110	1465	G159	-8415	130	15x110
1416	G257	-7680	270	15x110	1466	G157	-8430	270	15x110
1417	G255	-7695	130	15x110	1467	G155	-8445	130	15x110
1418	G253	-7710	270	15x110	1468	G153	-8460	270	15x110
1419	G251	-7725	130	15x110	1469	G151	-8475	130	15x110
1420	G249	-7740	270	15x110	1470	G149	-8490	270	15x110
1421	G247	-7755	130	15x110	1471	G147	-8505	130	15x110
1422	G245	-7770	270	15x110	1472	G145	-8520	270	15x110
1423	G243	-7785	130	15x110	1473	G143	-8535	130	15x110
1424	G241	-7800	270	15x110	1474	G141	-8550	270	15x110
1425	G239	-7815	130	15x110	1475	G139	-8565	130	15x110
1426	G237	-7830	270	15x110	1476	G137	-8580	270	15x110
1427	G235	-7845	130	15x110	1477	G135	-8595	130	15x110
1428	G233	-7860	270	15x110	1478	G133	-8610	270	15x110
1429	G231	-7875	130	15x110	1479	G131	-8625	130	15x110
1430	G229	-7890	270	15x110	1480	G129	-8640	270	15x110
1431	G227	-7905	130	15x110	1481	G127	-8655	130	15x110
1432	G225	-7920	270	15x110	1482	G125	-8670	270	15x110
1433	G223	-7935	130	15x110	1483	G123	-8685	130	15x110
1434	G221	-7950	270	15x110	1484	G121	-8700	270	15x110
1435	G219	-7965	130	15x110	1485	G119	-8715	130	15x110
1436	G217	-7980	270	15x110	1486	G117	-8730	270	15x110
1437	G215	-7995	130	15x110	1487	G115	-8745	130	15x110
1438	G213	-8010	270	15x110	1488	G113	-8760	270	15x110
1439	G211	-8025	130	15x110	1489	G111	-8775	130	15x110
1440	G209	-8040	270	15x110	1490	G109	-8790	270	15x110
1441	G207	-8055	130	15x110	1491	G107	-8805	130	15x110
1442	G205	-8070	270	15x110	1492	G105	-8820	270	15x110
1443	G203	-8085	130	15x110	1493	G103	-8835	130	15x110
1444	G201	-8100	270	15x110	1494	G101	-8850	270	15x110
1445	G199	-8115	130	15x110	1495	G99	-8865	130	15x110
1446	G197	-8130	270	15x110	1496	G97	-8880	270	15x110
1447	G195	-8145	130	15x110	1497	G95	-8895	130	15x110
1448	G193	-8160	270	15x110	1498	G93	-8910	270	15x110
1449	G191	-8175	130	15x110	1499	G91	-8925	130	15x110
1450	G189	-8190	270	15x110	1500	G89	-8940	270	15x110

No.	Name	X	Y	Bump Size
1501	G87	-8955	130	15x110
1502	G85	-8970	270	15x110
1503	G83	-8985	130	15x110
1504	G81	-9000	270	15x110
1505	G79	-9015	130	15x110
1506	G77	-9030	270	15x110
1507	G75	-9045	130	15x110
1508	G73	-9060	270	15x110
1509	G71	-9075	130	15x110
1510	G69	-9090	270	15x110
1511	G67	-9105	130	15x110
1512	G65	-9120	270	15x110
1513	G63	-9135	130	15x110
1514	G61	-9150	270	15x110
1515	G59	-9165	130	15x110
1516	G57	-9180	270	15x110
1517	G55	-9195	130	15x110
1518	G53	-9210	270	15x110
1519	G51	-9225	130	15x110
1520	G49	-9240	270	15x110
1521	G47	-9255	130	15x110
1522	G45	-9270	270	15x110
1523	G43	-9285	130	15x110
1524	G41	-9300	270	15x110
1525	G39	-9315	130	15x110
1526	G37	-9330	270	15x110
1527	G35	-9345	130	15x110
1528	G33	-9360	270	15x110
1529	G31	-9375	130	15x110
1530	G29	-9390	270	15x110
1531	G27	-9405	130	15x110
1532	G25	-9420	270	15x110
1533	G23	-9435	130	15x110
1534	G21	-9450	270	15x110
1535	G19	-9465	130	15x110
1536	G17	-9480	270	15x110
1537	G15	-9495	130	15x110
1538	G13	-9510	270	15x110
1539	G11	-9525	130	15x110
1540	G9	-9540	270	15x110
1541	G7	-9555	130	15x110
1542	G5	-9570	270	15x110
1543	G3	-9585	130	15x110
1544	G1	-9600	270	15x110
1545	DUMMY	-9615	130	15x110
1546	THROUGH7	-9630	270	15x110
1547	DUMMY	-9645	130	15x110
1548	THROUGH8	-9660	270	15x110
1549	L_MARK	-9605	-142.5	NA

Himax Confidential

This information contained herein is the exclusive property of Himax and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Himax.



November, 2008

6. Pin Description

Pin name	I/O	Description
S[1:720]	O	Source driver output.
D27~D20 D17~D10 D07~D00	I	Digital data input. Internally pulled low. (a) PS=H (parallel RGB interface): Dx7~Dx0 are used. (b) PS=L (serial RGB interface): only D07~D00 are used.
G[1:544]	O	Gate driver output. If RES=L, G481 ~ G544 are disabled.
LR	I	Shift direction selection signal. Internally pulled high. Shift direction of the internal shift register is controlled by this pin as shown below: (a) LR=H: S1→S2→•••→S720 (b) LR=L: S720→S719→•••→S1
UD	I	Scan direction selection signal. Internally pulled high. (a) UD=H: G1→G2→•••→G544 (b) UD=L: G544→G543→•••→G1
CLK	I	Clock signal for data latching and internal counter of the timing controller.
CLK_TRG	I	Clock edge selection signal for the data sampling. Internally pulled high. (a) CLK_TRG=H: Data sampling at the CLK falling edge. (b) CLK_TRG=L: Data sampling at the CLK rising edge.
HS	I	Horizontal sync input with negative polarity. Internally pull high.
VS	I	Vertical sync input with negative polarity. Internally pull high.
DE	I	Input data enable control. Internally pulled low.
DISP	I	Display on/off mode control. Internally pulled high. (a) DISP=L, standby mode. (b) DISP=H, normal display mode.
RESETB	I	Active low global reset signal input. Internally pulled high.
PS	I	Input data format select signal. Internally pulled high. (a) PS=H: Parallel RGB (b) PS=L: Serial RGB
RES	I	Resolution select signal. Internally pulled high. (a) RES=H: 480RGB x 272 (b) RES=L: 480RGB x 240
NBW	I	LC type selection. Internally pulled high. (a) NBW=H: Normally black LC. (b) NBW=L: Normally white LC.
POL	O	Polarity signal to monitor VCOM signal.
PSHUT	I	Input pin to enable internal charge pump circuit. Internal pull high. - Connect to VDDIO to enable internal charge pump VCL, VGH, VGL, VCIX2 and VCOM. - Connect to DVSS to disable internal charge pump VGH, VGL, VCIX2 and VCOM.
CSB	I	Chip select pin of serial interface. Internal pull high. - Leave it OPEN when not used (Refer to Serial Interface block)
SCL	I	Clock pin of serial interface. Internal pull high. - Leave it OPEN when not used (Refer to Serial Interface block)
SDI	I	Data input pin in serial mode. Internal pull high. - Leave it OPEN when not used (Refer to Serial Interface block)
SDO	O	Data output pin in serial mode. - Leave it OPEN when not used (Refer to Serial Interface block)

Himax奇景光電

2008.12.25

DCC文件管制中心

P25

Pin name	I/O	Description
VGR	O	Output pin of internal regulator circuit.
COMH	O	Output pin of regulator for COMMON output high level.
COML	O	Output pin of regulator for COMMON output low level.
COMPP	I	Adjust the amplitude voltage level for COMMON output. If not used, please leave it open.
COMC	I	Adjust the DC voltage level for COMMON output. If not used, please leave it open.
VCOM	O	This is output pin for COMMON signal of a TFT panel.
VDDIO	VI	Voltage input pin for I/O logic.
VCI	VI	Booster input voltage pin.
VCIP	VI	Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. Can be connected to VCI on system board or FPC.
VDD	V	Internal regulator output voltage for logic circuit. Connect a capacitor for stabilization.
VCIX2	V	Equal to 2 x VCI. Connect a capacitor for stabilization.
VCIX2J	V	This is the power supply used for analog blocks and VLCD/VDC regulation.
VLCD	V	Internal generated power for gamma circuit. Connect a capacitor for stabilization.
VDC	V	Power for reference voltage of VGH/VGL pumping.
VGH	V	Positive power pin for gate driver.
VGL	V	Negative power pin for gate driver.
VCL	V	Negative voltage of VCI. Connect a capacitor for stabilization.
C1AP/C1BP, C1N, C2P, C2N C3P, C3N C4P, C4N C5P, C5N CX1P, CX1N CX2P, CX2N	I	Connect 0.1uF capacitor between CnP and CnN pins.
DVSS	VI	Digital ground.
AVSS	VI	Analog ground.
VCHS	VI	Ground for booster circuit.
VSSRC	VI	Ground for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages.
EXVR	I	External reference of internal gamma resistor.
DRV1	O	Power transistor gate signal for the boost converter 1. 1 st PWM can be used for LED backlight power.
VFB1	I	Main boost regulator feedback input 1. Connect feedback resistive divider to GND. If 1 st PWM is not used, please connect VFB1 to GND. VFB1 default threshold is 1.0 V.

Himax奇景光電

2008.12.25

DCC文件管制中心

P26

Pin name	I/O	Description
DRV2	O	Power transistor gate signal for the boost converter 2. 2 nd PWM can be used for generate VCIX2J power if needed.
VFB2	I	Main boost regulator feedback input 2. Connect feedback resistive divider to GND. If 2 nd PWM is not used, please connect VFB2 to GND. VFB2 default threshold is 1.0 V.
DU[4:0]	I	Set 1 st PWM duty cycle for LED backlight. This setting is only effective when DUS bit = 1(R05h). If this function is not used, connect DU[4:0] to VDDIO or floating them. Internally pull high.
CPWM	O	Duty cycle control signal of CABC function output.
PSW	I	Internal switch input. This is used only for 2 nd PWM (PWM B). If 2 nd PWM is not used, please leave it open.
TEST1~10	O	Test pins. Floating it on panel.
PRT1	-	Dummy pads. These two pins are short circuited within the chip
PRB1	-	
PRT2	-	Dummy pads. These two pins are short circuited within the chip
PRB2	-	
PRT3	-	Dummy pads. These two pins are short circuited within the chip
PRB3	-	
PRT4	-	Dummy pads. These two pins are short circuited within the chip
PRB4	-	
PLT1	-	Dummy pads. These two pins are short circuited within the chip
PLB1	-	
PLT2	-	Dummy pads. These two pins are short circuited within the chip
PLB2	-	
PLT3	-	Dummy pads. These two pins are short circuited within the chip
PLB3	-	
PLT4	-	Dummy pads. These two pins are short circuited within the chip
PLB4	-	
THROUGH5	-	Dummy pads. Used to measure the COG contact resistance. These two pins are short circuited within the chip
THROUGH6	-	
THROUGH7	-	Dummy pads. Used to measure the COG contact resistance. These two pins are short circuited within the chip
THROUGH8	-	
DUMMY	-	Dummy pins. Floating it on panel.

7. Function Description

7.1 Power relationship

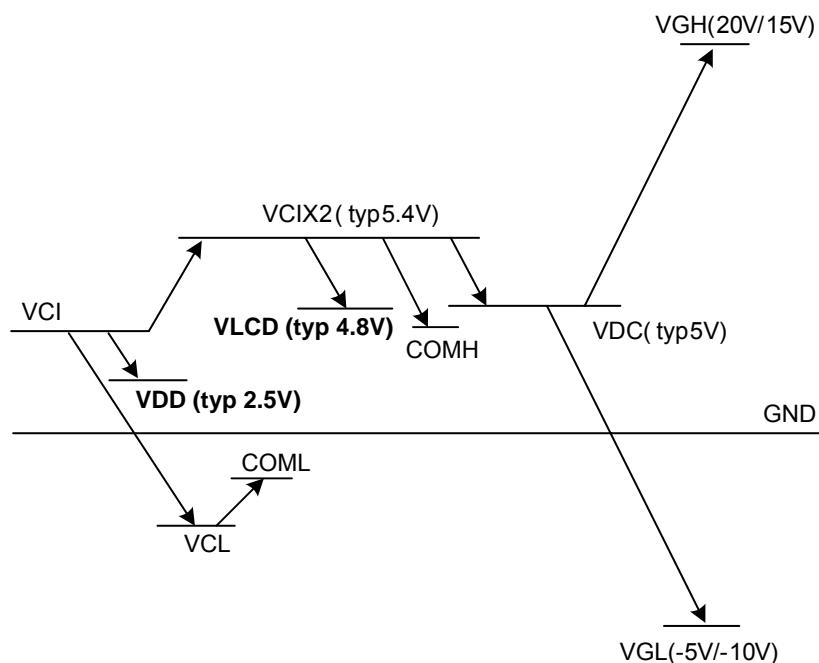


Figure 7.1 Power Block

You can get different VGH/VGL voltage by following different component configuration.

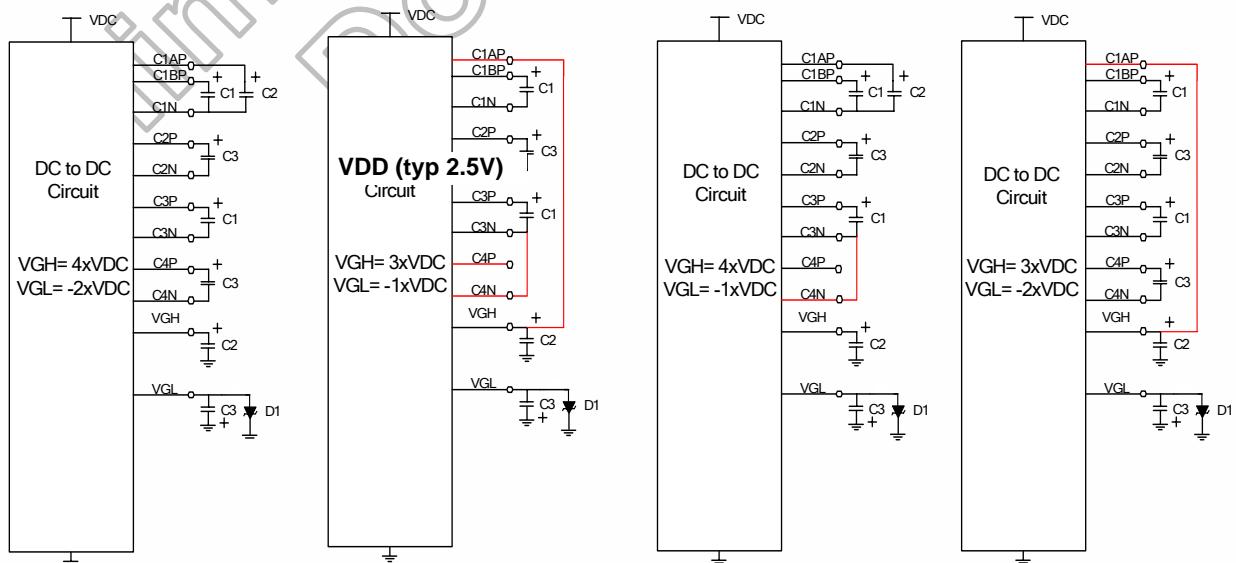


Figure 7.2 VGH/VGL External Setting

7.2 VCOM block

You can use internal circuit to generate COMPP and COMC voltage level. Register VDV[4:0] and VMC[4:0] are used to adjust COMPP and COMC voltage. If you want to set COMPP and COMC voltage level from external, just set VDV[4:0]=00000 and VMC[4:0]=00000. Then you can input COMPP and COMC from hardware pins. The HX8257-A has a regulator circuit for VGR output power level. Connect VGR with outside resistor strings. These resistor strings can generate COMPP and COMC voltage levels for internal VCOM generation circuit. VGR voltage level is 4.5V. (Typ.) If COMC/COMPP is generated internally, VGR circuit will be disabled.

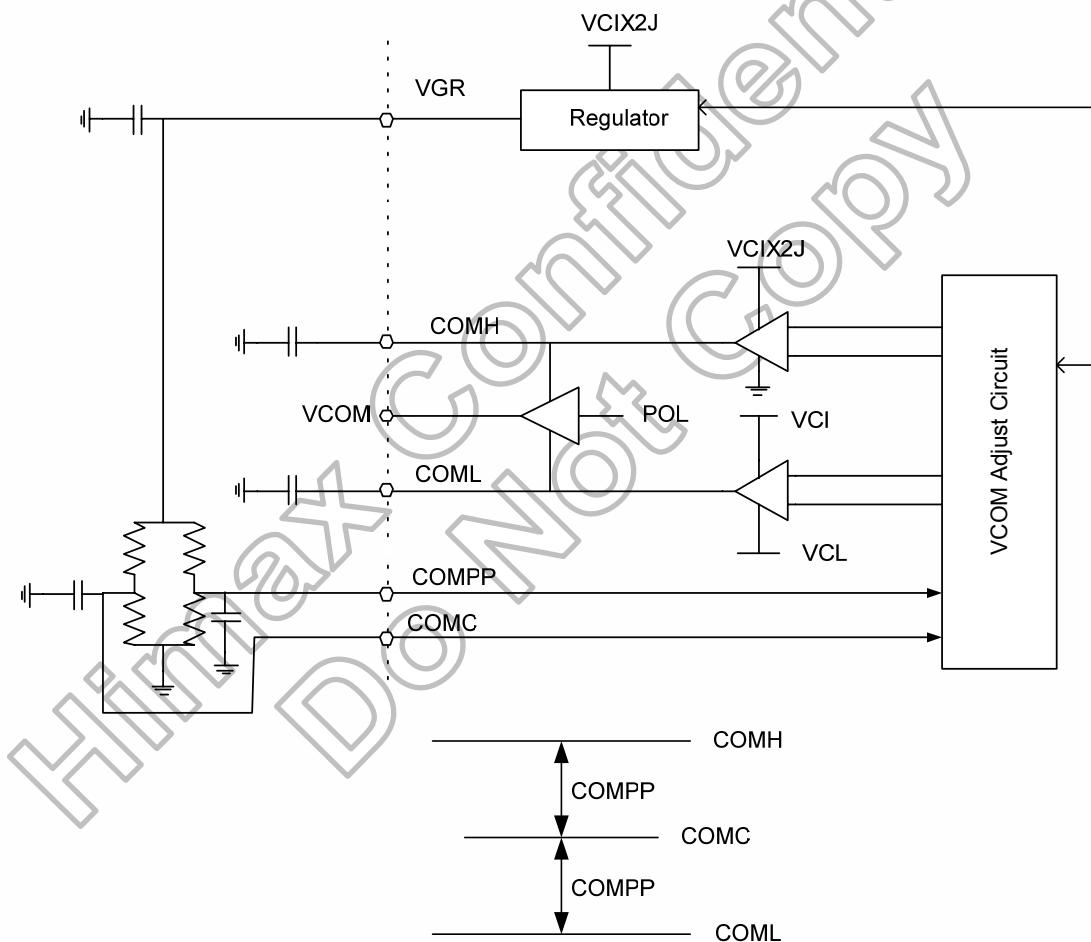


Figure 7.3 VCOM Block

7.3 Gate driver

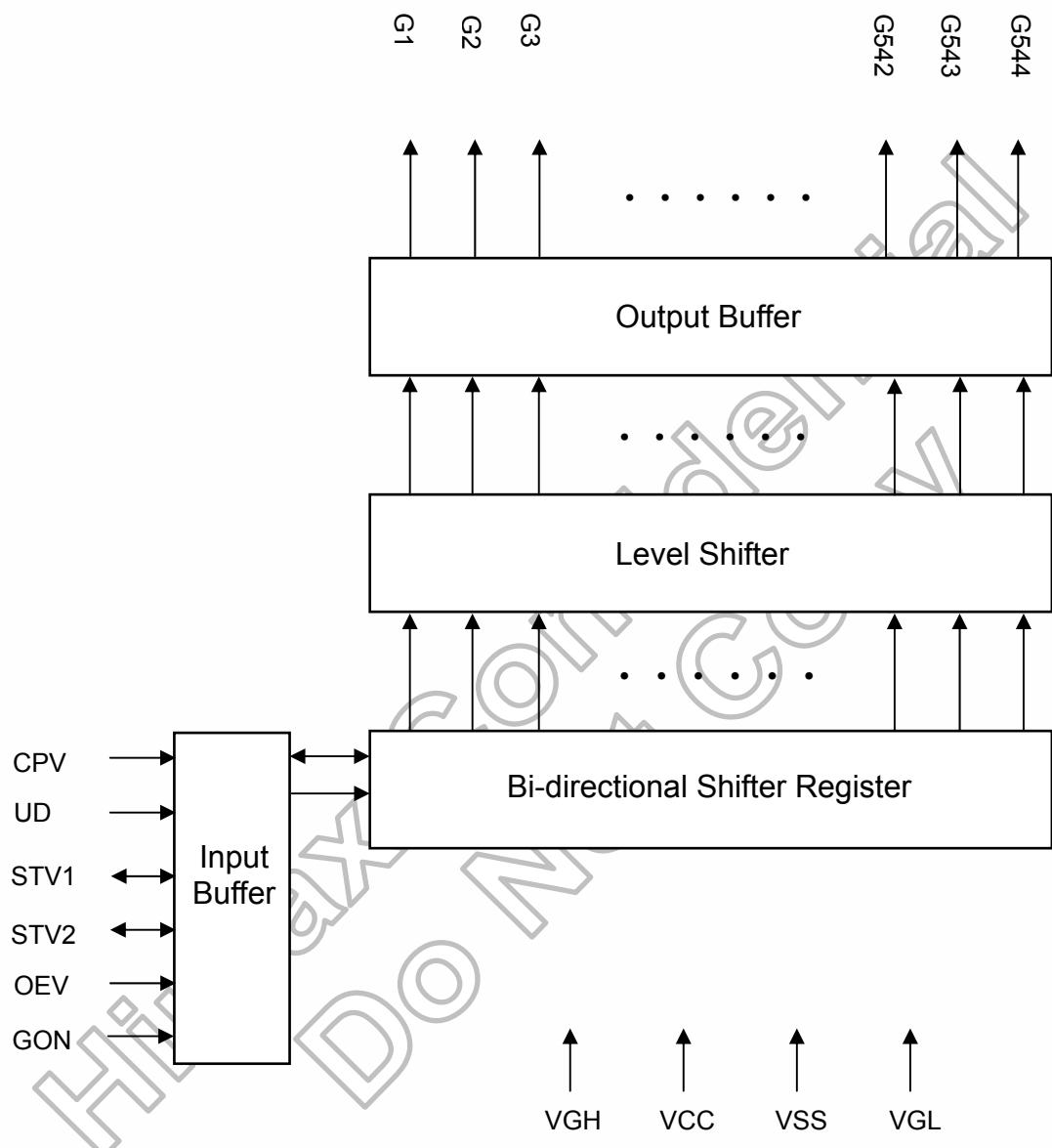
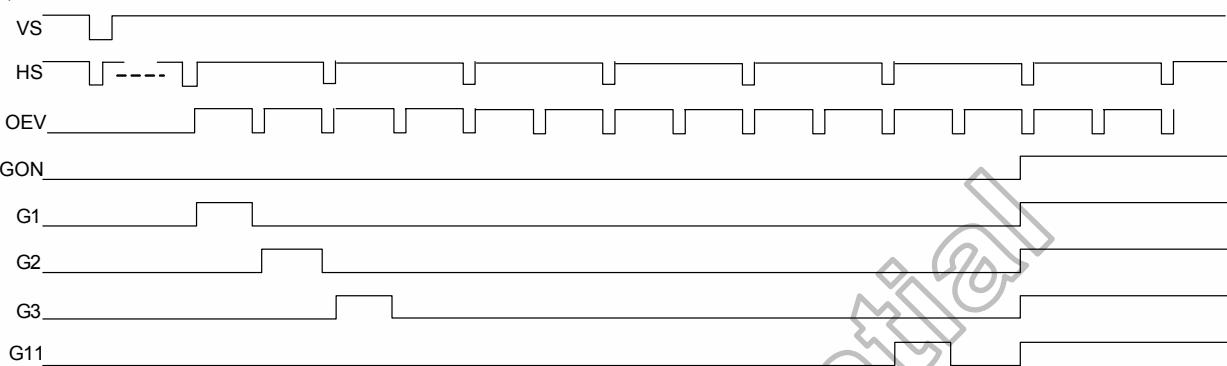
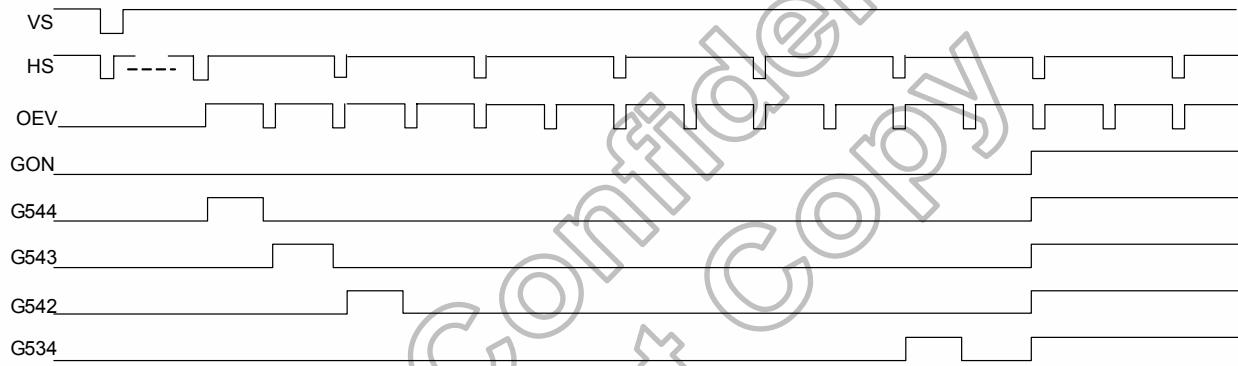


Figure 7.4 Gate Driver

UD=1, normal scan



UD=0, reverse scan

**Figure 7.5 Gate Sequence**

7.4 Source driver

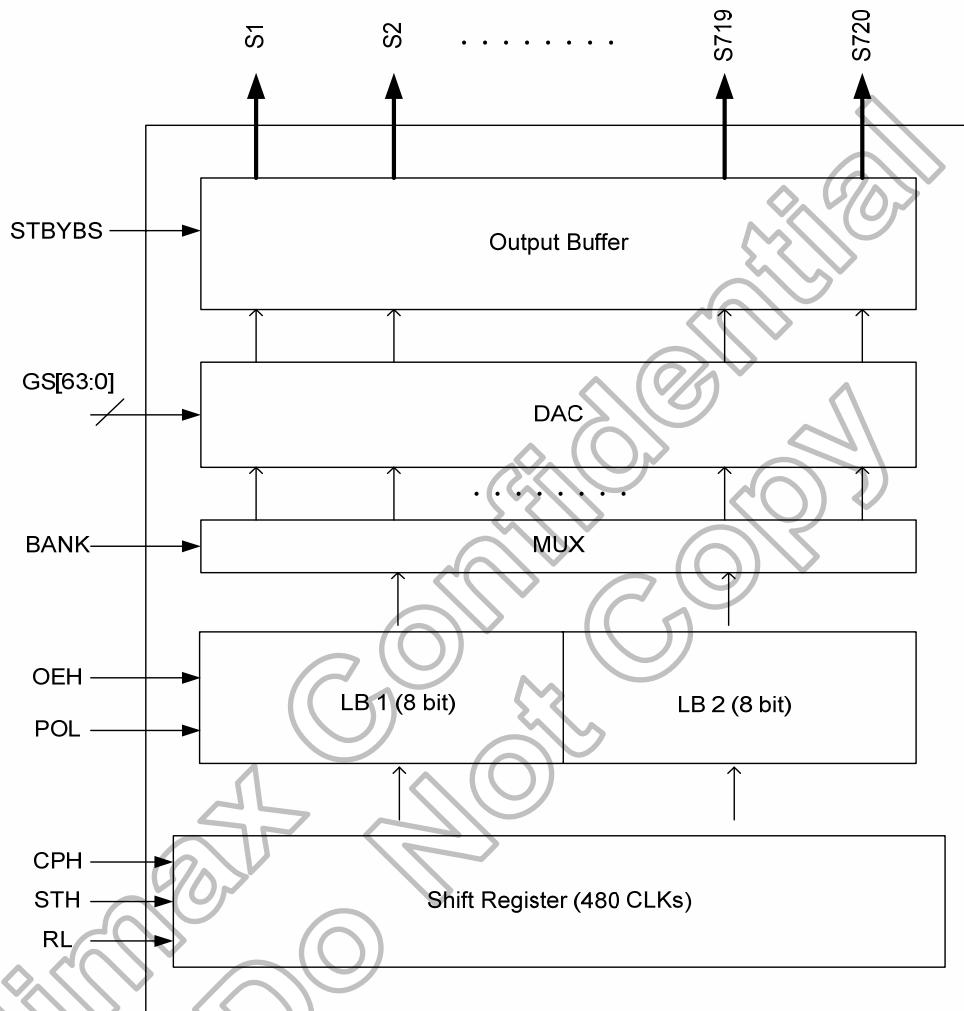


Figure 7.6 Source Block

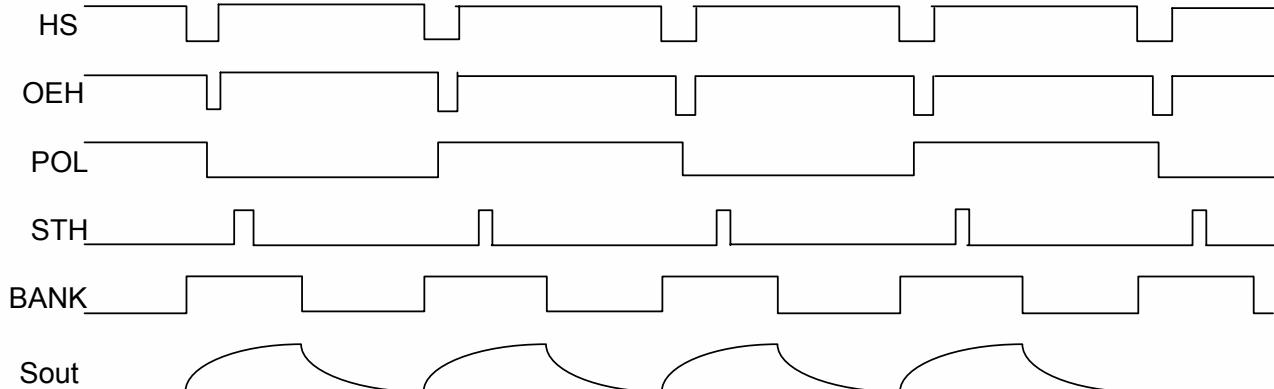


Figure 7.7 Source Sequence

7.5 Gamma adjustment

The HX8257-A incorporates gamma adjustment function for the 256-color display. Gamma adjustment is implemented by deciding the 6-grayscale levels with gradient adjustment and micro adjustment register. Also, gradient adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

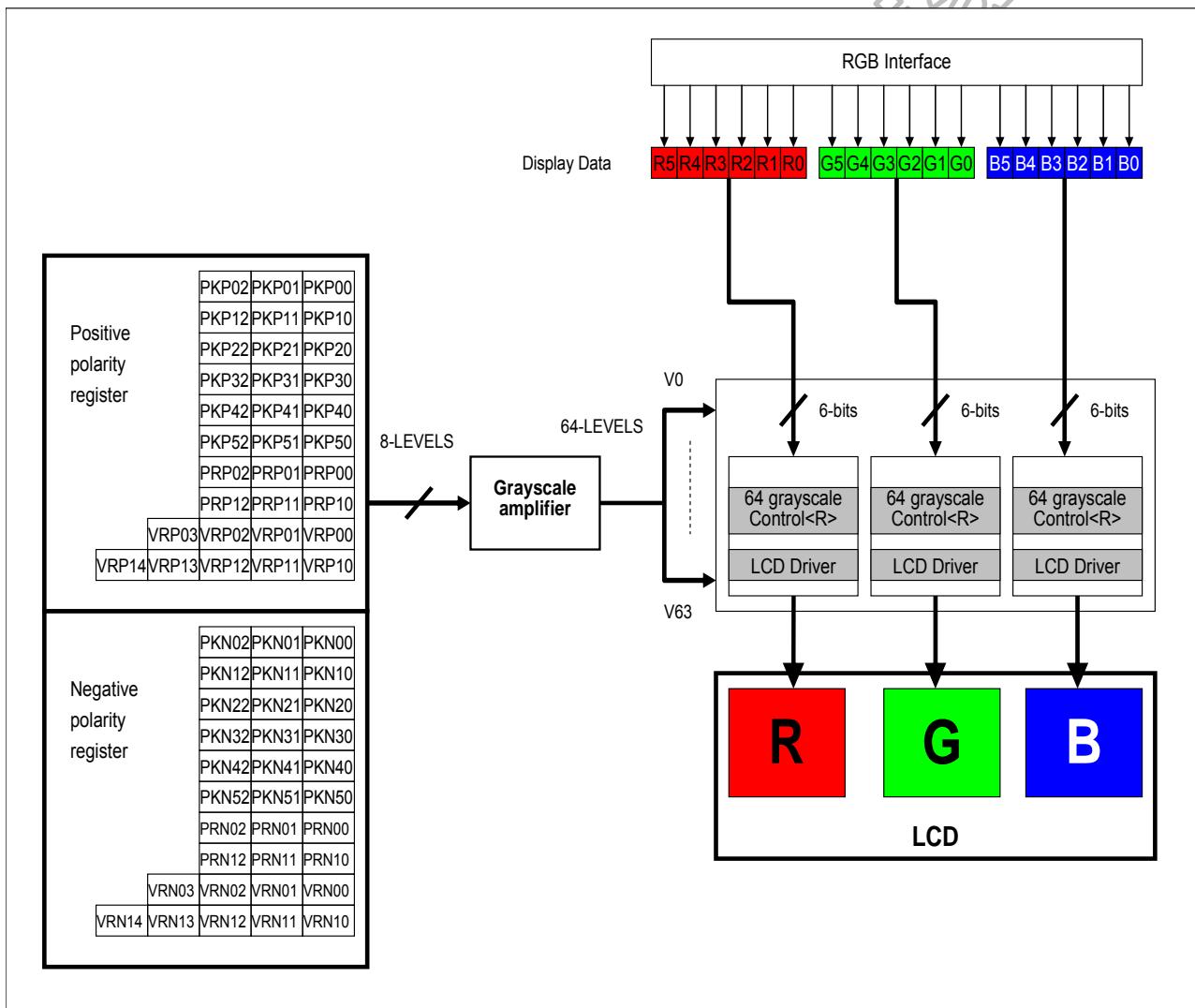


Figure 7.8 Grayscale Control Block

7.5.1 Structure of grayscale amplifier

Below figure indicates the structure of the grayscale amplifier (Positive Gray Scale). Different voltages are decided by the gradient adjustment register and the micro adjustment register, which are used for the Grayscale Amplifier. Then HX8257-A will generate 64 voltages (GS0 to GS63) by ladder resistors.

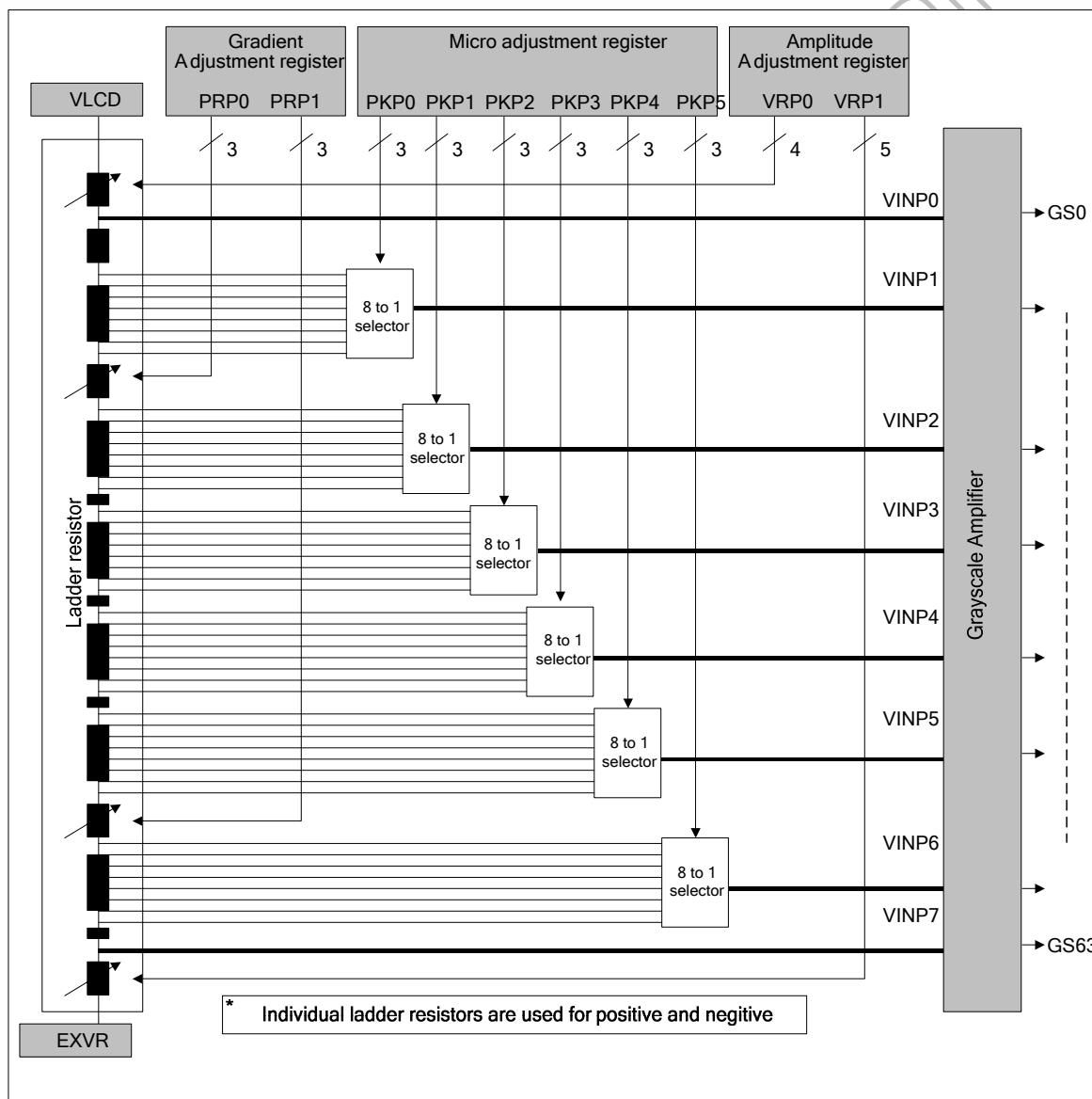


Figure 7.9 Grayscale Amplifier

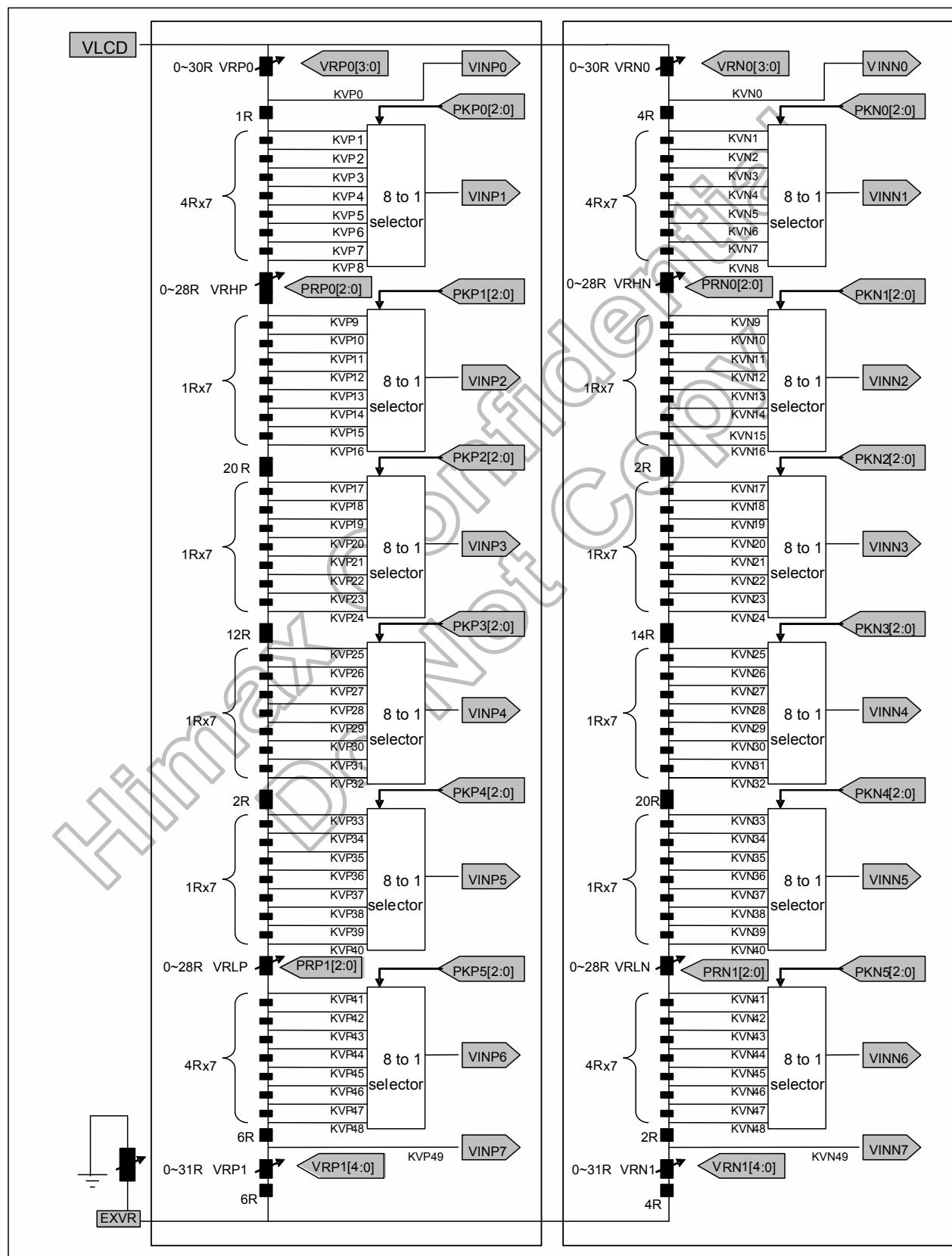


Figure 7.10 Resistor Ladder for Gamma Voltages Generation

Himax奇景光電

2008.12.25

DCC文件管制中心

P 35

7.5.2 Gamma adjustment register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Use the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.

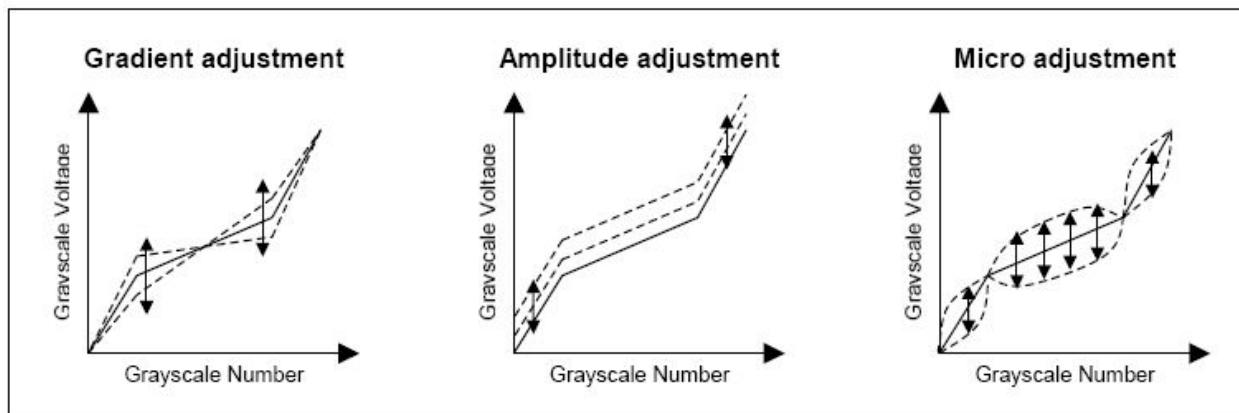


Figure 7.11 Gamma Adjustment Function

7.5.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

7.5.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

7.5.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.



7.5.3 Ladder resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there has pin (EXVR) that can be connected to VSS or an external variable resistor for compensating the dispersion of length according to different panels.

Variable resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

PRP(N)

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
⋮	⋮
Step = 2R	⋮
1110	28R
1111	30R

VRP(N)0

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
⋮	⋮
Step = 1R	⋮
11110	30R
11111	31R

VRP(N)1

Table 7.1 Variable Resistor

8 to 1 selector

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro adjusting register and the selecting voltage.

Register PKP[2:0]	Positive polarity						Negative polarity						
	Selected voltage						Register PKN[2:0]	Selected voltage					
	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6		VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Table 7.2 PKP and PKN

Reference	Formula	Micro-adjusting register	Reference voltage
KVP0	VLCD63 - $\Delta V \times VRP0 / SUMRP$	-	VINP0
KVP1	VLCD63 - $\Delta V \times (VRP0 + 1R) / SUMRP$	PKP0[2:0] = "000"	VINP1
KVP2	VLCD63 - $\Delta V \times (VRP0 + 5R) / SUMRP$	PKP0[2:0] = "001"	
KVP3	VLCD63 - $\Delta V \times (VRP0 + 9R) / SUMRP$	PKP0[2:0] = "010"	
KVP4	VLCD63 - $\Delta V \times (VRP0 + 13R) / SUMRP$	PKP0[2:0] = "011"	
KVP5	VLCD63 - $\Delta V \times (VRP0 + 17R) / SUMRP$	PKP0[2:0] = "100"	
KVP6	VLCD63 - $\Delta V \times (VRP0 + 21R) / SUMRP$	PKP0[2:0] = "101"	
KVP7	VLCD63 - $\Delta V \times (VRP0 + 25R) / SUMRP$	PKP0[2:0] = "110"	
KVP8	VLCD63 - $\Delta V \times (VRP0 + 29R) / SUMRP$	PKP0[2:0] = "111"	
KVP9	VLCD63 - $\Delta V \times (VRP0 + 29R + VRHP) / SUMRP$	PKP1[2:0] = "000"	
KVP10	VLCD63 - $\Delta V \times (VRP0 + 30R + VRHP) / SUMRP$	PKP1[2:0] = "001"	
KVP11	VLCD63 - $\Delta V \times (VRP0 + 31R + VRHP) / SUMRP$	PKP1[2:0] = "010"	
KVP12	VLCD63 - $\Delta V \times (VRP0 + 32R + VRHP) / SUMRP$	PKP1[2:0] = "011"	
KVP13	VLCD63 - $\Delta V \times (VRP0 + 33R + VRHP) / SUMRP$	PKP1[2:0] = "100"	
KVP14	VLCD63 - $\Delta V \times (VRP0 + 34R + VRHP) / SUMRP$	PKP1[2:0] = "101"	
KVP15	VLCD63 - $\Delta V \times (VRP0 + 35R + VRHP) / SUMRP$	PKP1[2:0] = "110"	
KVP16	VLCD63 - $\Delta V \times (VRP0 + 36R + VRHP) / SUMRP$	PKP1[2:0] = "111"	
KVP17	VLCD63 - $\Delta V \times (VRP0 + 56R + VRHP) / SUMRP$	PKP2[2:0] = "000"	
KVP18	VLCD63 - $\Delta V \times (VRP0 + 57R + VRHP) / SUMRP$	PKP2[2:0] = "001"	
KVP19	VLCD63 - $\Delta V \times (VRP0 + 58R + VRHP) / SUMRP$	PKP2[2:0] = "010"	
KVP20	VLCD63 - $\Delta V \times (VRP0 + 59R + VRHP) / SUMRP$	PKP2[2:0] = "011"	
KVP21	VLCD63 - $\Delta V \times (VRP0 + 60R + VRHP) / SUMRP$	PKP2[2:0] = "100"	
KVP22	VLCD63 - $\Delta V \times (VRP0 + 61R + VRHP) / SUMRP$	PKP2[2:0] = "101"	
KVP23	VLCD63 - $\Delta V \times (VRP0 + 62R + VRHP) / SUMRP$	PKP2[2:0] = "110"	
KVP24	VLCD63 - $\Delta V \times (VRP0 + 63R + VRHP) / SUMRP$	PKP2[2:0] = "111"	
KVP25	VLCD63 - $\Delta V \times (VRP0 + 75R + VRHP) / SUMRP$	PKP3[2:0] = "000"	
KVP26	VLCD63 - $\Delta V \times (VRP0 + 76R + VRHP) / SUMRP$	PKP3[2:0] = "001"	
KVP27	VLCD63 - $\Delta V \times (VRP0 + 77R + VRHP) / SUMRP$	PKP3[2:0] = "010"	
KVP28	VLCD63 - $\Delta V \times (VRP0 + 78R + VRHP) / SUMRP$	PKP3[2:0] = "011"	
KVP29	VLCD63 - $\Delta V \times (VRP0 + 79R + VRHP) / SUMRP$	PKP3[2:0] = "100"	
KVP30	VLCD63 - $\Delta V \times (VRP0 + 80R + VRHP) / SUMRP$	PKP3[2:0] = "101"	
KVP31	VLCD63 - $\Delta V \times (VRP0 + 81R + VRHP) / SUMRP$	PKP3[2:0] = "110"	
KVP32	VLCD63 - $\Delta V \times (VRP0 + 82R + VRHP) / SUMRP$	PKP3[2:0] = "111"	
KVP33	VLCD63 - $\Delta V \times (VRP0 + 84R + VRHP) / SUMRP$	PKP4[2:0] = "000"	
KVP34	VLCD63 - $\Delta V \times (VRP0 + 85R + VRHP) / SUMRP$	PKP4[2:0] = "001"	
KVP35	VLCD63 - $\Delta V \times (VRP0 + 86R + VRHP) / SUMRP$	PKP4[2:0] = "010"	
KVP36	VLCD63 - $\Delta V \times (VRP0 + 87R + VRHP) / SUMRP$	PKP4[2:0] = "011"	
KVP37	VLCD63 - $\Delta V \times (VRP0 + 88R + VRHP) / SUMRP$	PKP4[2:0] = "100"	
KVP38	VLCD63 - $\Delta V \times (VRP0 + 89R + VRHP) / SUMRP$	PKP4[2:0] = "101"	
KVP39	VLCD63 - $\Delta V \times (VRP0 + 90R + VRHP) / SUMRP$	PKP4[2:0] = "110"	
KVP40	VLCD63 - $\Delta V \times (VRP0 + 91R + VRHP) / SUMRP$	PKP4[2:0] = "111"	
KVP41	VLCD63 - $\Delta V \times (VRP0 + 91R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "000"	
KVP42	VLCD63 - $\Delta V \times (VRP0 + 95R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "001"	
KVP43	VLCD63 - $\Delta V \times (VRP0 + 99R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "010"	
KVP44	VLCD63 - $\Delta V \times (VRP0 + 103R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "011"	
KVP45	VLCD63 - $\Delta V \times (VRP0 + 107R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "100"	
KVP46	VLCD63 - $\Delta V \times (VRP0 + 111R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "101"	
KVP47	VLCD63 - $\Delta V \times (VRP0 + 115R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "110"	
KVP48	VLCD63 - $\Delta V \times (VRP0 + 119R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "111"	
KVP49	VLCD63 - $\Delta V \times (VRP0 + 125R + VRHP + VRLP) / SUMRP$	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = $131R + VRHP + VRLP + VRP0 + VRP1$ ΔV : Voltage difference between VLCD and EXVR.

Table 7.4 Reference Voltages of Positive Polarity

Reference	Formula	Micro-adjusting register	Reference voltage
KVN0	VLCD63 - $\Delta V \times VRN0 / SUMRN$	-	VINN0
KVN1	VLCD63 - $\Delta V \times (VRN0 + 4R) / SUMRN$	PKN0[2:0] = "000"	VINN1
KVN2	VLCD63 - $\Delta V \times (VRN0 + 8R) / SUMRN$	PKN0[2:0] = "001"	
KVN3	VLCD63 - $\Delta V \times (VRN0 + 12R) / SUMRN$	PKN0[2:0] = "010"	
KVN4	VLCD63 - $\Delta V \times (VRN0 + 16R) / SUMRN$	PKN0[2:0] = "011"	
KVN5	VLCD63 - $\Delta V \times (VRN0 + 20R) / SUMRN$	PKN0[2:0] = "100"	
KVN6	VLCD63 - $\Delta V \times (VRN0 + 24R) / SUMRN$	PKN0[2:0] = "101"	
KVN7	VLCD63 - $\Delta V \times (VRN0 + 28R) / SUMRN$	PKN0[2:0] = "110"	
KVN8	VLCD63 - $\Delta V \times (VRN0 + 32R) / SUMRN$	PKN0[2:0] = "111"	
KVN9	VLCD63 - $\Delta V \times (VRN0 + 32R + VRHN) / SUMRN$	PKN1[2:0] = "000"	VINN2
KVN10	VLCD63 - $\Delta V \times (VRN0 + 33R + VRHN) / SUMRN$	PKN1[2:0] = "001"	
KVN11	VLCD63 - $\Delta V \times (VRN0 + 34R + VRHN) / SUMRN$	PKN1[2:0] = "010"	
KVN12	VLCD63 - $\Delta V \times (VRN0 + 35R + VRHN) / SUMRN$	PKN1[2:0] = "011"	
KVN13	VLCD63 - $\Delta V \times (VRN0 + 36R + VRHN) / SUMRN$	PKN1[2:0] = "100"	
KVN14	VLCD63 - $\Delta V \times (VRN0 + 37R + VRHN) / SUMRN$	PKN1[2:0] = "101"	
KVN15	VLCD63 - $\Delta V \times (VRN0 + 38R + VRHN) / SUMRN$	PKN1[2:0] = "110"	
KVN16	VLCD63 - $\Delta V \times (VRN0 + 39R + VRHN) / SUMRN$	PKN1[2:0] = "111"	
KVN17	VLCD63 - $\Delta V \times (VRN0 + 41R + VRHN) / SUMRN$	PKN2[2:0] = "000"	VINN3
KVN18	VLCD63 - $\Delta V \times (VRN0 + 42R + VRHN) / SUMRN$	PKN2[2:0] = "001"	
KVN19	VLCD63 - $\Delta V \times (VRN0 + 43R + VRHN) / SUMRN$	PKN2[2:0] = "010"	
KVN20	VLCD63 - $\Delta V \times (VRN0 + 44R + VRHN) / SUMRN$	PKN2[2:0] = "011"	
KVN21	VLCD63 - $\Delta V \times (VRN0 + 45R + VRHN) / SUMRN$	PKN2[2:0] = "100"	
KVN22	VLCD63 - $\Delta V \times (VRN0 + 46R + VRHN) / SUMRN$	PKN2[2:0] = "101"	
KVN23	VLCD63 - $\Delta V \times (VRN0 + 47R + VRHN) / SUMRN$	PKN2[2:0] = "110"	
KVN24	VLCD63 - $\Delta V \times (VRN0 + 48R + VRHN) / SUMRN$	PKN2[2:0] = "111"	
KVN25	VLCD63 - $\Delta V \times (VRN0 + 62R + VRHN) / SUMRN$	PKN3[2:0] = "000"	VINN4
KVN26	VLCD63 - $\Delta V \times (VRN0 + 63R + VRHN) / SUMRN$	PKN3[2:0] = "001"	
KVN27	VLCD63 - $\Delta V \times (VRN0 + 64R + VRHN) / SUMRN$	PKN3[2:0] = "010"	
KVN28	VLCD63 - $\Delta V \times (VRN0 + 65R + VRHN) / SUMRN$	PKN3[2:0] = "011"	
KVN29	VLCD63 - $\Delta V \times (VRN0 + 66R + VRHN) / SUMRN$	PKN3[2:0] = "100"	
KVN30	VLCD63 - $\Delta V \times (VRN0 + 67R + VRHN) / SUMRN$	PKN3[2:0] = "101"	
KVN31	VLCD63 - $\Delta V \times (VRN0 + 68R + VRHN) / SUMRN$	PKN3[2:0] = "110"	
KVN32	VLCD63 - $\Delta V \times (VRN0 + 69R + VRHN) / SUMRN$	PKN3[2:0] = "111"	
KVN33	VLCD63 - $\Delta V \times (VRN0 + 89R + VRHN) / SUMRN$	PKN4[2:0] = "000"	VINN5
KVN34	VLCD63 - $\Delta V \times (VRN0 + 90R + VRHN) / SUMRN$	PKN4[2:0] = "001"	
KVN35	VLCD63 - $\Delta V \times (VRN0 + 91R + VRHN) / SUMRN$	PKN4[2:0] = "010"	
KVN36	VLCD63 - $\Delta V \times (VRN0 + 92R + VRHN) / SUMRN$	PKN4[2:0] = "011"	
KVN37	VLCD63 - $\Delta V \times (VRN0 + 93R + VRHN) / SUMRN$	PKN4[2:0] = "100"	
KVN38	VLCD63 - $\Delta V \times (VRN0 + 94R + VRHN) / SUMRN$	PKN4[2:0] = "101"	
KVN39	VLCD63 - $\Delta V \times (VRN0 + 95R + VRHN) / SUMRN$	PKN4[2:0] = "110"	
KVN40	VLCD63 - $\Delta V \times (VRN0 + 96R + VRHN) / SUMRN$	PKN4[2:0] = "111"	
KVN41	VLCD63 - $\Delta V \times (VRN0 + 96R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "000"	VINN6
KVN42	VLCD63 - $\Delta V \times (VRN0 + 100R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "001"	
KVN43	VLCD63 - $\Delta V \times (VRN0 + 104R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "010"	
KVN44	VLCD63 - $\Delta V \times (VRN0 + 108R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "011"	
KVN45	VLCD63 - $\Delta V \times (VRN0 + 112R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "100"	
KVN46	VLCD63 - $\Delta V \times (VRN0 + 116R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "101"	
KVN47	VLCD63 - $\Delta V \times (VRN0 + 120R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "110"	
KVN48	VLCD63 - $\Delta V \times (VRN0 + 124R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "111"	
KVN49	VLCD63 - $\Delta V \times (VRN0 + 126R + VRHN + VRLN) / SUMRN$	-	VINN7

SUMRN: Total of the negative polarity ladder resistance = $130R + VRHN + VRLN + VRN0 + VRN1$
 ΔV : Voltage difference between VLCD and EXVR.

Table 7.5 Reference Voltages of Negative Polarity

7.6 PWM

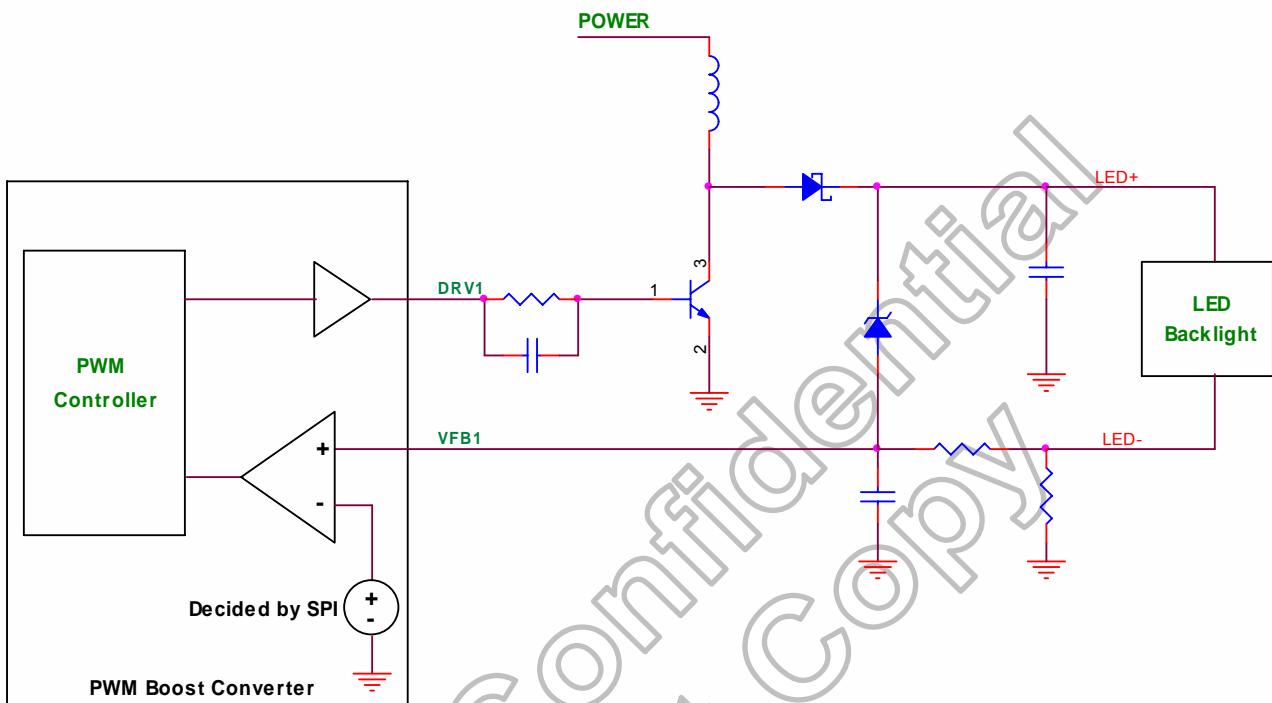


Figure 7.12 PWM Block

The HX8257-A is built in 2 independent PWM control circuits. The internal reference voltage is adjustable by FBA[2:0] and FBB[2:0] in R05h. By adjusting the voltage, you can get different VO to meet your system application. For 1st PWM, the VO also can be adjusted by DU[4:0] setting. (Input pins or register setting) This setting is combined with CABC function to provide power for LED backlight. 2nd PWM is designed to generate VCIX2J if charge pump circuit is not used.

7.7 TCON

The HX8257-A has 2 modes for input interface, parallel and serial interface. In parallel interface (PS="H"), 24-bit data are transferred into the HX8257-A each cycle when DE is activated. D07 to D00 is displayed for R dot on panel, D17 to D10 are displayed for G data, and D27 to D20 are displayed for B data. The relationship between display data and source output is shown in the following figure.

Input data format		24-bit RGB, 3 dots (sub-pixels) per clock					
Input data width		24 bits with Dx7 is MSB and Dx0 is LSB, x = 1 ~ 3					

LR	First			→	Last		
	D00~ D07	D10~ D17	D20~ D27	...	D00~ D07	D10~ D17	D20~ D27
H	R1	G1	B1	...	R480	G480	B480

LR	Last			←	First		
	D00~ D07	D10~ D17	D20~ D27	...	D00~ D07	D10~ D17	D20~ D27
L	R1	G1	B1	...	R480	G480	B480

In serial interface (PS="L"), 8-bit data are transferred into the HX8257-A through D07~D00 pins. The data are latched sequentially for display R_n, G_n, B_n, n=1, 2 ... 480 when LR="H", and for B_n, G_n, R_n, n=480, 479, 478 ... to 1 when LR="L".

Input data format		8-bit RGB, 1 dot (sub-pixel) per clock					
Input data width		8 bits with D07 is MSB and D00 is LSB					

LR	First		→	Last		
	D00~ D07	D00~ D07	D00~ D07	...	D00~ D07	D00~ D07
H	R1	G1	B1	...	R480	G480

LR	Last		←	First		
	D00~ D07	D00~ D07	D00~ D07	...	D00~ D07	D00~ D07
L	R1	G1	B1	...	R480	G480

7.7.1 LR/UD function

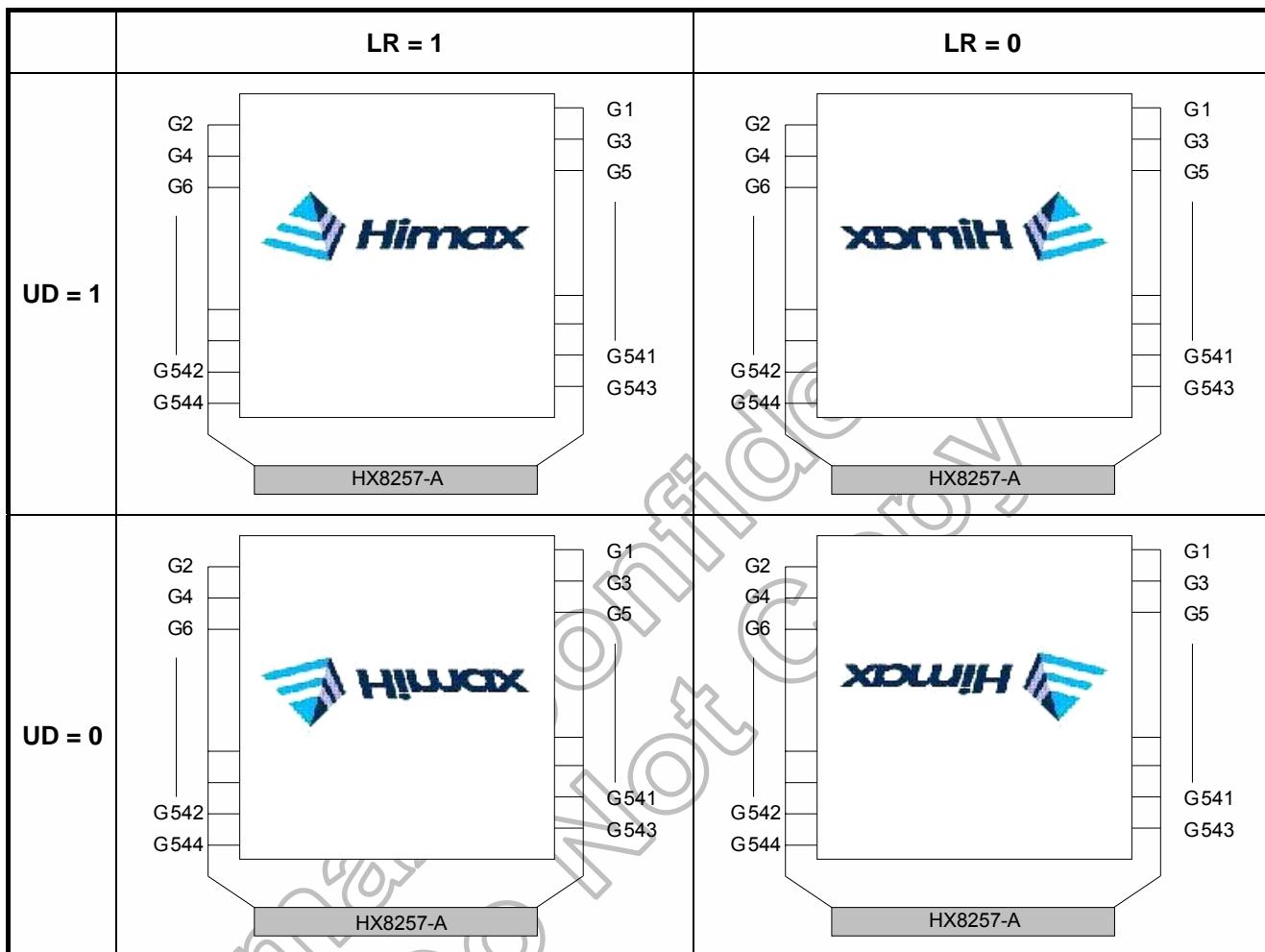


Figure 7.13 LR/UD Function

7.7.2 Aging mode

If only CLK is sent into driver IC without VS, HS, and DE signals, the HX8257-A will enter Aging Mode after power on. In Aging mode, the display picture can change automatically or be controlled manually by access register R04h.

7.7.3 TCON power on/off control

The HX8257-A has a power ON/OFF sequence control function. When DISP pin is pulled "H", blank data is outputted for 10-frames first, from the falling edge of the following VSYNC signal. Similarly, when DISP is pulled "L", 10-frames of blank data will be outputted from the falling edge of the following VSYNC, too. The blank data would be gray level 0 for normally black LC (NBW="H"), and be gray level 255 for normally white LC (NBW="L").

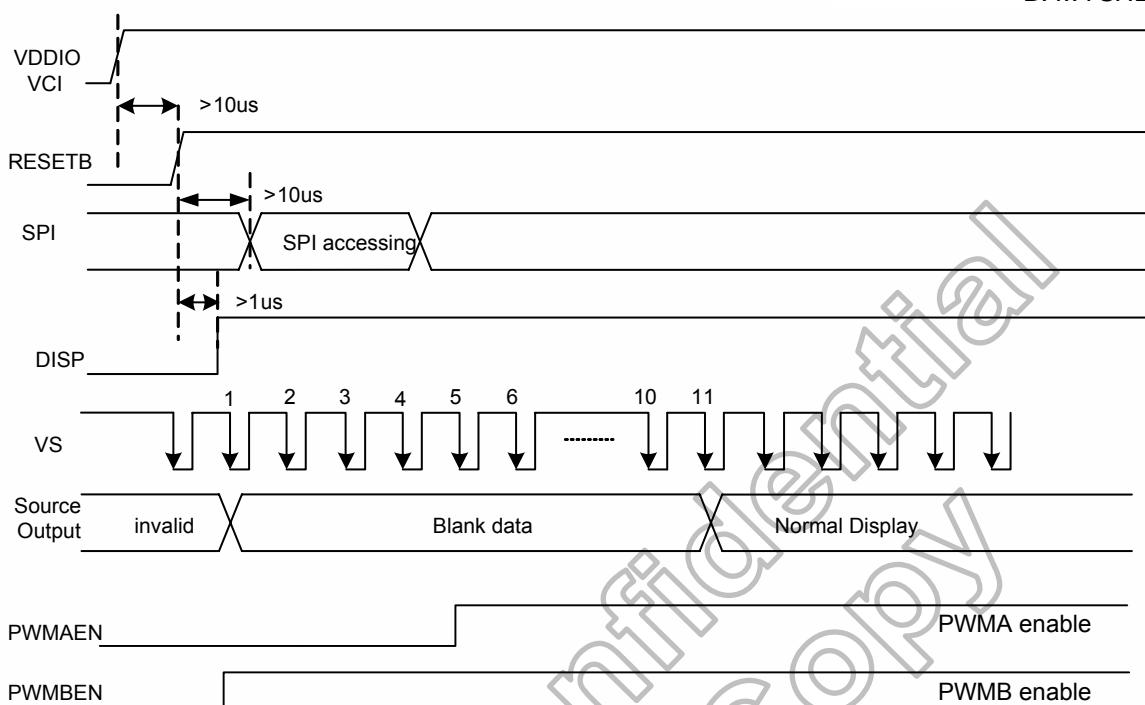


Figure 7.14 Power On Sequence

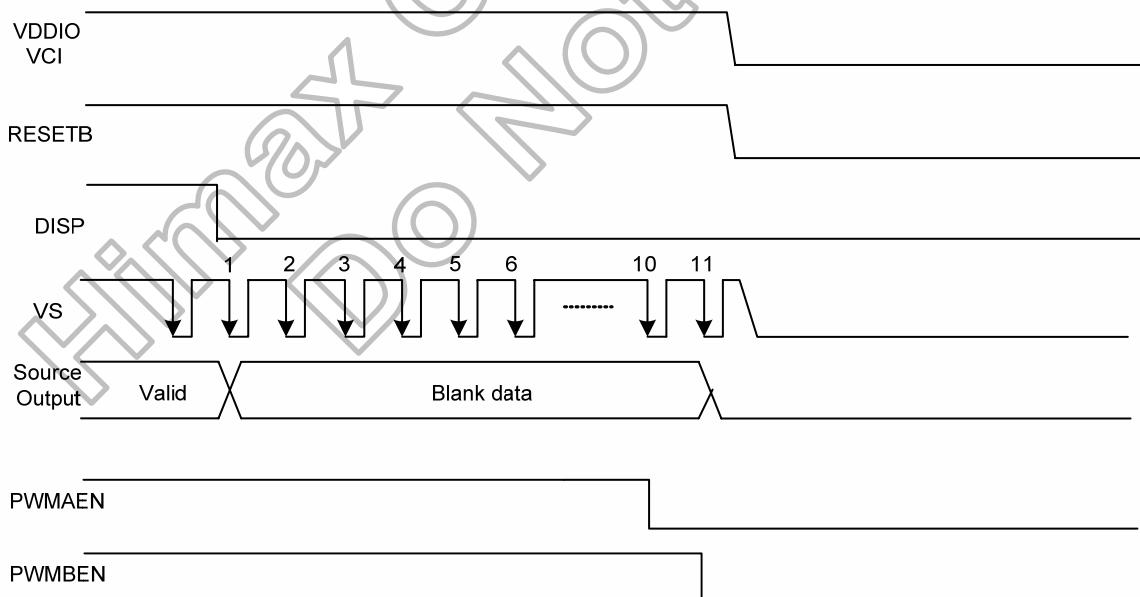


Figure 7.15 Power Off Sequence

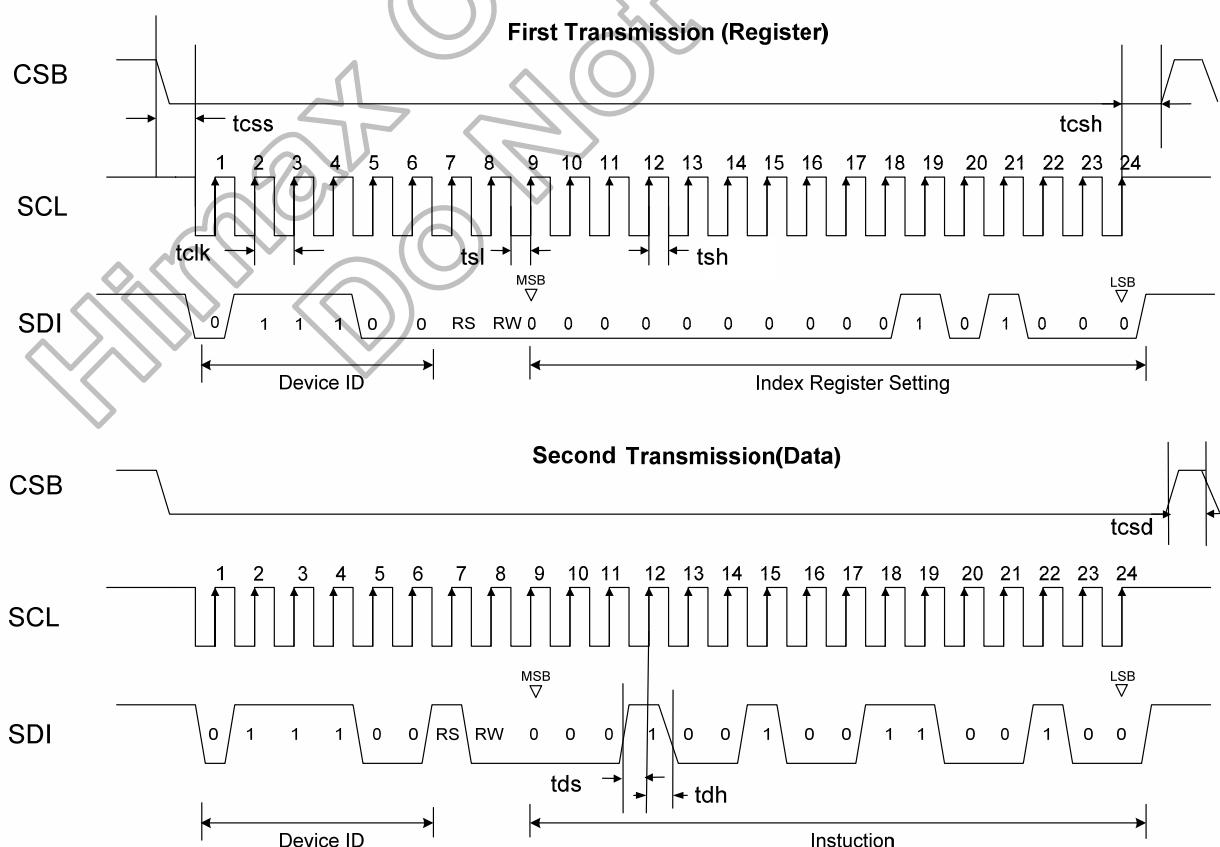
8. SPI Register

The HX8257-A is internally initialized by the global reset signal, RESETB. The reset input must be held for at least 1ms after power is stable.

HX8257-A supports 24-bit serial bus interface. 24-bit data are latched by SCL's rising edge step-by-step. Serial bus interface is active while CSB=L (from CSB's falling to CSB's rising). After CSB has transmitted twenty-four units of CLK, it has to change into High.

Under the standard condition, the number of SCL is twenty-four units. While CSB=L, if SCL < 24 cycles is input, then the input data won't be latched and will become invalid data. While CSB=L, if SCL >24 cycles is input, the 24-bit data in front of CSB's rising edge will become valid.

- Write SPI



Note: The example writes “0x1264h” to register R28h.

Figure 8.1 Write SPI Timing

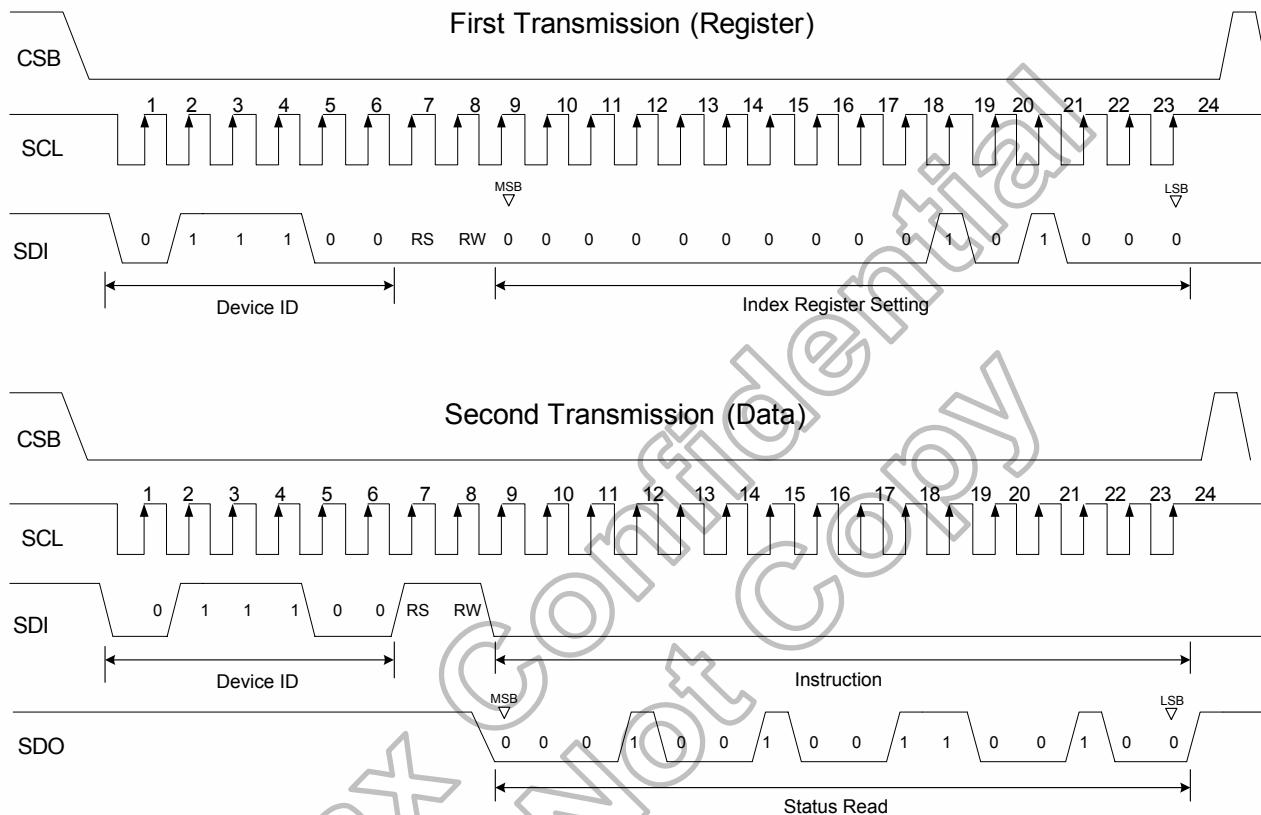


2008.12.25



P45

- Read SPI



Note: The example reads "0x1264h" from register R28h.

Figure 8.2 Read SPI Timing

RS	RW	Status
0	0	Write SPI Address
0	1	NA
1	0	Write SPI Data
1	1	Read SPI Data

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Chip Select Setup Time	tcss	0	-	-	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns



CLK_TRG: Clock edge selection signal for the data sampling.

CLK_TRG=1: Data sampling at the CLK falling edge.

CLK_TRG=0: Data sampling at the CLK rising edge.

VSP: When VSP=0, VSYNC is negative polarity. When VSP=1, VSYNC is positive polarity.

HSP: When HSP=0, HSYNC is negative polarity. When HSP=1, HSYNC is positive polarity.

DEP: When DEP=0, DEN is negative polarity active. When DEP=1, DEN is positive polarity active.

DEO: When DEO=0, VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP[6:0] and the horizontal first valid data is defined by DE signal. When DEO=1, only DEN signal is needed in DE mode.

PALM: Set the input data line number in PAL mode. **Only effective in 480RGBx240 resolution.** Our driver IC will auto detect NTSC/PAL mode under 480RGBx240 resolution)

0: 280 lines

1: 288 lines

OEA1-0: Odd/Even field advanced function. **Only effective in SYNC mode.**

OEA1	OEA0	Description
0	0	Start pulse start @ VBP delay for Odd field and @ VBP-1 for Even field.
0	1	Start pulse start @ VBP delay for Odd field and @ VBP for Even field.
1	0	Start pulse start @ VBP delay for Odd field and @ VBP+1 for Even field.
1	1	No use

Power Control 1 (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VDS1	VDS0	0	EQ2	EQ1	EQ0	DC3	DC2	DC1	DC0	0	AP2	AP1	AP0
Default		0	0	0	1	0	1	1	0	0	1	1	0	0	0	1	0

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode, set AP2-0 = "000" to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

Himax奇景光電

2008.12.25

DCC文件管制中心

P48

DC3-0: Set the step-up cycle of the step-up circuit. When the cycle is accelerated, the VCL and VCIX2 driving ability of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Note: Fline = horizontal frequency (Fline Typ. 17 KHz)

EQ2-0: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	1 us
0	1	0	2 us
0	1	1	3 us
1	0	0	4 us
1	0	1	5 us
1	1	0	6 us
1	1	1	7 us

VDS1-0: Set the VDD regulator voltage.

VDS[1:0]=00, 1.8V

VDS[1:0]=11, 2.0V

VDS[1:0]=10, 2.2V

VDS[1:0]=01, 2.5V

Power Control 2 (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X2EN	XDK	VRC1	VRC0	VDC3	VDC2	VDC1	VDC0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
	Default	1	1	0	1	1	0	1	1	0	0	1	0	1	1	0	0

VRC1-0: Set the VCIX2 charge pump voltage clamp.

VRC[1:0]=00, 5.2V

VRC[1:0]=01, 5.4V

VRC[1:0]=10, 5.6V

VRC[1:0]=11, 5.8V

XDK: When XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2=3 x VCI) When XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2=2 x VCI)

X2EN: When X2EN=0, VCIX2 pumping circuit is disabled. When X2EN=1, VCIX2 pumping circuit is enabled.

Function Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	REV	PA2	PA1	PA0	AGM	SEQ	PS	0	REG	PSHUT	GDIS	COMG
	Default	0	0	0	0	0	0	0	0	1	0	x	0	1	x	1	1

COMG: When COMG=0, VCOM circuit is disabled. When COMG=1, VCOM circuit is enabled.

GDIS: When GDIS=0, VGL has no discharge path to VSS in standby mode. When GDIS=1, VGL will discharge to VSS in standby mode.

PSHUT: When PSHUT=0, all power circuits are shut down. When PSHUT=1, all internal power circuits are enabled.

REG: REG=1, internal VDD regulator is turn on. REG=0, VDD should be shorted to VDDIO on system.

PS: PS=1, parallel RGB input interface. PS=0, serial RGB input interface.

SEQ: SEQ=1, reverse data pin sequence. SEQ=0, data pin sequence is as pad define.

AGM: AGM=1, aging mode pattern is auto changed. AGM=0, aging mode pattern is controlled by PA2-0.

PA2-0: Define the display pattern in aging mode when AGM=0.

REV: REV=1, input data is inverted. REV=0, input data is send to display without inversion.

PWM Control (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	PSWE	DUS	DU4	DU3	DU2	DU1	DU0	PWMA	FBA2	FBA1	FBA0	PWMB	FBB2	FBB1	FBB0
	Default	0	0	0	1	1	1	1	1	1	1	0	0	1	1	0	0

FBB2-0: Set 2nd PWM feedback level adjustment.

- 000: 0.8V
- 001: 0.85V
- 010: 0.9V
- 011: 0.95V
- 100: 1.0V
- 101: 1.05V
- 110: 1.1V
- 111: 1.15V

PWMB: When PWMB=0, 2nd PWM function is disabled. When PWMB=1, 2nd PWM function is enabled.

FBA2-0: Set 1st PWM feedback level adjustment.

- 000: 0.8V
- 001: 0.85V
- 010: 0.9V
- 011: 0.95V
- 100: 1.0V
- 101: 1.05V
- 110: 1.1V
- 111: 1.15V

PWMA: When PWMA=0, 1st PWM function is disabled. When PWMA=1, 1st PWM function is enabled.

DU4-0: Define the supply current of 1st PWM (PWM A) for LED backlight. The register value is effective only when DUS bit=0. This setting will combine with CABC function to control the LED backlight brightness dynamically.

DU4-0	Supply current
00000	1/32
00001	2/32
00010	3/32
00011	4/32
00100	5/32
00101	6/32
00110	7/32
00111	8/32
01000	9/32
01001	10/32
01010	11/32
01011	12/32
01100	13/32
01101	14/32
01110	15/32
01111	16/32

DU4-0	Supply current
10000	17/32
10001	18/32
10010	19/32
10011	20/32
10100	21/32
10101	22/32
10110	23/32
10111	24/32
11000	25/32
11001	26/32
11010	27/32
11011	28/32
11100	29/32
11101	30/32
11110	31/32
11111	32/32

DUS: Set the DU4-0 is defined by SPI register or hardware pins. When DUS=0, SPI register is effective. When DUS=1, hardware pins are effective.

PSWE: When PSWE=0, internal switch for 2nd PWM is disabled. When PSWE=1, internal switch for 2nd PWM is enabled.

VCOM Control (R06h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	nOTP	VMC4	VMC3	VMC2	VMC1	VMC0	0	0	eOTP	VDV4	VDV3	VDV2	VDV1	VDV0
	Default	0	0	0	1	0	0	0	1	0	0	0	1	0	1	1	0

VDV4-0: Set the COMPP voltage. These bits define the VCOMPP voltage 1.5 to 2.7 times the Vref voltage.

VDV4	VDV3	VDV2	VDV1	VDV0	COMPP
0	0	0	0	0	Reference from external voltage
0	0	0	0	1	Vref x 1.50
0	0	0	1	0	Vref x 1.54
0	0	0	1	1	Vref x 1.58
0	0	1	0	0	Vref x 1.62
:		:		Step = 0.04	
:		:		:	
1	1	1	0	0	Vref x 2.58
1	1	1	0	1	Vref x 2.62
1	1	1	1	0	Vref x 2.66
1	1	1	1	1	Vref x 2.70

Note: Vref is the internal reference voltage equals to 1.25V.

eOTP: eOTP=0, COMPP voltage is set by programmed OTP value. eOTP=1, COMPP voltage is set by VD4-0 SPI register.

VMC4-0: Set the COMC voltage. These bits define the VCOM DC voltage 0.22 to 2.02 times the Vref voltage.

VMC4	VMC3	VMC2	VMC1	VMC0	COMC
0	0	0	0	0	Reference from external voltage
0	0	0	0	1	Vref x 0.22
0	0	0	1	0	Vref x 0.28
0	0	0	1	1	Vref x 0.34
0	0	1	0	0	Vref x 0.40
:		:		Step = 0.06	
:		:		:	
1	1	1	0	0	Vref x 1.84
1	1	1	0	1	Vref x 1.90
1	1	1	1	0	Vref x 1.96
1	1	1	1	1	Vref x 2.02

Note: Vref is the internal reference voltage equals to 1.25V.

nOTP: nOTP=0, COMC voltage is set by programmed OTP value. nOTP=1, COMC voltage is set by VMC4-0 SPI register.



Vertical Porch (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
Default	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	

PS: RES=1, VBP default value: 0001100, RES=0, VBP default value: 0010010

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line. The setting is only effective in SYNC mode timing.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
							Step = 1
							:
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

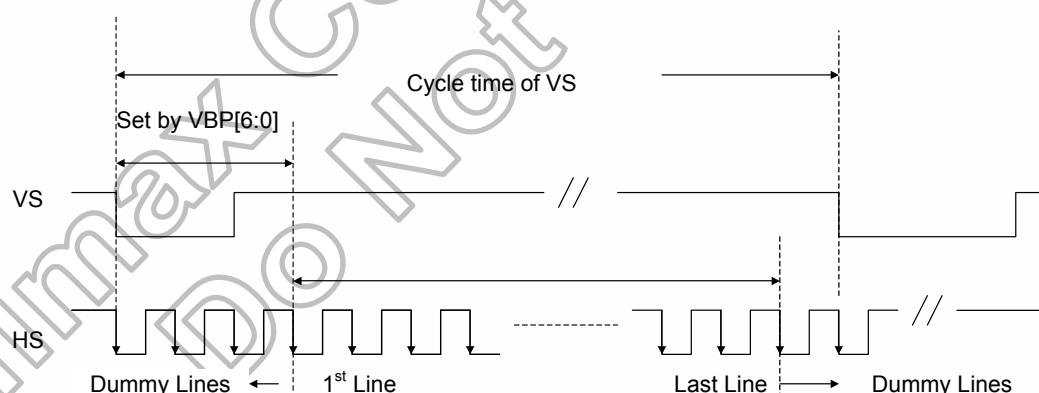


Figure 8.3 Vertical Data

Horizontal Porch (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	STH1	STH0	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
Default	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	

Note: RES=1, HBP default value: 00101011, RES=0, HBP default value: 01100110

HBP7-0: Set the delay period from falling edge of HSYNC signal to first valid data.

The data exceeds 480 pixels and before the first valid data will be treated as dummy data. The setting is only effective in SYNC mode timing.

HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle
0	0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	0	1	Can't set
0	0	0	0	0	0	1	0	Can't set
0	0	0	0	0	0	1	1	Can't set
0	0	0	0	0	1	0	0	Can't set
0	0	0	0	0	1	0	1	Can't set
0	0	0	0	0	1	1	0	Can't set
0	0	0	0	0	1	1	1	Can't set
0	0	0	0	1	0	0	0	Can't set
0	0	0	0	1	0	0	1	9
								Step = 1
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

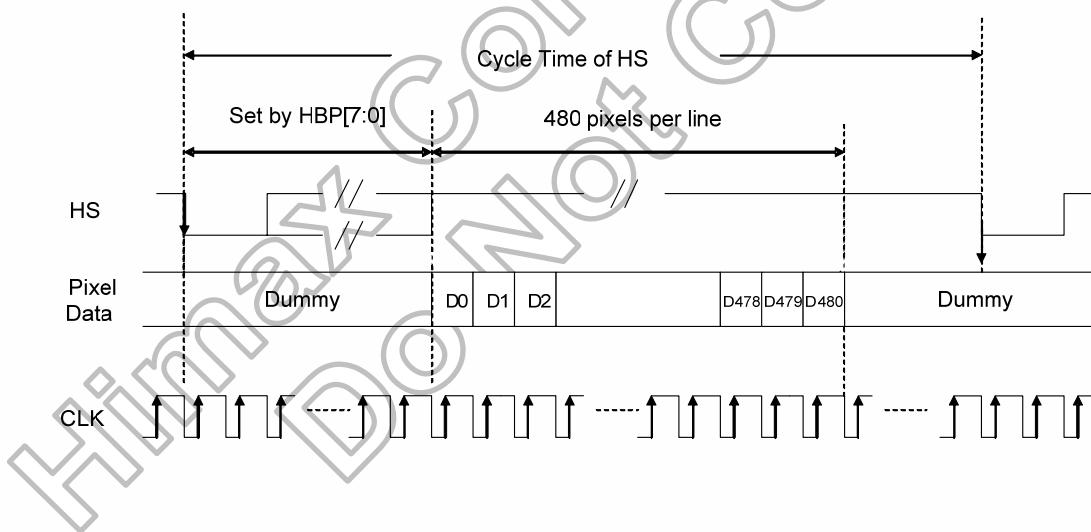


Figure 8.4 Horizontal Data

STH1-0: Adjust the first valid data by dot clock. This setting is only valid in serial RGB input interface.

STH=00: +0 dot clock

STH=01: +1 dot clock

STH=10: +2 dot clock

STH=11: +3 dot clock

Gamma control 7 (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
Default		0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1

Gamma control 8 (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
Default		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Gamma control 9 (R18h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
Default		0	0	0	0	1	1	1	1	0	0	0	0	1	0	0	1

Gamma control 10 (R19h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9. OTP Programming

OTP write sequence

Step	VMC OTP Operation
1	Power up the module. Set nOTP=1 and find out the appropriate value of VMC[4:0] and power off the system.
2	Power up the system with VDD=VDDIO=2.5V. If REG bit=1, set R02h=16'h3662.
3	Set appropriate values found from step 1 to register of VMC (R06h)
4	Set 04h=16'h0001 to stop internal power circuit. Wait 0.5s.
5	Set R60h=16'h8000
6	Set R60h=16'hC000
7	Connect 7.3V to VGH and 0V to VGL
8	Set R60h=16'hC200
9	Set R60h=16'hC280
10	Wait 200us for completing this program
11	Set R60h=16'hC200
12	Remove 7.3V from VGH and 0V from VGL
13	Set R60h=16'h8200
14	Set R60h=16'h0200
15	Set R60h=16'h0040
16	Set R60h=16'h0000

Step	VDV OTP Operation
1	Power up the module. Set eOTP=1 and find out the appropriate value of VDV[4:0] and power off the system.
2	Power up the system with VDD=VDDIO=2.5V. If REG bit=1, set R02h=16'h3662.
3	Set appropriate values found from step 1 to register of VDV (R06h)
4	Set 04h=16'h0001 to stop internal power circuit. Wait 0.5s.
5	Set R60h=16'h8000
6	Set R60h=16'hC000
7	Connect 7.3V to VGH and 0V to VGL
8	Set R60h=16'hC200
9	Set R60h=16'hC080
10	Wait 200us for completing this program
11	Set R60h=16'hC000
12	Remove 7.3V from VGH and 0V from VGL
13	Set R60h=16'h8000
14	Set R60h=16'h0000
15	Set R60h=16'h0040
16	Set R60h=16'h0000

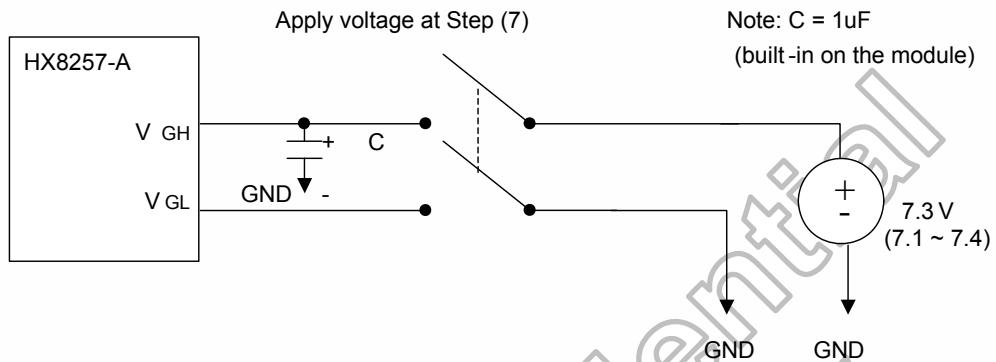
If you want to check if the OTP cell is still available for COMC/COMPP programming, you can read the current status from R61h shown below. R61h is only for read.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0	IDA	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	IDC	VMC 4	VMC 3	VMC 2	VMC 1	VMC 0

You can check the IDC/IDA bit to see if the VMC/VDV is still programmable or not. If IDC=0, you can program new VMC[4:0] value to OTP. If IDC=1, it means that the OTP cell have already programmed twice and you can't program it any more. The meaning of IDA is the same.



The
Himax奇景光電
2008.12.25

OTP programming circuit**Figure 9.1 OTP Programming Circuit**

10. DC Characteristics

Absolute Maximum Rating

(DVSS = AVSS = VCHS = VSSRC = 0V)

Symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
VDDIO	Logic Power Supply	-0.3	-	4.0	V
VCI	Booster Power Supply	-0.3	-	5.0	V
VCIP	Analog Circuit Power Supply	-0.3	-	5.0	V
VCIX2J	Power supply of analog block and VLCD/VDC regulation	-0.3	-	6.0	V
VDD	Power pin for internal logic circuit	-0.3	-	2.7	V
VGH-VGL	Using External VGH、VGL	-0.3	-	45.0	V
T _A	Operating Temperature	-30	-	85	V
T _{STG}	Storage Temperature	-55	-	125	°C

DC characteristics

(Unless otherwise specified, Voltage Referenced to DVSS, VDDIO = 2.2V, T_A = 25°C)

Symbol	Parameter	Test condition	Spec.			Unit
			Min.	Typ.	Max.	
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.8	-	3.6	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	≥VDDIO & ≥3	-	3.6	V
I _{Sleep}	Sleep mode current	-	-	50	-	μA
I _{VCI}	VCI Operating mode current	VCI=3.3V、VDDIO=3.3V at Black Pattern with 4.3" Panel	-	13	16	mA
VCL	Negative V _{CI} Output Voltage	No panel loading	-VCI	-	-VCI+0.7	V
VCIX2	VCIX2 primary booster efficiency ⁽³⁾	No panel loading, ITO for VCIX2,VCI and VCHS = 10 Ohm	5.2	5.4	5.6	V
VDC	VDC Output Voltage	VDC[3:0]=1011	4.9	5	5.1	V
VGH	Gate driver High Output Voltage	No panel loading; 3x booster	84	89.5	-	%
	Booster efficiency ⁽¹⁾	No panel loading; 4x booster	80	88.5	-	%
VGL	Gate driver Low Output Voltage	VGL= -2 x VDC VDC[3:0]=1011	-10	-10	-9	V
COMH	VCOM High Output Voltage ⁽²⁾	-	-3%	COMC+COMPP	3%	V
COML	VCOM Low Output Voltage ⁽²⁾	-	-3%	COMC-COMPP	3%	V
VLCD	VLCD Output Voltage	VRH[5:0]=110011	5.0	5.1	5.2	V
V _{OH1}	Logic High Output Voltage	I out = -100μA	0.9*VDDIO	-	VDDIO	V
V _{VD}	Source Output Voltage Deviation	-	-	±20	±30	mV
V _{OS}	Source Output Voltage Offset	-	-	-	±30	mV
V _{OL1}	Logic Low Output Voltage	I out = 100μA	0	-	0.1*VDDIO	V
V _{IH1}	Logic High Input voltage	2.5V < VDDIO < 3.6V 1.8V < VDDIO ≤ 2.5V	0.7*VDDIO 0.8*VDDIO	-	VDDIO	V
V _{IL1}	Logic Low Input voltage	2.5V < VDDIO < 3.6V 1.8V < VDDIO ≤ 2.5V	0	-	0.3*VDDIO 0.2*VDDIO	V
I _{OH}	Logic High Output Current Source	V out = VDD – 0.4V	50	-	-	μA
I _{OL}	Logic Low Output Current Drain	V out = 0.4V	-	-	-50	μA
I _{OZ}	Logic Output Tri-state Current Drain Source	-	-1	-	1	μA
I _{IL/IH}	Logic Input Current	-	-1	-	1	μA

Note : (1) VGH efficiency = VGH / (VDC x n) x 100% (where n = booster factor)

(2) COML < 0V, COMH < VCIX2J, COMH > VCI

(3) VCIX2 voltage is related with VCI voltage & VCIX2 loading. Figure 10.1 shows the estimated VCIX2 voltage under different VCIX2 current loading when ITO for VCIX2、VCI and VCHS = 10Ω.

Himax奇景光電

2008.12.25

DCC文件管制中心

P60

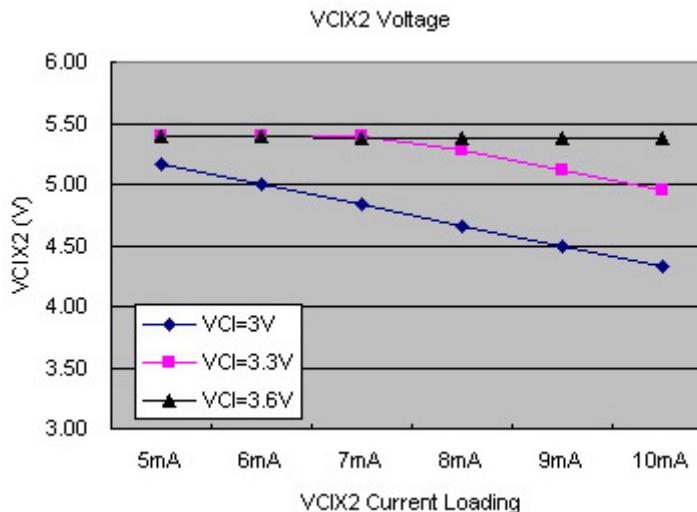


Figure 10.1 VCIX2 Voltage

Himax Confidential
DO Not Copy

11.AC Characteristics

The HX8257-A both supports DE mode and Sync mode timing. The mode was decided by DE signal internally. When DE is pulled low, the HX8257-A uses HS+VS for timing control and this timing mode is sync mode. When DE is pulled high for active data and pulled low for blanking data, the HX8257-A uses DE for timing control and this timing mode is DE mode. The detail timing chart showed below.

11.1 Timing relationship among DE、Source Output、Gate Output、VCOM

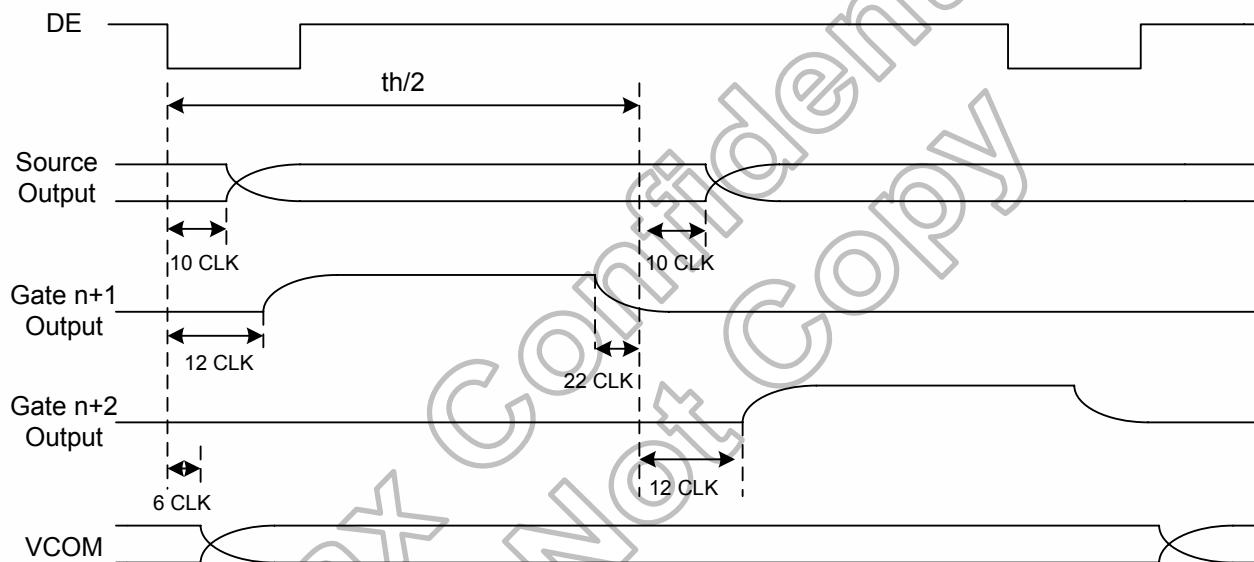


Figure 11.1 Timing Relationship

11.2 Parallel RGB input timing requirement

(480RGBx272, $T_A=25^\circ\text{C}$, $VDDIO=1.8\text{V}$ to 3.6V , $DVSS=0\text{V}$)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock cycle	$f_{CLK}^{(1)}$	-	9	15	MHz
Hsync cycle	$1/th$	-	17.14	-	KHz
Vsync cycle	$1/tv$	-	59.94	-	Hz
Horizontal Signal					
Horizontal cycle	th	525	525	605	CLK
Horizontal display period	thd	480	480	480	CLK
Horizontal front porch	thf	2	2	82	CLK
Horizontal pulse width	thp ⁽²⁾	2	41	41	CLK
Horizontal back porch	thb ⁽²⁾	2	2	41	CLK
Vertical Signal					
Vertical cycle	tv	285	286	399	$H^{(1)}$
Vertical display period	tvd	272	272	272	$H^{(1)}$
Vertical front porch	tvf	1	2	227	$H^{(1)}$
Vertical pulse width	tvp ⁽²⁾	1	10	11	$H^{(1)}$
Vertical back porch	tvb ⁽²⁾	1	2	11	$H^{(1)}$

Note: (1) Unit: $CLK=1/f_{CLK}$, $H=th$,

(2) It is necessary to keep $tvp+tvb=12$ and $thp+thb=43$ in sync mode. DE mode is unnecessary to keep it.



Himax奇景光電

2008.12.25

DCC文件管制中心

P62

(480RGBx240, $T_A=25^\circ\text{C}$, $VDDIO=1.8\text{V}$ to 3.6V , $DVSS=0\text{V}$)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock cycle	$f_{CLK}^{(1)}$	-	9.6	15	MHz
Hsync cycle	1/th	-	15.72	-	KHz
Vsync cycle	1/tv	-	60	-	Hz
Horizontal Signal					
Horizontal cycle	th	525	612	-	CLK
Horizontal display period	thd	480	480	480	CLK
Horizontal front porch	thf	2	30	-	CLK
Horizontal pulse width	thp	2	46	-	CLK
Horizontal back porch	thb	2	56	-	CLK
Vertical Signal					
Vertical cycle	tv	-	262	275	$H^{(1)}$
Vertical display period	tvd	-	240	-	$H^{(1)}$
Vertical front porch	tvf	1	4	-	$H^{(1)}$
Vertical pulse width	tvp	1	3	-	$H^{(1)}$
Vertical back porch	tvb	1	15	-	$H^{(1)}$

Note: (1) Unit: CLK=1/ f_{CLK} , H=th,

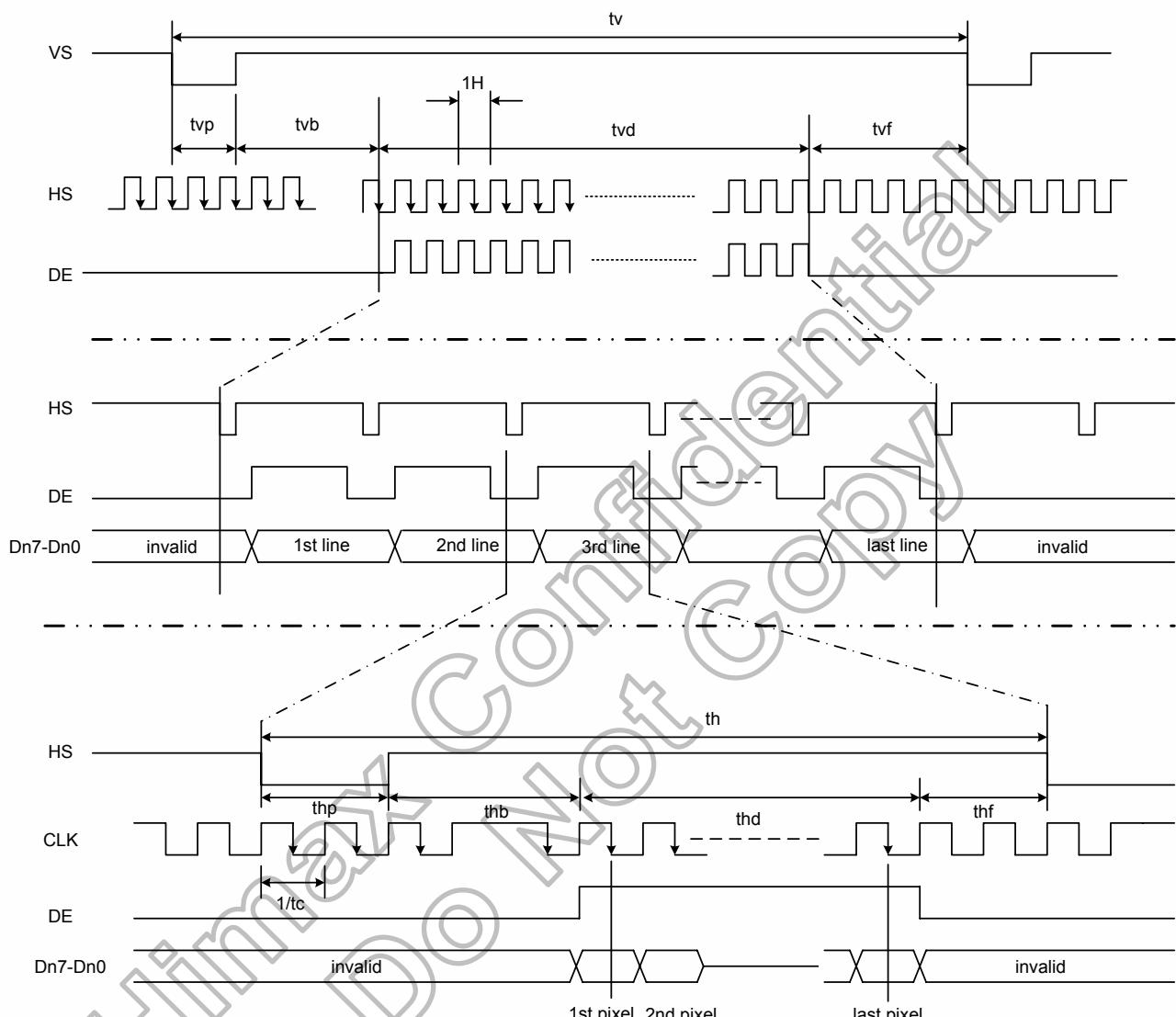


Figure 11.2 Parallel RGB Input Timing

11.3 Serial RGB input timing requirement

(480RGBx272, $T_A=25^\circ C$, $VDDIO=1.8V$ to $3.6V$, $DVSS=0V$)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock cycle	$f_{CLK}^{(1)}$	-	27	33	MHz
Hsync cycle	1/th	-	17.14	-	KHz
Vsync cycle	1/tv	-	59.94	-	Hz
Horizontal Signal					
Horizontal cycle	th	1575	1575	1815	CLK
Horizontal display period	thd	1440	1440	1440	CLK
Horizontal front porch	thf	6	6	246	CLK
Horizontal pulse width	thp	6	123	123	CLK
Horizontal back porch	thb	6	6	123	CLK
Vertical Signal					
Vertical cycle	tv	285	286	399	$H^{(1)}$
Vertical display period	tvd	272	272	272	$H^{(1)}$
Vertical front porch	tvf	1	2	227	$H^{(1)}$
Vertical pulse width	tvp	1	10	11	$H^{(1)}$
Vertical back porch	tvb	1	2	11	$H^{(1)}$

Note: (1) Unit: CLK=1/ f_{CLK} , H=th(480RGBx240, $T_A=25^\circ C$, $VDDIO=1.8V$ to $3.6V$, $DVSS=0V$)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock cycle	$f_{CLK}^{(1)}$	-	28.8	33	MHz
Hsync cycle	1/th	-	15.72	-	KHz
Vsync cycle	1/tv	-	60	-	Hz
Horizontal Signal					
Horizontal cycle	th	1575	1836	-	CLK
Horizontal display period	thd	1440	1440	1440	CLK
Horizontal front porch	thf	6	90	-	CLK
Horizontal pulse width	thp	6	138	-	CLK
Horizontal back porch	thb	6	168	-	CLK
Vertical Signal					
Vertical cycle	tv	-	262	275	$H^{(1)}$
Vertical display period	tvd	-	240	-	$H^{(1)}$
Vertical front porch	tvf	1	4	-	$H^{(1)}$
Vertical pulse width	tvp	1	3	-	$H^{(1)}$
Vertical back porch	tvb	1	15	-	$H^{(1)}$

Note: (1) Unit: CLK=1/ f_{CLK} , H=th

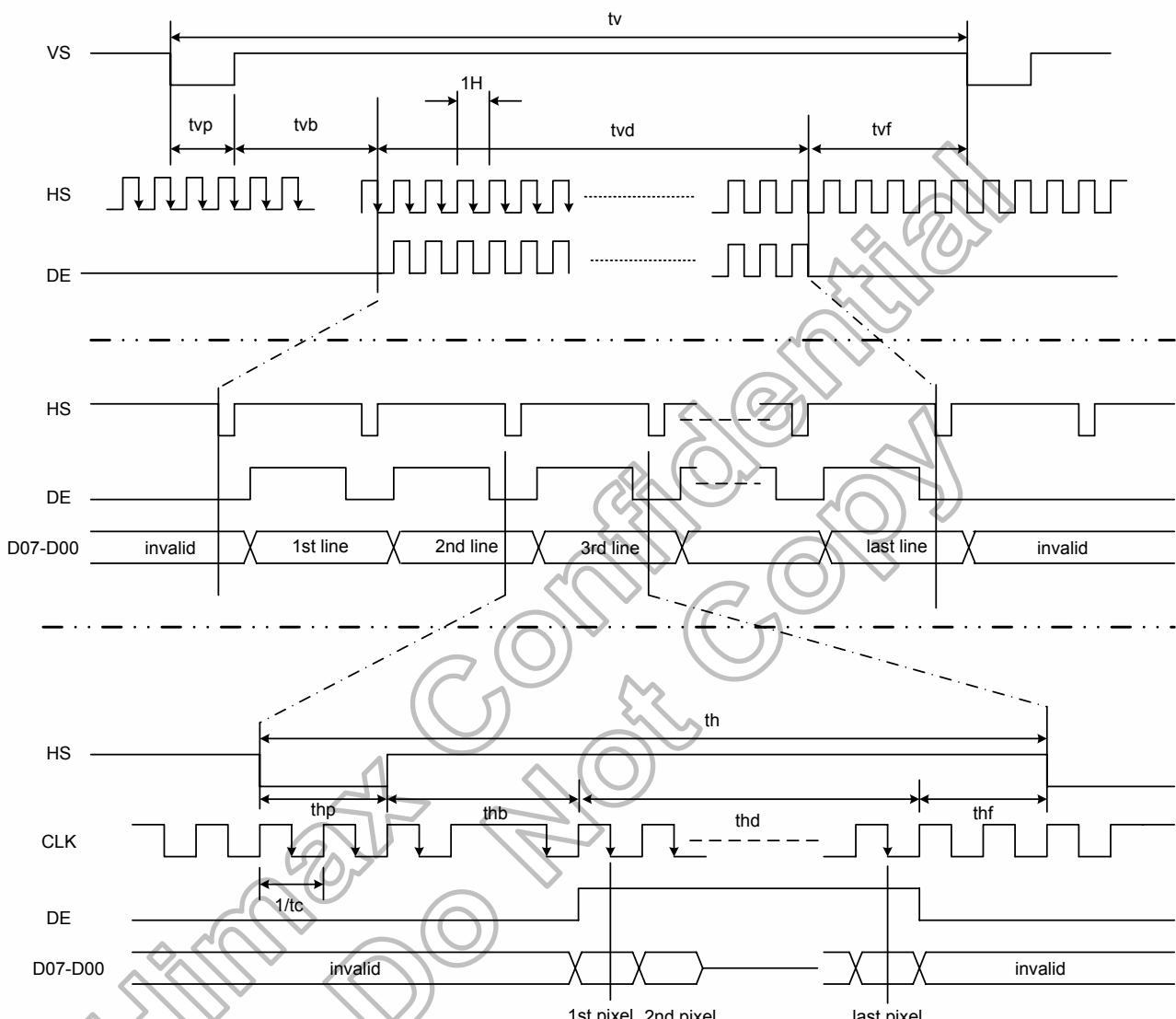


Figure 11.3 Serial RGB Input Timing

11.4 Input setup timing requirement

($T_A = 25^\circ\text{C}$, $VDDIO = 1.8\text{V}$ to 3.6V , $DVSS = 0\text{V}$, $t_r^{(1)} = t_f^{(1)} = 2\text{ns}$)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DISP setup time	t_{diss}	10	-	-	ns
DISP hold time	t_{dish}	10	-	-	ns
Clock period	$PW_{CLK}^{(2)}$	66.7	-	-	ns
Clock pulse high period	$PWH^{(2)}$	26.7	-	-	ns
Clock pulse low period	$PWL^{(2)}$	26.7	-	-	ns
Hsync setup time	t_{hs}	10	-	-	ns
Hsync hold time	t_{hh}	10	-	-	ns
Data setup time	t_{ds}	10	-	-	ns
Data hold time	t_{dh}	10	-	-	ns
DE setup time	t_{des}	10	-	-	ns
DE hold time	t_{deh}	10	-	-	ns
Vsync setup time	t_{vhs}	10	-	-	ns
Vsync hold time	t_{vhh}	10	-	-	ns

Note: (1) t_r , t_f is defined 10% to 90% of signal amplitude.

(2) For parallel interface, maximum clock frequency is 15MHz.

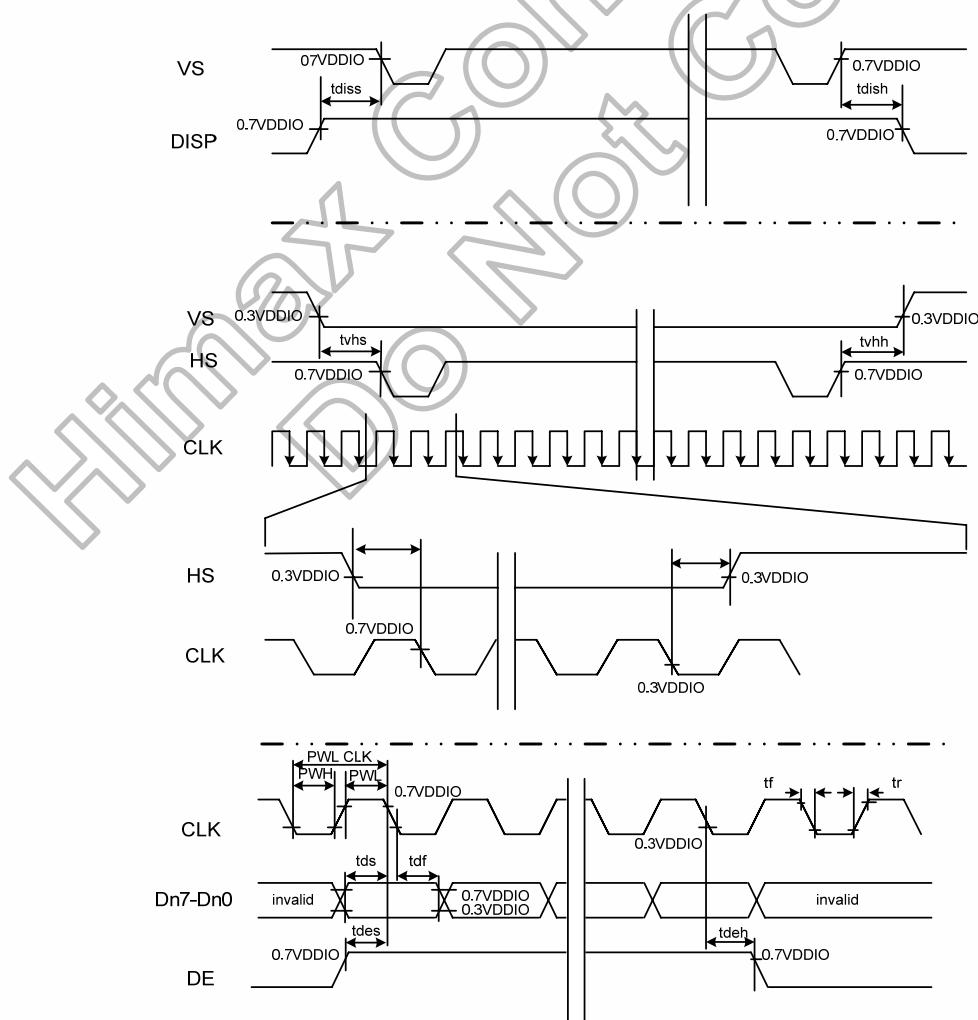


Figure 11.4 Input Setup Timing Requirement

12. Application Circuit

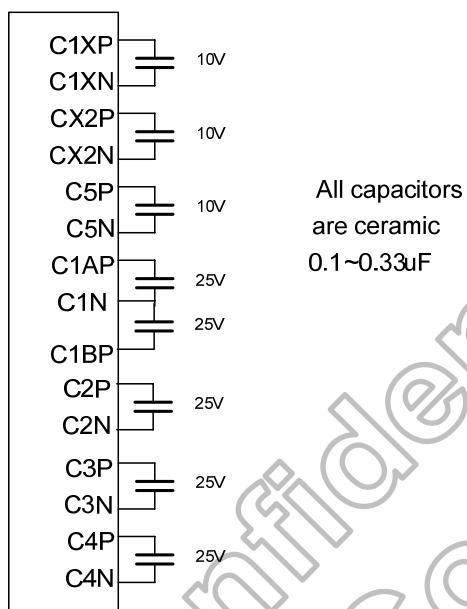


Figure 12.1 Booster Capacitors (VGH=4VDC/VGL=-2VDC)

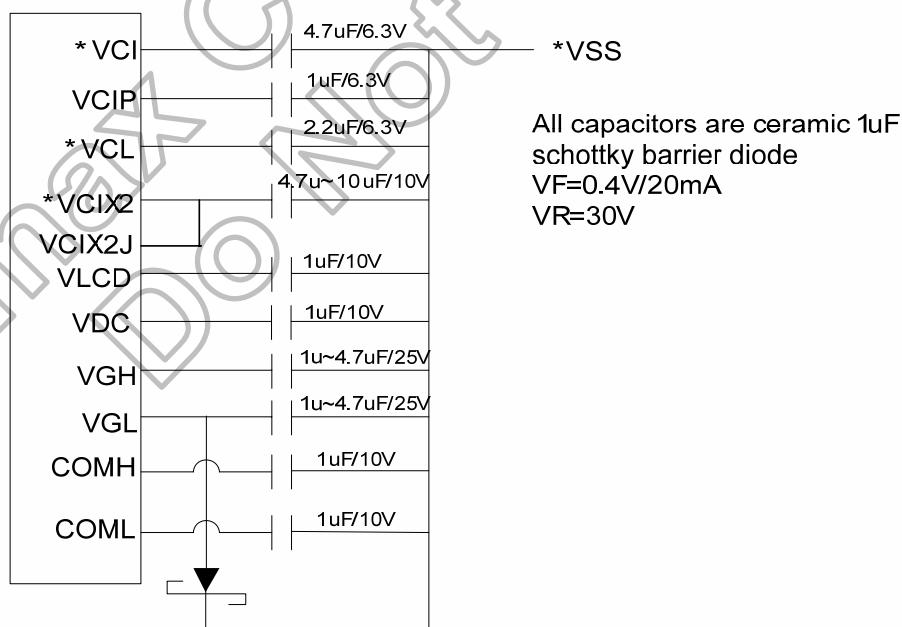


Figure 12.2 Voltage Stable Capacitors & Schottky Diode

- (a) Capacitors on VCI should be 4.7uF.
- (b) Capacitors on VCL should be 2.2uF
- (c) Capacitors on VCIX2 should be 4.7~10uF
- (d) Capacitors on VGH, VGL should be 1~4.7uF
- (e) Other capacitors should be 1uF

Note: (1) VCI should be separated from VCIP at ITO layout on glass to provide noise free path
 (2) DVSS, VCHS, AVSS, and VSSRC should be separated at ITO layout on glass to provide noise free path



13. Ordering Information

Part NO.	Package
HX8257-A01BPDXXX	PD : means COG XXX : means chip thickness(μm), default 400μm

14. Revision History

Version	Date	Description of Changes
01	2008/11/30	New setup