FT6x06

Self-Capacitive Touch Panel Controller

INTRODUCTION

The FT6x06 Series ICs are single-chip capacitive touch panel controller ICs with a built-in 8 bit enhanced Micro-controller unit (MCU).They adopt the self-capacitance technology, which supports single point and gesture touch. In conjunction with a self-capacitive touch panel, Friendly UI can be applied on many portable devices, such as cellular phones, GPS and digital camera.

The FT6x06 series ICs include FT6206 /FT6306, the difference of their specifications will be listed individually in this datasheet.

FEATURES

- Self-Capacitive Sensing Techniques support single point touch and differential sensing
- Absolute X and Y Coordinates or gesture
- Auto-calibration: Insensitive to Capacitance and Environmental Variations
- Built-in Enhanced MCU
- FT6206 supports up to 28 channels of sensors /drivers
- FT6306 supports up to 36 channels of sensors /drivers
- Report Rate: Up to 80Hz
- Support Interfaces :IIC
- Support single Film material TP and diamond pattern without additional shield
- Internal accuracy ADC and smooth Filter
- Support 2.8V to 3.6V Operating Voltage
- Supports independent IOVCC
- Built-in LDO for Digital Circuits
- High efficient consumption management with 3 Operating Modes
  - Active Mode
  - Monitor Mode
  - Hibernation Mode
- Operating Temperature Range: -20°C to +85°C
- ESD:HBM≥5000V,

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT6x06 accommodate a wide range of applications with a set of buttons up to a 2D touch sensing device, their typical applications are listed below.

- Mobile phones, smart phones
- GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT6x06 Series ICs support up to 7" Touch Panel, users may find out their target IC from the specs listed in the following table,

Model Name	Panel	Package			Touch Panel Size
	Channel	Type	Pin	Size	
FT6206GMA	28	QFN5*5	40	0.6-P0.4	2.8"～4.3"
FT6306DMB	36	QFN6*6	48	0.6-P0.4	4.3"～7"

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT6x06.

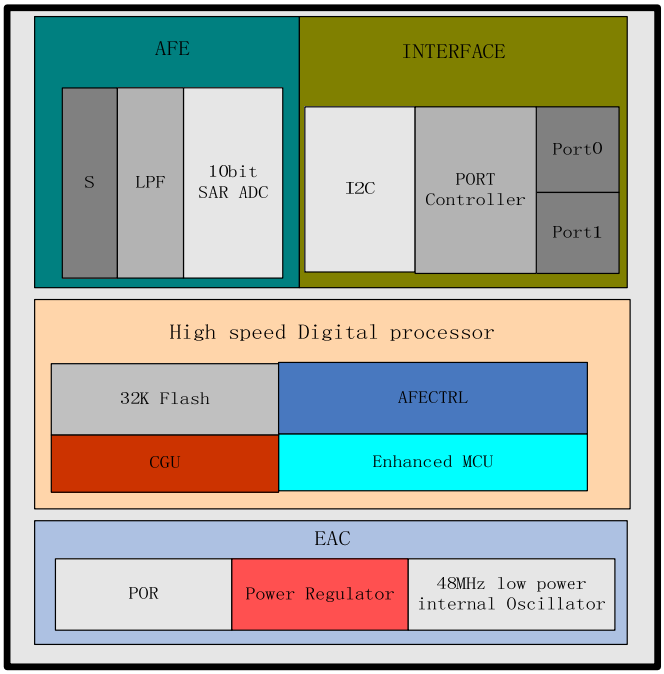


Figure 2-1 FT6x06 System Architecture Diagram

The FT6x06 is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So it supports both driver and Sensor functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU

For the Enhanced MCU, larger program and data memories are supported. Furthermore, A Flash ROM is implemented to store programs and some key parameters.
Complex signal Processing algorithms are implemented by MCU to detect the touches reliably and efficiently.
Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDDA supply.

2.2 MCU

This section describes some critical features and operations supported by the Enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the Enhanced MCU core, we have added the following circuits,

- Program Memory:32KB Flash
- Data Memory: 2KB SRAM
- Timer: A number of timers are available to generate different clocks
- Master Clock:12/24/ 48MHz from a 48MHz RC Oscillator
- Clock Manager: To control various clocks under different operation conditions of the system

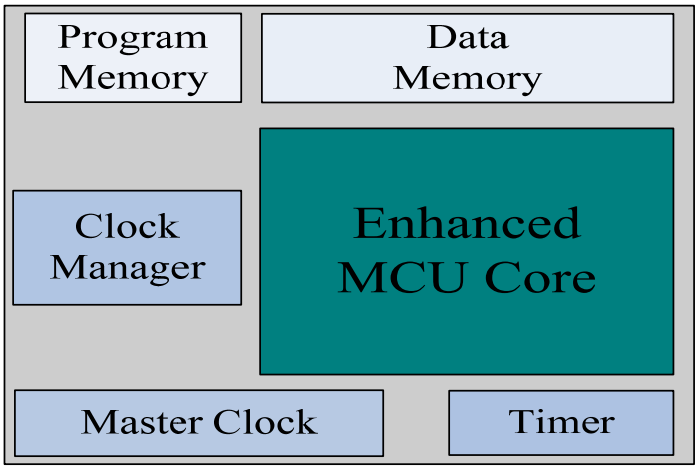


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT6x06 operates in the following three modes:

- Active Mode

In this mode, FT6x06 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT6x06 to speed up or to slow down.

- Monitor Mode

In this mode, FT6x06 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT6x06 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor

- Hibernation Mode

In this mode, the chip is set in a power down mode. It shall respond to the "RESET" or "Wakeup" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

Host InterfaceFigure *2-3* shows the interface between a host processor and FT6x06. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT6x06 to the Host
- Reset Signal from the Host to FT6x06

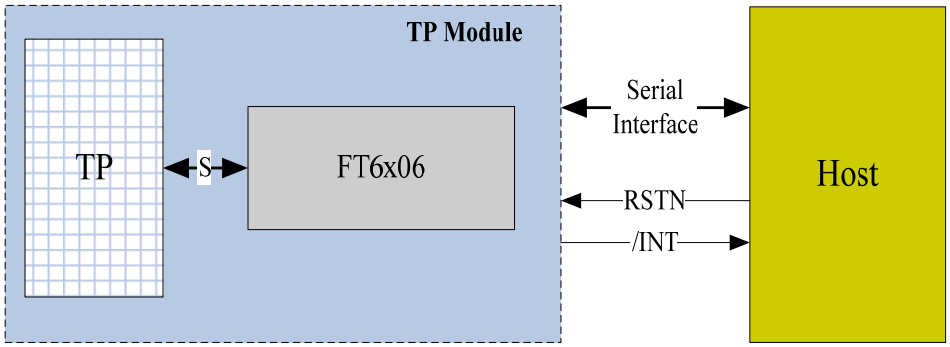


Figure 2-3 Host Interface Diagram

The serial interface of FT6x06 is I2C. The details of this interface are described in detail in Section 2.5. The interrupt signal (/INT) is used for FT6x06 to inform the host that data are ready for the host to receive. The RSTN signal is used for the host to reset FT6x06. After resetting, FT6x06 shall enter the Active mode.

2.4 Serial Interface

FT6x06 supports the I2C interfaces, which can be used by a host processor or other devices.

2.4.1 I2C

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

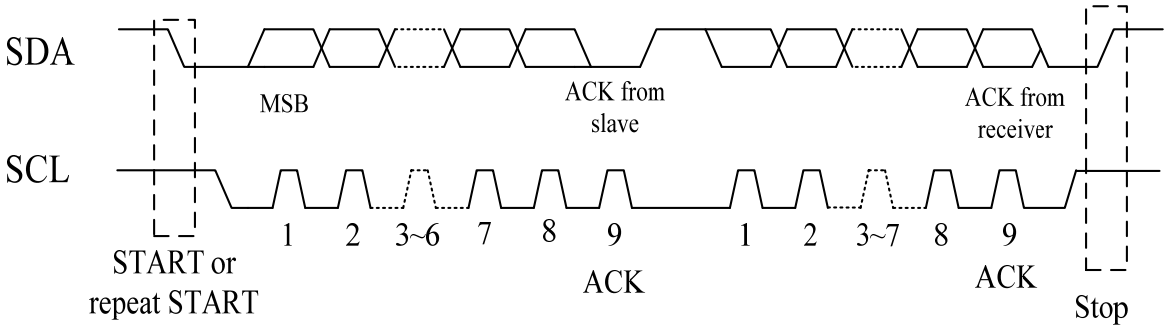


Figure 2-4 I2C Serial Data Transfer Format

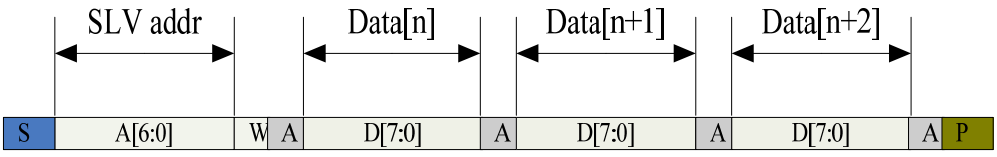


Figure 2-5 I2C master write, slave read

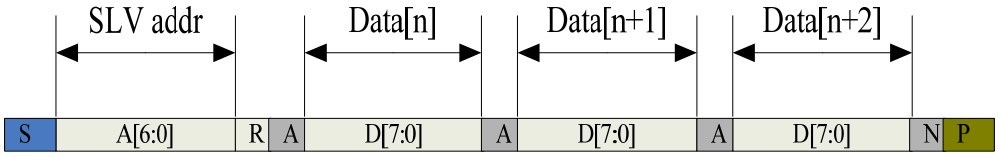


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDDA - VSSA	-0.3 ~ +3.6	V	1, 2
I/O Digital Voltage	IOVCC	1.8~3.6	V	1
Operating Temperature	Topr	-20 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

Notes
1. If used beyond the absolute maximum ratings, FT6x06 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDDA (high) ≥VSSA (low).

3.2 DC Characteristics

Table 3-2 DC Characteristics (VDDA=2.8~3.3V, Ta=-20~85℃)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		0.7 x IOVCC	--	IOVCC	V	
Input low -level voltage	VIL		-0.3	--	0.3 x IOVCC	V	
Output high -level voltage	VOH	IOH=-0.1mA	0.7 x IOVCC	--	--	V	
Output low -level voltage	VOL	IOH=0.1mA	--	--	0.3 x IOVCC	V	
I/O leakage current	ILI	Vin=0~VDDA	-1	--	1	μA	
Current consumption （Normal operation mode）	Iopr	VDDA = 3.3V Ta=25℃ MCLK=24MHz	--	2.1	--	mA	
Current consumption （Monitor mode）	Imon	VDDA = 3.3V Ta=25℃ MCLK=24MHz	--	TBD	--	mA	
Current consumption （Sleep mode）	Islp	VDDA = 3.3V Ta=25℃ MCLK=24MHz	--	0.03	--	mA	
Step-up output voltage	VDD5	VDDA = 3.3V	3.3	5	TBD	V	
Power Supply voltage	VDDA		2.8	-	3.6	V	

3.3 AC Characteristics

Table 3-3 AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
OSC clock 1	fosc1	VDDA= 3.3V Ta=25℃	47	48	49	MHz	

Table 3-4 AC Characteristics of #S

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
#S acceptable clock	F#s		-	160	-	KHz	
#S rise time	T#s r		-	1.5	-	nS	
#S fall time	T#s f		-	250	-	nS	

3.4 I/O Ports Circuits

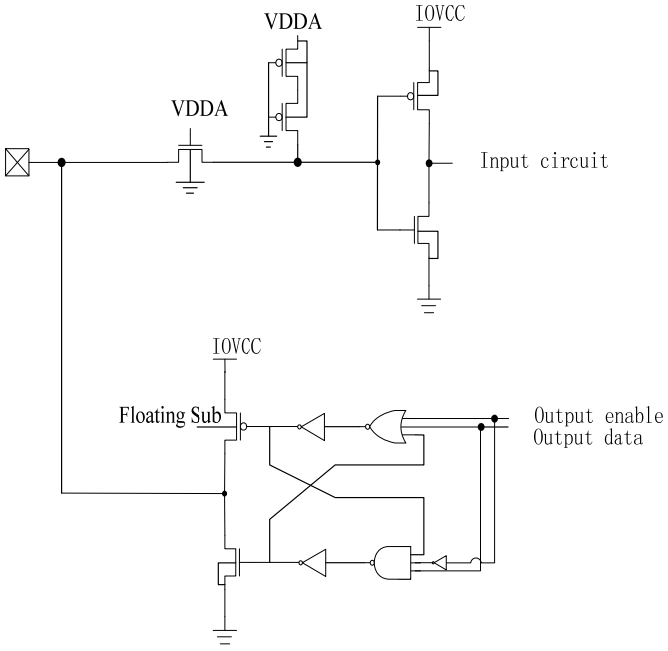


Figure 3-1 Digital In/Out Port Circuit

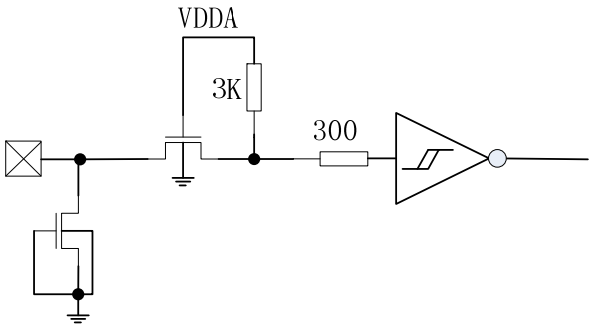


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset/Wake Sequence

The GPIO such as INT and I2C are advised to be low before powering on. Reset should be pulled down to be low before powering on. INT signal will be sent to the host after initializing all parameters and then start to report points to the host.

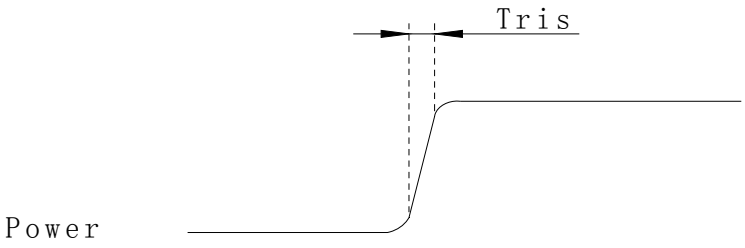


Figure 3-7 Power on time

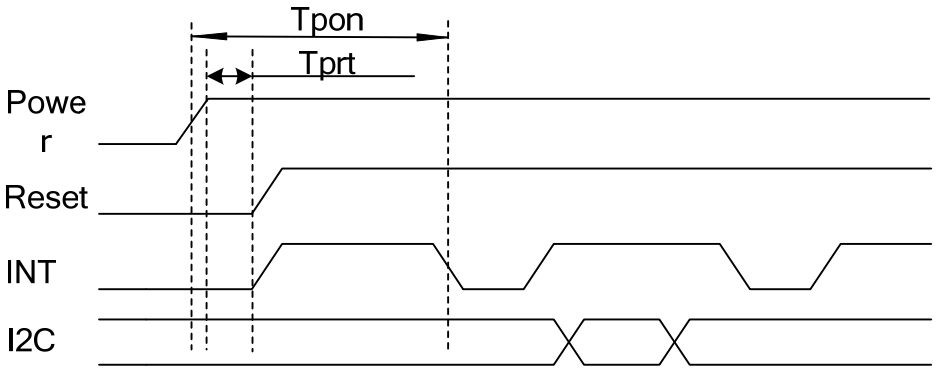


Figure 3-8 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

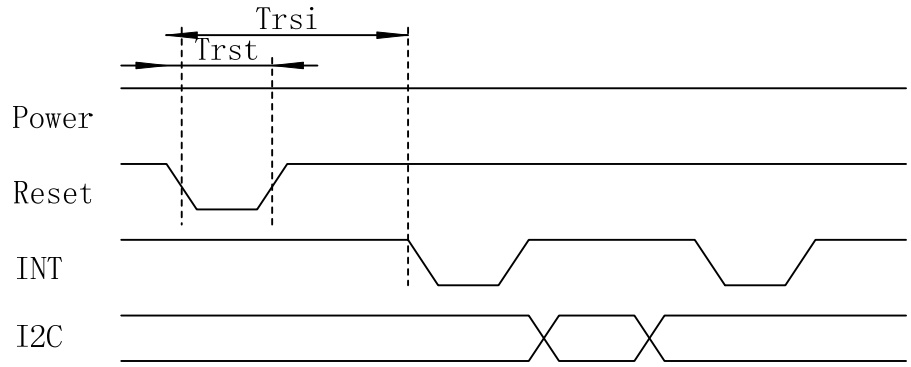


Figure 3-8 Reset Sequence

Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	3	ms
Tpon	Time of starting to report point after powering on	300	--	ms
Tprt	Time of being low after powering on	1	--	ms
Trsi	Time of starting to report point after resetting	300	--	ms
Trst	Reset time	5	--	ms

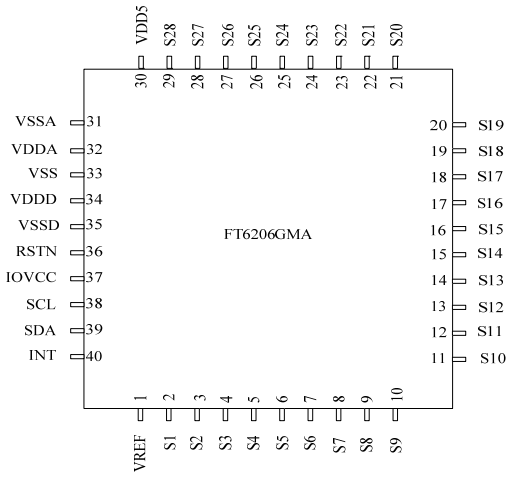
4 PIN CONFIGURATIONS

Pin List of FT6x06

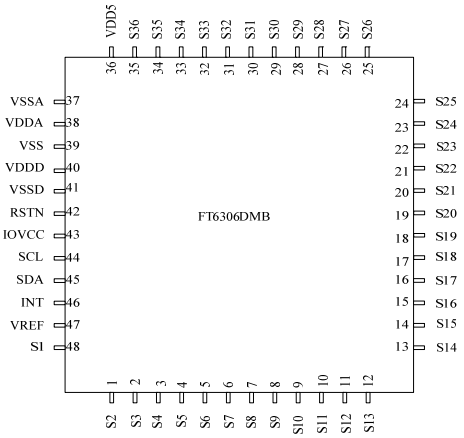
Table 4-1 Pin Definition of FT6x06

Name	Pin No.		Type	Description
	FT6206GMA	FT6306DMB		
VREF	1	47	PWR	Generated internal reference voltage. A 1μF ceramic capacitor to ground is required.
S1	2	48	I/O	Capacitance sensor /driver channel
S2	3	1	I/O	Capacitance sensor /driver channel
S3	4	2	I/O	Capacitance sensor /driver channel
S4	5	3	I/O	Capacitance sensor /driver channel
S5	6	4	I/O	Capacitance sensor /driver channel
S6	7	5	I/O	Capacitance sensor /driver channel
S7	8	6	I/O	Capacitance sensor /driver channel
S8	9	7	I/O	Capacitance sensor /driver channel
S9	10	8	I/O	Capacitance sensor /driver channel
S10	11	9	I/O	Capacitance sensor /driver channel
S11	12	10	I/O	Capacitance sensor /driver channel
S12	13	11	I/O	Capacitance sensor /driver channel
S13	14	12	I/O	Capacitance sensor /driver channel
S14	15	13	I/O	Capacitance sensor /driver channel
S15	16	14	I/O	Capacitance sensor /driver channel
S16	17	15	I/O	Capacitance sensor /driver channel
S17	18	16	I/O	Capacitance sensor /driver channel
S18	19	17	I/O	Capacitance sensor /driver channel
S19	20	18	I/O	Capacitance sensor /driver channel
S20	21	19	I/O	Capacitance sensor /driver channel
S21	22	20	I/O	Capacitance sensor /driver channel
S22	23	21	I/O	Capacitance sensor /driver channel
S23	24	22	I/O	Capacitance sensor /driver channel
S24	25	23	I/O	Capacitance sensor /driver channel
S25	26	24	I/O	Capacitance sensor /driver channel
S26	27	25	I/O	Capacitance sensor /driver channel
S27	28	26	I/O	Capacitance sensor /driver channel
S28	29	27	I/O	Capacitance sensor /driver channel
S29		28	I/O	Capacitance sensor /driver channel
S30		29	I/O	Capacitance sensor /driver channel
S31		30	I/O	Capacitance sensor /driver channel
S32		31	I/O	Capacitance sensor /driver channel
S33		32	I/O	Capacitance sensor /driver channel
S34		33	I/O	Capacitance sensor /driver channel
S35		34	I/O	Capacitance sensor /driver channel
S36		35	I/O	Capacitance sensor /driver channel

VDD5	30	36	PWR	High voltage power supply from the charge pump LDO generated internally. A 1μF ceramic to ground is required.
VSSA	31	37	GND	Analog ground
VDDA	32	38	PWR	Analog power supply, A 1μF ceramic capacitor to ground is required.
VSS	33	39	GND	Analog ground
VDDD	34	40	PWR	Digital power supply. A 1μF ceramic capacitor to ground is required.
VSSD	35	41	GND	Analog ground
RSTN	36	42	I	External Reset, Low is active
IOVCC	37	43	PWR	I/O power supply
SCL	38	44	I/O	I2C clock input
SDA	39	45	I/O	I2C data input and output
INT	40	46	I/O	External interrupt to the host



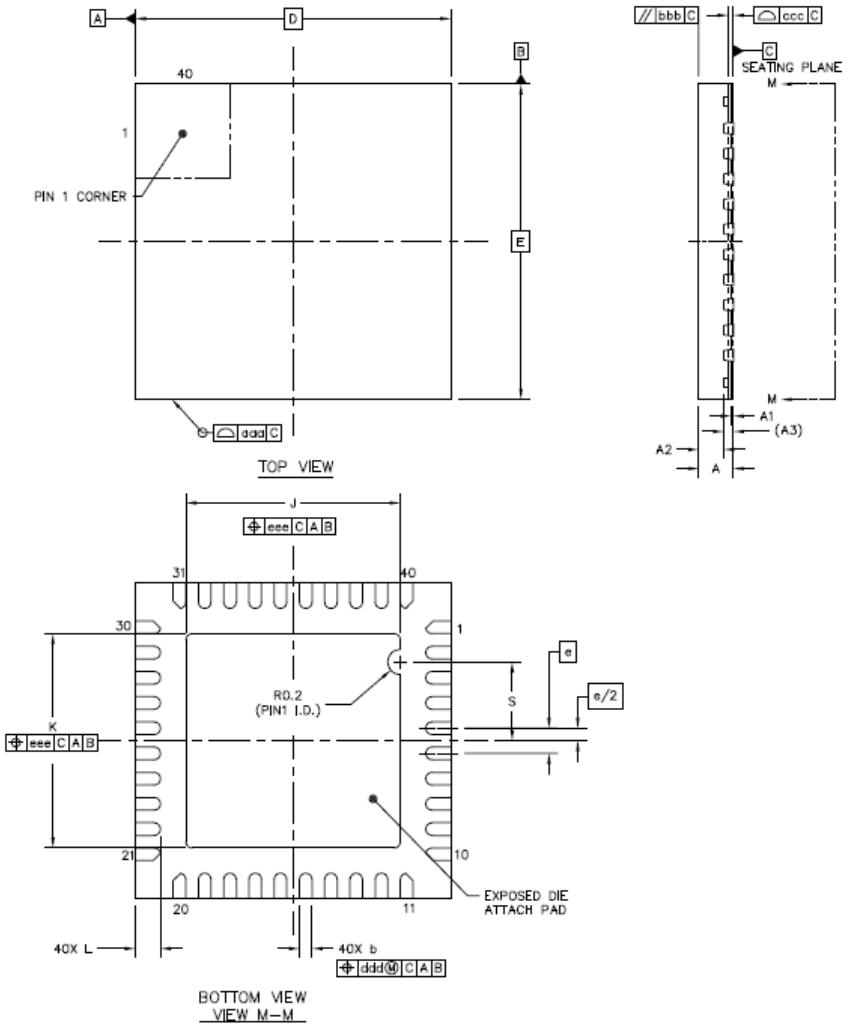
FT6206GMA Package Diagram



FT6306DMB Package Diagram

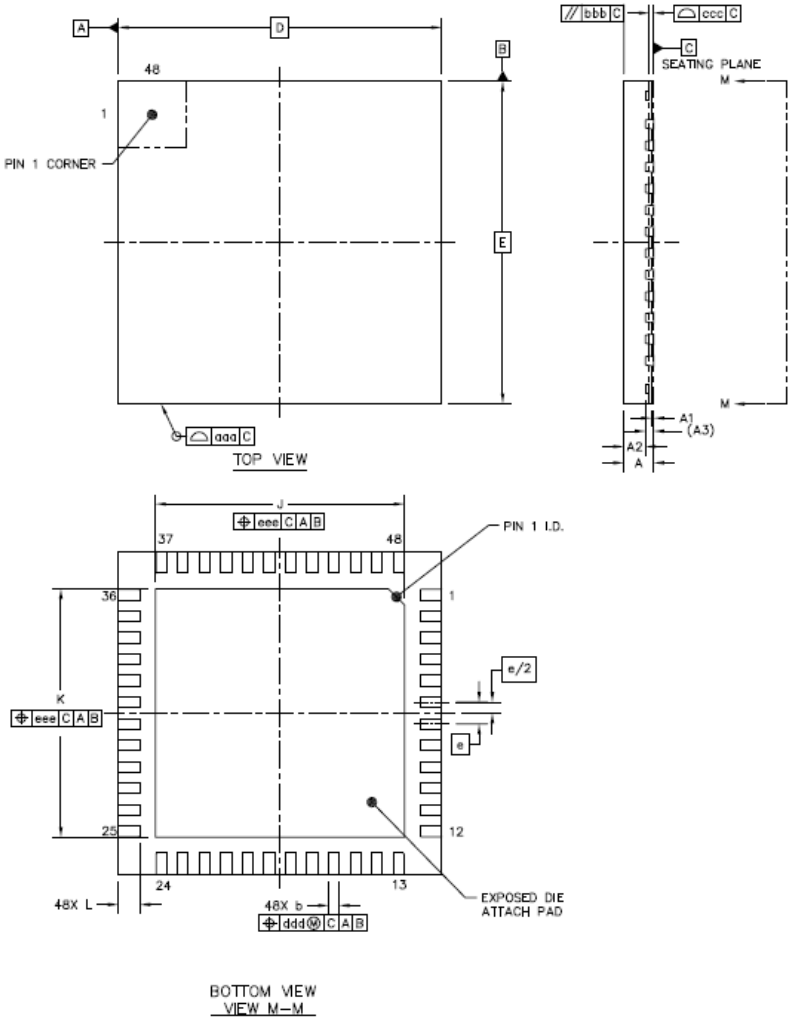
5 PACKAGE INFORMATION

5.1 Package Information of QFN-5x5-40L Package



Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	0.425
L/F Thickness	A3		0.152 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		5 BSC	
	E		5 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	3.3	3.4	3.5
	K	3.3	3.4	3.5
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.2 Package Information of QFN-6x6-48L Package



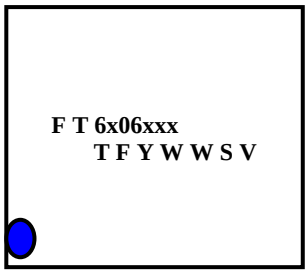
Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	0.425
L/F Thickness	A3	0.152 REF		
Lead Width	b	0.15	0.20	0.25
Body Size	D	6 BSC		
	E	6 BSC		
Lead Pitch	e	0.4 BSC		
EP Size	J	4.52	4.62	4.72
	K	4.52	4.62	4.72
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Co Planarity	ccc	0.08		
Lead Offset	ddd	0.1		
Exposed Pad Offset	eee	0.1		

5.3 Order Information

Package Type	QFN
	40Pin(5 * 5)/48Pin(6 * 6)
	0.6-P0.4
Product Name	FT6206GMA / FT6306DMB

Note:
1). The last two letters in the product name indicate the package type and lead pitch and thickness.
2). The three last letter indicates the package type..
D : QFN-6*6 , G : QFN-5*5
3). The second last letter indicates the lead pitch and thickness.
M : 0.6-P0.4
4). The last letter indicates the numbers of sensors.
A：28， B：36

T: Track Code
F/R:"F" for Lead Free process,
"R" for Halogen Free process
Y: Year Code
WW: Week Code
S: Lot Code
V：IC Version



Product Name	Package Type	#S Pins
FT6206GMA	**QFN-40L**	**28**
FT6306DMB	**QFN-48L**	**36**

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