FGD0801 Datasheet

1. General Description

The FGD0801 is a 262K-color, single-chip LCD driver for the TFT panel with 128RGB x 160 dots at maximum, which contains a gate driver, a source driver, power supply, timing controller circuit and internal RAM for graphics data of 128 RGB x 160 dots at maximum.

The FGD0801 supports five interfaces: 80-system 18-/16-/9-/8-bit bus interface, 68-system 18-/16-/9-/8-bit bus interface, serial data transfer interface, VSYNC interface (system interface + VSYNC) and RGB 18-/16-/6-bit bus interface (DOTCLOCK, VSYNC, HSYNC, ENABLE, DB17-0). In RGB 18-/16-/6-bit bus interface and VSYNC interface mode, using window address function to display moving picture and still picture simultaneously can reduce the power consumption. The FGD0801 can be operated in low-voltage (1.65V) condition to the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. The FGD0801 also supports various functions to reduce power consumption, such as 8-color display mode, sleep mode and standby mode.

The FGD0801A is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as digital cellular phones, small PDAs and bi-directional pagers.

2. Features

- Single chip solution to drive a TFT panel
- Internal operation circuit of liquid crystal display:
  - Source channel: 384
  - Gate line: 160
- Internal graphics RAM capacity: 46,080 bytes
- 128RGB x 160 dots graphics display LCD controller/driver and 262K colors
- The 262K colors can be displayed at the same time with gamma correction
- Support interface:
  - 80-system interface (18-/16-/9-/8-bit bus)
  - 68-system interface (18-/16-/9-/8-bit bus)
  - Serial data transfer interface
  - VSYNC data transfer interface
  - RGB interface (18-/16-/6-bit bus)
- Low-power consumption architecture supports:
  - VCI = 2.5 ~ 3.3 V (internal analog power supply)
  - VCC = 2.4 ~ 3.3 V (internal digital power supply)
  - IOVCC = 1.65 ~ 3.3 V (internal I/O power supply)
  - VLCD = 4.5~5.5V (internal driving power supply)
  - VDDD = 1.8V (internal logic power supply)
  - Power-saving functions
    8-color mode
    Standby mode
    Sleep mode
- To write data in a window-RAM address area by using a window-address function
- N-line inversion AC liquid-crystal drive
- Partial liquid crystal drive to display two screens at arbitrary positions
- Vertical scrolling function
- Internal oscillator and hardware reset function

3. Device Description

3.1 Block Diagram

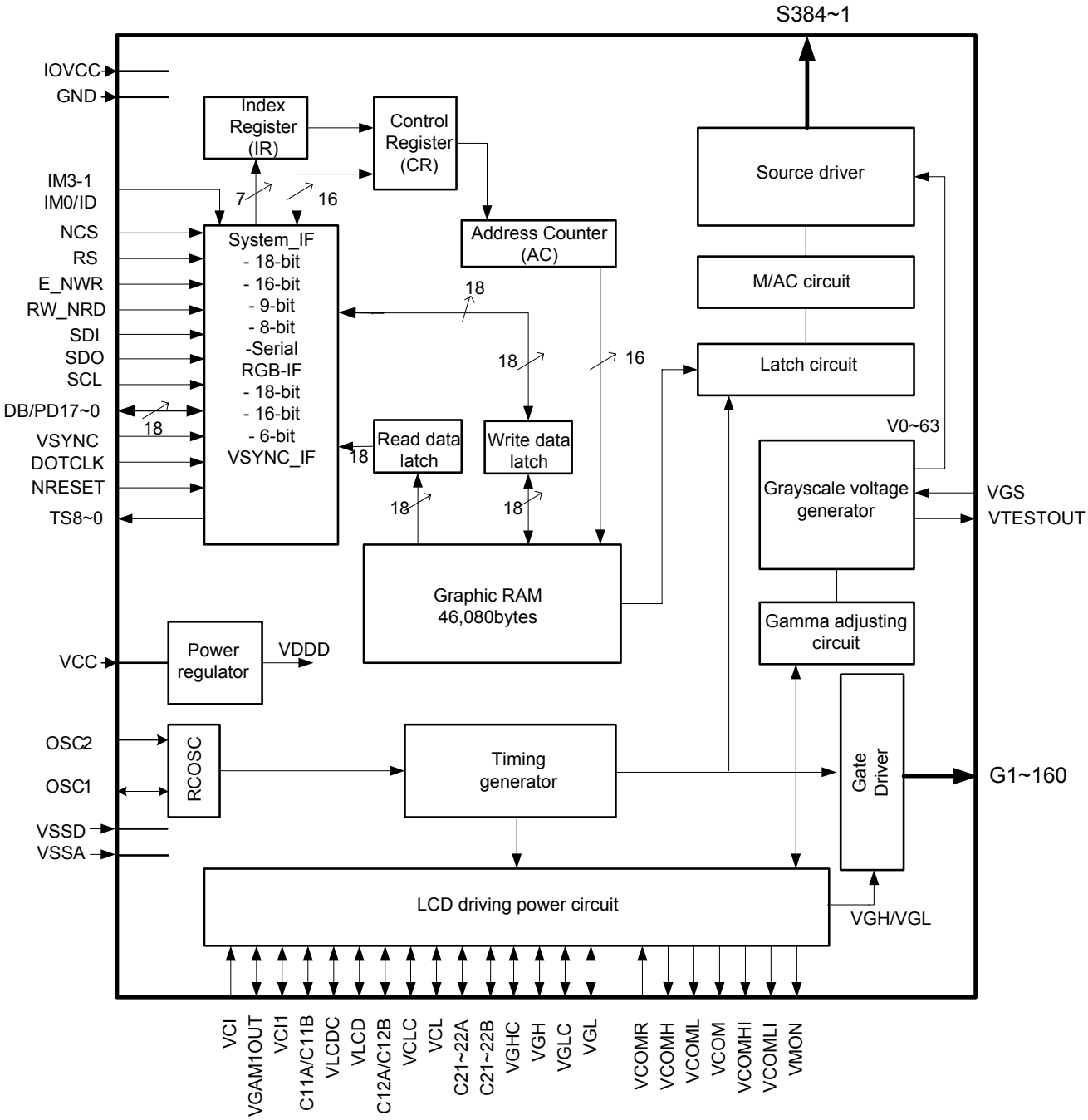


Figure 1 Block Diagram

3.2 Pin Description

Table 1 Pin description

<table>
<tr><th colspan="11">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th colspan="7">Descriptions</th></tr>
<tr><td rowspan="15">IM3-0</td><td rowspan="15">I</td><td rowspan="15">4</td><td rowspan="15">VSSD/IOVCC</td><td colspan="7">Select the MPU interface mode as listed below</td></tr>
<tr><td>IM0(ID)</td><td>IM1</td><td>IM2</td><td>IM3</td><td colspan="2">MPU interface mode</td><td>DB pins</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">16-bit interface, 68-system</td><td>DB17-10,8-1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td colspan="2">8-bit interface, 68-system</td><td>DB17-10</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="2">16-bit interface, 80-system</td><td>DB17-10,8-1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="2">8-bit interface, 80-system</td><td>DB17-10</td></tr>
<tr><td>ID</td><td>0</td><td>1</td><td>0</td><td colspan="2">Serial data transfer interface</td><td>DB1-0</td></tr>
<tr><td>*</td><td>1</td><td>1</td><td>0</td><td colspan="2">Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td colspan="2">18-bit interface, 68-system</td><td>DB17-0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td colspan="2">9-bit interface,68-system</td><td>DB17-9</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td colspan="2">18-bit interface, 80-system</td><td>DB17-0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td colspan="2">9-bit interface,80-system</td><td>DB17-9</td></tr>
<tr><td>*</td><td>*</td><td>1</td><td>1</td><td colspan="2">Setting invalid</td><td>-</td></tr>
<tr><td colspan="7">Note: if the serial data transfer interface was selected, IM0 pin is used like the ID setting for the device code in transfer data.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td colspan="7">Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
Must be connected to VSSD if not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>1</td><td>MPU</td><td colspan="7">The signal for register index or register command select.
Low: Register index or internal status (in read operation);
High: Register command.
Connect to IOVCC or VSSD level when serial data transfer interface is selected.</td></tr>
<tr><td>E_NWR</td><td>I</td><td>1</td><td>MPU</td><td colspan="7">In 80-system bus interface mode, serves as a write strobe signal. Write data at the ”low” level.
In 68-system Interface mode, serves as an ENABLE signal to control data read/write operation.</td></tr>
<tr><td>RW_NRD</td><td>I</td><td>1</td><td>MPU</td><td colspan="7">Serves as a read signal and reads data at the low level in 80-system interface. Fix it to IOVCC or VSSD level when using serial data transfer interface.</td></tr>
<tr><td rowspan="6">ENABLE</td><td rowspan="6">I</td><td rowspan="6">1</td><td rowspan="6">MPU</td><td colspan="7">A data ENABLE signal in RGB I/F mode. Fix the unused pin to either the VSSD level or the IOVCC level.
Low: Selected (access enabled)
The polarity of the ENABLE signal is inverted by the EPL bit.</td></tr>
<tr><td colspan="2">EPL</td><td>ENABLE</td><td colspan="2">RAM write</td><td>RAM address</td></tr>
<tr><td colspan="2">0</td><td>0</td><td colspan="2">Enable</td><td>Update</td></tr>
<tr><td colspan="2">0</td><td>1</td><td colspan="2">Disable</td><td>Keep</td></tr>
<tr><td colspan="2">1</td><td>0</td><td colspan="2">Disable</td><td>Keep</td></tr>
<tr><td colspan="2">1</td><td>1</td><td colspan="2">Enable</td><td>Update</td></tr>
</table>

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Descriptions**
SDI	I	1	MPU	Serial data transfer input in serial data transfer interface mode.Data would be latched on the rising edge of the SCL signal. Fixed to either IOVCC or VSSD if not in use.
SCL	I	1	MPU	A synchronizing clock signal in serial data transfer interface mode. Fixed to either IOVCC or VSSD if not in use.
VSYNC	I	1	MPU	Frame synchronizing signal. The polarity of the VSYNC signal is selected by VSPL bit. Fix to the IOVCC level when not used. If VSPL=0: Start in the low level. If VSPL=1: Start in the high level.
HSYNC	I	1	MPU	Line synchronizing signal. The polarity of the HSYNC signal is selected by HSPL bit. Fix to the IOVCC level when not used. If HSPL=0: Start in the low level. If HSPL=1: Start in the high level.
DOTCLK	I	1	MPU	Dot clock signal. Fix to the IOVCC level when not used. If DPL=0: Data are input on the falling edge of DOTCLK. If DPL=1: Data are input on the rising edge of DOTCLK.
NRESET	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
VCOMR	I	1	Variable Resistor or open	A VCOMH reference voltage. When adjusting VCOMH externally, set registers to halt the VCOMH internal adjusting circuit and place a variable resistor between VGAM1OUT and VSSD. Otherwise, leave this pin open and adjust VCOMH by setting the internal register of the FGD0801.
VLCD	I	4	Stabilizing capacitor VLCDC	A power supply for the source driver outputs. A reference voltage for step-up circuit2.
VGH	I	3	Stabilizing capacitor	A power supply for the TFT LCD's gate driver. Connect to Stabilizing capacitor. Max VGH = 16.5V
VGL	I	3	Stabilizing capacitor	A power supply for the TFT LCD's gate driver. Connect to Stabilizing capacitor. Min VGH = -16.5V
VCL	I	2	Stabilizing capacitor	A power supply for the VCOML level. Connect to Stabilizing capacitor. VCL=0~-3.3V
TEST1	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
TEST2	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
VGS	I	2	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel use.
VCI	I	7	Power supply	For analog power supply. Connect to an external power supply 2.5V~3.3V.
VCILVL	I	1	Power supply	Generates a reference voltage (VCIOUT, REGP) from the VCILVL level according to the ratio determined by the VC2-0 bits. Connect to VCI on the FPC.
VCC	-	6	Power supply	A power supply for the internal logic. VCC = 2.4 ~ 3.3V
IOVCC	-	2	Power supply	Power supply for interface pin. IOVCC = 1.65 ~3.3 V. Connect to VCC on the FPC, if IOVCC = VCC for preventing noise when using the COG method.
VSSD	-	9	Power supply	Ground for the logic side. VSSD = 0V
VSSA	-	5	Power supply	Analog ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
SDO	O	1	MPU	Serial data transfer output in serial data transfer interface mode. Data would be output on the falling edge of the SCL signal. When SDO is not used, leave it open.
S1-384	O	384	LCD	Output voltages applied to the liquid crystal. The shift direction of segment signal outputs is changeable with the SS bit. For example, if SS=0, data in the RAM address"0000"is output from S1. If SS=1,the same data in the RAM address"0000" is output from S384. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), S3, S6, S9, ... display blue (B) (SS = 0,BGR = 0).
G1-160	O	160	LCD	Output signals from gate lines. VGH: the level to select the gate lines. VGL: the level not to select the gate lines.
VCOM	O	4	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. The alternation cycle can be set by the POL pin. Connect this pin to the common electrode in TFT panel.
VCOMH	O	3	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	O	3	Stabilizing capacitor or open	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VCOML output stops and a capacitor for stabilization is not needed.
FLM	O	1	MPU or open	A frame head pulse (amplitude: IOVCC-VSSD). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it.
VLCDC	O	2	VLCD	A power supply for the source driver outputs. A reference voltage for the step-up circuit2. Connect to VLCD.
VGHC	O	1	VGH	A power supply for the TFT-LCD' s gate driver. Connect to VGH.
VGLC	O	1	VGL	A power supply for the TFT-LCD' s gate driver. Connect to VGL.
VCLC	O	1	VCL	An output from the step-up circuit of 1- time the VCI1 level. VCLC= 0 ~ 3.3V
TS0-8	O	8	Open	Test pins. Disconnect them.
VMON	O	1	Open	A test pin. Disconnect it.
IOVCCDUM1	O	1	Input pin	Internal IOVCC level outputs. When adjacent input pins are fixed to the IOVCC level , short-circuit them .
IOGNDDUM1~3	O	3	Input pin	Internal VSSD level outputs. When neighboring input pins are fixed to the VSSD level, short-circuit them.
VTESTOUT	O	1	-	A test pin. Disconnect it.
TVCOMHI	O	1	Stabilizing capacitor	A reference voltage for VCOMH. Must be connected with the capacitor 0.1uF.
TVCOMLI	I/O	1	Open	A test pin. Disconnect it.
TVMAG	O	1	Stabilizing capacitor	A reference voltage for VCOML. Must be connected with the capacitor 0.1uF.
VDDD	O	4	Stabilizing capacitor	A stabilizing capacitor for logic power. Connect with the capacitor 1uF.

Input/output Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Descriptions**
C11A,C11B	I/O	8	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
C12A,C12B C21A,C21B C22A,C22B	I/O	16	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2, according to the step-up rate. When not using the step-up circuit 2, disconnect them.
OSC1,OSC2	I/O	2	Oscillation Register	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
DB17~0	I/O	18	MPU	It is used liked an 18-bit bi-directional data bus. 8-bit bus: use DB17-10 9-bit bus: use DB17-9 16-bit bus: use DB17-10 and DB8-1 18-bit bus: use DB17-0 Connected unused pins to the IOVCC or VSSD level.
REGP	I/O	1	Open	A test pin for VGAM1OUT. Disconnect it.
VGAM1OUT	I/O	1	Stabilizing Capacitor or power supply	A reference voltage for VGAM between VSSD and VGL from the reference voltage between VCI and VSSD that is generated internally. VGAM1OUT serves as a source driver grayscale reference voltage, and a VCOM amplitude reference voltage. Connect to a stabilizing capacitor. VGAM1OUT=3.0~(VLCDC-0.5)V
VCI1OUT	O	6	Stabilizing capacitor	An reference voltage for the step-up circuit1. Connect to an external power supply of 2.75V of less when not using an internal reference voltage.
TESTO1,2	-	2	Open	Dummy pads. Disconnect them.
DUMMY 1-28	-	22	Open	Dummy pads. Disconnect them.
DUMMYR1-4	-	4	Open	Dummy pads. Disconnect them.

4. Interface

The FGD0801 supports system interface for setting instructions/data and RGB interface for data transferring during animated display. The FGD0801 can select the appropriate interface for the display (moving or still picture) in order to transfer data efficiently or improve the display quality. As external display interface, the FGD0801 supports RGB interface and VSYNC interface, which enables data rewrite operation without flicker when displaying the animated pictures on the panel.

4.1 System interface

The following kinds of system interface are available with the FGD0801 and the interface is selected by setting the IM3-0 pins. The system interface is used for instruction setting and RAM access. The FGD0801 supports three system interfaces:
an 80-System 18-/16-/9-/8-bit bus interface,
a 68-System 18-/16-/9-/8-bit bus interface and a serial data transfer bus interface.

The FGD0801 includes an index register (IR) storing index data of internal control register and RAM. There are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. The IR will be indexed to these two control registers through data bus by setting RS=1. When the data is written into the GRAM from the MPU, it is first written into the write data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

Operations	E_NWR	RW_NRD	RW	RS
Write Indexes into IR	0	1	0	0
Read Internal Status	1	0	1	0
Write Data into Control Register or GRAM	0	1	0	1
Read Control Register or GRAM data	1	0	1	1

Table 3 Register Selection (80/68 system:18-/16-/9-/8-bit System Interface)

Operations	R/W	RS
Write Indexes into IR	0	0
Read Internal Status	1	0
Write Data into Control Register or GRAM	0	1
Read Control Register or GRAM data	1	1

Table 4 Register Selection (Serial Data Transfer Interface)

4.1.1 80/68-System Interface

1) system 18-bit bus Interface

The 80-System 18-bit parallel data transfer can be used by setting IM3-0 pins to“1010”. And the 68-system 18-bit parallel data transfer can be used by setting IM3-0 pins to “1000”.The Figure 4 is the example of interface with i80/m68 Microcomputer and the Figure 5 is the data format of 18-bit system interface.

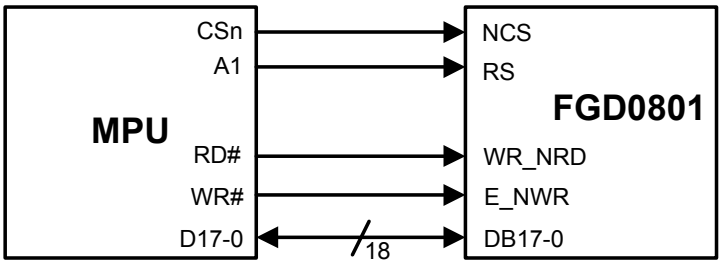


Figure 4 80/68-System 18-bit bus Interface

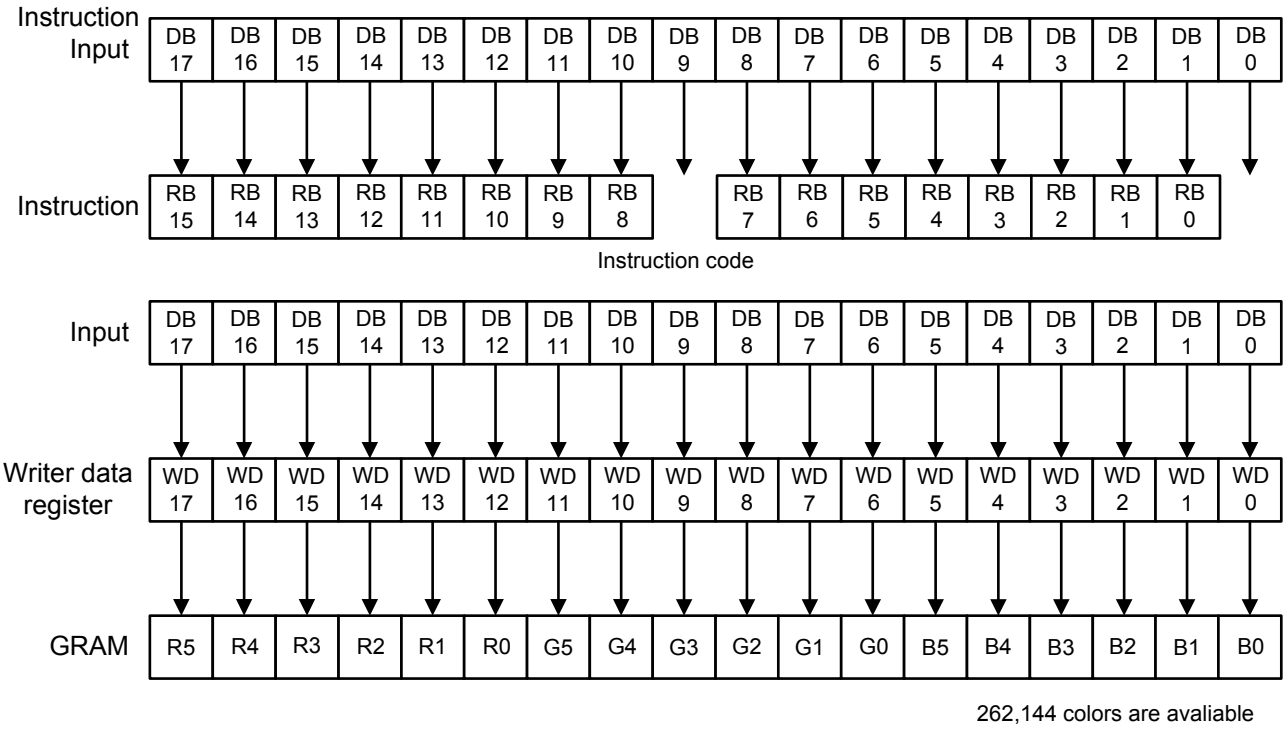


Figure 5 Instruction /GRAM Data Write (18-bit System Interface)

2) system 16-bit bus Interface

The 80-system 16-bit bus parallel data transfer can be used by setting IM3-0 pins to“0010”. And the 68-system 16-bit bus parallel data transfer can be used by setting IM3-0 pins to “0000”.The data written to GRAM is expanded to 18-bit bus data automatically in the LSI. Unused pins (DB9, DB0) must be fixed to the IOVCC or VSSD level.

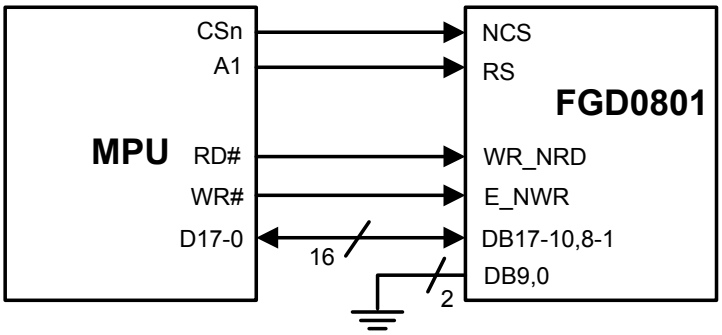


Figure 6 80/68-System 16-bit Bus Interface

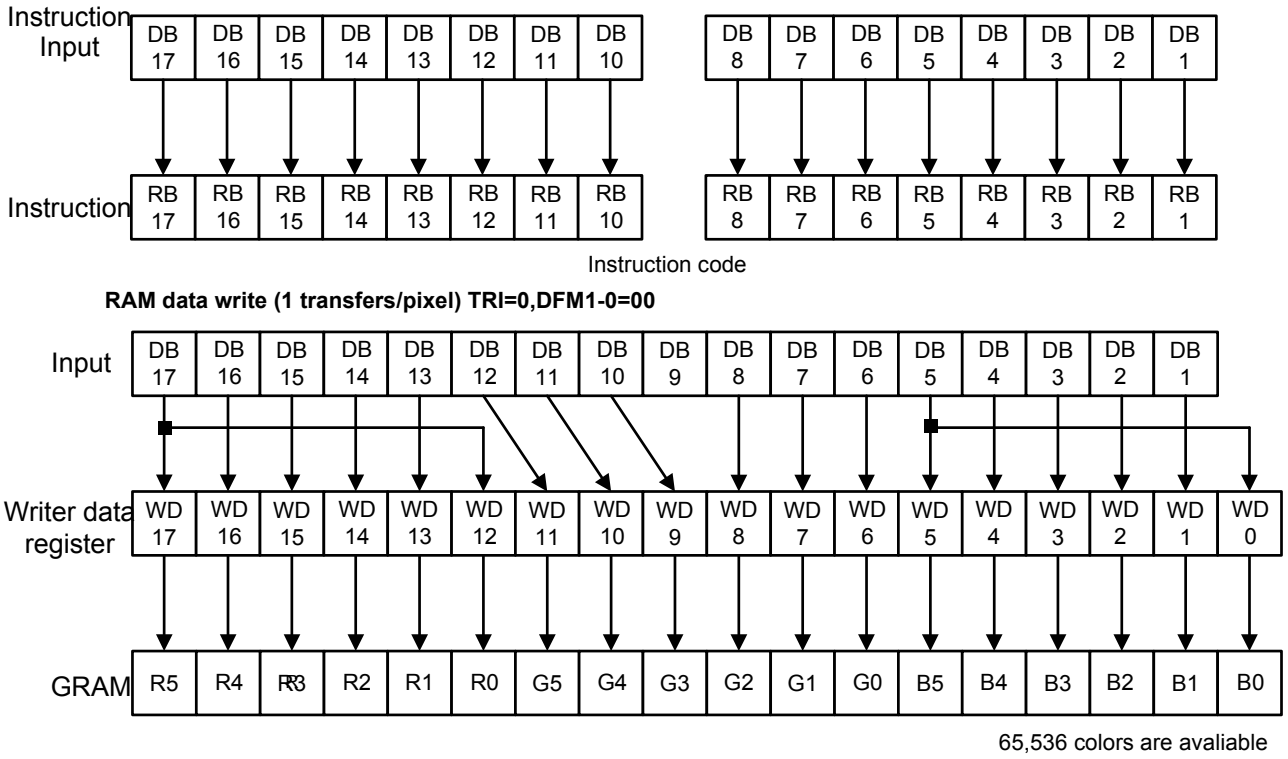


Figure 7 Instruction /GRAM Data Write (16-bit System Interface)

3) system 9-bit bus Interface

The 80-system 9-bit bus parallel data transfer can be used by setting IM3-0 pins to“1011”. And the 68-system 9-bit bus parallel data transfer can be used by setting IM3-0 pins to “1001”.In 80/68-system 9-bit bus parallel data transfer mode, the 16-bit bus instruction and GRAM write data are divided into lower and upper nine bits, and then the upper nine bits are transferred first. Unused pins (DB8-0) must be fixed to the IOVCC or VSSD level.

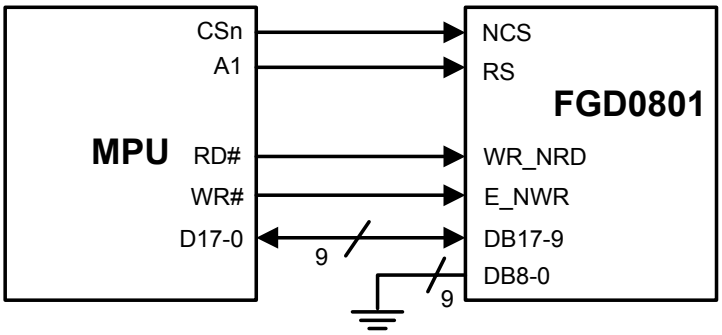
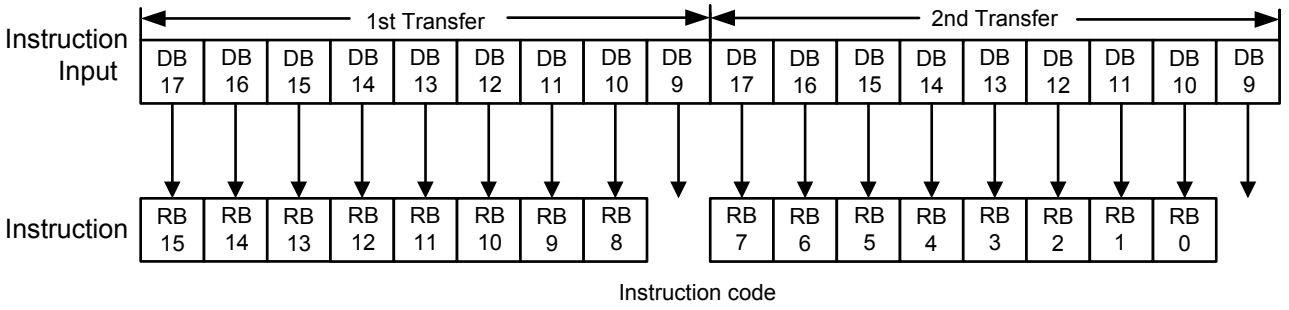


Figure 8 80/68-System 9-bit Bus Interface



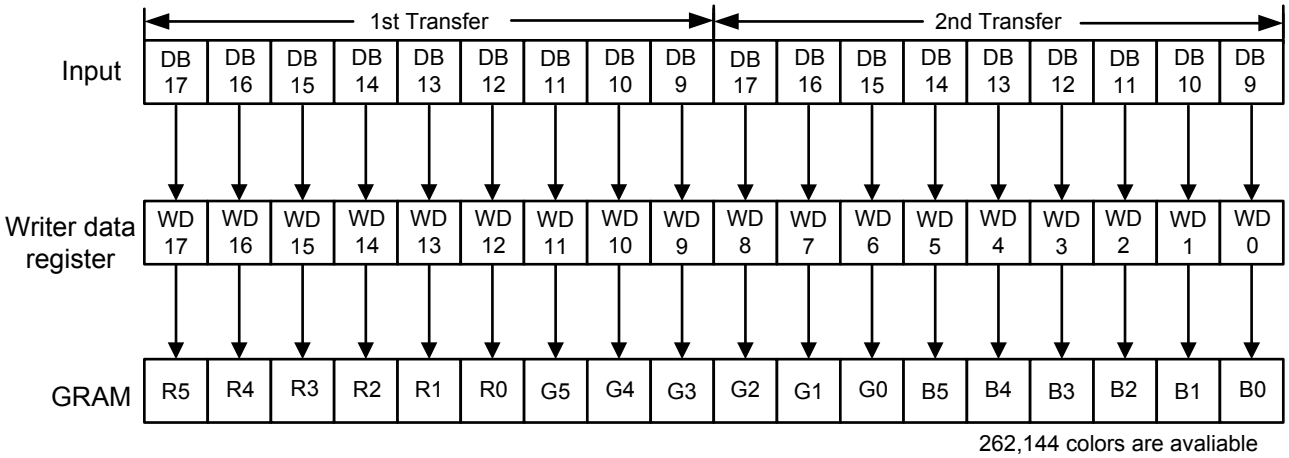


Figure 9 Instruction /GRAM Data Write (9-bit System Interface)

4) system 8-bit bus Interface

The 80-system 8-bit bus parallel data transfer can be used by setting IM3-0 pins to“0011”. And the 68-system 8-bit bus parallel data transfer can be used by setting IM3-0 pins to “0001”.The data format is same as 9-bit interface, Unused pins (DB9-0) must be fixed to the IOVCC or VSSD level.

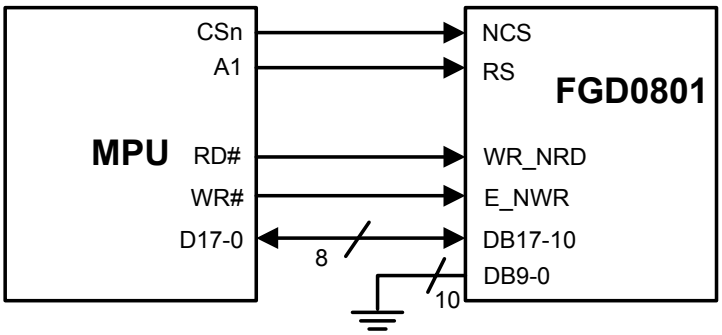


Figure 10 80/68-System 8-bit Bus Interface

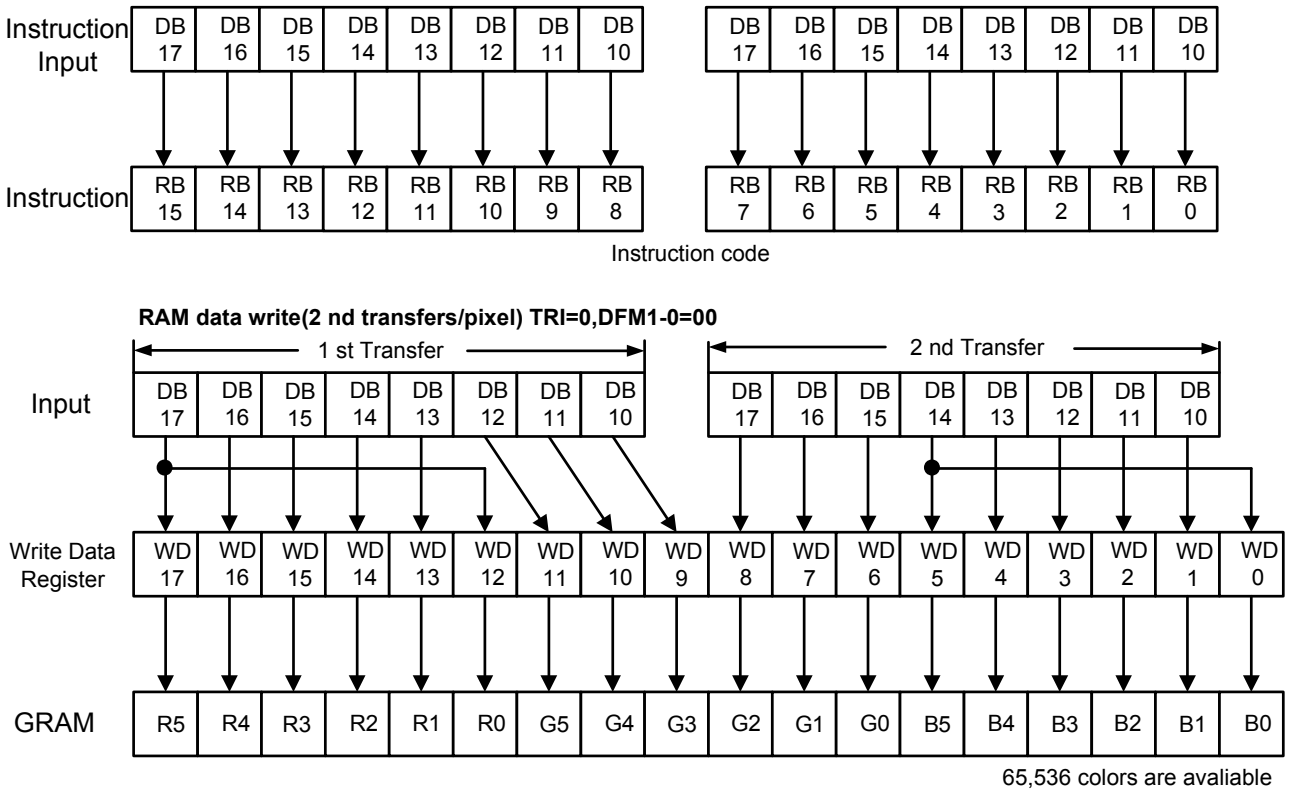
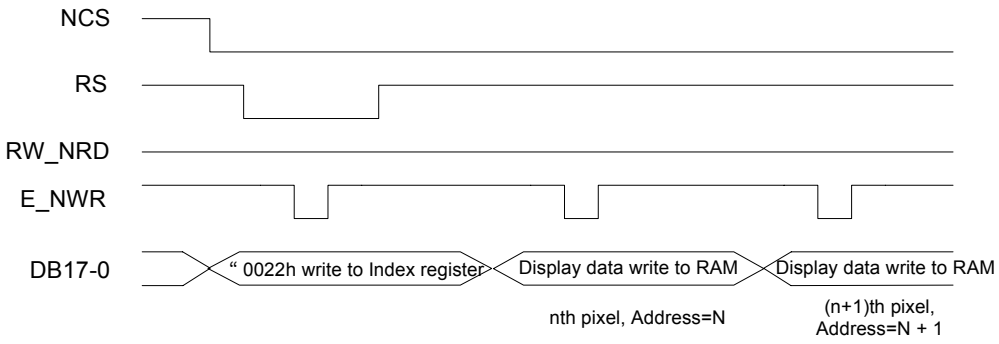
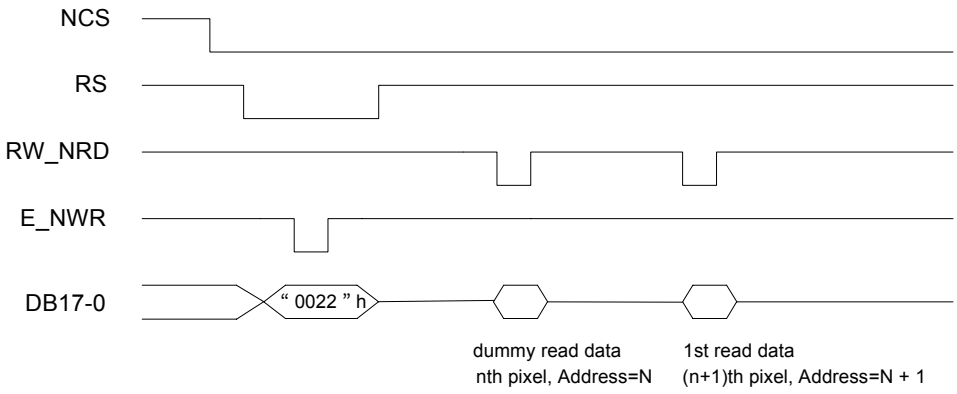


Figure 11 Instruction /GRAM Data Write (8-bit System Interface)

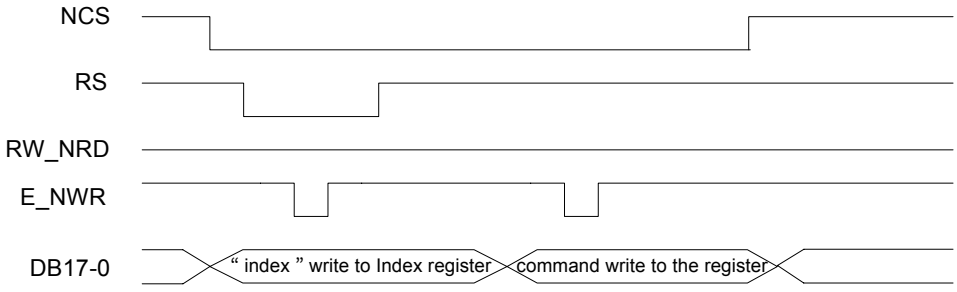
Write to the Graphic RAM



Read the Graphic RAM



Write to the Register



Read the Register

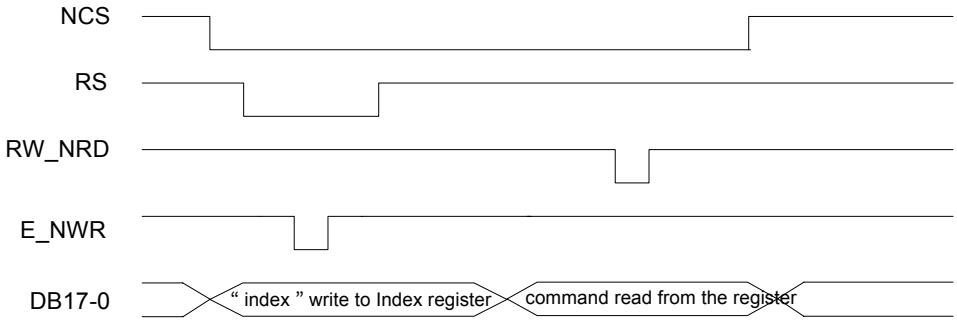
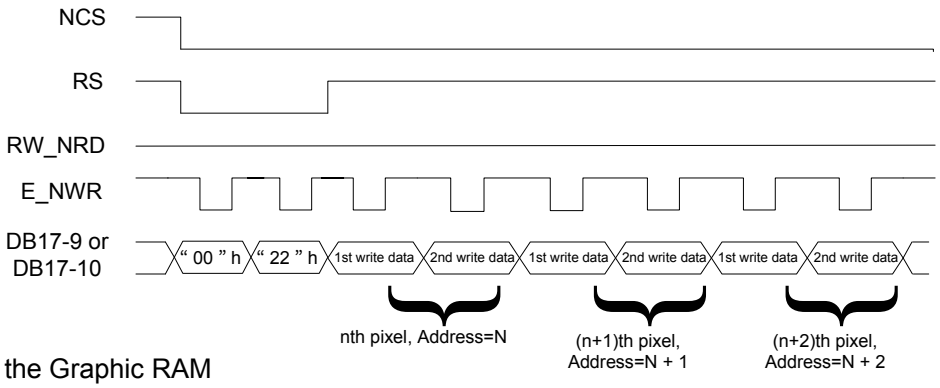
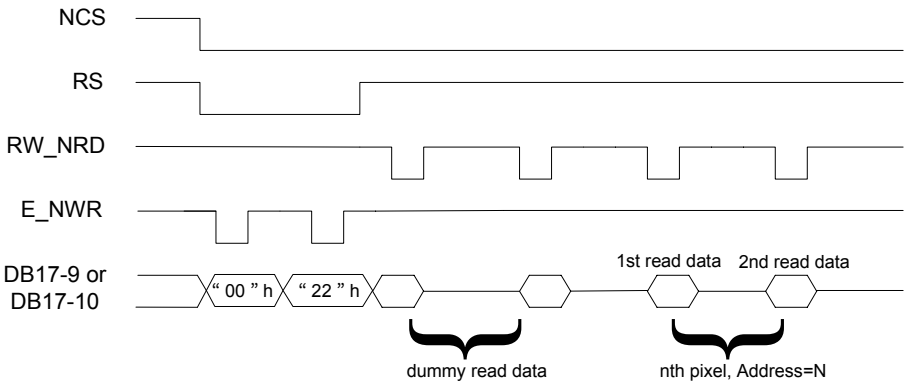


Figure 12 18 /16-bit System Interface Timing (for i80 series MPU)

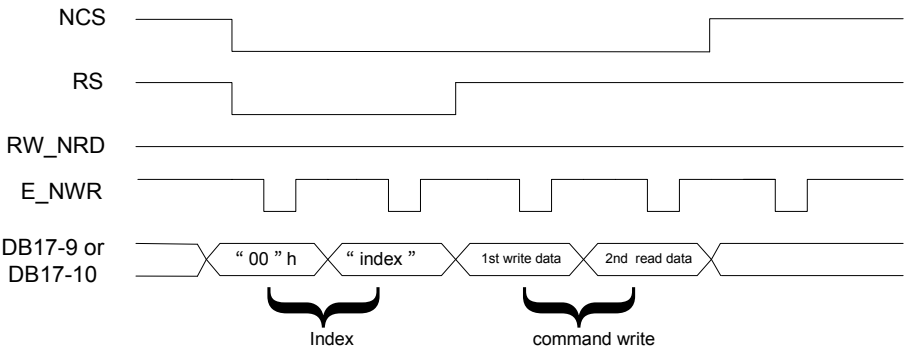
Write to the Graphic RAM



Read the Graphic RAM



Write to the Register



Read the Register

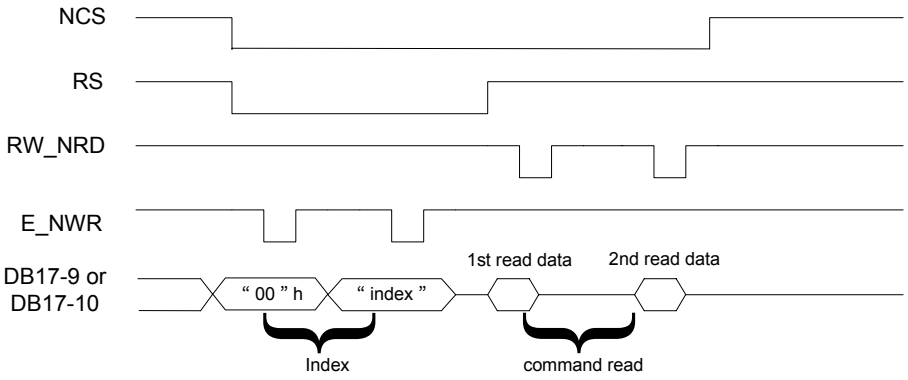
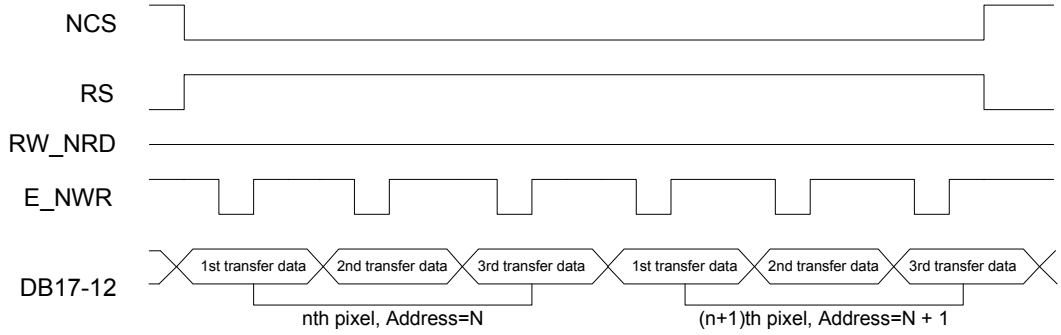
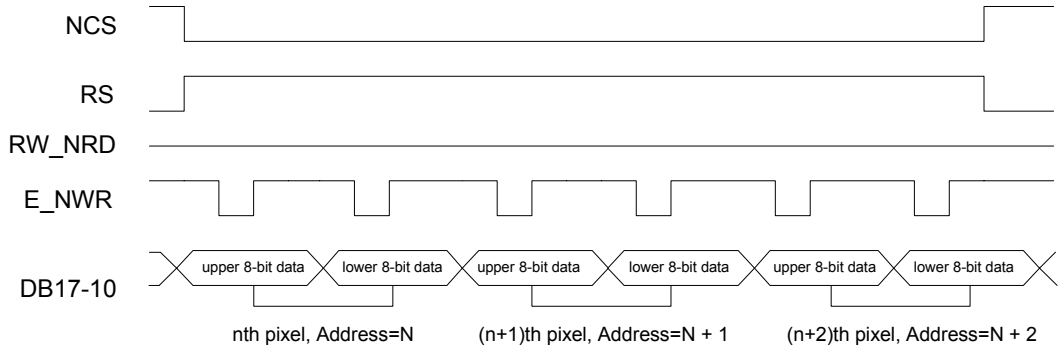


Figure 13 9/8-bit System Interface Timing (for i80 series MPU)

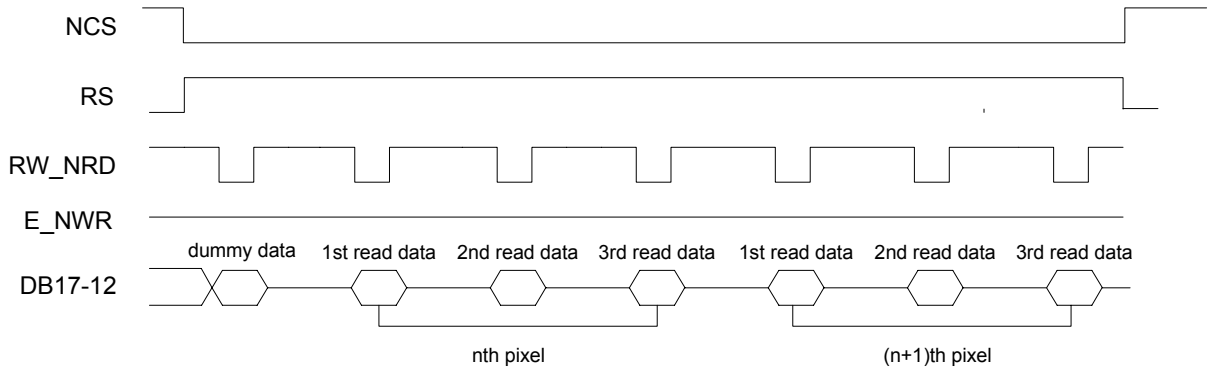
Write to the display data RAM



Write to the display data RAM



Read the display data RAM



Read the display data RAM

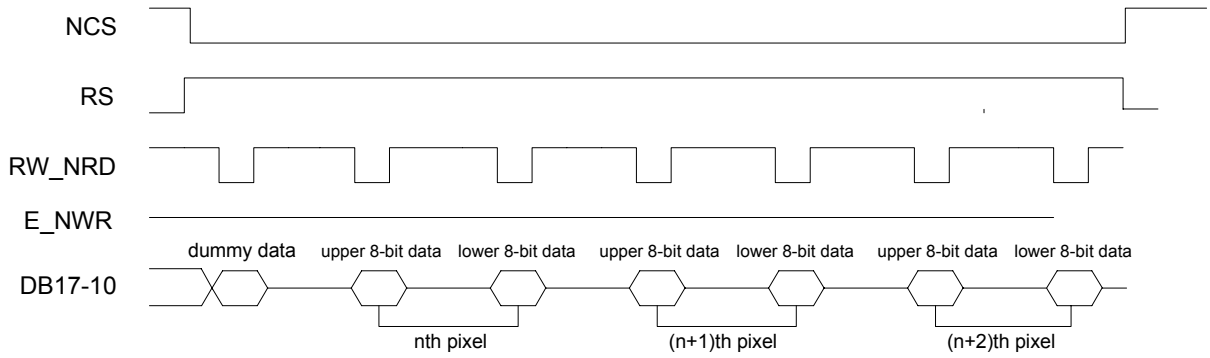
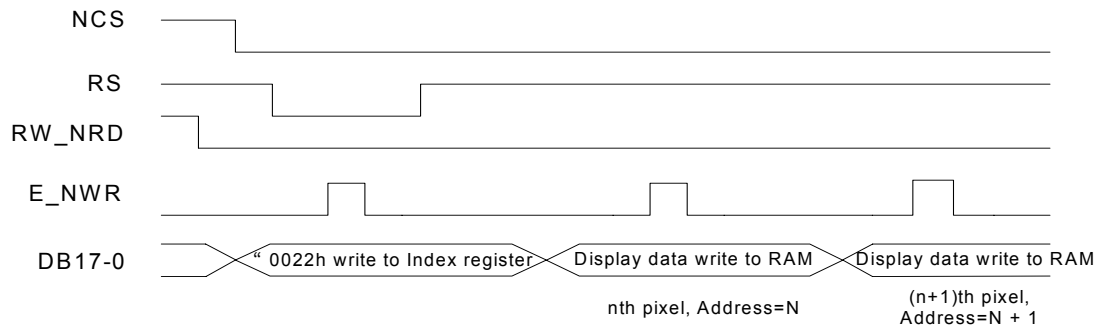
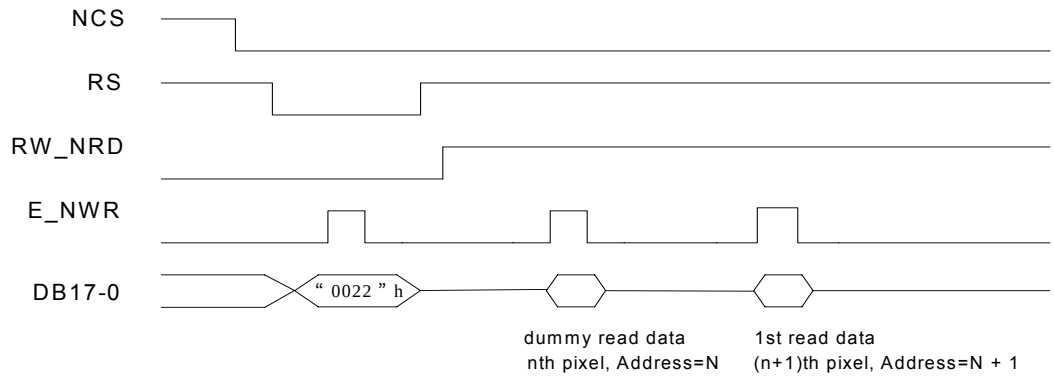


Figure 14 8-bit System Interface Timing (for i80 series MPU)

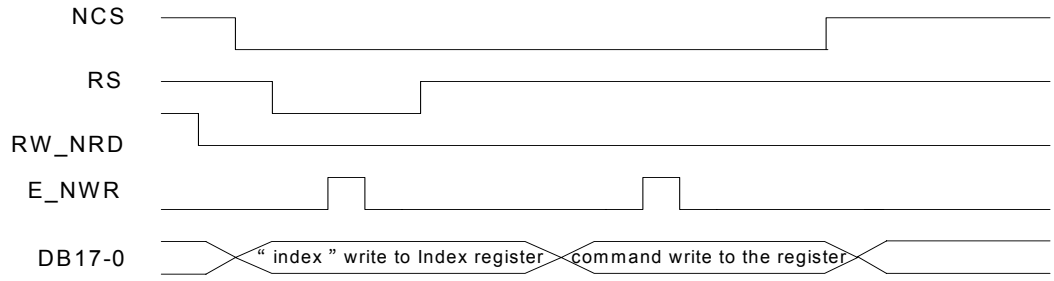
Write to the Graphic RAM



Read the Graphic RAM



Write to the Register



Read the Register

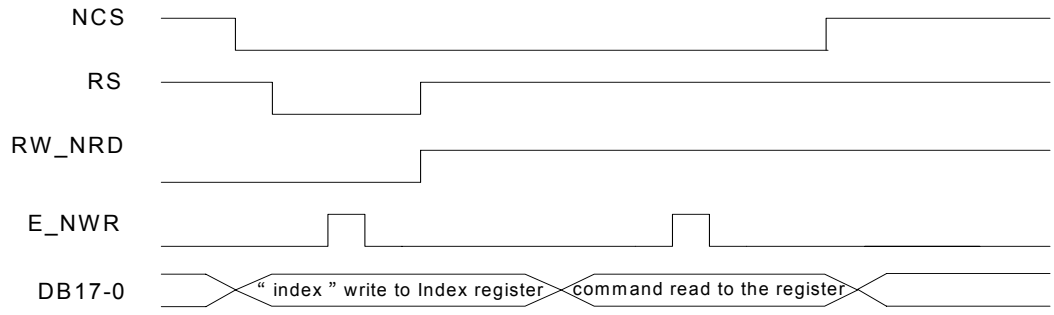
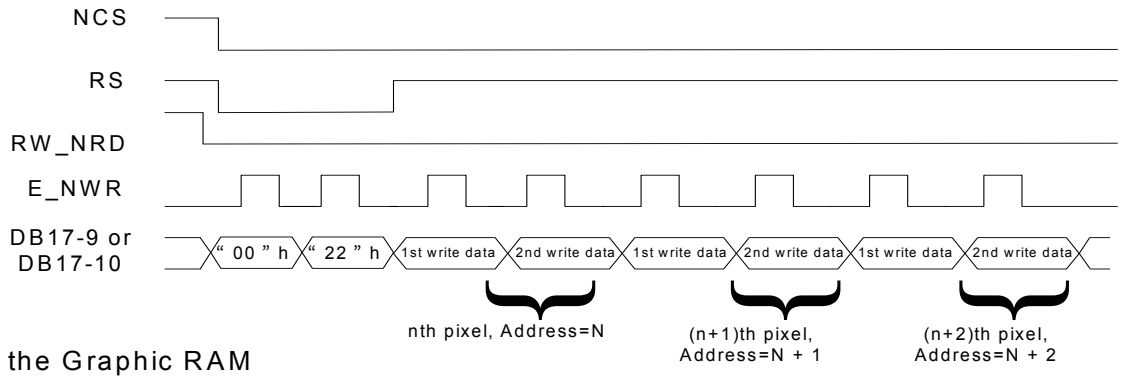
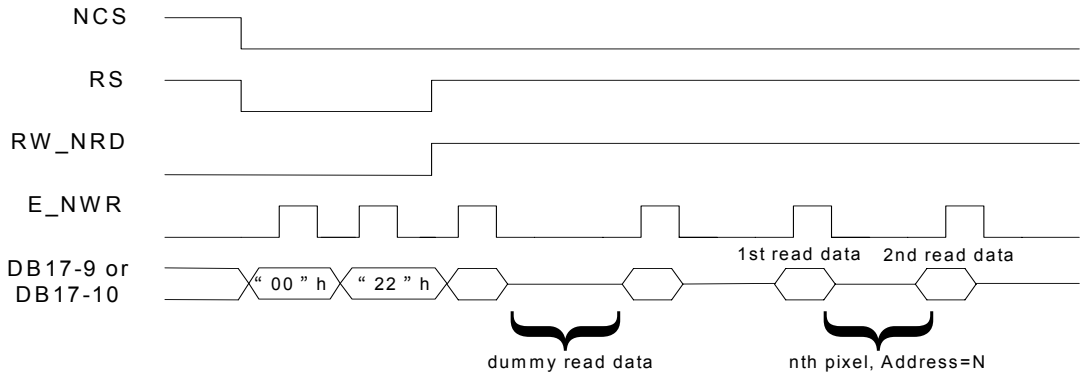


Figure 15 18 /16-bit System Interface Timing (for m68 series MPU)

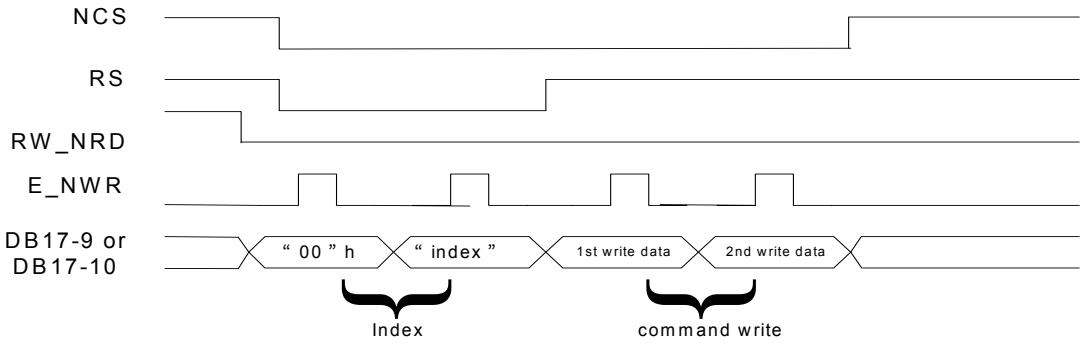
Write to the Graphic RAM



Read the Graphic RAM



Write to the Register



Read the Register

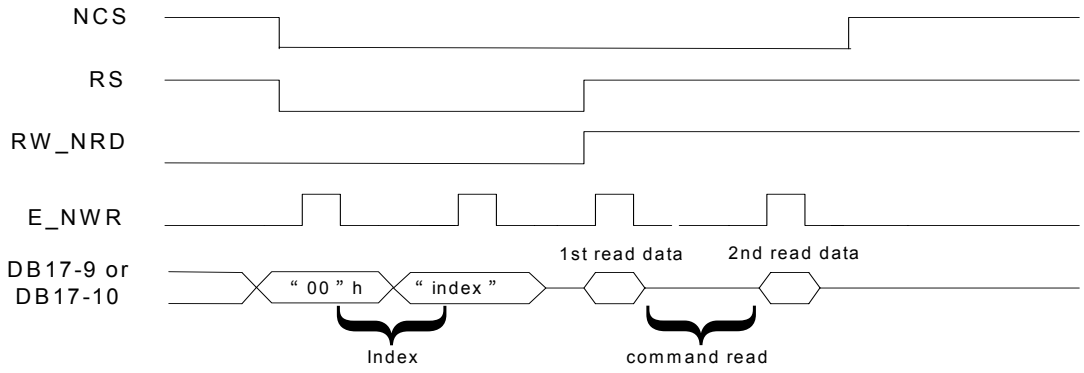
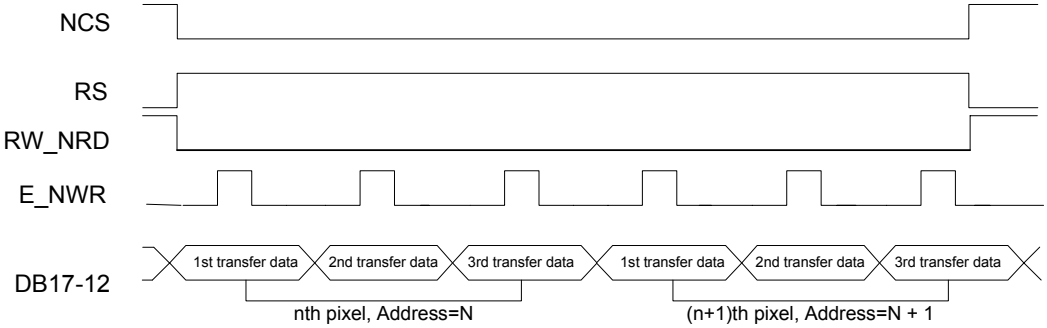
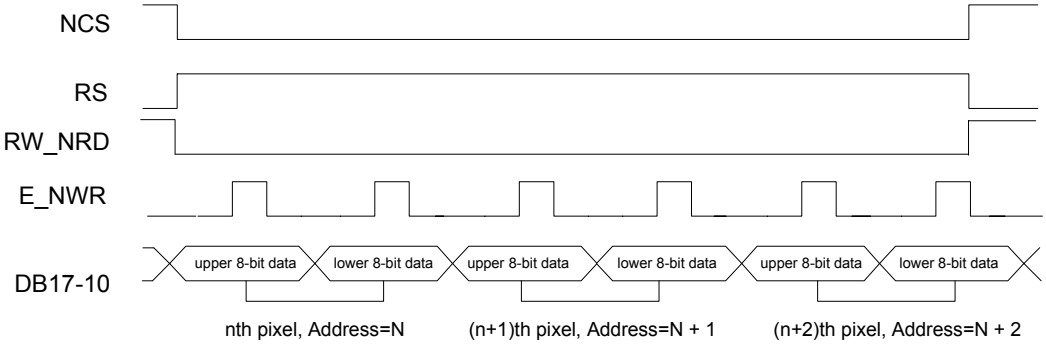


Figure 16 9/8-bit System Interface Timing (for m68 series MPU)

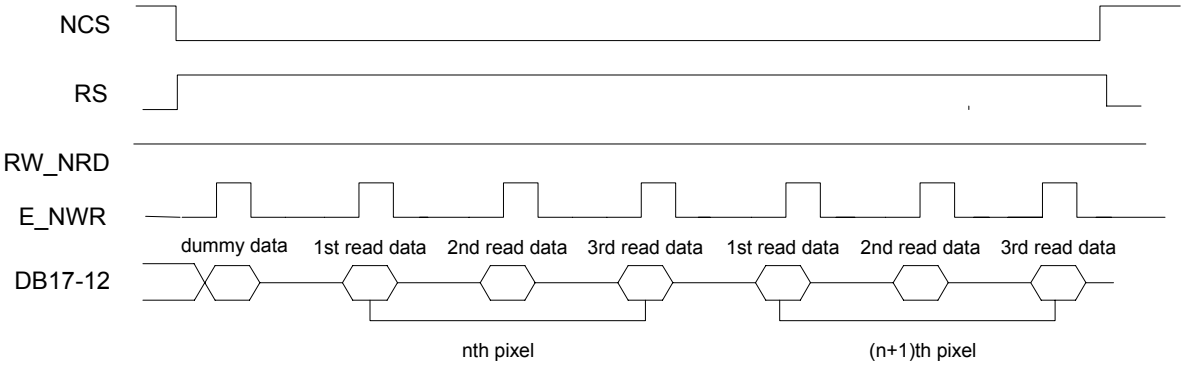
Write to the display data RAM



Write to the display data RAM



Read the display data RAM



Read the display data RAM

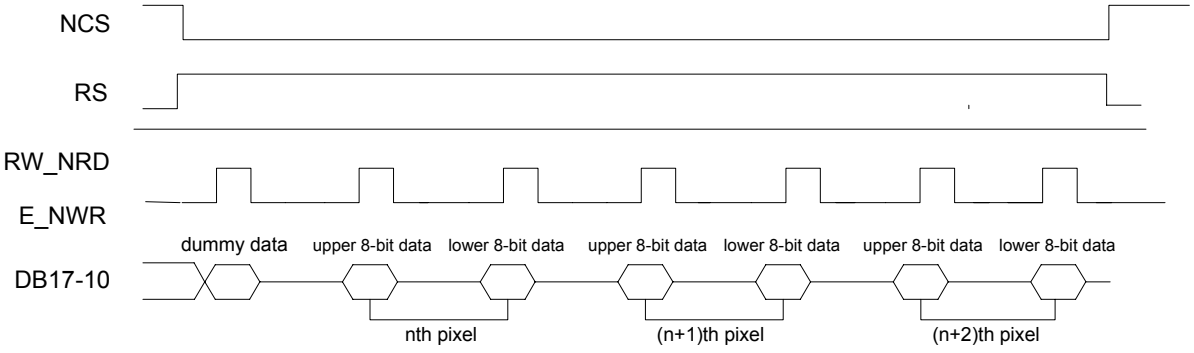


Figure 17 8-bit System Interface Timing (for m68 series MPU)

4.1.2 Serial Data Transfer Interface

The FGD0801 supports the serial data transfer interface by setting IM3-1 pins to“010”. The data is transferred via chip select line (NCS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB 17-0 pins, not used in this mode, must be fixed to either IOVCC or VSSD level.

The FGD0801 recognizes the start of data transfer on the falling edge of NCS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of NCS input. The FGD0801 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the FGD0801 are compared and both 6-bit data match. Then, the FGD0801 starts taking in subsequent data. The least significant bit of the device identification code is determined by setting the ID pin. Send "01110” to the five upper bits of the device identification code. Two different chip addresses must be assigned to the FGD0801 because the seventh bit of the start byte is register select bit (RS). When RS = 0, either index register write or status read operation is executed. When RS = 1, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The FGD0801 receives data when the R/W = 0, and transfers data when the R/W = 1.

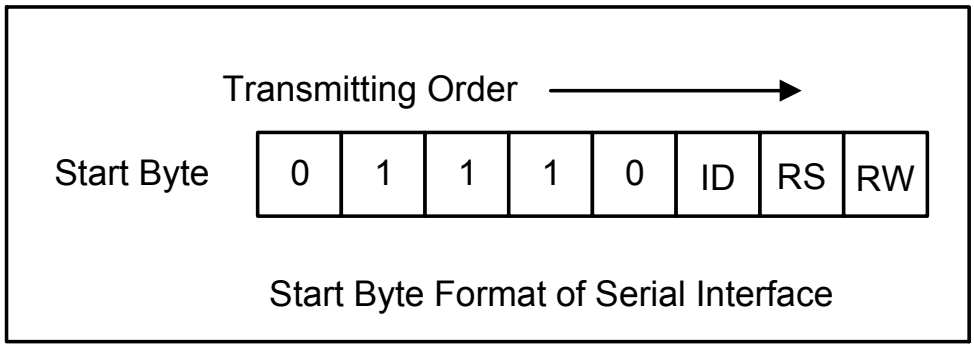


Figure 18 Start Byte Format of Serial Interface

When the serial data transfer interface is enabled, the FGD0801 starts taking in start byte and subsequent data that is transferred with the MSB first. Further, the registers of 16-bit bus format can be dividing to the upper eight bits as the first byte and lower eight bits as second byte when FGD0801 are executed from the MSB after transferring two bytes. The FGD0801 executed the write data operation to the GRAM after two-byte and then automatically expanded to the 18-bit bus format . When the read status/register operation is executed, the prior byte after start byte is invalid, and then the FGD0801 starts to read correct status/register data from second byte. As well as, when the read GRAM data operation, the prior five bytes of GRAM read data after the start byte are invalid. The FGD0801 starts to read correct GRAM data from the sixth byte.

RS	R/W	Function
0	0	Index Register Set
0	1	Status Read
1	0	Register or GRAM Data Write
1	1	Register or GRAM Data Read

Table 5 RS and R/W set for serial interface

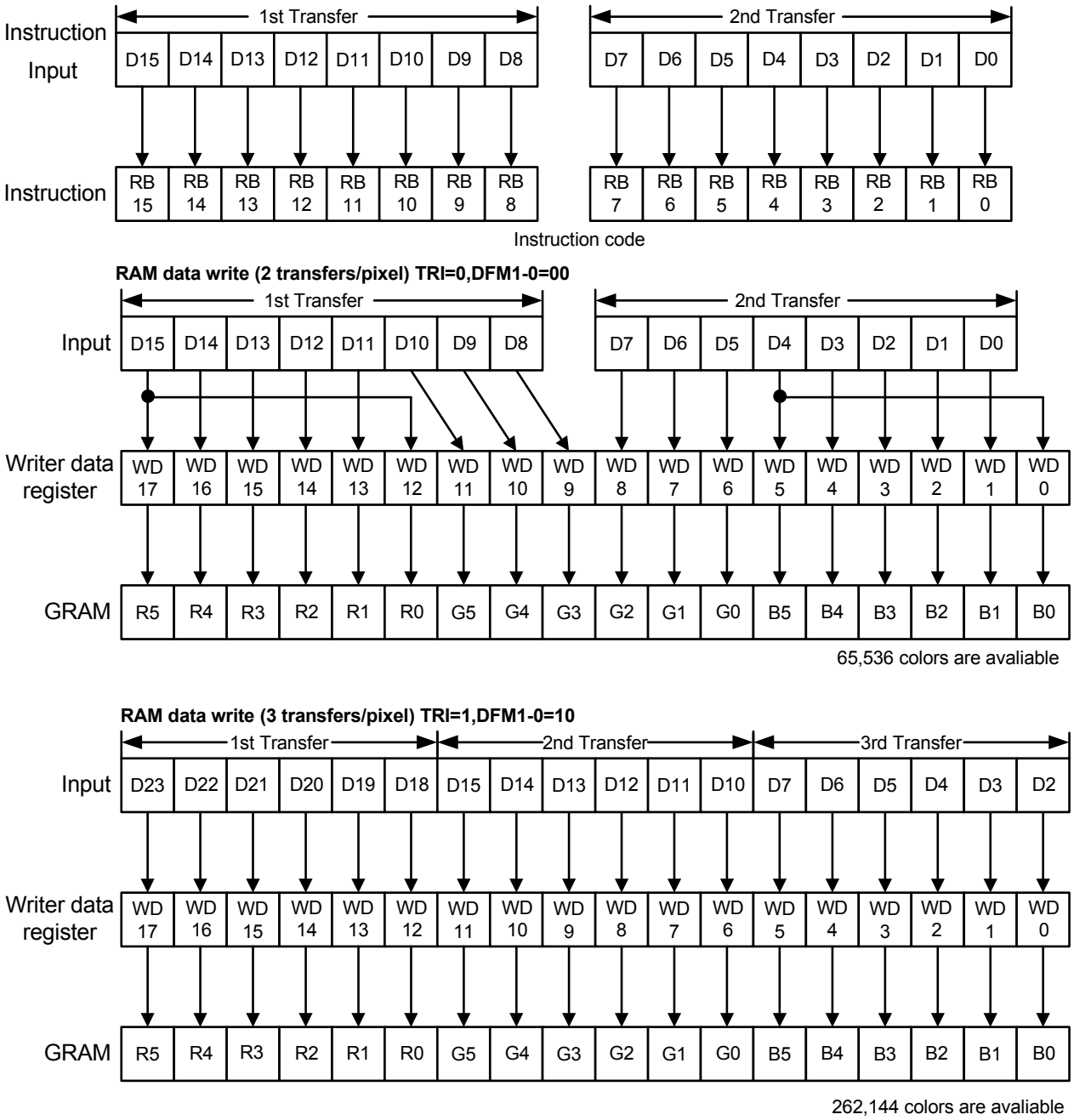
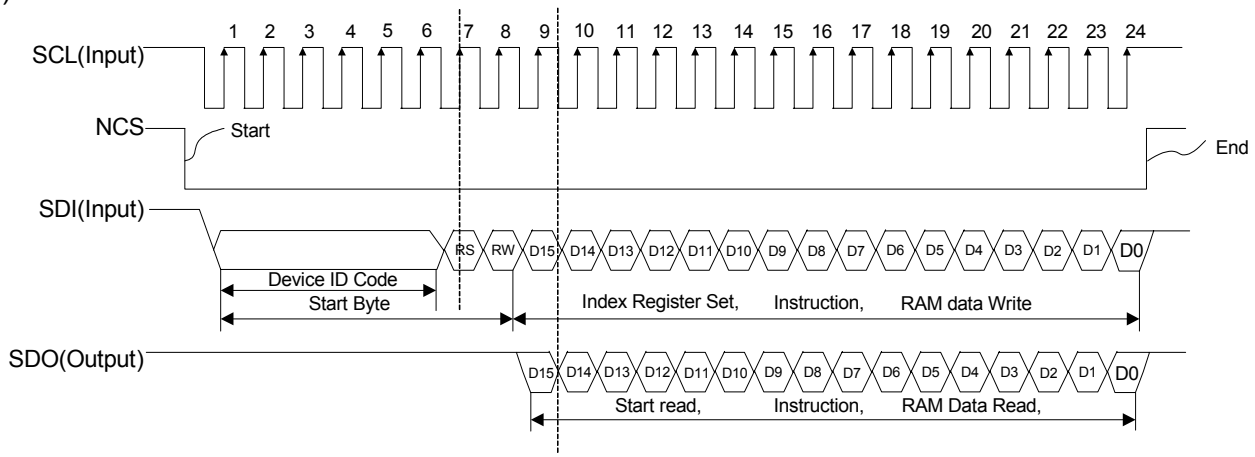
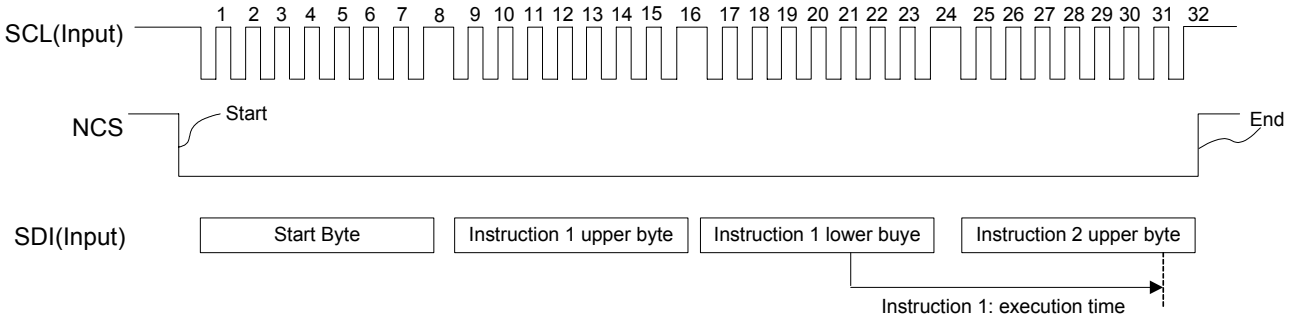


Figure 19 Instruction /RAM Data Write (Serial interface)

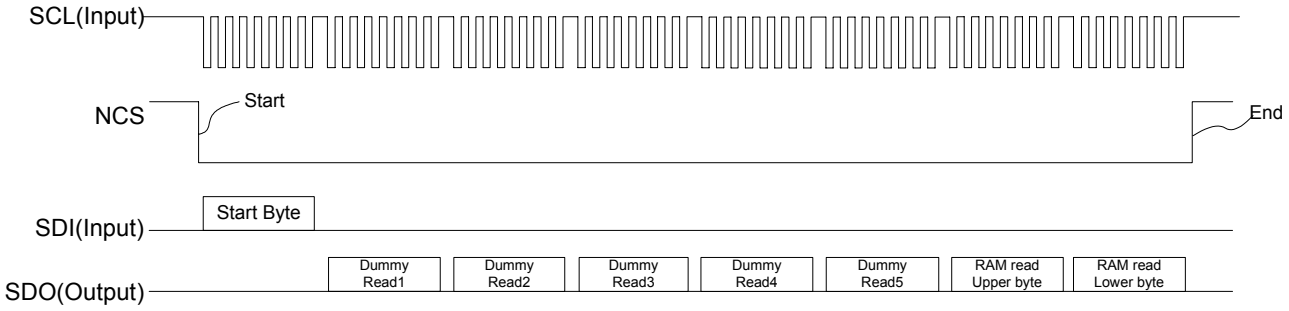
1) Basic data transfer via Serial interface



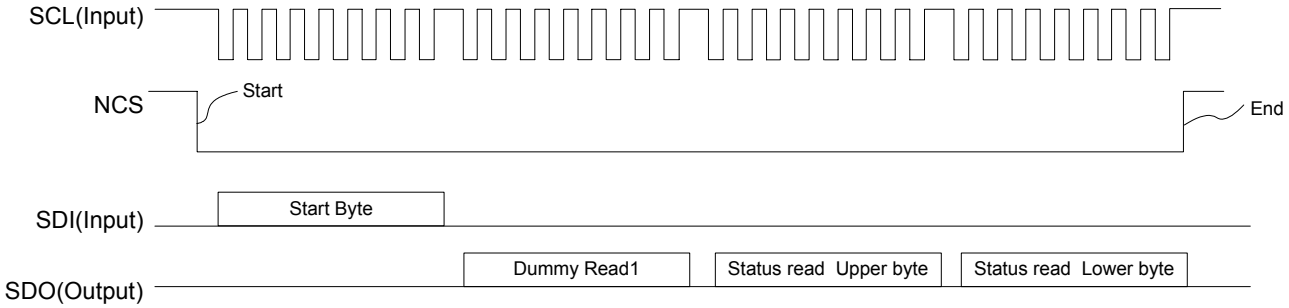
2) Consecutive data transfer via Serial interface



3) RAM data read transfer



4) Status Read/ Instruction Read



Note: One byte of the read data after the start byte is invalid. The FGD0801 starts to read the correct status or instruction data from the second byte

Figure 20 Serial Interface Data Transfer Timing

4.2 VSYNC Interface

The FGD0801 supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation. When the VSYNC interface mode is selected, the interface displays a moving picture through system interface with minimum modification that rewrites display data to the internal GRAM. The VSYNC interface can be used by setting DM1-0=10 and RM=0.

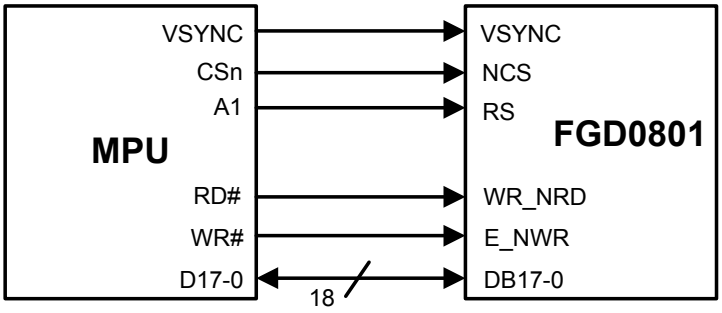


Figure 21 VSYNC Interface to MPU

DM1	DM0	Operation Mode
0	0	System Interface
0	1	RGB Interface
1	0	VSYNC Interface
1	1	Ignore

Table 6 DM1-0 Set

The VSYNC interface has some constraints in the internal clock and the RAM write speed via the system interface. It requires GRAM write speed more than the minimum value that system processed and calculated. The internal clock of VSYNC interfaces can be computed by the following formula that used some parameters with FP, BP and display lines duration (NL):

Internal oscillator clock (f_{osc})[Hz] = Frame Frequency × [NL + FP + BP] × RTN ×frequency fluctuation

The parameter of frequency fluctuation is ascribed to the external resistor or voltage variation, fabrication process condition, external temperature and humidity condition etc. The minimum speed for RAM can be computed by the following formula:

$$\textit{The Min. RAM Write Speed [Hz]} \geq \frac{128 \times \mathrm{NL} \times \mathrm{fosc}}{[\mathrm{BP} + \mathrm{NL} - \mathrm{Margin\ Line}] \times \mathrm{RTN}}$$

The margin line means when operate in VSYNC interface mode, it must be remained the several lines in advance for protection between the actual line of the display operation and the line address for the RAM write data operation. The calculated value is the theoretical value that the FGD0801 starts the RAM write operation must be taken into account. In other words, the actual value of RAM write speed must be more than theoretical value that calculated from forward formula by getting a internal oscillator clock (f_{osc}) first. An example of internal oscillator clock (f_{osc}) and minimum speed for RAM writing set up in VSYNC interface mode is as following.

Example
Display size: 128RGB x 160 lines
Lines of be used: 160 lines (10011)
FP: 2 lines (0010)
BP: 14 lines (1110)
Frequency fluctuation: 5%

Frame frequency: 60Hz
Internal oscillator clock (f_{osc}) [Hz] = 60 × [160 + 2 +14] × 16 × (1.05/0.95) ≈ 187 kHz
The Min. RAM Write Speed [Hz] ≧128 × 160 × 187k /{ [14 + 160 -2] × 16} ≈ 1.39MHz

In this example, the minimum RAM write speed of VSYNC interface is 1.39MHz and then necessary to setting enough or more on the falling edge of guarantees the completion write operation before the FGD0801 initiate the display operation and make it possible to rewrite the display area set previously. Further, if the display area were different with the anterior example, the calculated result and margin setting would be revised. For example, if the display area is smaller than that, an extra will be created between the RAM write operation and display with regard to each line.
When the FGD0801 make the transition with system interface mode and VSYNC interface mode, the difference between that is the used of signal VSYNC for synchronization. Therefore, both of them are used the internal oscillator to generate the reference clock. The Figure 22 illustrates the process of VSYNC interface with internal clock and system interface with internal clock mode transition, which is shown by setting register set.

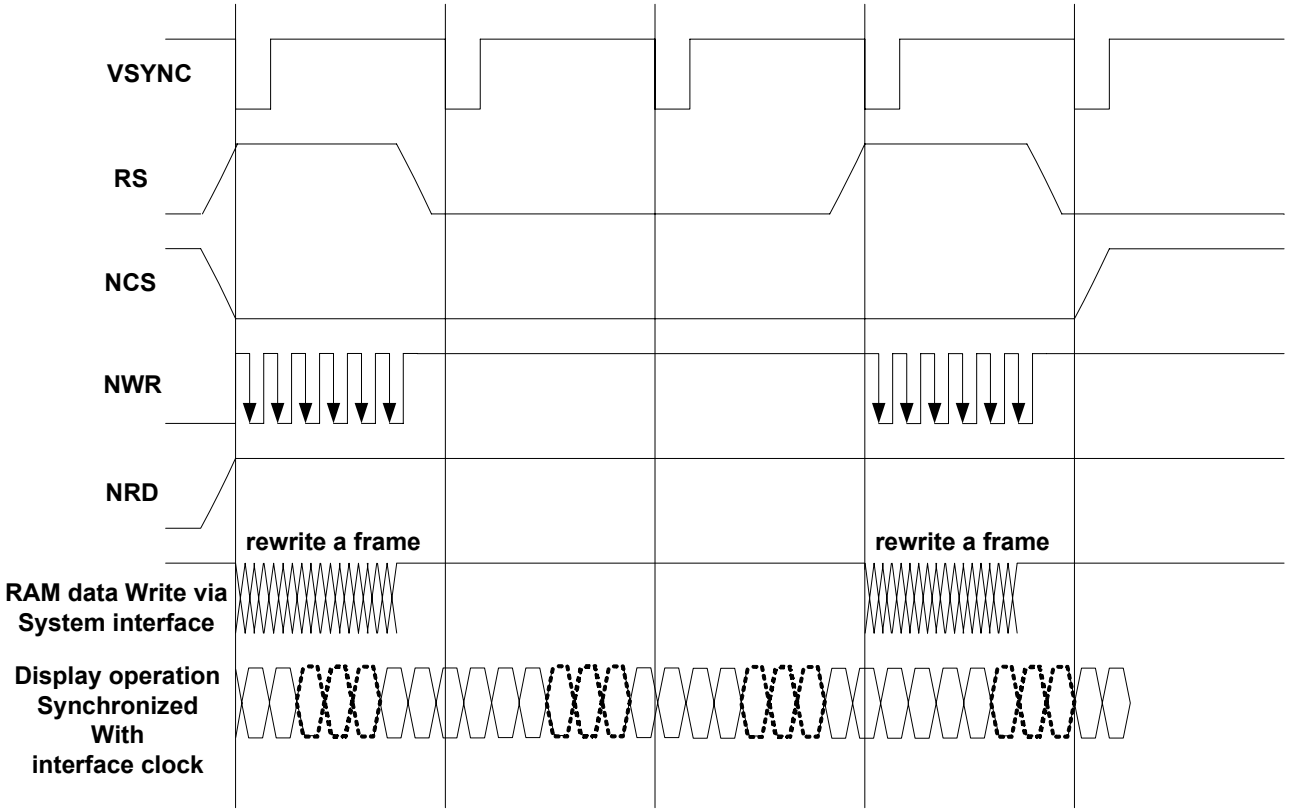


Figure 22 Moving picture data transfer via VSYNC interface

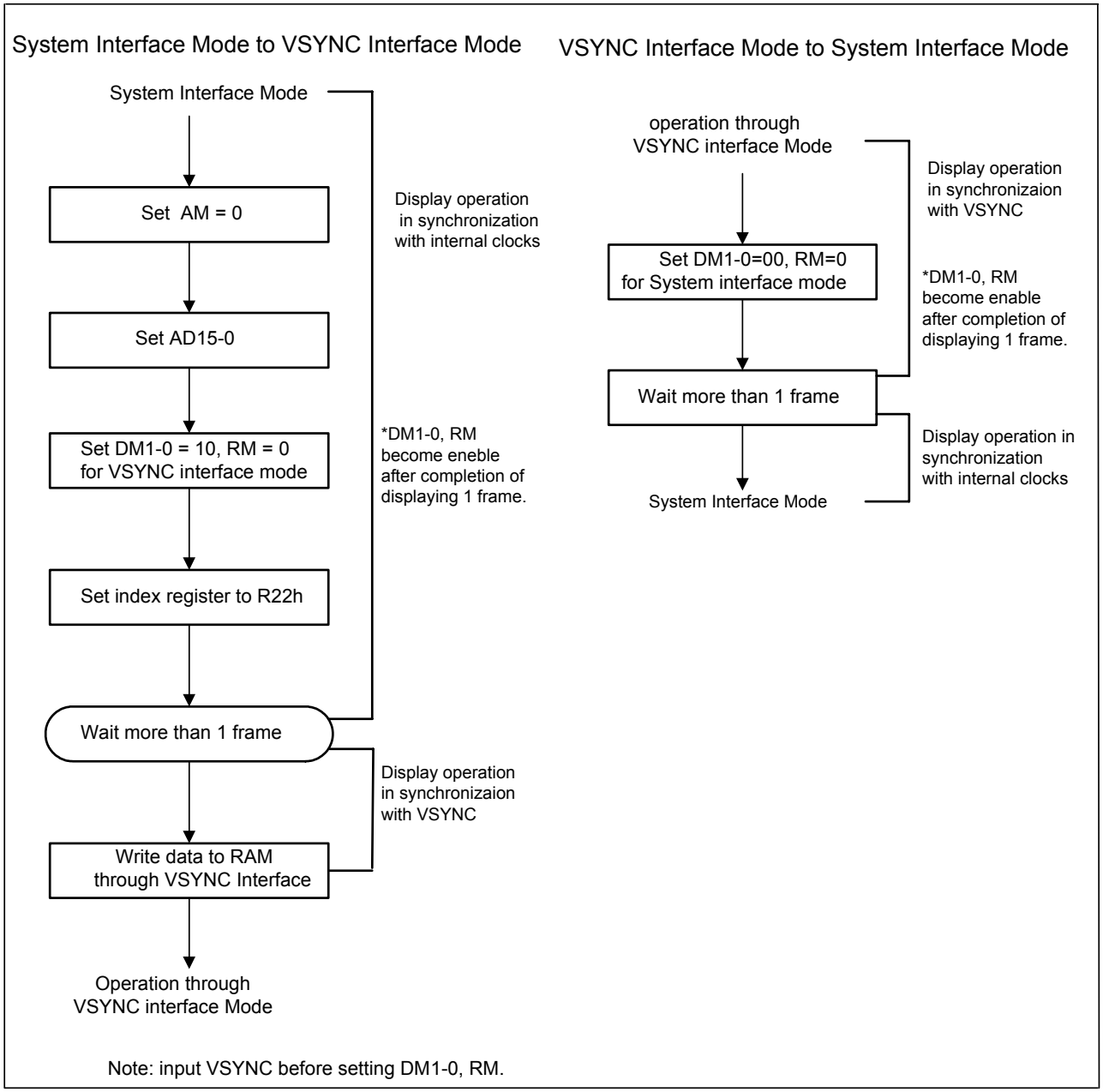


Figure 23 Exchange of VSYNC Interface and System Interface Mode

When FGD0801 is set up on VSYNC interface mode, the partial display function, vertical scroll function and interlaced scan function are invalid function in VSYNC interface mode.

4.3 RGB Interface

The FGD0801 supports RGB interface for moving picture display and incorporates RAM for storing display data, which provides the following advantages in displaying a moving picture.

1) The window address function enables transferring data only within the moving picture area.

2) It becomes possible to transfer only the data written over the moving picture area.

3) By reducing data transfer, it can contribute to lowering the power consumption of the whole system.

4) The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface.

The RGB interface executes in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via DB17-0 bits and according to the signal of data enable (ENABLE) be described on Table 7. The RGB interface can be used by setting DM1-0=01 and RM=1. In RGB interface mode, with use of a window address function, enables to display data in a moving picture area and makes it possible to transfer the display only by rewriting a screen with minimum data transfers.

EPL	ENABLE	RAM Write	RAM Address
0	0	Enable	Update
0	1	Disable	Keep
1	0	Disable	Keep
1	1	Enable	Update

Table 7 EPL and ENABLE Set

When the FGD0801 set up in RGB interface mode, a BP starts on the falling edge of VSYNC signal, which is made at the beginning by the display operation. Furthermore, the display duration (NL4-0) mean the numbers of driving lines is the subsequent data of display operation. And then the FP starts. The FP period would be continued until the next input of the VSYNC signal.

The FGD0801 supports two types of RGB interface mode, the difference between them is the RAM access using the RGB interface (DB17-0) or system interface (DB17-0). The data written to the internal GRAM are synchronized with DOTCLK inputs when ENABLE is setting low. Contrary to set ENABLE high, the data written to the GRAM would be entered to the process of using the system interface. Further, when select to use system interface, set ENABLE high to stop using the RGB interface for writing data, and then set the RAM access setting bit bus (RM) low to invert RAM access operation by using system interface. After that, set address AD15-0 on falling edge of VSYNC and then set the index field of register (R22h) to access RAM via the system interface. The FGD0801 allows rewriting data in the still picture area by using the system interface when displaying a moving picture in RGB interface mode. When return to use RGB interface to access RAM, set address AD15-0, RAM access setting bit bus (RM=1) and the index field of register (R22h) before accessing RAM via RGB interface.
The Figure24 is shown the process of RAM access via the system interface with rewriting still picture and then return to RGB interface while displaying a moving picture in RGB interface mode.

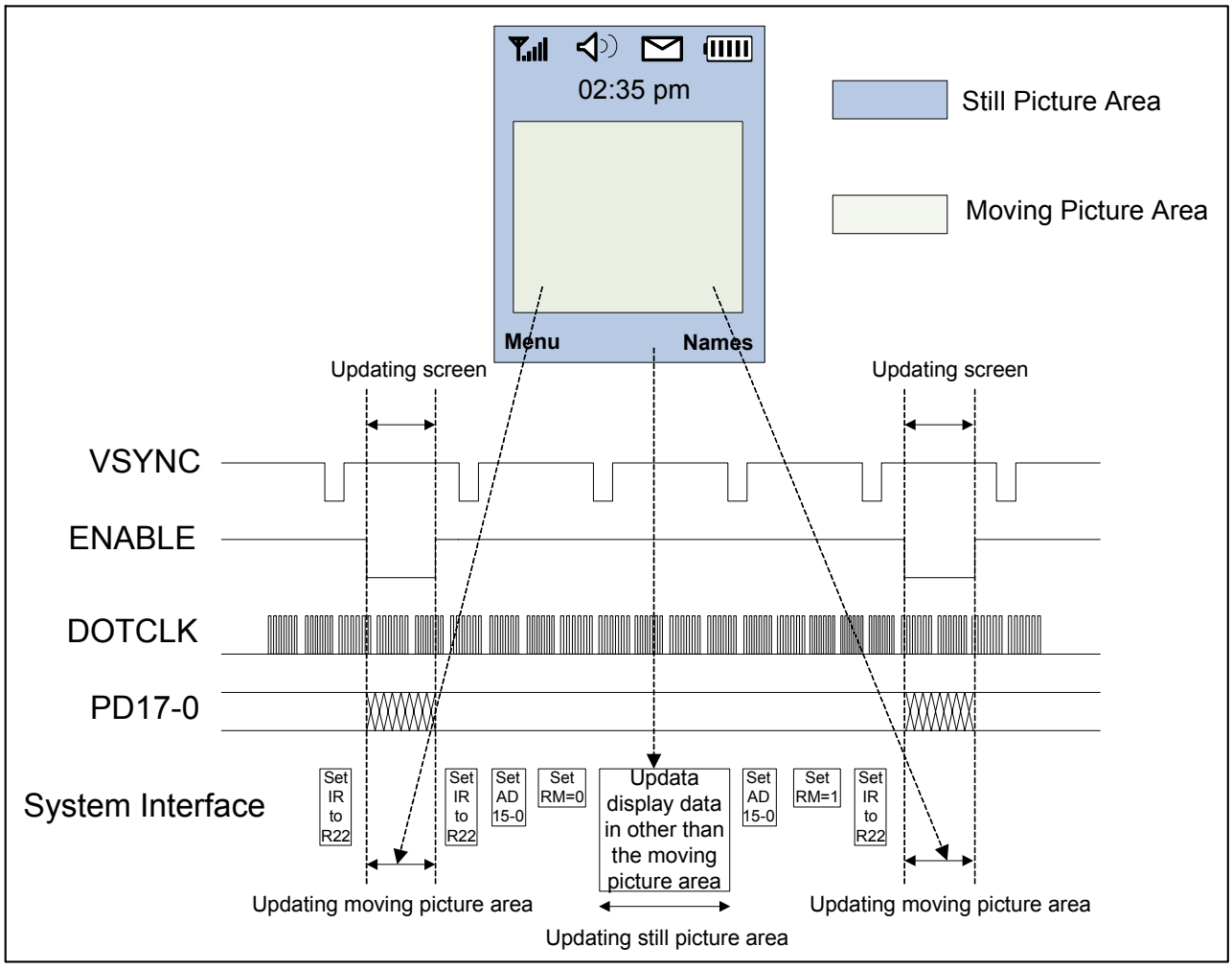


Figure 24 Update Still and Moving Picture

When set up in RGB interface mode, GRAM address (AD15-0) is set in the address counter for every frame on the falling edge of VSYNC. Furthermore, the FP period would be continues until the next input of the VSYNC signal. Such as VSYNC interface mode, partial screen display function, vertical scroll function and interlaced scan function are invalid function in VSYNC interface mode.

When the FGD0801 make the transition with system interface mode and RGB interface mode, the sequence of switching process must be following as Figure 25.

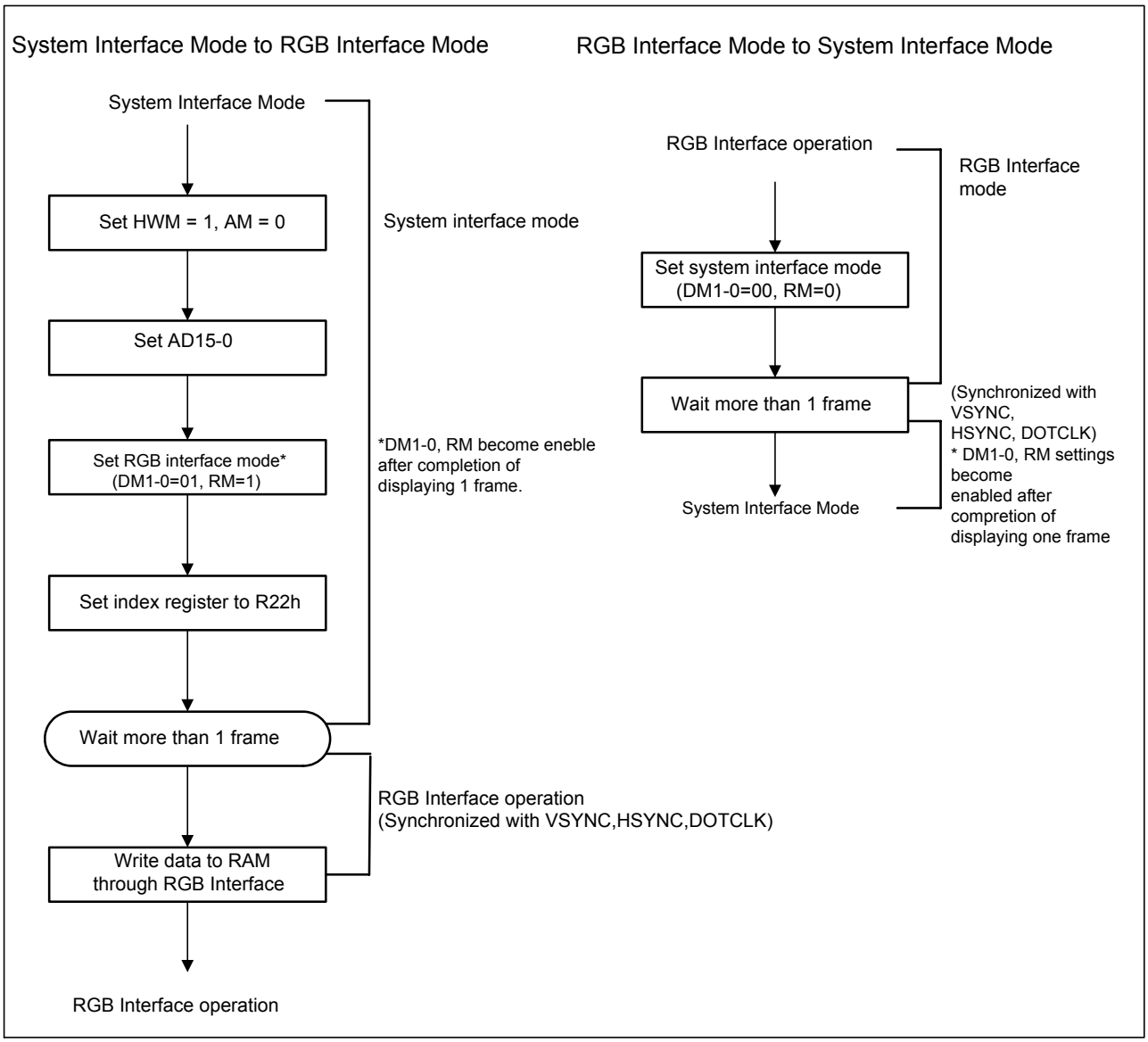


Figure 25 Transition between System Interface Mode and RGB Interface Mode

When operate in RGB interface and the RAM write data transfer through system interface, the sequence of switching process must be follow as Figure 26.

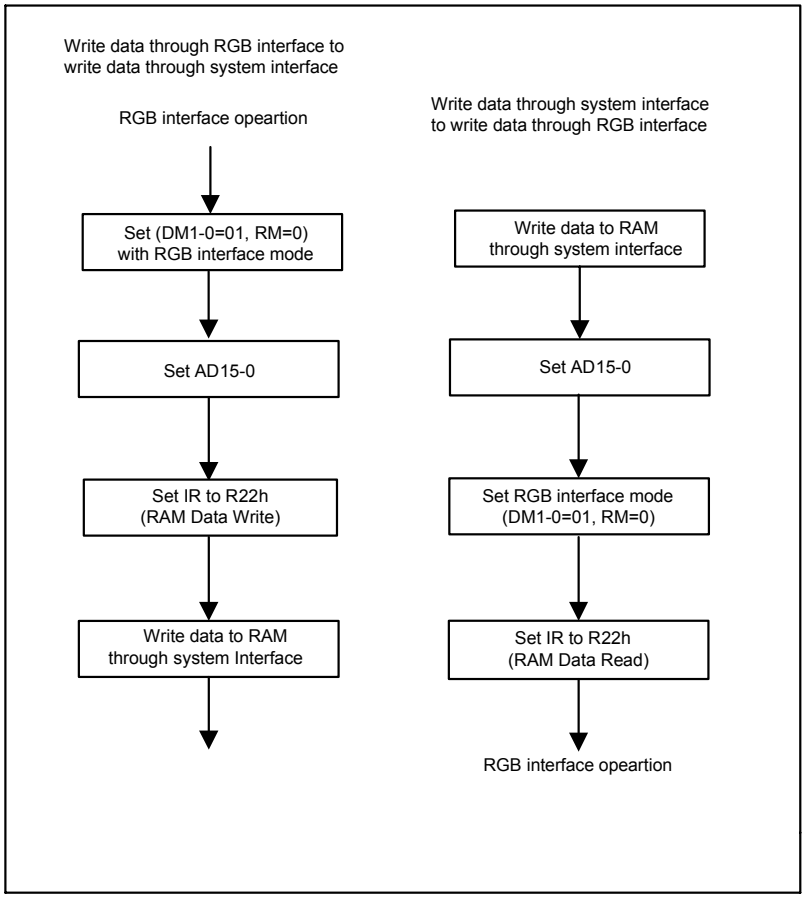


Figure 26 RAM Data Write Sequence during RGB Interface Mode

The FGD0801 supports 18-/16-/6-bit bus RGB interface by setting register RIM1-0 only through the system interface.

1) 18-bit bus RGB interface

The 18-bit interface can be used by setting RIM1-0 bits to “00”. The Figure 27 is the example of 18-bit RGB interface with LCD Controller and FGD0801. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via DB17-0 bits and according to the signal of data enable (ENABLE). The Figure 28 is the data format of 18-bit RGB interface.

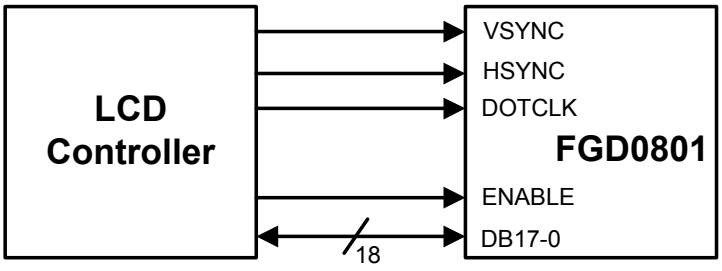


Figure 27 18-bit RGB Interface

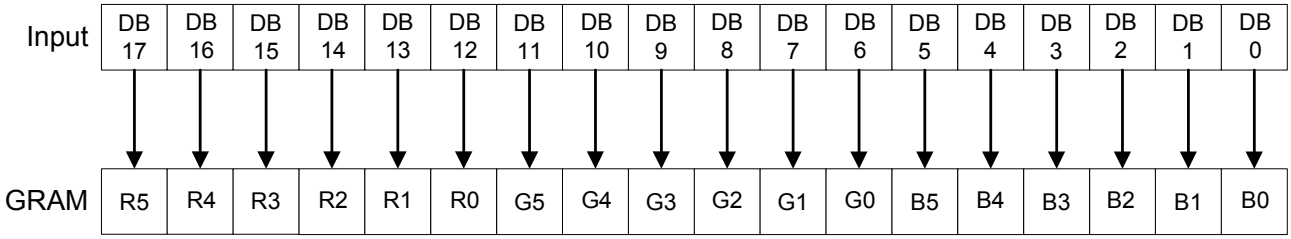


Figure 28 Data Format for 18-bit Interface (262,144 colors)

2) 16-bit bus RGB interface

The 16-bit bus interface can be used by setting RIM1-0 bits to “01”. The display data are transferred in pixel unit via DB data bus (DB17-13, DB11-1 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins (DB12, DB0) must be fixed to the IOVCC or VSSD level.

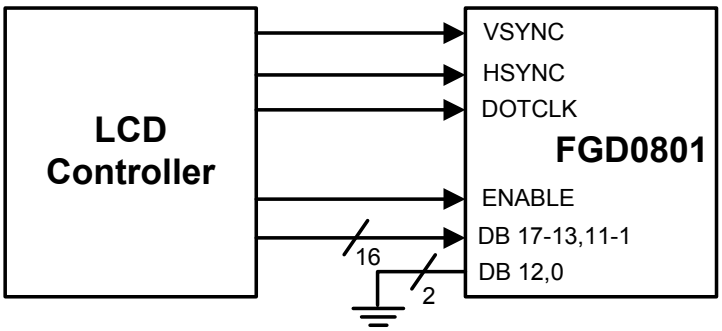


Figure 29 16-bit RGB Interface

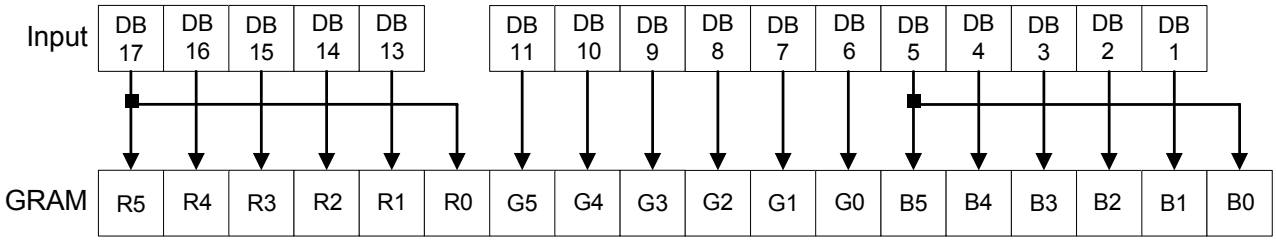


Figure 30 Data Format for16-bit Interface (65,536 colors)

3) 6-bit bus RGB interface

The 6-bit bus interface can be used by setting RIM1-0 bits to “10”. The display data are transferred in pixel unit via DB data bus (DB17-12 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins (DB11-0) must be fixed to the IOVCC or VSSD level.

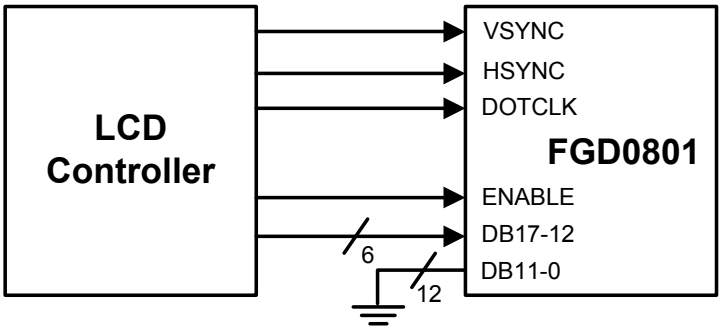


Figure 31 6-bit RGB Interface

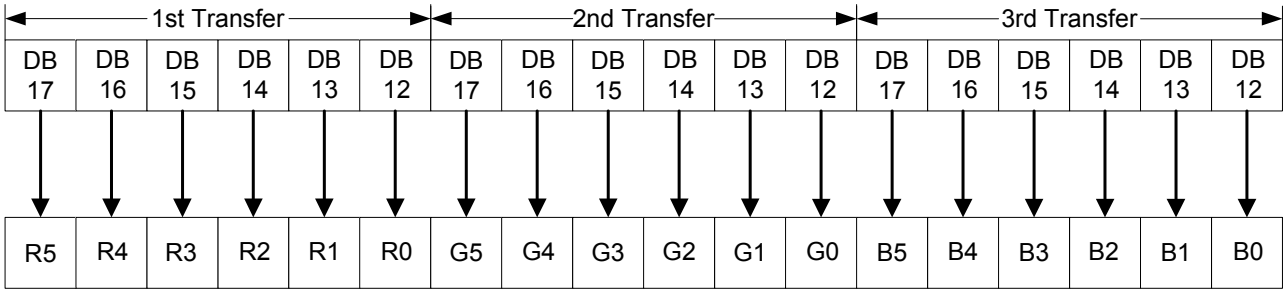


Figure 32 Data Format for 6-bit Interface (262,144 colors)

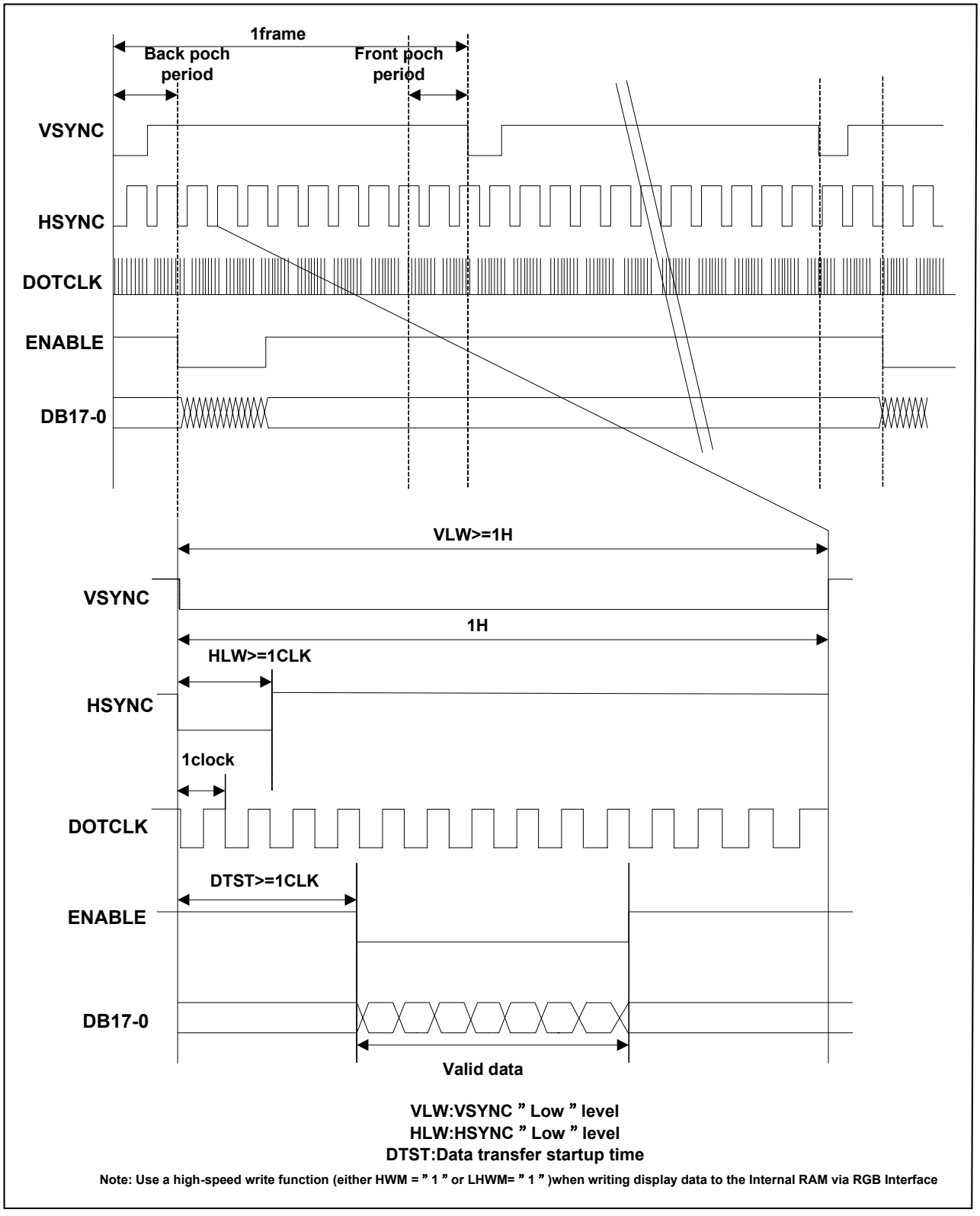
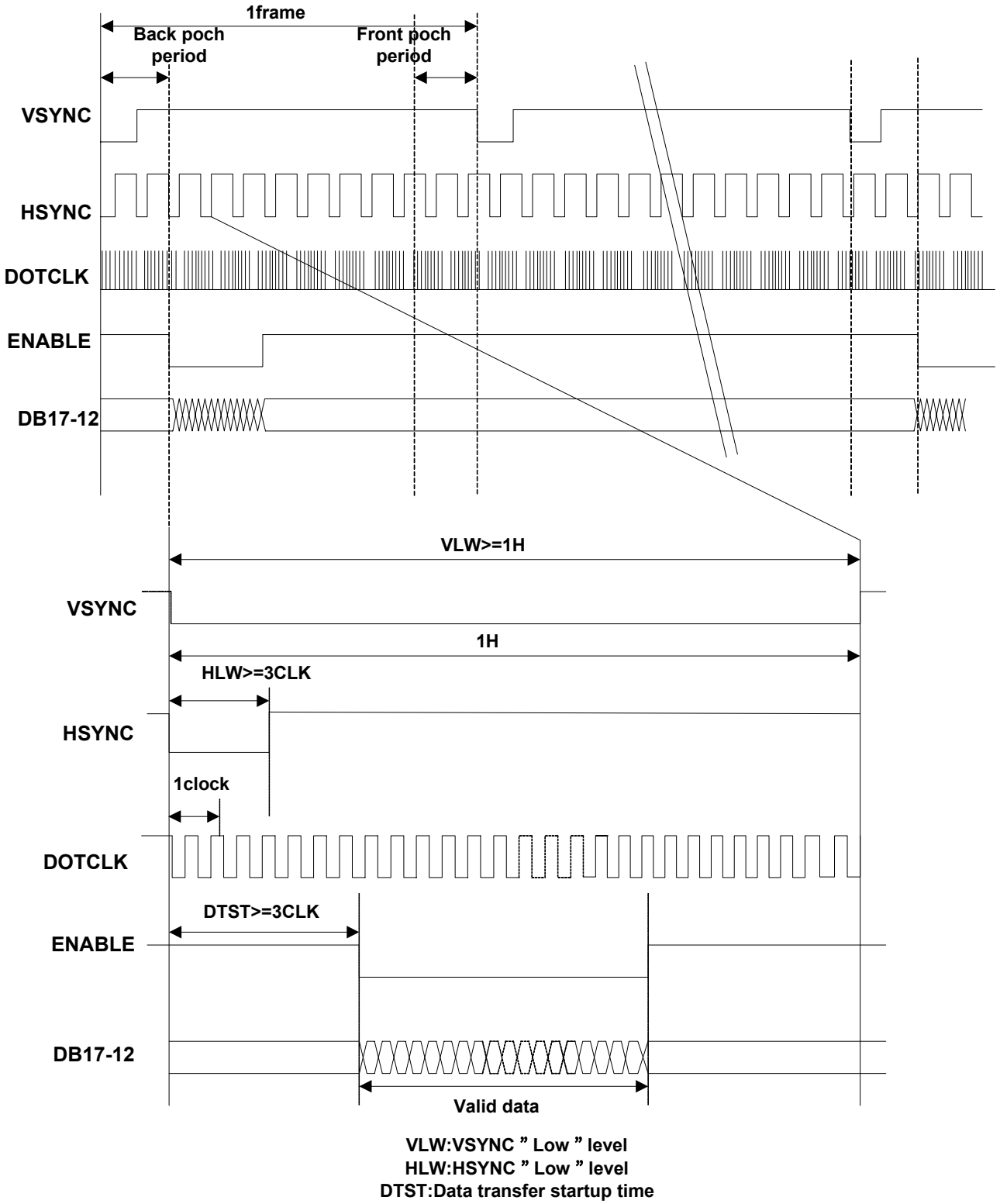


Figure 33 18/16-bit RGB Interface Timing



Notes: 1）Use a high-speed write function (either HWM = ” 1 ” or LHWM= ” 1 ”)when writing display data to the Internal RAM via RGB Interface .
2）Transfer data for one pixel (DB17-12*3) with 3 DOTCLKs. Also, the cycle of each RGB Interface signal (VSYNC ， HSYNC，ENABLE) must contain a multiple of 3 DOTCLKs.

Figure 34 6-bit RGB Interface Timing

5. Function Description

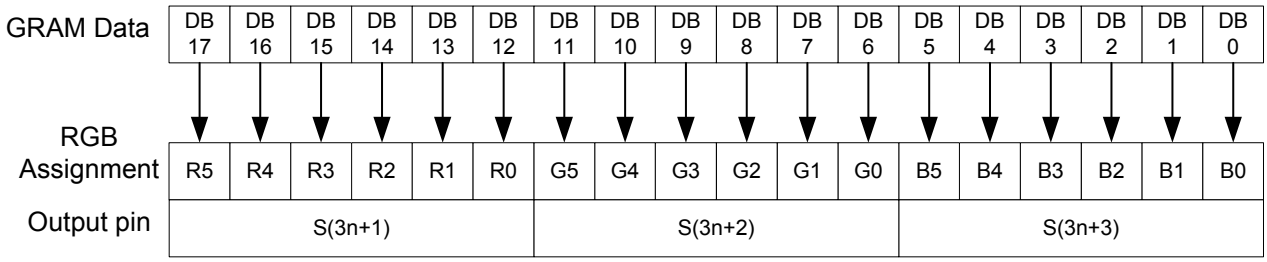
5.1 Graphics RAM

GRAM is graphics RAM, which can store a maximum 46,080-byte (128RGB x 160 (dots) x 18(bits)/8) pattern data using 18 bits per pixel. The GRAM address map is listed as following:

S pins / G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	------	S376	S377	S378	S379	S380	S381	S382	S383	S384
GS=1	**GS=0**	**DB17---DB0**			**DB17---DB0**			**DB17---DB0**			**------**	**DB17---DB0**			**DB17---DB0**			**DB17---DB0**		
G160	G1	0000H			0001H			0002H			------	007DH			007EH			007FH		
G159	G2	0100H			0101H			0102H			------	017DH			017EH			017FH		
G158	G3	0200H			0201H			0202H			------	027DH			027EH			027FH		
G157	G4	0300H			0301H			0302H			------	037DH			037EH			037FH		
G156	G5	0400H			0401H			0402H			------	047DH			047EH			047FH		
G155	G6	0500H			0501H			0502H			------	057DH			057EH			057FH		
G154	G7	0600H			0601H			0602H			------	067DH			067EH			067FH		
G153	G8	0700H			0701H			0702H			------	077DH			077EH			077FH		
G152	G9	0800H			0801H			0802H			------	087DH			087EH			087FH		
G151	G10	0900H			0901H			0902H			------	097DH			097EH			097FH		
⋮	⋮	⋮			⋮			⋮			------	⋮			⋮			⋮		
G10	G151	9600H			9601H			9602H			------	967DH			967EH			967FH		
G9	G152	9700H			9701H			9702H			------	977DH			977EH			977FH		
G8	G153	9800H			9801H			9802H			------	987DH			987EH			987FH		
G7	G154	9900H			9901H			9902H			------	997DH			997EH			997FH		
G6	G155	9A00H			9A01H			9A02H			------	9A7DH			9A7EH			9A7FH		
G5	G156	9B00H			9B01H			9B02H			------	9B7DH			9B7EH			9B7FH		
G4	G157	9C00H			9C01H			9C02H			------	9C7DH			9C7EH			9C7FH		
G3	G158	9D00H			9D01H			9D02H			------	9D7DH			9D7EH			9D7FH		
G2	G159	9E00H			9E01H			9E02H			------	9E7DH			9E7EH			9E7FH		
G1	G160	9F00H			9F01H			9F02H			------	9F7DH			9F7EH			9F7FH		

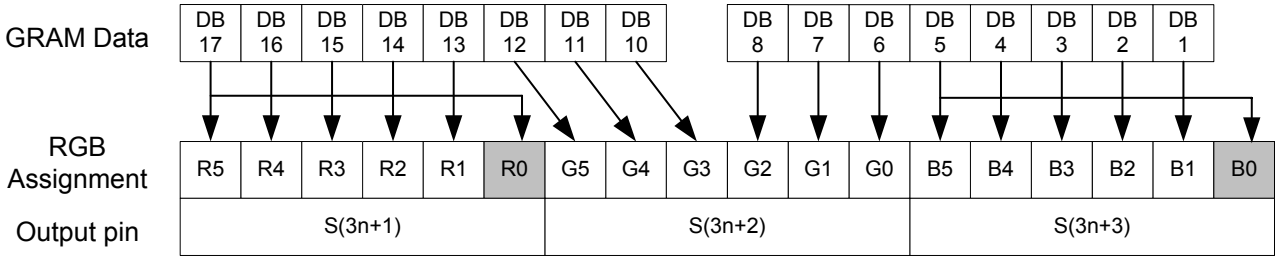
Table 8 GRAM Address and Display Panel Position (SS =“0”, BGR =“0”)

80-system/68-system 18-bit bus interface



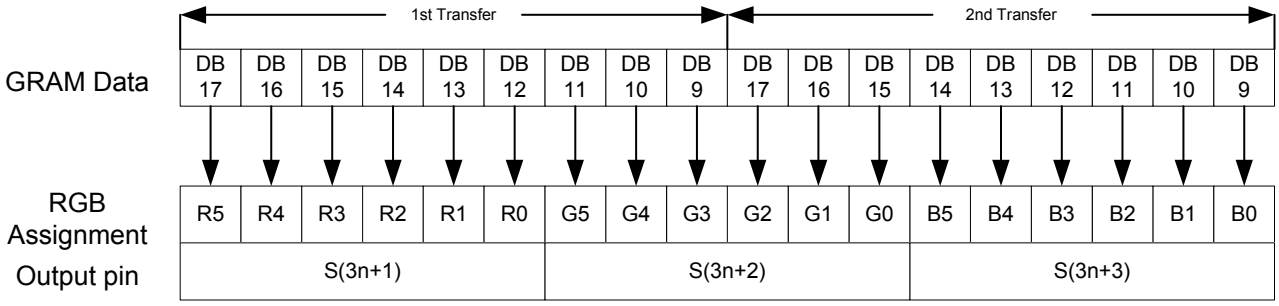
Note:n= lower eight bits of address (0 to 127)

80-system/68-system 16-bit bus interface



Note:n= lower eight bits of address (0 to 127)

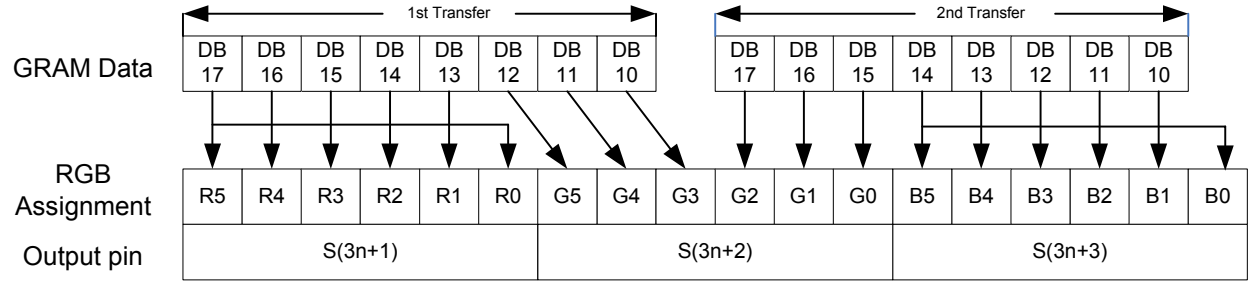
80-system/68-system 9-bit bus interface



Note:n= lower eight bits of address (0 to 127)

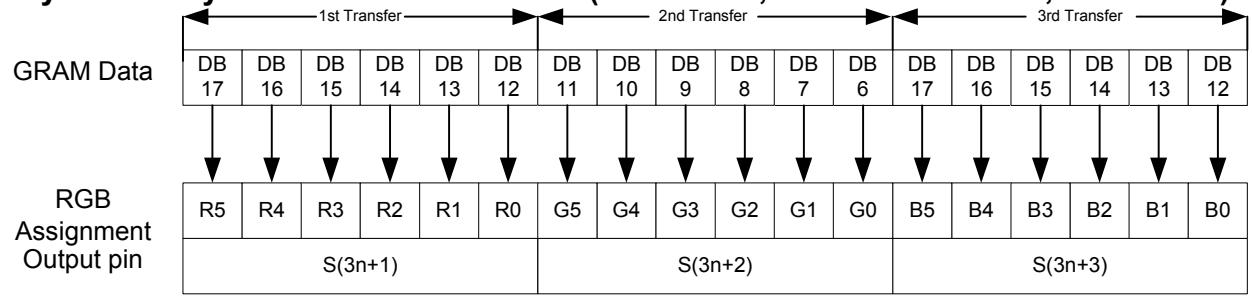
Figure 35 GRAM Data and Display Data of 18-/16-/ 9-bit Bus Interface (SS = “0”, BGR = “0”)

80-system/68-system 8-bit bus interface(2 transfers/pixel)



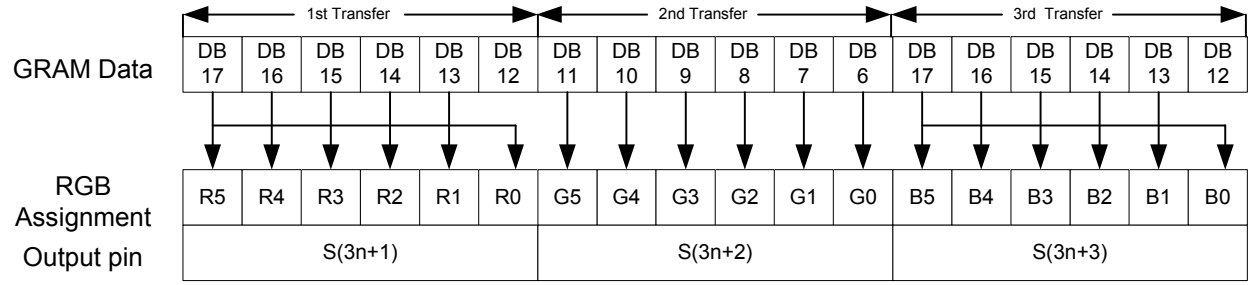
Note:n= lower eight bits of address (0 to 127)

80-system/68-system 8-bit bus interface(3 transfers,262k colors: TRI=1,DFM1-0=10)



Note:n= lower eight bits of address (0 to 127)

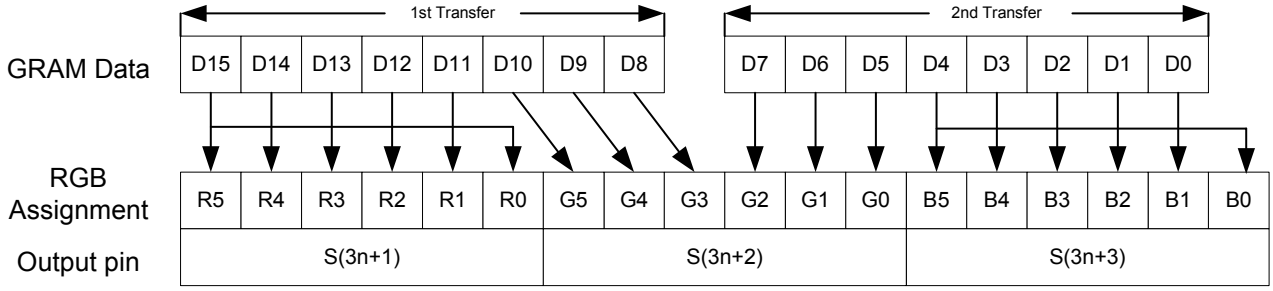
80-system/68-system 8-bit bus interface(3 transfers,65k colors: TRI=1,DFM1-0=11)



Note:n= lower eight bits of address (0 to 127)

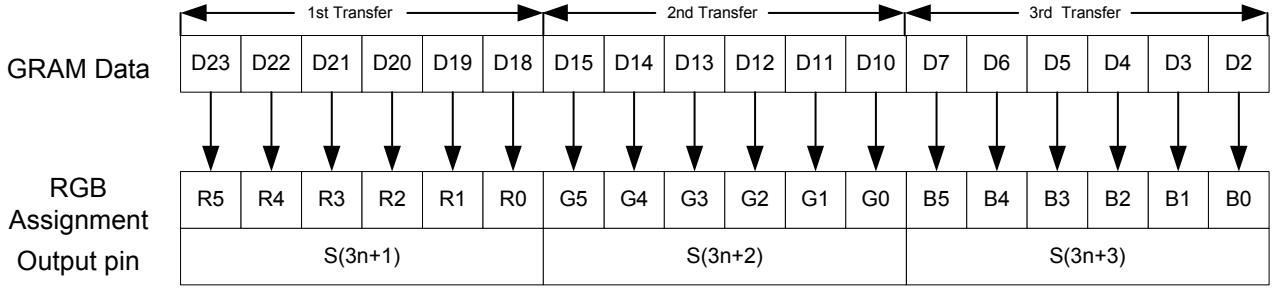
Figure 36 GRAM Data and Display Data of 8-bit Bus Interface (SS = “0”, BGR = “0”)

Serial Date Transfer interface (2 transfers/65k colors: TRI=0)



Note:n= lower eight bits of address (0 to 127)

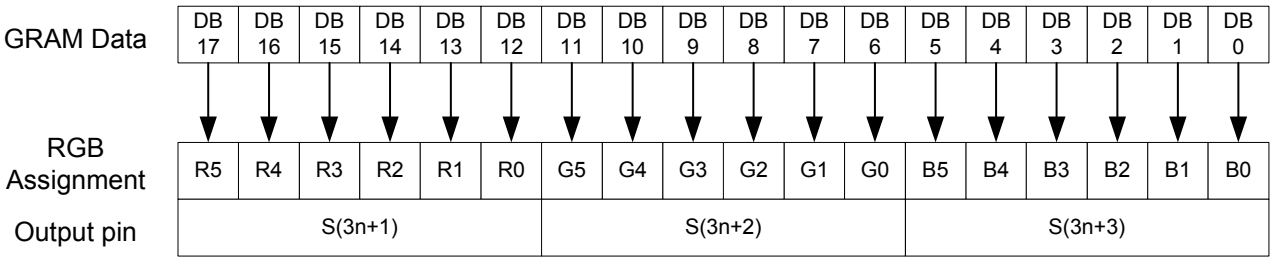
Serial Date Transfer interface (3 transfers/262k colors: TRI=1,DFM1-0=10)



Note:n= lower eight bits of address (0 to 127)

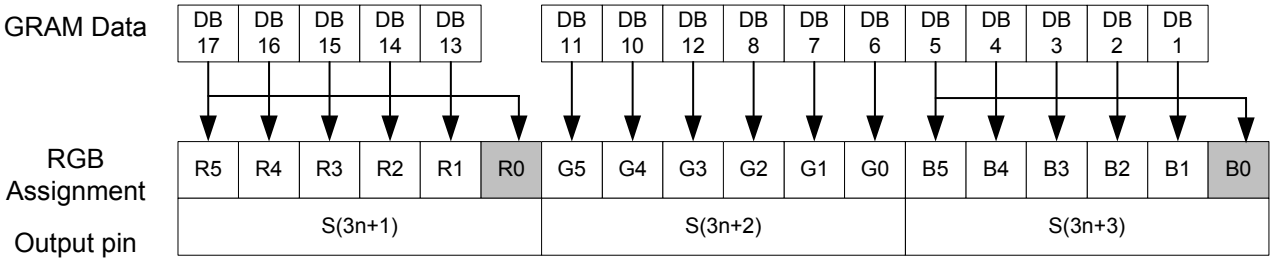
Figure 37GRAM data and display data of Serial Data transfer interface (SS = “0” ,BGR = “0”)

18-bit RGB Interface



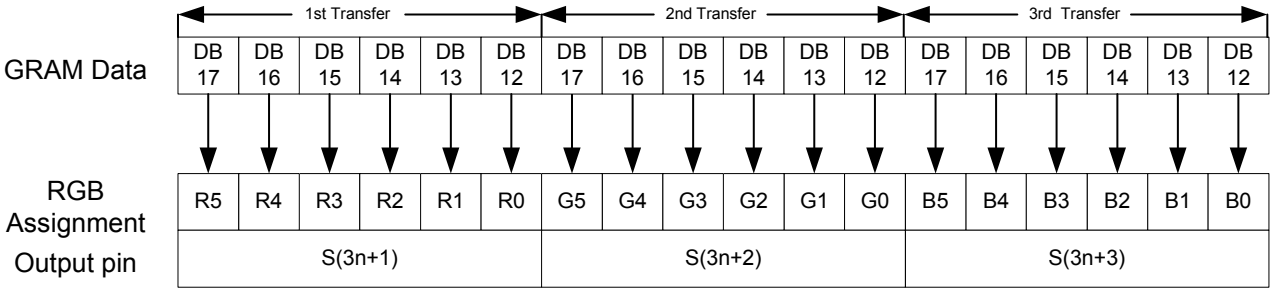
Note:n= lower eight bits of address (0 to 127)

16-bit RGB Interface



Note:n= lower eight bits of address (0 to 127)

6-bit RGB Interface



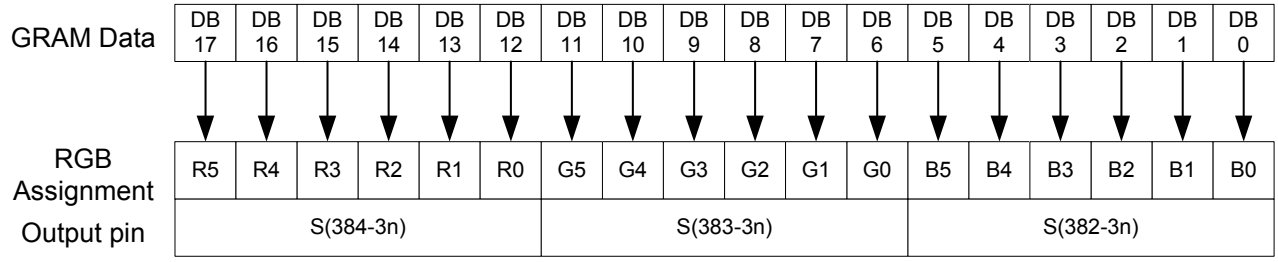
Note:n= lower eight bits of address (0 to 127)

Figure 38 GRAM Data and Display Data of RGB Interface (SS = “0”, BGR = “0”)

S pins / G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	------	S376	S377	S378	S379	S380	S381	S382	S383	S384
GS=0	**GS=1**	**DB17---DB0**			**DB17---DB0**			**DB17---DB0**			**------**	**DB17---DB0**			**DB17---DB0**			**DB17---DB0**		
G1	G160	007FH			007EH			007DH			------	0002H			0001H			0000H		
G2	G159	017FH			017EH			017DH			------	0102H			0101H			0100H		
G3	G158	027FH			027EH			027DH			------	0202H			0201H			0200H		
G4	G157	037FH			037EH			037DH			------	0302H			0301H			0300H		
G5	G156	047FH			047EH			047DH			------	0402H			0401H			0400H		
G6	G155	057FH			057EH			057DH			------	0502H			0501H			0500H		
G7	G154	067FH			067EH			067DH			------	0602H			0601H			0600H		
G8	G153	077FH			077EH			077DH			------	0702H			0701H			0700H		
G9	G152	087FH			087EH			087DH			------	0802H			0801H			0800H		
G10	G151	097FH			097EH			097DH			------	0902H			0901H			0900H		
⋮	⋮	⋮			⋮			⋮			------	⋮			⋮			⋮		
G152	G9	977FH			977EH			977DH			------	9702H			9701H			9700H		
G153	G8	987FH			987EH			987DH			------	9802H			9801H			9800H		
G154	G7	997FH			997EH			997DH			------	9902H			9901H			9900H		
G155	G6	9A7FH			9A7EH			9A7DH			------	9A02H			9A01H			9A00H		
G156	G5	9B7FH			9B7EH			9B7DH			------	9B02H			9B01H			9B00H		
G157	G4	9C7FH			9C7EH			9C7DH			------	9C02H			9C01H			9C00H		
G158	G3	9D7FH			9D7EH			9D7DH			------	9D02H			9D01H			9D00H		
G159	G2	9E7FH			9E7EH			9E7DH			------	9E02H			9E01H			9E00H		
G160	G1	9F7FH			9F7EH			9F7DH			------	9F02H			9F01H			9F00H		

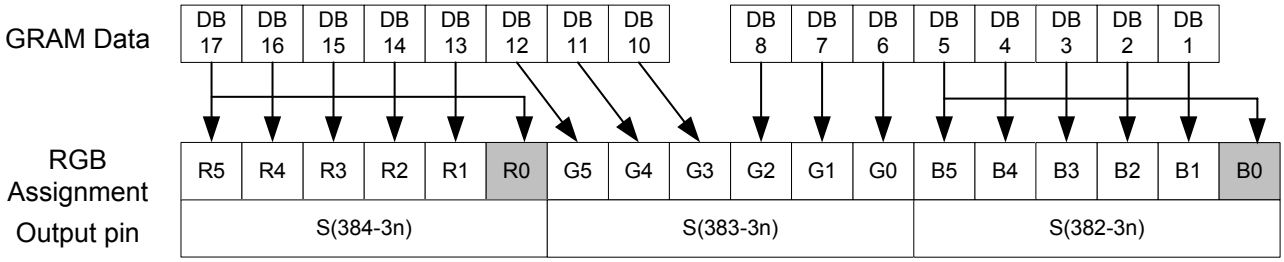
Table 9 GRAM Address and Display Panel Position (SS =”1”, BGR=”1”)

80-system 18-bit bus interface



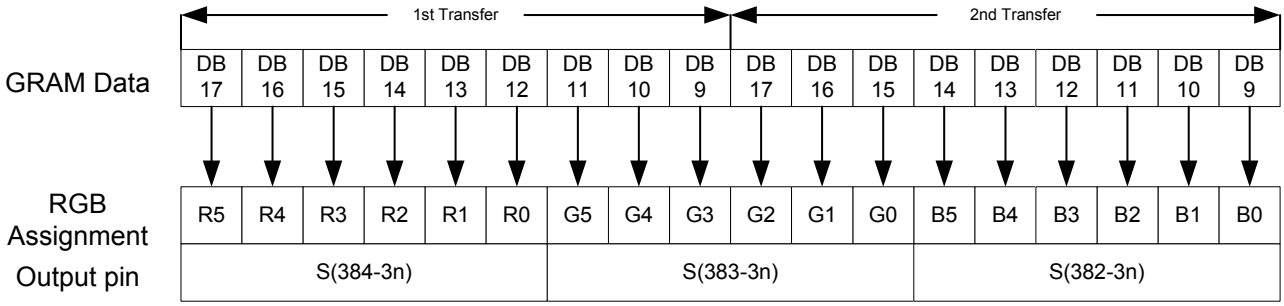
Note:n= lower eight bits of address (0 to 127)

80-system 16-bit bus interface



Note:n= lower eight bits of address (0 to 127)

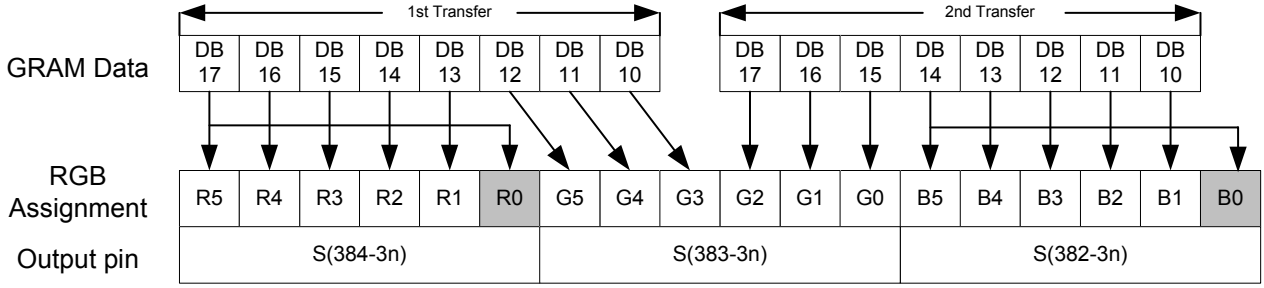
80-system 9-bit bus interface



Note:n= lower eight bits of address (0 to 127)

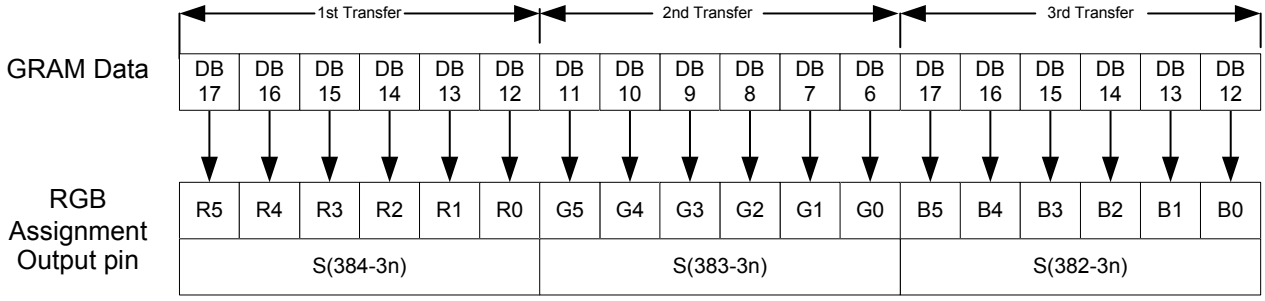
Figure 39 GRAM Data and Display Data of 18-/16-/ 9-bit Bus Interface (SS = “1”, BGR = “1”)

80-system 8-bit bus interface/ Serial Date Transfer Interface(2 transfers/pixel)



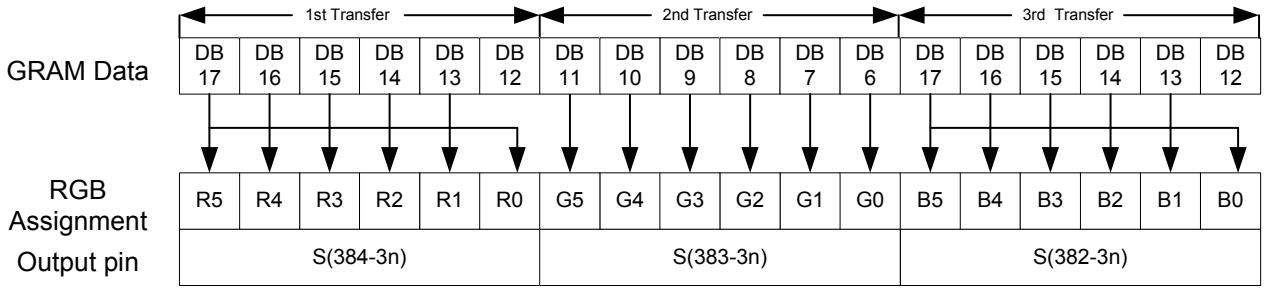
Note:n= lower eight bits of address (0 to 127)

80-system/68-system 8-bit bus interface(3 transfers,262k colors: TRI=1,DFM1-0=10)



Note:n= lower eight bits of address (0 to 127)

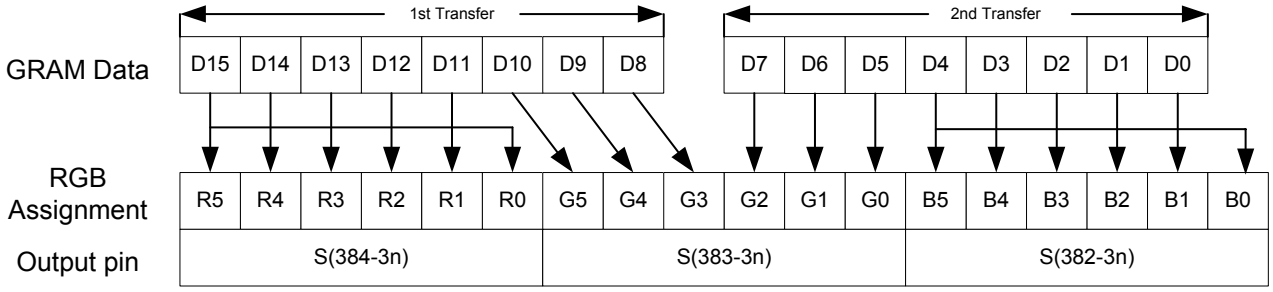
80-system/68-system 8-bit bus interface(3 transfers,65k colors: TRI=1,DFM1-0=11)



Note:n= lower eight bits of address (0 to 127)

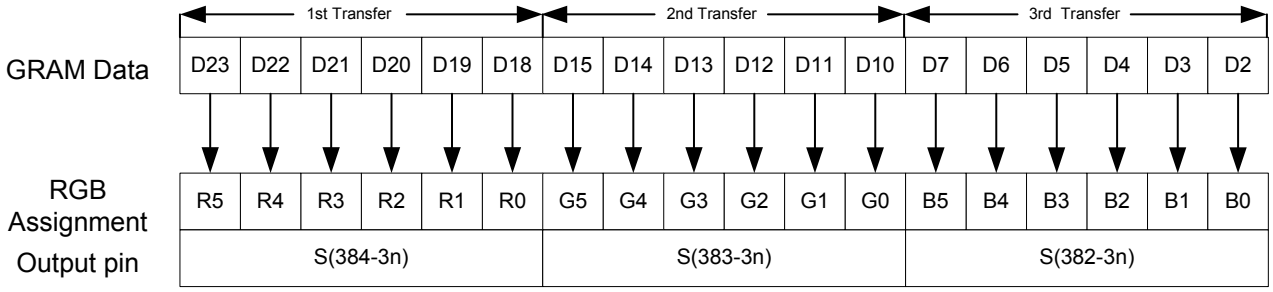
Figure 40 GRAM Data and Display Data of 8-bit Bus Interface (SS = “1”, BGR = “1”)

Serial Date Transfer interface (2 transfers/65k colors: TRI=0)



Note:n= lower eight bits of address (0 to 127)

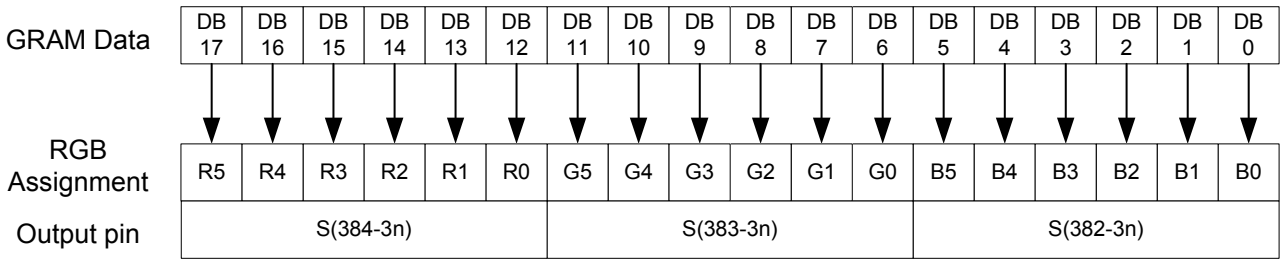
Serial Date Transfer interface (3 transfers/262k colors: TRI=1,DFM1-0=10)



Note:n= lower eight bits of address (0 to 127)

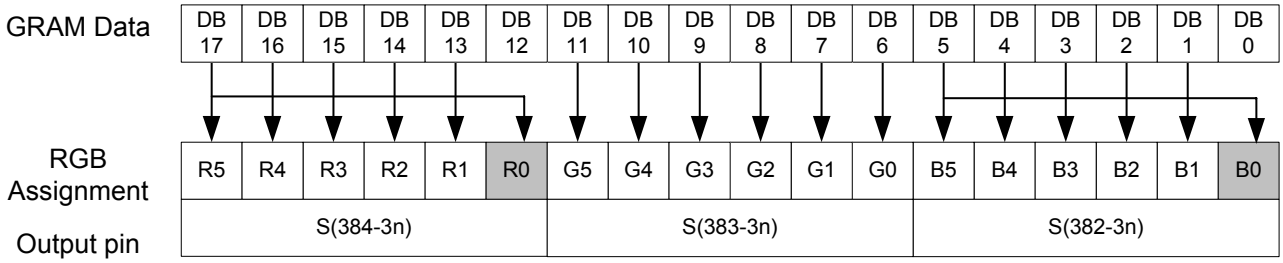
Figure 41GRAM data and display data of Serial Data transfer interface (SS = “1” ,BGR = “1”)

18-bit RGB Interface



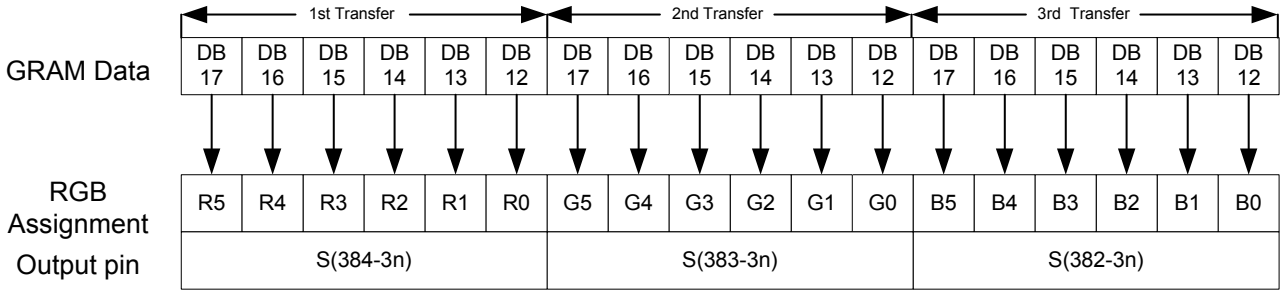
Note:n= lower eight bits of address (0 to 127)

16-bit RGB Interface



Note:n= lower eight bits of address (0 to 127)

6-bit RGB Interface



Note:n= lower eight bits of address (0 to 127)

Figure 42 GRAM Data and Display Data of RGB Interface (SS = “1”, BGR = “1”)

5.1.1 Window Address Function

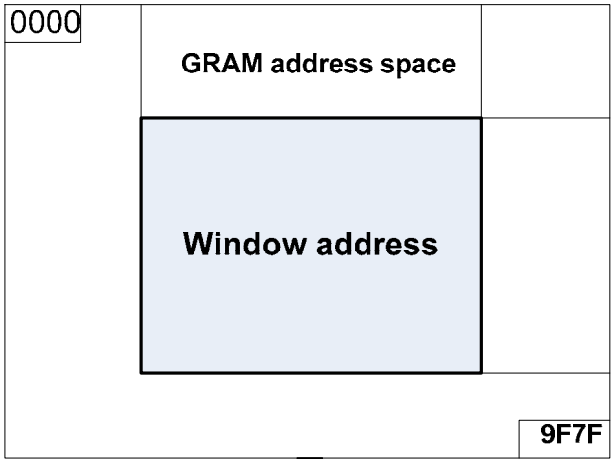
Data can be written consecutively without thinking a data wrap by those bit function through Window Address Function in FGD0801. The FGD0801 contains a GRAM 16-bit bus address counter (AC), when the address setting instruction is written in the IR, the address information is sent from the IR to the AC. When the data is written to the internal GRAM, the AC is automatically incremented (plus one) or decremented (minus one), which is decided by the register (AM bit and I/D bits) setting. The window address function enables writing data only within the rectangular area specified in GRAM by setting. The window address area is decided by setting the horizontal address register (start: HSA7-0, end: HEA7-0) and the vertical address register (start: VSA7-0, end: VEA7-0). The window address must be within the GRAM address map area, and the AD16-0 bits must be within the window address.

The window address setting range:

$$00H \le HSA7\text{-}0 \le HEA7\text{-}0 \le 7FH$$
$$00H \le VSA7\text{-}0 \le VEA7\text{-}0 \le 9FH$$

GRAM address setting range:

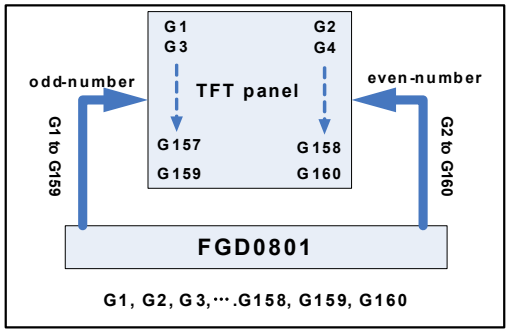
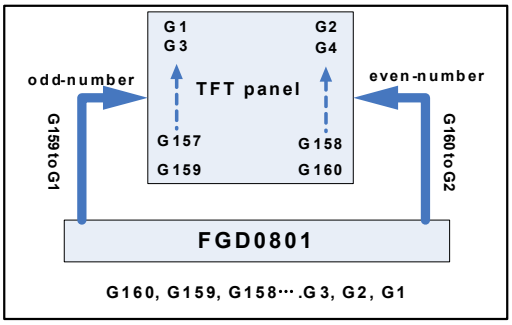
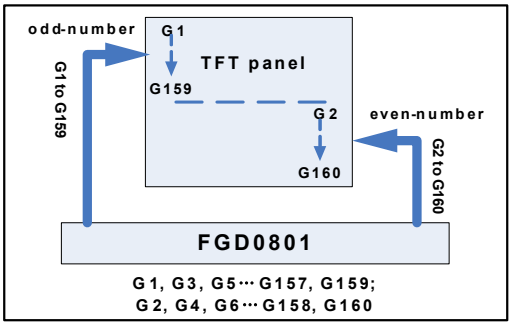
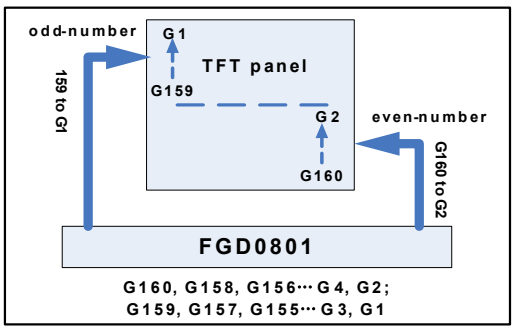
$$HSA7\text{-}0 \le AD7\text{-}0 \le HEA7\text{-}0$$
$$VSA7\text{-}0 \le AD15\text{-}8 \le VEA7\text{-}0$$



5.2 Display Function

5.2.1 Scan Mode Setting

The FGD0801 can set SM and GS bits to adapt various pins assignment of gate of different panels. The combination of SM and GS settings allows changing the different shift direction of gate outputs when connecting LCD panel.

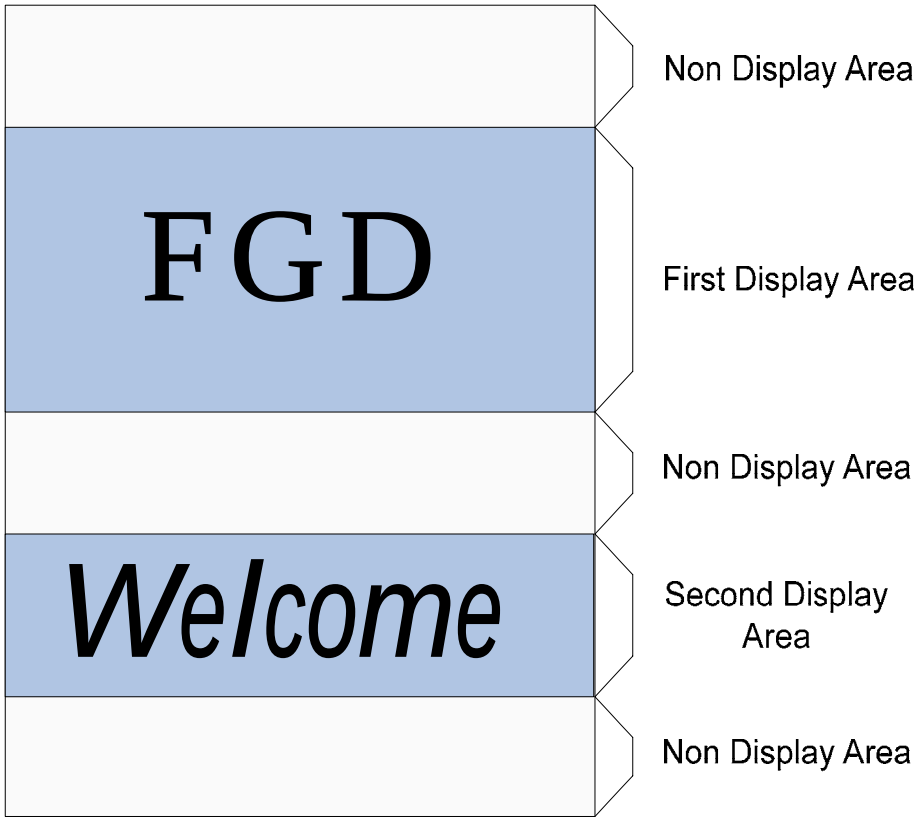
SM	GS	Scan direction
0	0	
0	1	
1	0	
1	1	

Note: scan mode is determined by the layout and design of glass on the panel.

Figure 43 Scan Mode setting

5.2.2 Partial Screen Display Function

The FGD0801 can drive one or two partial screen to display. The position of display screen register (R14h and R15h) can be set at any position of the whole screen. The total numbers of display lines that display on the first and second screens must be less than total LCD-driving lines determined by register NL4-0. The rest display area in the panel should be white if the type of LCD is normally white and should be black if the type of LCD is normally black. Therefore, the partial display can reduce the power consumption. As the below, the first screen start line from the SS1(7-0) and end line at SE1(7-0) are specified by the 1st Display Screen Driving Position Register(R14h), the second screen start line from SS2(7-0) and end line at SE2(7-0) are specified by 2nd Display Window Driving Position Register(R15h). And the second display screen display is valid when the SPT bit is set to 1. The number of the total selection driving lines included the 1st and 2nd display screen must be equal to or less than the total LCD Driving Lines (set by NL).



Notes: Number of Scan Line: NL (4-0) = "10011" (160 lines)
1st Screen Setting: SS1 (7-0) ="0E"h, SE1 (7-0) ="2C"h
2nd Screen Setting: SS2 (7-0) ="4A"h, SE2 (7-0) ="5E"h, SPT=1

Figure 44 Partial Screen Display Example in Two Windows Driving

The conditions as following must be satisfied when using this function by setting the start line SS1(7-0) and end line SE1(7-0) of the 1st display window at register(R14h) and the start line SS2(7-0) and end line SE2(7-0) of the 2nd display window at register(R14).

Note: That incorrect display may happen if the conditions are not satisfied.
Condition: 0 ≤SS1 (7-0) ≤ SE1 (7-0) ≤NL

Register Settings	Display Operation
SE1(7-0) – SS1(7-0) +1 = NL	Whole Screen Display The area of SE1 (7-0)-SS1 (7-0) is normally displayed
0 < SE1 (7-1) – SS1 (7-0) +1 < NL	Partial Screen Display The area of SE1 (7-0)-SS1 (7-0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

Table 10 Conditions on One Screen Driving (STP = 0)

Note: The SS2 (7-0) and SE2 (7-0) settings are ignored.
Condition: 0 ≤ SS1 (7-0) ≤ SE1 (7-0) < SS2 (7-0) ≤ SE2 (7-0) ≤ NL

Register Settings	Display Operation
(SE1 (7-0) – SS1 (7-0)+1)+ (SE2 (7-0) – SS2 (7-0)+1)=NL	Whole-Screen Display The area of SE2 (7-0)-SS1 (7-0) is normally displayed
0 < (SE1 (7-0) – SS1 (7-0)+1)+ (SE2 (7-0) – SS2 (7-0)+1) < NL	Partial Screen Display The area of SE1 (7-0)-SS1 (7-0) and SE2 (7-0) – SS2 (7-0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

Table 11 Conditions on Two Screen Driving (STP = 1)

The source outputs for non-display area on partial display can be determined by the register PT. Set the values to match the characteristics of the panel.

PT1	PT0	Source Output in Non Display Area		Gate Output in Non Display Area	VCOM Output
		Positive Polarity	Negative Polarity		
0	0	V63	V0	reference to PTG	VCOMH-VCOML
0	1	ignore	ignore	reference to PTG	VCOMH-VCOML
1	0	VSSD	VSSD	reference to PTG	VCOMH-VCOML
1	1	Hi-Z	Hi-Z	reference to PTG	--

Table 12 Source and Gate Output in Non-Display Area during Partial Display

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

PTG1	PTG0	Gate output in non-display area
0	0	Normal scan
0	1	VGL (Fixed)
1	0	Interval scan
1	1	Setting Disabled

Table 13 Gate Output in Non-Display Area in Partial Display

Setting of the partial display should follow the flow chart shown as below

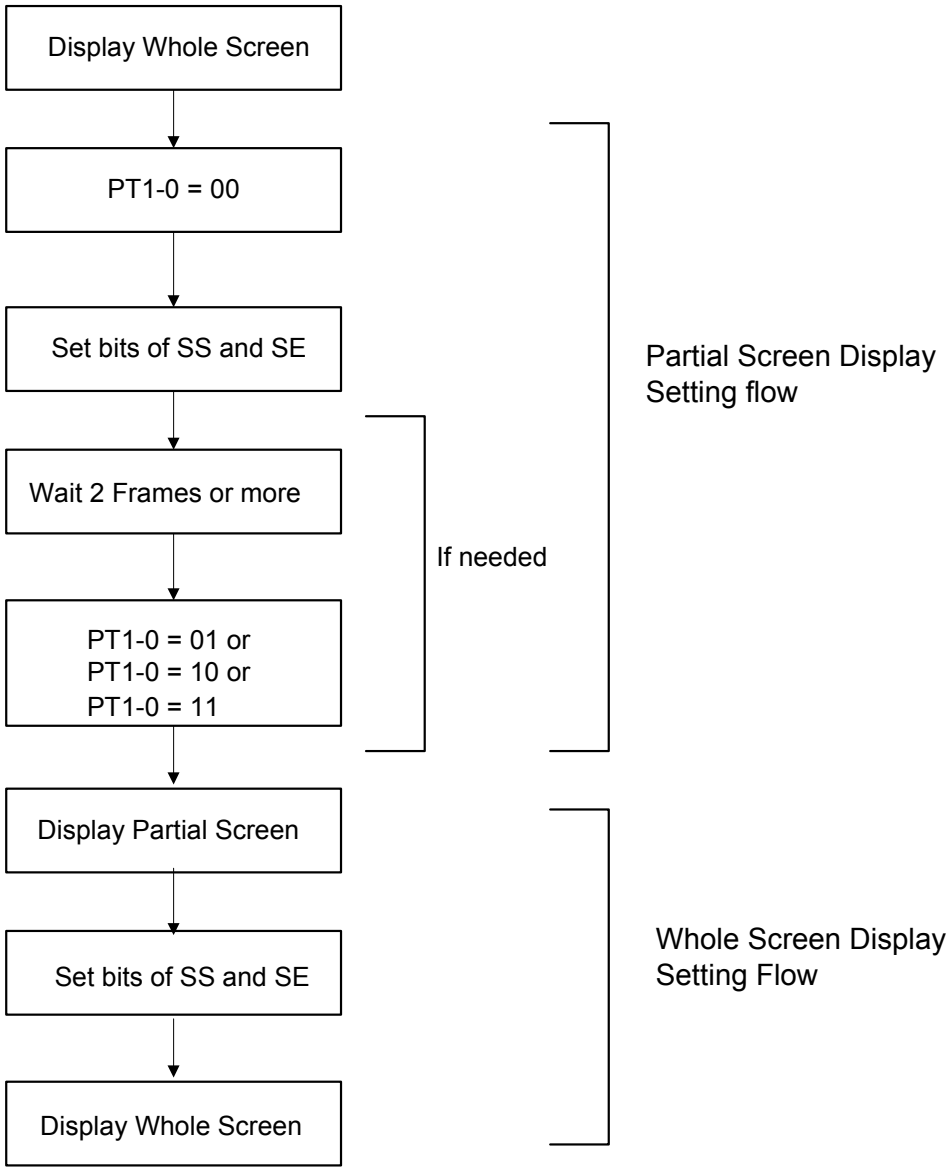


Figure 45 Partial Display Setting Flow

5.2.3 8-Color Display

The FGD0801 supports an 8-color display mode. The grayscale level to be used is V0 and V63 which is selected by R5, G5, B5 decoding, and the other levels (V1-V62) are halted in order to reduce the power consumption. In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

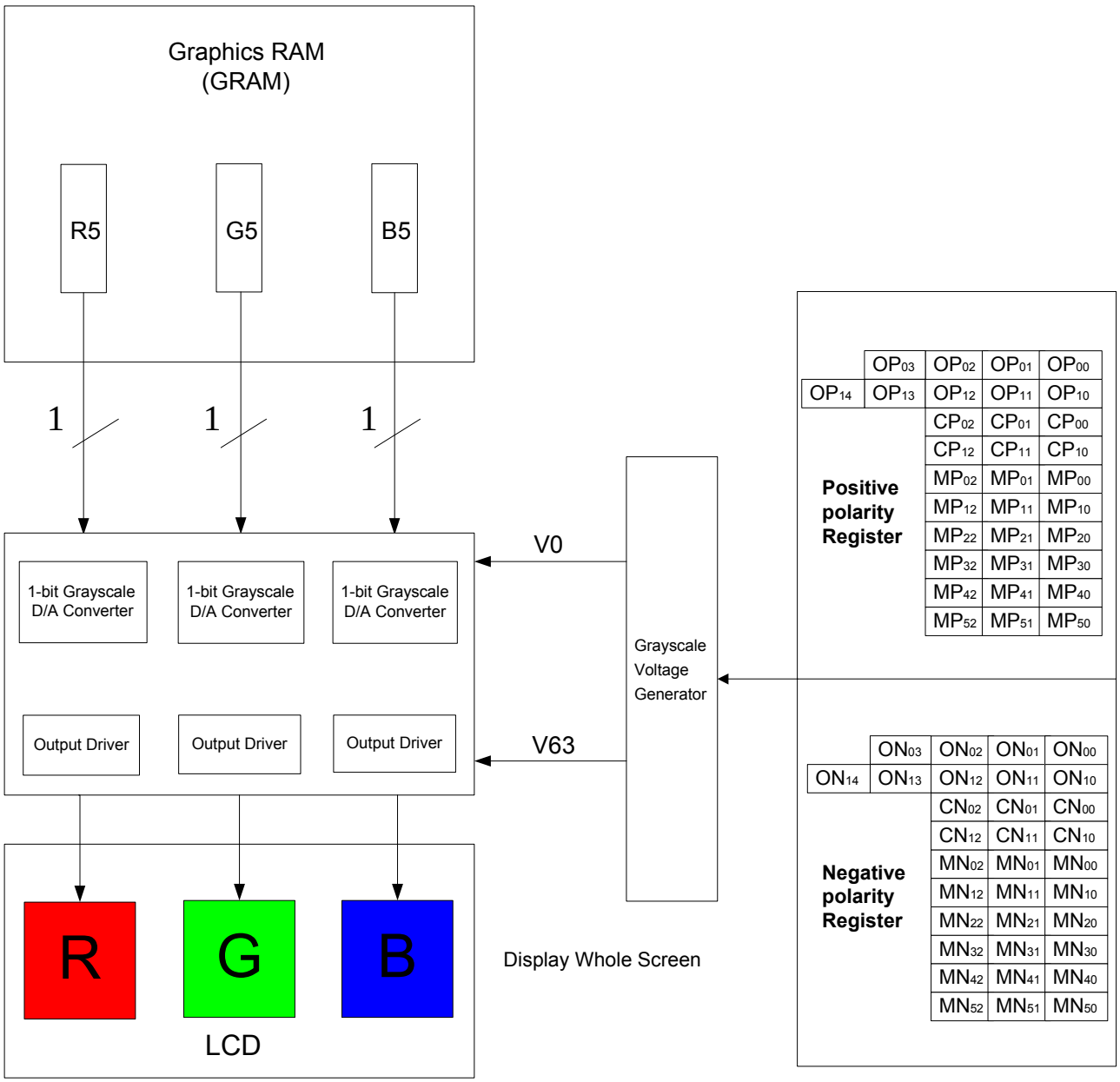


Figure 46 Grayscale Control in 8-Color Mode

The following figure is the switch sequence between the 262,144-color mode and 8-color mode:

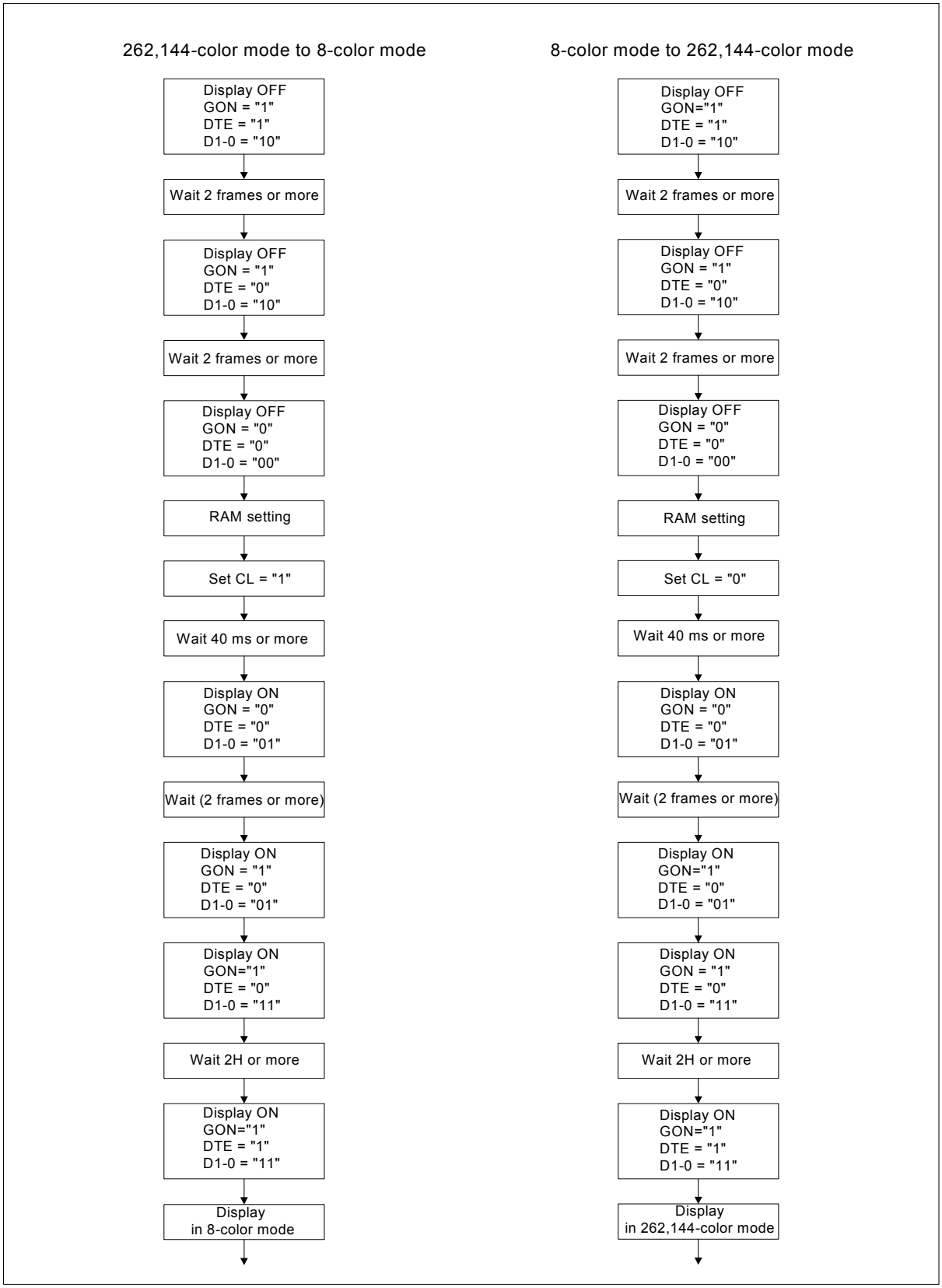
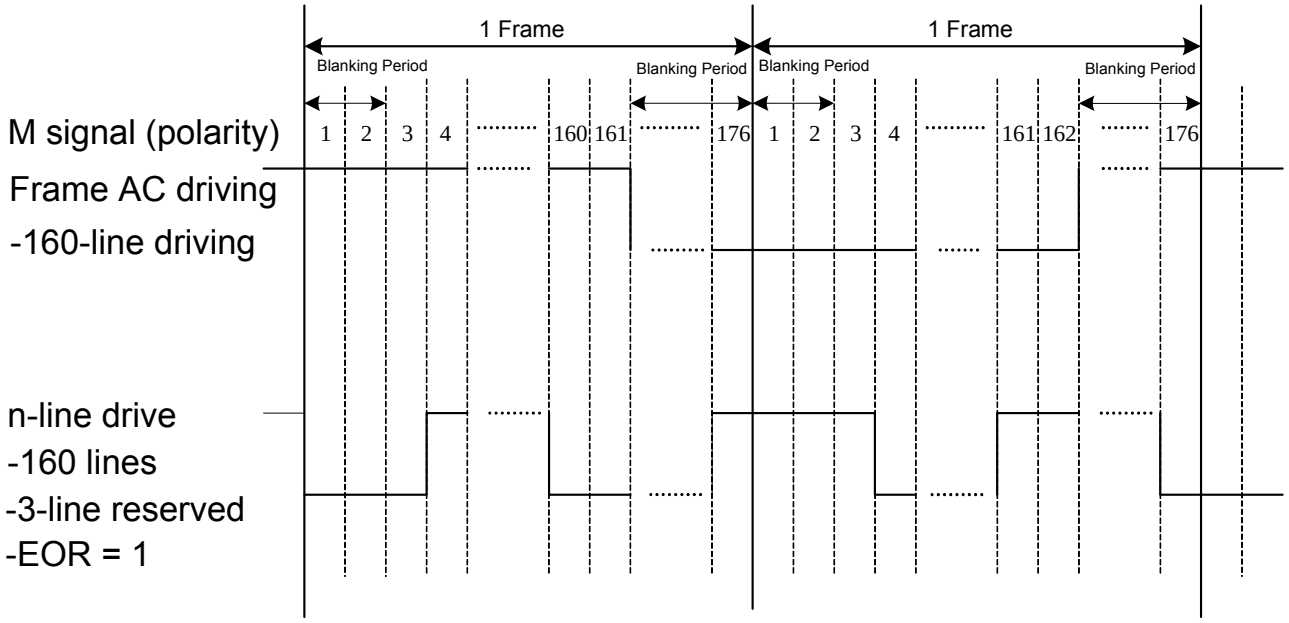


Figure 47 Switch Sequence between 262,144-color Mode and 8-color Mode

5.2.4 N-line Inversion LCD Driver

The FGD0801 supports frame inversion and n-line inversion LCD current driving at the same time, and in N-line inversion n chooses 1~64. The inversion operation is controlled by POL (Polarity of Liquid Crystal) signal whose interval is set by NW5-0 bits in R02h register. The FGD0801 internally generates POL signal for alternating the VCOM voltage and alternates source output voltage according to gamma register with POL signal, which changes the polarity of LCD driving voltage. The n-line inversion LCD drive can improve the quality by setting proper n value. The value of n also represented by the NW bits+1,which represented LCD alternating frequency becomes high when the number of inversion lines were setting a smaller value, hence, in the LCD cells, the charge or discharge current is increased.



Note: In an n-line driving, EOR should be set to 1 so that DC bias voltage is not applied

Figure 48 N-line Inversion Driving Diagram

5.2.5 Interlaced Driving Function

The FGD0801 has an interlaced function that can divide one frame into 3 fields to drive. To avoid flicker and confirm the display quality with the actual LCD display, the number of fields can be determined by users. As following figure, the output waveform is shown when 3 fields interlaced driving is performed.

GS = 0 FLD1-0=11

Field / Gate	1	2	3
G1	×		
G2		×	
G3			×
G4	×		
G5		×	
G6			×
G7	×		
G8		×	
G9			×
⋮	⋮	⋮	⋮
G157			
G158		×	
G159			×
G160	×		

GS = 1 FLD1-0=11

Field / Gate	1	2	3
G160	×		
G159		×	
G158			×
G157	×		
⋮	⋮	⋮	⋮
G9			
G8	×		
G7		×	
G6			×
G5			
G4			
G3		×	
G2			×
G1	×		

Figure 49 Combined with GS and FLD Setting

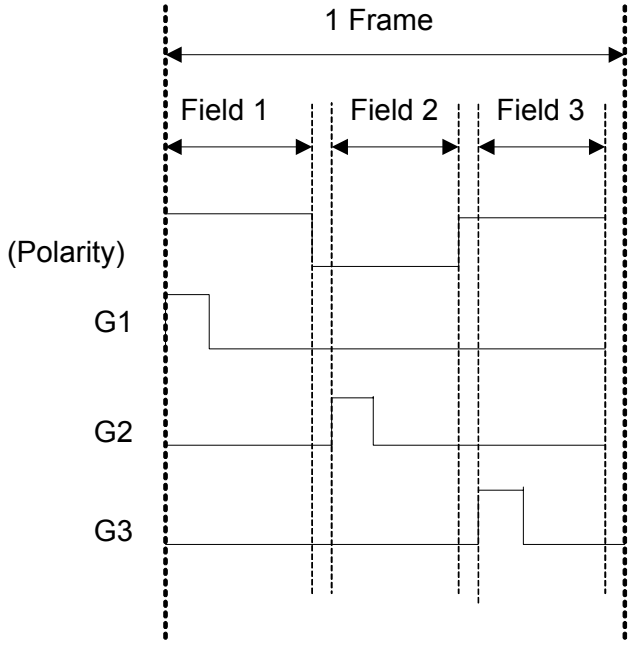


Figure 50 Output Timing for Interlaced Gate Signals (Three-Field is selected)

5.2.6 AC Driving Alternating Timing

LCD must be driven by alternating voltage polarity between liquid crystal layers. The operation of AC drive timing in each type is shown below. The period of AC drive timing is the same as the period of POL signal, which is controlled by the value in register R02h (NW).
In frame-inversion AC drive, LCD driving signal alternates after one frame display finish and then a FP or BP blanking period are inserted. During the blanking period all gate outputs remain VGL. In interlaced drive, LCD driving signal alternates after one field display finish and then a blanking period is inserted. The sum of blanking periods in three fields is equal to the sum of BP and FP blanking period set in a frame. For n-line inversion AC drive, LCD driving signal alternates before every n-line display starts. BP blanking period is inserted before all display operations start and FP blanking period is inserted after the completion of all display operations.

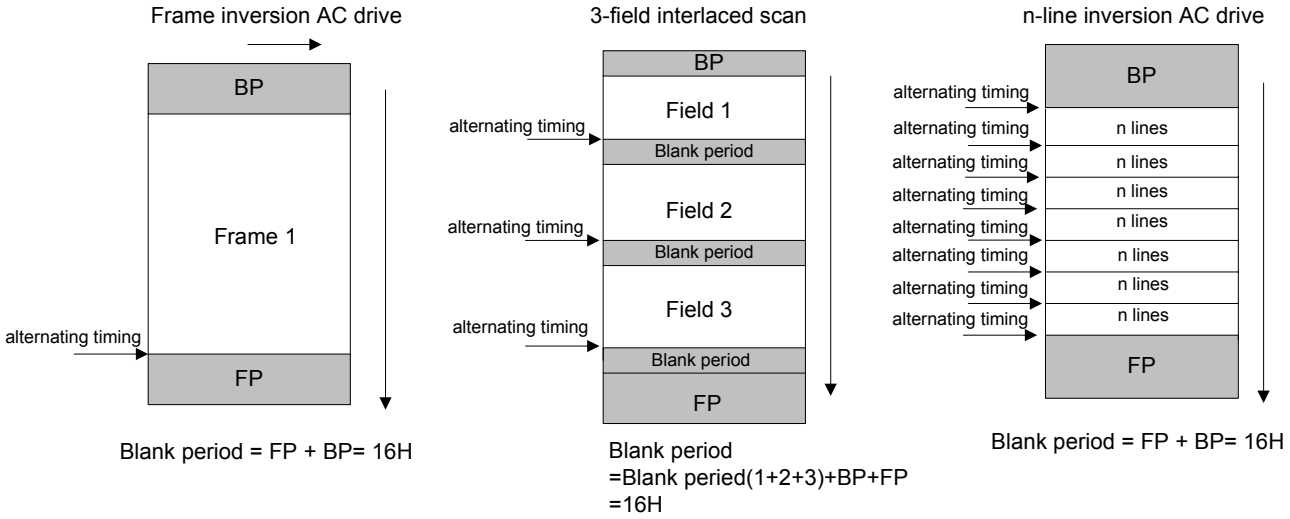


Figure 51 AC Driving Alternating Timing Diagram

5.3 Frame-Frequency Adjustment Function

The FGD0801 supports frame frequency adjustment function that can adjust the frame frequency via the register (DIV, RTN bits) setting in R0Bh during the oscillation frequency.
An animation or a static image can be displayed in suitable ways by changing the frame frequency.
When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered.

Relationship between LCD Drive Duty and Frame Frequency

The LCD driving duty and the frame frequency are obtained by the following calculation. The frame frequency can be adjusted in the 1-H line period bit (RTN) and in the operation clock division bit (DIV) by writing the instruction to the relative register.

Formula for the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{RTN} \times \text{DIV} \times (\text{NL}+\text{BP}+\text{FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency
RTN bit: Clocks per line
DIV bit: Division ratio
NL: The number of lines
FP: Number of lines for front porch
BP: Number of lines for back porch
BP+FP≦16

Example Calculation: To set the maximum frame frequency to 60 Hz

Number of drive lines: 160 lines
line period: 16 clock cycles (RTN3-0 = 0000)
Operation clock division ratio: 1 Division
fosc = 60 Hz × (0 + 16) clock × 1 division × (160+16) lines = 169 (KHz)

In this case, the R-C oscillation frequency becomes 169 KHz. The external resistance value of the R-C oscillator must be adjusted so that the frequency of internal R-C oscillator is equal to 169 KHz. The display duty can be changed by the partial display with the same frequency setting as above.

5.4 γ-Correction Function

The FGD0801 incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

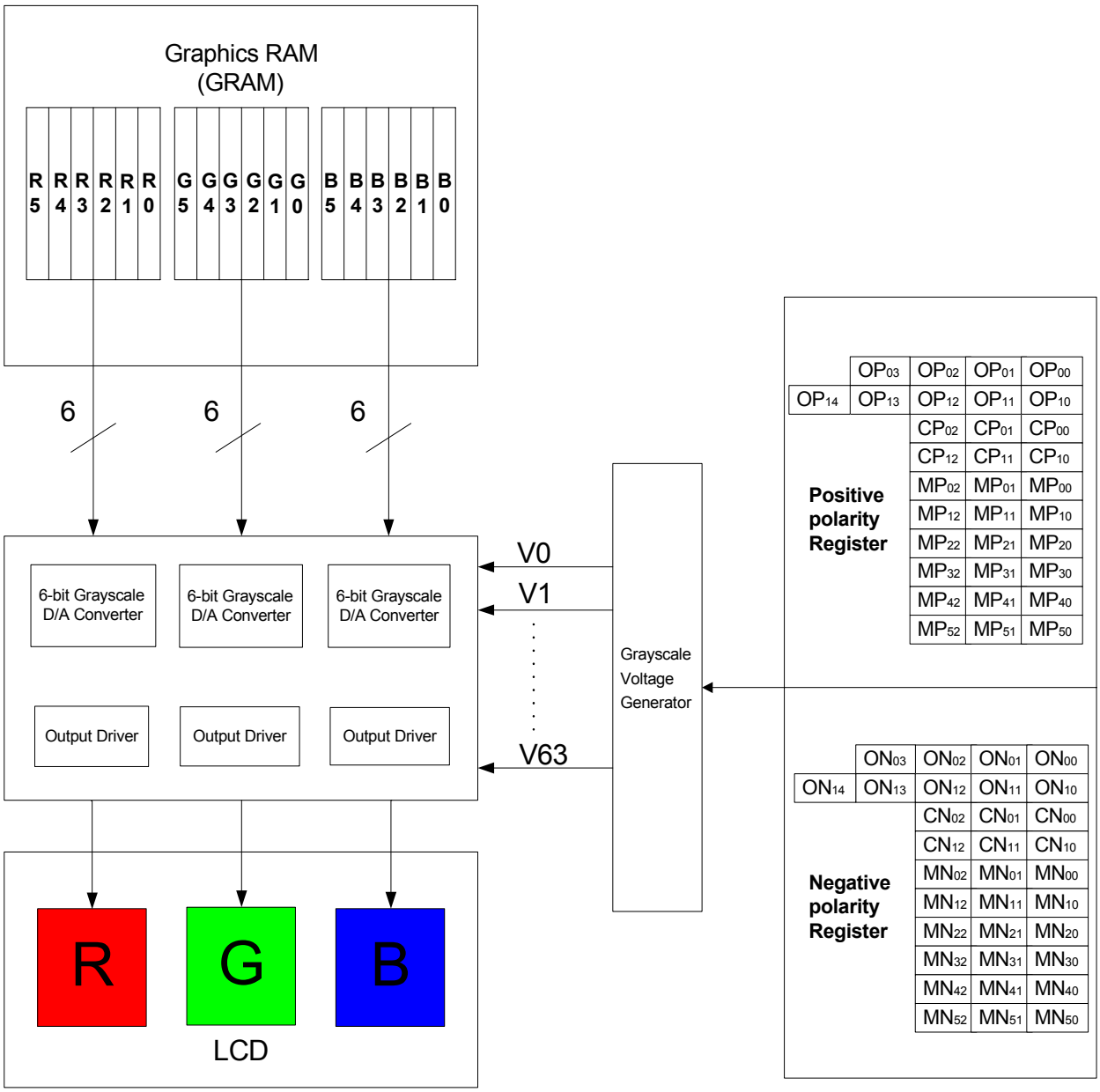


Figure 52 Grayscale Control

Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0～V63) can be generated from grayscale amplifier for LCD panel used.

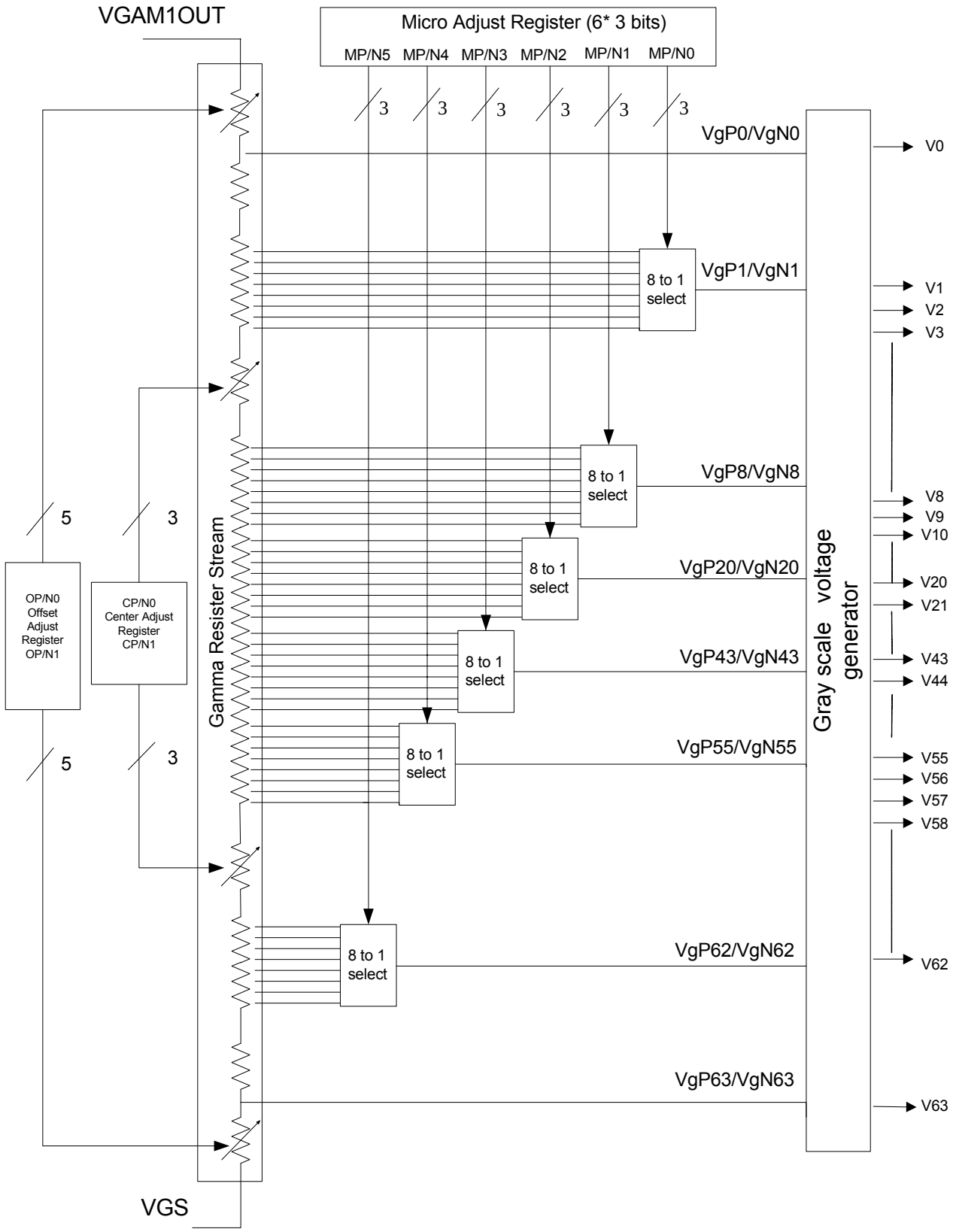


Figure 53 Structure of Grayscale Voltage Generator

Gamma-Characteristics Adjustment Register

This FGD0801 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the offset, center and micro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

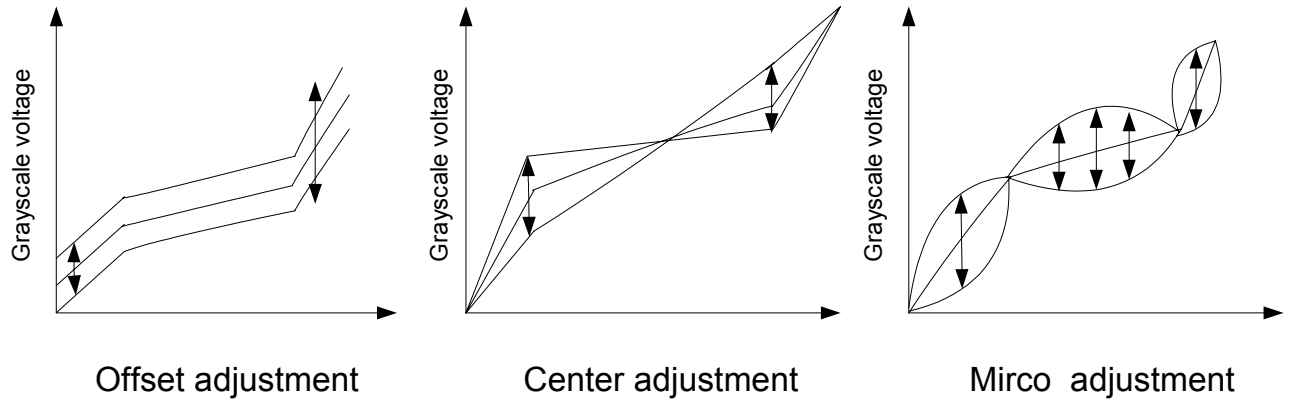


Figure 54 γ-Correction Register

1) Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resistors in the top and bottom of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

2) Center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

3) Micro adjustment registers

The gamma micro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8 to 1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output VgP/N (1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1) for center adjustment
Micro Adjustment	MP0 2-0	MN0 2-0	8 to 1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8 to 1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8 to 1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8 to 1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8 to 1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8 to 1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment

Table 14 Gamma-Adjustment Registers

Gamma resistor stream and 8 to 1 Selector

The block consists of two gamma resistor streams, one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages VgP/N (0,1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

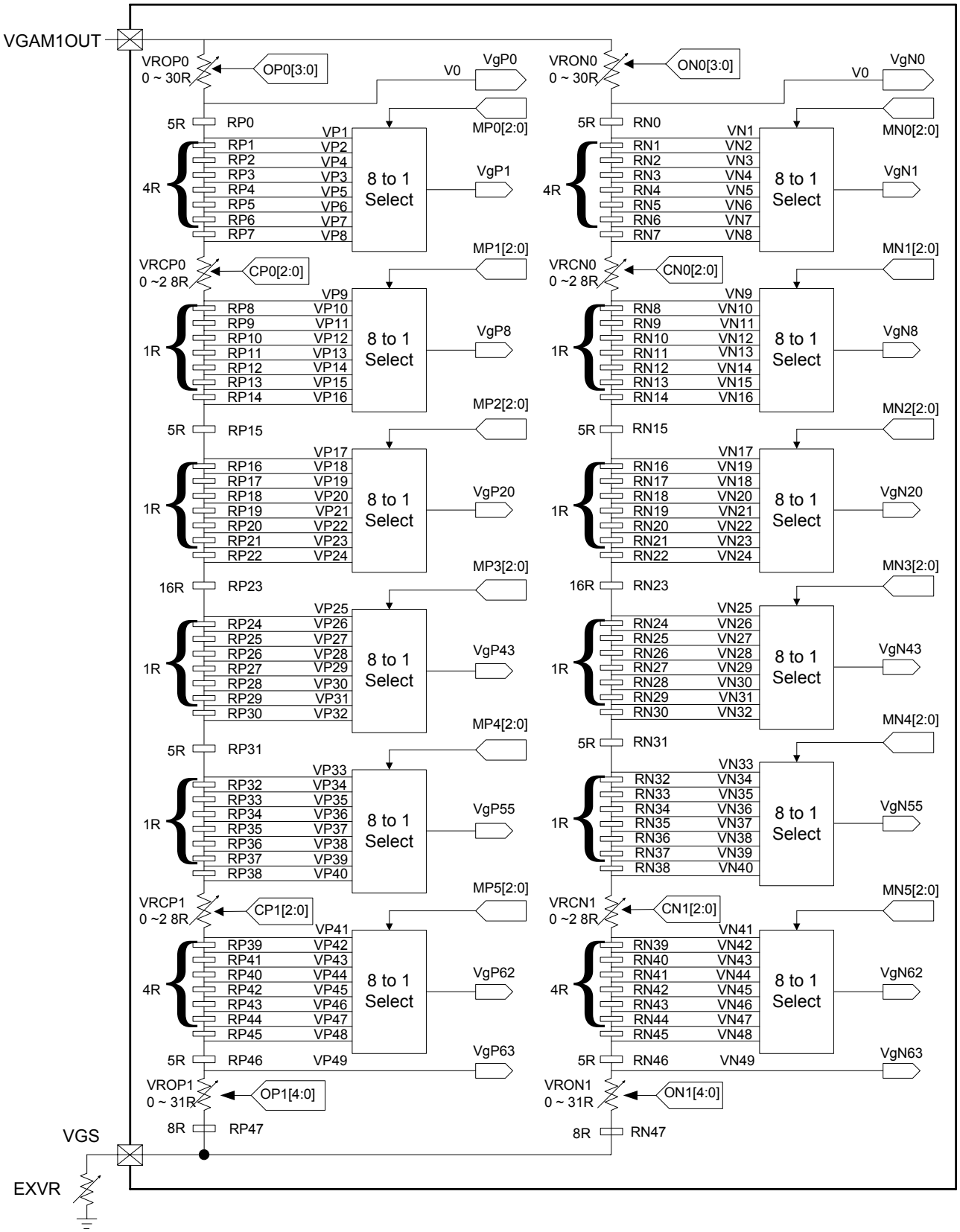


Figure 55 Gamma Resistor Stream and Gamma Reference Voltage

Variable resistor

There are two types of variable resistors, one is for center adjustment, and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment and offset adjustment registers. Their relationships are shown below.

Value in Register	Resistance
O(P/N)0 3-0	VRO(P/N)0
0000	0R
0001	2R
0010	4R
-	-
-	-
1101	26R
1110	28R
1111	30R

Value in Register	Resistance
O(P/N)1 4-0	VRO(P/N)1
00000	0R
00001	1R
00010	2R
-	-
-	-
11101	29R
11110	30R
11111	31R

Value in Register	Resistance
C(P/N)0/1 2-0	VRC(P/N)1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 15 Offset Adjustment 0, Offset Adjustment 1, Center Adjustment

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resistor stream. It outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in micro adjustment register. These six 8 to 1 selectors and the relationship are shown below.

Value in Register	Voltage level					
M(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 8	Vg(P/N) 20	Vg(P/N) 43	V(P/N) 55	V(P/N) 62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 16 Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas

Reference Voltage	Micro Adjustment Value	Formula	Pin
VgP0	----	VGAM1OUT-VD*VROP0 /sumRP	VP0
VgP1	MP0 2-0=000	VGAM1OUT-VD((VROP0+5R) /sumRP	VP1
	MP0 2-0=001	VGAM1OUT-VD((VROP0+9R) /sumRP	VP2
	MP0 2-0=010	VGAM1OUT-VD((VROP0+13R) /sumRP	VP3
	MP0 2-0=011	VGAM1OUT-VD((VROP0+17R) /sumRP	VP4
	MP0 2-0=100	VGAM1OUT-VD((VROP0+21R) /sumRP	VP5
	MP0 2-0=101	VGAM1OUT-VD((VROP0+25R) /sumRP	VP6
	MP0 2-0=110	VGAM1OUT-VD((VROP0+29R) /sumRP	VP7
	MP0 2-0=111	VGAM1OUT-VD((VROP0+33R) /sumRP	VP8
VgP8	MP1 2-0=000	VGAM1OUT-VD((VROP0+33R+VRCP0) /sumRP	VP9
	MP1 2-0=001	VGAM1OUT-VD((VROP0+34R+VRCP0) /sumRP	VP10
	MP1 2-0=010	VGAM1OUT-VD((VROP0+35R+VRCP0) /sumRP	VP11
	MP1 2-0=011	VGAM1OUT-VD((VROP0+36R+VRCP0) /sumRP	VP12
	MP1 2-0=100	VGAM1OUT-VD((VROP0+37R+VRCP0) /sumRP	VP13
	MP1 2-0=101	VGAM1OUT-VD((VROP0+38R+VRCP0) /sumRP	VP14
	MP1 2-0=110	VGAM1OUT-VD((VROP0+39R+VRCP0) /sumRP	VP15
	MP1 2-0=111	VGAM1OUT-VD((VROP0+40R+VRCP0) /sumRP	VP16
VgP20	MP2 2-0=000	VGAM1OUT-VD((VROP0+45R+VRCP0) /sumRP	VP17
	MP2 2-0=001	VGAM1OUT-VD((VROP0+46R+VRCP0) /sumRP	VP18
	MP2 2-0=010	VGAM1OUT-VD((VROP0+47R+VRCP0) /sumRP	VP19
	MP2 2-0=011	VGAM1OUT-VD((VROP0+48R+VRCP0) /sumRP	VP20
	MP2 2-0=100	VGAM1OUT-VD((VROP0+49R+VRCP0) /sumRP	VP21
	MP2 2-0=101	VGAM1OUT-VD((VROP0+50R+VRCP0) /sumRP	VP22
	MP2 2-0=110	VGAM1OUT-VD((VROP0+51R+VRCP0) /sumRP	VP23
	MP2 2-0=111	VGAM1OUT-VD((VROP0+52R+VRCP0) /sumRP	VP24
VgP43	MP3 2-0=000	VGAM1OUT-VD((VROP0+68R+VRCP0) /sumRP	VP25
	MP3 2-0=001	VGAM1OUT-VD((VROP0+69R+VRCP0) /sumRP	VP26
	MP3 2-0=010	VGAM1OUT-VD((VROP0+70R+VRCP0) /sumRP	VP27
	MP3 2-0=011	VGAM1OUT-VD((VROP0+71R+VRCP0) /sumRP	VP28
	MP3 2-0=100	VGAM1OUT-VD((VROP0+72R+VRCP0) /sumRP	VP29
	MP3 2-0=101	VGAM1OUT-VD((VROP0+73R+VRCP0) /sumRP	VP30
	MP3 2-0=110	VGAM1OUT-VD((VROP0+74R+VRCP0) /sumRP	VP31
	MP3 2-0=111	VGAM1OUT-VD((VROP0+75R+VRCP0) /sumRP	VP32
VgP55	MP4 2-0=000	VGAM1OUT-VD((VROP0+80R+VRCP0) /sumRP	VP33
	MP4 2-0=001	VGAM1OUT-VD((VROP0+81R+VRCP0) /sumRP	VP34
	MP4 2-0=010	VGAM1OUT-VD((VROP0+82R+VRCP0) /sumRP	VP35
	MP4 2-0=011	VGAM1OUT-VD((VROP0+83R+VRCP0) /sumRP	VP36
	MP4 2-0=100	VGAM1OUT-VD((VROP0+84R+VRCP0) /sumRP	VP37
	MP4 2-0=101	VGAM1OUT-VD((VROP0+85R+VRCP0) /sumRP	VP38
	MP4 2-0=110	VGAM1OUT-VD((VROP0+86R+VRCP0) /sumRP	VP39
	MP4 2-0=111	VGAM1OUT-VD((VROP0+87R+VRCP0) /sumRP	VP40
VgP62	MP5 2-0=000	VGAM1OUT-VD((VROP0+87R+VRCP0+VRCP1) /sumRP	VP41
	MP5 2-0=001	VGAM1OUT-VD((VROP0+91R+VRCP0+VRCP1) /sumRP	VP42
	MP5 2-0=010	VGAM1OUT-VD((VROP0+95R+VRCP0+VRCP1) /sumRP	VP43
	MP5 2-0=011	VGAM1OUT-VD((VROP0+99R+VRCP0+VRCP1) /sumRP	VP44
	MP5 2-0=100	VGAM1OUT-VD((VROP0+103R+VRCP0+VRCP1) /sumRP	VP45
	MP5 2-0=101	VGAM1OUT-VD((VROP0+107R+VRCP0+VRCP1) /sumRP	VP46
	MP5 2-0=110	VGAM1OUT-VD((VROP0+111R+VRCP0+VRCP1) /sumRP	VP47
	MP5 2-0=111	VGAM1OUT-VD((VROP0+115R+VRCP0+VRCP1) /sumRP	VP48
VgP63	----	VGAM1OUT-VD((VROP0+120R+VRCP0+VRCP1) /sumRP	VP49

Table 17 Voltage Calculation Formula (Positive Polarity)

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD=(VGAM1OUT-VGS)

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VgP0	V32	V43+(V20-V43)*(11/23)
V1	VgP1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VgP8	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VgP43
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VgP20	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VgP55
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VgP62
V31	V43+(V20-V43)*(12/23)	V63	VgP63

Table 18 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Note: The following relationship should be retained.
VLCD - V0 > 0.5V
VLCD - V8 > 1.1V
V55 - VSSD> 1.1V

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	----	VGAM1OUT-VD*VRON0 /sumRN	VN0
VgN1	MN0 2-0=000	VGAM1OUT-VD((VRON0+5R) /sumRN	VN1
	MN0 2-0=001	VGAM1OUT-VD((VRON0+9R) /sumRN	VN2
	MN0 2-0=010	VGAM1OUT-VD((VRON0+13R) /sumRN	VN3
	MN0 2-0=011	VGAM1OUT-VD((VRON0+17R) /sumRN	VN4
	MN0 2-0=100	VGAM1OUT-VD((VRON0+21R) /sumRN	VN5
	MN0 2-0=101	VGAM1OUT-VD((VRON0+25R) /sumRN	VN6
	MN0 2-0=110	VGAM1OUT-VD((VRON0+29R) /sumRN	VN7
	MN0 2-0=111	VGAM1OUT-VD((VRON0+33R) /sumRN	VN8
VgN8	MN1 2-0=000	VGAM1OUT-VD((VRON0+33R+VRCN0) /sumRN	VN9
	MN1 2-0=001	VGAM1OUT-VD((VRON0+34R+VRCN0) /sumRN	VN10
	MN1 2-0=010	VGAM1OUT-VD((VRON0+35R+VRCN0) /sumRN	VN11
	MN1 2-0=011	VGAM1OUT-VD((VRON0+36R+VRCN0) /sumRN	VN12
	MN1 2-0=100	VGAM1OUT-VD((VRON0+37R+VRCN0) /sumRN	VN13
	MN1 2-0=101	VGAM1OUT-VD((VRON0+38R+VRCN0) /sumRN	VN14
	MN1 2-0=110	VGAM1OUT-VD((VRON0+39R+VRCN0) /sumRN	VN15
	MN1 2-0=111	VGAM1OUT-VD((VRON0+40R+VRCN0) /sumRN	VN16
VgN20	MN2 2-0=000	VGAM1OUT-VD((VRON0+45R+VRCN0) /sumRN	VN17
	MN2 2-0=001	VGAM1OUT-VD((VRON0+46R+VRCN0) /sumRN	VN18
	MN2 2-0=010	VGAM1OUT-VD((VRON0+47R+VRCN0) /sumRN	VN19
	MN2 2-0=011	VGAM1OUT-VD((VRON0+48R+VRCN0) /sumRN	VN20
	MN2 2-0=100	VGAM1OUT-VD((VRON0+49R+VRCN0) /sumRN	VN21
	MN2 2-0=101	VGAM1OUT-VD((VRON0+50R+VRCN0) /sumRN	VN22
	MN2 2-0=110	VGAM1OUT-VD((VRON0+51R+VRCN0) /sumRN	VN23
	MN2 2-0=111	VGAM1OUT-VD((VRON0+52R+VRCN0) /sumRN	VN24
VgN43	MN3 2-0=000	VGAM1OUT-VD((VRON0+68R+VRCN0) /sumRN	VN25
	MN3 2-0=001	VGAM1OUT-VD((VRON0+69R+VRCN0) /sumRN	VN26
	MN3 2-0=010	VGAM1OUT-VD((VRON0+70R+VRCN0) /sumRN	VN27
	MN3 2-0=011	VGAM1OUT-VD((VRON0+71R+VRCN0) /sumRN	VN28
	MN3 2-0=100	VGAM1OUT-VD((VRON0+72R+VRCN0) /sumRN	VN29
	MN3 2-0=101	VGAM1OUT-VD((VRON0+73R+VRCN0) /sumRN	VN30
	MN3 2-0=110	VGAM1OUT-VD((VRON0+74R+VRCN0) /sumRN	VN31
	MN3 2-0=111	VGAM1OUT-VD((VRON0+75R+VRCN0) /sumRN	VN32
VgN55	MN4 2-0=000	VGAM1OUT-VD((VRON0+80R+VRCN0) /sumRN	VN33
	MN4 2-0=001	VGAM1OUT-VD((VRON0+81R+VRCN0) /sumRN	VN34
	MN4 2-0=010	VGAM1OUT-VD((VRON0+82R+VRCN0) /sumRN	VN35
	MN4 2-0=011	VGAM1OUT-VD((VRON0+83R+VRCN0) /sumRN	VN36
	MN4 2-0=100	VGAM1OUT-VD((VRON0+84R+VRCN0) /sumRN	VN37
	MN4 2-0=101	VGAM1OUT-VD((VRON0+85R+VRCN0) /sumRN	VN38
	MN4 2-0=110	VGAM1OUT-VD((VRON0+86R+VRCN0) /sumRN	VN39
	MN4 2-0=111	VGAM1OUT-VD((VRON0+87R+VRCN0) /sumRN	VN40
VgN62	MN5 2-0=000	VGAM1OUT-VD((VRON0+87R+VRCN0+VRCN1) /sumRN	VN41
	MN5 2-0=001	VGAM1OUT-VD((VRON0+91R+VRCN0+VRCN1) /sumRN	VN42
	MN5 2-0=010	VGAM1OUT-VD((VRON0+95R+VRCN0+VRCN1) /sumRN	VN43
	MN5 2-0=011	VGAM1OUT-VD((VRON0+99R+VRCN0+VRCN1) /sumRN	VN44
	MN5 2-0=100	VGAM1OUT-VD((VRON0+103R+VRCN0+VRCN1) /sumRN	VN45
	MN5 2-0=101	VGAM1OUT-VD((VRON0+107R+VRCN0+VRCN1) /sumRN	VN46
	MN5 2-0=110	VGAM1OUT-VD((VRON0+111R+VRCN0+VRCN1) /sumRN	VN47
	MN5 2-0=111	VGAM1OUT-VD((VRON0+115R+VRCN0+VRCN1) /sumRN	VN48
VgN63	----	VGAM1OUT-VD((VRON0+120R+VRCN0+VRCN1) /sumRN	VN49

Table 19 Voltage Calculation Formula (Negative Polarity)

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD = (VGAM1OUT-VGS)

Grayscale Voltage	Formula
V0	VgN0
V1	VgN1
V2	V8+(V1-V3)*(8/24)
V3	V8+(V1-V8)*(450/800)
V4	V8+(V3-V8)*(16/24)
V5	V8+(V3-V8)*(12/24)
V6	V8+(V3-V8)*(8/24)
V7	V8+(V3-V8)*(4/24)
V8	VgN8
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VgN20
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale Voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VgN43
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VgN55
V56	V62+(V55-V60)*(20/24)
V57	V62+(V55-V60)*(16/24)
V58	V62+(V55-V60)*(12/24)
V59	V62+(V55-V60)*(8/24)
V60	V62+(V55-V62)*(350/800)
V61	V62+(V60-V62)*(16/24)
V62	VgN62
V63	VgN63

Table 20 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

Note: The following relationship should be retained.

VLCD - V0 > 0.5V

VLCD - V8 > 1.1V

V55 - VSSD> 1.1V

Relationship between GRAM Data and Output Level

GRAM Data Set-up RGB	Selected Grayscale	
	N	P
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48

GRAM Data Set-up RGB	Selected Grayscale	
	N	P
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35
011101	V29	V34
011110	V30	V33
011111	V31	V32

GRAM Data Set-up RGB	Selected Grayscale	
	N	P
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16

GRAM Data Set-up RGB	Selected Grayscale	
	N	P
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

Table 21 GRAM Data and Grayscale Level

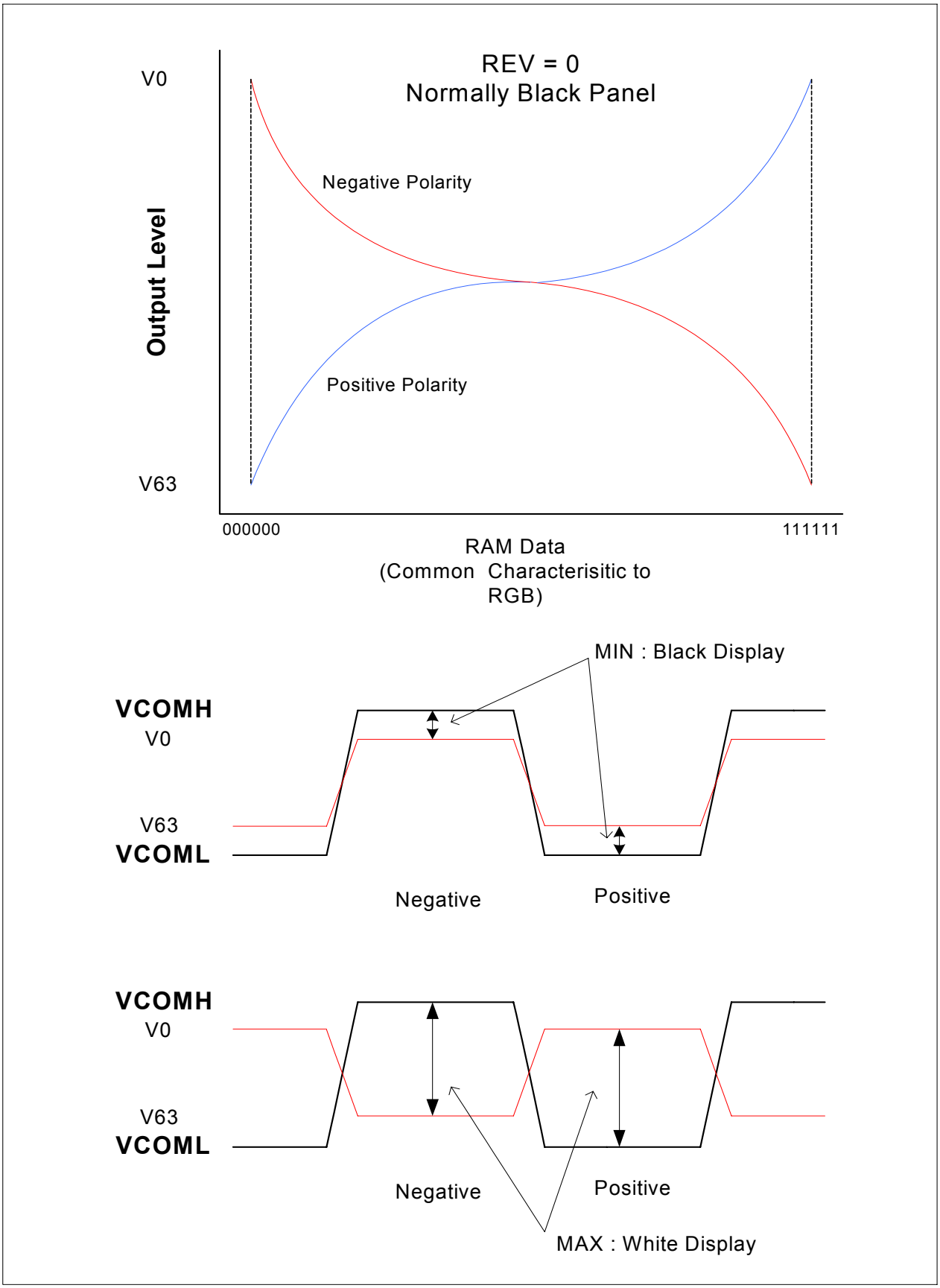


Figure 56 Relationship between RAM Data, Source Output and VCOM(REV = 0)

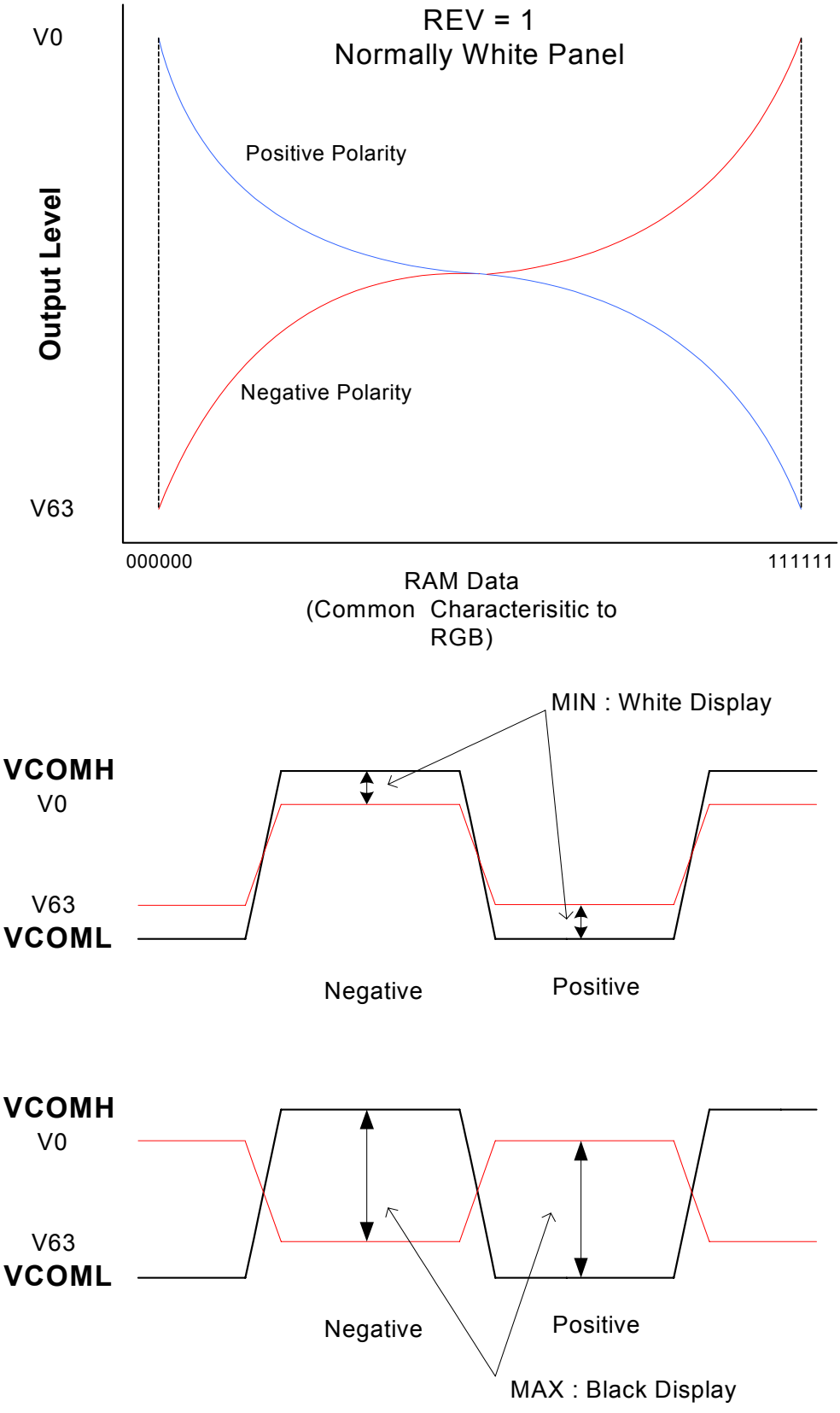


Figure 57 Relationship between RAM Data, Source output and VCOM(REV = 1)

5.5 Oscillator

The FGD0801 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor (R_f). The oscillation frequency is changed according to the external resistance value, wiring length, or operating power supply voltage. If R_f is increased or power supply voltage is decreased, the oscillation frequency decreases.

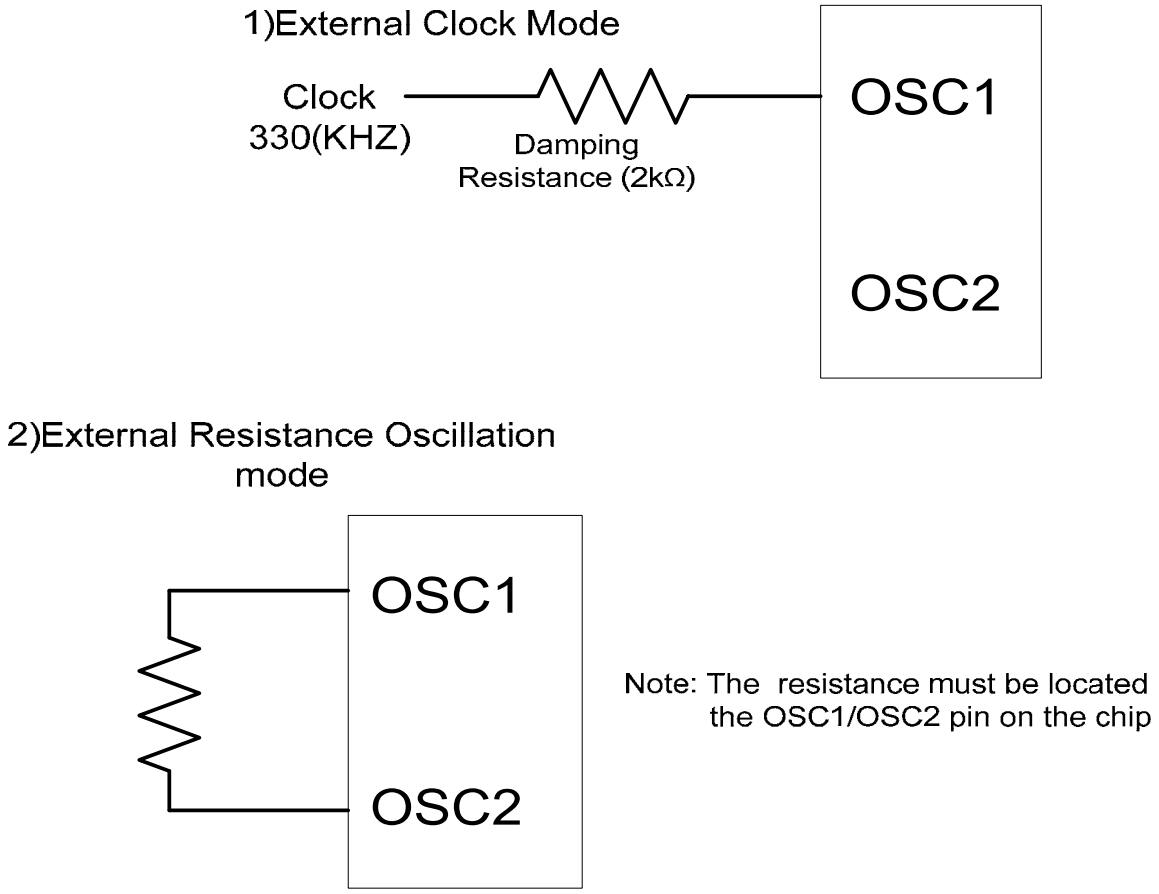


Figure 58 Oscillation Circuit

External Resistance	R-C Oscillation Frequency: fosc (KHz)			
R_f	VCC=2.4V	VCC=2.8V	VCC=3.0V	VCC=3.3V
10kΩ	712.9KHz	795.2KHz	830.2KHz	876.8KHz
20kΩ	466.6KHz	503.7KHz	520.3KHz	541.3KHz
30kΩ	347.9KHz	371.5KHz	381.6KHz	394.5KHz
50kΩ	232.2KHz	245.7KHz	251.1KHz	257.7KHz
70kΩ	175.4KHz	184.7KHz	188.1KHz	192.3KHz

Table 22 External Resistance Value and RC Oscillation Frequency (Temporally Define)

6. Registers

The FGD0801 adopts 18-bit bus architecture to interface to high-performance micro -computer. The FGD0801 starts internal processing when the control information sent via 18-/16-/9-/8-bit ports is stored in the index register (IR) and the control register (CR). Since the internal operation of the FGD0801 is controlled by the signals sent from the microcomputer, register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signals (DB15 to DB0) are called instruction. The FGD0801 accesses the internal GRAM in units of 18 bits.

The instructions of the FGD0801 are categorized into the following 8 groups.

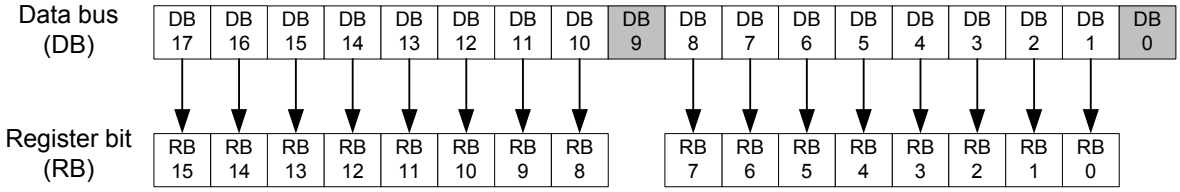
- Select the index
- Read back the status
- Control the display functions
- Control power management and save power function
- Process or operate the graphics data
- Set internal GRAM addresses for partial data uDBating
- Set grayscale level for the internal embedded grayscale gamma adjustment

The following specify the explanation of registers such as register format and bit function.

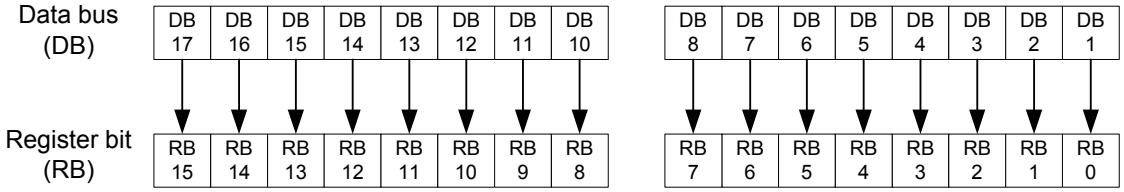
Table 23 List Table of Registers Setting

NO.	Register	W/R	RS	High								Low							
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
IR	Inedex	W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R00H	Start oscillator	W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_EN(1)
	Device code read	R	1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	1	0
R01H	Driver output control	W	1	0	0	0	0	0	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (0)	NL2 (0)	NL1 (1)	NL0 (1)
R02H	LCD AC driving control	W	1	0	0	0	0	FLD1 (0)	FLD0 (1)	B/C (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)
R03H	Power control (1)	W	1	0	0	0	0	0	BT2 (0)	BT1 (0)	BT0 (0)	DC02 (0)	DC01 (0)	DC00 (0)	AP2 (0)	AP1 (0)	AP0 (0)	SLP (0)	STB (0)
R05H	Entry mode	W	1		0	0	BGR (0)	0	0	0	0	0	0	ID1 (1)	ID0 (1)	AM (0)	0	0	0
R07H	Display control(1)	W	1	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	GON (0)	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)
R08H	Display control(2)	W	1	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	FP3 (0)	FP2 (0)	FP1 (1)	FP0 (1)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)	BP3 (0)	BP2 (0)	BP1 (1)	BP0 (1)
R09H	Power control (2)	W	1	0	0	0	0	0	0	DCM1 (0)	DCM0 (0)	DC12 (0)	DC11 (0)	DC10 (0)	0	DK (1)	SAP2 (1)	SAP1 (0)	SAP0 (0)
R0Ah	External display control	W	1	TRI (0)	DFM1 (0)	DFM0 (0)	0	0	PTG1 (0)	PTG0 (0)	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
R0BH	Frame cycle control	W	1	GD1 (0)	GD0 (0)	SDT1 (0)	SDT0 (0)	CE1 (0)	CE0 (0)	DIV1 (0)	DIV0 (0)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)
R0CH	Power control (3)	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2 (0)	VC1 (0)	VC0 (0)
R0DH	Power control (4)	W	1	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
R0EH	Power control (5)	W	1	0	0	VCOMG(0)	VDV4(0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2(0)	VCM1 0)	VCM0 (0)
R0FH	Gate scan start position	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
R11H	Vertical scroll control	W	1	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
R14H	First screen position	W	1	SE17 (1)	SE16 (0)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)
R15H	Second screen position	W	1	SE27 (1)	SE26 (0)	SE25 (0)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)
R16H	Horizontal RAM address	W	1	HEA7 (0)	HEA6 (1)	HEA5 (1)	HEA4 (1)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
R17H	Vertical RAM address	W	1	VEA7 (1)	VEA6 (0)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	VSA7(0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
R21H	RAM address set	W	1	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
R22H	Read/Write GRAM	R	1	WD17-0								RD17-0							
R30H	Gamma control(1)	W	1	0	0	0	0	0	MP12 (0)	MP11 (0)	MP10 (0)	0	0	0	0	0	MP02 (0)	MP01 (0)	MP00 (0)
R31H	Gamma control(2)	W	1	0	0	0	0	0	MP32 (0)	MP31 (0)	MP30 (0)	0	0	0	0	0	MP22 (0)	MP21 (0)	MP20 (0)
R32H	Gamma control(3)	W	1	0	0	0	0	0	MP52 (0)	MP51 (0)	MP50 (0)	0	0	0	0	0	MP42 (0)	MP41 (0)	MP40 (0)
R33H	Gamma control(4)	W	1	0	0	0	0	0	CP12 (0)	CP11 (0)	CP10 (0)	0	0	0	0	0	CP02 (0)	CP01 (0)	CP00 (0)
R34H	Gamma control(5)	W	1	0	0	0	0	0	MN12 (0)	MN11 (0)	MN10 (0)	0	0	0	0	0	MN02 (0)	MN01 (0)	MN00 (0)
R35H	Gamma control(6)	W	1	0	0	0	0	0	MN32 (0)	MN31 (0)	MN30 (0)	0	0	0	0	0	MN22 (0)	MN21 (0)	MN20 (0)
R36H	Gamma control(7)	W	1	0	0	0	0	0	MN52 (0)	MN51 (0)	MN50 (0)	0	0	0	0	0	MN42 (0)	MN41 (0)	MN40 (0)
R37H	Gamma control(8)	W	1	0	0	0	0	0	CN12 (0)	CN11 (0)	CN10 (0)	0	0	0	0	0	CN02 (0)	CN01 (0)	CN00 (0)
R3AH	Gamma control(9)	W	1	0	0	0	OP14 (0)	OP13 (0)	OP12 (0)	OP11 (0)	OP10 (0)	0	0	0	0	OP03 (0)	OP02 (0)	OP01 (0)	OP00 (0)
R3BH	Gamma control(10)	W	1	0	0	0	ON14 (0)	ON13 (0)	ON12 (0)	ON11 (0)	ON10 (0)	0	0	0	0	ON03 (0)	ON02 (0)	ON01 (0)	ON00 (0)

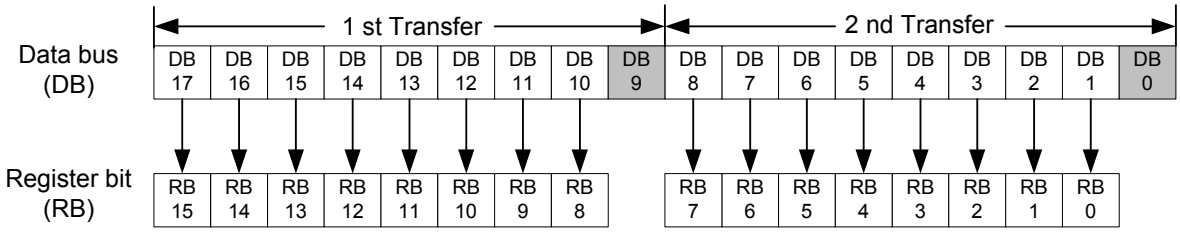
80-system 18-bit bus interface



80-system 16-bit bus interface



80-system 9-bit bus interface



80-system 8-bit bus interface/Serial Data Transfer Interface (2/3 transmission)

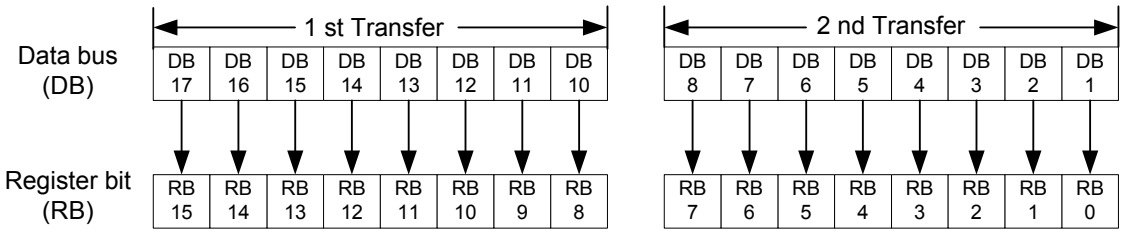


Figure 59 80 System interface mode

6.1 Index Register (IR)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 60 Index Register (IR)

ID6-0: Index register (IR) specifies Index of the register from R00h to R4Fh. It sets the register number (ID6-0) in the range from 0000000b to 1111111b in binary form.

6.2 Status Read Register (SR)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 61 Status Read Register (SR)

Status Read Register for reading the internal status of the FGD0801.

L7-0: Indicate the position of driving line, where the liquid crystal display is driven at resent.

6.3 Start Oscillation Register (R00H)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_EN
R	1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	1	0

Figure 62 Start Oscillation Register (R00H)

Start Oscillation Register restarts the oscillator from the suspend state at the standby mode. After setting this register, and wait at least 10 ms for oscillation stabilizing before setting the next register.

OSC_EN: When OSC_EN = 1, oscillator is enabled;
When OSC_EN = 0, oscillator is disabled.

When the read commend is issued, 6812h is read.

6.4 Driver Output Control Register (R01H)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 63 Driver output Control Register (R01H)

NL4–0: Specify the number of scan lines for the LCD driver and it can be adjusted by every 8 lines.

NL4	NL3	NL2	NL1	NL0	Gate Driver Used	Number of Scan Line	Display Size
0	0	0	0	0	Ignore	Ignore	Ignore
0	0	0	0	1	G1-G16	16	386*16 dots
0	0	0	1	0	G1-G24	24	386*24 dots
0	0	0	1	1	G1-G32	32	386*32 dots
0	0	1	0	0	G1-G40	40	386*40 dots
0	0	1	0	1	G1-G48	48	386*48 dots
0	0	1	1	0	G1-G56	56	386*56 dots
0	0	1	1	1	G1-G64	64	386*64 dots
0	1	0	0	0	G1-G72	72	386*72 dots
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	0	0	G1-G136	136	386*136 dots
1	0	0	0	1	G1-G144	144	386*144 dots
1	0	0	1	0	G1-G152	152	386*152 dots
1	0	0	1	1	G1-G160	160	386*160 dots
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	G1-G160	160	386*160 dots

Table 24 NL bits and Scan Line

SS: The source driver output shift direction selected.
When SS=0, the shift direction is from S1 to S384.;
When SS = 1, the shift direction is from S384 to S1.

GS: Specify the shift direction of gate driver output.
When GS = 0, the shift direction is from G1 to G160;
When GS = 1, the shift direction is from G160 to G1.

SM: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin.

6.5 LCD Driving Waveform Control Register (R02h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 64 LCD-Driving-Waveform Control Register (R02h)

NW5–0: Specify the number of n lines that will alternate POL signal when B/C = 1. The inversion is occurred every n + 1 line, and the 1st to the 64th lines can be selected.

EOR: EOR=1 will force POL signal alternate at the beginning of a frame in n-line inversion driving mode (B/C=1), no matter the last interval of POL signal is over or not in last frame. Therefore, EOR bit is used when the POL signal is not completely alternated in some number of drive lines in LCD display area. For details, see the “N-line Inversion LCD Drive” section.

B/C: When B/C = 0, POL signal alternates in every frame for LCD drive. When B/C = 1, POL signal alternates in each n line specified by bits EOR and NW5–NW0 in the LCD-driving-waveform control register. For details, see the “N-line Inversion LCD Drive” section.

FLD1-0: Set the number of n field for interlaced driving mode. For details, see the “Interlaced driving function section”.

FLD1	FLD0	Number of fields
0	0	Ignore
0	1	1 field
1	0	Ignore
1	1	3 fields

Table 25 FLD bits and interlaced field

6.6 Power control Register 1 (R03h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	BT2	BT1	BT0	DC02	DC01	DC00	AP2	AP1	AP0	SLP	STB

Figure 65 Power Control Register 1 (R03h)

STB: When STB = “1”, the FGD0801 into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. Anyway, have not any external clock are supplied. During the standby mode, only the following process can be executed.

a. Exit the Standby mode (STB = “0”)

b. Start the oscillation

Within the standby mode, the GRAM data and register content may be lost. For preventing this, they have to set again after the standby mode is exited.

SLP: When SLP = 1, the FGD0801 into the sleep mode, where the internal display operations are suspend except for the R-C oscillator, thus the current consumption can be reduced. Within the sleep mode, the GRAM data and register content cannot be accessed although they are retained.

AP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption.

During no display operation, when AP2–0 = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	Ignore
0	1	0	0.5
0	1	1	0.75
1	0	0	1
1	0	1	1.25
1	1	0	1.5
1	1	1	Ignore

Table 26 AP Bits and amount of current in Operational Amplifier

BT2-0: Switch the output factor for step-up circuit. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

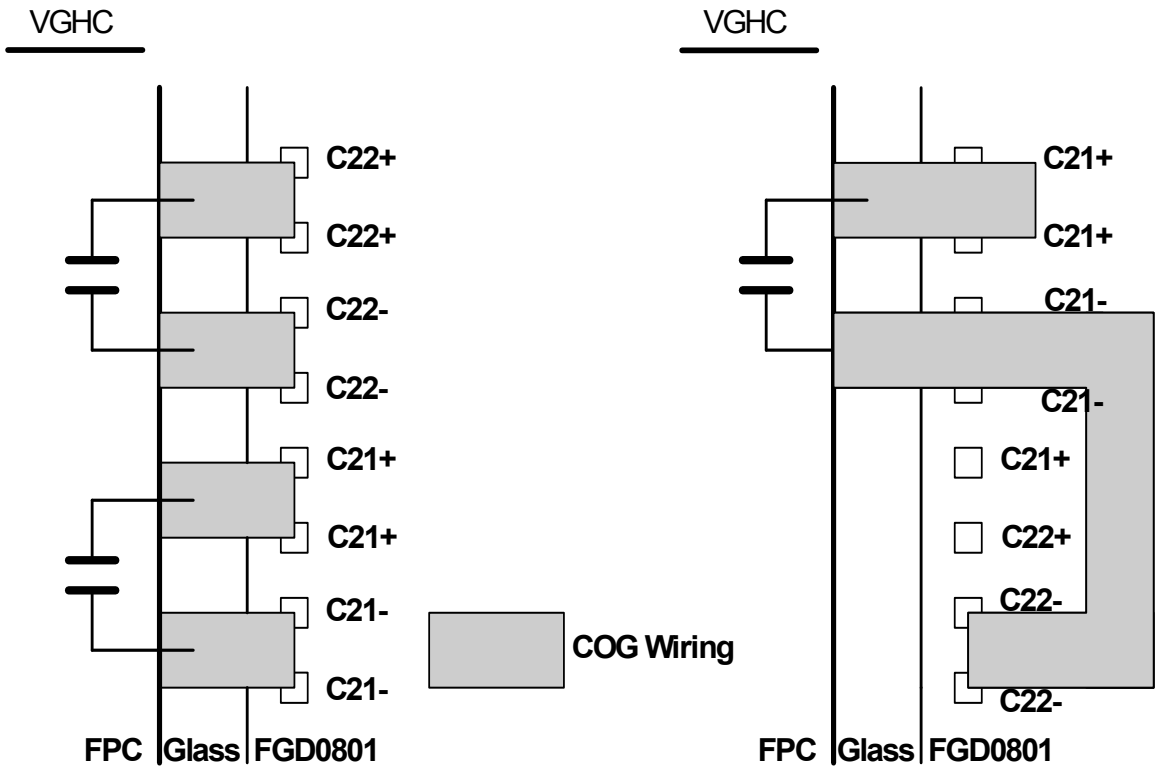


Figure 66 Different Connection of C22 Capacitor

BT2	BT1	BT0	VLCD	VCL	VGH	VGL	Capacitor connection pins
0	0	0	2xVCI1	-1xVCI1	6xVCI1	-5xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B, C22 A/B
0	0	1	2xVCI1	-1xVCI1	6xVCI1	-4xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B, C22 A/B
0	1	0	2xVCI1	-1xVCI1	6xVCI1	-3xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B, C22 A/B
0	1	1	2xVCI1	-1xVCI1	5xVCI1	-5xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B, C22 A/B
1	0	0	2xVCI1	-1xVCI1	5xVCI1	-4xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B, C22 A/B
1	0	1	2xVCI1	-1xVCI1	5xVCI1	-3xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B, C22 A/B
1	1	0	2xVCI1	-1xVCI1	4xVCI1	-4xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B, C22 A/B
1	1	1	-	-	-	-	Setting Disable

Table 27 BT Bits and VLCD, VGH and VGL Outputs

BT2	BT1	BT0	VLCD	VCL	VGH	VGL	Capacitor connection pins
0	0	0	2xVCI1	-1xVCI1	4xVCI1	-3xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B,
0	0	1	2xVCI1	-1xVCI1	4xVCI1	-2xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B,
0	1	0	2xVCI1	-1xVCI1	4xVCI1	-1xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B,
0	1	1	2xVCI1	-1xVCI1	3xVCI1	-3xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B,
1	0	0	2xVCI1	-1xVCI1	3xVCI1	-2xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B,
1	0	1	2xVCI1	-1xVCI1	3xVCI1	-1xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B,
1	1	0	2xVCI1	-1xVCI1	2xVCI1	-2xVCI1	VLCD, VGH, VGL, VCL,C11 A/B,C12A/B,C21A/B, C22 A/B
1	1	1	-	-	-	-	Setting Disable

Table 28 BT Bits and VLCD, VGH and VGL Outputs (without CapacitoC22)

Note: The factors of step-up for VGH are derived from VCI1 when VLCD and VCI2 are shorted. The conditions of VLCD 5.5V, ≦ VCL ≦ -3.3V, VGH 16.5V, and VGL ≦ ≦-16.5V must be satisfied.

DC02–00: Set the operating frequency for the step-up circuit 1. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DC02	DC01	DC00	Operation Frequency of Step-up Circuit 1
0	0	0	fosc / 4
0	0	1	fosc / 8
0	1	0	fosc / 16
0	1	1	fosc / 32
1	0	0	fosc / 64
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	Halted

Table 29 Operation Frequency of Step-up Circuit 1 (fdcdc1)

6.7 Entry Mode Register (R05h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	0	0	0

Figure 67 Entry Mode Register (R05h)

AM: The uDBating direction as write data to GRAM. The data will be written vertically when AM=1; the data will be written horizontally when AM=0. In case of window address range is given, data will be written to the GRAM in the range of the window address according to AM & I/D[1:0].

I/D1-0: The AC will incremented by 1 after data written to GRAM if I/D = 1; the AC will decremented by 1 after data written to GRAM if I/D=0.

The following figure depicts the Update method with I/D1-0 & AM bit.

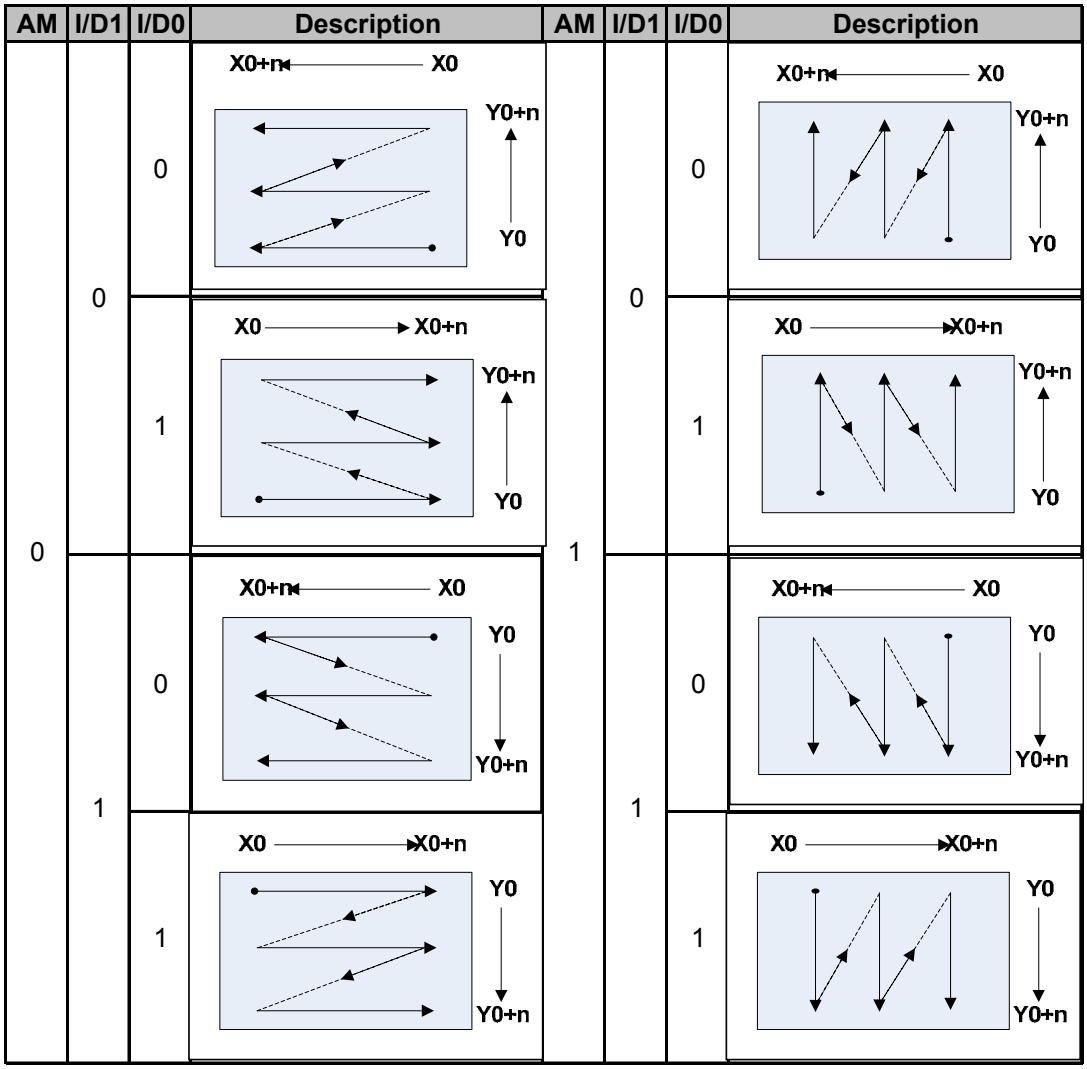


Figure 68 Address Direction Settings

BGR: The order of <R><G><B> dot color. When BGR = 1, the order sent from the MPU with expanding to 18 bits are reversed bit order from <R><G><B> order to <B><G><R> order. Setting BGR will change the bit order of (WM17-0) in the same way.

6.8 Display Control Register 1 (R07h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

Figure 69 Display Control Register 1 (R07h)

D1–0: When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the FGD0801 can control the charging current for the LCD with AC driving.

Control the display on/off while control GON and DTE. When D1–0 = 01, the internal display of the FGD0801 is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	Source Output	FGD0801 Internal Display operations	Gate-Driver Control Signals (CPV, FLM, M) (CPV, STV, POL)
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	Non-lit display	Operate	Operate
1	1	Display	Operate	Operate

Table 30 D Bits and Operation

Note: Data can be written to the GRAM from the MPU regardless of the content of D1-0.

REV: REV = 1 selects the inversion of the display of all characters and graphics. This bit allows the display of the same data on both normally-white and normally-black panels.

REV	GRAM data	Source output level							
		Display area		Non-display area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM= "L"	VCOM= "H"	VCOM= "L"	VCOM= "H"	VCOM= "L"	VCOM= "H"	VCOM= "L"	VCOM= "H"
0	18'h00000 : 18'h3FFFF	V63 : V0	V0 : V63	V63	V0	VSSD	VSSD	Hi-Z	Hi-Z
1	18'h00000 : 18'h3FFFF	V0 : V63	V63 : V0	V63	V0	VSSD	VSSD	Hi-Z	Hi-Z

Table 31 Display Control Instruction

CL: CL = 1, the display mode is set to the 8-color display mode. For details, see the section on the 8-color display mode section.

CL	Number of Display Colors
0	262,144
1	8

Table 32 CL Bit for 8-Color Display

Note: The display 262,114 colors when 18/9 bit bus interface is using, and display 65,536 colors when 16/8 bit bus interface is using.

DTE, GON: Specify the output level of gate line. VCOM level becomes VSSD when GON=0.

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

Table 33 GON and DTE bits

SPT: When SPT = 1, the 2-division LCD drive is performed so a LCD can be divided 2 split display windows. For details, see the Partial Screen Display Function section.

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st display window.
When VLE2 = 1, a vertical scroll is performed in the 2nd display window.
Vertical scrolling on the two windows cannot be controlled at the same time.

VLE1	VLE2	1st display(image)	2nd display (image)
0	0	Fixed Display	Fixed Display
1	0	Scrolled Display	Fixed Display
0	1	Fixed Display	Scrolled Display
1	1	Ignore	Ignore

Table 34 VLE Bits

PT1-0: When partial display is in use, these bits determine the source output in the non-display area. For details, see the Partial Screen Display Function section. The output on the source lines during the periods of the front and BP are also determined by PT1-0.

PT1	PT0	source output in non-display area		Gate Output in Non-Display Area	VCOM output
		Positive Polarity	Negative Polarity		
0	0	V63	V0	reference to PTG1-0	VCOMH-VCOML
0	1	V63	V0	reference to PTG1-0	VCOMH-VCOML
1	0	VSSD	VSSD	reference to PTG1-0	VCOMH-VCOML
1	1	Hi-Z	Hi-Z	reference to PTG1-0	-

Table 35 PT Bits for Source and Gate Output in Non-Display Area of Partial Display

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

6.9 Display Control Register 2 (R08h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSPL	HSPL	DPL	EPL	FP3	FP2	FP1	FP0	ISC3	ISC2	ISC1	ISC0	BP3	BP2	BP1	BP0

Figure 70 Display Control Register(2) (R08H)

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	GRAM address	Write to GRAM	Operation
0	Low	Update	Enable	Write data to DB17-0
0	High	Keep	Disable	Disable
1	Low	Keep	Disable	Disable
1	High	Update	Enable	Write data to DB17-0

Table 36 EPL bit and Enable pin

VSPL: The polarity of VSYNC pin.
When VSPL=0, the VSYNC pin is Low active.
When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin.
When HSPL=0, the HSYNC pin is Low active.
When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin.
When DPL=0, the data is read on the rising edge of DOTCLK signal.
When DPL=1, the data is read on the falling edge of DOTCLK signal.

ISC3-0: Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan cycle	f_{FLM}=60Hz
0	0	0	0	0 frame	Ignore
0	0	0	1	3 frames	50ms
0	0	1	0	5 frames	84ms
0	0	1	1	7 frames	117ms
0	1	0	0	9 frames	150ms
0	1	0	1	11 frames	184ms
0	1	1	0	13 frames	217ms
0	1	1	1	15 frames	251ms
1	0	0	0	17 frames	284ms
1	0	0	1	19 frames	317ms
1	0	1	0	21 frames	351ms
1	0	1	1	23 frames	384ms
1	1	0	0	25 frames	418ms
1	1	0	1	27 frames	451ms
1	1	1	0	29 frames	484ms
1	1	1	1	31 frames	518ms

Table 37 ISC bit setting

BP3-0: Specify the amount of scan line for back porch (BP).
FP3-0: Specify the amount of scan line for front porch (FP).

The setting value, ensure that:

BP + FP ≤ 16 lines
BP ≥ 2 lines
FP ≥ 2 lines

In external display interface mode, the BP start on the falling edge of VSYNC signal, followed by the display operation. The FP starts after driving the number of scan line set with NL4-0. After the FP, the blank period continues until the next input of the VSYNC signal.

FP3	FP2	FP1	FP0	Number of FP line	Number of BP Line
BP3	BP2	BP1	BP0		
0	0	0	0	Ignore	
0	0	0	1	Ignore	
0	0	1	0	2 lines	
0	0	1	1	3 lines	
0	1	0	0	4 lines	
0	1	0	1	5 lines	
0	1	1	0	6 lines	
0	1	1	1	7 lines	
1	0	0	0	8 lines	
1	0	0	1	9 lines	
1	0	1	0	10 lines	
1	0	1	1	11 lines	
1	1	0	0	12 lines	
1	1	0	1	13 lines	
1	1	1	0	14 lines	
1	1	1	1	Ignore	

Table 38 BP/FP bits

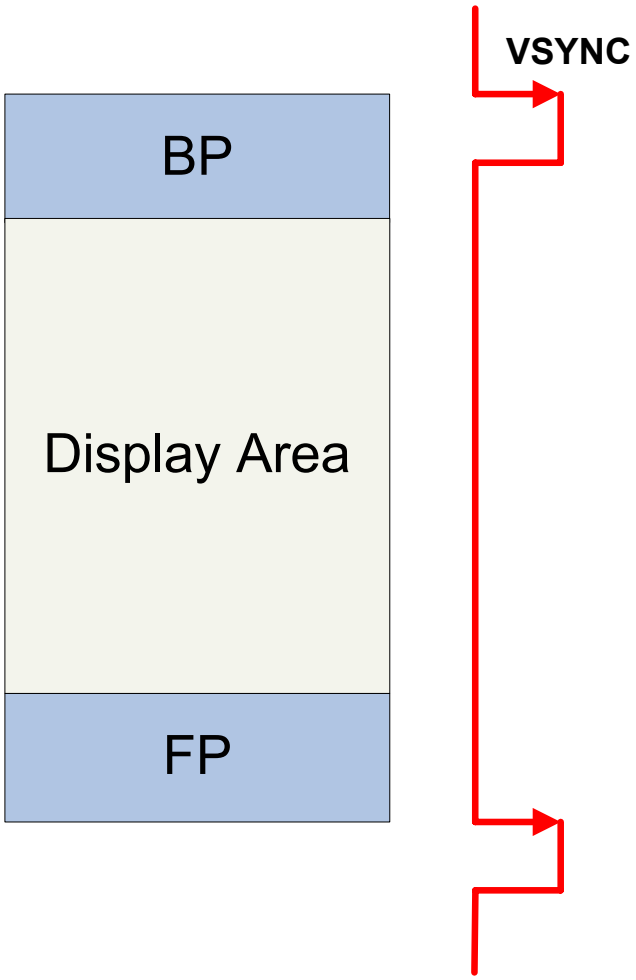


Figure 71 BP/FP

Note: The output signal is delay 2 lines timing from the VSYNC to the LCD

Operation mode	Number of interlaced Scan field	BP	FP	BP+FP
system interface	FLD1-0=01	>=2 lines	>=2 lines	<=16 lines
	FLD1-0=11	3 lines	5 lines	ignore
RGB Interface	ignore	>=2 lines	>=2 lines	<=16 lines
VSYNC Interface	ignore	>=2 line	>=2 lines	16 lines

Table 39 BP3-0, FP3-0 setting dependent on the operation mode

6.10 Power control Register 2 (R09h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	DCM1	DCM0	DC12	DC11	DC10	0	DK	SAP2	SAP1	SAP0

Figure 72 Power Control Register 2 (R09h)

SAP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the source driver. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. The tradeoff is between display quality and current consumption. During no display operation, when SAP2–0 = 000, the current consumption can be reduced by stopping the operational amplifier.

SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
0	0	0	Halt
0	0	1	Setting disabled
0	1	0	0.75
0	1	1	0.75
1	0	0	1
1	0	1	1
1	1	0	1.5
1	1	1	Setting disabled

Table 40 SAP Bits and amount of current in Operational Amplifier

DK: ON/OFF the operation of step-up circuit 1. When power on, the VLCD no output until VGHC is set up completely. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

Table 41 SAP Bits and amount of current in Operational Amplifier

DC12–10: Set the operating frequency for the step-up circuit 2. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DC12	DC11	DC10	Operation Frequency of Step-up Circuit 2
0	0	0	fosc / 8
0	0	1	fosc /16
0	1	0	fosc / 32
0	1	1	fosc / 64
1	0	0	fosc / 128
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	Halted

Table 42 Operation Frequency of Step-up Circuit 2 (fdcdc2)

Note: Ensure that the operation frequency of step-up circuit 1 step ≧ -up circuit 2
DCM1-0: Set the set-up frequency in a blank period during 8-color mode (CL=”1”).

DCM1	DCM0	Step-up frequency
0	0	Ignore
0	1	1/2 x fdcdc1,2
1	0	1/4 x fdcdc1,2
1	1	1/8 x fdcdc1,2

Table 43 Step-up frequency setting

6.11 External Display Interface Control Register 1 (R0Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TRI	DFM1	DFM0	0	0	PTG1	PTG0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

Figure 73 External Display Interface Control Register 1 (R0Ah)

RIM1- 0: Specify the transfer mode of RGB interface. RIM, DM, RM must be set Before LCD display operation through the RGB interface. During the LCD display, not allow changing the setting vale.

RIM1	RIM0	Transfer Mode
0	0	18-bit bus RGB interface Mode(1 transfer/pixel)
0	1	16-bit bus RGB interface Mode(1 transfer/pixel)
1	0	6-bit bus RGB interface Mode(3 transfers/pixel)
1	1	Ignore

Table 44 RIM bit for the Transfer Mode of RGB interface

DM1-0: Specify the operation mode of LCD display. DM1-0 allows the switch operation between the internal clock operation mode and external display interface mode (RGB and VSYNC interface mode), but can't switch between RGB and VSYNC interface mode.

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

Table 45 DM bit for the Operation Mode of LCD display

RM: Specify the access interface of GRAM. The setting value is not affected by the operation mode of LCD display. For example: In RGB interface operation mode, the data can be access to GRAM through RGB interface when RM=1, and then also access to GRAM through system interface when RM=0.

RM	Access Interface
0	System interface / VSYNC interface
1	RGB interface

Table 46 RM bit for the access interface of GRAM

Note: the register is set only through the system interface.
Note: A DOTCLK input and Data transfers must be executed in dot unit (R, G, B) for 6-bit bus RGB interface mode.

PTG1-0: Specify the scan mode of gate driver in non-display area.

PTG1	PTG0	Gate output in non-display area
0	0	Normal scan
0	1	VGL (Fixed)
1	0	Interval scan
1	1	Setting Disabled

Table 47 PTG bit setting

TRI: When TRI=1, a pixel data is written to GRAM through transfer 3 times 8-bit bus Interface. When TRI=0, 8-bit bus interface mode is unselected.

DFM1-0: Specify the data format when TRI=1, for 8-bit bus interface or serial data transfer interface. DFM1-0=10, 262K color mode. DFM1-0=11, 65K color mode.

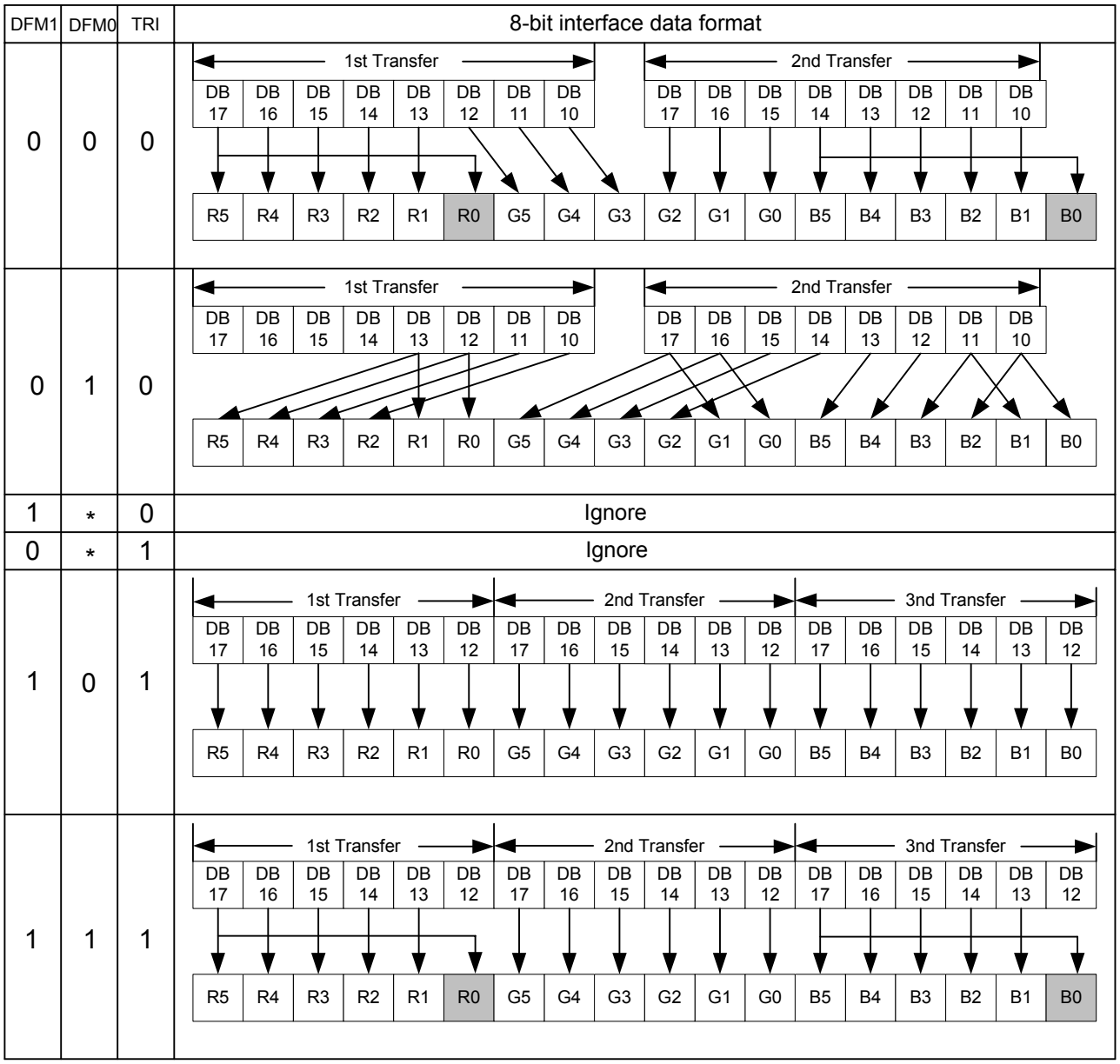


Figure 74 The setting of DFM and TRI (1)

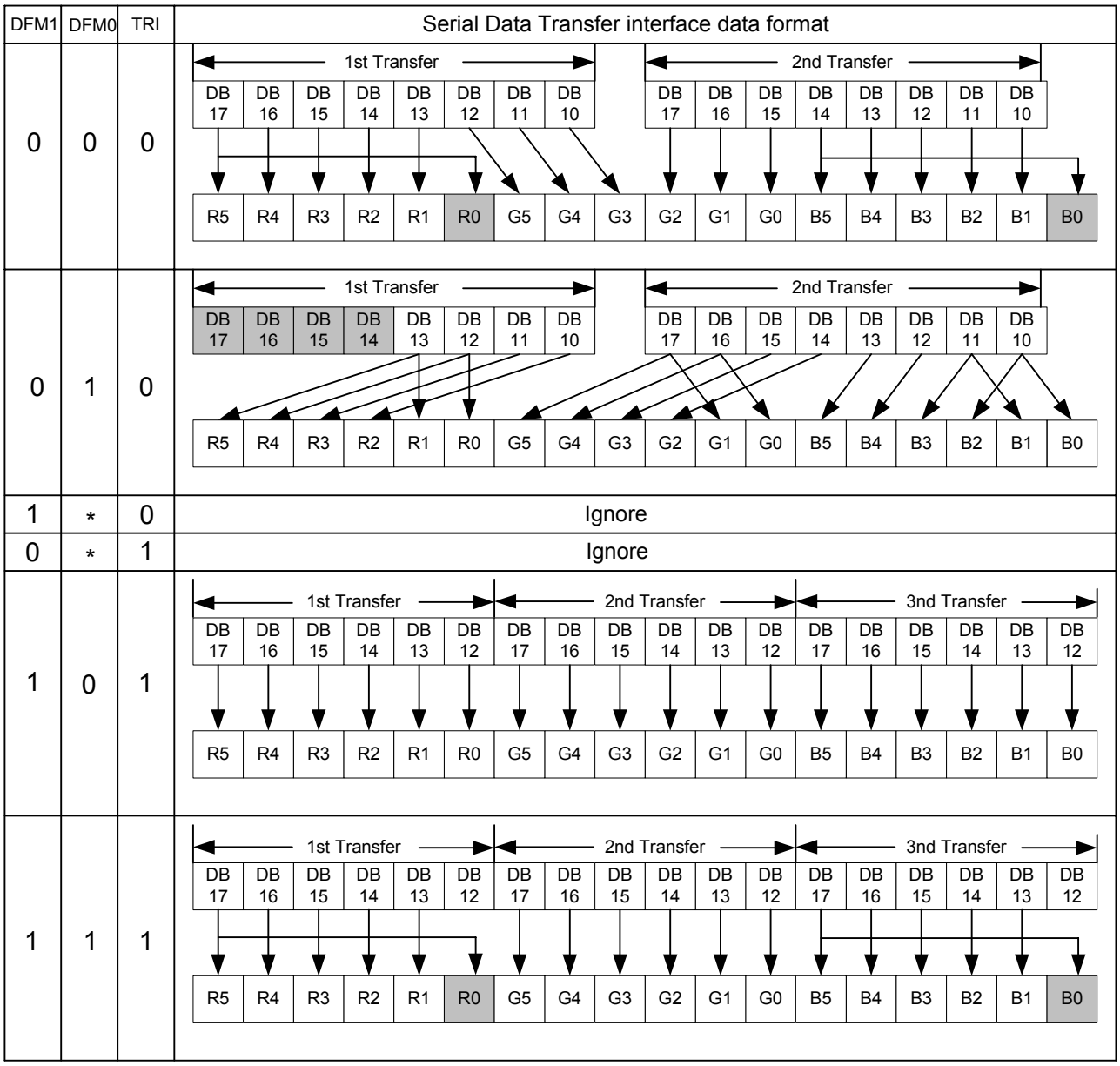


Figure 75 The setting of DFM and TRI (2)

6.12 Frame Cycle Control Register (R0Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GD1	GD0	SDT1	SDT 0	CE1	CE0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

Figure 76 Frame Cycle Control Register (R0Bh)

RTN3-0: Set the 1-line period in a clock unit.

Clock cycles=1/internal operation clock frequency

RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
0	0	0	0	16 clocks
0	0	0	1	17 clocks
0	0	1	0	18 clocks
:	:	:	:	:
1	1	0	1	29 clocks
1	1	1	0	30 clocks
1	1	1	1	31 clocks

Table 48 RTN Bits and Clock Cycles

DIV1-0: The division ratio of clocks for internal operation (DIV1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV1-0. Frame frequency can be adjusted along with the 1H period (RTN3-0). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

DIV1	DIV0	Division ratio	internal operation clock frequency
0	0	1	fosc/1
0	1	2	fosc/2
1	0	4	fosc/4
1	1	8	fosc/8

Table 49 DIV Bits and Clock Frequency

Formula for the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{(\text{RTN}*8 + 16) \times \text{DIV} \times (\text{NL}+\text{BP}+\text{FP})} [\text{Hz}]$$

fosc: RC oscillation frequency
RTN bit: Clocks per line
DIV bit: Division ratio
NL: The number of lines
FP: Number of lines for front porch
BP: Number of lines for back porch
BP+FP≦16

CE1-0: CE period can be set with CE1-0.

CE1	CE0	Internal operation (reference clock :internal oscillator)	RGB I/F Operation (reference clock:DOTCLK)
0	0	Not CE	Not CE
0	1	1 clock	8 clocks
1	0	2 clocks	16 clocks
1	1	3 clocks	24 clocks

Table 50 CE Bits for Equalized Period

SDT1-0: Set delay amount from falling edge of the gate output signal for the source outputs.

SDT1	SDT0	Internal operation (reference clock: internal oscillator)	RGB I/F Operation (reference clock: DOTCLK)
0	0	1 clock	8 clocks
0	1	2 clocks	16 clocks
1	0	3 clocks	24 clocks
1	1	4 clocks	32 clocks

Table 51 SDT Bits for Source Output Delay

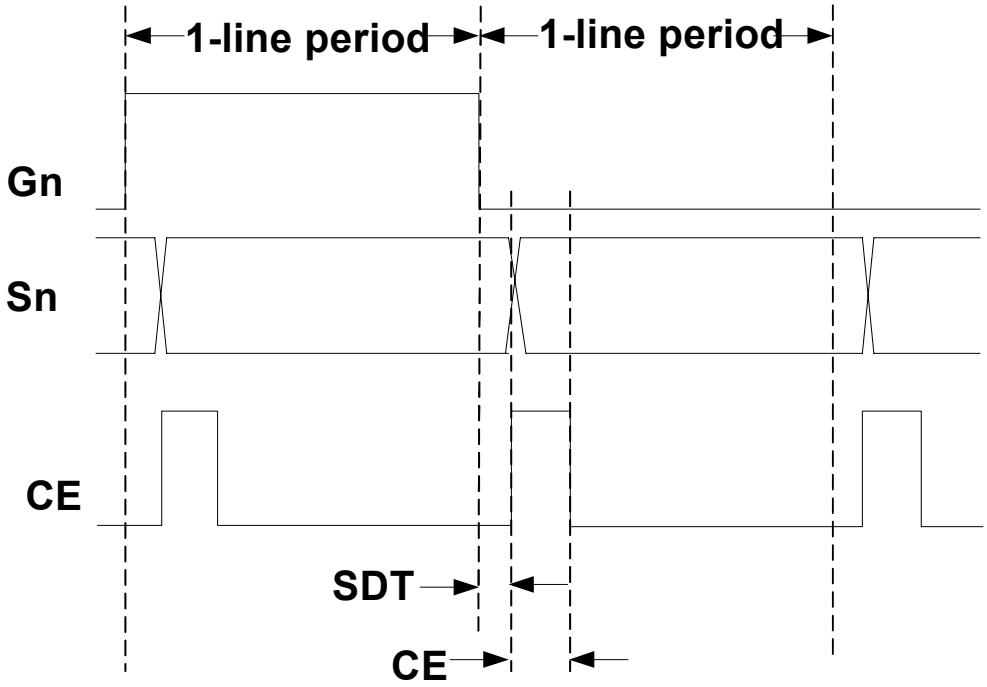


Figure 77 Equalized Period and Source Output Delay

GD1-0: Set amount of non-overlap for the gate output.

GD1	GD0	Internal operation (reference clock: internal oscillator)	RGB I/F operation (reference clock: DOTCLK)
0	0	0 clock	0 clock
0	1	4 clocks	32 clocks
1	0	6 clocks	48 clocks
1	1	8 clocks	64 clocks

Table 52 GD Bits for Non-overlap Time between Two Adjacent Gate Output Pulse

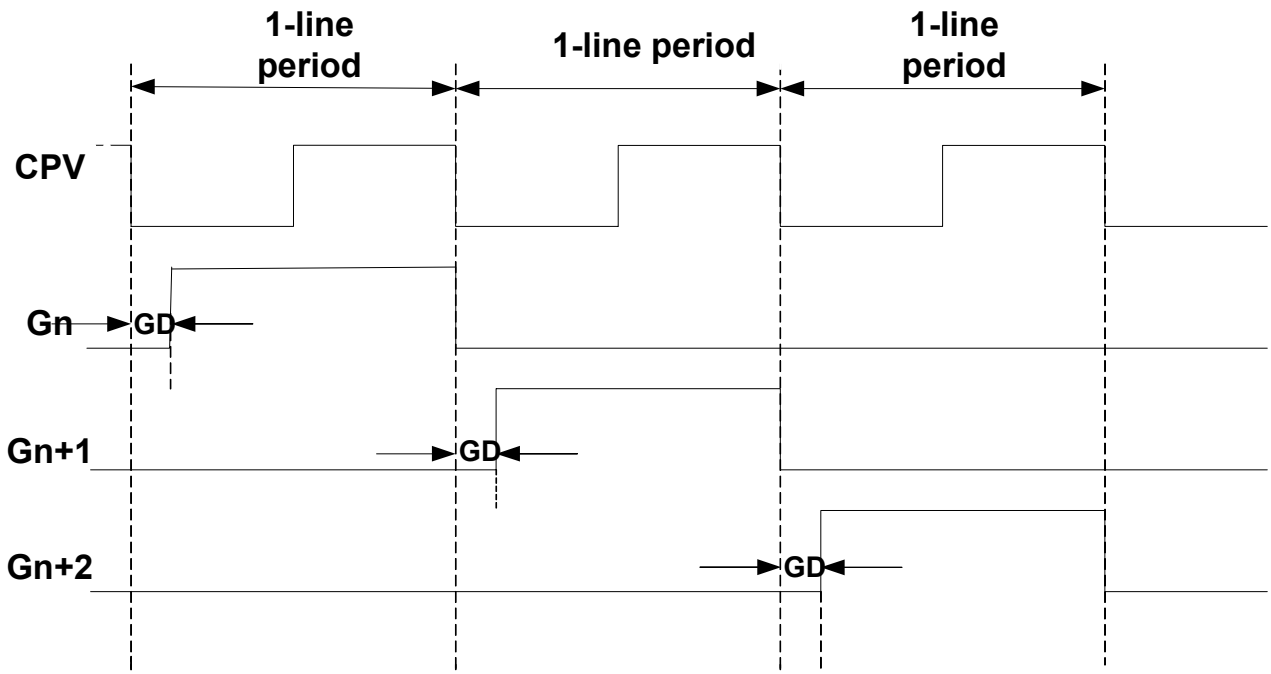


Figure 78 Non-overlap Time between Two Adjacent Gate Output Pulse

Interface	Clock Source
System interface mode	R-C oscillator
RGB interface mode	DOTCLK
VSYNC interface mode	R-C oscillator

Table 53 Clock Source for Interface Mode

6.13 Power Control Register 3 (R0Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0

Figure 79 Power Control Register 2 (R0Ch)

VC2-0: Set the reference voltage of VGAM1OUT and VCI1 by adjusting the rate of VCI.

VC2	VC1	VC0	Internal reference voltage (REGP) of VGM1OUT and VCI1
0	0	0	VCI
0	0	1	0.92 x VCI
0	1	0	0.87 x VCI
0	1	1	0.83 x VCI
1	0	0	0.76 x VCI
1	0	1	0.73 x VCI
1	1	0	Hi-z
1	1	1	Hi-z

Table 54 VC Settings and Internal Reference Voltage

6.14 Power Control Register 4 (R0Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0

Figure 80 Power Control Register 3 (R0Dh)

VRH3-0: Set the magnification of amplification for VGAM1OUT voltage. (VCOM, reference voltage for grayscale voltage) It allows magnify the amplification of REGP from 1.38 to 1.83 times.

VRH3	VRH2	VRH1	VRH0	VGAM1OUT Voltage
0	0	0	0	REGP x 1.33 times
0	0	0	1	REGP x 1.45 times
0	0	1	0	REGP x 1.55 times
0	0	1	1	REGP x 1.65 times
0	1	0	0	REGP x 1.75 times
0	1	0	1	REGP x 1.80 times
0	1	1	0	REGP x 1.85 times
0	1	1	1	Stopped
1	0	0	0	REGP x 1.900 times
1	0	0	1	REGP x 2.175 times
1	0	1	0	REGP x 2.325 times
1	0	1	1	REGP x 2.475 times
1	1	0	0	REGP x 2.625 times
1	1	0	1	REGP x 2.700 times
1	1	1	0	REGP x 2.775 times
1	1	1	1	Stopped

Table 55 VRH Bits and VGAM1OUT Voltage

Note: Adjust VC2-0 and VRH3-0 so that the VGAM1OUT voltage is lower than 5.0V.
Note: Set the VC and VRH bits so that VGAM1OUT is less than (VLCD-0.5)V.

PON: ON/OFF the operation of VGL and VCL in step-up circuit 2.
When PON = 0 VGL and VCL circuit is to stop.
When PON = 1 VGL and VCL circuit is to start.

6.15 Power Control Register 5 (R0Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 81 Power Control Register 4 (R0Eh)

VCM4-0: Set the VCOMH voltage (voltage of higher side when VCOM is driven in A/C.) It is possible to amplify from 0.4 to 0.98 times of VGAM1OUT voltage. When VCOM4-0 = “11111”, stop the internal volume adjustment and adjust the VCOMH with external resistance from VCOMR.

VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	VGAM1OUT x 0.40
0	0	0	0	1	VGAM1OUT x 0.42
0	0	0	1	0	VGAM1OUT x 0.44
0	0	0	1	1	VGAM1OUT x0.46
0	0	1	0	0	VGAM1OUT x0.48
0	0	1	0	1	VGAM1OUT x0.50
0	0	1	1	0	VGAM1OUT x0.52
0	0	1	1	1	VGAM1OUT x0.54
0	1	0	0	0	VGAM1OUT x0.56
0	1	0	0	1	VGAM1OUT x0.58
0	1	0	1	0	VGAM1OUT x0.60
0	1	0	1	1	VGAM1OUT x0.62
0	1	1	0	0	VGAM1OUT x0.64
0	1	1	0	1	VGAM1OUT x0.66
0	1	1	1	0	VGAM1OUT x 0.68
0	1	1	1	1	Stop the internal volume. VCOMH can be adjusted from VCOMR with a external VR (variable resister).
1	0	0	0	0	VGAM1OUT x 0.70
1	0	0	0	1	VGAM1OUT x 0.72
1	0	0	1	0	VGAM1OUT x 0.74
1	0	0	1	1	VGAM1OUT x0.76
1	0	1	0	0	VGAM1OUT x0.78
1	0	1	0	1	VGAM1OUT x0.80
1	0	1	1	0	VGAM1OUT x0.82
1	0	1	1	1	VGAM1OUT x0.84
1	1	0	0	0	VGAM1OUT x0.86
1	1	0	0	1	VGAM1OUT x0.88
1	1	0	1	0	VGAM1OUT x0.90
1	1	0	1	1	VGAM1OUT x0.92
1	1	1	0	0	VGAM1OUT x 0.94
1	1	1	0	1	VGAM1OUT x 0.96
1	1	1	1	0	VGAM1OUT x 0.98
1	1	1	1	1	Stop the internal volume. VCOMH can be adjusted from VCOMR with a external VR (variable resister).

Table 56 VCM4-0 Bits and VCOMH Voltage

Note: Adjust VGAM1OUT and VCM4-0 so that the VCOMH voltage is lower than VGAM1OUT.

VCOMG: When VCOMG =1, VCOML voltage can output to negative voltage (1.0V~ -VCI +0.5V). When VCOMG =0, VCOML voltage becomes VSSD and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, when VCOMG =0, setting of the VDV4-0 is invalid. In this case, adjustment of VCOM A/C amplitude must be adjusted with VCOMH using VCM4-0.

VDV4-0: Set the amplification factors for VCOM and Vgoff while VCOM AC drive is being performed. It is possible to setup from 0.6 to 1.23 times of VGAM1OUT. When VCOMG=0, the setup is invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	VGAM1OUT x 0.60
0	0	0	0	1	VGAM1OUT x 0.63
0	0	0	1	0	VGAM1OUT x 0.66
0	0	0	1	1	VGAM1OUT x 0.69
0	0	1	0	0	VGAM1OUT x 0.72
0	0	1	0	1	VGAM1OUT x 0.75
0	0	1	1	0	VGAM1OUT x 0.78
0	0	1	1	1	VGAM1OUT x 0.81
0	1	0	0	0	VGAM1OUT x 0.84
0	1	0	0	1	VGAM1OUT x 0.87
0	1	0	1	0	VGAM1OUT x 0.90
0	1	0	1	1	VGAM1OUT x 0.93
0	1	1	0	0	VGAM1OUT x 0.96
0	1	1	0	1	VGAM1OUT x 0.99
0	1	1	1	0	VGAM1OUT x 1.02
0	1	1	1	1	Inhibition
1	0	0	0	0	VGAM1OUT x 1.05
1	0	0	0	1	VGAM1OUT x 1.08
1	0	0	1	0	VGAM1OUT x 1.11
1	0	0	1	1	VGAM1OUT x 1.14
1	0	1	0	0	VGAM1OUT x 1.17
1	0	1	0	1	VGAM1OUT x 1.20
1	0	1	1	0	VGAM1OUT x 1.23
1	0	1	1	1	Inhibition
1	1	-	-	-	

Table 57 VDV4-0 Bits and VCOM Amplitude

Note: adjust VGAM1OUT and VDV4-0 so that VCOM amplitudes are lower than 6.0V.

6.16 Gate Scan Position Register (R0Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 82 Gate Scan Position Register (R0Fh)

SCN4-0: Set the scanning starting position of the gate driver.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G160	G1	G160
0	0	0	0	1	G9	G152	G17	G144
0	0	0	1	0	G17	G144	G33	G128
0	0	0	1	1	G25	G136	G49	G112
0	0	1	0	0	G33	G128	G65	G96
0	0	1	0	1	G41	G120	G81	G80
0	0	1	1	0	G49	G112	G97	G64
0	0	1	1	1	G57	G104	G113	G48
0	1	0	0	0	G65	G96	G129	G32
0	1	0	0	1	G73	G88	G145	G16
0	1	0	1	0	G81	G80	G2	G159
0	1	0	1	1	G89	G72	G18	G143
0	1	1	0	0	G97	G64	G34	G127
0	1	1	0	1	G105	G56	G50	G111
0	1	1	1	0	G113	G48	G66	G95
0	1	1	1	1	G121	G40	G82	G79
1	0	0	0	0	G129	G32	G98	G63
1	0	0	0	1	G137	G24	G114	G47
1	0	0	1	0	G145	G16	G130	G31
1	0	0	1	1	G153	G8	G146	G15

Table 58 SCN bits and Scanning Start Position for Gate Driver

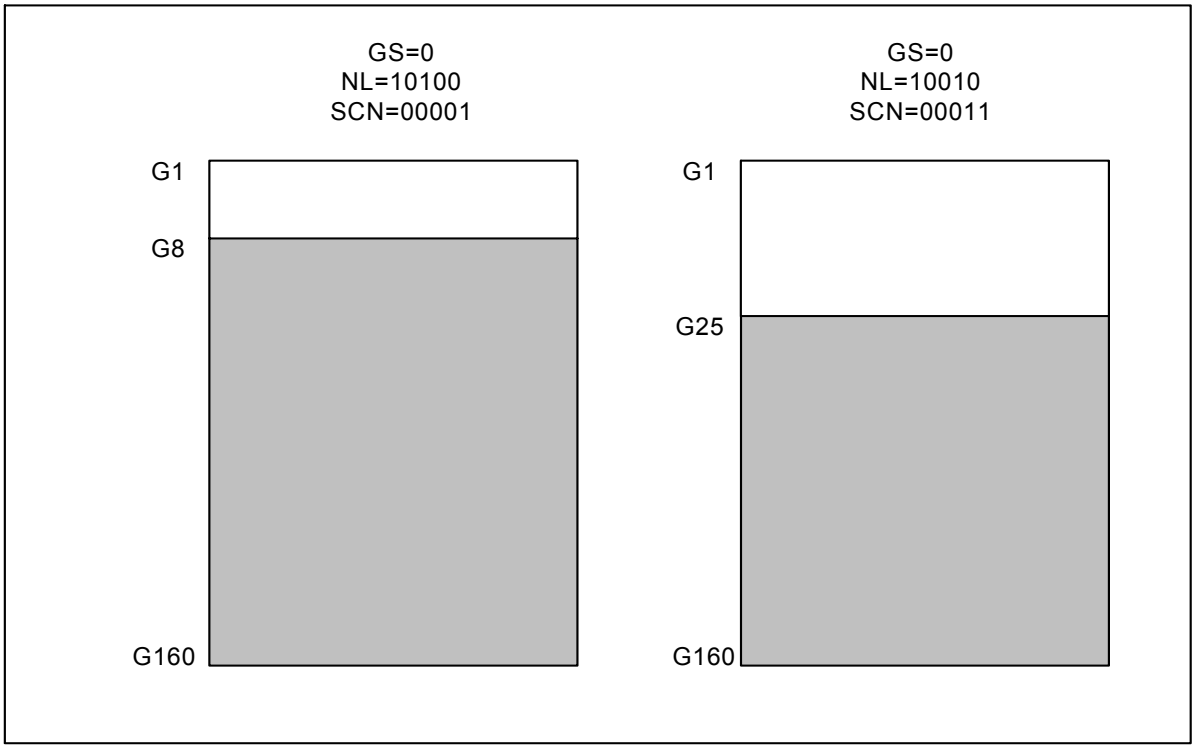


Figure 83 SCN bits and Scanning Start Position for Gate Driver

Note: Don't set NL, SCN over the end position of gate line (G160)
Note: Set NL4-0 and SCN4-0 so that the number for the end position of the gate line scans will not exceed 160.

6.17 Vertical Scroll Control Register (R11h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

Figure 84 Vertical Scroll Control Register (R11h)

VL7-0: Specify the amount of scrolling line from 0 to 160 in the display to enable smooth vertical scrolling. If GRAM address mapping would exceed “9Fxx”H, GRAM address mapping would restart from “00XX”H after the data in “9Fxx”H of GRAM being displayed. The display-start line (VL7–0) is valid only when VLE1 =1 or VLE2 =1. The display-start line is fixed to zero when VLE2-1 =00. (VLE1 is the 1st display window vertical-scroll enable bit, and VLE2 is the 2nd display window vertical-scroll enable bit.)

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Srolling length
0	0	0	0	0	0	0	0	0 lines
0	0	0	0	0	0	0	1	1 lines
0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	1	1	3 lines
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1	157 lines
1	0	0	1	1	1	1	0	158 lines
1	0	0	1	1	1	1	1	159 lines

Table 59 VL bits and scrolling Length

6.18 First Display Window Driving Position Register (R14h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

Figure 85 First Screen Driving Position Register (R14h)

SS17–10: Specify the driving start position for the first display window in a line unit. The LCD driving starts from the 'setting value + 1' scan line of gate driver.

SE17–10: Specify the driving end position for the first display window in a line unit. The LCD driving is performed to the 'setting value + 1' gate driver. See the Partial-Screen Display Function section for details.

6.19 Second Display Window Driving Position Register (R15h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 86 Second Screen Driving Position Register (R15h)

SS27–20: Specify the driving start position for the second display window in a line unit. The LCD driving starts from the 'setting value + 1' scan line of gate driver. The second display window is driven when SPT = 1.

SE27–20: Specify the driving end position for the second display window in a line unit. The LCD driving is performed to the ' setting value + 1' gate driver.

Note: Ensure that SS17–10 < SE17–10 < SS27–20 < SE27–20 ≤9Fh. For details, see the Partial Screen Display Function section.

6.20 Horizontal RAM Address Position Register (R16h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

Figure 87 Horizontal RAM Address Position Register (R16h)

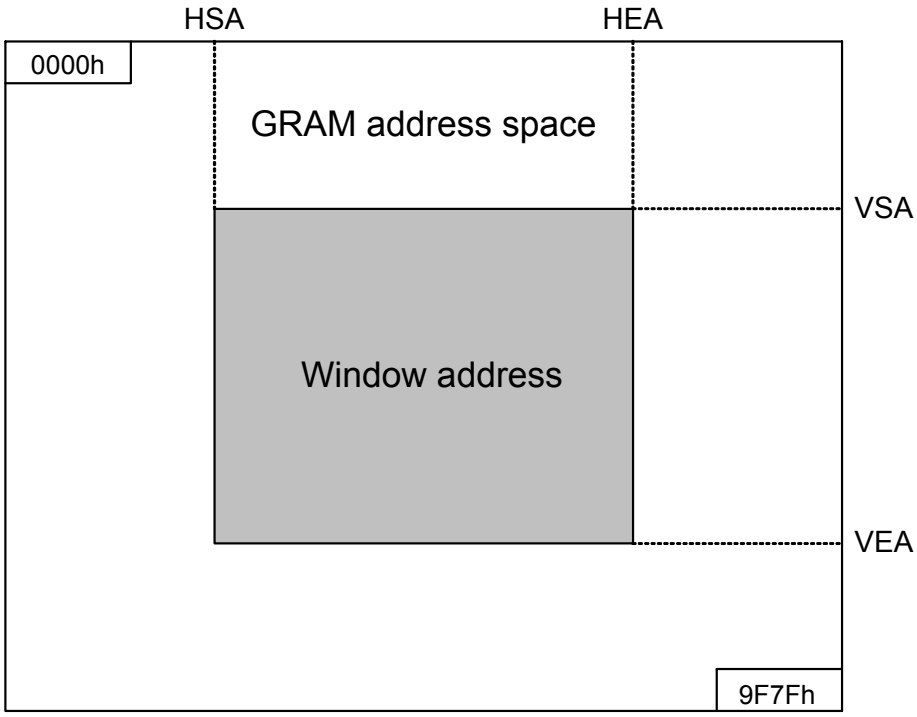
HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by HSA7-0 to the address specified by HEA7-0.Ensure that “00”h≤HSA7-0 ≤HEA7-0 ≤“7F”h.

6.21 Vertical RAM Address Position Register (R17h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 88 Vertical RAM Address Position Register (R17h)

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by VSA7-0 to the address specified by VEA7-0. Ensure that “00”h ≤VSA7-0≤VEA7-0 ≤“9F”h



Window address setting range
"00"h ≤HSA7-0 ≤HEA7-0 ≤"7F"h
"00"h ≤VSA7-0 ≤VEA7-0 ≤"9F"h

Figure 89 Window Address Setting Range

Note: 1. The window address range must be within the GRAM address space.
2. Data are written to GRAM in four words when operating in high speed mode so dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

6.22 RAM Address Register (R21h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 90 RAM Address Register (R21h)

AD15–0: Set GRAM addresses to the address counter (AC) before access the GRAM. Once the GRAM data is written, the AC is automatically Updated according to the AM and I/D bits. During the standby mode, the GRAM cannot be accessed.

AD15-AD0	GRAM Setting
"0000"h-"007F"h	Bitmap data for G1
"0100"h-"017F"h	Bitmap data for G2
"0200"h-"027F"h	Bitmap data for G3
:	:
"9D00"h-"9D7F"h	Bitmap data for G158
"9E00"h-"9E7F"h	Bitmap data for G159
"9F00"h-"9F7F"h	Bitmap data for G160

Table 60 GRAM address mapping

6.23 Write Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

RGB-I/F mode:

R/W	RS	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
W	1	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Figure 91 Write Data Register (R22h)

WD17–0: Transform the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically Updated according to the AM and I/D bits.

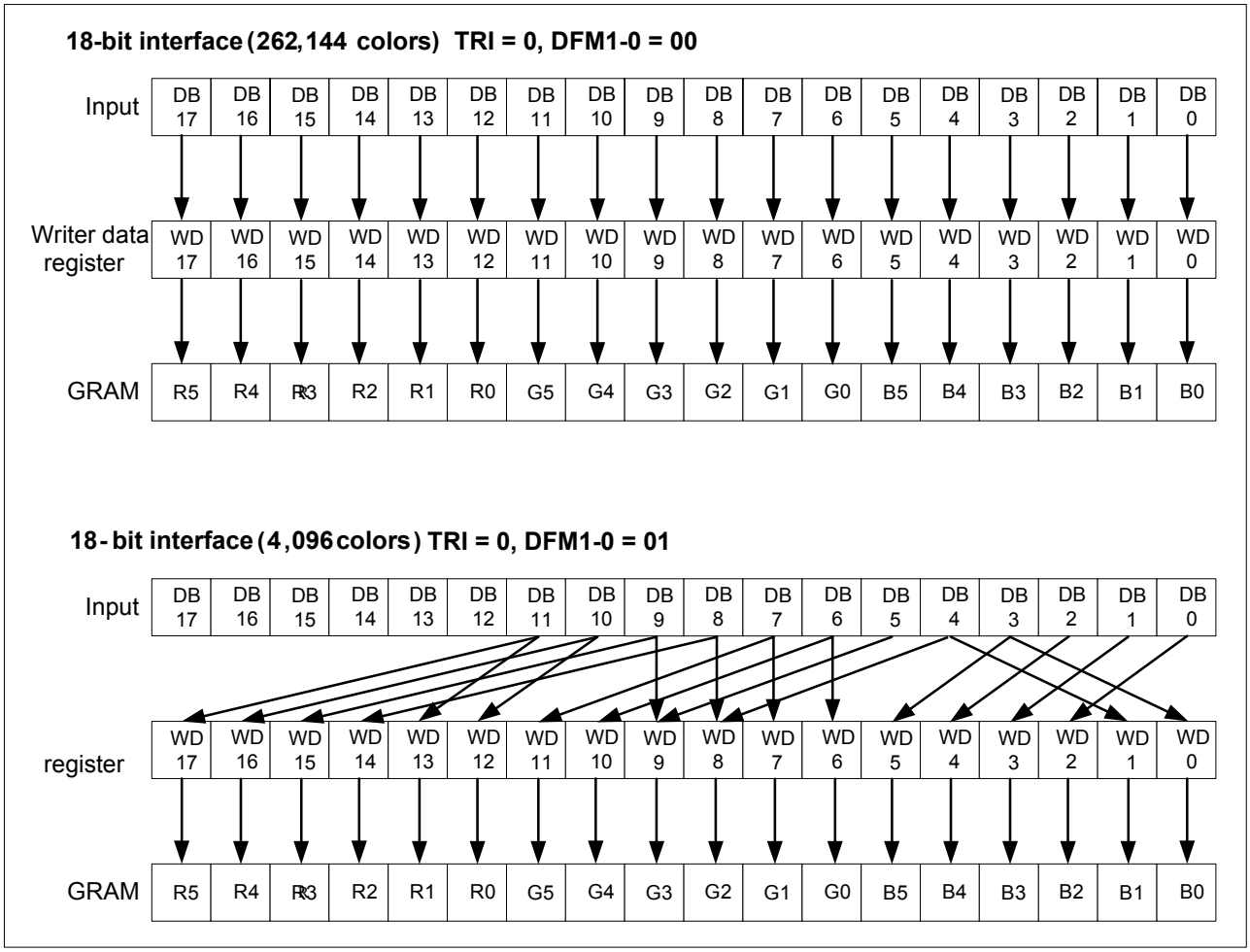


Figure 92 Bit Mapping of One Pixel Data: Input Data (18-bit Interface) Written to GRAM through Write Data Register

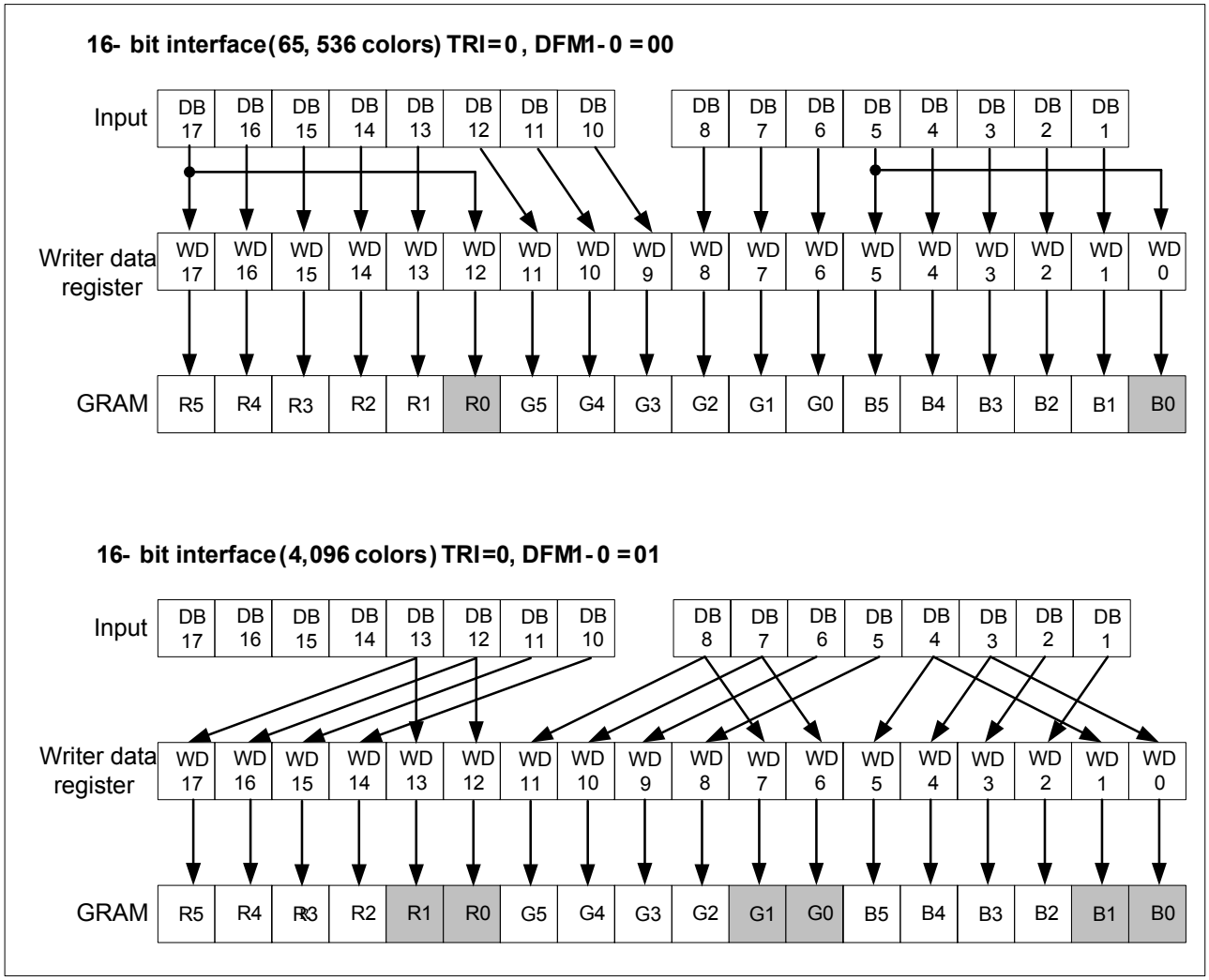


Figure 93 Bit Mapping of One Pixel Data: Input Data (16-bit Interface) Written to GRAM through Write Data Register

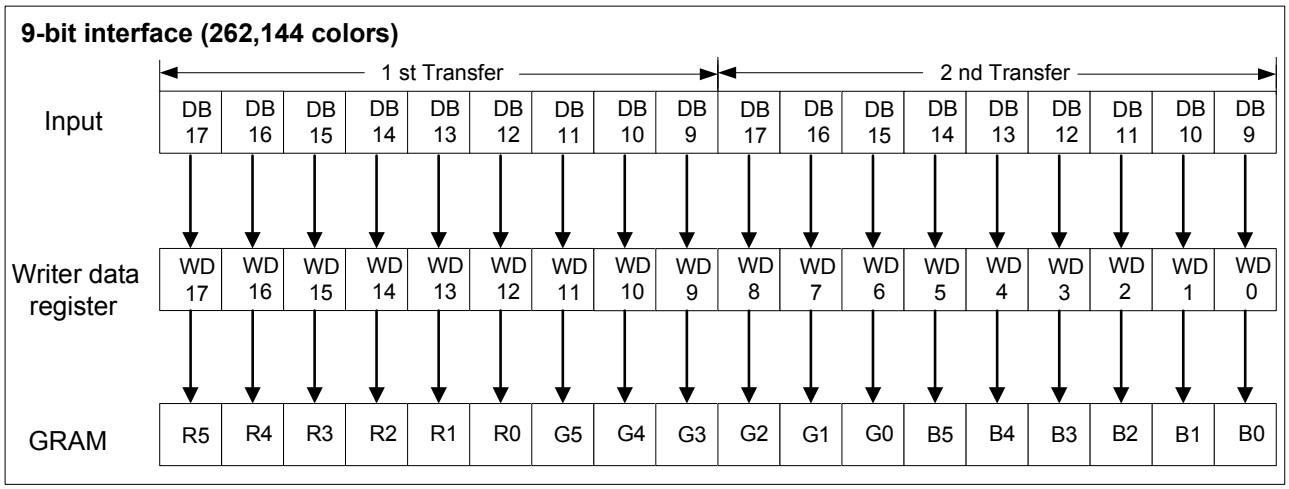


Figure 94 Bit Mapping of One Pixel Data: Input Data (9-bit interface) Written to GRAM through Write Data Register

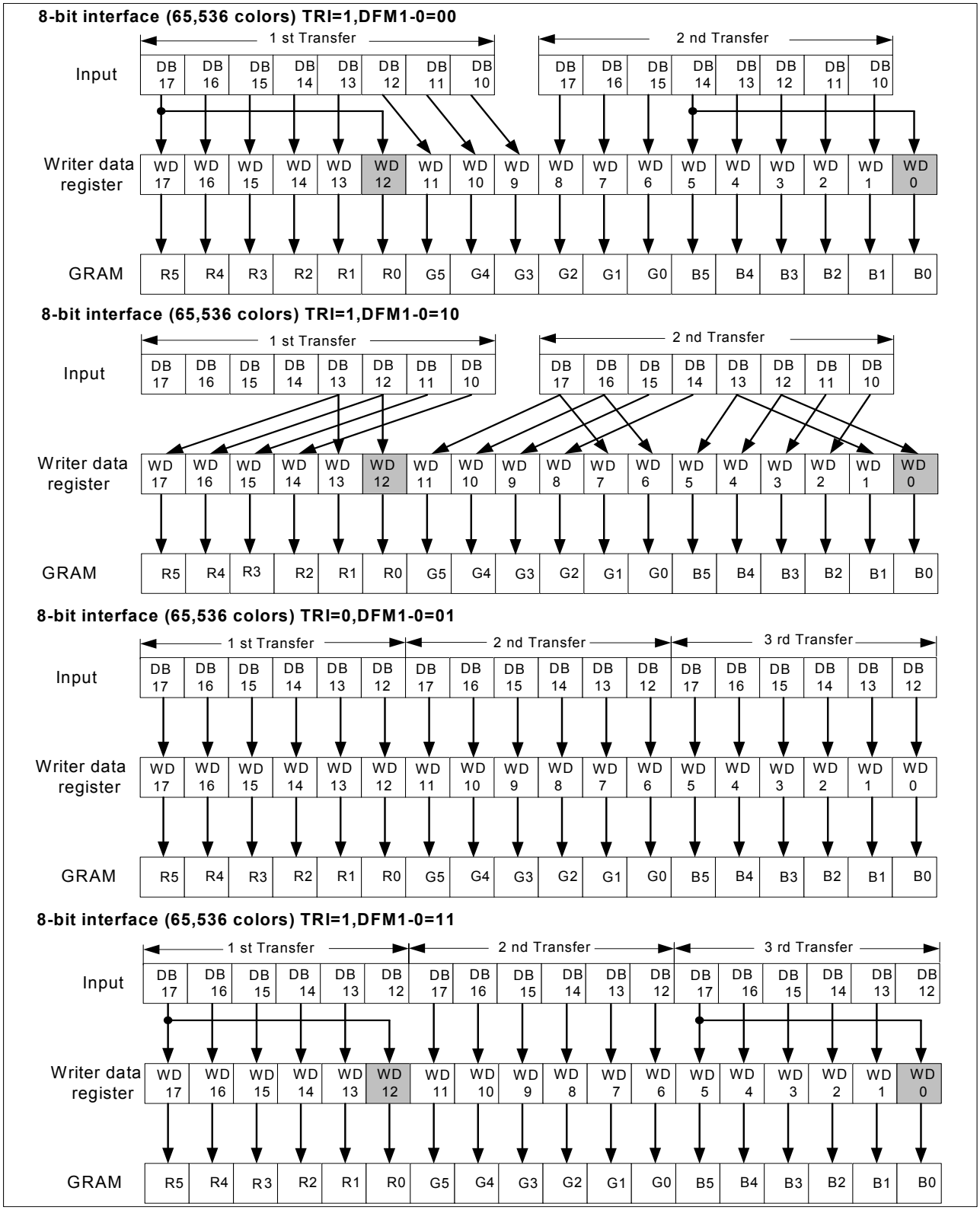


Figure 95 Bit Mapping of One pixel Data: Input Data (8-bit interface) Written to GRAM through Write Data Register

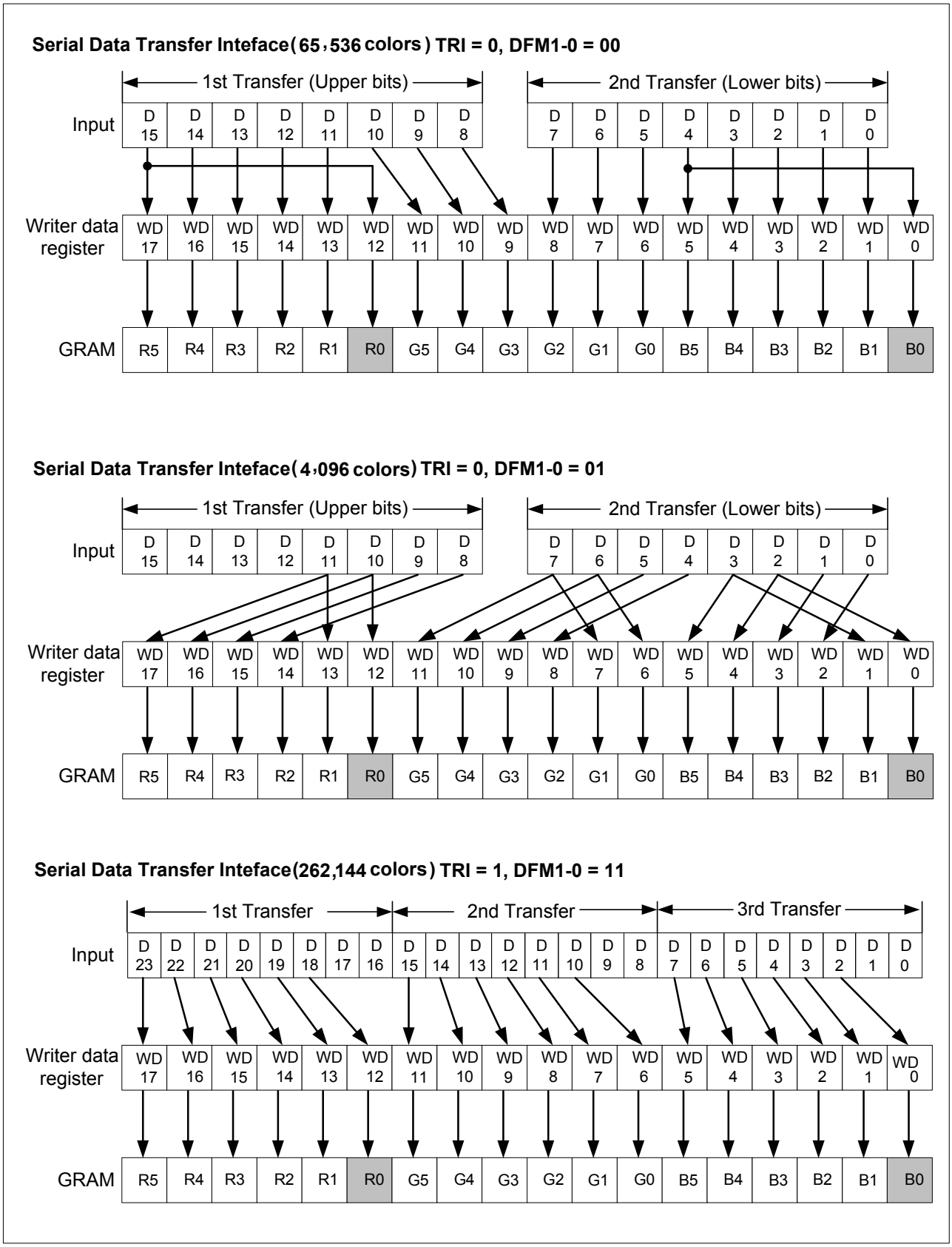


Figure 96 Bit Mapping of One Pixel Data: Input Data (serial Data Transfer interface) Written to GRAM through Write Data Register

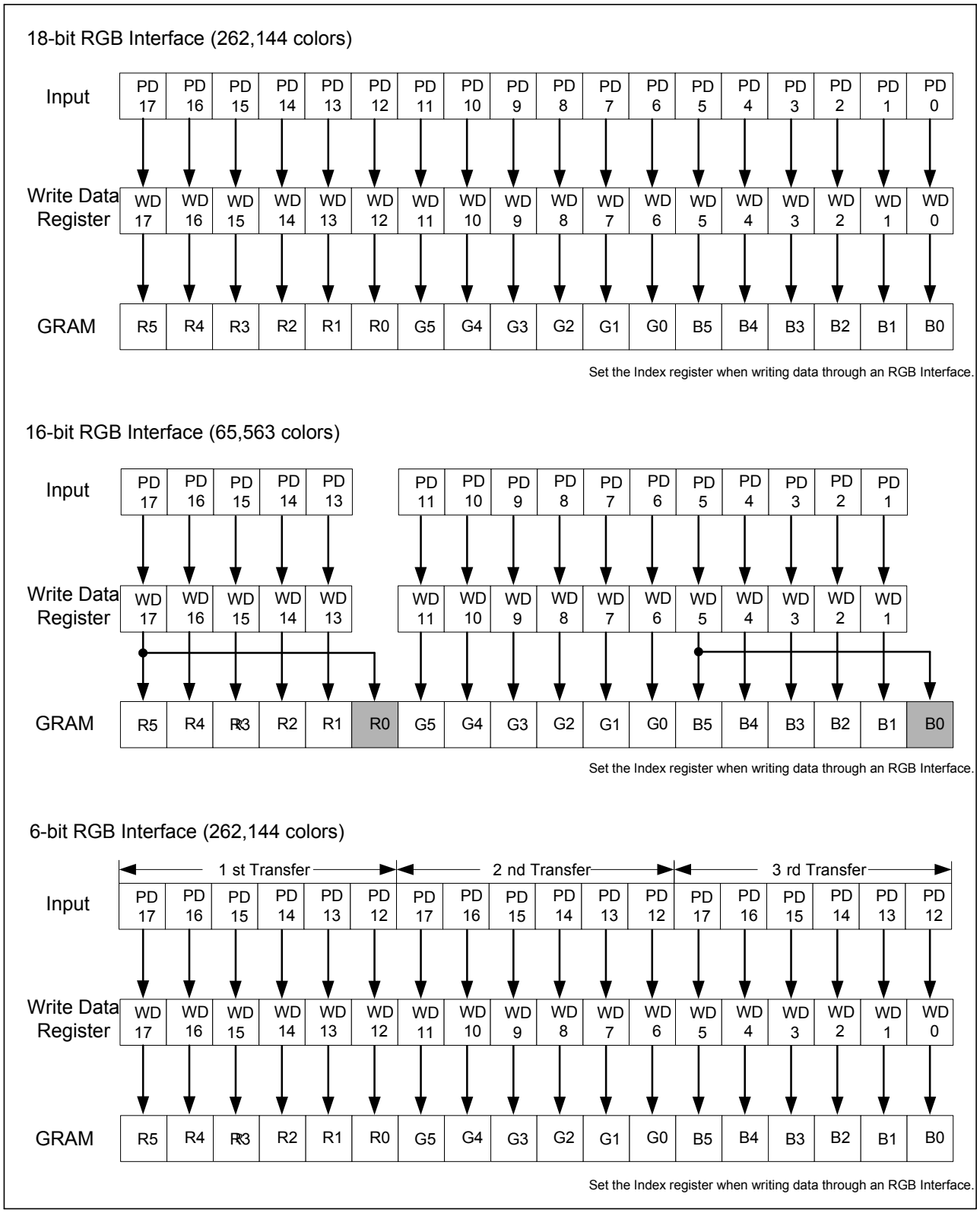


Figure 97 Bit Mapping of One Pixel Data: input Data (18/16/6-bit RGB interface) Written to GRAM through Write Data Register

6.24 Read Data Register (R22h)

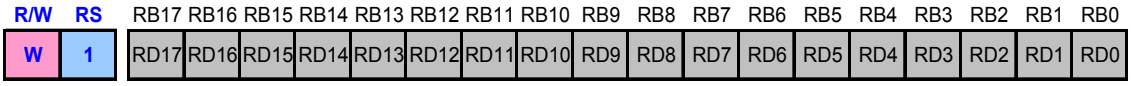


Figure 98 Read Data Register (R22h)

RD17–0: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

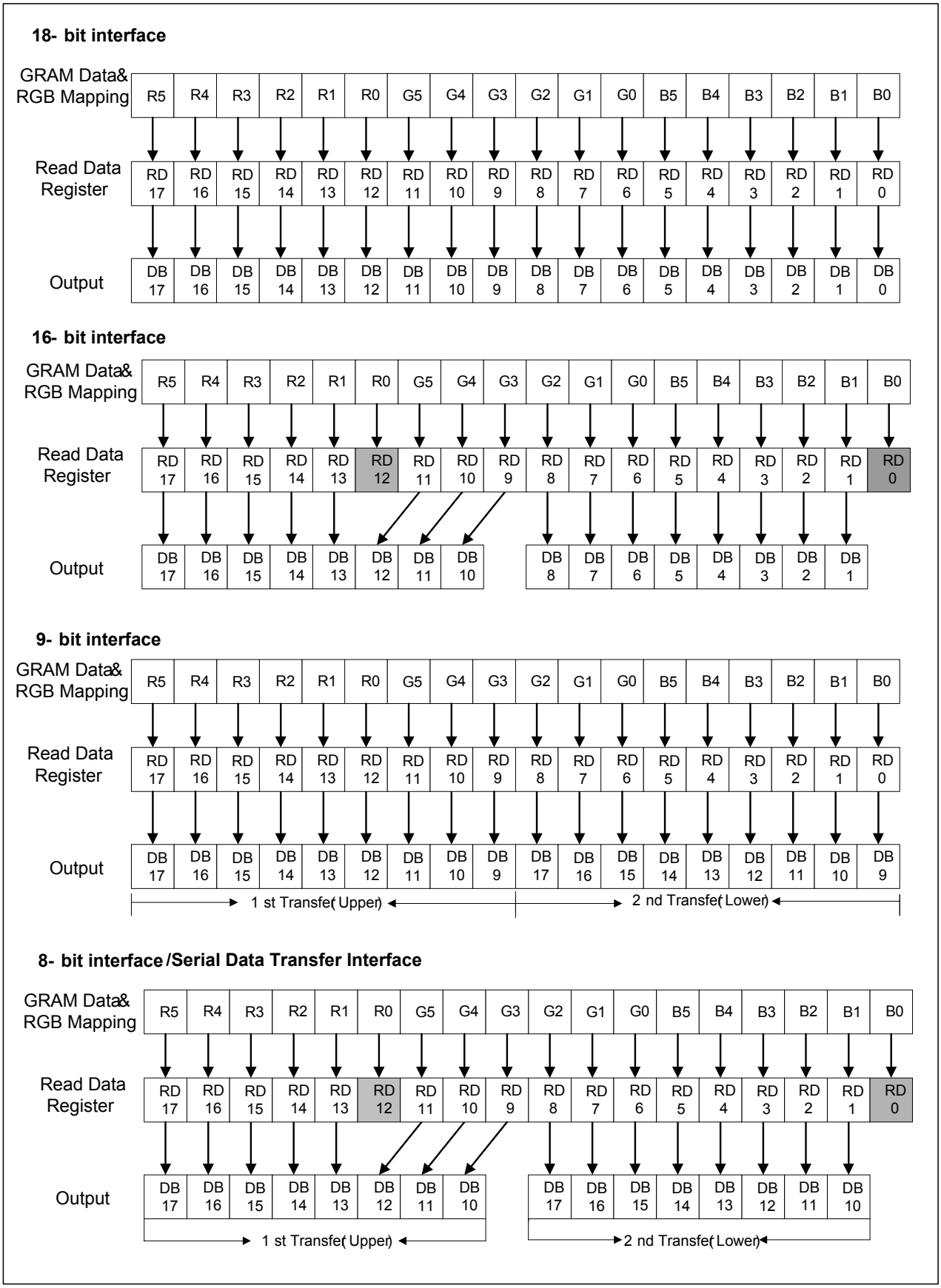


Figure 99 Output Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit interface Mode

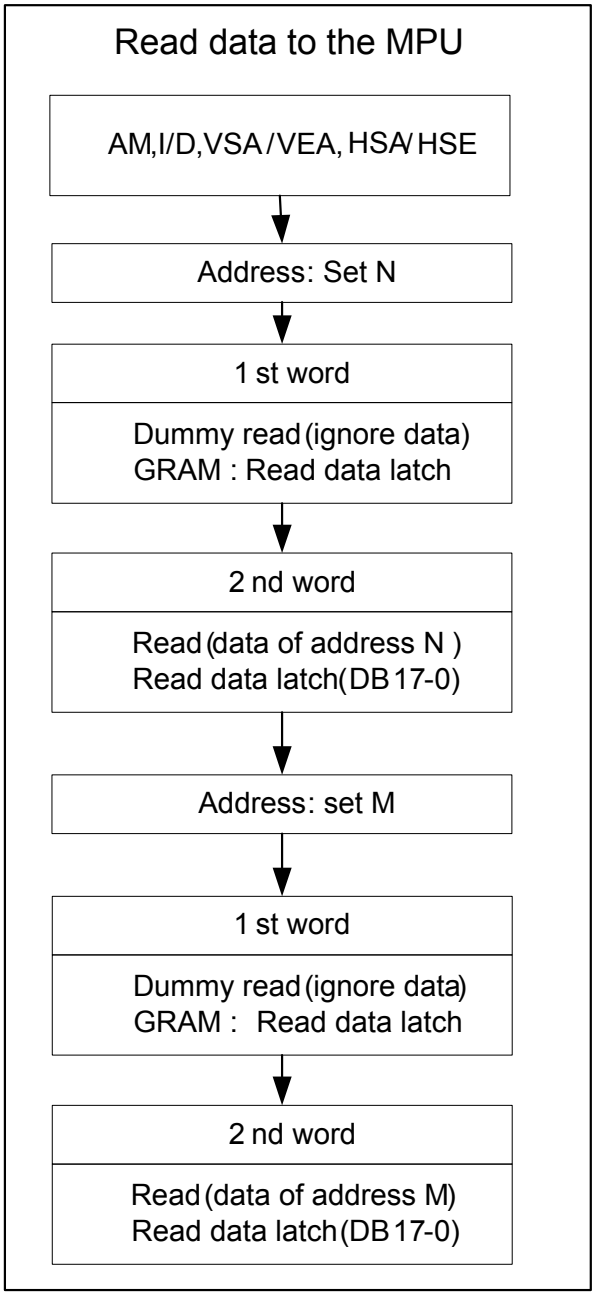


Figure 100 Flow Chart of GRAM Read Data

6.25 Gamma Control Register Set

Gamma Control Register 1~10 (R30h~R3Bh)

	R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R30	W	1	0	0	0	0	0	MP1(2)	MP1(1)	MP1(0)	0	0	0	0	0	MP0(2)	MP0(1)	MP0(0)
R31	W	1	0	0	0	0	0	MP3(2)	MP3(1)	MP3(0)	0	0	0	0	0	MP2(2)	MP2(1)	MP2(0)
R32	W	1	0	0	0	0	0	MP5(2)	MP5(1)	MP5(0)	0	0	0	0	0	MP4(2)	MP4(1)	MP4(0)
R33	W	1	0	0	0	0	0	CP1(2)	CP1(1)	CP1(0)	0	0	0	0	0	CP0(2)	CP0(1)	CP0(0)
R34	W	1	0	0	0	0	0	MN1(2)	MN1(1)	MN1(0)	0	0	0	0	0	MN0(2)	MN0(1)	MN0(0)
R35	W	1	0	0	0	0	0	MN3(2)	MN3(1)	MN3(0)	0	0	0	0	0	MN2(2)	MN2(1)	MN2(0)
R36	W	1	0	0	0	0	0	MN5(2)	MN5(1)	MN5(0)	0	0	0	0	0	MN4(2)	MN4(1)	MN4(0)
R37	W	1	0	0	0	0	0	CN1(2)	CN1(1)	CN1(0)	0	0	0	0	0	CN0(2)	CN0(1)	CN0(0)
R3A	W	1	0	0	0	OP1(4)	OP1(3)	OP1(2)	OP1(1)	OP1(0)	0	0	0	0	OP0(3)	OP0(2)	OP0(1)	OP0(0)
R3B	W	1	0	0	0	ON1(4)	ON1(3)	ON1(2)	ON1(1)	ON1(0)	0	0	0	0	ON0(3)	ON0(2)	ON0(1)	ON0(0)

MP5-0 (2:0): Gamma adjustment registers for positive polarity output
CP1-0 (2:0): Gamma gradient adjustment registers for positive polarity output
MN5-0(2:0): Gamma adjustment registers for negative polarity output
CN1-0(2:0): Gamma gradient adjustment registers for negative polarity output
OP0 (3:0)/OP1 (4:0): Amplification adjustment resistor for positive polarity output
ON0 (3:0)/ON1 (4:0): Amplification average adjustment resistor for negative polarity output

Figure 101 Gamma Control Register 1~10 (R30h~R3Bh)

6.26 Initialization

Output Pin Initialization

1. Driver output pins (source outputs): Output VSSD level
2. Driver output pins (Gate outputs): Output VGH level
3. Oscillator output pin (OSC2): Output oscillation signal

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4-0 =10011, SS = 0, GS = 0, SM = 0)
3. LCD driving AC control (FLD1-0 = 01, B/C =0, EOR =0, NW5-0 =00000)
4. Power control 1 (BT2-0=000, DC02-10 =000, AP2-0 =000: LCD power off, SLP =0: Sleep mode off, STB = 0: Standby mode off)
5. Entry mode set (BGR= 0, I/D1-0=11: Increment by 1, AM=0: Horizontal move)
6. Display control 1 (PT1-0=00, VLE2-1=00: No vertical scroll, SPT=0, GON=0, DTE=0, CL=0: 262144-color mode, REV=0, D1-0=00: Display off)
7. Display control 2 (VSPL=0, HSPL=0, DPL=0, FP3-0=0011, ISC3-0=0000, BP3-0=0101)
8. Power control 2 (DCM1-0=00, DC12-10=000, DK=0, SAP2-0=100)
9. External display interface control 1 (TRI=0, DFM1-0=00, PTG1-0=00, RM=0: System interface, DM1-0=00: internal clock operation, RIM1-0=00: 18-bit RGB interface)
10. Frame cycle control(GD1-0=00, SDT1-0=00, CE1-0=00:No equalization, DIV1-0=00: 1-divided clock, RTN3-0=0000: 16 clocks in 1-line period)
11. Power control 3 (VC2-0=000)
12. Power control 4 (PON=0, VRH3-0=0000)
13. Power control 5 (VCOMG=0, VDV4-0=00000, VCM4-0=00000)
14. Gate scan starting position (SCN4-0=00000)
15. Vertical scroll (VL7-0=00000000)
16. 1st screen division (SE17-10=10011111, SS17-10=00000000)
17. 2nd screen division (SE27-20=10011111, SS27-20=00000000)
18. Horizontal RAM address position(HEA7-0=01111111, HSA7-0=00000000)
19. Vertical RAM address position (VEA7-0=10011111, VSA7-0=00000000)
20. RAM address set (AD15-0=0000h)
21. Gamma control
    (MP02-00=000, MP12-10=000, MP22-20=000, MP32-30=000,
    MP42-40=000, MP52-50=000, CP02-00=000, CP12-10=000)
    (MN02-00=000, MN12-10=000, MN22-20=000, MN32-30=000,
    MN42-40=000, MN52-50=000, CN02-00=000, CN12-10=000)
    (OP03-00=0000, OP14-10=00000, ON03-00=0000, ON14-10=0000)

6.27 Reset Function

The FGD0801 is internally initialized by NRESET input. During the reset period, no instruction or GRAM data access from the MPU can be accepted. The reset input must be held for at least 1 ms. do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

GRAM Data Initialization:

It must be initialized by software while display is off (D1-0=00)

7. Power Generation

7.1 Specification

The following tables show the specification of power supply circuit and pins connection:

Pins connection	Recommended voltage	Capacity
VDDD, VGAM1OUT, VCI1, VCL,VCOMH,VCOML, C11A/B, C12A/B	6V	1 μF
VLCD, C21A/B, C22A/B	10V	1 μF
TVCOMHI, TVMAG	16V	0.1μF
VGH, VGL	25V	1 μF

Table 61 Adoptability of Capacitor

Pins connection	Feature
VGL – VSSD VCI – VGH VCI – VLCD	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: RB521S-30)

Table 62 Adoptability of Schottkey diode

Reusable	Pins to connect
> 200 kΩ	VCOMR

Table 63 Adoptability of Variable resistor

7.2 Power supply Circuit

The power supply circuit of FGD0801 presides over generating supply voltages to drive a LCD panel. The following is the diagram:

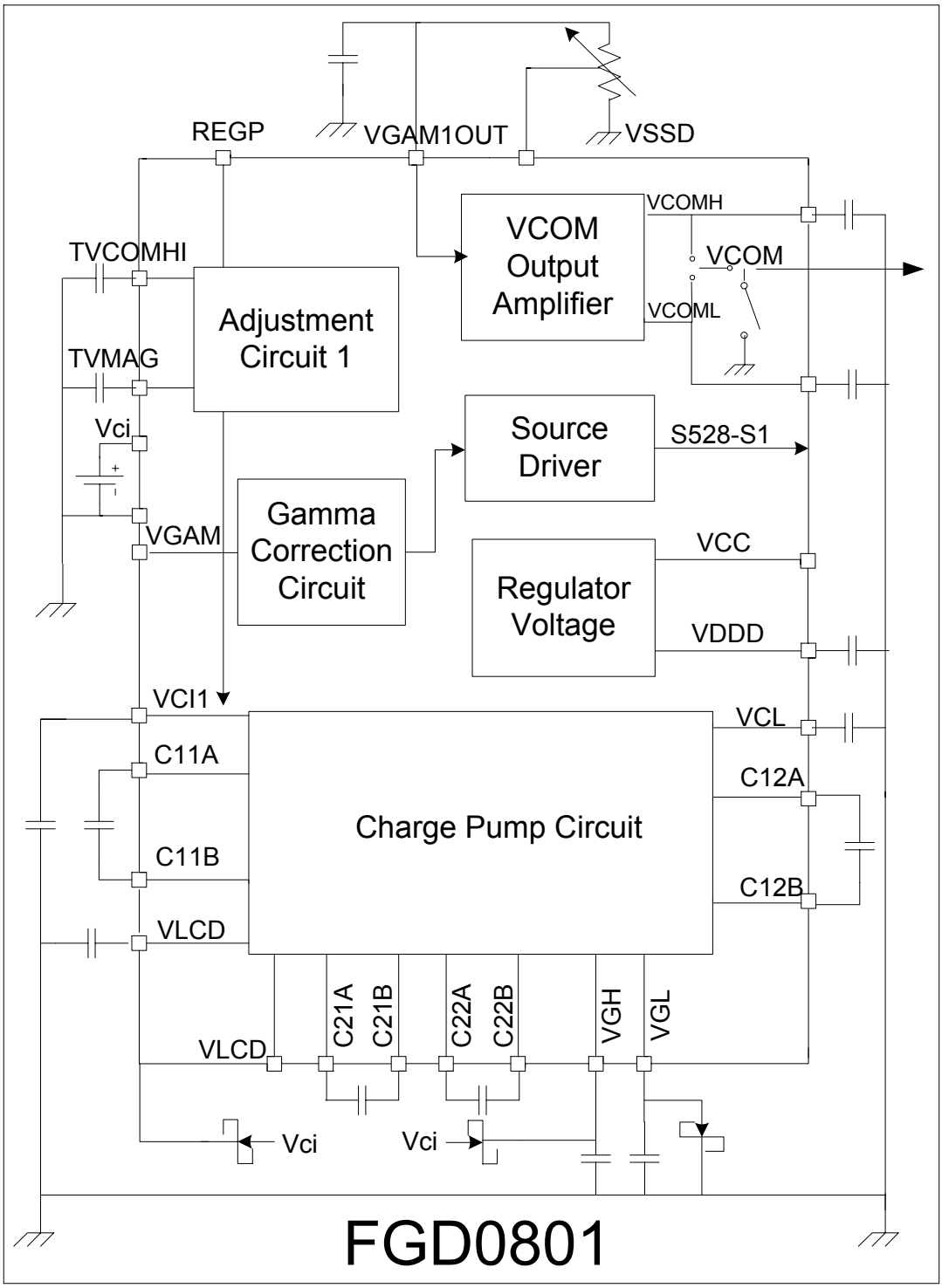


Figure 102 Block Diagram of Power Supply Circuit

7.3 Voltage Setting

The voltage setting pattern diagram of the FGD0801 illustrates as following figure. The outputs of VLCD, VGH, VGL, and VCL are sensitive to the voltage drop that set from the idea setting voltage in virtue of current consumption. When the VCOM voltage alternating cycle is high, the large current will be consumed.

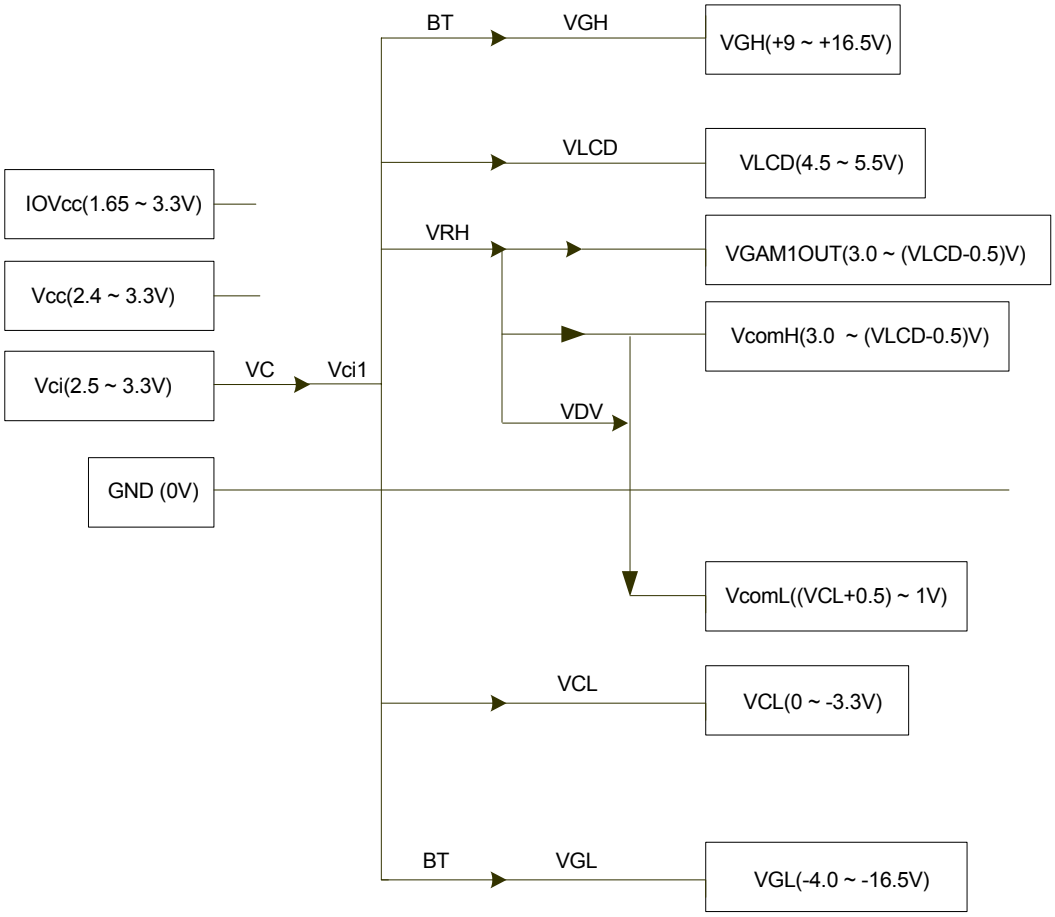


Figure 103 Voltage Setting Diagram

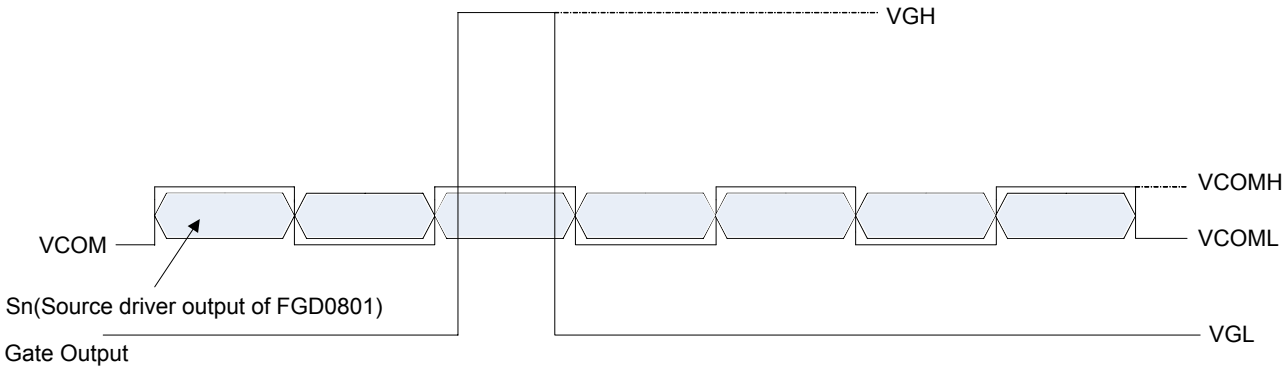


Figure 104 Applied Voltage of TFT Display

7.4 Register Setting

The following are the sequences of register setting flow that applied to the FGD0801 driving the TFT display.

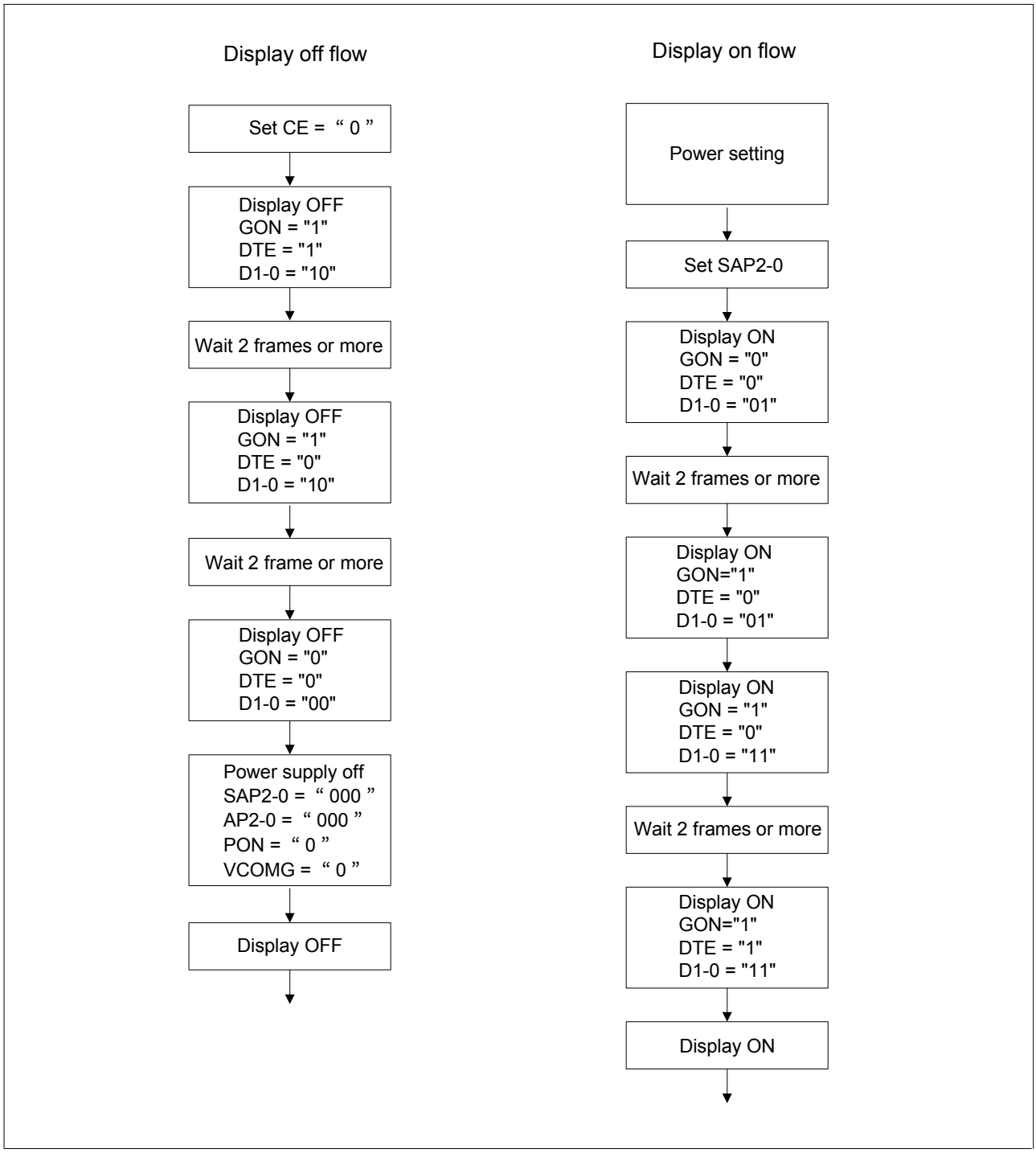


Figure 105 Register Setting Sequence

Standby mode and Sleep Mode setting flow:

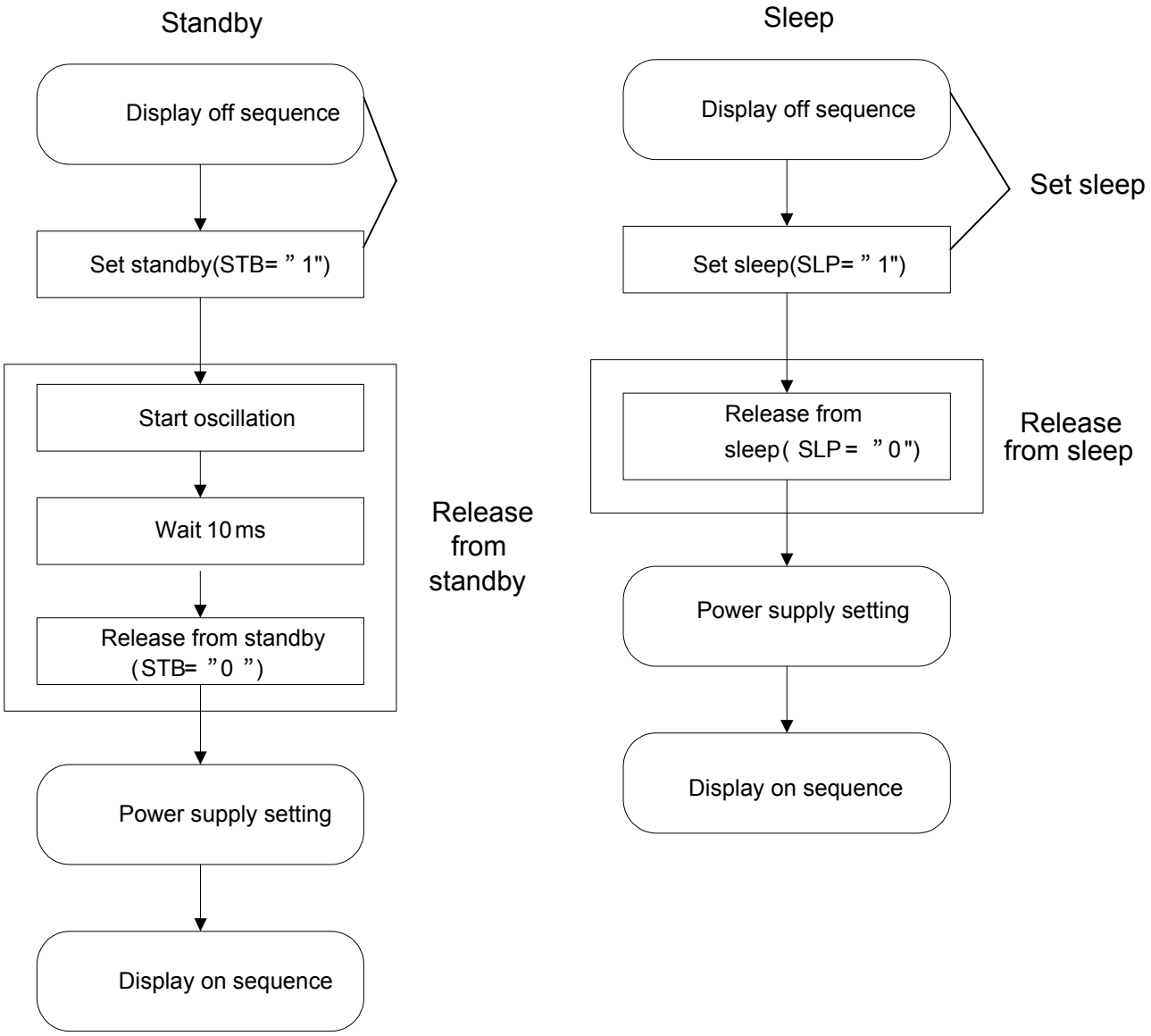
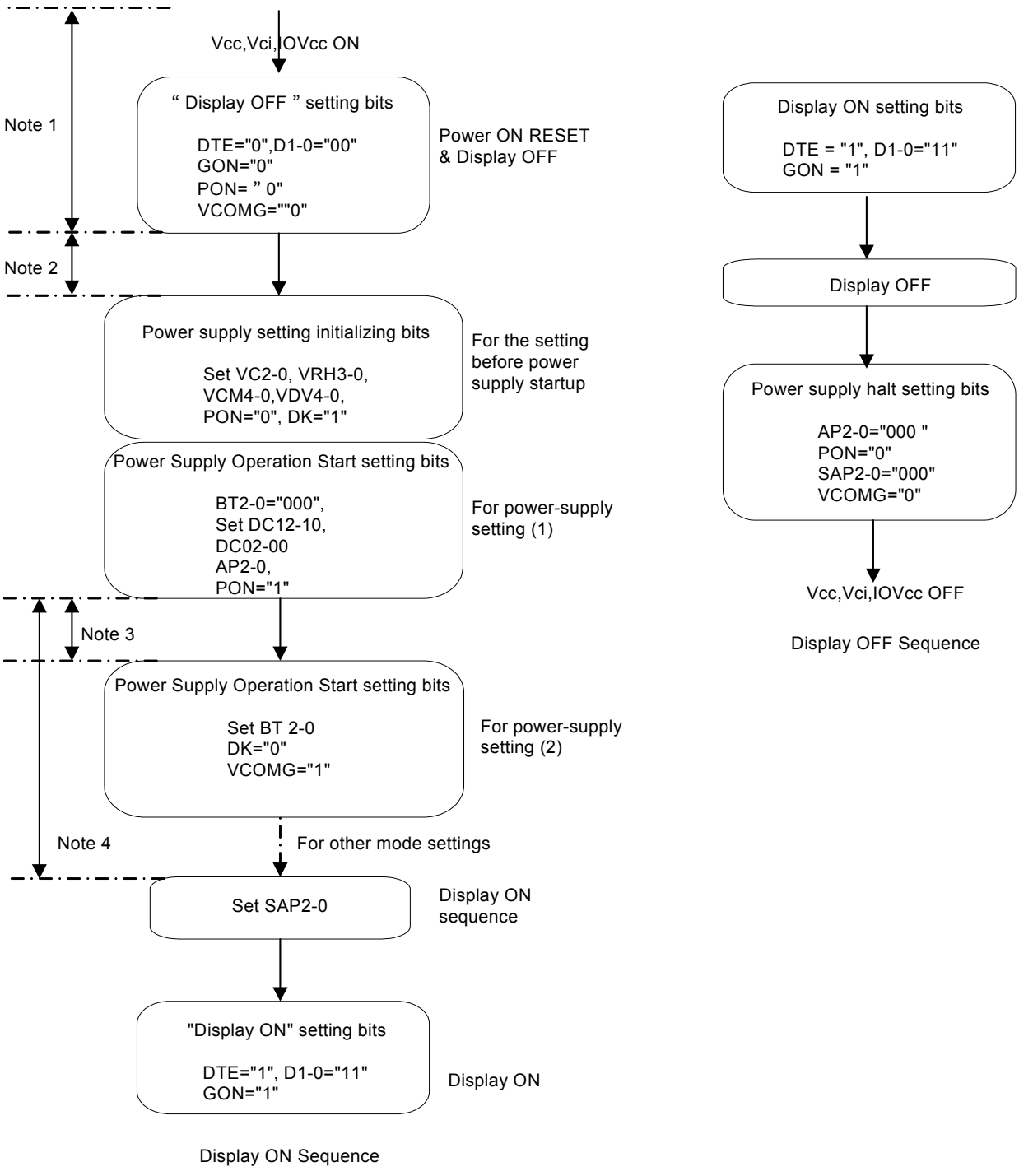


Figure 106 Standby Mode and Sleep Mode Setting Sequence

7.5 Power Supply Setting

The power supply setting sequence of the FGD0801 is as following.



Note1)1ms or more
Note2)10ms or more Oscillation Circuit Stabilizing time
Note3)40ms or more Step-up Circuit Stabilizing time
Note4)100ms or more Operational Amplifier Stabilizing Time

Figure 107 Power Supply Setting Flow

8. Electrical Characteristic

8.1 Absolute Maximum Ratings

The following table describes the absolute maximum ratings .The LSI may be permanently damaged if out of the absolute maximum ratings. It is crucial to use the LSI within the following electrical characteristics limitation, as the LSI will malfunction and cause poor reliability if the electrical characteristics conditions are exceeded.

Item	Symbol	Unit	Value	Note
Power Supply Voltage (1)	VCC, IOVCC	V	-0.3 to +4.6	1,2
Power Supply Voltage (2)	VCI ~ VSSA	V	-0.3 to +4.6	1,3
Power Supply Voltage (3)	VLCD ~ VSSA	V	-0.3 to +6.0	1,4
Power Supply Voltage (4)	VSSA ~ VCL	V	-0.3 to +4.6	1,5
Power Supply Voltage (5)	VLCD ~ VCL	V	-0.3 to +9.0	1,5
Power Supply Voltage (6)	VGH ~ VSSA	V	-0.3 to +18.5	1,6
Power Supply Voltage (7)	VSSA ~ VGL	V	-0.3 to +16.5	1,7
Input Voltage	Vt	V	-0.3 to Vcc+0.3	1
Operating Temperature	Topr	°C	-40 to +85	8,9
Storage Temperature	Tstg	°C	-55 to +110	8,9

Table 64 Absolute Maximum Rating

Notes: 1. VCC, VSSD must be maintained.
2. (High) VCC ≥ VSSD (Low), (High) IOVCC ≥ VSSD (Low).
3. To make sure (High) VCI ≥ VSSA (Low).
4. To make sure (High) VLCD ≥ VSSA (Low).
5. To make sure (High) VLCD ≥ VCL (Low).
6. To make sure (High) VGH ≥ VSSA (Low).
7. To make sure (High) VSSA ≥ VGL (Low).
8. For die and wafer products, specified up to +85°C.
9. This temperature specifications apply to the COG package.

8.2 AC Characteristic

Clock Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
External clock frequency	fcp	KHz	100	176	600	VCC= 2.4 ~ 3.3V
External clock duty ratio	Duty	%	45	50	55	VCC=2.4 ~ 3.3V
External clock rise time	Trcp	μs	-	-	0.2	VCC= 2.4 ~ 3.3V
External clock fall time	Tfcp	μs	-	-	0.2	VCC= 2.4 ~ 3.3V
R-C oscillation clock	fosc	KHz	260	270	280	VCC= 2.4 ~ 3.3V

Table 65 Clock Characteristics ((IOVCC = 1.65 ~ 3.3V, VCC = 2.4 ~ 3.3V)

80/68-System(18/16 Bits) Bus Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	200	-	-	Figure 108
	Read	t_{CYCR}	ns	500	-	-	Figure 108
Write low-level pulse width		PW_{LW}	ns	50	-	-	Figure 108
Read low-level pulse width		PW_{LR}	ns	150	-	-	Figure 108
Write high-level pulse width		PW_{HW}	ns	50	-	-	Figure 108
Read high-level pulse width		PW_{HR}	ns	150	-	-	Figure 108
Write / Read rise / fall time		t_{WRr} ,t_{WRf}	ns	-	-	-	Figure 108
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	20	-	-	Figure 108
	Read (RS to NCS, RW_NRD)			20	-	-	Figure 108
Address hold time		t_{AH}	ns	5	-	-	Figure 108
Write data setup time		t_{DSW}	ns	15	-	-	Figure 108
Write data hold time		t_H	ns	15	-	-	Figure 108
Read data delay time		t_{DDR}	ns	120	-	-	Figure 108
Read data hold time		t_{DHR}	ns	10	-	-	Figure 108

Table 66 80-System Normal Write Mode (IOVCC = 1.65 ~ 3.3V,VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	200	-	-	Figure 109
	Read	t_{CYCR}	ns	500	-	-	Figure 109
Write low-level pulse width		PW_{LW}	ns	50	-	-	Figure 109
Read low-level pulse width		PW_{LR}	ns	150	-	-	Figure 109
Write high-level pulse width		PW_{HW}	ns	50	-	-	Figure 109
Read high-level pulse width		PW_{HR}	ns	150	-	-	Figure 109
Write / Read rise / fall time		t_{WRr} ,t_{WRf}	ns	-	-	-	Figure 109
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	20	-	-	Figure 109
	Read (RS to NCS, RW_NRD)			20	-	-	Figure 109
Address hold time		t_{AH}	ns	5	-	-	Figure 109
Write data setup time		t_{DSW}	ns	15	-	-	Figure 109
Write data hold time		t_H	ns	15	-	-	Figure 109
Read data delay time		t_{DDR}	ns	120	-	-	Figure 109
Read data hold time		t_{DHR}	ns	10	-	-	Figure 109

Table 67 68-System Normal Write Mode (IOVCC = 1.65 ~ 3.3V,VCC=2.4~3.3V)

Serial Data Transfer Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	us	120	-	-	Figure110
	Read (transmitted)	t_{SCYC}	us	300	-	-	Figure110
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	50	-	-	Figure110
	Read (transmitted)	t_{SCH}	ns	150	-	-	Figure110
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	50	-	-	Figure110
	Read (transmitted)	t_{SCL}	ns	150	-	-	Figure110
Serial clock rise / fall time		t_{scr}, t_{scf}	ns	-	-	-	Figure110
Chip select set up time		t_{CSU}	ns	20	-	-	Figure110
Chip select hold time		t_{CH}	ns	-	-	-	Figure110
Serial input data set up time		t_{SISU}	ns	20	-	-	Figure110
Serial input data hold time		t_{SIH}	ns	20	-	-	Figure110
Serial output data set up time		t_{SOD}	ns	120	-	-	Figure110
Serial output data hold time		t_{SOH}	ns	-	-	-	Figure110

Table 68 (IOVCC=1.65~3.3V,VCC=2.4~3.3V)

RGB Interface Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	t_{SYNCS}	ns	20	-	-	Figure111
ENABLE set up time	t_{ENS}	ns	20	-	-	Figure111
ENABLE hold time	t_{ENH}	ns	20	-	-	Figure111
DOTCLK “low” level pulse width	PW_{DL}	ns	40	-	-	Figure111
DOTCLK “high” level pulse width	PW_{DH}	ns	40	-	-	Figure111
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	Figure111
DATA set up time	t_{DBS}	ns	40	-	-	Figure111
DATA hold time	t_{DBH}	ns	100	-	-	Figure111
DOTCLK , VSYNC , HSYNC rising and falling time	t_{rgbr} , t_{rgbf}	ns	-	-	-	Figure111

Table 69 18-/16-bit Bus RGB Interface Mode (IOVCC=1.65~3.3V) / (VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	t_{SYNCS}	ns	20	-	-	Figure111
ENABLE set up time	t_{ENS}	ns	20	-	-	Figure111
ENABLE hold time	t_{ENH}	ns	20	-	-	Figure111
DOTCLK “low” level pulse width	PW_{DL}	ns	40	-	-	Figure111
DOTCLK “high” level pulse width	PW_{DH}	ns	40	-	-	Figure111
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	Figure111
DATA set up time	t_{DBS}	ns	40	-	-	Figure111
DATA hold time	t_{DBH}	ns	100	-	-	Figure111
DOTCLK , VSYNC , HSYNC rising and falling time	t_{rgbr} , t_{rgbf}	ns	-	-	-	Figure111

Table 70 6-bit Bus RGB Interface Mode (IOVCC=1.65~3.3V,VCC=2.4~3.3V)

8.3 DC Characteristic

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	IOVCC=1.65～3.3V; VCC=2.4～3.3V	0.8*IOVCC	-	-	-
Input low voltage	V_{IL}	V	IOVCC=1.65～3.3V; VCC=2.4～3.3V	-	-	0.2*IOVCC	-
Output high voltage	V_{OH}	V	IOH=-0.1mA	0.9*IOVCC	-	-	-
Output low voltage	V_{OL}	V	IOVCC=1.65～3.3V; VCC=2.4～3.3V; IOL=0.1mA	-	-	0.1*IOVCC	-
I/O leakage current	I_{LI}	uA	VIN=0～IOVCC	-0.1	-	0.1	IOVCC=2.8V
Current consumption during normal operation (VCC-VSSD)	I_{CP}	uA	IOVCC=3.0V,VCC=3.0V, VGAM1OUT=4.93V,VLCDC=5.5V(VC=3'b001,0.92*VCI),fosc=236KHz(160 line),Ta=25ºC,GRAM data=0000h,REV="1",SAP="100",ON4-0="0",OP4-0="0",MP52-00="0",MN52-00="0",CP12-00="0",CN12-00="0"	-	120uA (VCC)	200uA (VCC)	-
Current consumption during standby mode (VCC-VSSD)	I_{ST}	uA	IOVCC=3.0V,VCC=3.0V, Ta=25ºC	-	10(IOVCC,VCC)	40(IOVCC,VCC)	-
Output voltage deviation		mV	-	-	30mV	-	-
Dispersion of the Average Output Voltage	V	mV	-	-50mV	-	10mV	-

Table 71 DC Characteristic (IOVCC=1.65～3.3V, VCC=2.4～3.3V, Ta=-40ºC～85ºC)

8.4 Clock Charateristic

Item	Symbol	Unit	Test Conditon	Min.	Typ.	Max.
RC Oscillation Clock	f_{OSC}	KHz	R_f=100KΩ, VCC=3.0V	260	270	280

Table 72 Clock Characteristics (VCC = 2.4~3.3V,IOVCC = 1.65~3.3V)

8.5 Reset Timing Characteristic

Item	Symbol	Unit	Test Conditon	Min.	Typ.	Max.
Reset low-level width	tRES	ms	Figure 113 Reset Timing	1	-	-
Reset rise time	trRES	us	Figure 113 Reset Timing	-	-	10

Table 73 Reset Timing Characteristics (VCC = 2.4~3.3V,IOVCC = 1.65~3.3V)

8.6 LCD Driver output characteristics

Item	Symbol	Unit	Test Conditon	Min.	Typ.	Max.
Driver output delay time	tdd	us	IOVCC=3V,VCC=3V,VGAM1OUT=5.0V, RC oscillation: Fosc=315KHz (160 lines), Ta=25ºC, REV=0, SAP=010, AP=010, ON14-00=0, OP14-00=0, MP52-00=0, MN52-00=0, CP12-00=0, CN12-00=0, Load Resistance R=10KΩ, Load Capacitance=20pF, ● when the level changes from a same grayscale level on all pins ● Time to reach +/-35mv when VCOM polarity inverts	-	35	-

Table 74 LCD Driver Output Characteristics

8.7 Timing Characteristic

80-System Bus Operation

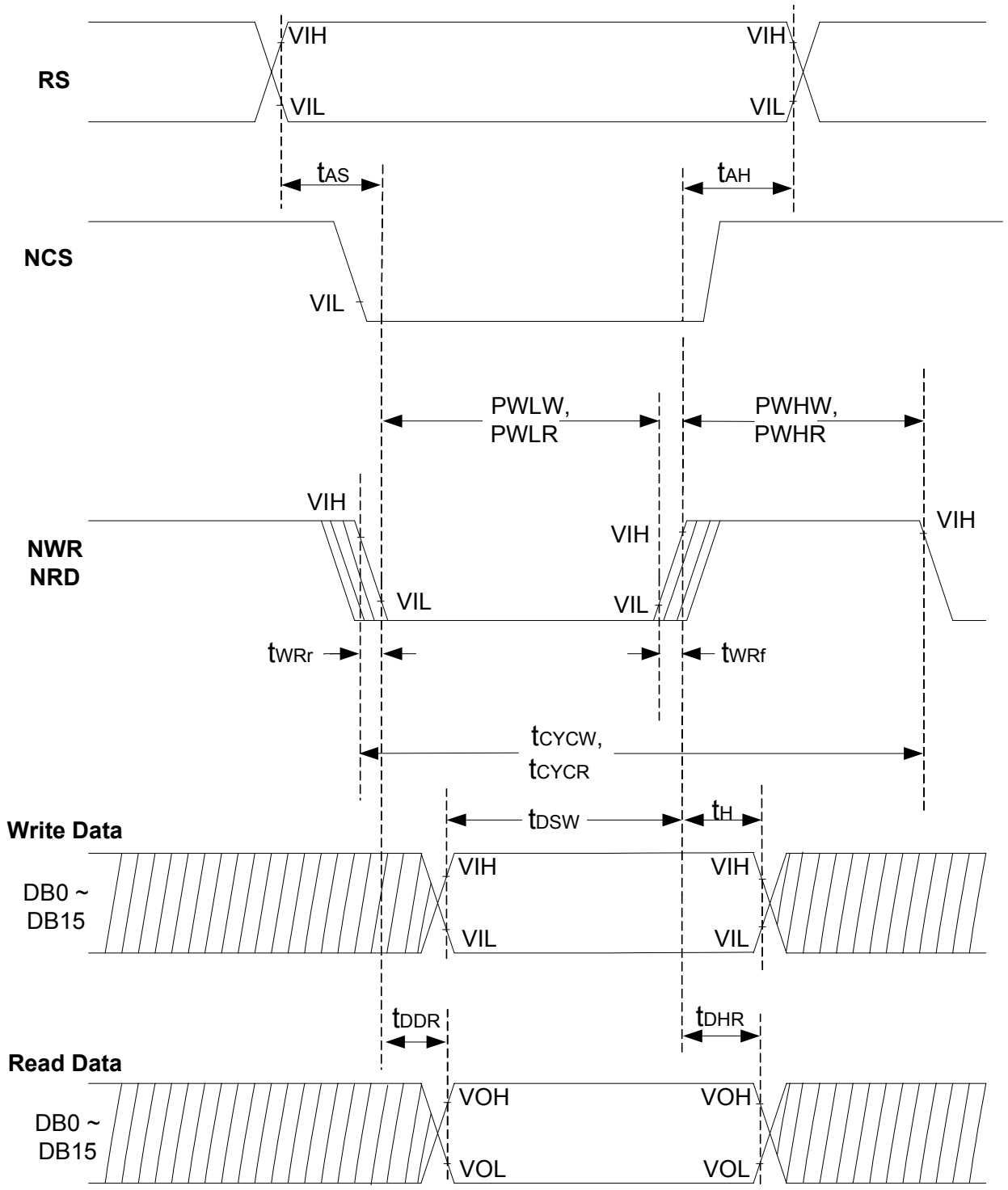


Figure 108109 80-System Bus Timing

68-system Bus Operation

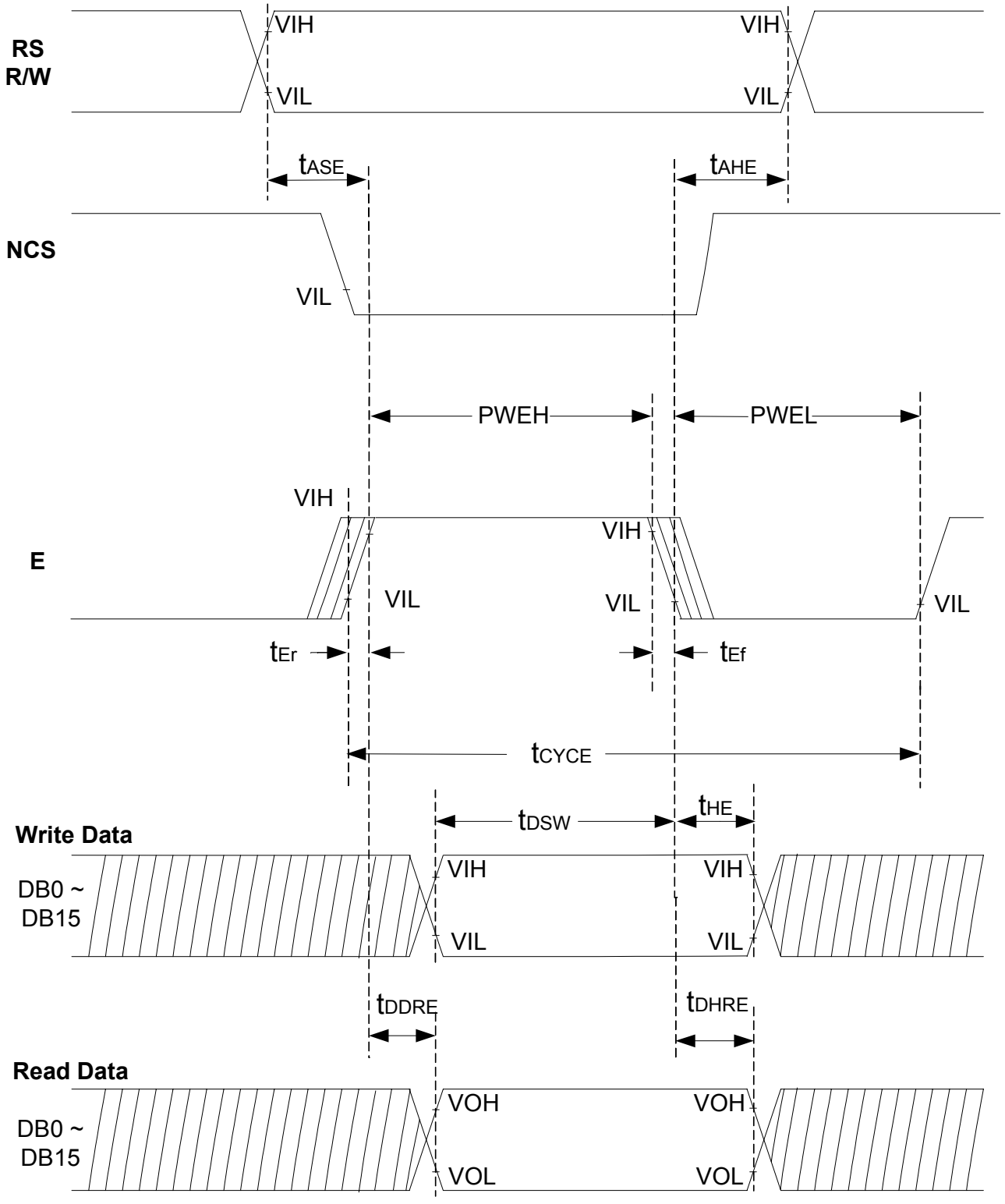


Figure 110 68-system Bus Operation

Clock Synchronized Serial Data Transfer Interface Operation

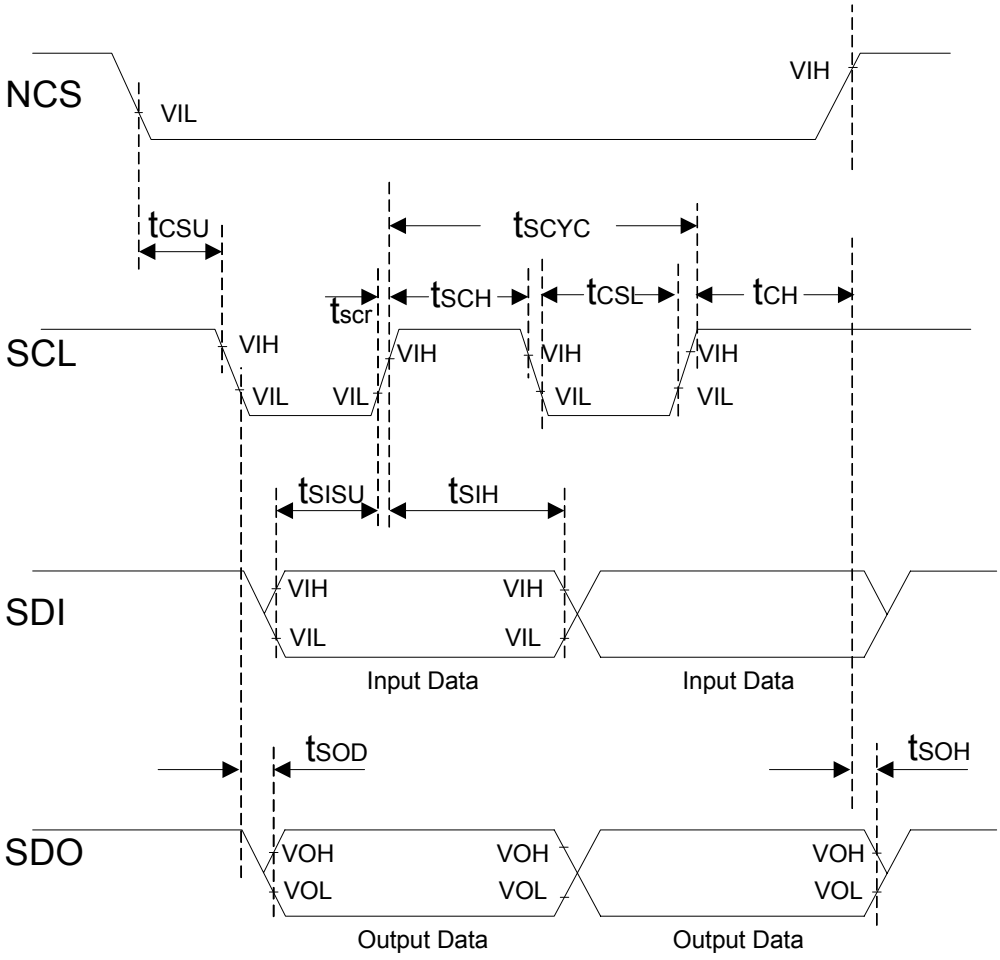


Figure 111 Clock Synchronized Serial Data Transfer Interface Timing

RGB Interface Operation

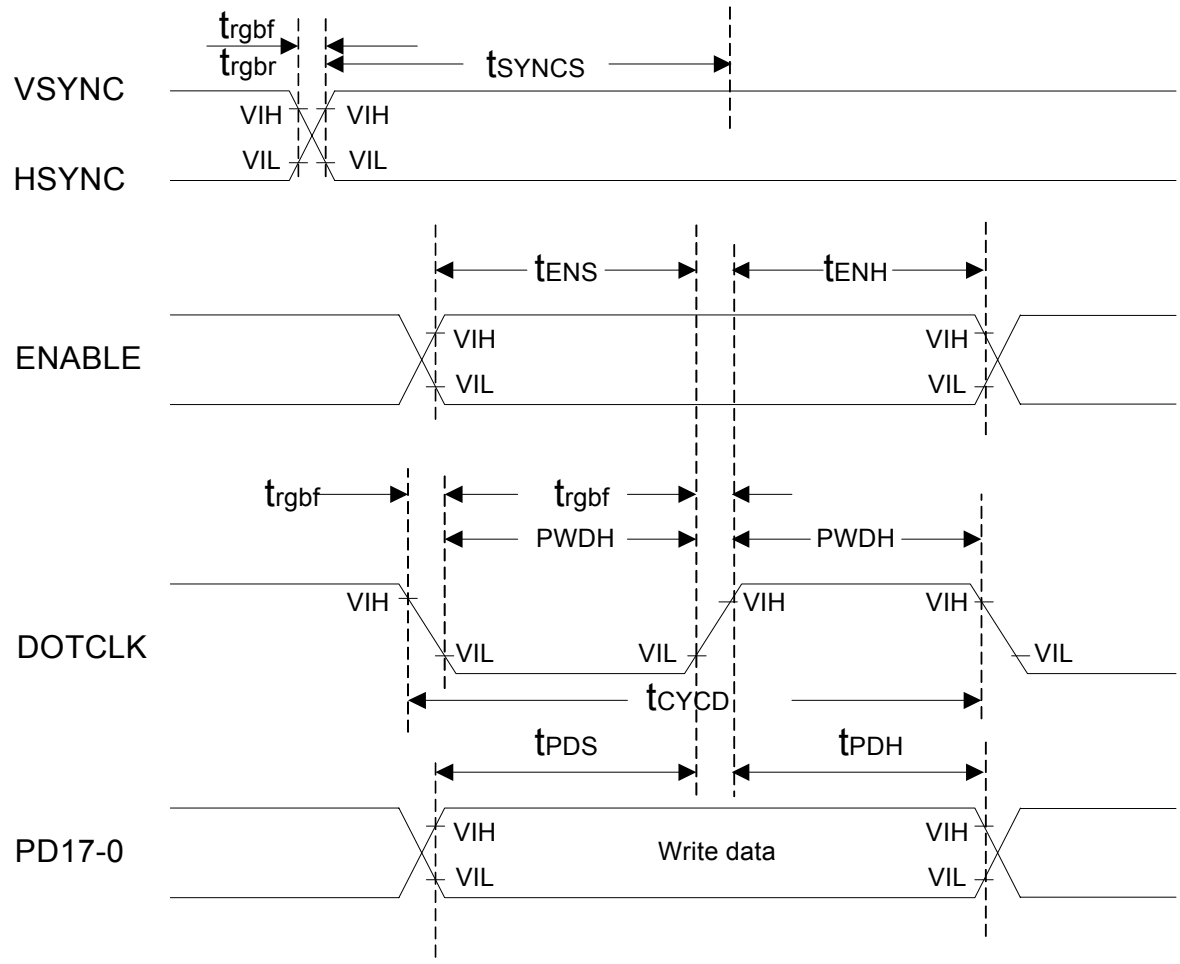


Figure 112 RGB Interface Operation

LCD Driving Output

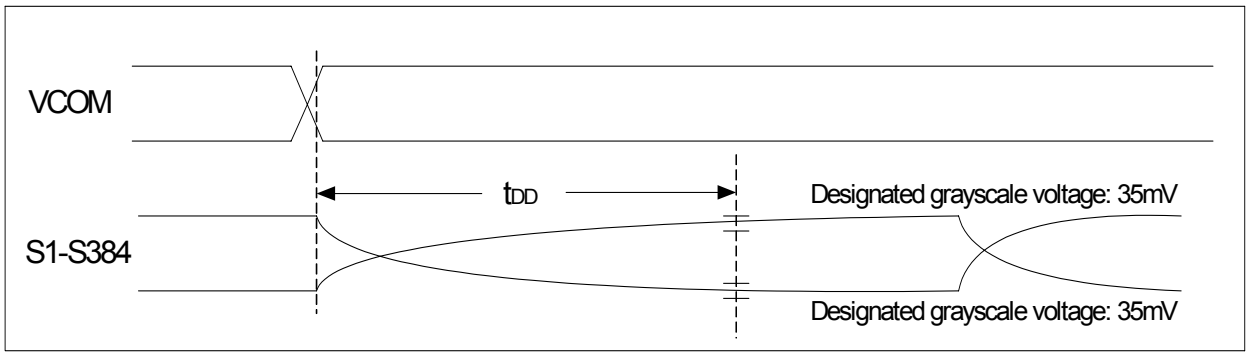


Figure 113 LCD Driving Output

Reset Operation

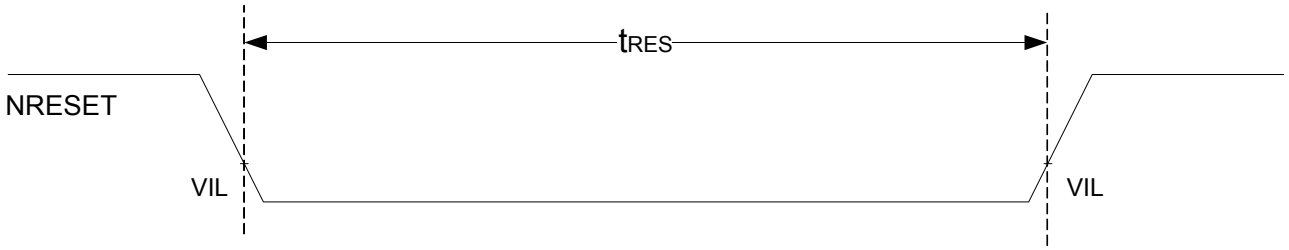


Figure 114 Reset Timing

9. System Configuration

9.1 System Diagram

The system configuration diagram illustrates as following:

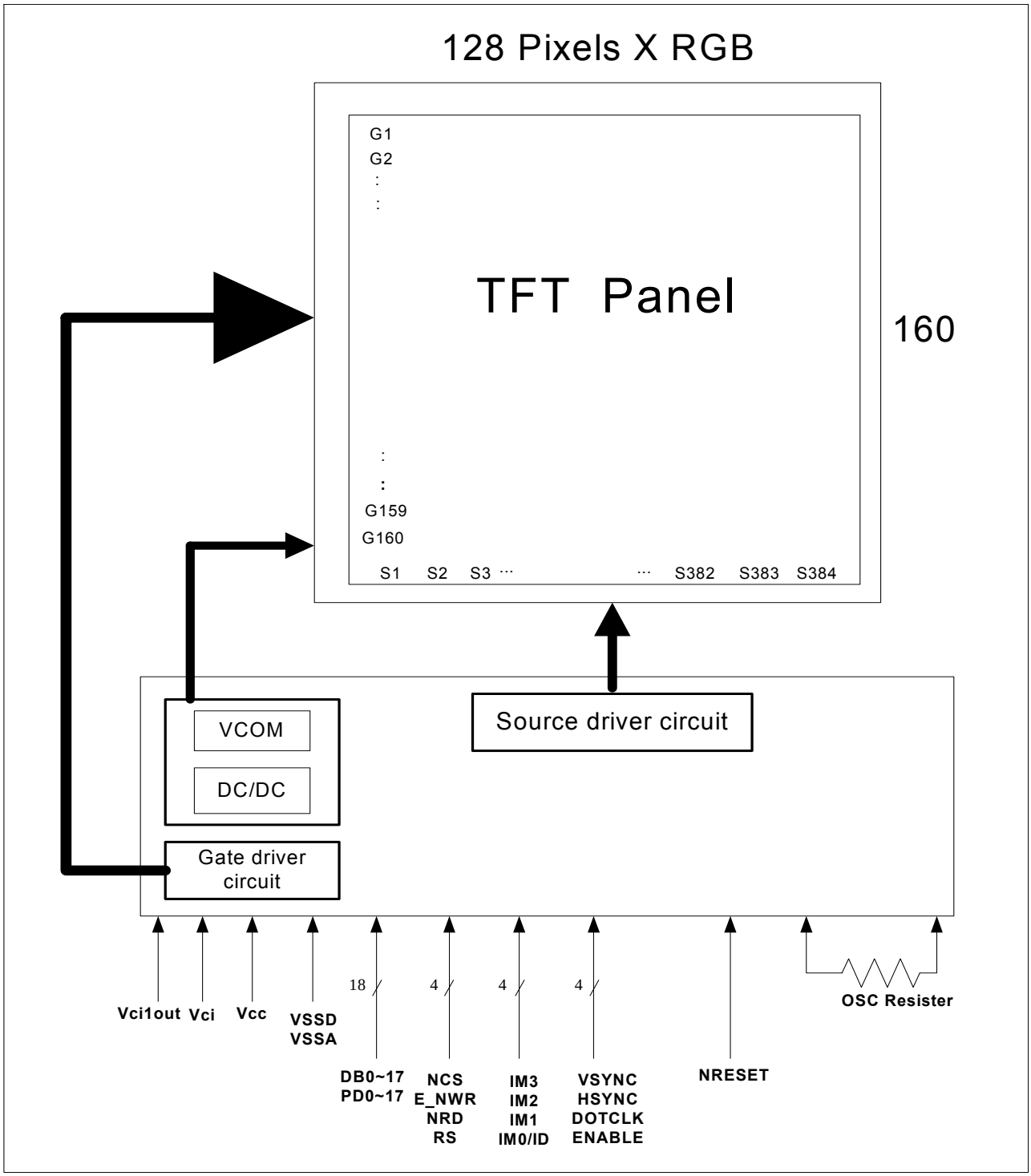


Figure 115 System Diagram of FGD0801

9.2 Layout Recommendation

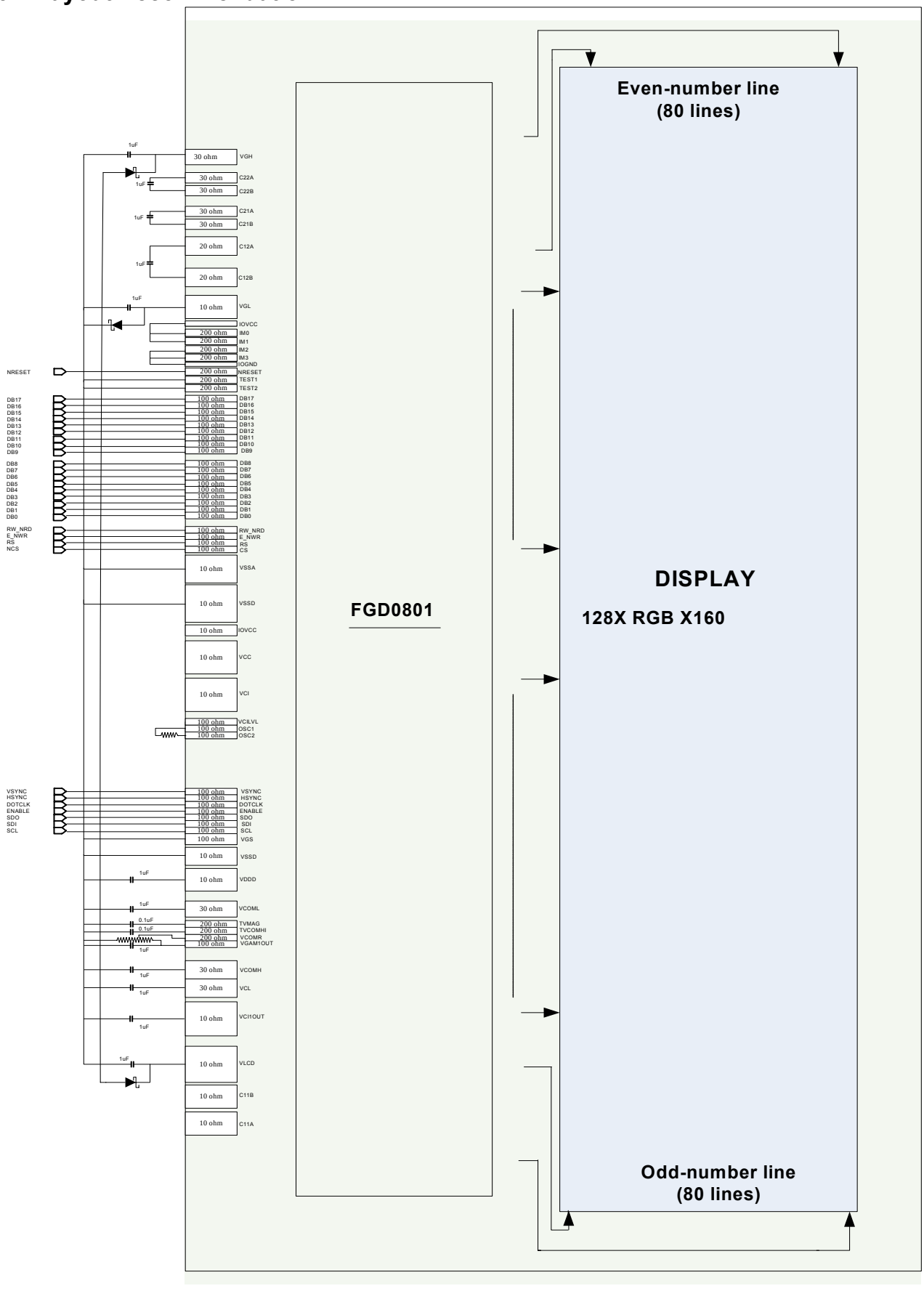


Figure 116 Layout Recommendation