EK79030

Rev. 0.6

PRELIMINARY DATA SHEET

1440CH Source Driver with TCON MIPI/LVDS Interface

fitipower integrated technology Inc.

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Single Chip 1440 Channel Source Driver with Timing Controller for TFT LCD

1. GENERAL DESCRIPTION

The EK79030 is a highly integrated solution for small size to middle size α-Si TFT-LCD panels. This chip integrates 1440ch source driver with MIPI/LVDS input interface.

2. FEATURES

- Integrate 1440 channel source driver and timing controller
- Display Resolution :
  - 400 x RGB x (1280, (8 x SLN)), (Source output from S1201 to S2400)
  - 480 x RGB x (1280, (8 x SLN)), (Source output from S961 to S2400)
- Full color mode:
  - 16.7M colors (24-bit per pixel, R:G:B = 8:8:8)

  Reduced color mode:
  - 262K colors (18-bit per pixel, R:G:B = 6:6:6)
  - 65K colors (16-bit per pixel, R:G:B = 5:6:5)

- System Interfaces:
  - MIPI DSI (3/4 data lane): MIPI DSI(DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01)
  - LVDS interface(DE mode only)

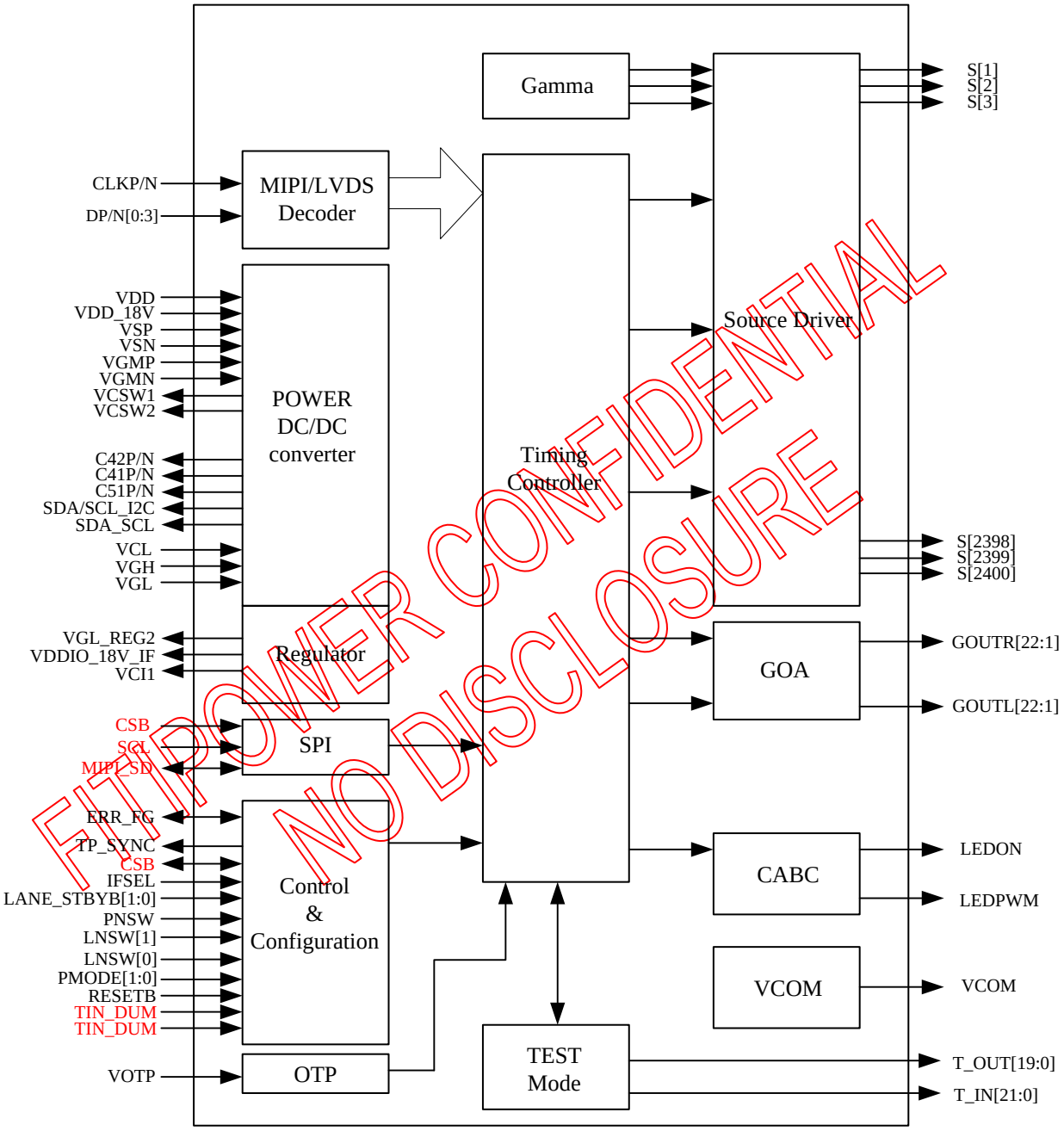
- Gate driver control signals for GIP
- Internal level shifter for Gate driver control
- Support SPI/I2C interface
- Supports 1-dot / 2-dot / 4-dot / Column inversion
- Gamma correction (1 preset gamma curve)
- GAS function for preventing image sticking when abnormal power off
- Support DC COM driving
- Built-In Charge pump for VGH / VGL , and VCOM generator
- Built-In Enhanced BIST pattern
- Support for Programming Gamma correction
- Support Dither Function
- OTP memory to store initialization register settings
- Built-In OTP (4 Times) to store VCOM calibration
- Built-In OTP (1 Times) to store gamma, panel timing, and analog power setting
- COG package

- Input voltage ranges:
  - I/O and interface power supply (VDDIO): 1.8V to 5.5V
  - High speed interface power supply (VDDIO_IF): 1.8V to 5.5V
  - Analog power supply (VDD): 2.5V to 6.0V
  - DC/DC set-up supply (VDDP): 2.5V to 6.0V
  - OTP programming voltage (VOTP): 7.5V+/- 0.2V
  - Analog voltage range for VSP to VSSP: 4.5V to 6.0V
  - Analog voltage range for VSN to VSSP: -4.5V to -6.0V
  - Analog voltage range for VGH to VSSP: 9.0V to 20V
  - Analog voltage range for VGL to VSSP: -9V to -18V
  - VGH,VGL: VGH-VGL<32V

- Output voltage ranges:
  - Analog voltage range for VSP to VSSP: 4.5V to 6.0V
  - Analog voltage range for VSN to VSSP: -4.5V to -6.0V
  - Analog voltage range for VCL to VSSP: -3.0V

- Positive source output voltage level: VGMP= 3.5V to 5.8V
- Negative source output voltage level: VGMN= -3.5V to -5.8V
- Positive gate driver output voltage level: VGH= 9.0V to 20V
- Positive gate driver output voltage level: VGH_REG= 9.0V to 19V
- Negative gate driver output voltage level: VGL= -9V to -18V
- Negative gate driver output voltage level: VGL_REG= -6V to -15V
- VCOM= -3.5V to -0.2V, a step=12mV
- VGH,VGL: VGH-VGL<32V

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

4.1 Pin define

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td colspan="3">Interface and Control</td></tr>
<tr><td>DP[0]/DN[0]
DP[1]/DN[1]
DP[2]/DN[2]
DP[3]/DN[3]</td><td>Input</td><td>MIPI or LVDS data Input. Select by “IFSEL” pin.</td></tr>
<tr><td>CKP/CKN</td><td>Input</td><td>MIPI or LVDS clock Input. Select by “IFSEL” pin.</td></tr>
<tr><td rowspan="2">IFSEL</td><td rowspan="2">Input</td><td>“0” : LVDS interface</td></tr>
<tr><td>“1” : MIPI interface (default)</td></tr>
<tr><td>LNSW[1:0]
(VDDIO)</td><td>Input</td><td>MIPI data lane swapping selection pins.
<table>
<tr><th rowspan="2">LNSW[1:0]</th><th colspan="5">MIPI Lane Mapping</th></tr>
<tr><th>D0(PAD)</th><th>D1(PAD)</th><th>CLK(PAD)</th><th>D2(PAD)</th><th>D3(PAD)</th></tr>
<tr><td>00</td><td>D3</td><td>D2</td><td>CLK</td><td>D1</td><td>D0</td></tr>
<tr><td>01</td><td>D3</td><td>D0</td><td>CLK</td><td>D1</td><td>D2</td></tr>
<tr><td>10</td><td>D0</td><td>D1</td><td>CLK</td><td>D2</td><td>D3</td></tr>
<tr><td>11</td><td>D2</td><td>D1</td><td>CLK</td><td>D0</td><td>D3</td></tr>
</table>
Note: MIPI data lane sequence are unused when IFSEL=”0”
LVDS data/clk lane swapping selection pins.
<table>
<tr><th rowspan="2">LNSW[1:0]</th><th colspan="5">LVDS Lane Mapping</th></tr>
<tr><th>D0(PAD)</th><th>D1(PAD)</th><th>CLK(PAD)</th><th>D2(PAD)</th><th>D3(PAD)</th></tr>
<tr><td>00</td><td>D3</td><td>D2</td><td>CLK</td><td>D1</td><td>D0</td></tr>
<tr><td>01</td><td>D3</td><td>CLK</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>10</td><td>D0</td><td>D1</td><td>CLK</td><td>D2</td><td>D3</td></tr>
<tr><td>11</td><td>D0</td><td>D1</td><td>D2</td><td>CLK</td><td>D3</td></tr>
</table>
Note: LVDS data lane sequence are unused when IFSEL=”1”
Detail LVDS lane swapping please refer section 8.4.2</td></tr>
<tr><td>PNSW
(VDDIO)</td><td>Input</td><td>MIPI/LVDS polarity selection pins.
<table>
<tr><th rowspan="2">PNSW</th><th colspan="5">MIPI/LVDS Lane Mapping</th></tr>
<tr><th>D0P/N</th><th>D1P/N</th><th>CLKP/N</th><th>D2P/N</th><th>D3P/N</th></tr>
<tr><td>0</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>1</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
</table></td></tr>
<tr><td>PMODE[1:0]
(VDDIO)</td><td>Input</td><td>Power mode selection. Normally pull high.
<table>
<tr><th>PMODE[1:0]</th><th>VSP</th><th>VSN</th><th>VGH</th><th>VGL</th></tr>
<tr><td>00</td><td>JD5001/2</td><td>JD5001/2</td><td>External</td><td>External</td></tr>
<tr><td>01</td><td>External</td><td>External</td><td>Charge pump</td><td>Charge pump</td></tr>
<tr><td>10</td><td>JD5001/2</td><td>JD5001/2</td><td>Charge pump</td><td>Charge pump</td></tr>
<tr><td>11</td><td>External</td><td>External</td><td>External</td><td>External</td></tr>
</table></td></tr>
<tr><td>RES[2:0]
(VDDIO)</td><td>Input</td><td>Panel resolution setting selection.
<table>
<tr><th colspan="3">RESOL[2:0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>400RGB x 1280
480RGB x 1280</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>LVBIT
(VDDIO)</td><td>Input</td><td>6-bit / 8-bit input select for LVDS mode. Normally pull high.
(only for LVDS, MIPI Mode = Dummy)
LVBIT = L, 6-bit.
LVBIT = H, 8-bit. (Default)</td></tr>
<tr><td>LVFMT
(VDDIO)</td><td>Input</td><td>8-bit input format select for LVDS mode. Normally pull high.
(only for LVDS, MIPI Mode = Dummy)
LVFMT = L, JEIDA format.
LVFMT = H, VESA format. (Default)</td></tr>
<tr><td>RESETB
(VDDIO)</td><td>Input</td><td>Global reset pin. Normally pull high.
RESETB = L, The controller is in reset state.
RESETB = H, Normal operation.(Default)
Suggest to connecting with an RC reset circuit for stability.</td></tr>
<tr><td>LANE[1]_STBYB
(VDDIO)</td><td>Input</td><td>MIPI mode(IFSEL=1) : MIPI LANE number control pin
LVDS mode(IFSEL=0) : Standby mode signal (low :standby mode)
LANE[1]_STBYB default pull hi
<table>
<tr><th>LANE[1]_STBYB</th><th>LANE[0]_BISTB</th><th>Interface mode</th></tr>
<tr><td>0</td><td>0</td><td>Not used</td></tr>
<tr><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>1</td><td>0</td><td>3 Lanes</td></tr>
<tr><td>1</td><td>1</td><td>4 Lanes (default)</td></tr>
</table></td></tr>
<tr><td>LANE[0]_BISTB
(VDDIO)</td><td>Input</td><td>MIPI mode(IFSEL=1) : MIPI LANE number control pin
LVDS mode(IFSEL=0) : BIST mode signal (low :BIST mode)
LANE[0]_BISTB default pull hi</td></tr>
<tr><td>LEDPWM
(VDDIO)</td><td>Output</td><td>This pin is connected to the external LED driver.
PWM type control signal for brightness of the LED backlight.
If not used, please float this pin.</td></tr>
<tr><td>LEDON
(VDDIO)</td><td>Output</td><td>Back-light enable signal.</td></tr>
<tr><td>CMD_SEL
(VDDIO)</td><td>Input</td><td>Command interface selection. Normally pull high.
<table>
<tr><th>CMD_SEL</th><th>Function</th></tr>
<tr><td>0</td><td>3-Wire (Default)</td></tr>
<tr><td>1</td><td>I2C</td></tr>
</table>MIPI and 3-wire/I2C command can’t receive at the same time.</td></tr>
<tr><td>CSB
(VDDIO)</td><td>Input</td><td>Serial communication enables. Normally pull high</td></tr>
<tr><td>SDA
(VDDIO)</td><td>I/O</td><td>Serial communication data input.</td></tr>
<tr><td>SCL
(VDDIO)</td><td>Input</td><td>Serial communication clock input.</td></tr>
</table>

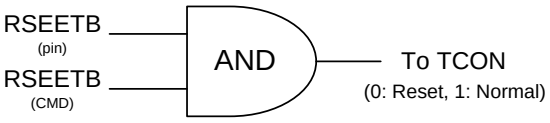
Pin Name	Pin Type	Description
SDA_I2C (VDDIO)	I/O	Serial communication data input.
SCL_I2C (VDDIO)	Input	Serial communication clock input.
Panel driver output		
S[2400:961]	Output	Source Driver output signals. Source output mapping with different resolution. **Resolution** / **Source channel** 400RGB / S[2400:1201] 480RGB / S[2400:961]
SDUMY[3:0]	Output	Source dummy output.
GOUTL[1]~ GOUTL[22]	Output	These pins are used for Panel gate control signals. If not used, let it open.
GOUTR[1]~ GOUTR[22]	Output	These pins are used for Panel gate control signals. If not used, let it open.
Power supply pins		
VDDIO	PI	A power supply for the I/O circuit. VDDIO=1.8V to 5.5V When VDDIO=1.8V, connect VDDIO to VDD_18V.
VDD	PI	A power supply for DC/DC circuit. VDD=2.5V to 6.0V VCI input level should be same as VCIP input level to avoid the level-mismatching at internal level shifter circuit.
VDDP	PI	A power supply for DC/DC circuit. VDD=2.5V to 6.0V VCIP input level should be same as VCI input level to avoid the level-mismatching at internal level shifter circuit.
VDDIO_IF	PI	Interface and I/O power supply for the MIPI power regulator circuits. VDDIO=1.8V to 5.5V. When VDDIO_IF=1.8V, connect VDDIO_IF to VDD_18V_IF.
VDD_18V	Output	Internal power supply for logic circuits. Connect to a stabilizing capacitor.
VDD_18V_IF	Output	Internal power supply for MIPI circuits. Connect to a stabilizing capacitor.
VSSA	PI	Analog ground. VSS=0V. When using the COG method, connect to VSS on the FPC to prevent noise.
VSS	PI	GND for the internal logic. VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VSSP	PI	GND for the DC/DC circuit. VSSP=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VSS_IF	PI	Ground for interface.
VOTP	PI	External high voltage pin used in OTP mode and operates at 7.5V. If not used, let it open.
VSP	PI	Input voltage from the set-up circuit (4.5V to 6.0V). It is generated from VDDP.
VSN	PI	Input voltage from the set-up circuit (-4.5V to -6.0V). It is generated from VSN. Place a schottkey barrier diode between VSN and VGL.
VCL	PO	Input voltage from the set-up circuit (~-3.0V). It is generated from VSN.
VGH	PO	Output voltage from the step-up circuit Connect to stabilizing capacitor between VSSA and VGH.

Pin Name	Pin Type	Description
VGL	PO	Output voltage from the step-up circuit Connect to stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VSSA and VGL.
VCI1	PO	Reference voltage from internal band gap circuit. The tolerance of VCI1 voltage is +/- 3% .
VGMP	PO	Positive regulated voltage output (3.5V to 5.8V)
VGMN	PO	Negative regulated voltage output (-3.5V to -5.8V)
VGH_REG	PO	Regulator output voltage generated from VGH. Connect to a stabilizing capacitor between VSSA and VGH_REG. If not used, please open.
VGL_REG	PO	Regulator output voltage generated from VGL. Connect to a stabilizing capacitor between VSSA and VGL_REG. If not used, please open.
VCOM	PO	The power supply of common voltage in DC com driving. The voltage range is set between -3.5V to -0.2V. It must connected a stabilizing capacitor 2.2u to VSS.
DC/DC pumping		
C41P, C41N C42P, C42N	C	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH voltage. If not used, let them open.
C51P, C51N C11P_VGL, C11N_VGL	C	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGL voltage. If not used, let them open.
VCSW1, VCSW2	PO	**In external power IC mode:** VCSW1 and VCSW2 connect to external power IC. **If not used, Please open these pin.**
Other pins		
TP_SYNC (VDDIO)	Output	Touch sync signal. Float these pins for normal operation.
T_IRX	T	Test pin. Float these pins for normal operation.
T_VREF	T	Test pin. Float these pins for normal operation.
T_IBIAS	T	Test pin. Float these pins for normal operation.
TOUT[15:0]	T	Test pin. Float these pins for normal operation.
T_CSB_DUM	T	Test pin. Float these pins for normal operation.
TEST_EN	T	Test pin. Float these pins for normal operation.
TIN[19:0]	T	Test pin. Float these pins for normal operation.
T_SCL_DUM	T	Test pin. Float these pins for normal operation.
T_SDA_DUM	T	Test pin. Float these pins for normal operation.
TEST_IO[2:0]	T	Test pin. Float these pins for normal operation.
TIN_DUM[10:0]	T	Test pin. Float these pins for normal operation.
T_OTP_RLOAD	T	Test pin. Float these pins for normal operation.
T_VDDN15	T	Test pin. Float these pins for normal operation.
T_VDDN3	T	Test pin. Float these pins for normal operation.
T_EXT_VCOMI	T	Test pin. Float these pins for normal operation.
C13P_DUM	T	Test pin. Float these pins for normal operation.
C12N_DUM	T	Test pin. Float these pins for normal operation.
C12P_DUM	T	Test pin. Float these pins for normal operation.

Note: P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, PS: Power Setting, C: Capacitor pin.

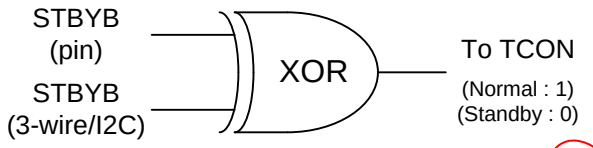
4.2 The relationship between Pin and Register

4.2.1 RESETB PIN/CMD control

Combination Logic	Truth Table
	

RESETB(pin)	GRB(CMD)	TCON
0	0	0
0	1	0
1	0	0
1	1	1

4.2.2 STBYB PIN/CMD control

Combination Logic	Truth Table
For LVDS Register Command interface in use 	

PIN	Register(3wire/I2C)	TCON
0	0	0
0	1	1
1	0	1
1	1	0

4.2.3 Function PIN/CMD control

Combination Logic	Truth Table
	

PIN	Register	TCON
0	0	0
0	1	1
1	0	1
1	1	0

Combination with XNOR
CMD is the function register; include MIPI, 3-wire and I2C command.
Pin the function control pin.
Function list:
IFSEL, LNSW[1:0], PNSW, PMODE[1:0], RES[2:0], LVBIT, LVFMT, LANE[1]_STBYB, LANE[0]_BISTB, CMD_SEL.

4.3 Value of wiring resistance to each pin

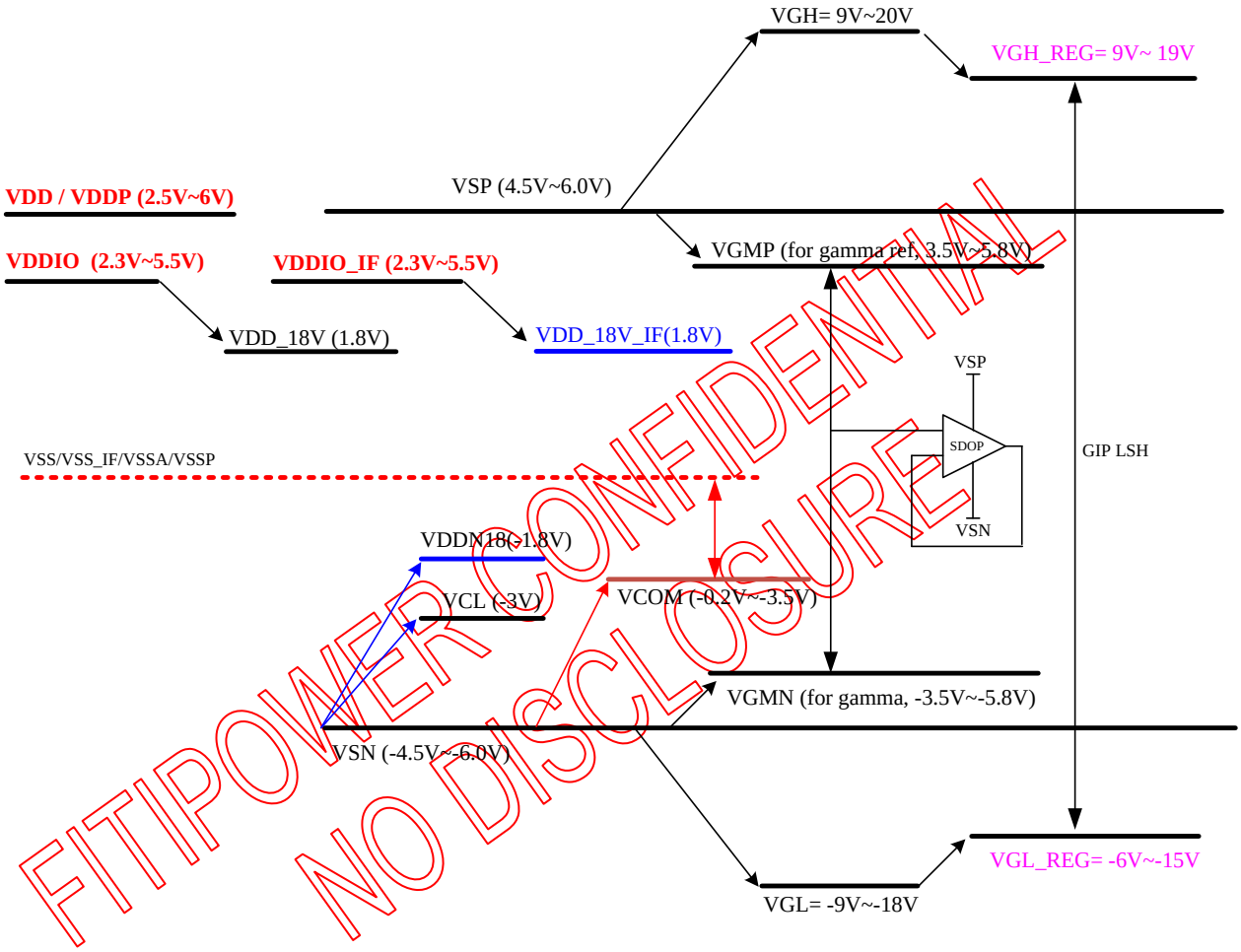
The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Source wiring

Pin name	Wiring resistance (Ω)	Pin name	Wiring resistance (Ω)
DP[0]/DN[0]	<5	VDDIO	<5
DP[1]/DN[1]	<5	VDDIO	<5
DP[2]/DN[2]	<5	VDDP	<5
DP[3]/DN[3]	<5	VDDIO_IF	<5
CKP/CKN	<5	VDD_18V	<5
IFSEL	<100	VDD_18V_IF	<5
LNSW[1:0]	<100	VSSA	<5
PNSW	<100	VSS	<5
PMODE[1:0]	<100	VSSP	<5
RES[2:0]	<100	VSS_IF	<5
LVBIT	<100	VOTP	<5
LVFMT	<100	VSP	<5
RESETB	<100	VSN	<5
LANE[1]_STBYB	<100	VCL	<5
LANE[0]_BISTB	<100	VGH	<5
LEDPWM	<100	VGL	<5
LEDON	<100	VGMP	<5
CMD_SEL	<100	VGMN	<5
CSB	<100	VGH_REG	<5
SDA	<100	VGL_REG	<5
SAL	<100	VCOM	<5
SDA_I2C	<100	C41P/C41N	<5
SCL_I2C	<100	C42P/C42N	<5
VCSW1/VCSW2	<10	C51P/C51N	<5
TP_SYNC	<100	C11P_VGL	<5
GOUTL[1]~GOUTL[22]	<50	C11N_VGL	<5
GOUTR[1]~GOUTR[22]	<50		

5. APPLICATION POWER CIRCUIT

5.1 Power Generation



5.2 Power Supply Configution

Four power structures for different applications controlled by PMODE[1:0] pins, like the following table.

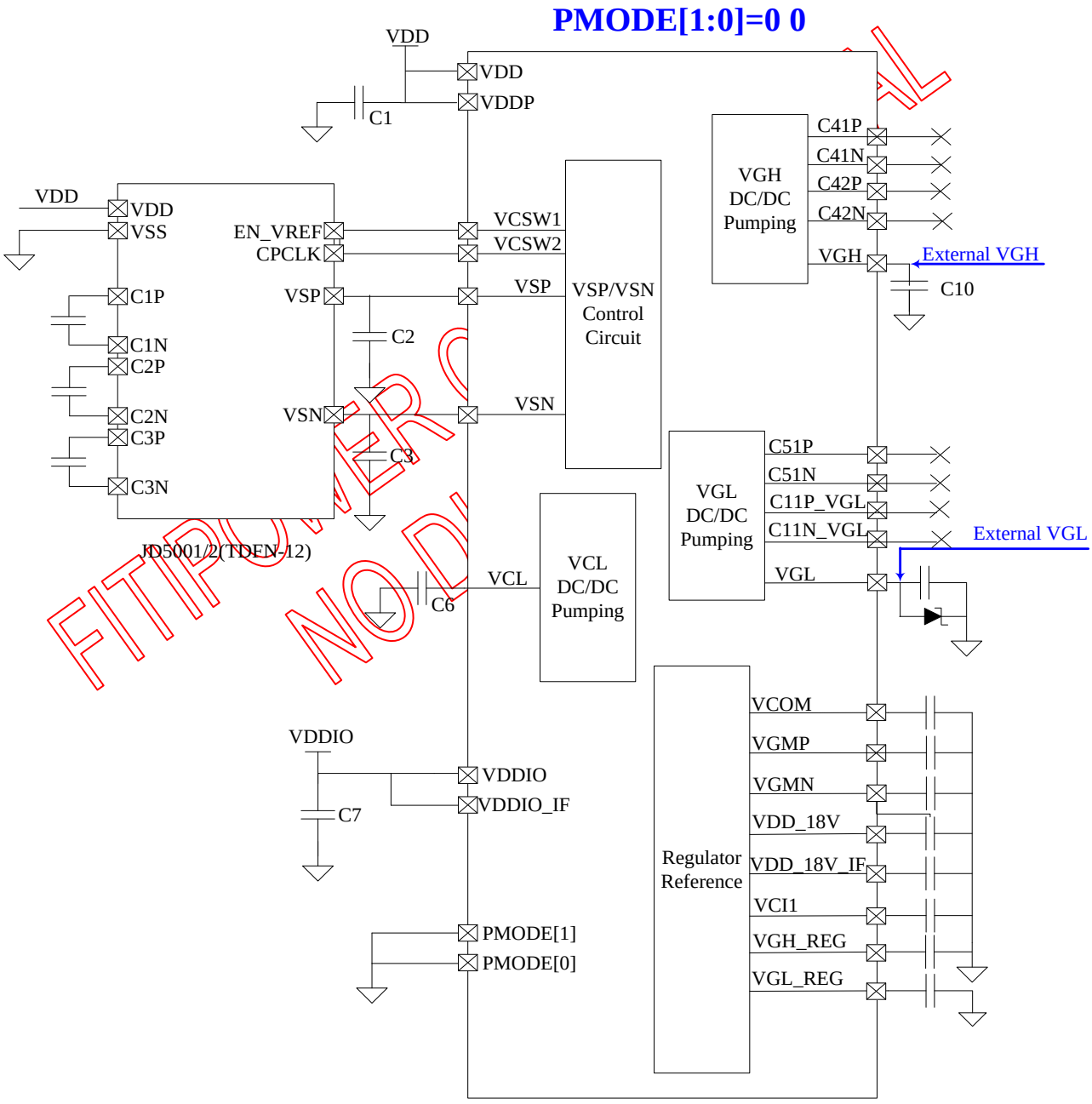
PMODE[1:0]	VSP	VSN	VGH	VGL
00	JD5001/2	JD5001/2	External	External
01	External	External	Charge pump	Charge pump
10	JD5001/2	JD5001/2	Charge pump	Charge pump
11	External	External	External	External

5.3. DC/DC converter circuit

5.3.1 DC/DC power mode 1

VSP/VSN with JD5001/2 controlled by driver IC
External power input: VDDIO(VDDIO_IF), VDD(VDDP), VGH, VGL

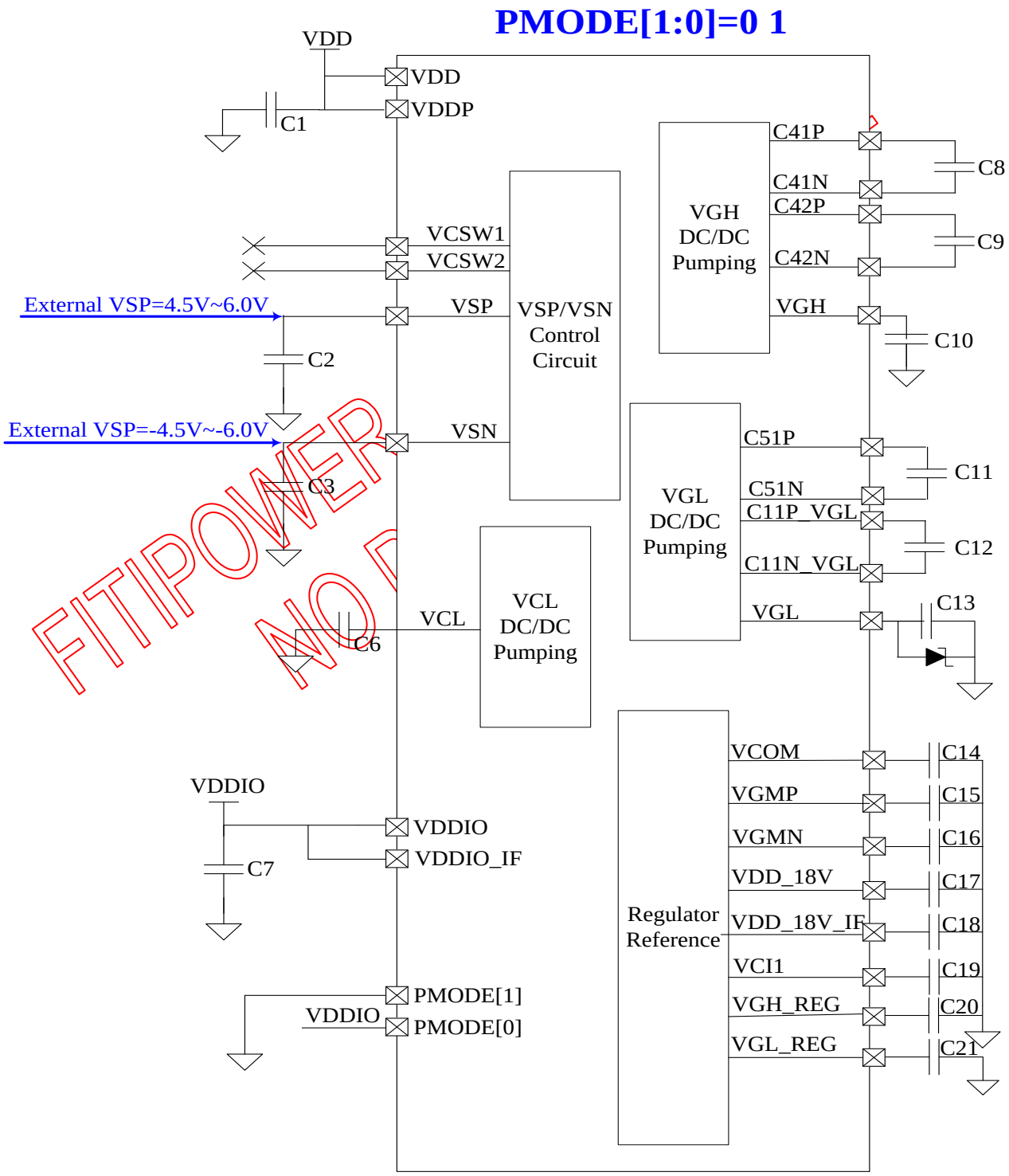
VDDIO=VDDIO_IF=1.8~5.5V, VDD=VDDP=2.5~4.8V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



5.3.2 DC/DC power mode 2

Charge Pump: VGH, VGL
External power input: VDDIO(VDDIO_IF), VDD(VDDP), VSP, VSN

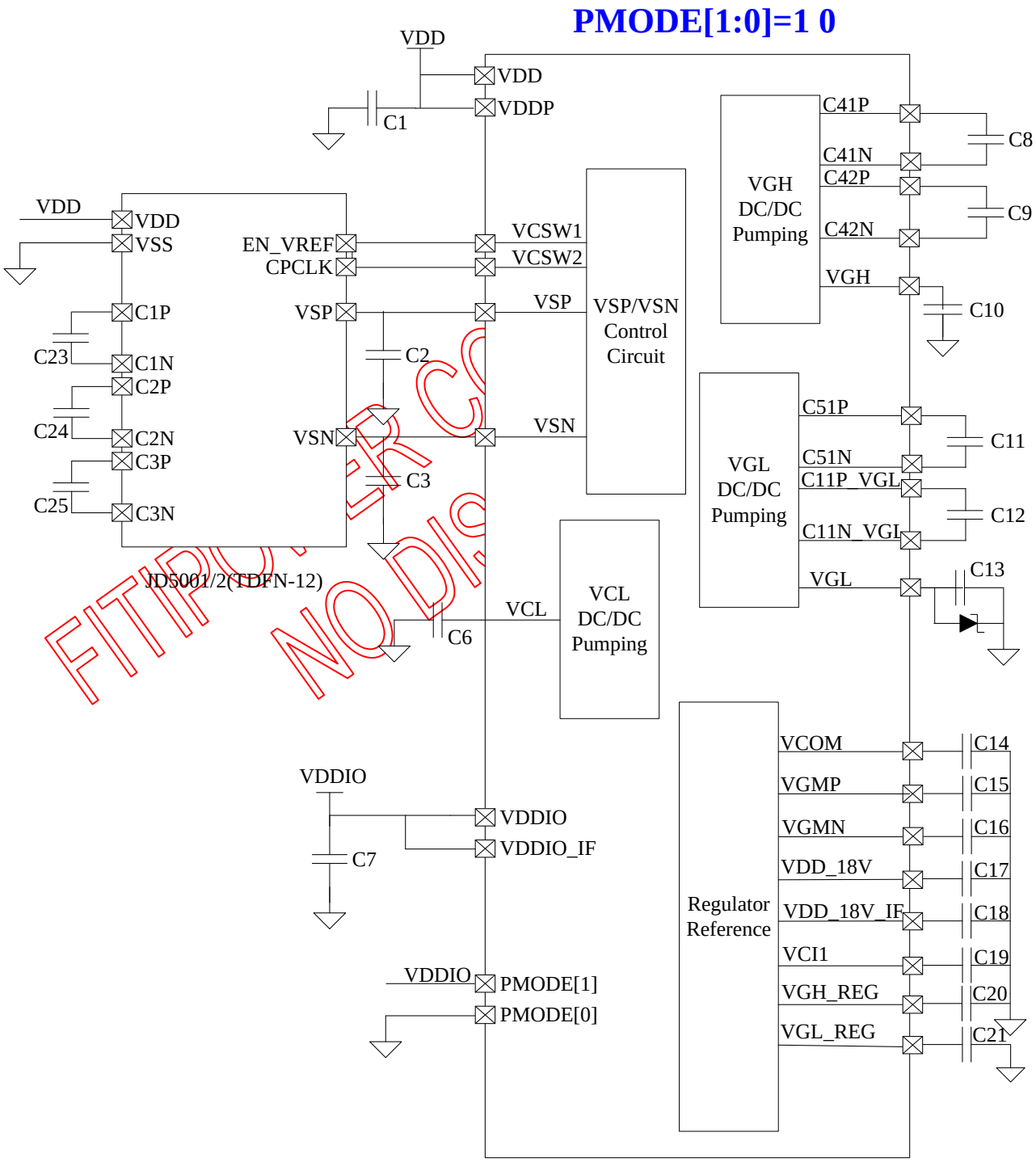
VDDIO=VDDIO_IF=1.8~5.5V, VDD=VDDP=2.5~6.0V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



5.3.3 DC/DC power mode 3

VSP/VSN with JD5001/2 controlled by driver IC; Charge Pump: VGH, VGL
External power input: VDDIO(VDDIO_IF), VDD(VDDP)

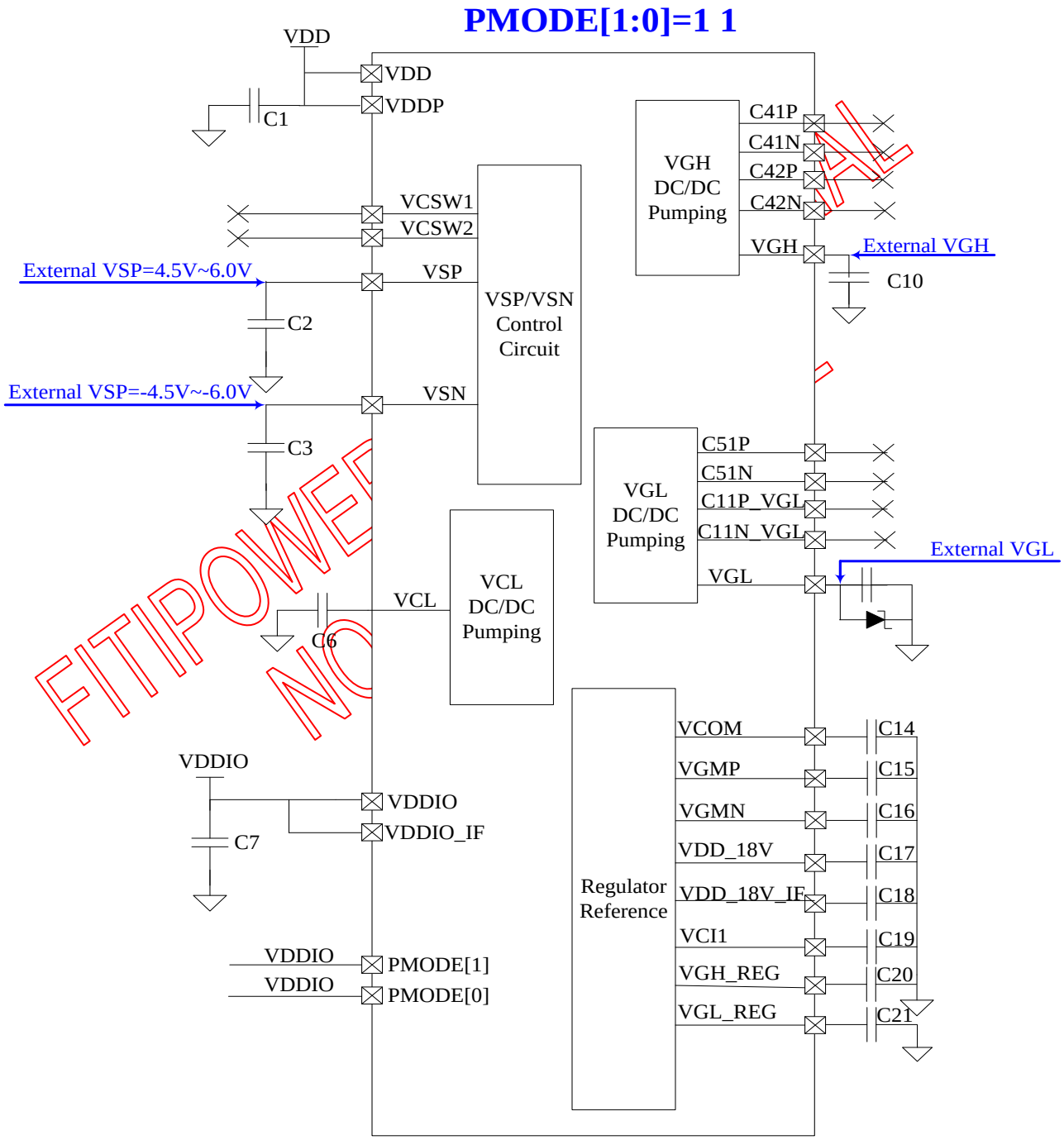
VDDIO=VDDIO_IF=1.8~5.5V, VDD=VDDP=2.5~4.8V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



5.3.4 DC/DC power mode 4

External power input: VDDIO(VDDIO_IF), VDD(VDDP), VSP, VSN, VGH, VGL

VDDIO=VDDIO_IF=1.8~5.5V, VDD=VDDP=2.5~6.0V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



5.4. Power on/off sequence

5.4.1 Power on sequence PMODE[1:0]=00b

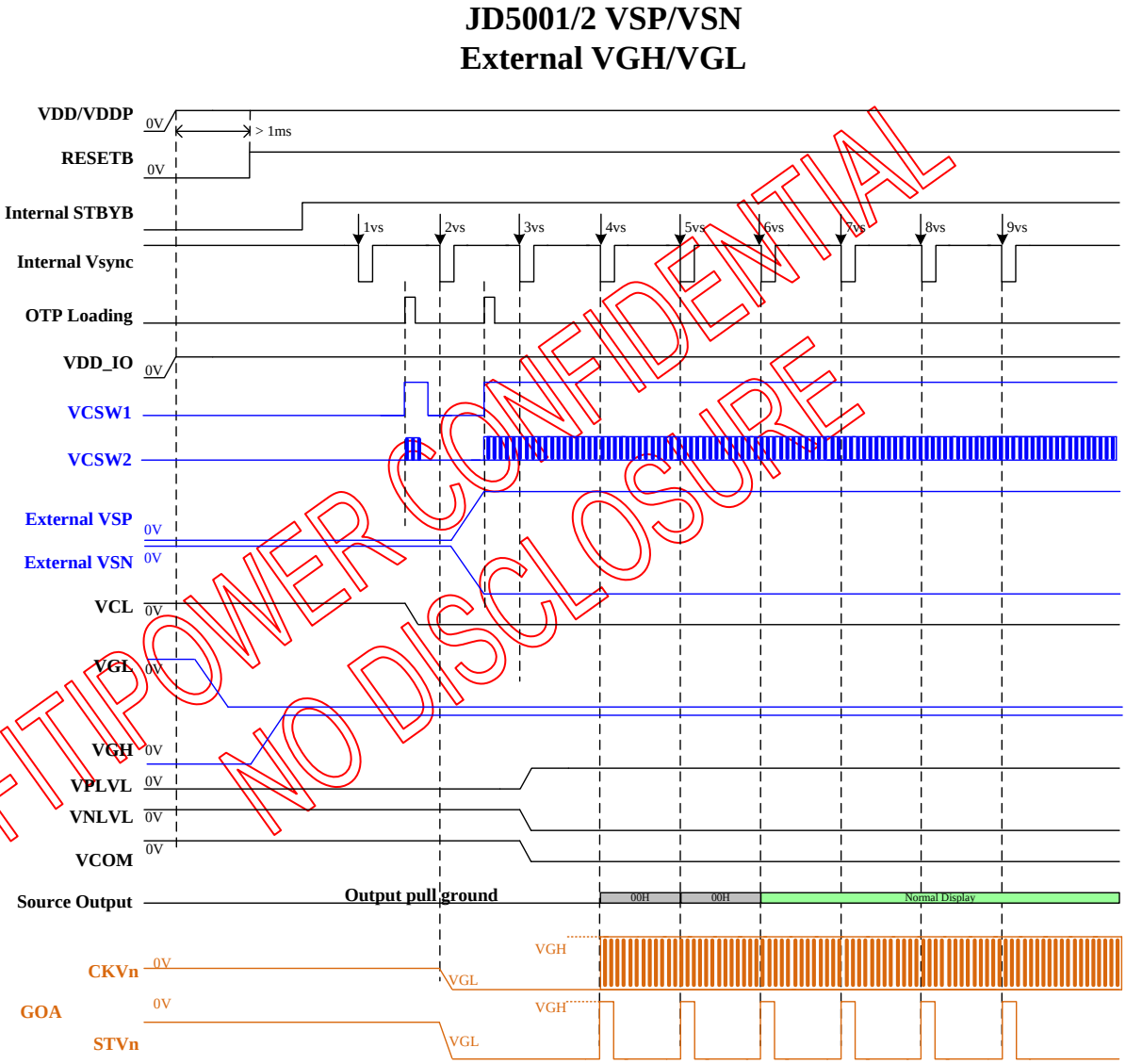


Figure 5.1: Power on sequence with PMODE[1:0]=00b

5.4.2 Power off sequence PMODE[1:0]=00b

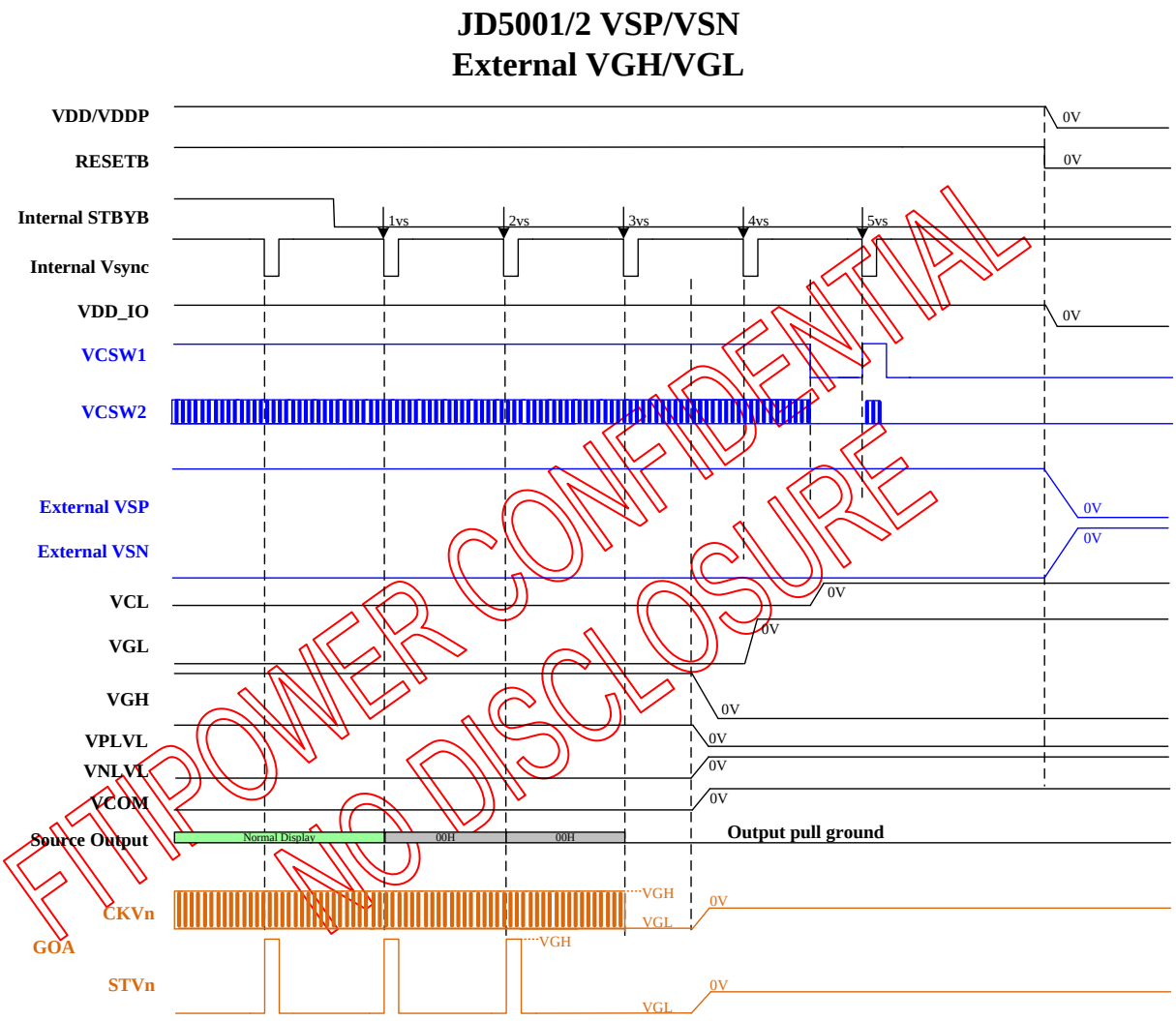


Figure 5.2: Power off sequence with PMODE[1:0]=00b

5.4.3 Power on sequence PMODE[1:0]=01b

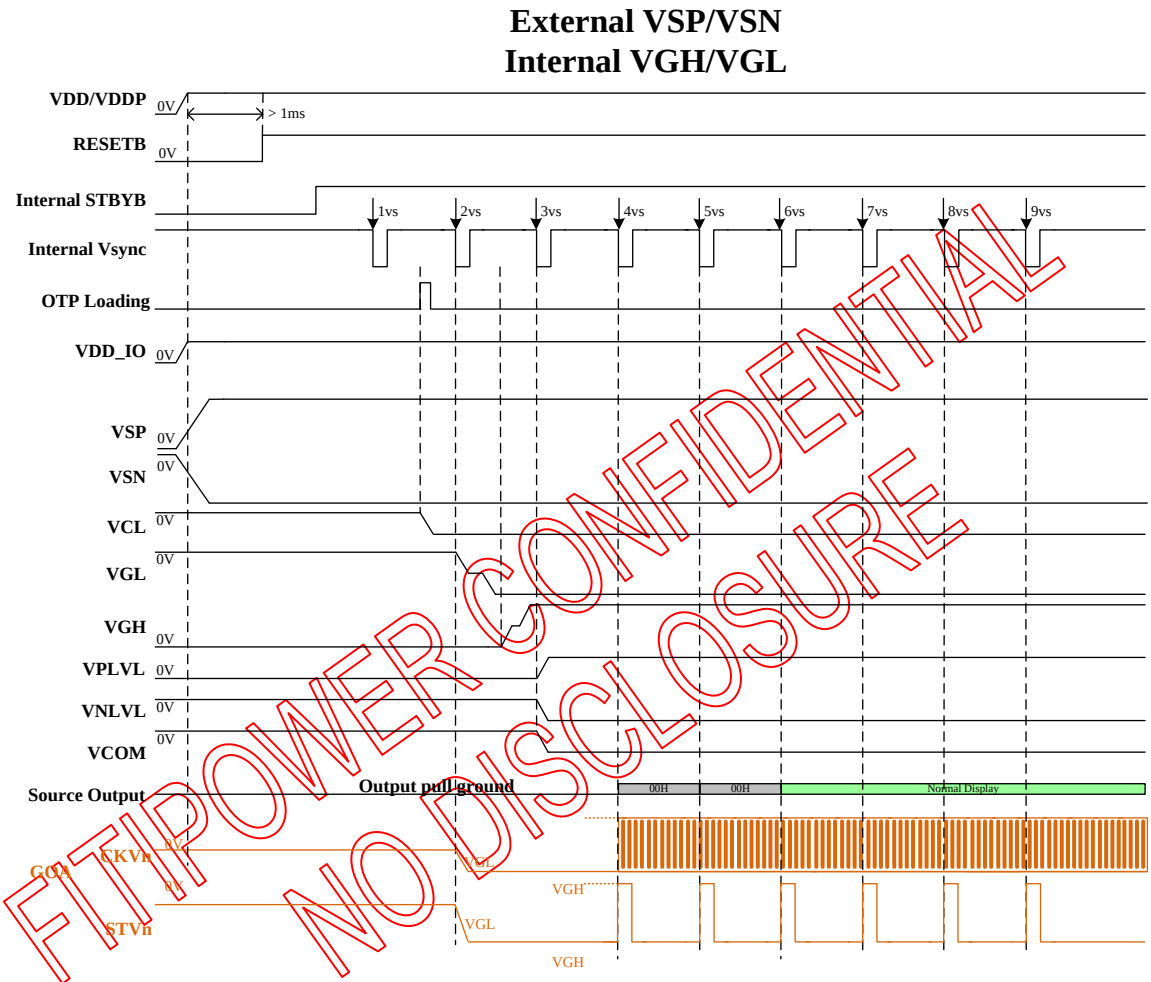


Figure 5.3: Power on sequence with PMODE[1:0]=01b

5.4.4 Power off sequence PMODE[1:0]=01b

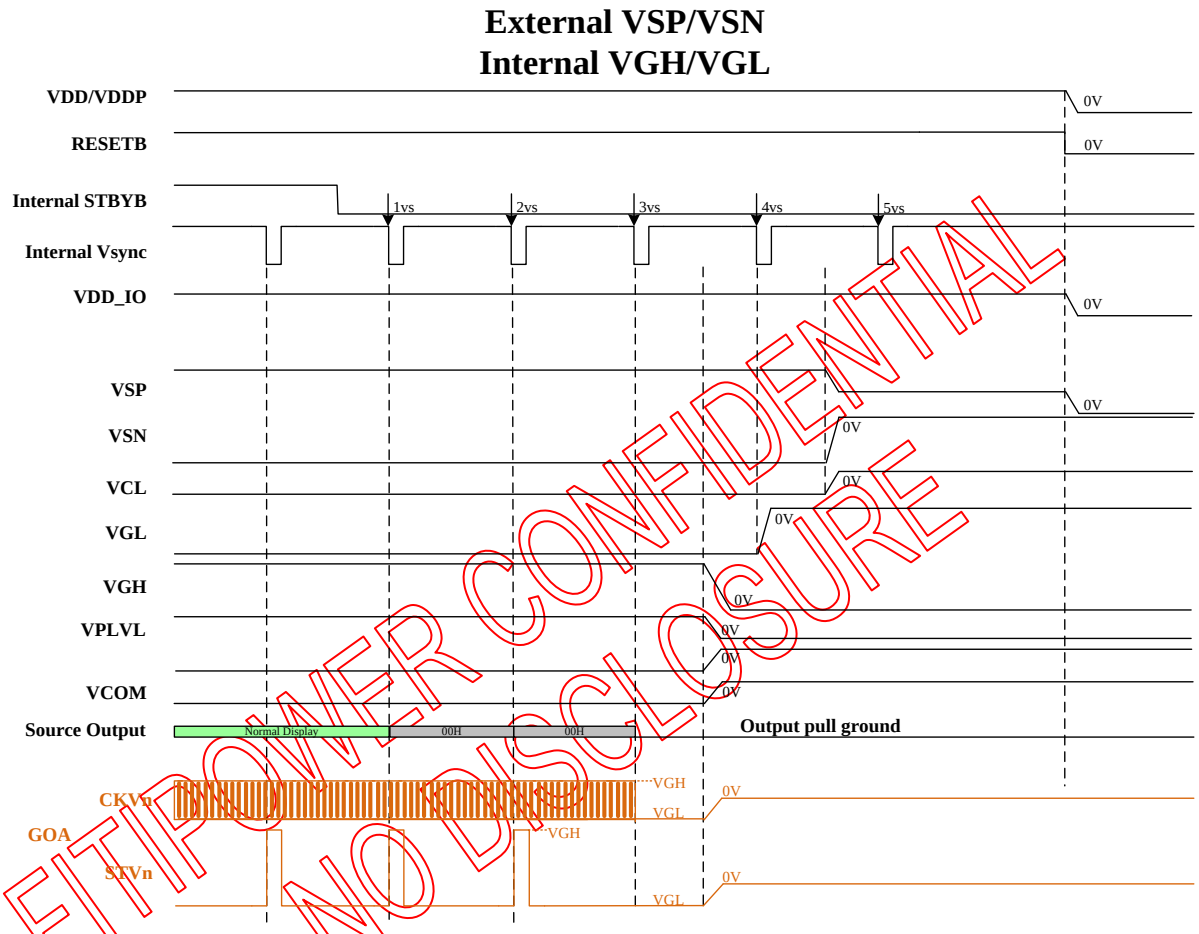


Figure 5.4: Power off sequence with PMODE[1:0]=01b

5.4.5 Power on sequence PMODE[1:0]=10b

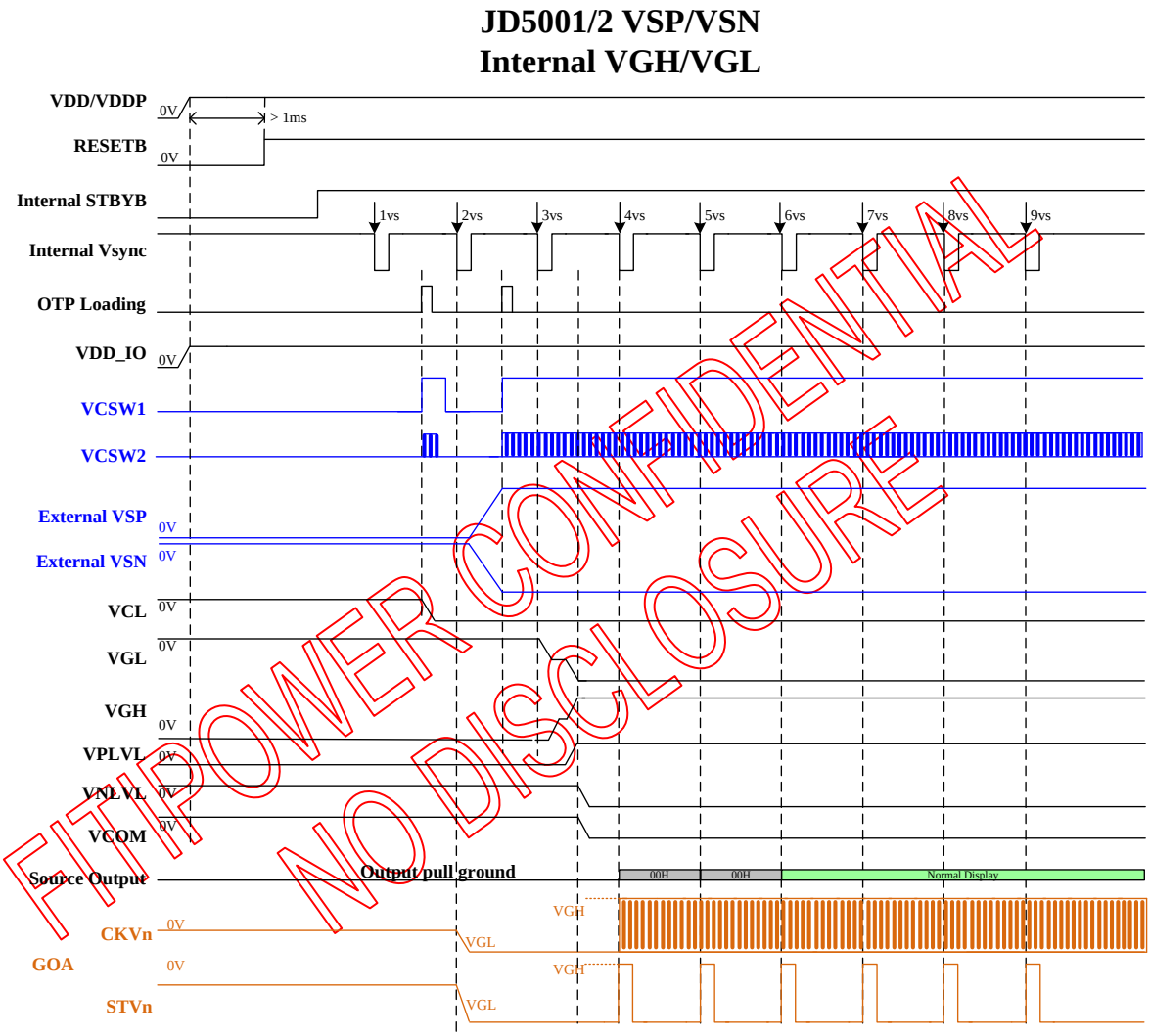


Figure 5.5: Power on sequence with PMODE[1:0]=10b

5.4.6 Power off sequence PMODE[1:0]=10b

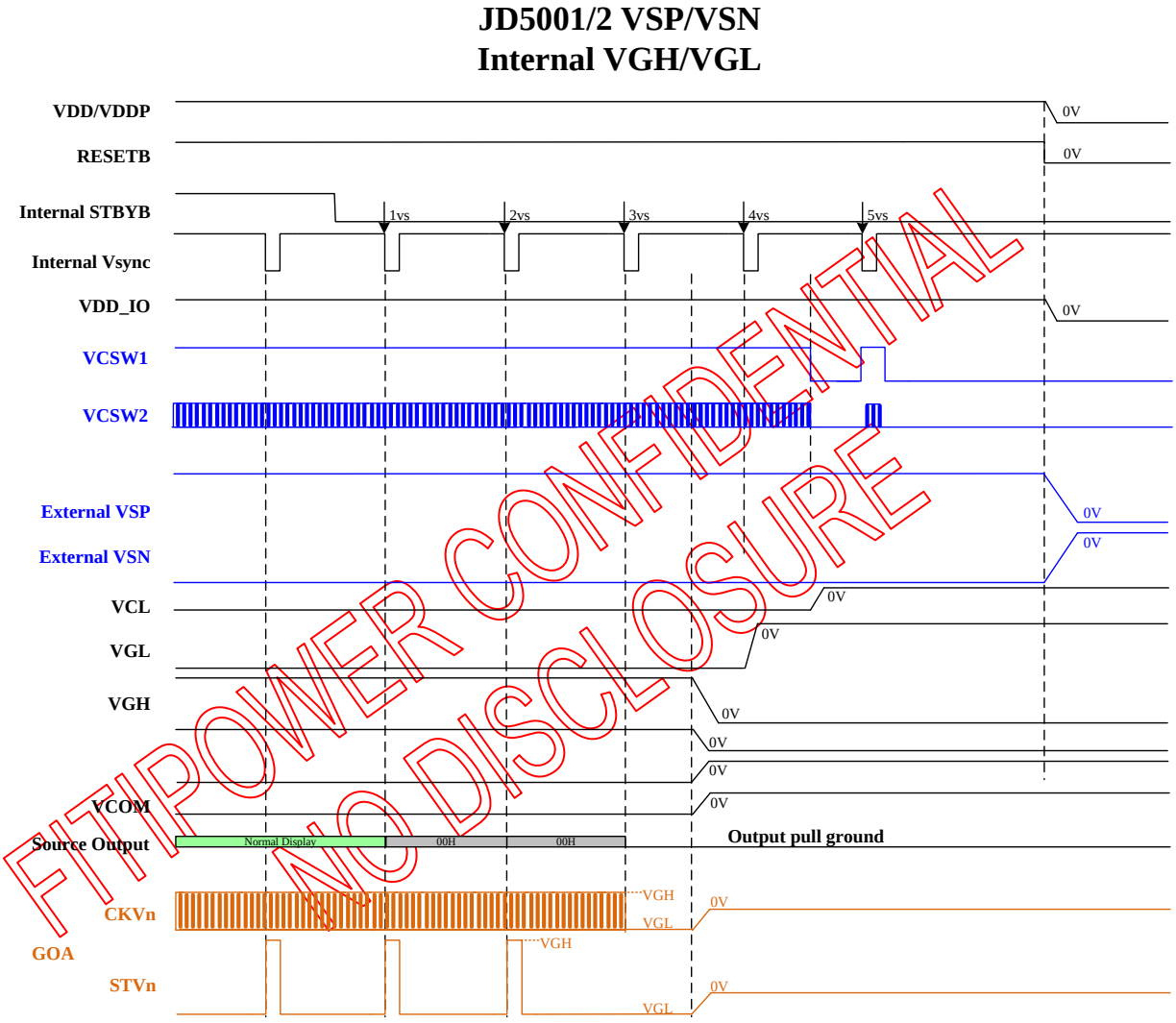


Figure 5.6: Power off sequence with PMODE[1:0]=10b

5.4.7 Power on sequence PMODE[1:0]=11b

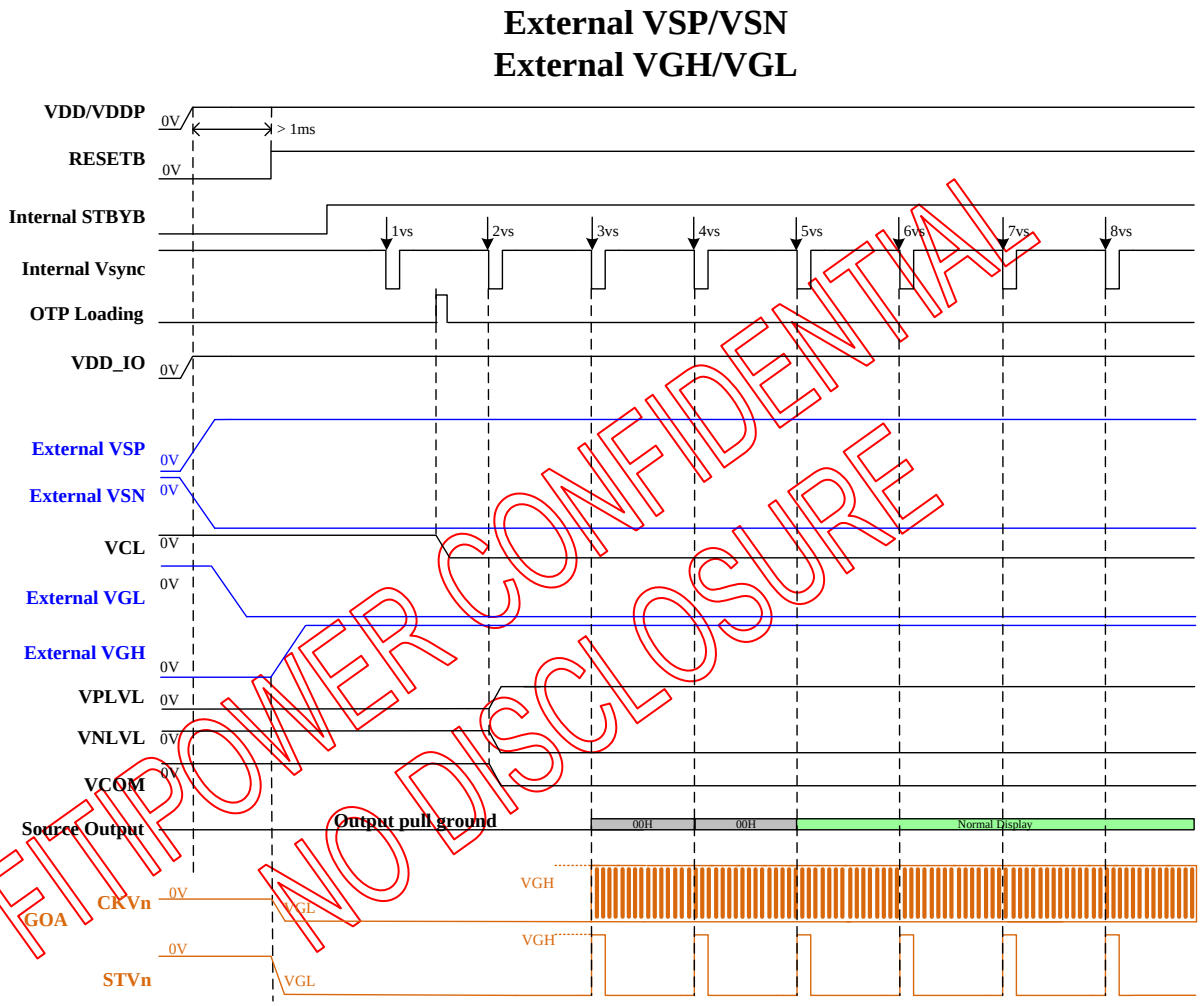


Figure 5.7: Power on sequence with PMODE[1:0]=11b

5.4.8 Power off sequence PMODE[1:0]=11b

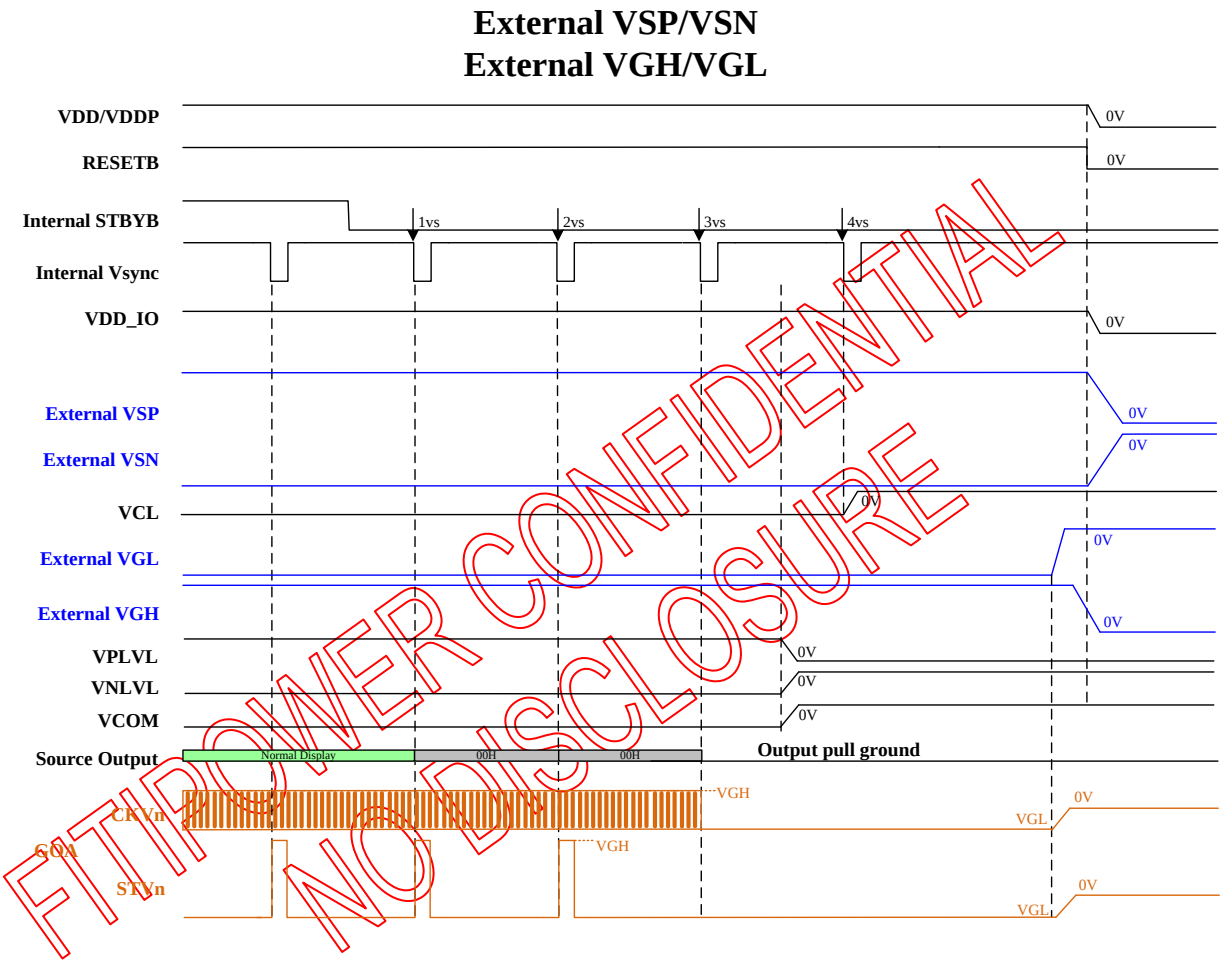


Figure 5.8: Power off sequence with PMODE[1:0]=11b

6. RECOMMEND VALUE OF WIRING RESISTANCE AND CAPACITORS

Recommended specification of wiring resistance and capacitors

Pad Name	Pin Definition	Maximum series resistance(ohm)
VDDIO,VDDIO_IF	Power supply	5
VDD,VDDP	Power supply	5
VSS,VSSA,VSS_IF,VSSP	Power supply	5
VOTP	OTP Power supply	10
RESETB,CSB,SCL,SDA,SCL_I2C,SDA_I2C	Input	100
PMODE[1:0],LANE1_STBYB,LANE0_BISTB,LNSW[1:0],RES[2:0],PNSW	Input	100
VCSW1,VCSW2,LEDPWM,LEDON,ERR_FG	Output	100
DP[0],DN[0]	Input+Output	5
DP[1],DN[1],DP[2],DN[2],DP[3],DN[3],CKP,CKN	Input	5
VCOM	Output,Capacitor connection	5
VDD_18V,VDD_18V_IF	Output,Capacitor connection	5
VSP,VSN,VCL	Output,Capacitor connection	10
VGMP,VGMN,VREF	Output,Capacitor connection	10
VGH,VGH_REG,VGL,VGL_REG	Output,Capacitor connection	10
C41P,C41N,C42P,C42N,C51P,C51N,C11P_VGL,C11N_VGL	Capacitor connection	5
GOUTL[22:1],GOUTR[22:1]	Output	50

Pad Name	Withstanding voltage (V)	CAP (uF)
VGH	25	1
VGL	25	1
VGH_REG	25	1
VGL_REG	25	1
VSP	10	1
VSN	10	1
VGMP	10	1
VGMN	10	1
VCOM	6.3	2.2
VDD/VDDP	6.3	2.2
VDDIO/VDDIO_IF	6.3	2.2
VDD_18V	6.3	1
VDD_18V_IF	6.3	1
VCL	6.3	1
VCI1	6.3	1
C41P/C41N	25	1
C42P/C42N	25	1
C51P/C51N	25	1

7. PANEL APPLICATION

The EK79030 supports the resolution of 400RGBx1280 and 480RGBx1280.

The TCON also can generate gate controller timing. These signals can support for general gate driver or GOA (Gate driver on Array).

7.1 GOA connection

The EK79030 can support GOA/GIP (Gate driver on array) function.

GOA output pin define can set by register. A multiplexer is built in GOA function that selects one of several GOA signals. GOA function showed as below. The detail GOA output signal setting please refer application note.

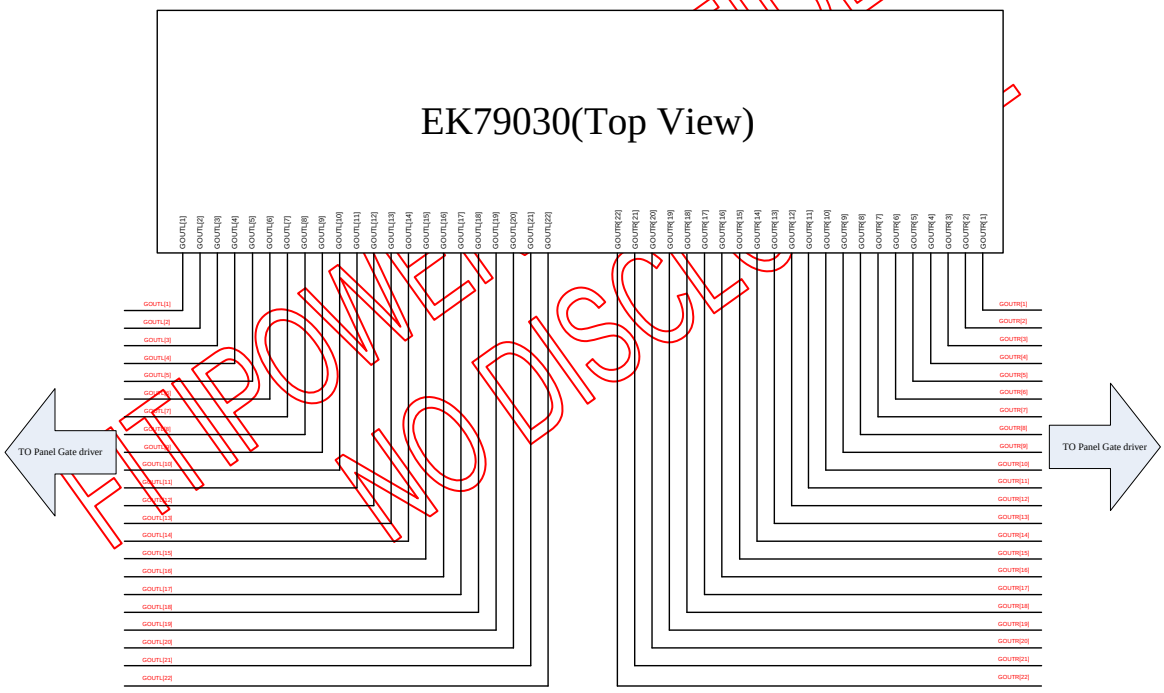


Figure 6.1 : GOA wire example

7.2 Panel Structure

7.2.1. Driving method for panel structure

EK79030 only support stripe panel type as following Figure:

7.2.1.1. Stripe driving method for panel structure

Normal driving method: ZIGZAG = 0

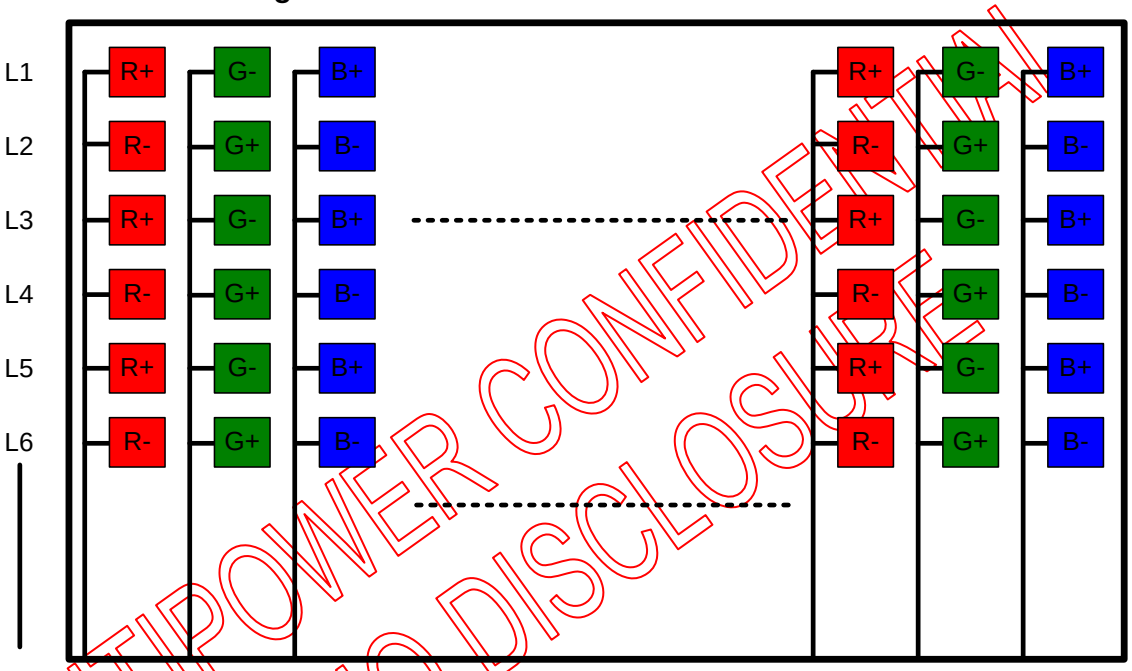
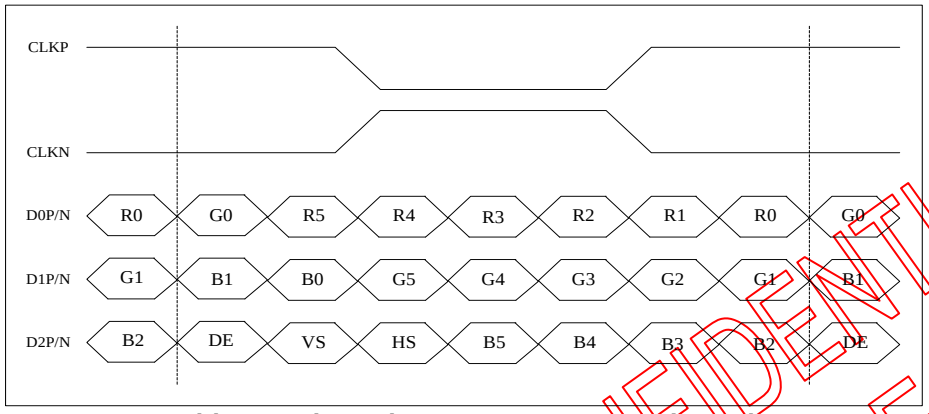


Figure 6.2 : Stripe driving method

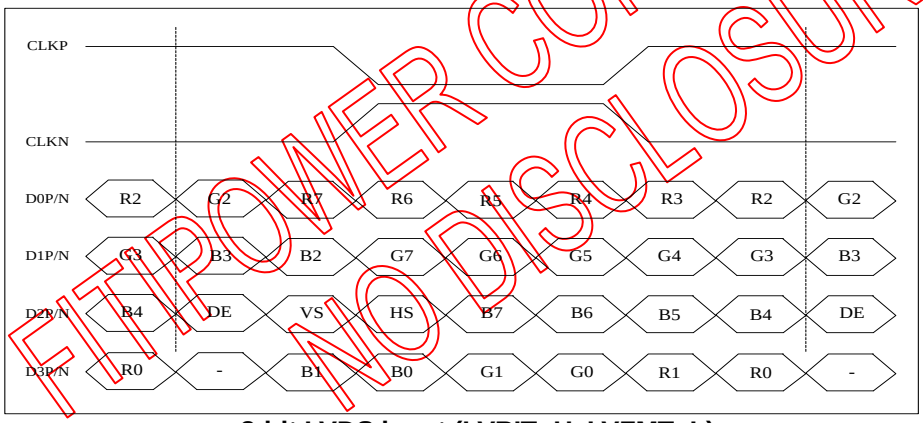
8. INTERFACE

8.1 LVDS interface

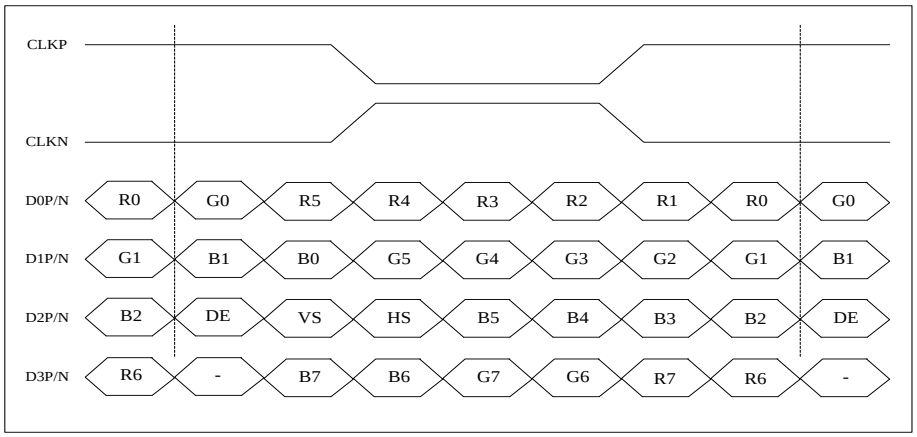
8.1.1 Data input format for LVDS



6-bit LVDS input (LVBIT=L, LVFMT=Don't care)



8-bit LVDS input (LVBIT=H, LVFMT=L)



8-bit LVDS input(LVBIT=H, LVFMT=H)

8.2 MIPI interface

8.2.1 DSI protocol

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. These terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode(saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero.

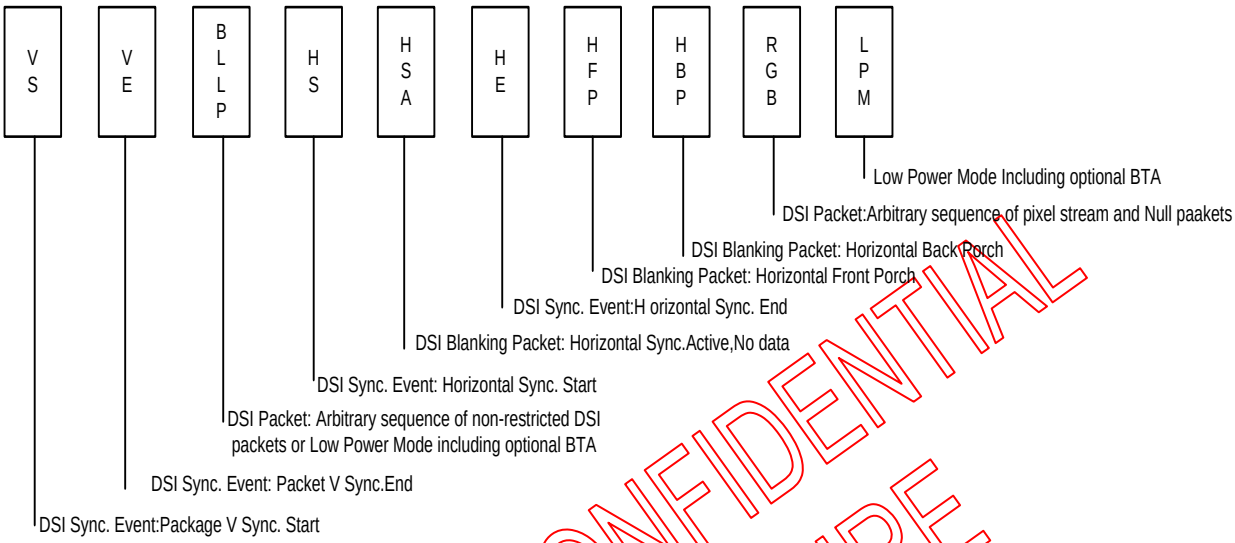
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. Individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

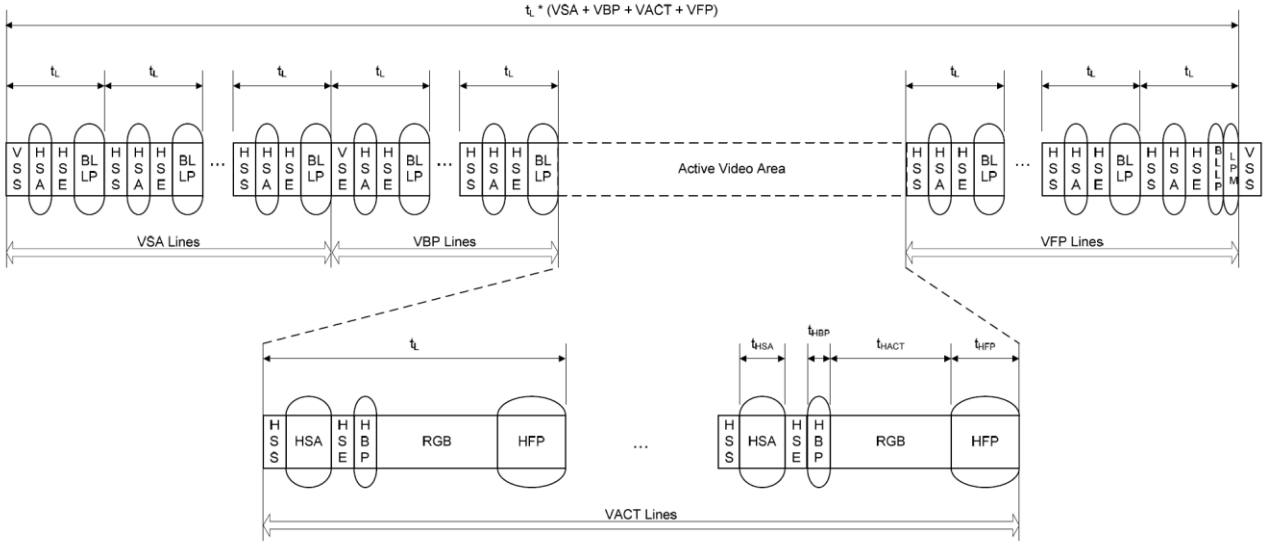
If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

Clock Requirements

A DSI host processor shall support continuous clock on the Clock Lane for display module that require it, so the host processor needs to keep the HS serial clock running.

●Non-Burst Mode with Sync Pulses

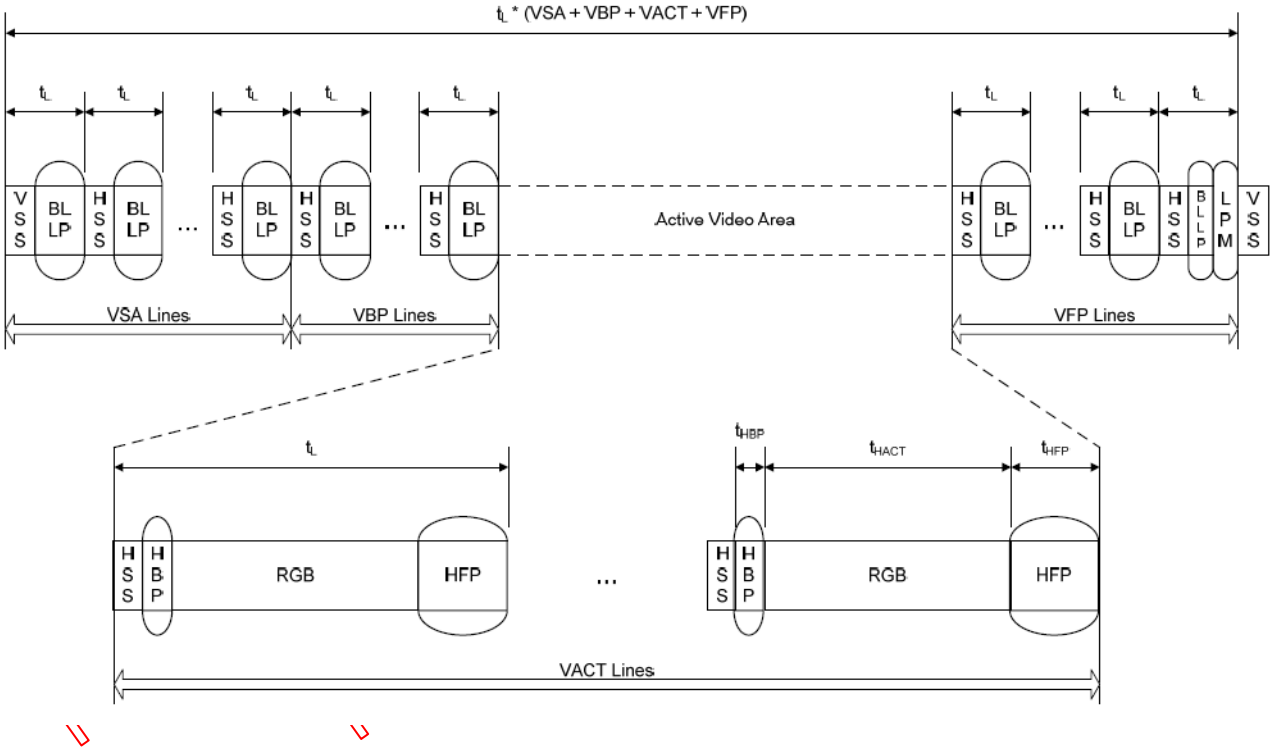
With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.



Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

●Non-Burst Mode with Sync Events

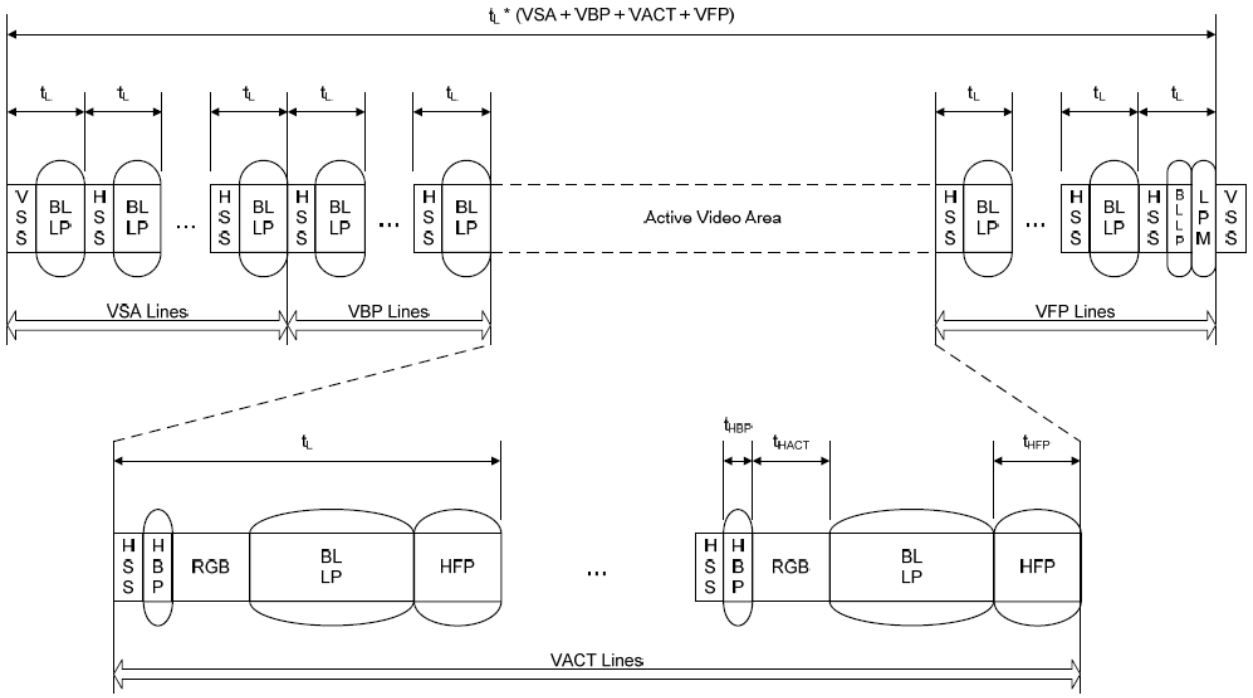
This mode is a simplification of the format described in section "Non-Burst Mode with Sync Pulse" .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.



As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

● Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.3 LVDS/MIPI Input Timing Table

For 400RGBx1280

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
MIPI (4 Lane) @Frame rate=60Hz			349		Mbps
MIPI (3 Lane) @Frame rate=60Hz			465		Mbps
DCLK frequency @Frame rate=60Hz	F_{DCLK}		58.2		MHz
HSYNC period time	T_H		744		DCLK
Horizontal display area	T_{HD}		400		DCLK
HSYNC pulse width	T_{HPW}		24	-	DCLK
HSYNC back porch	T_{HBP}		160	-	DCLK
HSYNC front porch	T_{FBP}		160	-	DCLK
VSYNC period time	T_V		1304		H
Vertical display area	T_{VD}		1280		H
VSYNC pulse width	T_{VPW}		2	-	H
VSYNC back porch	T_{VBP}		10	-	H
VSYNC front porch	T_{VFP}		12	-	H

For 480RGBx1280

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
MIPI (4 Lane) @Frame rate=60Hz			386		Mbps
MIPI (3 Lane) @Frame rate=60Hz			515		Mbps
DCLK frequency @Frame rate=60Hz	F_{DCLK}		64.4		MHz
HSYNC period time	T_H		824		DCLK
Horizontal display area	T_{HD}		480		DCLK
HSYNC pulse width	T_{HPW}		24	-	DCLK
HSYNC back porch	T_{HBP}		160	-	DCLK
HSYNC front porch	T_{FBP}		160	-	DCLK
VSYNC period time	T_V		1304		H
Vertical display area	T_{VD}		1280		H
VSYNC pulse width	T_{VPW}		2	-	H
VSYNC back porch	T_{VBP}		10	-	H
VSYNC front porch	T_{VFP}		12	-	H

MIPI Frequency = (Frame rate) x TH x TV x 24bits.

9. REGISTER TABLE

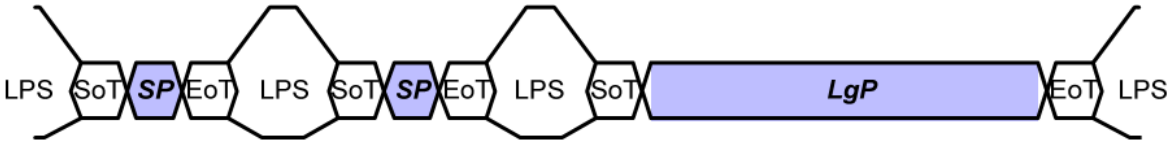
The EK79030 supports set internal register by MIPI interface, SPI interface and I2C interface. MIPI and SPI/I2C interface use different register address. The MSB bit [7] of address is only for MIPI interface. The SPI and I2C must be ignored its. “MIPI address” and “SPI/I2C address” showed in register table.

9.1 MIPI command mode control register

In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup. The diagram illustrates as multiple packets being sent separately, and as concatenated packets in a single HS transmission.

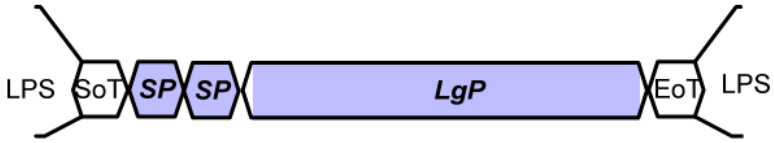
In HS Mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT between packets. This constraint does not apply to LP transmissions



Separate Transmissions

KEY:

LPS	– Low Power State	SP	– Short Packet
SoT	– Start of Transmission	LgP	– Long Packet
EoT	– End of Transmission		



Single Transmission

9.2 SPI format

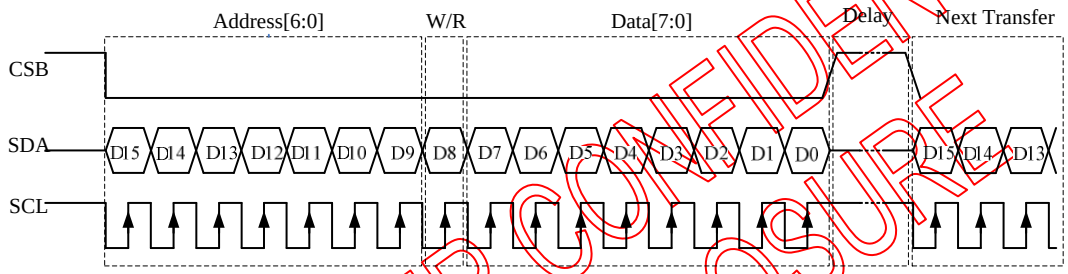
EK79030 use the 3-wire serial port as communication interface for all the function and command setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK79030 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing. Because the 3-wire only can read/write one address. So we put the “parameter index” at the address 0x2F. When 3-wire command sends, it will refer to the address 0x2F[4:0] as the parameter index value.



3-Wire Command Format:

Bit	Description
D15-D9	Register Address [6:0].
D8	W/R control bit. “0” for Write; “1” for Read
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							0	Data (Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							1	Data (Issue by 3-Wire engine)							

9.3 I2C format

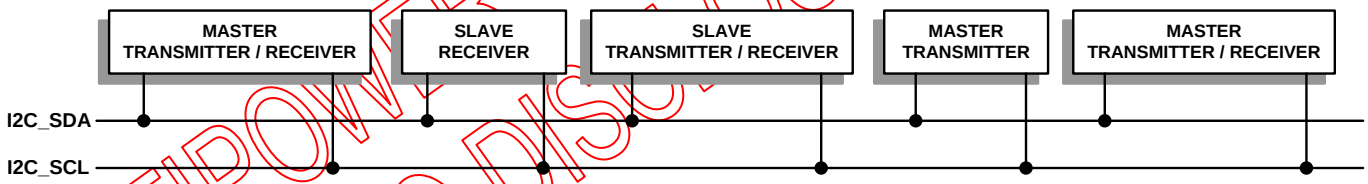
The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I²C_SDA) and the Serial Clock Line (I²C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I²C-Bus Protocol:

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

(b) Definitions:

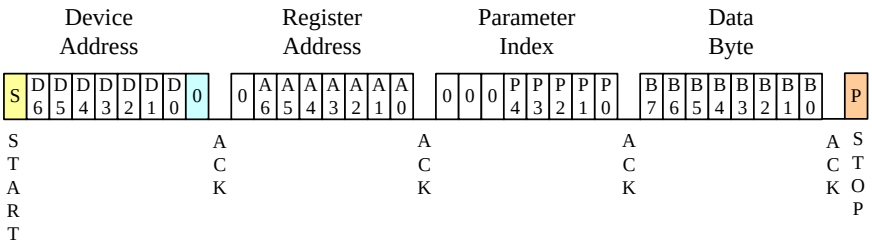
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



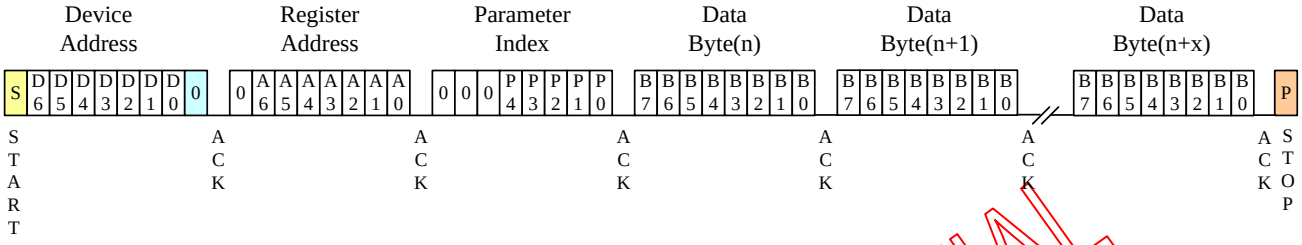
9.3.1 Register Write Sequence of I²C Interface

EK79030 supports register write sequence via I²C-bus transfer. The register writing support single register write mode and multi-register write mode. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in below.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to "0" for WRITE.
(3) The slave issues an ACK to master.
(4) 8 bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) EK79030 DA[6:0]=110_1000



Single Register Writing Timing

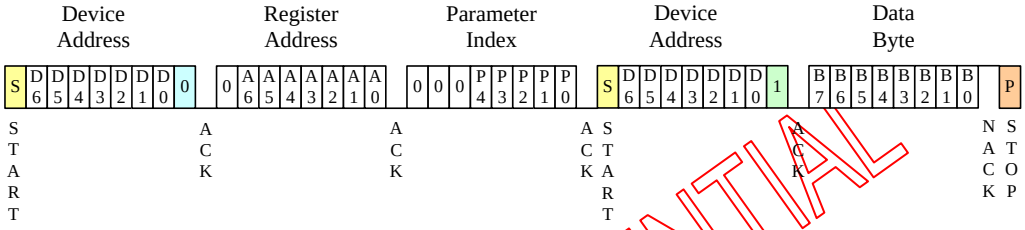


Multi Register Writing Timing

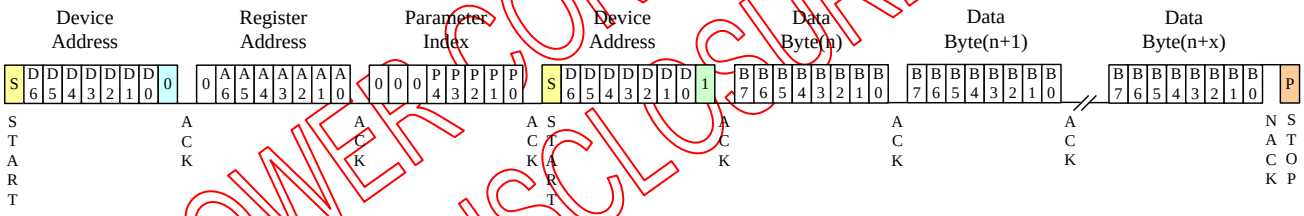
9.3.2 Register Read Sequence of I2C Interface

EK79030 supports register read sequence via I^{2}C-bus transfer. The register reading only support single register read mode.

Register data reading transfers follow the format and is shown in below.



Single Register Reading Timing



Multi Register Reading Timing

9.4 User Define Command List and Description (For MIPI command mode, SPI mode, and I2C mode)

9.4.1 User Define Command List Table

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)	Function
0xCD	1	R/W	FITI_CMD[7:0]								00	Enter FITI_CMD
0x4D	1	R/W	FITI_CMD[7:0]								00	Exit FITI_CMD
0x04	1	R	core_state[8]	-	-	-	-	-	-	-		Core_state
0x06	1	R	core_state[7:0]									
0X1B	1	R/W	-	-	-	-	-	otp_pwr_rd_key	otp_prog_reg	-	00	OTP setting
0x27	1	R/W	-	-	-	-	-	otp_lock	-	-	00	
0x28	1	R/W	-	-	-	-	-	eco_pclk_ledon_sel	-	-	11	Power enable setting
0x29	1	R/W	-	-	-	-	-	-	-	res_400	10	Panel control
0x2D	1	R/W	-	-	-	VGL_REG_SEL[4:0]					11	VGL_REG voltage
0x2E	1	R/W	-	-	-	-	PWRIC_CLK1[3:0]				0E	JD5001/2 pump clock
0x2F	1	R/W	-	-	-	parameter_index[4:0]					00	parameter_index
0x30	1	R/W	LNSW[7:4]				VRES_FIX	RES[2:0]			00	Panel control
0x31	1	R/W	VRES[7:0]								9F	
0x32	1	R/W	-	STBYB	UPDNB	SHLR	-	-	NBW	BIST	00	
0x33	1	R/W	-	-	PMODE[5:4]		ZIGZAG	Z_LEFT	Z_SCAN	Z_TYPE	21	
0x34	1	R/W	-	HFRC	DITHER	LED_EN	LEDPWPOL	LEDONPOL			FC	
0x35	1	R/W	PNSW	SWDIV	RTREM_EN	LVFMT	LVBIT	MODE	INVSEL[1:0]		24	
0x36	1	R/W	-	-	-	-	BLK_SW	GOA_MODE[2:0]			41	GOA
0x39	1	R/W	-	-	-	pwm_to_pwr_sel	-	-	-	-	11	JD5001/2 pump clk
0x3A	1	R/W	-	-	goa_sel[5:4]		dummy_sel[3:0]				00	GOA
0x3D	1	R/W	-	-	-	VCOM_SET_1	-	-	-	programmed	1F	OTP setting
0x3F	1	R/W	-	-	cmd_sel	-	-	-	-	if_sel	1A	OTP/IFSEL setting
0x41	1	R/W	VCOM_SEL[7:0]								5E	VCOM voltage
0x44	1	R/W	TRIM_VDD18[7:5]			-	-	-	-	-	A8	Logic circuit power supply

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0x47	1	R/W	-	-	-	VGH_S[4:0]					14	VGH voltage
0x48	1	R/W	-	-	-	VGL_S[4:0]					66	VGL voltage
0x4E	1	R/W	-	VNLVLH_SEL[6:0]							4F	GAML voltage
0x4F	1	R/W	-	VPLVLH_SEL[6:0]							50	GAMH voltage
0x53	1	R/W	-	-	-	GP_00[4:0]					1F	Gamma positive voltage
	2	R/W	-	-	-	GP_01[4:0]					1B	
	3	R/W	-	-	-	GP_02[4:0]					19	
	4	R/W	-	-	-	GP_03[4:0]					15	
	5	R/W	-	-	-	GP_04[4:0]					15	
	6	R/W	-	-	-	GP_05[4:0]					15	
	7	R/W	-	-	-	GP_06[4:0]					17	
	8	R/W	-	-	-	GP_07[4:0]					19	
	9	R/W	-	-	-	GP_08[4:0]					19	
	10	R/W	-	-	-	GP_09[4:0]					14	
	11	R/W	-	-	-	GP_10[4:0]					11	
	12	R/W	-	-	-	GP_11[4:0]					0F	
	13	R/W	-	-	-	GP_12[4:0]					0F	
	14	R/W	-	-	-	GP_13[4:0]					0F	
	15	R/W	-	-	-	GP_14[4:0]					0C	
	16	R/W	-	-	-	GP_15[4:0]					0A	
	17	R/W	-	-	-	GP_16[4:0]					07	
	18	R/W	-	-	-	GP_17[4:0]					03	
	19	R/W	-	-	-	GP_18[4:0]					01	
0x54	1	R/W	-	-	-	GN_00[4:0]					1F	Gamma negative voltage
	2	R/W	-	-	-	GN_01[4:0]					1A	

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0x54	3	R/W	-	-	-	GN_02[4:0]					18	Gamma negative voltage
	4	R/W	-	-	-	GN_03[4:0]					14	
	5	R/W	-	-	-	GN_04[4:0]					14	
	6	R/W	-	-	-	GN_05[4:0]					14	
	7	R/W	-	-	-	GN_06[4:0]					16	
	8	R/W	-	-	-	GN_07[4:0]					18	
	9	R/W	-	-	-	GN_08[4:0]					19	
	10	R/W	-	-	-	GN_09[4:0]					15	
	11	R/W	-	-	-	GN_10[4:0]					12	
	12	R/W	-	-	-	GN_11[4:0]					0F	
	13	R/W	-	-	-	GN_12[4:0]					0E	
	14	R/W	-	-	-	GN_13[4:0]					0E	
	15	R/W	-	-	-	GN_14[4:0]					0B	
	16	R/W	-	-	-	GN_15[4:0]					09	
	17	R/W	-	-	-	GN_16[4:0]					06	
	18	R/W	-	-	-	GN_17[4:0]					03	
	19	R/W	-	-	-	GN_18[4:0]					01	
0x55	1	R/W	-	-	gstv1_rise[5:0]						00	GOA STV
	2	R/W	-	-	gstv1_fall[5:0]						0F	
	3	R/W	-	-	gstv2_rise[5:0]						00	
	4	R/W	-	-	gstv2_fall[5:0]						0F	
	5	R/W	-	-	gstv3_rise[5:0]						00	
	6	R/W	-	-	gstv3_fall[5:0]						0F	
	7	R/W	-	-	gstv4_rise[5:0]						00	
	8	R/W	-	-	gstv4_fall[5:0]						0F	

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0x56	1	R/W	-	-	gckv1_rise[5:0]						00	GOA CLK
	2	R/W	-	-	gckv1_fall[5:0]						0F	
	3	R/W	-	-	gckv2_rise[5:0]						00	
	4	R/W	-	-	gckv2_fall[5:0]						0F	
	5	R/W	-	-	gckv3_rise[5:0]						00	
	6	R/W	-	-	gckv3_fall[5:0]						0F	
	7	R/W	-	-	gckv4_rise[5:0]						00	
	8	R/W	-	-	gckv4_fall[5:0]						0F	
	9	R/W	-	-	gckv5_rise[5:0]						00	
	10	R/W	-	-	gckv5_fall[5:0]						0F	
	11	R/W	-	-	gckv6_rise[5:0]						00	
	12	R/W	-	-	gckv6_fall[5:0]						0F	
	13	R/W	-	-	gckv7_rise[5:0]						00	
	14	R/W	-	-	gckv7_fall[5:0]						0F	
	15	R/W	-	-	gckv8_rise[5:0]						00	
	16	R/W	-	-	gckv8_fall[5:0]						0F	
0x57	1	R/W	-	-	grst1_rise[5:0]						00	GOA RESET
	2	R/W	-	-	grst1_fall[5:0]						16	
	3	R/W	-	-	grst2_rise[5:0]						00	
	4	R/W	-	-	grst2_fall[5:0]						16	
	5	R/W	-	-	grst3_rise[5:0]						00	
	6	R/W	-	-	grst3_fall[5:0]						16	
	7	R/W	-	-	grst4_rise[5:0]						00	
	8	R/W	-	-	grst4_fall[5:0]						16	
0x58	1	R/W	GFLC[7:0]								08	flc toggle frequency select

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0X5E	1	R/W	-	nchg_cs_en	-	-	-	-	-	-	03	Source EQ
0X60	1	R/W	TRIM_VDD18F[7:5]			-	-	-	-	-	B0	Receiver circuit power supply
0x63	1	R/W	-	lan_sel[6:5]		-	-	-	-	-	06	MIPI lane number selection
0x65	1	R/W	-	-	-	-	goa_updn	-	-	-	08	GOA
0X67	1	R/W	phase[7:4]				ckv_width[3:0]				82	
0X68	1	R/W	ckv_blksw_revl[7:4]				flc_trans_stvsp_dis[3:0]				16	
0X69	1	R/W	stv_width[7:4]				flc_stag_trans_stvsp_dis[3:0]				27	
0X6A	1	R/W	ckv_blkpulse_stv_rise_dis[7:4]				ckv_blkpulse_stv_fall_dis[3:0]				C3	
0x6B	1	R/W	eq_fall				eq_rise				00	GOA clock EQ
0X6C	1	R/W	dummy_en	flc_stag_en	ckv_blkpulse_stagger_sel[5:4]		ckv_blkpulse_phase_sel	ckv_blkpulse_en	ckv_blksw_logic	stv_ckv_select	08	GOA
0X6D	1	R/W	-	-	-	sft_goe_scale	-	sft_goe_drct[2:1]		stv_ckv_sft	01	
0x73	1	R/W	-	-	hv_learn	de_edge_sel	-	-	-	-	30	Panel control
0x74	1	R/W	-	-	-	mipi_gip_hss_sel	-	-	-	-	10	
0x77	1	R/W	-	-	-	-	CLK_SEL_VGL[3:2]		-	-	00	VGL pump clock
0X78	1	R/W	-	-	-	VGH_REG_SEL[4:0]					47	VGH_REG voltage
0X7B	1	R/W	-	-	-	-	-	-	-	GRB	01	Global reset bit
0XFA	1	R	VENDER_id[7:0]								29	Vender ID

MIPI Address : 0xCD

Address	Bit							
0xCD	D7	D6	D5	D4	D3	D2	D1	D0
Name	FITI_CMD							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	FITI_CMD	CD=”AA” → Enter fiti command.

MIPI Address : 0x4D

Address	Bit							
0xCD	D7	D6	D5	D4	D3	D2	D1	D0
Name	FITI_CMD							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	FITI_CMD	4D=”00” → Exit fiti command.

MIPI Address : 0x04

Address	Bit							
0x04	D7	D6	D5	D4	D3	D2	D1	D0
Name	core_state[8]	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7	core_state[8]	Core state description: 04=”80” → Standby status.

MIPI Address : 0x06

Address	Bit							
0x06	D7	D6	D5	D4	D3	D2	D1	D0
Name	core_state[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	core_state[8]	Core state description: **core_state[8:0]** — **status** **[0,0,0,0,0,0,0,0,1]** — **Idle** **[0,0,0,0,0,0,1,0,0]** — **FreeRun** **[0,0,0,0,1,0,0,0,0]** — **MIPI vedio mode** **[0,1,0,0,0,0,0,0,0]** — **BIST**

MIPI Address : 0x1B

Address	Bit							
0x1B	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-			otp_pwr_rdy	otp_prog_reg	-
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
1	otp_prog_reg	1B=”02” → OTP function enable. 1B=”00” → OTP function disable.
2	otp_pwr_rdy	1B=”06” → Enable OTP power, and blow the e-fuse. 1B=”00” → Disable OTP power.

MIPI Address : 0x27

Address	Bit							
0x27	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	otp_lock	-	-
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
1	otp_lock	27=”04” → Unlock OTP register. 27=”00” → Lock OTP register.

MIPI Address : 0x28

Address	Bit							
0x28	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	eco_pclk_ledon_sel	-	-
Default	0	0	0	1	0	0	0	1

Bit	Name	Description
2	eco_pclk_ledon_sel	28=”31” → LEDON pin output power enable signal. 28=”35” → LEDON pin output JD5001 pump clock signal.

MIPI Address : 0x29

Address	Bit							
0x29	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	res_400
Default	0	0	0	1	0	0	0	0

Bit	Name	Description
0	res_400	29=”01” → Only for 400RGBx1280 resolution. 29=”00” → Other resolution.

MIPI Address : 0x2D

Address	Bit							
0x2D	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VGL_REG_SEL				
Default	0	0	0	1	0	0	0	1

Bit	Name	Description
4:0	VGL_REG_SEL	VGL_REG voltage selection. | VGL_REG|=|VGL|-1.

[0,0,0,0,0]	-6.000V
[0,0,0,0,1]	-6.283V
[0,0,0,1,0]	-6.579V
[0,0,0,1,1]	-6.875V
[0,0,1,0,0]	-7.178V
[0,0,1,0,1]	-7.470V
[0,0,1,1,0]	-7.760V
[0,0,1,1,1]	-8.075V
[0,1,0,0,0]	-8.347V
[0,1,0,0,1]	-8.637V
[0,1,0,1,0]	-8.947V
[0,1,0,1,1]	-9.23V
[0,1,1,0,0]	-9.55V
[0,1,1,0,1]	-9.83V
[0,1,1,1,0]	-10.13V
[0,1,1,1,1]	-10.40V
[1,0,0,0,0]	-10.74V
[1,0,0,0,1]	-11.04V
[1,0,0,1,0]	-11.29V
[1,0,0,1,1]	-11.62V
[1,0,1,0,0]	-11.90V
[1,0,1,0,1]	-12.19V
[1,0,1,1,0]	-12.52V
[1,0,1,1,1]	-12.92V
[1,1,0,0,0]	-13.18V
[1,1,0,0,1]	-13.44V
[1,1,0,1,0]	-13.44V
[1,1,0,1,1]	-13.44V
[1,1,1,0,0]	-13.44V
[1,1,1,0,1]	-13.44V
[1,1,1,1,0]	-13.44V
[1,1,1,1,1]	-13.44V

MIPI Address : 0x2E

Address	Bit							
0x2D	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	PWRIC_CLK1			
Default	0	0	0	0	1	1	1	0

Bit	Name	Description
3:0	PWRIC_CLK1	JD5001/2 pump clock [0,0,0,0] 2.79 MHz [0,0,0,1] 2.79 MHz [0,0,1,0] 1.24 MHz [0,0,1,1] 864.83 kHz [0,1,0,0] 621.18 kHz [0,1,0,1] 508.01 kHz [0,1,1,0] 414.73 kHz [0,1,1,1] 360.87 kHz [1,0,0,0] 310.69 kHz [1,0,0,1] 279.51 kHz [1,0,1,0] 248.30 kHz [1,0,1,1] 228.26 kHz [1,1,0,0] 206.90 kHz [1,1,0,1] 192.86 kHz [1,1,1,0] 177.40 kHz [1,1,1,1] 166.76 kHz

MIPI Address : 0x2F

Address	Bit							
0x2F	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	parameter_index				
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
2	parameter_index	TCON will read/write the particular parameter according to this data.

MIPI Address : 0x30

Address	Bit							
0X30	D7	D6	D5	D4	D3	D2	D1	D0
Name	LNSW				VRES_FIX	RES		
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
2:0	RES	Display resolution selection. It do XOR operation with Pin setting.
3	VRES_FIX	Display vertical Line decided by 1:VRES[7:0] 0:RES[2:0]
7:4	LNSW	MIPI lane swap. (to pin RES do XOR operation) It do XOR operation with Pin setting. LVDS lane swap. (to pin RES do XOR operation) It do XOR operation with Pin setting.

MIPI Address : 0x31

Address	Bit							
0xB1	D7	D6	D5	D4	D3	D2	D1	D0
Name	VRES							
Default	1	0	0	1	1	1	1	1

Bit	Name	Description
7:0	VRES	Vertical Resolution selection=(VRES+1)*8, range=0~255.

MIPI Address : 0x32

Address	Bit							
0x32	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	STBYB	UPDNB	SHLR	-	-	NBW	BIST
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
0	BIST	Normal Operaton / Bist pattern selection. It do XOR operation with Pin setting. (Only LVDS)
1	NBW	Normally black or normally white setting.
4	SHLR	Source Right/Left sequence control.
5	UPDNB	Gate up or Down scan control.
6	STBYB	STBYB mode selection. Timing control, Driver and DC-DC converter are off. It do XOR operation with Pin setting. (Only LVDS)

MIPI Address : 0X33

Address	Bit							
0XB3	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	PWRMD		ZIGZAG	Z_LEFT	Z_SCAN	Z_TYPE
Default	0	0	1	0	0	0	0	1

Bit	Name	Description
0	Z_TYPE	Zig-Zag driving method selection.
1	Z_SCAN	Zig-Zag panel, Source Right/Left selection.
2	Z_LEFT	Zig-Zag panel layout type selection.
3	ZIGZAG	Panel type selection.
5:4	PWRMD	Power mode selection. It do XOR operation with Pin setting.

MIPI Address : 0X34

Address	Bit							
0xB4	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	HFRC	DITHER	LED_EN	LEDPWPOL	LEDONPOL	-	-
Default	1	1	1	1	1	1	0	0

Bit	Name	Description
2	LEDONPOL	Set the enable active polarity for external LED driver control.
3	LEDPWPOL	Set the PWM active polarity for external LED driver control.
4	LED_EN	The output of LEDON / LEDPWM signal on/off control. LED_EN = 0, Disable LEDON / LEDPWM signal. LED_EN = 1, Enable LEDON / LEDPWM signal.
5	DITHER	Dithering function enable control. Dither = 0, Dither disable. Dither = 1, Dither enable.
6	HFRC	H-FRC selection. HFRC = 0, FRC enable. HFRC = 1, H-FRC enable. If DITHER = “1” and HFRC = “0”, only FRC dithering function is enabled. If DITHER = “0”, disable dithering function, H-FRC and FRC are both disabled.

MIPI Address : 0X35

Address	Bit							
0xB5	D7	D6	D5	D4	D3	D2	D1	D0
Name	PNSW	SWDIV	RTERM_EN	LVFMT	LVBIT	MODE	INVSEL	
Default	0	0	1	0	0	1	0	0

Bit	Name	Description
1:0	INVSEL	Inversion method selection. INVSEL[1:0] = “00”, 1 line inversion. INVSEL[1:0] = “01”, 2 line one dot inversion. INVSEL[1:0] = “10”, 4 line one dot inversion. INVSEL[1:0] = “11”, Column inversion.
2	MODE	DE / HV mode select for LVDS mode. MODE = 0, HV mode. MODE = 1, DE mode.
3	LVBIT	6-bit / 8-bit input select for LVDS mode. It do XOR operation with Pin setting.
4	LVFMT	8-bit input format select for LVDS mode. It do XOR operation with Pin setting.
5	RTREM_EN	Terminal resistor disenable/enable selection. (only for LVDS)
7	PNSW	MIPI Lane polarity swap. It do XOR operation with Pin setting.

MIPI Address : 0X36

Address	Bit							
0x36	D7	D6	D5	D4	D3	D2	D1	D0
Name				-	BLK_SW	GOA_MODE		
Default	0	1	0	0	0	0	0	1

Bit	Name	Description
3	BLK_SW	ckv switch at blanking 0 : ckv stops at blanking 1 : ckv keeps toggling at blanking
2:0	GOA_MODE	differenct goa timing defined by vendor

MIPI Address : 0X39

Address	Bit							
0x39	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	pwm_to_pwr_sel	-	-	-	-
Default	0	0	0	1	0	0	0	1

Bit	Name	Description
4	pwm_to_pwr_sel	JD5001/2 pump clock 0 : LEDPWM output 1 : VCSW2 output

MIPI Address : 0X3A

Address	Bit							
0x3A	D7	D6	D5	D4	D3	D2	D1	D0
Name			goa_sel		dummy_sel			
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
5:4	goa_sel	goa vendor select
3:0	dummy_sel	ckv pre-dummy select dummy_sel[0000] :all dummy_sel[0001] :1 clk dummy_sel[0010] :2 clk … dummy_sel[0010] :15 clk

MIPI Address : 0X3D

Address	Bit							
0XB3	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-		VCOM_SET_1	-	-	-	programmed
Default	0	0	0	1	1	1	1	1

Bit	Name	Description
0	programmed	programmed=1, OTP Vender_id password.
4	VCOM_SET_1	VCOM_SET_1=1, OTP VCOM password.

MIPI Address : 0X3F

Address	Bit							
0XB3	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	cmd_sel	-	-	-	-	if_sel
Default	0	0	0	1	1	0	1	0

Bit	Name	Description
0	if_sel	MIPI/LVDS I/F selection. It do XOR operation with Pin setting. if_sel = 1, MIPI I/F. if_sel = 0, LVDS I/F.
5	cmd_sel	3-wire/I2C selection. It do XOR operation with Pin setting. cmd_sel = 0, 3-wire. cmd_sel = 1, I2C.

MIPI Address : 0X41

Address	Bit							
0x44	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOM_SEL[7:0]							
Default	0	1	0	1	1	1	1	0

Bit	Name	Description
7:0	VCOM_SEL	The register is defines vender id for customer.

[0,0,0,0,0,0,0,0]	**-0.205V**
[0,0,0,0,0,0,0,1]	**-0.217V**
[0,0,0,0,0,0,1,0]	**-0.230V**
[0,0,0,0,0,0,1,1]	**-0.243V**
[0,0,0,0,0,1,0,0]	**-0.256V**
:	**-13mv/step**
[0,1,0,1,1,1,0,0]	**-1.400V**
[0,1,0,1,1,1,0,1]	**-1.413V**
[0,1,0,1,1,1,1,0]	**-1.426V**
[0,1,0,1,1,1,1,1]	**-1.439V**
:	**-13mv/step**
[1,1,1,1,1,1,1,0]	**-3.492V**
[1,1,1,1,1,1,1,1]	**-3.505V**

MIPI Address : 0X44

Address	Bit							
0x44	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRIM_VDD18[7:5]			-	-	-	-	-
Default	1	0	1	0	1	0	0	0

Bit	Name	Description
7:5	TRIM_VDD18	Internal power supply for logic circuits.

[0,0,0]	**1.768V**
[0,0,1]	**1.693V**
[0,1,0]	**1.615V**
[0,1,1]	**1.536V**
[1,0,0]	**1.842V**
[1,0,1]	**1.917V**
[1,1,0]	**1.989V**
[1,1,1]	**2.062V**

MIPI Address : 0x47

Address	Bit							
0x47	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VGH_S[4:0]				
Default	0	0	0	1	0	1	0	0

Bit	Name	Description
4:0	VGH_S	VGH voltage selection.

[0,0,0,0,0]	**7.559V**
[0,0,0,0,1]	**8.061V**
[0,0,0,1,0]	**8.657V**
[0,0,0,1,1]	**9.054V**
[0,0,1,0,0]	**9.350V**
[0,0,1,0,1]	**9.647V**
[0,0,1,1,0]	**9.946V**
[0,0,1,1,1]	**10.241V**
[0,1,0,0,0]	**10.837V**
[0,1,0,0,1]	**11.43V**
[0,1,0,1,0]	**12.02V**
[0,1,0,1,1]	**12.62V**
[0,1,1,0,0]	**12.91V**
[0,1,1,0,1]	**13.21V**
[0,1,1,1,0]	**13.50V**
[0,1,1,1,1]	**13.79V**
[1,0,0,0,0]	**14.09V**
[1,0,0,0,1]	**14.26V**
[1,0,0,1,0]	**14.26V**
[1,0,0,1,1]	**14.26V**
[1,0,1,0,0]	**14.26V**
[1,0,1,0,1]	**14.26V**
[1,0,1,1,0]	**14.26V**
[1,0,1,1,1]	**14.26V**
[1,1,0,0,0]	**14.26V**
[1,1,0,0,1]	**14.26V**
[1,1,0,1,0]	**14.26V**
[1,1,0,1,1]	**14.26V**
[1,1,1,0,0]	**14.26V**
[1,1,1,0,1]	**14.26V**
[1,1,1,1,0]	**14.26V**
[1,1,1,1,1]	**14.26V**

MIPI Address : 0x48

Address	Bit							
0x48	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VGL_S[4:0]				
Default	0	1	1	0	0	1	1	0

Bit	Name	Description
4:0	VGL_S	VGL voltage selection.

[0,0,0,0,0]	**-9.28V**
[0,0,0,0,1]	**-9.61V**
[0,0,0,1,0]	**-9.94V**
[0,0,0,1,1]	**-10.26V**
[0,0,1,0,0]	**-10.59V**
[0,0,1,0,1]	**-10.92V**
[0,0,1,1,0]	**-11.24V**
[0,0,1,1,1]	**-11.57V**
[0,1,0,0,0]	**-11.89V**
[0,1,0,0,1]	**-12.22V**
[0,1,0,1,0]	**-12.54V**
[0,1,0,1,1]	**-12.87V**
[0,1,1,0,0]	**-13.20V**
[0,1,1,0,1]	**-13.52V**
[0,1,1,1,0]	**-13.83V**
[0,1,1,1,1]	**-14.00V**
[1,0,0,0,0]	**-14.00V**
[1,0,0,0,1]	**-14.00V**
[1,0,0,1,0]	**-14.00V**
[1,0,0,1,1]	**-14.00V**
[1,0,1,0,0]	**-14.00V**
[1,0,1,0,1]	**-14.00V**
[1,0,1,1,0]	**-14.00V**
[1,0,1,1,1]	**-14.00V**
[1,1,0,0,0]	**-14.00V**
[1,1,0,0,1]	**-14.00V**
[1,1,0,1,0]	**-14.00V**
[1,1,0,1,1]	**-14.00V**
[1,1,1,0,0]	**-14.00V**
[1,1,1,0,1]	**-14.00V**
[1,1,1,1,0]	**-14.00V**
[1,1,1,1,1]	**-14.00V**

MIPI Address : 0x4E

Address	Bit							
0x4E	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VNLVLH_SEL[6:0]						
Default	0	1	0	0	1	1	1	1

Bit	Name	Description
6:0	VNLVLH_SEL	GAML voltage selection.

[0,0,0,0,0,0,0]	**4.997V**
[0,0,0,0,0,0,1]	**4.997V**
:	**4.997V**
[0,1,0,1,0,0,1]	**4.997V**
[0,1,0,1,0,0,1]	**4.979V**
[0,1,0,1,0,1,1]	**4.961V**
[0,1,0,1,1,0,0]	**4.943V**
[0,1,0,1,1,0,1]	**4.925V**
[0,1,0,1,1,1,0]	**4.907V**
[0,1,0,1,1,1,1]	**4.899V**
:	**-18mv/step**
[1,0,0,1,0,0,0]	**4.455V**
[1,0,0,1,0,0,1]	**4.437V**
[1,0,0,1,0,1,0]	**4.419V**
[1,0,0,1,0,1,1]	**4.401V**
:	**-18mv/step**
[1,1,1,1,1,1,1]	**3.488V**
[1,1,1,1,1,1,1]	**3.470V**

MIPI Address : 0x4F

Address	Bit							
0x4F	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VPLVLH_SEL[6:0]						
Default	0	1	0	1	0	0	0	0

Bit	Name	Description
6:0	VPLVLH_SEL	GAMH voltage selection. [0,0,0,0,0,0,0] -4.997V [0,0,0,0,0,0,1] -4.997V : -4.997V [0,1,0,1,0,0,1] -4.997V [0,1,0,1,0,0,1] -4.989V [0,1,0,1,0,1,1] -4.971V [0,1,0,1,1,0,0] -4.953V [0,1,0,1,1,0,1] -4.935V [0,1,0,1,1,1,0] -4.917V [0,1,0,1,1,1,1] -4.899V : -18mv/step [1,0,0,1,0,0,0] -4.498V [1,0,0,1,0,0,1] -4.480V [1,0,0,1,0,1,0] -4.462V [1,0,0,1,0,1,1] -4.444V : -18mv/step [1,1,1,1,1,1,1] -3.508V [1,1,1,1,1,1,1] -3.490V

MIPI Address : 0X53

Address	Bit							
0x53	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	Positive gamma correction				
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
4:0	Positive gamma correction	For normal black type. 1. GP_00: Setting gamma positive voltage for level 255 . 2. GP_01: Setting gamma positive voltage for level 253 . 3. GP_02: Setting gamma positive voltage for level 250 . 4. GP_03: Setting gamma positive voltage for level 246 . 5. GP_04: Setting gamma positive voltage for level 240 . 6. GP_05: Setting gamma positive voltage for level 232 . 7. GP_06: Setting gamma positive voltage for level 224 . 8. GP_07: Setting gamma positive voltage for level 208 . 9. GP_08: Setting gamma positive voltage for level 176 . 10. GP_09: Setting gamma positive voltage for level 128 . 11. GP_10: Setting gamma positive voltage for level 80 . 12. GP_11: Setting gamma positive voltage for level 48 . 13. GP_12: Setting gamma positive voltage for level 30 . 14. GP_13: Setting gamma positive voltage for level 22 . 15. GP_14: Setting gamma positive voltage for level 14 . 16. GP_15: Setting gamma positive voltage for level 8 . 17. GP_16: Setting gamma positive voltage for level 4 . 18. GP_17: Setting gamma positive voltage for level 2 . 19. GP_18: Setting gamma positive voltage for level 0 . Example: GAMH=4.3V GP_00 voltage is defined as follows

[0,0,0,0,0]	**2.819V**
[0,0,0,0,1]	**2.867V**
[0,0,0,1,0]	**2.914V**
[0,0,0,1,1]	**2.962V**
[0,0,1,0,0]	**3.010V**
:	
[1,1,0,1,1]	**4.109V**
[1,1,1,0,0]	**4.157V**
[1,1,1,0,1]	**4.204V**
[1,1,1,1,0]	**4.252V**
[1,1,1,1,1]	**4.300V**

MIPI Address : 0X54

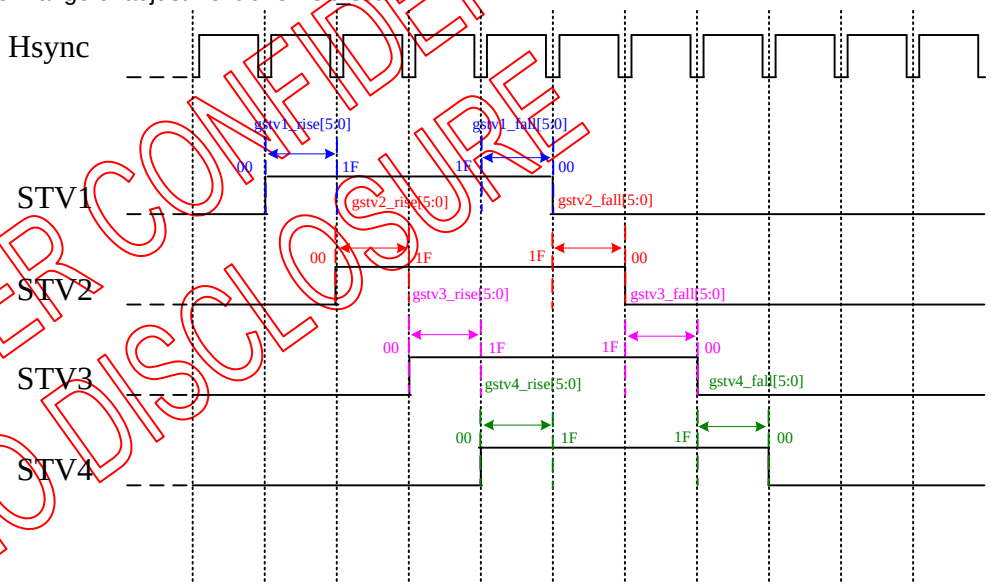
Address	Bit							
0x54	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	Negative gamma correction				
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
4:0	Negative gamma correction	For normal black type. 1. GN_00: Setting gamma negative voltage for level 255 . 2. GN_01: Setting gamma negative voltage for level 253 . 3. GN_02: Setting gamma negative voltage for level 250 . 4. GN_03: Setting gamma negative voltage for level 246 . 5. GN_04: Setting gamma negative voltage for level 240 . 6. GN_05: Setting gamma negative voltage for level 232 . 7. GN_06: Setting gamma negative voltage for level 224 . 8. GN_07: Setting gamma negative voltage for level 208 . 9. GN_08: Setting gamma negative voltage for level 176 . 10. GN_09: Setting gamma negative voltage for level 128 . 11. GN_10: Setting gamma negative voltage for level 80 . 12. GN_11: Setting gamma negative voltage for level 48 . 13. GN_12: Setting gamma negative voltage for level 30 . 14. GN_13: Setting gamma negative voltage for level 22 . 15. GN_14: Setting gamma negative voltage for level 14 . 16. GN_15: Setting gamma negative voltage for level 8 . 17. GN_16: Setting gamma negative voltage for level 4 . 18. GN_17: Setting gamma negative voltage for level 2 . 19. GN_18: Setting gamma negative voltage for level 0 . Example: GAML=-4.3V GN_00 voltage is defined as follows

[0,0,0,0,0]	**-2.819V**
[0,0,0,0,1]	**-2.867V**
[0,0,0,1,0]	**-2.914V**
[0,0,0,1,1]	**-2.962V**
[0,0,1,0,0]	**-3.010V**
:	
[1,1,0,1,1]	**-4.109V**
[1,1,1,0,0]	**-4.157V**
[1,1,1,0,1]	**-4.204V**
[1,1,1,1,0]	**-4.252V**
[1,1,1,1,1]	**-4.300V**

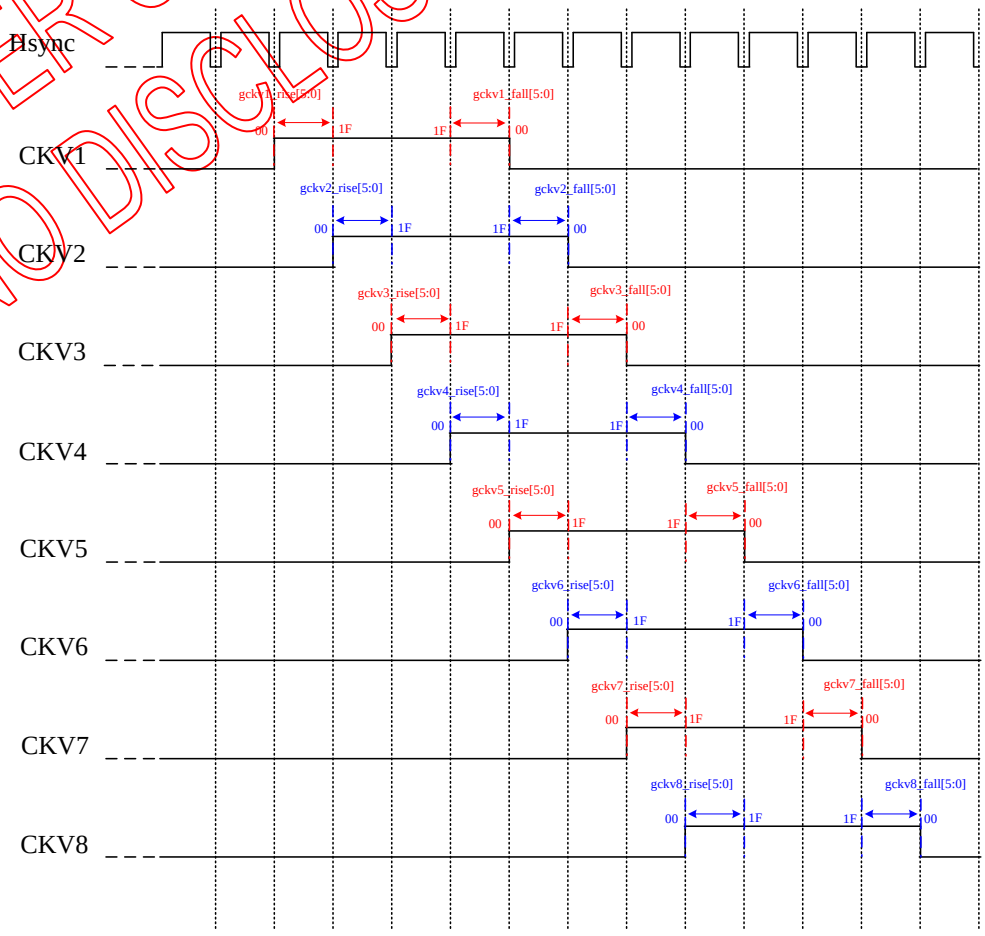
MIPI Address : 0X55

Address	Bit							
0x55	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		gstv					
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
5:0	gstv	1. gstv1_rise: Setting time between Hsync and GIP STV1 rising. 2. gstv1_fall : Setting time between Hsync and GIP STV1 falling. 3. gstv2_rise: Setting time between Hsync and GIP STV2 rising. 4. gstv2_fall : Setting time between Hsync and GIP STV2 falling. 5. gstv3_rise: Setting time between Hsync and GIP STV3 rising. 6. gstv3_fall : Setting time between Hsync and GIP STV3 falling. 7. gstv4_rise: Setting time between Hsync and GIP STV4 rising. 8. gstv4_fall : Setting time between Hsync and GIP STV4 falling. Note : range of adjustment 0~31*sft_scale 

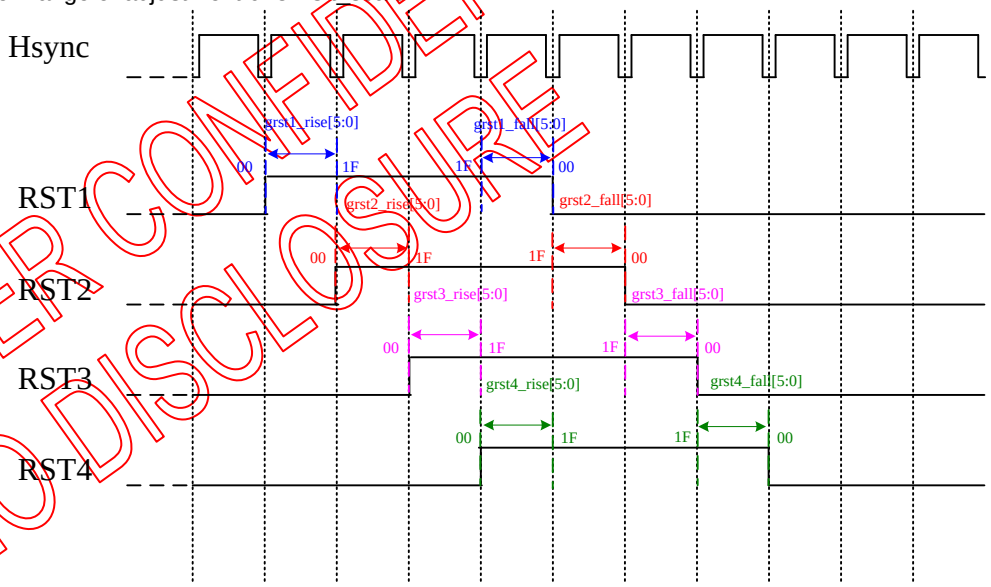
MIPI Address : 0X56

Address	Bit							
0x56	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		gckv					
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
5:0	gckv	1. gckv1_rise: Setting time between Hsync and GIP CKV1 rising. 2. gckv1_fall : Setting time between Hsync and GIP CKV1 falling. 3. gckv2_rise: Setting time between Hsync and GIP CKV2 rising. 4. gckv2_fall : Setting time between Hsync and GIP CKV2 falling. 5. gckv3_rise: Setting time between Hsync and GIP CKV3 rising. 6. gckv3_fall : Setting time between Hsync and GIP CKV3 falling. 7. gckv4_rise: Setting time between Hsync and GIP CKV4 rising. 8. gckv4_fall : Setting time between Hsync and GIP CKV4 falling. 9. gckv5_rise: Setting time between Hsync and GIP CKV5 rising. 10. gckv5_fall : Setting time between Hsync and GIP CKV5 falling. 11. gckv6_rise: Setting time between Hsync and GIP CKV6 rising. 12. gckv6_fall : Setting time between Hsync and GIP CKV6 falling. 13. gckv7_rise: Setting time between Hsync and GIP CKV7 rising. 14. gckv7_fall : Setting time between Hsync and GIP CKV7 falling. 15. gckv8_rise: Setting time between Hsync and GIP CKV8 rising. 16. gckv8_fall : Setting time between Hsync and GIP CKV8 falling. Note : range of adjustment 0~31*stf_scale 

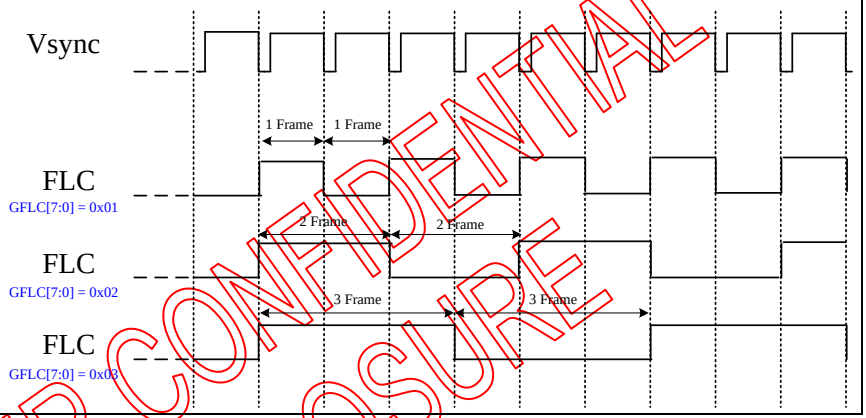
MIPI Address : 0X57

Address	Bit							
0x57	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		grst					
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
5:0	grst	1. grst1_rise : Setting time between Hsync and GIP RST1 rising. 2. grst1_fall : Setting time between Hsync and GIP RST1 falling. 3. grst2_rise: Setting time between Hsync and GIP RST2 rising. 4. grst2_fall : Setting time between Hsync and GIP RST2 falling. 5. grst3_rise: Setting time between Hsync and GIP RST3 rising. 6. grst3_fall : Setting time between Hsync and GIP RST3 falling. 7. grst4_rise: Setting time between Hsync and GIP RST4 rising. 8. grst4_fall : Setting time between Hsync and GIP RST4 falling. Note : range of adjustment 0~31*sft_scale 

MIPI Address : 0X58

Address	Bit							
0x58	D7	D6	D5	D4	D3	D2	D1	D0
Name	GFLC							
Default	0	0	0	0	1	0	0	0

Bit	Name	Description
7:0	GFLC	GFLC : flc toggle frequency select Note : range of adjustment 1~255 Frame , 0 is diable 

MIPI Address : 0X5E

Address	Bit							
0x5E	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	nchg_cs_en	-	-	-	-	-	-
Default	0	0	0	0	0	0	1	1

Bit	Name	Description
6	nchg_cs_en	Source EQ 0 : Disable 1 : Enable

MIPI Address : 0X60

Address	Bit							
0x60	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRIM_VDD18F[7:5]							
Default	1	0	1	1	0	0	0	0

Bit	Name	Description
7:5	TRIM_VDD18F	Internal power supply for MIPI/LVDS circuits. **[0,0,0] 1.763V** **[0,0,1] 1.690V** **[0,1,0] 1.615V** **[0,1,1] 1.539V** **[1,0,0] 1.834V** **[1,0,1] 1.905V** **[1,1,0] 1.976V** **[1,1,1] 2.046V**

MIPI Address : 0X63

Address	Bit							
0x65	D7	D6	D5	D4	D3	D2	D1	D0
Name		lan_sel			-	-		
Default	0	0	0	0	0	1	1	0

Bit	Name	Description
6:5	lan_sel	MIPI lane number selection It do XOR operation with Pin setting.

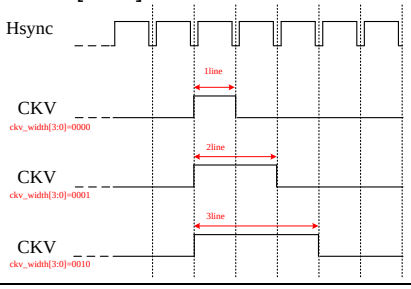
MIPI Address : 0X65

Address	Bit							
0x65	D7	D6	D5	D4	D3	D2	D1	D0
Name	-				goa_updn	-		
Default	0	0	0	0	1	0	0	0

Bit	Name	Description
3	goa_updn	GIP signal Scan direction 1: Forward 0: Backward

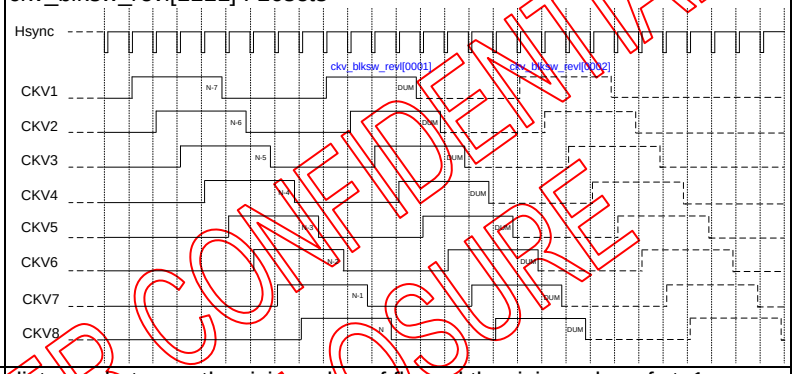
MIPI Address : 0X67

Address	Bit							
0x67	D7	D6	D5	D4	D3	D2	D1	D0
Name	phase				ckv_width			
Default	1	0	0	0	0	0	1	0

Bit	Name	Description
7:4	phase	ckv phase select. phase[0000] : 2phase phase[0001] : 2phase phase[0010] : 2phase phase[0011] : 3phase phase[0100] : 4phase phase[0101] : 5phase … phase[1111] : 12phase
3:0	ckv_width	ckv width ckv width[0000] : 1line ckv width[0001] : 2line ckv width[0010] : 3line … ckv width[1111] : 16line 

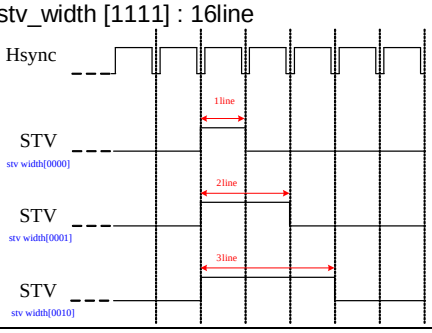
MIPI Address : 0X68

Address	Bit							
0x68	D7	D6	D5	D4	D3	D2	D1	D0
Name	ckv_blksw_revl				flc_trans_stvsp_dis			
Default	0	0	0	1	0	1	1	0

Bit	Name	Description
7:4	ckv_blksw_revl	when ckv keeps toggling at blanking, the quantity of sets of ckv. ckv_blksw_revl[0000] : 1sets ckv_blksw_revl[0001] : 2sets ckv_blksw_revl[0010] : 3sets … ckv_blksw_revl[1111] : 16sets 
3:0	flc_trans_stvsp_dis	distance between the rising edge of flc and the rising edge of stv1 flc_trans_stvsp_dis[0000] : 0line flc_trans_stvsp_dis[0001] : 1line … flc_trans_stvsp_dis[1111] : 15line

MIPI Address : 0X69

Address	Bit							
0x69	D7	D6	D5	D4	D3	D2	D1	D0
Name	stv_width				flc_stag_trans_stvsp_dis			
Default	0	0	1	0	0	1	1	1

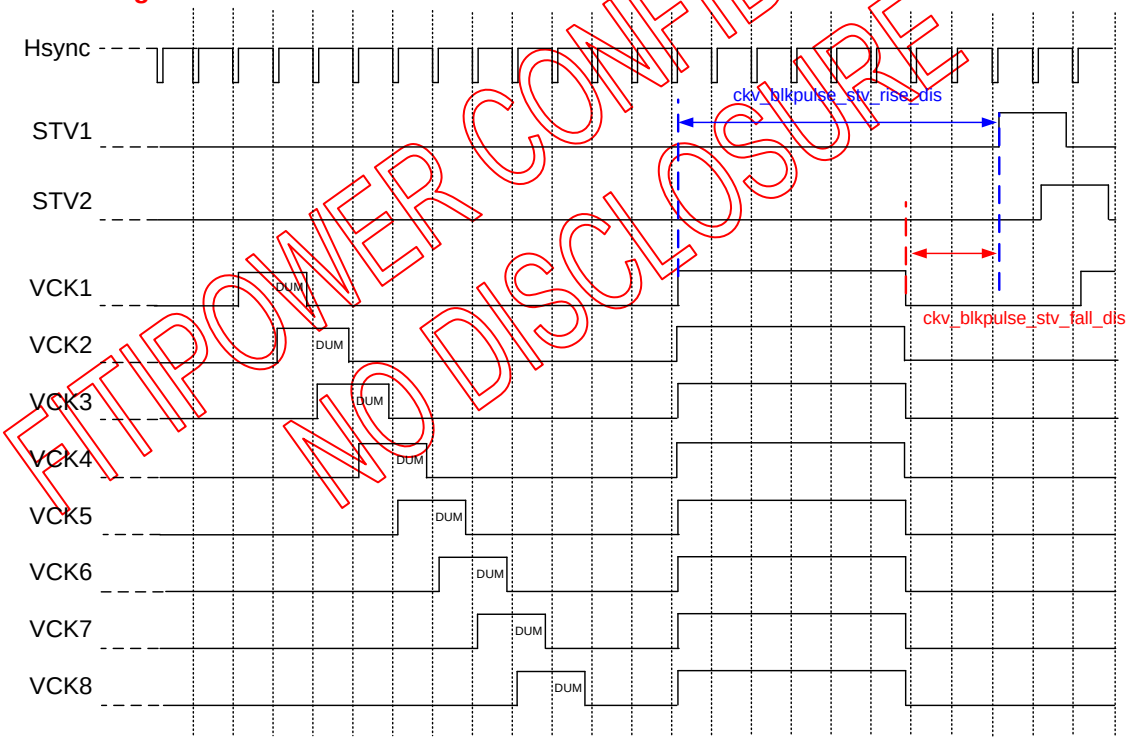
Bit	Name	Description
7:4	stv_width	stv width. stv_width [0000] : 1line stv_width [0001] : 2line … stv_width [1111] : 16line 
3:0	flc_stag_trans_stvsp_dis	distance between the falling edge of flc and the rising edge of stv1 flc_stag_trans_stvsp_dis[0000] : 0lime flc_stag_trans_stvsp_dis[0001] : 1lime … flc_stag_trans_stvsp_dis[1111] : 1lime

MIPI Address : 0X6A

Address	Bit							
0x6A	D7	D6	D5	D4	D3	D2	D1	D0
Name	ckv_blkpulse_stv_rise_dis				ckv_blkpulse_stv_fall_dis			
Default	1	0	1	0	0	0	1	0

Bit	Name	Description
7:4	ckv_blkpulse_stv_rise_dis	distance between the rising edge of ckv xon and the rising edge of stv1. ckv_blkpulse_stv_rise_dis[0000] : 0line ckv_blkpulse_stv_rise_dis[0001] : 1line … ckv_blkpulse_stv_rise_dis[1111] : 15line
3:0	ckv_blkpulse_stv_fall_dis	distance between the falling edge of ckv xon and the rising edge of stv1 ckv_blkpulse_stv_fall_dis[0000] : 0line ckv_blkpulse_stv_fall_dis[0001] : 1line … ckv_blkpulse_stv_fall_dis[1111] : 15line

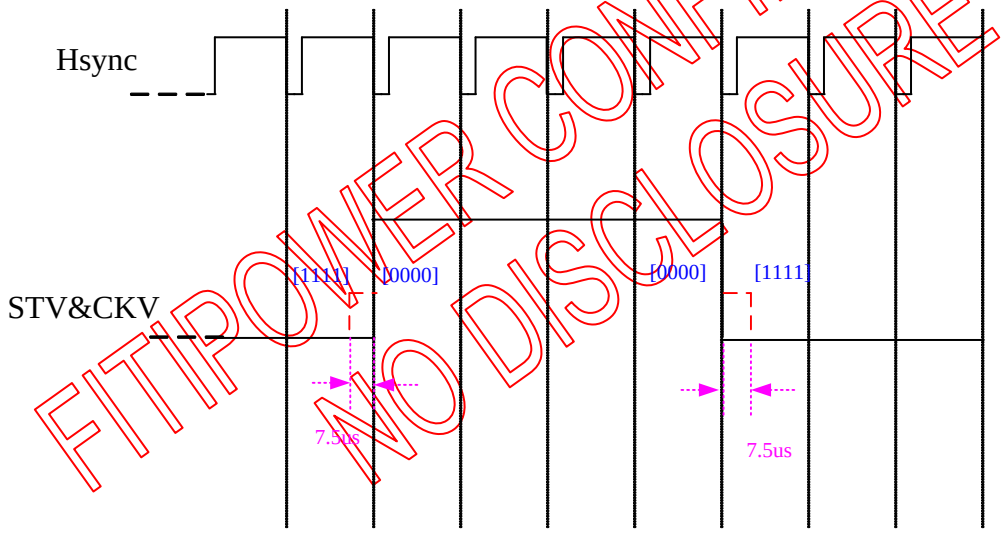
GIP timing



MIPI Address : 0X6B

Address	Bit							
0x6B	D7	D6	D5	D4	D3	D2	D1	D0
Name	eq_fall				eq_rise			
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	eq_fall	eq time select for falling edge [0000] : disable [0001] : 0.5us [0010] : 1us … [1111] : 7.5us
3:0	eq_rise	eq time select for rising edge [0000] : disable [0001] : 0.5us [0010] : 1us … [1111] : 7.5us



MIPI Address : 0X6C

Address	Bit							
0x6C	D7	D6	D5	D4	D3	D2	D1	D0
Name	dummy_en	flc_stag_en	ckv_blkpulse_stagger_sel		ckv_blkpulse_phase_sel	ckv_blkpulse_en	ckv_blksw_logic	stv_ckv_select
Default	0	0	0	0	1	0	0	0

Bit	Name	Description
7	dummy_en	ckv pre-dummy
6	flc_stag_en	the relation between flc1 and flc2 0 : not stagger 1 : stagger
5:4	ckv_blkpulse_stagger_sel	stagger time select for ckv blanking xon [00] : disable [01] : 0.5u [10] : 1u [11] : 1.5u
3	ckv_blkpulse_phase_sel	stagger phase select for ckv blanking xon 0 : 2 phase 1 : 4 phase
2	ckv_blkpulse_en	when ckv stops at blanking, ckv xon at blanking 0 : disable 1 : enable
1	ckv_blksw_logic	ckv logic when ckv stops at blanking 0 : logic 0 1 : logic 1
0	stv_ckv_select	the relation between stv and ckv 0 : overlap 1 : stagger

MIPI Address : 0X6D

Address	Bit							
0x6D	D7	D6	D5	D4	D3	D2	D1	D0
Name		-		sft_goe_scale	-	sft_goe_drct		stv_ckv_sft
Default	0	0	0	0	0	0	0	1

Bit	Name	Description
4	sft_goe_scale	sft_dat scale 0 : 8*osc_clk 1 : 24*osc_clk
2:1	sft_goe_drct	sft_goe_drct rising forward, falling backward (default)
0	stv_ckv_sft	the shift between stv and ckv when overlap 0 : 1 line 1 : 2line

MIPI Address : 0X73

Address	Bit							
0x73	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	hv_learn	de_edge_sel	-	-	-	-
Default	0	0	1	1	0	0	0	1

Bit	Name	Description
4	de_edge_sel	set Gate clock falling location depend on DE rising or DE falling in MIPI mode. 0 : Rising 1 : Falling
5	hv_learn	learning H line length and V line numbers from TX, not reference RES setting value. 0:Non-Learning 1: Learning

MIPI Address : 0X74

Address	Bit							
0x74	D7	D6	D5	D4	D3	D2	D1	D0
Name	-			mipi_gip_hss_sel				
Default	0	0	0	1	0	0	0	0

Bit	Name	Description
4	mipi_gip_hss_sel	GIP reference H sync / V sync pulse from TX in MIPI mode. 0 : Disable 1 : Enable

MIPI Address : 0X77

Address	Bit							
0x77	D7	D6	D5	D4	D3	D2	D1	D0
Name	-			-	CLK_SEL_VGL		-	-
Default	0	0	0	1	0	0	0	0

Bit	Name	Description
4	CLK_SEL_VGL	VGL pump clock frequency selection.

MIPI Address : 0x78

Address	Bit							
0x78	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VGH_REG_SEL[4:0]				
Default	0	1	0	0	0	1	1	1

Bit	Name	Description
4:0	VGH_REG_SEL	VGH_REG voltage selection.

[0,0,0,0,0]	**14.17V**
[0,0,0,0,1]	**14.17V**
[0,0,0,1,0]	**14.17V**
[0,0,0,1,1]	**14.17V**
[0,0,1,0,0]	**14.17V**
[0,0,1,0,1]	**14.17V**
[0,0,1,1,0]	**14.17V**
[0,0,1,1,1]	**14.17V**
[0,1,0,0,0]	**14.17V**
[0,1,0,0,1]	**14.17V**
[0,1,0,1,0]	**14.17V**
[0,1,0,1,1]	**14.10V**
[0,1,1,0,0]	**13.86V**
[0,1,1,0,1]	**13.62V**
[0,1,1,1,0]	**13.29V**
[0,1,1,1,1]	**13.07V**
[1,0,0,0,0]	**12.85V**
[1,0,0,0,1]	**12.54V**
[1,0,0,1,0]	**12.25V**
[1,0,0,1,1]	**12.07V**
[1,0,1,0,0]	**11.80V**
[1,0,1,0,1]	**11.54V**
[1,0,1,1,0]	**11.29V**
[1,0,1,1,1]	**11.06V**
[1,1,0,0,0]	**10.76V**
[1,1,0,0,1]	**10.57V**
[1,1,0,1,0]	**10.28V**
[1,1,0,1,1]	**10.03V**
[1,1,1,0,0]	**9.78V**
[1,1,1,0,1]	**9.54V**
[1,1,1,1,0]	**9.27V**
[1,1,1,1,1]	**9.06V**

MIPI Address : 0X7B

Address	Bit							
0x7B	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	GRB
Default	0	0	0	0	0	0	0	1

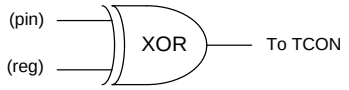
Bit	Name	Description
0	GRB	7B=”00” → Reset status. 7B=”01” → Normal display.

MIPI Address : 0XFA

Address	Bit							
0xFA	D7	D6	D5	D4	D3	D2	D1	D0
Name	Vender ID							
Default	0	0	1	0	1	0	0	1

Bit	Name	Description
7:0	Vender ID	The register is defines vender id for customer.

9.4.2 Function truth table

Combination Logic	Truth table		
	PIN	REG	To Tcon
	0	0	0
	0	1	1
	1	0	1
	1	1	0

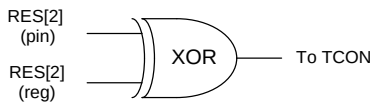
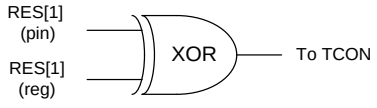
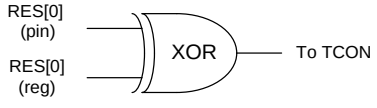
LNSW[1:0] do XOR operation.(MIPI I/F)

To Tcon		MIPI Lane Mapping				
LNSW[1]	LNSW[0]	D0(PAD)	D1(PAD)	CLK(PAD)	D2(PAD)	D3(PAD)
0	0	D3	D2	CLK	D1	D0
0	1	D3	D0	CLK	D1	D2
1	0	D0	D1	CLK	D2	D3
1	1	D2	D1	CLK	D0	D3

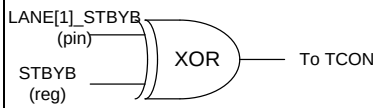
LNSW[1:0] do XOR operation.(LVDS I/F)

To Tcon				LVDS Lane Mapping				
LNSW[3] (OTP)	LNSW[2] (OTP)	LNSW[1]	LNSW[0]	D0(PAD)	D1(PAD)	CLK(PAD)	D2(PAD)	D3(PAD)
0	0	0	0	D3	D2	CLK	D1	D0
0	0	0	1	D3	D0	CLK	D1	D2
0	0	1	0	D0	D1	CLK	D2	D3
0	0	1	1	D0	D1	D2	CLK	D3
0	1	0	0	CLK	D0	D1	D2	D3
0	1	0	1	CLK	D3	D2	D1	D0
0	1	1	0	D3	D2	D1	D0	CLK
0	1	1	1	D0	D1	D2	D3	CLK
1	0	0	0	D3	D0	CLK	D1	D2
1	0	0	1	D2	D1	CLK	D0	D3

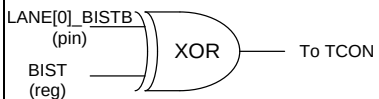
RES[2:0] do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	Display resolution selection. RES[2:0] = 000, 400RGBx1280/480RGBx1280.
	0	1	1	
	1	0	1	
	1	1	0	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	

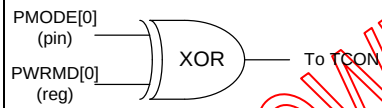
STBYB do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	STBYB mode selection. STBYB = 0, STBYB mode. STBYB = 1, Normal Display mode.
	0	1	1	
	1	0	1	
	1	1	0	

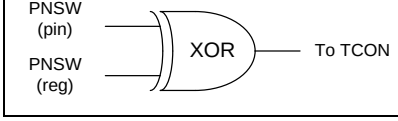
BIST do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	Normal Operation / BIST pattern select. BIST_EN = 0, BIST. BIST_EN = 1, Normal Operation.
	0	1	1	
	1	0	1	
	1	1	0	

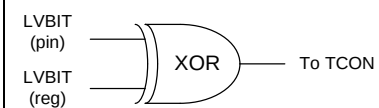
PWRMD do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	Power mode selection. PWRMD[1:0] = 00, VSP/VSN: JD5001/2. VGH/VGL: External. PWRMD[1:0] = 01, VSP/VSN: External. VGH/VGL: Charge pump. PWRMD[1:0] = 10, VSP/VSN: JD5001/2. VGH/VGL: Charge pump. PWRMD[1:0] = 11, VSP/VSN: External. VGH/VGL: External.
	0	1	1	
	1	0	1	
	1	1	0	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	

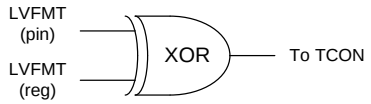
PNSW do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	MIPI Lane polarity swap. PNSW = 0, P/N polarity swap. PNSW = 1, Normal.
	0	1	1	
	1	0	1	
	1	1	0	

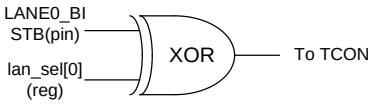
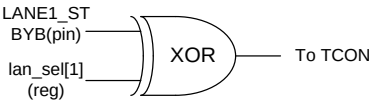
LVBIT do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	6-bit / 8-bit input select for LVDS mode. LVBIT = 0, 6-bit. LVBIT = 1, 8-bit.
	0	1	1	
	1	0	1	
	1	1	0	

LVFMT do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	8-bit input format select for LVDS mode. LVFMT = 0, JEIDA format. LVFMT = 1, VESA format.
	0	1	1	
	1	0	1	
	1	1	0	

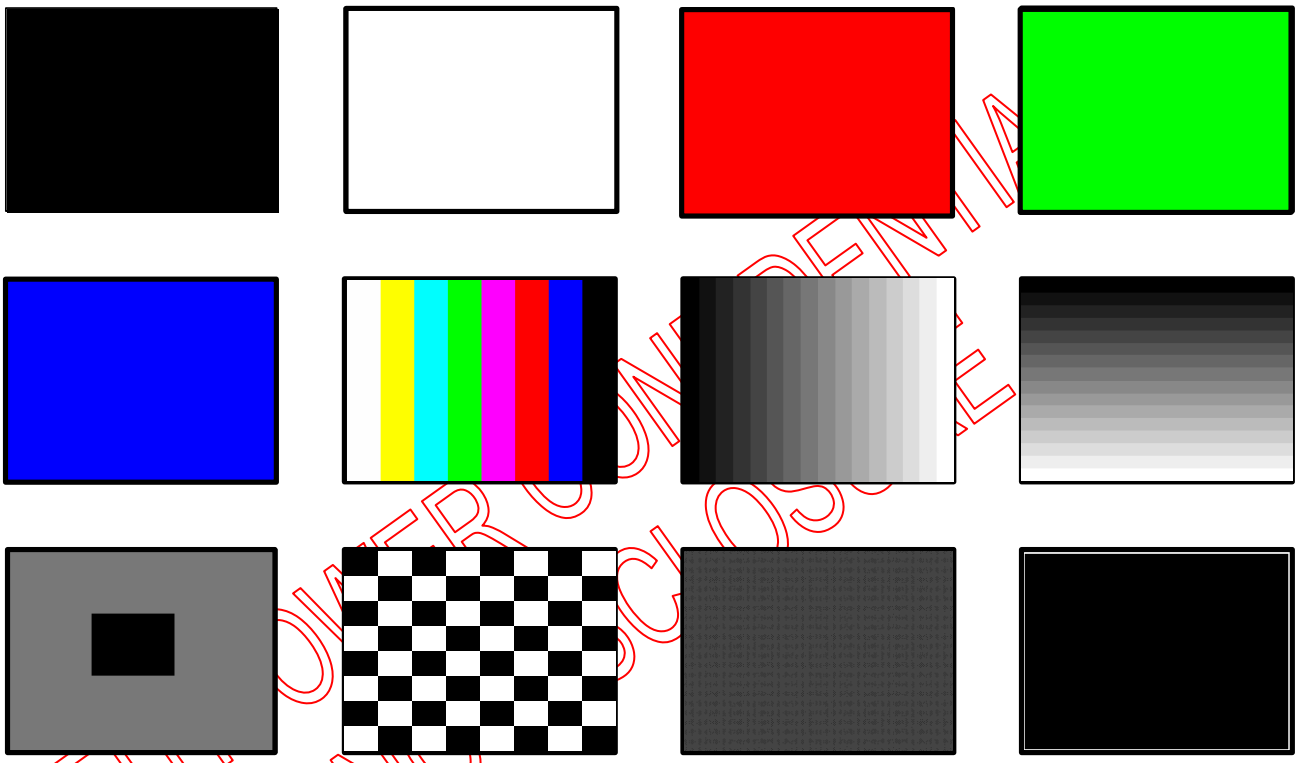
lan_sel do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	MIPI lane number selection . lan_sel[1:0] = 10, MIPI 3 lane. lan_sel[1:0] = 11, MIPI 4 lane.
	0	1	1	
	1	0	1	
	1	1	0	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	

10. FUNCTION DESCRIPTION

10.1 BIST pattern

We support the BIST mode to test panel and debug. It can stop pattern at any time while LANE[0]_BISTB set to high. The pattern sequence is listed below.



Black→White→R→G→B→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Flicker pattern→Black background with white out frame

10.2 XON function

When power is removed from an electronic device during display, the image still keeps on the LCD panel for a long time. XON function can speed the process that image disappears.

The XON function is a voltage detector. By XON circuit, EK79030 can detect low voltage of power and send control signal to discharge residual potential in LCD panel and remove image.

In the following case, the chip will entry XON function.

1. VDD is lower than 1.7V.

XON function:

1. Source output pull to VSSA.
2. All GOA signals will be set to VGH voltage level.
3. Stop charge pump function.
4. VCOM output pull to VSSA.

The XON function has debounce protection circuit. EX: If duration of voltage drop on VDD is less than 20us (**EX: induced by ESD pulse**), the XON function will not be active even the VDD voltage level is less than 1.7V.

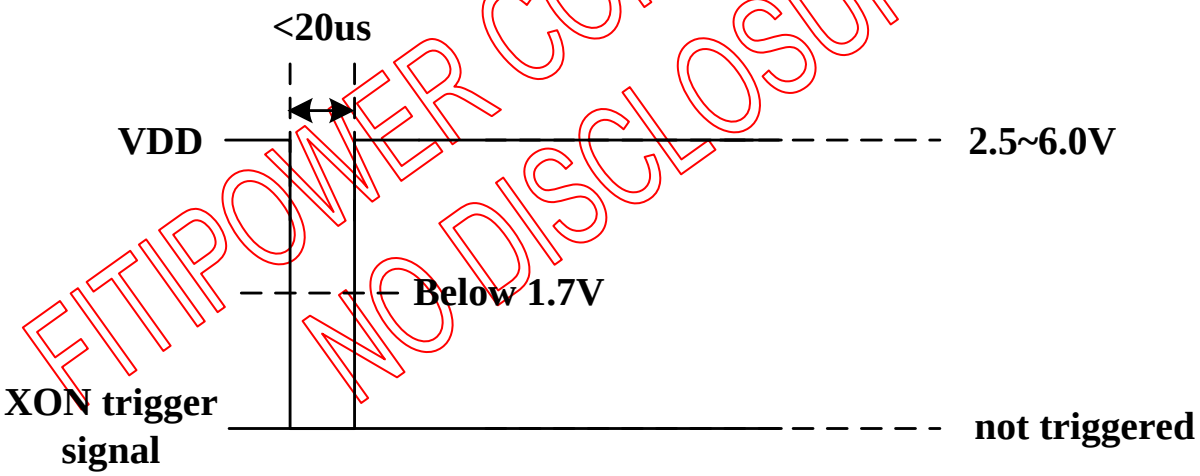
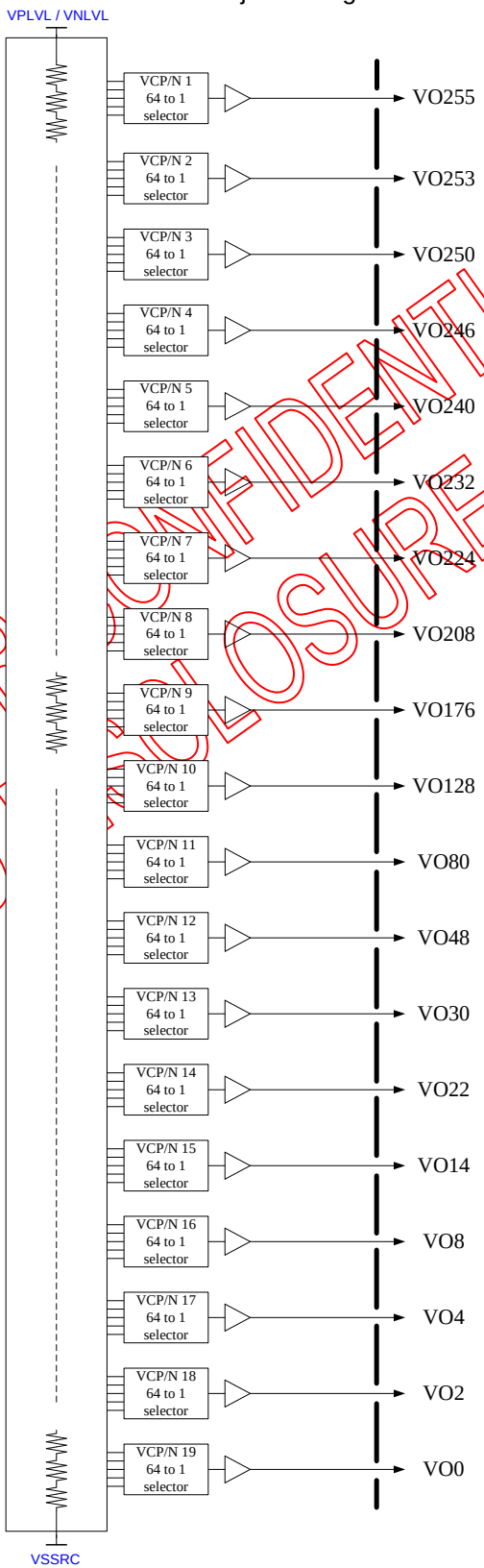


Figure 9.1: XON function vs. VDD

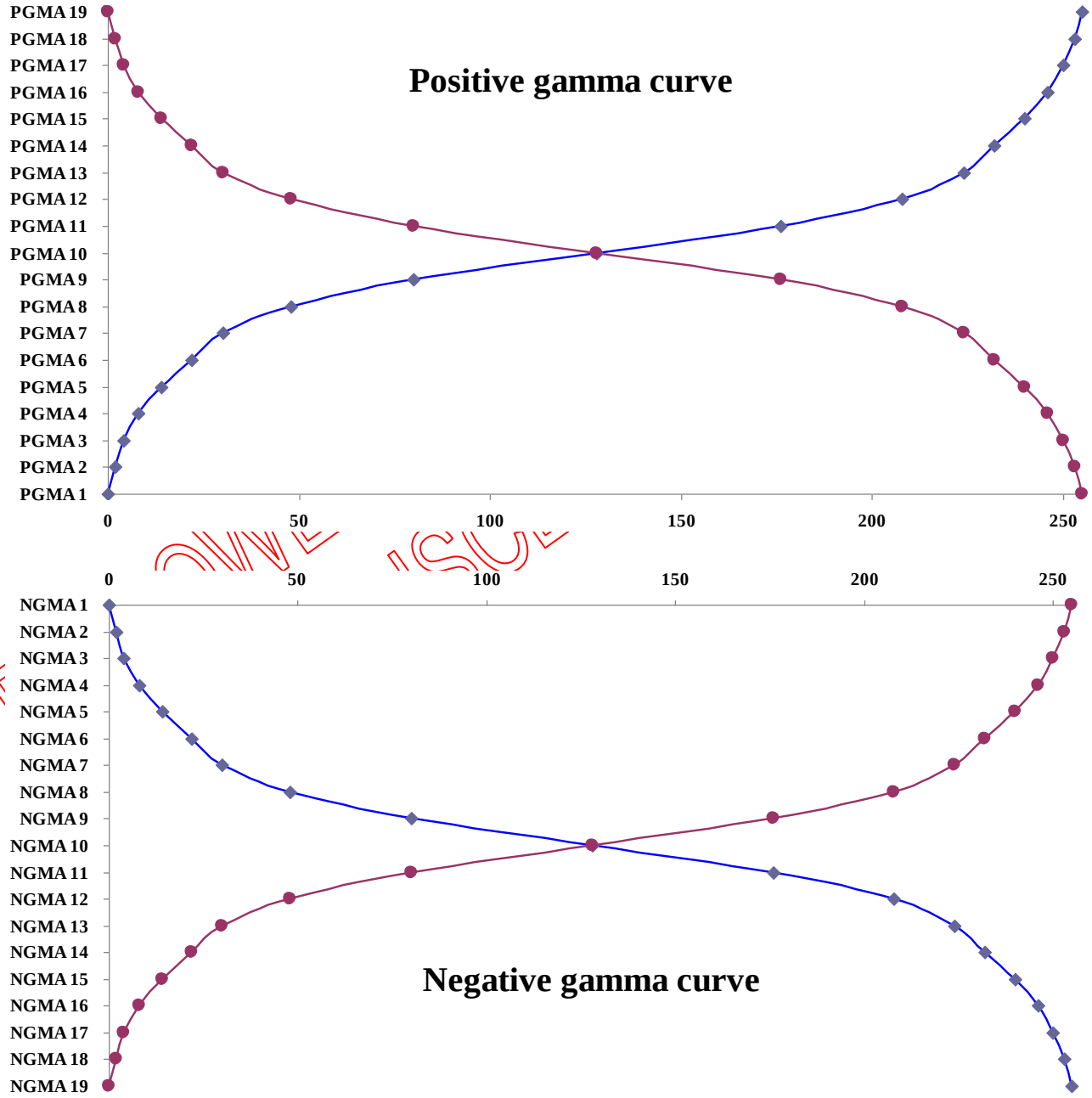
11. GAMMA CORRECTION CIRCUIT

We use the gamma resistor stream and 64-to-1 selector to adjust voltage



11.1 Gamma Architecture

The gamma correction are done by 18-segment piecewise linear interpolation. The 18 segments are defined with 19 register values for level 0, 2, 4, 8, 14, 22, 30, 48, 80, 128, 176, 208, 224, 232, 240, 246, 250, 253 and 255. These total 19 register values defined the positive and negative gamma curve.



The blue line is for normal black type, the red line is for normal white type.

12. DC CHARACTERISTICS

12.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
I/O voltage	VDDIO_IF	1.8	-	3.6	V	
	VDDIO					
Power input	VDD	2.5	-	3.6	V	
VSP voltage	VSP	4.5	-	6	V	
VSN voltage	VSN	-4.5	-	-6	V	
VOTP power	VOTP	-	7.5	-	V	
Operating Temperature		-20	-	85	℃	(1)

Note :(1) Do not let condensation for low temperature

Table 12.1: Absolute maximum rating

12.2 Typical operating condition

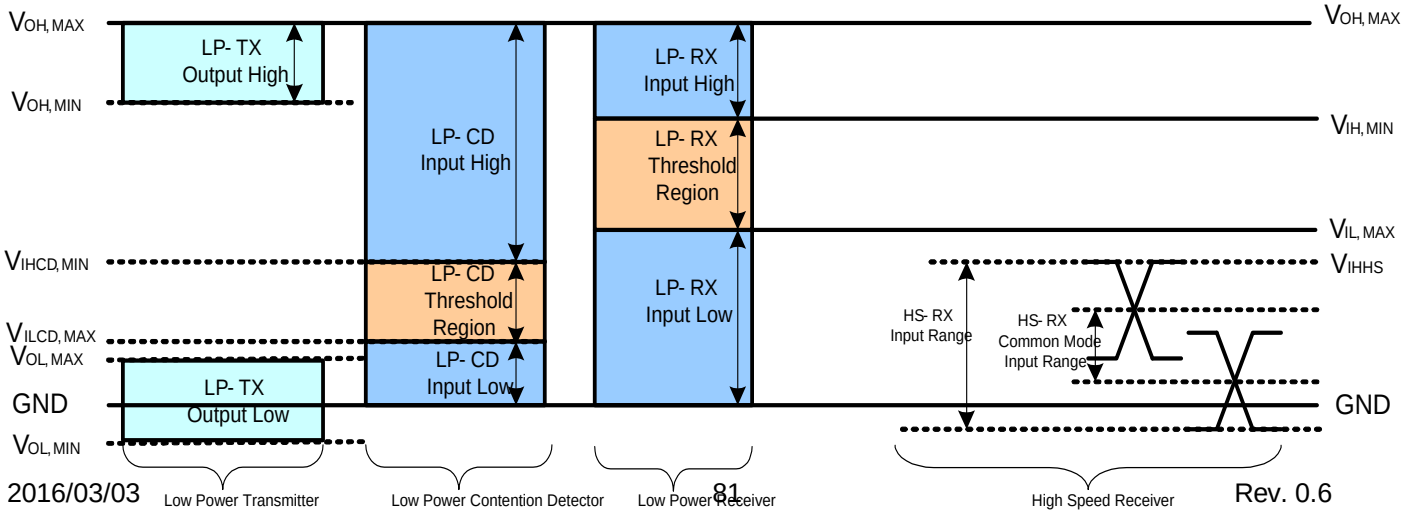
Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
VDD voltage	VDD	-	3.3	-	V	Digital supply voltage
VDDP voltage	VDDP	-	3.3	-	V	Analog supply voltage
VDDIO voltage	VDDIO	-	3.3	-	V	I/O Power supply voltage
VOTP voltage	VOTP	-	7.5	-	V	Programming voltage
VSP voltage	VSP	4.5	5.0	6	V	VSP voltage
VSN voltage	VSN	-4.5	-5.0	-6	V	VSN voltage
VGH voltage	VGH	9.3	-	18	V	VGH voltage
VGL voltage	VGL	-16	-	-6.7	V	VGL voltage

Table 12.2 : Typical operating conditions

12.3 DC electrical characteristics

(Test condition: VCI=1.6~3.6V, TA=-20℃~+85℃,VSS=VSSA=0V)

Parameter		Symbol	Spec.			Unit	Note
			Min.	Typ.	Max.		
VDDIO Input high level voltage		VIH	0.8 x VDDIO		VDDIO	V	
VDDIO input low level voltage		VIL	VSS		0.2 x VDDIO	V	
Input Leakage Current		Ileak	(-1)		(+1)	μA	
VGL_REG2 output voltage		VGL_REG2		TBD		V	
VGMP output voltage		VGMP		TBD		V	
VGMN output voltage		VGMN		TBD		V	
VCI1 output voltage		VCI1		TBD		V	
VGL output voltage		VGL_O	-16		-6	V	
VGH output voltage		VGH_O	8		19	V	
VCL output voltage		VCL	-2.1	-2.4	-3	V	
VOM output voltage		VCOM	-2.75	-1.48	-0.2	V	
Input terminal resistance		ZID		100		ohm	
Source output level deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255			TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240			TBD		mV	
	Graycode = 32 ~ 207			TBD		mV	
Source output offset deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255	-		TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240	-		TBD		mV	
	Graycode = 32 ~ 207	-		TBD		mV	
Current consumption	Analog Operating	IAOP		TBD		mA	
	Analog Stand-by	IAST		TBD		mA	
Rush current		Ivddpeak		TBD		mA	
VOTP operation current		Ivpp		TBD		mA	



13. AC CHARACTERISTICS

13.1 MIPI AC characteristics

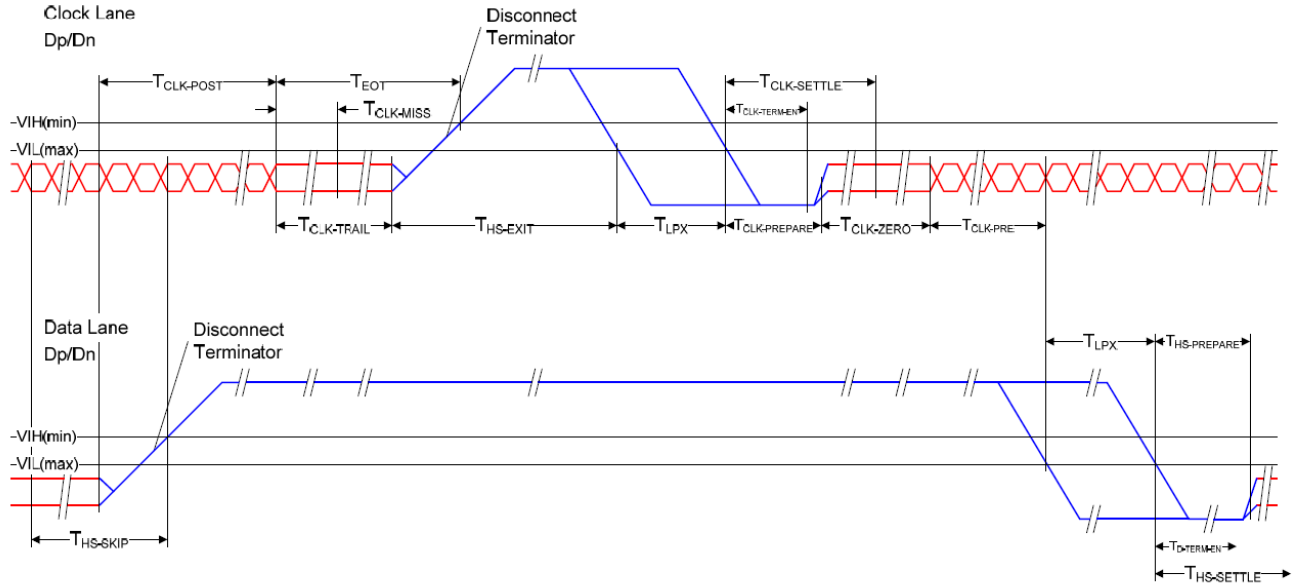


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

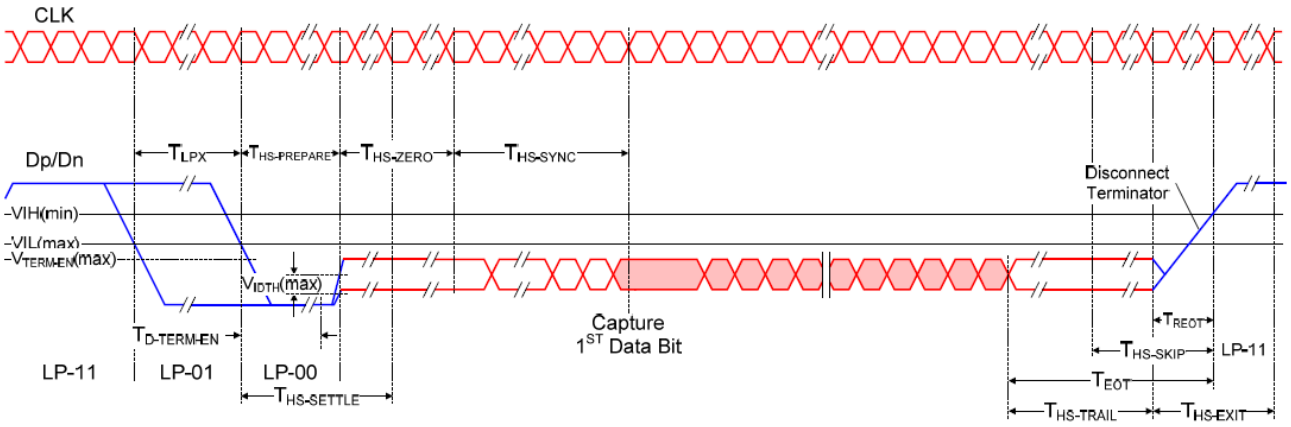


Figure 13.2: Timing of high-speed data transmission in bursts

13.2 MIPI data-clock timing specification

Parameter	Descript	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI (For DCS)	-		ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-		ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

13.3 LVDS mode AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{xFCLK}	30	-	TBD	MHz	Refer to input timing table for each display resolution
Input data skew margin	T_{RSKM}	500	-	-	ps	|VID| = 200mV RxVCM = 1.2V RxFCLK = 81MHz
Clock high time	T_{LVCH}	-	4/(7* R_{xFCLK})	-	ns	
Clock low time	T_{LVCL}	-	3/(7* R_{xFCLK})	-	ns	
PLL wake-up time	T_{enPLL}	-	-	150	us	

Table 13.1: LVDS mode AC electrical characteristics

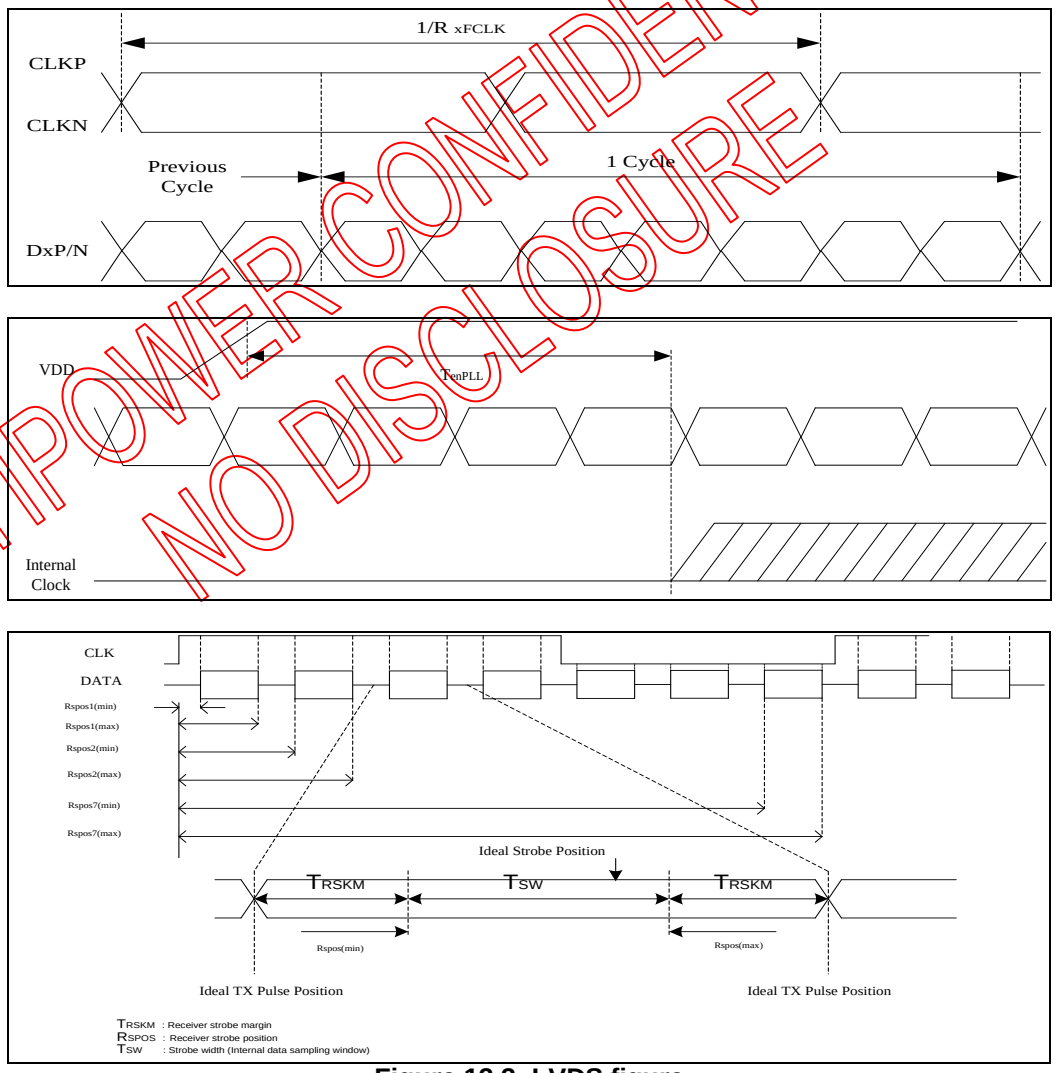
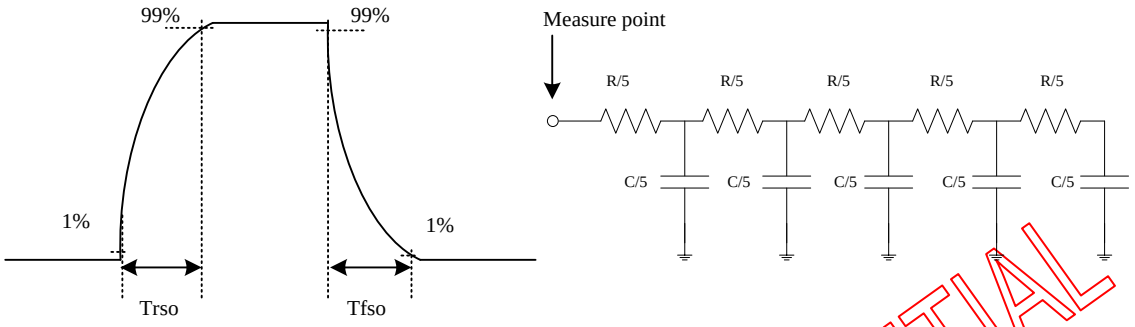


Figure 13.3: LVDS figure

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Modulation Frequency	SSC_{MF}	23	-	93	KHz	
Modulation Rate	SSC_{MR}	-	-	+3	%	

Table 12.2: SSC table

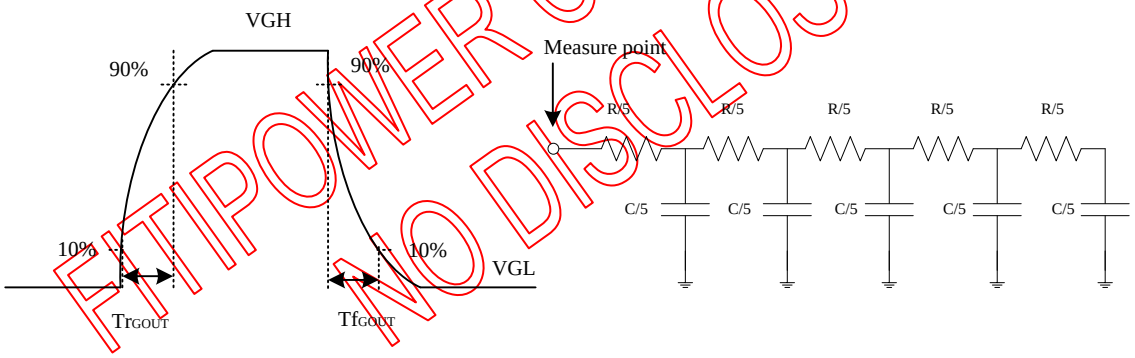
13.4 Source output timing (SOUT961 ~ SOUT2400, SDUMY)



Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Source driver rising time	Trso	TBD	-	-	TBD	µs
Source driver falling time	Tfso	TBD	-	-	TBD	µs

Table 13.3: Source output timing

Panel control signal output (GOUTL[1]~GOUTL[22] , GOUTR[1]~GOUTR[22])



Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Panel control signal rising time	T_{rGOUT}	TBD	-	-	TBD	µs
Panel control signal falling time	T_{fGOUT}	TBD	-	-	TBD	µs

Table 13.4: GOA output timing

13.5 Serial interface characteristics

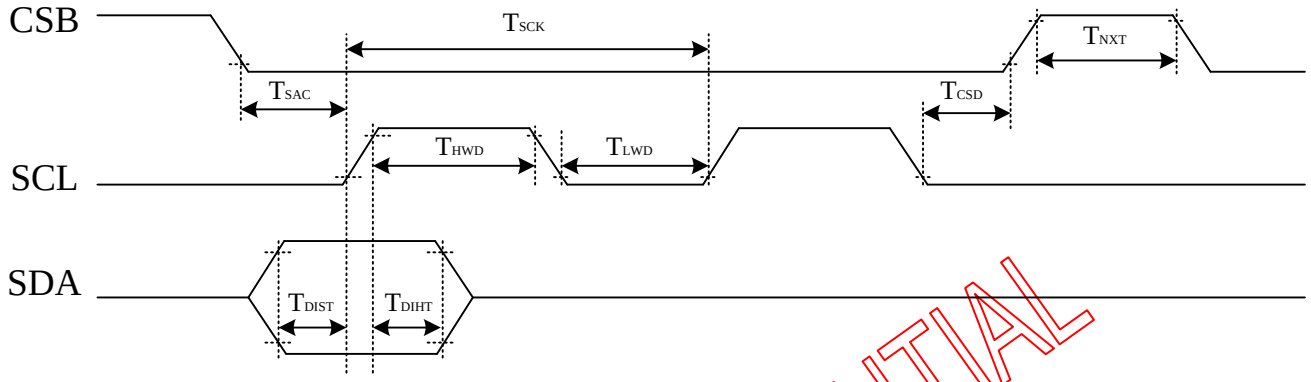


Figure 13.4: Serial interface characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
CSB assertion to first clock edge	T_{SAC}		120	-	-	ns
CSB deassertion frome last clock edge	T_{CSD}		120	-	-	ns
CSB next control enable	T_E		200	-	-	ns
SCL period time	T_{SCK}		200	-	-	ns
SCL high period time	T_{HWD}		100	-	-	ns
SCL low period time	T_{LWD}		100	-	-	ns
SDA input data setup time	T_{DIST}		50	-	-	ns
SDA input data hold time	T_{DIHT}		50	-	-	ns

13.6 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.6V, VSS=0V, T_A=-20 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		20	-	-	μs

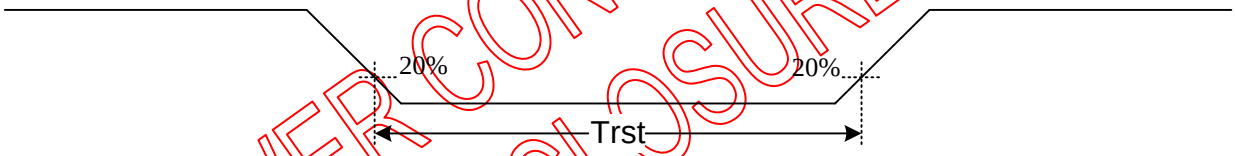
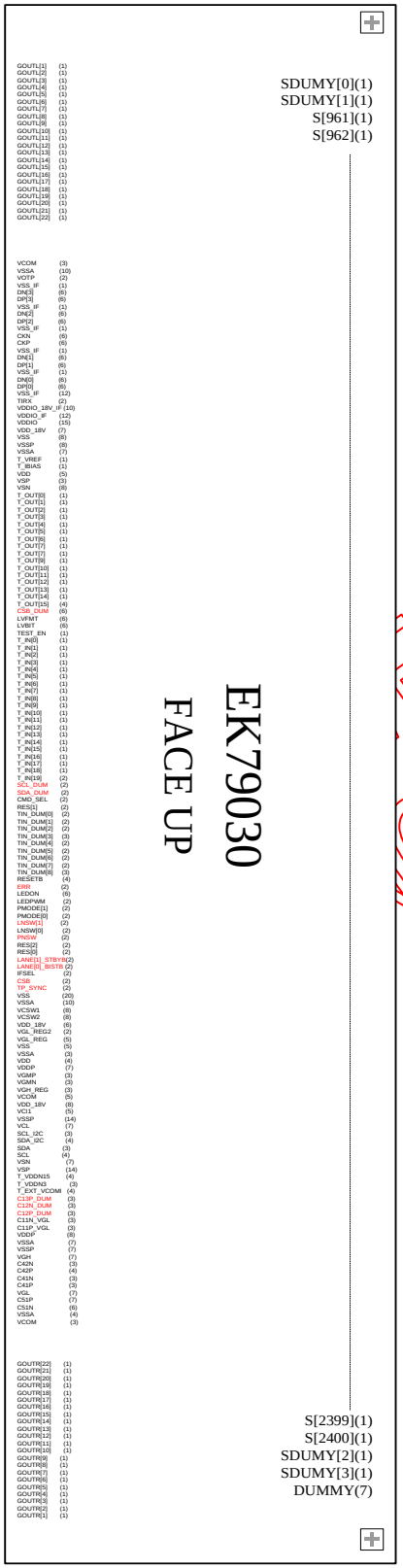


Figure 13.5: Reset timing

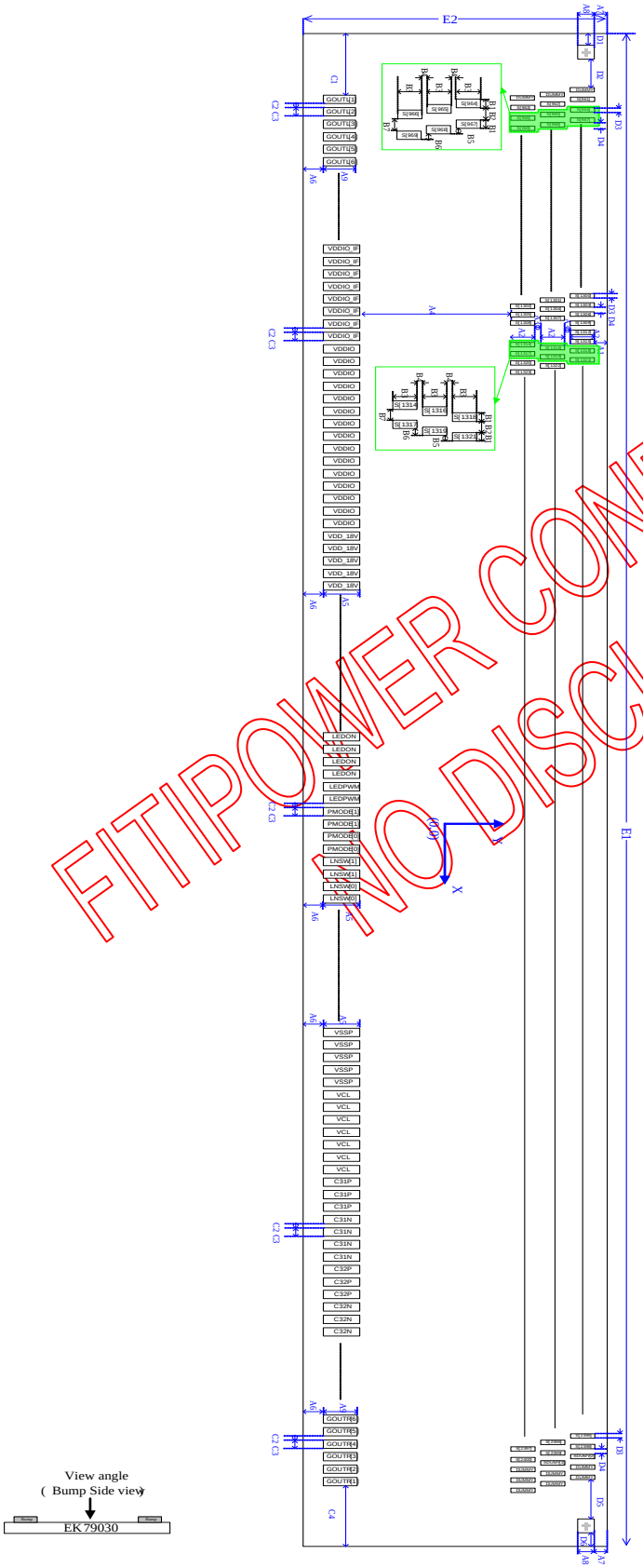
14. PIN ASSIGNMENT (IC FACE VIEW)

14.1 Pad sequence



14.2 Bump information

14.2.1 Chip outline dimension



14.2.2 Pad information

Symbol	Dimension
A1	33
A2	73
A3	17
A4	469
A5	93
A6	32
A7	33
A8	50
A9	43

Symbol	Dimension
B1	16
B2	17
B3	73
B4	17
B5	11
B6	11
B7	17
-	
-	

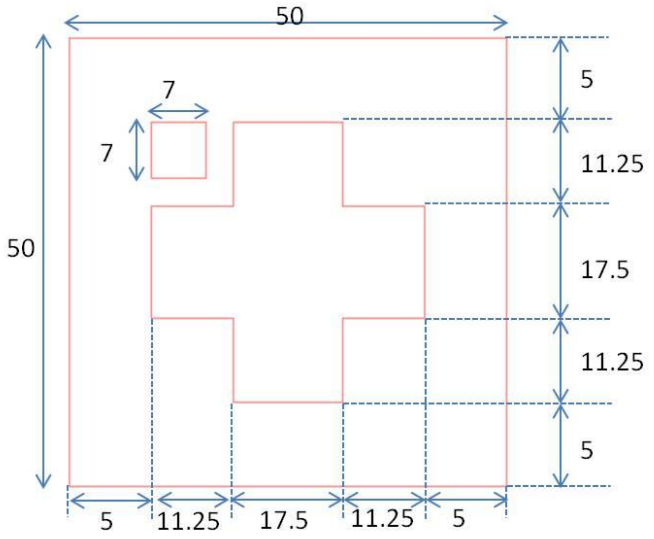
Symbol	Dimension
C1	206.5
C2	13
C3	32
C4	15
C5	30
C6	25
C7	206.5
-	
-	

Symbol	Dimension
D1	69
D2	49.5
D3	16
D4	17
D5	71.5
D6	69
E1	27600
E2	880
-	
-	

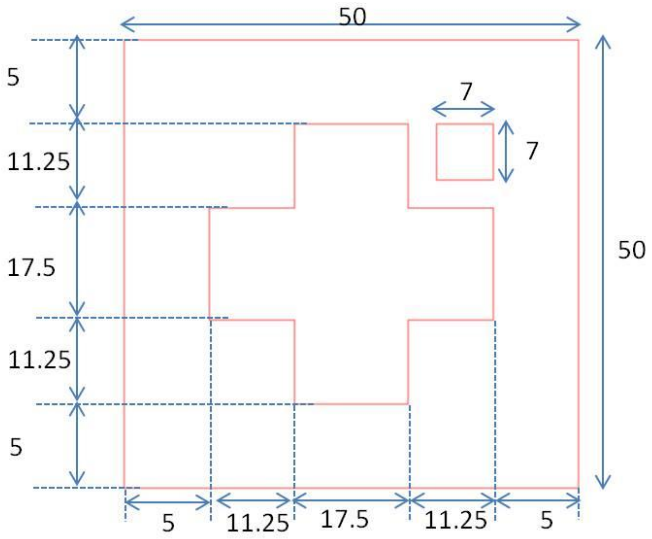
14.2.3 Alignment mark

Unit : um

Left Side



Right Side



14.3 Pad coordinates

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
1	GOUTL[1]	-13577.5	-386.5	32x43	81	DN[1]	-9967.5	-361.5	30x93
2	GOUTL[2]	-13532.5	-386.5	32x43	82	DN[1]	-9922.5	-361.5	30x93
3	GOUTL[3]	-13487.5	-386.5	32x43	83	DN[1]	-9877.5	-361.5	30x93
4	GOUTL[4]	-13442.5	-386.5	32x43	84	DP[1]	-9832.5	-361.5	30x93
5	GOUTL[5]	-13397.5	-386.5	32x43	85	DP[1]	-9787.5	-361.5	30x93
6	GOUTL[6]	-13352.5	-386.5	32x43	86	DP[1]	-9742.5	-361.5	30x93
7	GOUTL[7]	-13307.5	-386.5	32x43	87	DP[1]	-9697.5	-361.5	30x93
8	GOUTL[8]	-13262.5	-386.5	32x43	88	DP[1]	-9652.5	-361.5	30x93
9	GOUTL[9]	-13217.5	-386.5	32x43	89	DP[1]	-9607.5	-361.5	30x93
10	GOUTL[10]	-13172.5	-386.5	32x43	90	VSS_IF	-9562.5	-361.5	30x93
11	GOUTL[11]	-13127.5	-386.5	32x43	91	DN[0]	-9517.5	-361.5	30x93
12	GOUTL[12]	-13082.5	-386.5	32x43	92	DN[0]	-9472.5	-361.5	30x93
13	GOUTL[13]	-13037.5	-386.5	32x43	93	DN[0]	-9427.5	-361.5	30x93
14	GOUTL[14]	-12992.5	-386.5	32x43	94	DN[0]	-9382.5	-361.5	30x93
15	GOUTL[15]	-12947.5	-386.5	32x43	95	DN[0]	-9337.5	-361.5	30x93
16	GOUTL[16]	-12902.5	-386.5	32x43	96	DN[0]	-9292.5	-361.5	30x93
17	GOUTL[17]	-12857.5	-386.5	32x43	97	DP[0]	-9247.5	-361.5	30x93
18	GOUTL[18]	-12812.5	-386.5	32x43	98	DP[0]	-9202.5	-361.5	30x93
19	GOUTL[19]	-12767.5	-386.5	32x43	99	DP[0]	-9157.5	-361.5	30x93
20	GOUTL[20]	-12722.5	-386.5	32x43	100	DP[0]	-9112.5	-361.5	30x93
21	GOUTL[21]	-12677.5	-386.5	32x43	101	DP[0]	-9067.5	-361.5	30x93
22	GOUTL[22]	-12632.5	-386.5	32x43	102	DP[0]	-9022.5	-361.5	30x93
23	VCOM	-12587.5	-361.5	30x93	103	VSS_IF	-8977.5	-361.5	30x93
24	VCOM	-12542.5	-361.5	30x93	104	VSS_IF	-8932.5	-361.5	30x93
25	VCOM	-12497.5	-361.5	30x93	105	VSS_IF	-8887.5	-361.5	30x93
26	VSSA	-12442.5	-361.5	30x93	106	VSS_IF	-8842.5	-361.5	30x93
27	VSSA	-12397.5	-361.5	30x93	107	VSS_IF	-8797.5	-361.5	30x93
28	VSSA	-12352.5	-361.5	30x93	108	VSS_IF	-8752.5	-361.5	30x93
29	VSSA	-12307.5	-361.5	30x93	109	VSS_IF	-8707.5	-361.5	30x93
30	VSSA	-12262.5	-361.5	30x93	110	VSS_IF	-8662.5	-361.5	30x93
31	VSSA	-12217.5	-361.5	30x93	111	VSS_IF	-8617.5	-361.5	30x93
32	VSSA	-12172.5	-361.5	30x93	112	VSS_IF	-8572.5	-361.5	30x93
33	VSSA	-12127.5	-361.5	30x93	113	VSS_IF	-8527.5	-361.5	30x93
34	VSSA	-12082.5	-361.5	30x93	114	VSS_IF	-8482.5	-361.5	30x93
35	VSSA	-12037.5	-361.5	30x93	115	T_IRX	-8437.5	-361.5	30x93
36	VOTP	-11992.5	-361.5	30x93	116	T_IRX	-8392.5	-361.5	30x93
37	VOTP	-11947.5	-361.5	30x93	117	VDD_18V_IF	-8347.5	-361.5	30x93
38	VSS_IF	-11902.5	-361.5	30x93	118	VDD_18V_IF	-8302.5	-361.5	30x93
39	DN[3]	-11857.5	-361.5	30x93	119	VDD_18V_IF	-8257.5	-361.5	30x93
40	DN[3]	-11812.5	-361.5	30x93	120	VDD_18V_IF	-8212.5	-361.5	30x93
41	DN[3]	-11767.5	-361.5	30x93	121	VDD_18V_IF	-8167.5	-361.5	30x93
42	DN[3]	-11722.5	-361.5	30x93	122	VDD_18V_IF	-8122.5	-361.5	30x93
43	DN[3]	-11677.5	-361.5	30x93	123	VDD_18V_IF	-8077.5	-361.5	30x93
44	DN[3]	-11632.5	-361.5	30x93	124	VDD_18V_IF	-8032.5	-361.5	30x93
45	DP[3]	-11587.5	-361.5	30x93	125	VDD_18V_IF	-7987.5	-361.5	30x93
46	DP[3]	-11542.5	-361.5	30x93	126	VDD_18V_IF	-7942.5	-361.5	30x93
47	DP[3]	-11497.5	-361.5	30x93	127	VDDIO_IF	-7897.5	-361.5	30x93
48	DP[3]	-11452.5	-361.5	30x93	128	VDDIO_IF	-7852.5	-361.5	30x93
49	DP[3]	-11407.5	-361.5	30x93	129	VDDIO_IF	-7807.5	-361.5	30x93
50	DP[3]	-11362.5	-361.5	30x93	130	VDDIO_IF	-7762.5	-361.5	30x93
51	VSS_IF	-11317.5	-361.5	30x93	131	VDDIO_IF	-7717.5	-361.5	30x93
52	DN[2]	-11272.5	-361.5	30x93	132	VDDIO_IF	-7672.5	-361.5	30x93
53	DN[2]	-11227.5	-361.5	30x93	133	VDDIO_IF	-7627.5	-361.5	30x93
54	DN[2]	-11182.5	-361.5	30x93	134	VDDIO_IF	-7582.5	-361.5	30x93
55	DN[2]	-11137.5	-361.5	30x93	135	VDDIO_IF	-7537.5	-361.5	30x93
56	DN[2]	-11092.5	-361.5	30x93	136	VDDIO_IF	-7492.5	-361.5	30x93
57	DN[2]	-11047.5	-361.5	30x93	137	VDDIO_IF	-7447.5	-361.5	30x93
58	DP[2]	-11002.5	-361.5	30x93	138	VDDIO_IF	-7402.5	-361.5	30x93
59	DP[2]	-10957.5	-361.5	30x93	139	VDDIO	-7357.5	-361.5	30x93
60	DP[2]	-10912.5	-361.5	30x93	140	VDDIO	-7312.5	-361.5	30x93
61	DP[2]	-10867.5	-361.5	30x93	141	VDDIO	-7267.5	-361.5	30x93
62	DP[2]	-10822.5	-361.5	30x93	142	VDDIO	-7222.5	-361.5	30x93
63	DP[2]	-10777.5	-361.5	30x93	143	VDDIO	-7177.5	-361.5	30x93
64	VSS_IF	-10732.5	-361.5	30x93	144	VDDIO	-7132.5	-361.5	30x93
65	CKN	-10687.5	-361.5	30x93	145	VDDIO	-7087.5	-361.5	30x93
66	CKN	-10642.5	-361.5	30x93	146	VDDIO	-7042.5	-361.5	30x93
67	CKN	-10597.5	-361.5	30x93	147	VDDIO	-6997.5	-361.5	30x93
68	CKN	-10552.5	-361.5	30x93	148	VDDIO	-6952.5	-361.5	30x93
69	CKN	-10507.5	-361.5	30x93	149	VDDIO	-6907.5	-361.5	30x93
70	CKN	-10462.5	-361.5	30x93	150	VDDIO	-6862.5	-361.5	30x93
71	CKP	-10417.5	-361.5	30x93	151	VDDIO	-6817.5	-361.5	30x93
72	CKP	-10372.5	-361.5	30x93	152	VDDIO	-6772.5	-361.5	30x93
73	CKP	-10327.5	-361.5	30x93	153	VDDIO	-6727.5	-361.5	30x93
74	CKP	-10282.5	-361.5	30x93	154	VDD_18V	-6682.5	-361.5	30x93
75	CKP	-10237.5	-361.5	30x93	155	VDD_18V	-6637.5	-361.5	30x93
76	CKP	-10192.5	-361.5	30x93	156	VDD_18V	-6592.5	-361.5	30x93
77	VSS_IF	-10147.5	-361.5	30x93	157	VDD_18V	-6547.5	-361.5	30x93
78	DN[1]	-10102.5	-361.5	30x93	158	VDD_18V	-6502.5	-361.5	30x93
79	DN[1]	-10057.5	-361.5	30x93	159	VDD_18V	-6457.5	-361.5	30x93
80	DN[1]	-10012.5	-361.5	30x93	160	VDD_18V	-6412.5	-361.5	30x93

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
161	VSS	-6367.5	-361.5	30x93	241	TIN[1]	-2767.5	-361.5	30x93
162	VSS	-6322.5	-361.5	30x93	242	TIN[2]	-2722.5	-361.5	30x93
163	VSS	-6277.5	-361.5	30x93	243	TIN[3]	-2677.5	-361.5	30x93
164	VSS	-6232.5	-361.5	30x93	244	TIN[4]	-2632.5	-361.5	30x93
165	VSS	-6187.5	-361.5	30x93	245	TIN[5]	-2587.5	-361.5	30x93
166	VSS	-6142.5	-361.5	30x93	246	TIN[6]	-2542.5	-361.5	30x93
167	VSS	-6097.5	-361.5	30x93	247	TIN[7]	-2497.5	-361.5	30x93
168	VSS	-6052.5	-361.5	30x93	248	TIN[8]	-2452.5	-361.5	30x93
169	VSS	-6007.5	-361.5	30x93	249	TIN[9]	-2407.5	-361.5	30x93
170	VSS	-5962.5	-361.5	30x93	250	TIN[10]	-2362.5	-361.5	30x93
171	VSS	-5917.5	-361.5	30x93	251	TIN[11]	-2317.5	-361.5	30x93
172	VSS	-5872.5	-361.5	30x93	252	TIN[12]	-2272.5	-361.5	30x93
173	VSS	-5827.5	-361.5	30x93	253	TIN[13]	-2227.5	-361.5	30x93
174	VSS	-5782.5	-361.5	30x93	254	TIN[14]	-2182.5	-361.5	30x93
175	VSS	-5737.5	-361.5	30x93	255	TIN[15]	-2137.5	-361.5	30x93
176	VSS	-5692.5	-361.5	30x93	256	TIN[16]	-2092.5	-361.5	30x93
177	VSSA	-5647.5	-361.5	30x93	257	TIN[17]	-2047.5	-361.5	30x93
178	VSSA	-5602.5	-361.5	30x93	258	TIN[18]	-2002.5	-361.5	30x93
179	VSSA	-5557.5	-361.5	30x93	259	TIN[19]	-1957.5	-361.5	30x93
180	VSSA	-5512.5	-361.5	30x93	260	TIN[19]	-1912.5	-361.5	30x93
181	VSSA	-5467.5	-361.5	30x93	261	T_SCL_DUM	-1867.5	-361.5	30x93
182	VSSA	-5422.5	-361.5	30x93	262	T_SCL_DUM	-1822.5	-361.5	30x93
183	VSSA	-5377.5	-361.5	30x93	263	T_SDA_DUM	-1777.5	-361.5	30x93
184	T_VREF	-5332.5	-361.5	30x93	264	T_SDA_DUM	-1732.5	-361.5	30x93
185	T_IBIAS	-5287.5	-361.5	30x93	265	CMD_SEL	-1687.5	-361.5	30x93
186	VDD	-5242.5	-361.5	30x93	266	CMD_SEL	-1642.5	-361.5	30x93
187	VDD	-5197.5	-361.5	30x93	267	RES[1]	-1597.5	-361.5	30x93
188	VDD	-5152.5	-361.5	30x93	268	RES[1]	-1552.5	-361.5	30x93
189	VDD	-5107.5	-361.5	30x93	269	TEST_IO[0]	-1507.5	-361.5	30x93
190	VDD	-5062.5	-361.5	30x93	270	TEST_IO[0]	-1462.5	-361.5	30x93
191	VSP	-5017.5	-361.5	30x93	271	TEST_IO[1]	-1417.5	-361.5	30x93
192	VSP	-4972.5	-361.5	30x93	272	TEST_IO[1]	-1372.5	-361.5	30x93
193	VSP	-4927.5	-361.5	30x93	273	TEST_IO[2]	-1327.5	-361.5	30x93
194	VSN	-4882.5	-361.5	30x93	274	TEST_IO[2]	-1282.5	-361.5	30x93
195	VSN	-4837.5	-361.5	30x93	275	TEST_IO[2]	-1237.5	-361.5	30x93
196	VSN	-4792.5	-361.5	30x93	276	TEST_IO[2]	-1192.5	-361.5	30x93
197	VSN	-4747.5	-361.5	30x93	277	TIN_DUM[0]	-1147.5	-361.5	30x93
198	VSN	-4702.5	-361.5	30x93	278	TIN_DUM[1]	-1102.5	-361.5	30x93
199	VSN	-4657.5	-361.5	30x93	279	TIN_DUM[2]	-1057.5	-361.5	30x93
200	VSN	-4612.5	-361.5	30x93	280	TIN_DUM[3]	-1012.5	-361.5	30x93
201	VSN	-4567.5	-361.5	30x93	281	TIN_DUM[4]	-967.5	-361.5	30x93
202	TOUT[0]	-4522.5	-361.5	30x93	282	TIN_DUM[5]	-922.5	-361.5	30x93
203	TOUT[1]	-4477.5	-361.5	30x93	283	TIN_DUM[6]	-877.5	-361.5	30x93
204	TOUT[1]	-4432.5	-361.5	30x93	284	TIN_DUM[7]	-832.5	-361.5	30x93
205	TOUT[2]	-4387.5	-361.5	30x93	285	TIN_DUM[8]	-787.5	-361.5	30x93
206	TOUT[3]	-4342.5	-361.5	30x93	286	TIN_DUM[9]	-742.5	-361.5	30x93
207	TOUT[3]	-4297.5	-361.5	30x93	287	TIN_DUM[10]	-697.5	-361.5	30x93
208	TOUT[4]	-4252.5	-361.5	30x93	288	T_OTP_RLOAD	-652.5	-361.5	30x93
209	TOUT[5]	-4207.5	-361.5	30x93	289	RESETB	-607.5	-361.5	30x93
210	TOUT[5]	-4162.5	-361.5	30x93	290	RESETB	-562.5	-361.5	30x93
211	TOUT[6]	-4117.5	-361.5	30x93	291	RESETB	-517.5	-361.5	30x93
212	TOUT[7]	-4072.5	-361.5	30x93	292	RESETB	-472.5	-361.5	30x93
213	TOUT[7]	-4027.5	-361.5	30x93	293	ERR_FG	-427.5	-361.5	30x93
214	TOUT[8]	-3982.5	-361.5	30x93	294	ERR_FG	-382.5	-361.5	30x93
215	TOUT[9]	-3937.5	-361.5	30x93	295	LEDON	-337.5	-361.5	30x93
216	TOUT[9]	-3892.5	-361.5	30x93	296	LEDON	-292.5	-361.5	30x93
217	TOUT[10]	-3847.5	-361.5	30x93	297	LEDON	-247.5	-361.5	30x93
218	TOUT[11]	-3802.5	-361.5	30x93	298	LEDON	-202.5	-361.5	30x93
219	TOUT[11]	-3757.5	-361.5	30x93	299	LEDON	-157.5	-361.5	30x93
220	TOUT[12]	-3712.5	-361.5	30x93	300	LEDON	-112.5	-361.5	30x93
221	TOUT[13]	-3667.5	-361.5	30x93	301	LEDPWM	-67.5	-361.5	30x93
222	TOUT[13]	-3622.5	-361.5	30x93	302	LEDPWM	-22.5	-361.5	30x93
223	TOUT[14]	-3577.5	-361.5	30x93	303	PMODE[1]	22.5	-361.5	30x93
224	TOUT[15]	-3532.5	-361.5	30x93	304	PMODE[1]	67.5	-361.5	30x93
225	TOUT[15]	-3487.5	-361.5	30x93	305	PMODE[0]	112.5	-361.5	30x93
226	T_CSB_DUM	-3442.5	-361.5	30x93	306	PMODE[0]	157.5	-361.5	30x93
227	LVFMT	-3397.5	-361.5	30x93	307	LNSW[1]	202.5	-361.5	30x93
228	LVFMT	-3352.5	-361.5	30x93	308	LNSW[1]	247.5	-361.5	30x93
229	LVFMT	-3307.5	-361.5	30x93	309	LNSW[0]	292.5	-361.5	30x93
230	LVFMT	-3262.5	-361.5	30x93	310	LNSW[0]	337.5	-361.5	30x93
231	LVFMT	-3217.5	-361.5	30x93	311	PNSW	382.5	-361.5	30x93
232	LVFMT	-3172.5	-361.5	30x93	312	PNSW	427.5	-361.5	30x93
233	LVBIT	-3127.5	-361.5	30x93	313	RES[2]	472.5	-361.5	30x93
234	LVBIT	-3082.5	-361.5	30x93	314	RES[2]	517.5	-361.5	30x93
235	LVBIT	-3037.5	-361.5	30x93	315	RES[0]	562.5	-361.5	30x93
236	LVBIT	-2992.5	-361.5	30x93	316	RES[0]	607.5	-361.5	30x93
237	LVBIT	-2947.5	-361.5	30x93	317	LANE1_STBYB	652.5	-361.5	30x93
238	LVBIT	-2902.5	-361.5	30x93	318	LANE1_STBYB	697.5	-361.5	30x93
239	TEST_EN	-2857.5	-361.5	30x93	319	LANE0_BISTB	742.5	-361.5	30x93
240	TIN[0]	-2812.5	-361.5	30x93	320	LANE0_BISTB	787.5	-361.5	30x93

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
321	IFSEL	832.5	-361.5	30x93	401	VDDP	4432.5	-361.5	30x93
322	IFSEL	877.5	-361.5	30x93	402	VDDP	4477.5	-361.5	30x93
323	CSB	922.5	-361.5	30x93	403	VDDP	4522.5	-361.5	30x93
324	CSB	967.5	-361.5	30x93	404	VDDP	4567.5	-361.5	30x93
325	TP_SYNC	1012.5	-361.5	30x93	405	VGMP	4612.5	-361.5	30x93
326	TP_SYNC	1057.5	-361.5	30x93	406	VGMP	4657.5	-361.5	30x93
327	VSS	1102.5	-361.5	30x93	407	VGMP	4702.5	-361.5	30x93
328	VSS	1147.5	-361.5	30x93	408	VGMN	4747.5	-361.5	30x93
329	VSS	1192.5	-361.5	30x93	409	VGMN	4792.5	-361.5	30x93
330	VSS	1237.5	-361.5	30x93	410	VGMN	4837.5	-361.5	30x93
331	VSS	1282.5	-361.5	30x93	411	VGH_REG	4882.5	-361.5	30x93
332	VSS	1327.5	-361.5	30x93	412	VGH_REG	4927.5	-361.5	30x93
333	VSS	1372.5	-361.5	30x93	413	VGH_REG	4972.5	-361.5	30x93
334	VSS	1417.5	-361.5	30x93	414	VCOM	5017.5	-361.5	30x93
335	VSS	1462.5	-361.5	30x93	415	VCOM	5062.5	-361.5	30x93
336	VSS	1507.5	-361.5	30x93	416	VCOM	5107.5	-361.5	30x93
337	VSS	1552.5	-361.5	30x93	417	VCOM	5152.5	-361.5	30x93
338	VSS	1597.5	-361.5	30x93	418	VCOM	5197.5	-361.5	30x93
339	VSS	1642.5	-361.5	30x93	419	VDD_18V	5242.5	-361.5	30x93
340	VSS	1687.5	-361.5	30x93	420	VDD_18V	5287.5	-361.5	30x93
341	VSS	1732.5	-361.5	30x93	421	VDD_18V	5332.5	-361.5	30x93
342	VSS	1777.5	-361.5	30x93	422	VDD_18V	5377.5	-361.5	30x93
343	VSS	1822.5	-361.5	30x93	423	VDD_18V	5422.5	-361.5	30x93
344	VSS	1867.5	-361.5	30x93	424	VDD_18V	5467.5	-361.5	30x93
345	VSS	1912.5	-361.5	30x93	425	VDD_18V	5512.5	-361.5	30x93
346	VSS	1957.5	-361.5	30x93	426	VDD_18V	5557.5	-361.5	30x93
347	VSSA	2002.5	-361.5	30x93	427	VCI1	5602.5	-361.5	30x93
348	VSSA	2047.5	-361.5	30x93	428	VCI1	5647.5	-361.5	30x93
349	VSSA	2092.5	-361.5	30x93	429	VCI1	5692.5	-361.5	30x93
350	VSSA	2137.5	-361.5	30x93	430	VCI1	5737.5	-361.5	30x93
351	VSSA	2182.5	-361.5	30x93	431	VCI1	5782.5	-361.5	30x93
352	VSSA	2227.5	-361.5	30x93	432	VSSP	5827.5	-361.5	30x93
353	VSSA	2272.5	-361.5	30x93	433	VSSP	5872.5	-361.5	30x93
354	VSSA	2317.5	-361.5	30x93	434	VSSP	5917.5	-361.5	30x93
355	VSSA	2362.5	-361.5	30x93	435	VSSP	5962.5	-361.5	30x93
356	VSSA	2407.5	-361.5	30x93	436	VSSP	6007.5	-361.5	30x93
357	VCSW1	2452.5	-361.5	30x93	437	VSSP	6052.5	-361.5	30x93
358	VCSW1	2497.5	-361.5	30x93	438	VSSP	6097.5	-361.5	30x93
359	VCSW1	2542.5	-361.5	30x93	439	VSSP	6142.5	-361.5	30x93
360	VCSW1	2587.5	-361.5	30x93	440	VSSP	6187.5	-361.5	30x93
361	VCSW1	2632.5	-361.5	30x93	441	VSSP	6232.5	-361.5	30x93
362	VCSW1	2677.5	-361.5	30x93	442	VSSP	6277.5	-361.5	30x93
363	VCSW1	2722.5	-361.5	30x93	443	VSSP	6322.5	-361.5	30x93
364	VCSW1	2767.5	-361.5	30x93	444	VSSP	6367.5	-361.5	30x93
365	VCSW2	2812.5	-361.5	30x93	445	VSSP	6412.5	-361.5	30x93
366	VCSW2	2857.5	-361.5	30x93	446	VCL	6457.5	-361.5	30x93
367	VCSW2	2902.5	-361.5	30x93	447	VCL	6502.5	-361.5	30x93
368	VCSW2	2947.5	-361.5	30x93	448	VCL	6547.5	-361.5	30x93
369	VCSW2	2992.5	-361.5	30x93	449	VCL	6592.5	-361.5	30x93
370	VCSW2	3037.5	-361.5	30x93	450	VCL	6637.5	-361.5	30x93
371	VCSW2	3082.5	-361.5	30x93	451	VCL	6682.5	-361.5	30x93
372	VCSW2	3127.5	-361.5	30x93	452	VCL	6727.5	-361.5	30x93
373	VDD_18V	3172.5	-361.5	30x93	453	SCL_I2C	6772.5	-361.5	30x93
374	VDD_18V	3217.5	-361.5	30x93	454	SCL_I2C	6817.5	-361.5	30x93
375	VDD_18V	3262.5	-361.5	30x93	455	SCL_I2C	6862.5	-361.5	30x93
376	VDD_18V	3307.5	-361.5	30x93	456	SDA_I2C	6907.5	-361.5	30x93
377	VDD_18V	3352.5	-361.5	30x93	457	SDA_I2C	6952.5	-361.5	30x93
378	VDD_18V	3397.5	-361.5	30x93	458	SDA_I2C	6997.5	-361.5	30x93
379	VGL_REG	3442.5	-361.5	30x93	459	SDA_I2C	7042.5	-361.5	30x93
380	VGL_REG	3487.5	-361.5	30x93	460	SDA	7087.5	-361.5	30x93
381	VGL_REG	3532.5	-361.5	30x93	461	SDA	7132.5	-361.5	30x93
382	VGL_REG	3577.5	-361.5	30x93	462	SDA	7177.5	-361.5	30x93
383	VGL_REG	3622.5	-361.5	30x93	463	SCL	7222.5	-361.5	30x93
384	VGL_REG	3667.5	-361.5	30x93	464	SCL	7267.5	-361.5	30x93
385	VGL_REG	3712.5	-361.5	30x93	465	SCL	7312.5	-361.5	30x93
386	VSS	3757.5	-361.5	30x93	466	SCL	7357.5	-361.5	30x93
387	VSS	3802.5	-361.5	30x93	467	VSN	7402.5	-361.5	30x93
388	VSS	3847.5	-361.5	30x93	468	VSN	7447.5	-361.5	30x93
389	VSS	3892.5	-361.5	30x93	469	VSN	7492.5	-361.5	30x93
390	VSS	3937.5	-361.5	30x93	470	VSN	7537.5	-361.5	30x93
391	VSSA	3982.5	-361.5	30x93	471	VSN	7582.5	-361.5	30x93
392	VSSA	4027.5	-361.5	30x93	472	VSN	7627.5	-361.5	30x93
393	VSSA	4072.5	-361.5	30x93	473	VSN	7672.5	-361.5	30x93
394	VDD	4117.5	-361.5	30x93	474	VSP	7717.5	-361.5	30x93
395	VDD	4162.5	-361.5	30x93	475	VSP	7762.5	-361.5	30x93
396	VDD	4207.5	-361.5	30x93	476	VSP	7807.5	-361.5	30x93
397	VDD	4252.5	-361.5	30x93	477	VSP	7852.5	-361.5	30x93
398	VDDP	4297.5	-361.5	30x93	478	VSP	7897.5	-361.5	30x93
399	VDDP	4342.5	-361.5	30x93	479	VSP	7942.5	-361.5	30x93
400	VDDP	4387.5	-361.5	30x93	480	VSP	7987.5	-361.5	30x93

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
481	VSP	8032.5	-361.5	30x93	561	VGL	11632.5	-361.5	30x93
482	VSP	8077.5	-361.5	30x93	562	VGL	11677.5	-361.5	30x93
483	VSP	8122.5	-361.5	30x93	563	C51P	11722.5	-361.5	30x93
484	VSP	8167.5	-361.5	30x93	564	C51P	11767.5	-361.5	30x93
485	VSP	8212.5	-361.5	30x93	565	C51P	11812.5	-361.5	30x93
486	VSP	8257.5	-361.5	30x93	566	C51P	11857.5	-361.5	30x93
487	VSP	8302.5	-361.5	30x93	567	C51P	11902.5	-361.5	30x93
488	T_VDDN15	8347.5	-361.5	30x93	568	C51P	11947.5	-361.5	30x93
489	T_VDDN15	8392.5	-361.5	30x93	569	C51P	11992.5	-361.5	30x93
490	T_VDDN15	8437.5	-361.5	30x93	570	C51N	12037.5	-361.5	30x93
491	T_VDDN15	8482.5	-361.5	30x93	571	C51N	12082.5	-361.5	30x93
492	T_VDDN3	8527.5	-361.5	30x93	572	C51N	12127.5	-361.5	30x93
493	T_VDDN3	8572.5	-361.5	30x93	573	C51N	12172.5	-361.5	30x93
494	T_VDDN3	8617.5	-361.5	30x93	574	C51N	12217.5	-361.5	30x93
495	T_EXT_VCOMI	8662.5	-361.5	30x93	575	C51N	12262.5	-361.5	30x93
496	T_EXT_VCOMI	8707.5	-361.5	30x93	576	VSSA	12307.5	-361.5	30x93
497	T_EXT_VCOMI	8752.5	-361.5	30x93	577	VSSA	12352.5	-361.5	30x93
498	T_EXT_VCOMI	8797.5	-361.5	30x93	578	VSSA	12397.5	-361.5	30x93
499	C13P_DUM	8842.5	-361.5	30x93	579	VSSA	12442.5	-361.5	30x93
500	C13P_DUM	8887.5	-361.5	30x93	580	VCOM	12497.5	-361.5	30x93
501	C13P_DUM	8932.5	-361.5	30x93	581	VCOM	12542.5	-361.5	30x93
502	C12N_DUM	8977.5	-361.5	30x93	582	VCOM	12587.5	-361.5	30x93
503	C12N_DUM	9022.5	-361.5	30x93	583	GOUTR[22]	12632.5	-386.5	32x43
504	C12N_DUM	9067.5	-361.5	30x93	584	GOUTR[21]	12677.5	-386.5	32x43
505	C12P_DUM	9112.5	-361.5	30x93	585	GOUTR[20]	12722.5	-386.5	32x43
506	C12P_DUM	9157.5	-361.5	30x93	586	GOUTR[19]	12767.5	-386.5	32x43
507	C12P_DUM	9202.5	-361.5	30x93	587	GOUTR[18]	12812.5	-386.5	32x43
508	C11N_VGL	9247.5	-361.5	30x93	588	GOUTR[17]	12857.5	-386.5	32x43
509	C11N_VGL	9292.5	-361.5	30x93	589	GOUTR[16]	12902.5	-386.5	32x43
510	C11N_VGL	9337.5	-361.5	30x93	590	GOUTR[15]	12947.5	-386.5	32x43
511	C11P_VGL	9382.5	-361.5	30x93	591	GOUTR[14]	12992.5	-386.5	32x43
512	C11P_VGL	9427.5	-361.5	30x93	592	GOUTR[13]	13037.5	-386.5	32x43
513	C11P_VGL	9472.5	-361.5	30x93	593	GOUTR[12]	13082.5	-386.5	32x43
514	VDDP	9517.5	-361.5	30x93	594	GOUTR[11]	13127.5	-386.5	32x43
515	VDDP	9562.5	-361.5	30x93	595	GOUTR[10]	13172.5	-386.5	32x43
516	VDDP	9607.5	-361.5	30x93	596	GOUTR[9]	13217.5	-386.5	32x43
517	VDDP	9652.5	-361.5	30x93	597	GOUTR[8]	13262.5	-386.5	32x43
518	VDDP	9697.5	-361.5	30x93	598	GOUTR[7]	13307.5	-386.5	32x43
519	VDDP	9742.5	-361.5	30x93	599	GOUTR[6]	13352.5	-386.5	32x43
520	VDDP	9787.5	-361.5	30x93	600	GOUTR[5]	13397.5	-386.5	32x43
521	VDDP	9832.5	-361.5	30x93	601	GOUTR[4]	13442.5	-386.5	32x43
522	VSSA	9877.5	-361.5	30x93	602	GOUTR[3]	13487.5	-386.5	32x43
523	VSSA	9922.5	-361.5	30x93	603	GOUTR[2]	13532.5	-386.5	32x43
524	VSSA	9967.5	-361.5	30x93	604	GOUTR[1]	13577.5	-386.5	32x43
525	VSSA	10012.5	-361.5	30x93	605	DUMMY[73]	13623.5	190.5	16x73
526	VSSA	10057.5	-361.5	30x93	606	DUMMY[72]	13612.5	280.5	16x73
527	VSSA	10102.5	-361.5	30x93	607	DUMMY[71]	13601.5	370.5	16x73
528	VSSA	10147.5	-361.5	30x93	608	DUMMY[70]	13590.5	190.5	16x73
529	VSSP	10192.5	-361.5	30x93	609	DUMMY[69]	13579.5	280.5	16x73
530	VSSP	10237.5	-361.5	30x93	610	DUMMY[68]	13568.5	370.5	16x73
531	VSSP	10282.5	-361.5	30x93	611	DUMMY[67]	13557.5	190.5	16x73
532	VSSP	10327.5	-361.5	30x93	612	SDUMY[3]	13546.5	280.5	16x73
533	VSSP	10372.5	-361.5	30x93	613	SDUMY[2]	13535.5	370.5	16x73
534	VSSP	10417.5	-361.5	30x93	614	S[2400]	13524.5	190.5	16x73
535	VSSP	10462.5	-361.5	30x93	615	S[2399]	13513.5	280.5	16x73
536	VGH	10507.5	-361.5	30x93	616	S[2398]	13502.5	370.5	16x73
537	VGH	10552.5	-361.5	30x93	617	S[2397]	13491.5	190.5	16x73
538	VGH	10597.5	-361.5	30x93	618	S[2396]	13480.5	280.5	16x73
539	VGH	10642.5	-361.5	30x93	619	S[2395]	13469.5	370.5	16x73
540	VGH	10687.5	-361.5	30x93	620	S[2394]	13458.5	190.5	16x73
541	VGH	10732.5	-361.5	30x93	621	S[2393]	13447.5	280.5	16x73
542	VGH	10777.5	-361.5	30x93	622	S[2392]	13436.5	370.5	16x73
543	C42N	10822.5	-361.5	30x93	623	S[2391]	13425.5	190.5	16x73
544	C42N	10867.5	-361.5	30x93	624	S[2390]	13414.5	280.5	16x73
545	C42N	10912.5	-361.5	30x93	625	S[2389]	13403.5	370.5	16x73
546	C42P	10957.5	-361.5	30x93	626	S[2388]	13392.5	190.5	16x73
547	C42P	11002.5	-361.5	30x93	627	S[2387]	13381.5	280.5	16x73
548	C42P	11047.5	-361.5	30x93	628	S[2386]	13370.5	370.5	16x73
549	C42P	11092.5	-361.5	30x93	629	S[2385]	13359.5	190.5	16x73
550	C41N	11137.5	-361.5	30x93	630	S[2384]	13348.5	280.5	16x73
551	C41N	11182.5	-361.5	30x93	631	S[2383]	13337.5	370.5	16x73
552	C41N	11227.5	-361.5	30x93	632	S[2382]	13326.5	190.5	16x73
553	C41P	11272.5	-361.5	30x93	633	S[2381]	13315.5	280.5	16x73
554	C41P	11317.5	-361.5	30x93	634	S[2380]	13304.5	370.5	16x73
555	C41P	11362.5	-361.5	30x93	635	S[2379]	13293.5	190.5	16x73
556	VGL	11407.5	-361.5	30x93	636	S[2378]	13282.5	280.5	16x73
557	VGL	11452.5	-361.5	30x93	637	S[2377]	13271.5	370.5	16x73
558	VGL	11497.5	-361.5	30x93	638	S[2376]	13260.5	190.5	16x73
559	VGL	11542.5	-361.5	30x93	639	S[2375]	13249.5	280.5	16x73
560	VGL	11587.5	-361.5	30x93	640	S[2374]	13238.5	370.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
641	S[2373]	13227.5	190.5	16x73	721	S[2293]	12347.5	368.5	16x73
642	S[2372]	13216.5	280.5	16x73	722	S[2292]	12336.5	190.5	16x73
643	S[2371]	13205.5	370.5	16x73	723	S[2291]	12325.5	280.5	16x73
644	S[2370]	13194.5	190.5	16x73	724	S[2290]	12314.5	370.5	16x73
645	S[2369]	13183.5	280.5	16x73	725	S[2289]	12303.5	190.5	16x73
646	S[2368]	13172.5	370.5	16x73	726	S[2288]	12292.5	280.5	16x73
647	S[2367]	13161.5	190.5	16x73	727	S[2287]	12281.5	370.5	16x73
648	S[2366]	13150.5	280.5	16x73	728	S[2286]	12270.5	190.5	16x73
649	S[2365]	13139.5	370.5	16x73	729	S[2285]	12259.5	280.5	16x73
650	S[2364]	13128.5	190.5	16x73	730	S[2284]	12248.5	370.5	16x73
651	S[2363]	13117.5	280.5	16x73	731	S[2283]	12237.5	190.5	16x73
652	S[2362]	13106.5	370.5	16x73	732	S[2282]	12226.5	280.5	16x73
653	S[2361]	13095.5	190.5	16x73	733	S[2281]	12215.5	370.5	16x73
654	S[2360]	13084.5	280.5	16x73	734	S[2280]	12204.5	190.5	16x73
655	S[2359]	13073.5	370.5	16x73	735	S[2279]	12193.5	280.5	16x73
656	S[2358]	13062.5	190.5	16x73	736	S[2278]	12182.5	370.5	16x73
657	S[2357]	13051.5	280.5	16x73	737	S[2277]	12171.5	190.5	16x73
658	S[2356]	13040.5	370.5	16x73	738	S[2276]	12160.5	280.5	16x73
659	S[2355]	13029.5	190.5	16x73	739	S[2275]	12149.5	370.5	16x73
660	S[2354]	13018.5	280.5	16x73	740	S[2274]	12138.5	190.5	16x73
661	S[2353]	13007.5	370.5	16x73	741	S[2273]	12127.5	280.5	16x73
662	S[2352]	12996.5	190.5	16x73	742	S[2272]	12116.5	370.5	16x73
663	S[2351]	12985.5	280.5	16x73	743	S[2271]	12105.5	190.5	16x73
664	S[2350]	12974.5	370.5	16x73	744	S[2270]	12094.5	280.5	16x73
665	S[2349]	12963.5	190.5	16x73	745	S[2269]	12083.5	370.5	16x73
666	S[2348]	12952.5	280.5	16x73	746	S[2268]	12072.5	190.5	16x73
667	S[2347]	12941.5	370.5	16x73	747	S[2267]	12061.5	280.5	16x73
668	S[2346]	12930.5	190.5	16x73	748	S[2266]	12050.5	370.5	16x73
669	S[2345]	12919.5	280.5	16x73	749	S[2265]	12039.5	190.5	16x73
670	S[2344]	12908.5	370.5	16x73	750	S[2264]	12028.5	280.5	16x73
671	S[2343]	12897.5	190.5	16x73	751	S[2263]	12017.5	370.5	16x73
672	S[2342]	12886.5	280.5	16x73	752	S[2262]	12006.5	190.5	16x73
673	S[2341]	12875.5	370.5	16x73	753	S[2261]	11995.5	280.5	16x73
674	S[2340]	12864.5	190.5	16x73	754	S[2260]	11984.5	370.5	16x73
675	S[2339]	12853.5	280.5	16x73	755	S[2259]	11973.5	190.5	16x73
676	S[2338]	12842.5	370.5	16x73	756	S[2258]	11962.5	280.5	16x73
677	S[2337]	12831.5	190.5	16x73	757	S[2257]	11951.5	370.5	16x73
678	S[2336]	12820.5	280.5	16x73	758	S[2256]	11940.5	190.5	16x73
679	S[2335]	12809.5	370.5	16x73	759	S[2255]	11929.5	280.5	16x73
680	S[2334]	12798.5	190.5	16x73	760	S[2254]	11918.5	370.5	16x73
681	S[2333]	12787.5	280.5	16x73	761	S[2253]	11907.5	190.5	16x73
682	S[2332]	12776.5	370.5	16x73	762	S[2252]	11896.5	280.5	16x73
683	S[2331]	12765.5	190.5	16x73	763	S[2251]	11885.5	370.5	16x73
684	S[2330]	12754.5	280.5	16x73	764	S[2250]	11874.5	190.5	16x73
685	S[2329]	12743.5	370.5	16x73	765	S[2249]	11863.5	280.5	16x73
686	S[2328]	12732.5	190.5	16x73	766	S[2248]	11852.5	370.5	16x73
687	S[2327]	12721.5	280.5	16x73	767	S[2247]	11841.5	190.5	16x73
688	S[2326]	12710.5	370.5	16x73	768	S[2246]	11830.5	280.5	16x73
689	S[2325]	12699.5	190.5	16x73	769	S[2245]	11819.5	370.5	16x73
690	S[2324]	12688.5	280.5	16x73	770	S[2244]	11808.5	190.5	16x73
691	S[2323]	12677.5	370.5	16x73	771	S[2243]	11797.5	280.5	16x73
692	S[2322]	12666.5	190.5	16x73	772	S[2242]	11786.5	370.5	16x73
693	S[2321]	12655.5	280.5	16x73	773	S[2241]	11775.5	190.5	16x73
694	S[2320]	12644.5	370.5	16x73	774	S[2240]	11764.5	280.5	16x73
695	S[2319]	12633.5	190.5	16x73	775	S[2239]	11753.5	370.5	16x73
696	S[2318]	12622.5	280.5	16x73	776	S[2238]	11742.5	190.5	16x73
697	S[2317]	12611.5	370.5	16x73	777	S[2237]	11731.5	280.5	16x73
698	S[2316]	12600.5	190.5	16x73	778	S[2236]	11720.5	370.5	16x73
699	S[2315]	12589.5	280.5	16x73	779	S[2235]	11709.5	190.5	16x73
700	S[2314]	12578.5	370.5	16x73	780	S[2234]	11698.5	280.5	16x73
701	S[2313]	12567.5	190.5	16x73	781	S[2233]	11687.5	370.5	16x73
702	S[2312]	12556.5	280.5	16x73	782	S[2232]	11676.5	190.5	16x73
703	S[2311]	12545.5	370.5	16x73	783	S[2231]	11665.5	280.5	16x73
704	S[2310]	12534.5	190.5	16x73	784	S[2230]	11654.5	370.5	16x73
705	S[2309]	12523.5	280.5	16x73	785	S[2229]	11643.5	190.5	16x73
706	S[2308]	12512.5	370.5	16x73	786	S[2228]	11632.5	280.5	16x73
707	S[2307]	12501.5	190.5	16x73	787	S[2227]	11621.5	370.5	16x73
708	S[2306]	12490.5	280.5	16x73	788	S[2226]	11610.5	190.5	16x73
709	S[2305]	12479.5	370.5	16x73	789	S[2225]	11599.5	280.5	16x73
710	S[2304]	12468.5	190.5	16x73	790	S[2224]	11588.5	370.5	16x73
711	S[2303]	12457.5	280.5	16x73	791	S[2223]	11577.5	190.5	16x73
712	S[2302]	12446.5	370.5	16x73	792	S[2222]	11566.5	280.5	16x73
713	S[2301]	12435.5	190.5	16x73	793	S[2221]	11555.5	370.5	16x73
714	S[2300]	12424.5	280.5	16x73	794	S[2220]	11544.5	190.5	16x73
715	S[2299]	12413.5	370.5	16x73	795	S[2219]	11533.5	280.5	16x73
716	S[2298]	12402.5	190.5	16x73	796	S[2218]	11522.5	370.5	16x73
717	S[2297]	12391.5	280.5	16x73	797	S[2217]	11511.5	190.5	16x73
718	S[2296]	12380.5	370.5	16x73	798	S[2216]	11500.5	280.5	16x73
719	S[2295]	12369.5	190.5	16x73	799	S[2215]	11489.5	370.5	16x73
720	S[2294]	12358.5	280.5	16x73	800	S[2214]	11478.5	190.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
801	S[2213]	11467.5	280.5	16x73	881	S[2133]	10587.5	190.5	16x73
802	S[2212]	11456.5	370.5	16x73	882	S[2132]	10576.5	280.5	16x73
803	S[2211]	11445.5	190.5	16x73	883	S[2131]	10565.5	370.5	16x73
804	S[2210]	11434.5	280.5	16x73	884	S[2130]	10554.5	190.5	16x73
805	S[2209]	11423.5	370.5	16x73	885	S[2129]	10543.5	280.5	16x73
806	S[2208]	11412.5	190.5	16x73	886	S[2128]	10532.5	370.5	16x73
807	S[2207]	11401.5	280.5	16x73	887	S[2127]	10521.5	190.5	16x73
808	S[2206]	11390.5	370.5	16x73	888	S[2126]	10510.5	280.5	16x73
809	S[2205]	11379.5	190.5	16x73	889	S[2125]	10499.5	370.5	16x73
810	S[2204]	11370.5	280.5	16x73	890	S[2124]	10488.5	190.5	16x73
811	S[2203]	11357.5	370.5	16x73	891	S[2123]	10477.5	280.5	16x73
812	S[2202]	11346.5	190.5	16x73	892	S[2122]	10466.5	370.5	16x73
813	S[2201]	11335.5	280.5	16x73	893	S[2121]	10455.5	190.5	16x73
814	S[2200]	11324.5	370.5	16x73	894	S[2120]	10444.5	280.5	16x73
815	S[2199]	11313.5	190.5	16x73	895	S[2119]	10433.5	370.5	16x73
816	S[2198]	11302.5	280.5	16x73	896	S[2118]	10422.5	190.5	16x73
817	S[2197]	11291.5	370.5	16x73	897	S[2117]	10411.5	280.5	16x73
818	S[2196]	11280.5	190.5	16x73	898	S[2116]	10400.5	370.5	16x73
819	S[2195]	11269.5	280.5	16x73	899	S[2115]	10389.5	190.5	16x73
820	S[2194]	11258.5	370.5	16x73	900	S[2114]	10378.5	280.5	16x73
821	S[2193]	11247.5	190.5	16x73	901	S[2113]	10367.5	370.5	16x73
822	S[2192]	11236.5	280.5	16x73	902	S[2112]	10356.5	190.5	16x73
823	S[2191]	11225.5	370.5	16x73	903	S[2111]	10345.5	280.5	16x73
824	S[2190]	11214.5	190.5	16x73	904	S[2110]	10334.5	370.5	16x73
825	S[2189]	11203.5	280.5	16x73	905	S[2109]	10323.5	190.5	16x73
826	S[2188]	11192.5	370.5	16x73	906	S[2108]	10312.5	280.5	16x73
827	S[2187]	11181.5	190.5	16x73	907	S[2107]	10301.5	370.5	16x73
828	S[2186]	11170.5	280.5	16x73	908	S[2106]	10290.5	190.5	16x73
829	S[2185]	11159.5	370.5	16x73	909	S[2105]	10279.5	280.5	16x73
830	S[2184]	11148.5	190.5	16x73	910	S[2104]	10268.5	370.5	16x73
831	S[2183]	11137.5	280.5	16x73	911	S[2103]	10257.5	190.5	16x73
832	S[2182]	11126.5	370.5	16x73	912	S[2102]	10246.5	280.5	16x73
833	S[2181]	11115.5	190.5	16x73	913	S[2101]	10235.5	370.5	16x73
834	S[2180]	11104.5	280.5	16x73	914	S[2100]	10224.5	190.5	16x73
835	S[2179]	11093.5	370.5	16x73	915	S[2099]	10213.5	280.5	16x73
836	S[2178]	11082.5	190.5	16x73	916	S[2098]	10202.5	370.5	16x73
837	S[2177]	11071.5	280.5	16x73	917	S[2097]	10191.5	190.5	16x73
838	S[2176]	11060.5	370.5	16x73	918	S[2096]	10180.5	280.5	16x73
839	S[2175]	11049.5	190.5	16x73	919	S[2095]	10169.5	370.5	16x73
840	S[2174]	11038.5	280.5	16x73	920	S[2094]	10158.5	190.5	16x73
841	S[2173]	11027.5	370.5	16x73	921	S[2093]	10147.5	280.5	16x73
842	S[2172]	11016.5	190.5	16x73	922	S[2092]	10136.5	370.5	16x73
843	S[2171]	11005.5	280.5	16x73	923	S[2091]	10125.5	190.5	16x73
844	S[2170]	10994.5	370.5	16x73	924	S[2090]	10114.5	280.5	16x73
845	S[2169]	10983.5	190.5	16x73	925	S[2089]	10103.5	370.5	16x73
846	S[2168]	10972.5	280.5	16x73	926	S[2088]	10092.5	190.5	16x73
847	S[2167]	10961.5	370.5	16x73	927	S[2087]	10081.5	280.5	16x73
848	S[2166]	10950.5	190.5	16x73	928	S[2086]	10070.5	370.5	16x73
849	S[2165]	10939.5	280.5	16x73	929	S[2085]	10059.5	190.5	16x73
850	S[2164]	10928.5	370.5	16x73	930	S[2084]	10048.5	280.5	16x73
851	S[2163]	10917.5	190.5	16x73	931	S[2083]	10037.5	370.5	16x73
852	S[2162]	10906.5	280.5	16x73	932	S[2082]	10026.5	190.5	16x73
853	S[2161]	10895.5	370.5	16x73	933	S[2081]	10015.5	280.5	16x73
854	S[2160]	10884.5	190.5	16x73	934	S[2080]	10004.5	370.5	16x73
855	S[2159]	10873.5	280.5	16x73	935	S[2079]	9993.5	190.5	16x73
856	S[2158]	10862.5	370.5	16x73	936	S[2078]	9982.5	280.5	16x73
857	S[2157]	10851.5	190.5	16x73	937	S[2077]	9971.5	370.5	16x73
858	S[2156]	10840.5	280.5	16x73	938	S[2076]	9960.5	190.5	16x73
859	S[2155]	10829.5	370.5	16x73	939	S[2075]	9949.5	280.5	16x73
860	S[2154]	10818.5	190.5	16x73	940	S[2074]	9938.5	370.5	16x73
861	S[2153]	10807.5	280.5	16x73	941	S[2073]	9927.5	190.5	16x73
862	S[2152]	10796.5	370.5	16x73	942	S[2072]	9916.5	280.5	16x73
863	S[2151]	10785.5	190.5	16x73	943	S[2071]	9905.5	370.5	16x73
864	S[2150]	10774.5	280.5	16x73	944	S[2070]	9894.5	190.5	16x73
865	S[2149]	10763.5	370.5	16x73	945	S[2069]	9883.5	280.5	16x73
866	S[2148]	10752.5	190.5	16x73	946	S[2068]	9872.5	370.5	16x73
867	S[2147]	10741.5	280.5	16x73	947	S[2067]	9861.5	190.5	16x73
868	S[2146]	10730.5	370.5	16x73	948	S[2066]	9850.5	280.5	16x73
869	S[2145]	10719.5	190.5	16x73	949	S[2065]	9839.5	370.5	16x73
870	S[2144]	10708.5	280.5	16x73	950	S[2064]	9828.5	190.5	16x73
871	S[2143]	10697.5	370.5	16x73	951	S[2063]	9817.5	280.5	16x73
872	S[2142]	10686.5	190.5	16x73	952	S[2062]	9806.5	370.5	16x73
873	S[2141]	10675.5	280.5	16x73	953	S[2061]	9795.5	190.5	16x73
874	S[2140]	10664.5	370.5	16x73	954	S[2060]	9784.5	280.5	16x73
875	S[2139]	10653.5	190.5	16x73	955	S[2059]	9773.5	370.5	16x73
876	S[2138]	10642.5	280.5	16x73	956	S[2058]	9762.5	190.5	16x73
877	S[2137]	10631.5	370.5	16x73	957	S[2057]	9751.5	280.5	16x73
878	S[2136]	10620.5	190.5	16x73	958	S[2056]	9740.5	370.5	16x73
879	S[2135]	10609.5	280.5	16x73	959	S[2055]	9729.5	190.5	16x73
880	S[2134]	10598.5	370.5	16x73	960	S[2054]	9718.5	280.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
961	S[2053]	9707.5	370.5	16x73	1041	S[1973]	8827.5	280.5	16x73
962	S[2052]	9696.5	190.5	16x73	1042	S[1972]	8816.5	370.5	16x73
963	S[2051]	9685.5	280.5	16x73	1043	S[1971]	8805.5	190.5	16x73
964	S[2050]	9674.5	370.5	16x73	1044	S[1970]	8794.5	280.5	16x73
965	S[2049]	9663.5	190.5	16x73	1045	S[1969]	8783.5	370.5	16x73
966	S[2048]	9652.5	280.5	16x73	1046	S[1968]	8772.5	190.5	16x73
967	S[2047]	9641.5	370.5	16x73	1047	S[1967]	8761.5	280.5	16x73
968	S[2046]	9630.5	190.5	16x73	1048	S[1966]	8750.5	370.5	16x73
969	S[2045]	9619.5	280.5	16x73	1049	S[1965]	8739.5	190.5	16x73
970	S[2044]	9608.5	370.5	16x73	1050	S[1964]	8728.5	280.5	16x73
971	S[2043]	9597.5	190.5	16x73	1051	S[1963]	8717.5	370.5	16x73
972	S[2042]	9586.5	280.5	16x73	1052	S[1962]	8706.5	190.5	16x73
973	S[2041]	9575.5	370.5	16x73	1053	S[1961]	8695.5	280.5	16x73
974	S[2040]	9564.5	190.5	16x73	1054	S[1960]	8684.5	370.5	16x73
975	S[2039]	9553.5	280.5	16x73	1055	S[1959]	8673.5	190.5	16x73
976	S[2038]	9542.5	370.5	16x73	1056	S[1958]	8662.5	280.5	16x73
977	S[2037]	9531.5	190.5	16x73	1057	S[1957]	8651.5	370.5	16x73
978	S[2036]	9520.5	280.5	16x73	1058	S[1956]	8640.5	190.5	16x73
979	S[2035]	9509.5	370.5	16x73	1059	S[1955]	8629.5	280.5	16x73
980	S[2034]	9498.5	190.5	16x73	1060	S[1954]	8618.5	370.5	16x73
981	S[2033]	9487.5	280.5	16x73	1061	S[1953]	8607.5	190.5	16x73
982	S[2032]	9476.5	370.5	16x73	1062	S[1952]	8596.5	280.5	16x73
983	S[2031]	9465.5	190.5	16x73	1063	S[1951]	8585.5	370.5	16x73
984	S[2030]	9454.5	280.5	16x73	1064	S[1950]	8574.5	190.5	16x73
985	S[2029]	9443.5	370.5	16x73	1065	S[1949]	8563.5	280.5	16x73
986	S[2028]	9432.5	190.5	16x73	1066	S[1948]	8552.5	370.5	16x73
987	S[2027]	9421.5	280.5	16x73	1067	S[1947]	8541.5	190.5	16x73
988	S[2026]	9410.5	370.5	16x73	1068	S[1946]	8530.5	280.5	16x73
989	S[2025]	9399.5	190.5	16x73	1069	S[1945]	8519.5	370.5	16x73
990	S[2024]	9388.5	280.5	16x73	1070	S[1944]	8508.5	190.5	16x73
991	S[2023]	9377.5	370.5	16x73	1071	S[1943]	8497.5	280.5	16x73
992	S[2022]	9366.5	190.5	16x73	1072	S[1942]	8486.5	370.5	16x73
993	S[2021]	9355.5	280.5	16x73	1073	S[1941]	8475.5	190.5	16x73
994	S[2020]	9344.5	370.5	16x73	1074	S[1940]	8464.5	280.5	16x73
995	S[2019]	9333.5	190.5	16x73	1075	S[1939]	8453.5	370.5	16x73
996	S[2018]	9322.5	280.5	16x73	1076	S[1938]	8442.5	190.5	16x73
997	S[2017]	9311.5	370.5	16x73	1077	S[1937]	8431.5	280.5	16x73
998	S[2016]	9300.5	190.5	16x73	1078	S[1936]	8420.5	370.5	16x73
999	S[2015]	9289.5	280.5	16x73	1079	S[1935]	8409.5	190.5	16x73
1000	S[2014]	9280.5	370.5	16x73	1080	S[1934]	8398.5	280.5	16x73
1001	S[2013]	9267.5	190.5	16x73	1081	S[1933]	8387.5	370.5	16x73
1002	S[2012]	9256.5	280.5	16x73	1082	S[1932]	8376.5	190.5	16x73
1003	S[2011]	9245.5	370.5	16x73	1083	S[1931]	8365.5	280.5	16x73
1004	S[2010]	9234.5	190.5	16x73	1084	S[1930]	8354.5	370.5	16x73
1005	S[2009]	9223.5	280.5	16x73	1085	S[1929]	8343.5	190.5	16x73
1006	S[2008]	9212.5	370.5	16x73	1086	S[1928]	8332.5	280.5	16x73
1007	S[2007]	9201.5	190.5	16x73	1087	S[1927]	8321.5	370.5	16x73
1008	S[2006]	9190.5	280.5	16x73	1088	S[1926]	8310.5	190.5	16x73
1009	S[2005]	9179.5	370.5	16x73	1089	S[1925]	8299.5	280.5	16x73
1010	S[2004]	9168.5	190.5	16x73	1090	S[1924]	8288.5	370.5	16x73
1011	S[2003]	9157.5	280.5	16x73	1091	S[1923]	8277.5	190.5	16x73
1012	S[2002]	9146.5	370.5	16x73	1092	S[1922]	8266.5	280.5	16x73
1013	S[2001]	9135.5	190.5	16x73	1093	S[1921]	8255.5	370.5	16x73
1014	S[2000]	9124.5	280.5	16x73	1094	S[1920]	8244.5	190.5	16x73
1015	S[1999]	9113.5	370.5	16x73	1095	S[1919]	8233.5	280.5	16x73
1016	S[1998]	9102.5	190.5	16x73	1096	S[1918]	8222.5	370.5	16x73
1017	S[1997]	9091.5	280.5	16x73	1097	S[1917]	8211.5	190.5	16x73
1018	S[1996]	9080.5	370.5	16x73	1098	S[1916]	8200.5	280.5	16x73
1019	S[1995]	9069.5	190.5	16x73	1099	S[1915]	8189.5	370.5	16x73
1020	S[1994]	9058.5	280.5	16x73	1100	S[1914]	8178.5	190.5	16x73
1021	S[1993]	9047.5	370.5	16x73	1101	S[1913]	8167.5	280.5	16x73
1022	S[1992]	9036.5	190.5	16x73	1102	S[1912]	8156.5	370.5	16x73
1023	S[1991]	9025.5	280.5	16x73	1103	S[1911]	8145.5	190.5	16x73
1024	S[1990]	9014.5	370.5	16x73	1104	S[1910]	8134.5	280.5	16x73
1025	S[1989]	9003.5	190.5	16x73	1105	S[1909]	8123.5	370.5	16x73
1026	S[1988]	8992.5	280.5	16x73	1106	S[1908]	8112.5	190.5	16x73
1027	S[1987]	8981.5	370.5	16x73	1107	S[1907]	8101.5	280.5	16x73
1028	S[1986]	8970.5	190.5	16x73	1108	S[1906]	8090.5	370.5	16x73
1029	S[1985]	8959.5	280.5	16x73	1109	S[1905]	8079.5	190.5	16x73
1030	S[1984]	8948.5	370.5	16x73	1110	S[1904]	8068.5	280.5	16x73
1031	S[1983]	8937.5	190.5	16x73	1111	S[1903]	8057.5	370.5	16x73
1032	S[1982]	8926.5	280.5	16x73	1112	S[1902]	8046.5	190.5	16x73
1033	S[1981]	8915.5	370.5	16x73	1113	S[1901]	8035.5	280.5	16x73
1034	S[1980]	8904.5	190.5	16x73	1114	S[1900]	8024.5	370.5	16x73
1035	S[1979]	8893.5	280.5	16x73	1115	S[1899]	8013.5	190.5	16x73
1036	S[1978]	8882.5	370.5	16x73	1116	S[1898]	8002.5	280.5	16x73
1037	S[1977]	8871.5	190.5	16x73	1117	S[1897]	7991.5	370.5	16x73
1038	S[1976]	8860.5	280.5	16x73	1118	S[1896]	7980.5	190.5	16x73
1039	S[1975]	8849.5	370.5	16x73	1119	S[1895]	7969.5	280.5	16x73
1040	S[1974]	8838.5	190.5	16x73	1120	S[1894]	7958.5	370.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
1121	S[1893]	7947.5	190.5	16x73	1201	S[1813]	7067.5	370.5	16x73
1122	S[1892]	7936.5	280.5	16x73	1202	S[1812]	7056.5	190.5	16x73
1123	S[1891]	7925.5	370.5	16x73	1203	S[1811]	7045.5	280.5	16x73
1124	S[1890]	7914.5	190.5	16x73	1204	S[1810]	7034.5	370.5	16x73
1125	S[1889]	7903.5	280.5	16x73	1205	S[1809]	7023.5	190.5	16x73
1126	S[1888]	7892.5	370.5	16x73	1206	S[1808]	7012.5	280.5	16x73
1127	S[1887]	7881.5	190.5	16x73	1207	S[1807]	7001.5	370.5	16x73
1128	S[1886]	7870.5	280.5	16x73	1208	S[1806]	6990.5	190.5	16x73
1129	S[1885]	7859.5	370.5	16x73	1209	S[1805]	6979.5	280.5	16x73
1130	S[1884]	7848.5	190.5	16x73	1210	S[1804]	6968.5	370.5	16x73
1131	S[1883]	7837.5	280.5	16x73	1211	S[1803]	6957.5	190.5	16x73
1132	S[1882]	7826.5	370.5	16x73	1212	S[1802]	6946.5	280.5	16x73
1133	S[1881]	7815.5	190.5	16x73	1213	S[1801]	6935.5	370.5	16x73
1134	S[1880]	7804.5	280.5	16x73	1214	DUMMY	6924.5	190.5	16x73
1135	S[1879]	7793.5	370.5	16x73	1215	DUMMY	6913.5	280.5	16x73
1136	S[1878]	7782.5	190.5	16x73	1216	DUMMY	6902.5	370.5	16x73
1137	S[1877]	7771.5	280.5	16x73	1217	DUMMY	6891.5	190.5	16x73
1138	S[1876]	7760.5	370.5	16x73	1218	DUMMY	6880.5	280.5	16x73
1139	S[1875]	7749.5	190.5	16x73	1219	DUMMY	6869.5	370.5	16x73
1140	S[1874]	7738.5	280.5	16x73	1220	DUMMY	6858.5	190.5	16x73
1141	S[1873]	7727.5	370.5	16x73	1221	DUMMY	6847.5	280.5	16x73
1142	S[1872]	7716.5	190.5	16x73	1222	DUMMY	6836.5	370.5	16x73
1143	S[1871]	7705.5	280.5	16x73	1223	DUMMY	6825.5	190.5	16x73
1144	S[1870]	7694.5	370.5	16x73	1224	DUMMY	6814.5	280.5	16x73
1145	S[1869]	7683.5	190.5	16x73	1225	DUMMY	6803.5	370.5	16x73
1146	S[1868]	7672.5	280.5	16x73	1226	DUMMY	6792.5	190.5	16x73
1147	S[1867]	7661.5	370.5	16x73	1227	DUMMY	6781.5	280.5	16x73
1148	S[1866]	7650.5	190.5	16x73	1228	DUMMY	6770.5	370.5	16x73
1149	S[1865]	7639.5	280.5	16x73	1229	DUMMY	6759.5	190.5	16x73
1150	S[1864]	7628.5	370.5	16x73	1230	DUMMY	6748.5	280.5	16x73
1151	S[1863]	7617.5	190.5	16x73	1231	DUMMY	6737.5	370.5	16x73
1152	S[1862]	7606.5	280.5	16x73	1232	S[1800]	6726.5	190.5	16x73
1153	S[1861]	7595.5	370.5	16x73	1233	S[1799]	6715.5	280.5	16x73
1154	S[1860]	7584.5	190.5	16x73	1234	S[1798]	6704.5	370.5	16x73
1155	S[1859]	7573.5	280.5	16x73	1235	S[1797]	6693.5	190.5	16x73
1156	S[1858]	7562.5	370.5	16x73	1236	S[1796]	6682.5	280.5	16x73
1157	S[1857]	7551.5	190.5	16x73	1237	S[1795]	6671.5	370.5	16x73
1158	S[1856]	7540.5	280.5	16x73	1238	S[1794]	6660.5	190.5	16x73
1159	S[1855]	7529.5	370.5	16x73	1239	S[1793]	6649.5	280.5	16x73
1160	S[1854]	7518.5	190.5	16x73	1240	S[1792]	6638.5	370.5	16x73
1161	S[1853]	7507.5	280.5	16x73	1241	S[1791]	6627.5	190.5	16x73
1162	S[1852]	7496.5	370.5	16x73	1242	S[1790]	6616.5	280.5	16x73
1163	S[1851]	7485.5	190.5	16x73	1243	S[1789]	6605.5	370.5	16x73
1164	S[1850]	7474.5	280.5	16x73	1244	S[1788]	6594.5	190.5	16x73
1165	S[1849]	7463.5	370.5	16x73	1245	S[1787]	6583.5	280.5	16x73
1166	S[1848]	7452.5	190.5	16x73	1246	S[1786]	6572.5	370.5	16x73
1167	S[1847]	7441.5	280.5	16x73	1247	S[1785]	6561.5	190.5	16x73
1168	S[1846]	7430.5	370.5	16x73	1248	S[1784]	6550.5	280.5	16x73
1169	S[1845]	7419.5	190.5	16x73	1249	S[1783]	6539.5	370.5	16x73
1170	S[1844]	7408.5	280.5	16x73	1250	S[1782]	6528.5	190.5	16x73
1171	S[1843]	7397.5	370.5	16x73	1251	S[1781]	6517.5	280.5	16x73
1172	S[1842]	7386.5	190.5	16x73	1252	S[1780]	6506.5	370.5	16x73
1173	S[1841]	7375.5	280.5	16x73	1253	S[1779]	6495.5	190.5	16x73
1174	S[1840]	7364.5	370.5	16x73	1254	S[1778]	6484.5	280.5	16x73
1175	S[1839]	7353.5	190.5	16x73	1255	S[1777]	6473.5	370.5	16x73
1176	S[1838]	7342.5	280.5	16x73	1256	S[1776]	6462.5	190.5	16x73
1177	S[1837]	7331.5	370.5	16x73	1257	S[1775]	6451.5	280.5	16x73
1178	S[1836]	7320.5	190.5	16x73	1258	S[1774]	6440.5	370.5	16x73
1179	S[1835]	7309.5	280.5	16x73	1259	S[1773]	6429.5	190.5	16x73
1180	S[1834]	7298.5	370.5	16x73	1260	S[1772]	6418.5	280.5	16x73
1181	S[1833]	7287.5	190.5	16x73	1261	S[1771]	6407.5	370.5	16x73
1182	S[1832]	7276.5	280.5	16x73	1262	S[1770]	6396.5	190.5	16x73
1183	S[1831]	7265.5	370.5	16x73	1263	S[1769]	6385.5	280.5	16x73
1184	S[1830]	7254.5	190.5	16x73	1264	S[1768]	6374.5	370.5	16x73
1185	S[1829]	7243.5	280.5	16x73	1265	S[1767]	6363.5	190.5	16x73
1186	S[1828]	7232.5	370.5	16x73	1266	S[1766]	6352.5	280.5	16x73
1187	S[1827]	7221.5	190.5	16x73	1267	S[1765]	6341.5	370.5	16x73
1188	S[1826]	7210.5	280.5	16x73	1268	S[1764]	6330.5	190.5	16x73
1189	S[1825]	7199.5	370.5	16x73	1269	S[1763]	6319.5	280.5	16x73
1190	S[1824]	7190.5	190.5	16x73	1270	S[1762]	6308.5	370.5	16x73
1191	S[1823]	7177.5	280.5	16x73	1271	S[1761]	6297.5	190.5	16x73
1192	S[1822]	7166.5	370.5	16x73	1272	S[1760]	6286.5	280.5	16x73
1193	S[1821]	7155.5	190.5	16x73	1273	S[1759]	6275.5	370.5	16x73
1194	S[1820]	7144.5	280.5	16x73	1274	S[1758]	6264.5	190.5	16x73
1195	S[1819]	7133.5	370.5	16x73	1275	S[1757]	6253.5	280.5	16x73
1196	S[1818]	7122.5	190.5	16x73	1276	S[1756]	6242.5	370.5	16x73
1197	S[1817]	7111.5	280.5	16x73	1277	S[1755]	6231.5	190.5	16x73
1198	S[1816]	7100.5	370.5	16x73	1278	S[1754]	6220.5	280.5	16x73
1199	S[1815]	7089.5	190.5	16x73	1279	S[1753]	6209.5	370.5	16x73
1200	S[1814]	7078.5	280.5	16x73	1280	S[1752]	6198.5	190.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
1281	S[1751]	6187.5	280.5	16x73	1361	S[1671]	5307.5	190.5	16x73
1282	S[1750]	6176.5	370.5	16x73	1362	S[1670]	5296.5	280.5	16x73
1283	S[1749]	6165.5	190.5	16x73	1363	S[1669]	5285.5	370.5	16x73
1284	S[1748]	6154.5	280.5	16x73	1364	S[1668]	5274.5	190.5	16x73
1285	S[1747]	6143.5	370.5	16x73	1365	S[1667]	5263.5	280.5	16x73
1286	S[1746]	6132.5	190.5	16x73	1366	S[1666]	5252.5	370.5	16x73
1287	S[1745]	6121.5	280.5	16x73	1367	S[1665]	5241.5	190.5	16x73
1288	S[1744]	6110.5	370.5	16x73	1368	S[1664]	5230.5	280.5	16x73
1289	S[1743]	6099.5	190.5	16x73	1369	S[1663]	5219.5	370.5	16x73
1290	S[1742]	6088.5	280.5	16x73	1370	S[1662]	5208.5	190.5	16x73
1291	S[1741]	6077.5	370.5	16x73	1371	S[1661]	5197.5	280.5	16x73
1292	S[1740]	6066.5	190.5	16x73	1372	S[1660]	5186.5	370.5	16x73
1293	S[1739]	6055.5	280.5	16x73	1373	S[1659]	5175.5	190.5	16x73
1294	S[1738]	6044.5	370.5	16x73	1374	S[1658]	5164.5	280.5	16x73
1295	S[1737]	6033.5	190.5	16x73	1375	S[1657]	5153.5	370.5	16x73
1296	S[1736]	6022.5	280.5	16x73	1376	S[1656]	5142.5	190.5	16x73
1297	S[1735]	6011.5	370.5	16x73	1377	S[1655]	5131.5	280.5	16x73
1298	S[1734]	6000.5	190.5	16x73	1378	S[1654]	5120.5	370.5	16x73
1299	S[1733]	5989.5	280.5	16x73	1379	S[1653]	5109.5	190.5	16x73
1300	S[1732]	5978.5	370.5	16x73	1380	S[1652]	5098.5	280.5	16x73
1301	S[1731]	5967.5	190.5	16x73	1381	S[1651]	5087.5	370.5	16x73
1302	S[1730]	5956.5	280.5	16x73	1382	S[1650]	5076.5	190.5	16x73
1303	S[1729]	5945.5	370.5	16x73	1383	S[1649]	5065.5	280.5	16x73
1304	S[1728]	5934.5	190.5	16x73	1384	S[1648]	5054.5	370.5	16x73
1305	S[1727]	5923.5	280.5	16x73	1385	S[1647]	5043.5	190.5	16x73
1306	S[1726]	5912.5	370.5	16x73	1386	S[1646]	5032.5	280.5	16x73
1307	S[1725]	5901.5	190.5	16x73	1387	S[1645]	5021.5	370.5	16x73
1308	S[1724]	5890.5	280.5	16x73	1388	S[1644]	5010.5	190.5	16x73
1309	S[1723]	5879.5	370.5	16x73	1389	S[1643]	4999.5	280.5	16x73
1310	S[1722]	5868.5	190.5	16x73	1390	S[1642]	4988.5	370.5	16x73
1311	S[1721]	5857.5	280.5	16x73	1391	S[1641]	4977.5	190.5	16x73
1312	S[1720]	5846.5	370.5	16x73	1392	S[1640]	4966.5	280.5	16x73
1313	S[1719]	5835.5	190.5	16x73	1393	S[1639]	4955.5	370.5	16x73
1314	S[1718]	5824.5	280.5	16x73	1394	S[1638]	4944.5	190.5	16x73
1315	S[1717]	5813.5	370.5	16x73	1395	S[1637]	4933.5	280.5	16x73
1316	S[1716]	5802.5	190.5	16x73	1396	S[1636]	4922.5	370.5	16x73
1317	S[1715]	5791.5	280.5	16x73	1397	S[1635]	4911.5	190.5	16x73
1318	S[1714]	5780.5	370.5	16x73	1398	S[1634]	4900.5	280.5	16x73
1319	S[1713]	5769.5	190.5	16x73	1399	S[1633]	4889.5	370.5	16x73
1320	S[1712]	5758.5	280.5	16x73	1400	S[1632]	4878.5	190.5	16x73
1321	S[1711]	5747.5	370.5	16x73	1401	S[1631]	4867.5	280.5	16x73
1322	S[1710]	5736.5	190.5	16x73	1402	S[1630]	4856.5	370.5	16x73
1323	S[1709]	5725.5	280.5	16x73	1403	S[1629]	4845.5	190.5	16x73
1324	S[1708]	5714.5	370.5	16x73	1404	S[1628]	4834.5	280.5	16x73
1325	S[1707]	5703.5	190.5	16x73	1405	S[1627]	4823.5	370.5	16x73
1326	S[1706]	5692.5	280.5	16x73	1406	S[1626]	4812.5	190.5	16x73
1327	S[1705]	5681.5	370.5	16x73	1407	S[1625]	4801.5	280.5	16x73
1328	S[1704]	5670.5	190.5	16x73	1408	S[1624]	4790.5	370.5	16x73
1329	S[1703]	5659.5	280.5	16x73	1409	S[1623]	4779.5	190.5	16x73
1330	S[1702]	5648.5	370.5	16x73	1410	S[1622]	4768.5	280.5	16x73
1331	S[1701]	5637.5	190.5	16x73	1411	S[1621]	4757.5	370.5	16x73
1332	S[1700]	5626.5	280.5	16x73	1412	S[1620]	4746.5	190.5	16x73
1333	S[1699]	5615.5	370.5	16x73	1413	S[1619]	4735.5	280.5	16x73
1334	S[1698]	5604.5	190.5	16x73	1414	S[1618]	4724.5	370.5	16x73
1335	S[1697]	5593.5	280.5	16x73	1415	S[1617]	4713.5	190.5	16x73
1336	S[1696]	5582.5	370.5	16x73	1416	S[1616]	4702.5	280.5	16x73
1337	S[1695]	5571.5	190.5	16x73	1417	S[1615]	4691.5	370.5	16x73
1338	S[1694]	5560.5	280.5	16x73	1418	S[1614]	4680.5	190.5	16x73
1339	S[1693]	5549.5	370.5	16x73	1419	S[1613]	4669.5	280.5	16x73
1340	S[1692]	5538.5	190.5	16x73	1420	S[1612]	4658.5	370.5	16x73
1341	S[1691]	5527.5	280.5	16x73	1421	S[1611]	4647.5	190.5	16x73
1342	S[1690]	5516.5	370.5	16x73	1422	S[1610]	4636.5	280.5	16x73
1343	S[1689]	5505.5	190.5	16x73	1423	S[1609]	4625.5	370.5	16x73
1344	S[1688]	5494.5	280.5	16x73	1424	S[1608]	4614.5	190.5	16x73
1345	S[1687]	5483.5	370.5	16x73	1425	S[1607]	4603.5	280.5	16x73
1346	S[1686]	5472.5	190.5	16x73	1426	S[1606]	4592.5	370.5	16x73
1347	S[1685]	5461.5	280.5	16x73	1427	S[1605]	4581.5	190.5	16x73
1348	S[1684]	5450.5	370.5	16x73	1428	S[1604]	4570.5	280.5	16x73
1349	S[1683]	5439.5	190.5	16x73	1429	S[1603]	4559.5	370.5	16x73
1350	S[1682]	5428.5	280.5	16x73	1430	S[1602]	4548.5	190.5	16x73
1351	S[1681]	5417.5	370.5	16x73	1431	S[1601]	4537.5	280.5	16x73
1352	S[1680]	5406.5	190.5	16x73	1432	S[1600]	4526.5	370.5	16x73
1353	S[1679]	5395.5	280.5	16x73	1433	S[1599]	4515.5	190.5	16x73
1354	S[1678]	5384.5	370.5	16x73	1434	S[1598]	4504.5	280.5	16x73
1355	S[1677]	5373.5	190.5	16x73	1435	S[1597]	4493.5	370.5	16x73
1356	S[1676]	5362.5	280.5	16x73	1436	S[1596]	4482.5	190.5	16x73
1357	S[1675]	5351.5	370.5	16x73	1437	S[1595]	4471.5	280.5	16x73
1358	S[1674]	5340.5	190.5	16x73	1438	S[1594]	4460.5	370.5	16x73
1359	S[1673]	5329.5	280.5	16x73	1439	S[1593]	4449.5	190.5	16x73
1360	S[1672]	5318.5	370.5	16x73	1440	S[1592]	4438.5	280.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
1441	S[1591]	4427.5	370.5	16x73	1521	S[1511]	3547.5	280.5	16x73
1442	S[1590]	4416.5	190.5	16x73	1522	S[1510]	3536.5	370.5	16x73
1443	S[1589]	4405.5	280.5	16x73	1523	S[1509]	3525.5	190.5	16x73
1444	S[1588]	4394.5	370.5	16x73	1524	S[1508]	3514.5	280.5	16x73
1445	S[1587]	4383.5	190.5	16x73	1525	S[1507]	3503.5	370.5	16x73
1446	S[1586]	4372.5	280.5	16x73	1526	S[1506]	3492.5	190.5	16x73
1447	S[1585]	4361.5	370.5	16x73	1527	S[1505]	3481.5	280.5	16x73
1448	S[1584]	4350.5	190.5	16x73	1528	S[1504]	3470.5	370.5	16x73
1449	S[1583]	4339.5	280.5	16x73	1529	S[1503]	3459.5	190.5	16x73
1450	S[1582]	4328.5	370.5	16x73	1530	S[1502]	3448.5	280.5	16x73
1451	S[1581]	4317.5	190.5	16x73	1531	S[1501]	3437.5	370.5	16x73
1452	S[1580]	4306.5	280.5	16x73	1532	S[1500]	3426.5	190.5	16x73
1453	S[1579]	4295.5	370.5	16x73	1533	S[1499]	3415.5	280.5	16x73
1454	S[1578]	4284.5	190.5	16x73	1534	S[1498]	3404.5	370.5	16x73
1455	S[1577]	4273.5	280.5	16x73	1535	S[1497]	3393.5	190.5	16x73
1456	S[1576]	4262.5	370.5	16x73	1536	S[1496]	3382.5	280.5	16x73
1457	S[1575]	4251.5	190.5	16x73	1537	S[1495]	3371.5	370.5	16x73
1458	S[1574]	4240.5	280.5	16x73	1538	S[1494]	3360.5	190.5	16x73
1459	S[1573]	4229.5	370.5	16x73	1539	S[1493]	3349.5	280.5	16x73
1460	S[1572]	4218.5	190.5	16x73	1540	S[1492]	3338.5	370.5	16x73
1461	S[1571]	4207.5	280.5	16x73	1541	S[1491]	3327.5	190.5	16x73
1462	S[1570]	4196.5	370.5	16x73	1542	S[1490]	3316.5	280.5	16x73
1463	S[1569]	4185.5	190.5	16x73	1543	S[1489]	3305.5	370.5	16x73
1464	S[1568]	4174.5	280.5	16x73	1544	S[1488]	3294.5	190.5	16x73
1465	S[1567]	4163.5	370.5	16x73	1545	S[1487]	3283.5	280.5	16x73
1466	S[1566]	4152.5	190.5	16x73	1546	S[1486]	3272.5	370.5	16x73
1467	S[1565]	4141.5	280.5	16x73	1547	S[1485]	3261.5	190.5	16x73
1468	S[1564]	4130.5	370.5	16x73	1548	S[1484]	3250.5	280.5	16x73
1469	S[1563]	4119.5	190.5	16x73	1549	S[1483]	3239.5	370.5	16x73
1470	S[1562]	4108.5	280.5	16x73	1550	S[1482]	3228.5	190.5	16x73
1471	S[1561]	4097.5	370.5	16x73	1551	S[1481]	3217.5	280.5	16x73
1472	S[1560]	4086.5	190.5	16x73	1552	S[1480]	3206.5	370.5	16x73
1473	S[1559]	4075.5	280.5	16x73	1553	S[1479]	3195.5	190.5	16x73
1474	S[1558]	4064.5	370.5	16x73	1554	S[1478]	3184.5	280.5	16x73
1475	S[1557]	4053.5	190.5	16x73	1555	S[1477]	3173.5	370.5	16x73
1476	S[1556]	4042.5	280.5	16x73	1556	S[1476]	3162.5	190.5	16x73
1477	S[1555]	4031.5	370.5	16x73	1557	S[1475]	3151.5	280.5	16x73
1478	S[1554]	4020.5	190.5	16x73	1558	S[1474]	3140.5	370.5	16x73
1479	S[1553]	4009.5	280.5	16x73	1559	S[1473]	3129.5	190.5	16x73
1480	S[1552]	3998.5	370.5	16x73	1560	S[1472]	3118.5	280.5	16x73
1481	S[1551]	3987.5	190.5	16x73	1561	S[1471]	3107.5	370.5	16x73
1482	S[1550]	3976.5	280.5	16x73	1562	S[1470]	3096.5	190.5	16x73
1483	S[1549]	3965.5	370.5	16x73	1563	S[1469]	3085.5	280.5	16x73
1484	S[1548]	3954.5	190.5	16x73	1564	S[1468]	3074.5	370.5	16x73
1485	S[1547]	3943.5	280.5	16x73	1565	S[1467]	3063.5	190.5	16x73
1486	S[1546]	3932.5	370.5	16x73	1566	S[1466]	3052.5	280.5	16x73
1487	S[1545]	3921.5	190.5	16x73	1567	S[1465]	3041.5	370.5	16x73
1488	S[1544]	3910.5	280.5	16x73	1568	S[1464]	3030.5	190.5	16x73
1489	S[1543]	3899.5	370.5	16x73	1569	S[1463]	3019.5	280.5	16x73
1490	S[1542]	3888.5	190.5	16x73	1570	S[1462]	3008.5	370.5	16x73
1491	S[1541]	3877.5	280.5	16x73	1571	S[1461]	2997.5	190.5	16x73
1492	S[1540]	3866.5	370.5	16x73	1572	S[1460]	2986.5	280.5	16x73
1493	S[1539]	3855.5	190.5	16x73	1573	S[1459]	2975.5	370.5	16x73
1494	S[1538]	3844.5	280.5	16x73	1574	S[1458]	2964.5	190.5	16x73
1495	S[1537]	3833.5	370.5	16x73	1575	S[1457]	2953.5	280.5	16x73
1496	S[1536]	3822.5	190.5	16x73	1576	S[1456]	2942.5	370.5	16x73
1497	S[1535]	3811.5	280.5	16x73	1577	S[1455]	2931.5	190.5	16x73
1498	S[1534]	3800.5	370.5	16x73	1578	S[1454]	2920.5	280.5	16x73
1499	S[1533]	3789.5	190.5	16x73	1579	S[1453]	2909.5	370.5	16x73
1500	S[1532]	3778.5	280.5	16x73	1580	S[1452]	2898.5	190.5	16x73
1501	S[1531]	3767.5	370.5	16x73	1581	S[1451]	2887.5	280.5	16x73
1502	S[1530]	3756.5	190.5	16x73	1582	S[1450]	2876.5	370.5	16x73
1503	S[1529]	3745.5	280.5	16x73	1583	S[1449]	2865.5	190.5	16x73
1504	S[1528]	3734.5	370.5	16x73	1584	S[1448]	2854.5	280.5	16x73
1505	S[1527]	3723.5	190.5	16x73	1585	S[1447]	2843.5	370.5	16x73
1506	S[1526]	3712.5	280.5	16x73	1586	S[1446]	2832.5	190.5	16x73
1507	S[1525]	3701.5	370.5	16x73	1587	S[1445]	2821.5	280.5	16x73
1508	S[1524]	3690.5	190.5	16x73	1588	S[1444]	2810.5	370.5	16x73
1509	S[1523]	3679.5	280.5	16x73	1589	S[1443]	2799.5	190.5	16x73
1510	S[1522]	3668.5	370.5	16x73	1590	S[1442]	2788.5	280.5	16x73
1511	S[1521]	3657.5	190.5	16x73	1591	S[1441]	2777.5	370.5	16x73
1512	S[1520]	3646.5	280.5	16x73	1592	S[1440]	2766.5	190.5	16x73
1513	S[1519]	3635.5	370.5	16x73	1593	S[1439]	2755.5	280.5	16x73
1514	S[1518]	3624.5	190.5	16x73	1594	S[1438]	2744.5	370.5	16x73
1515	S[1517]	3613.5	280.5	16x73	1595	S[1437]	2733.5	190.5	16x73
1516	S[1516]	3602.5	370.5	16x73	1596	S[1436]	2722.5	280.5	16x73
1517	S[1515]	3591.5	190.5	16x73	1597	S[1435]	2711.5	370.5	16x73
1518	S[1514]	3580.5	280.5	16x73	1598	S[1434]	2700.5	190.5	16x73
1519	S[1513]	3569.5	370.5	16x73	1599	S[1433]	2689.5	280.5	16x73
1520	S[1512]	3558.5	190.5	16x73	1600	S[1432]	2678.5	370.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
1601	S[1431]	2667.5	190.5	16x73	1681	S[1351]	1787.5	370.5	16x73
1602	S[1430]	2656.5	280.5	16x73	1682	S[1350]	1776.5	190.5	16x73
1603	S[1429]	2645.5	370.5	16x73	1683	S[1349]	1765.5	280.5	16x73
1604	S[1428]	2634.5	190.5	16x73	1684	S[1348]	1754.5	370.5	16x73
1605	S[1427]	2623.5	280.5	16x73	1685	S[1347]	1743.5	190.5	16x73
1606	S[1426]	2612.5	370.5	16x73	1686	S[1346]	1732.5	280.5	16x73
1607	S[1425]	2601.5	190.5	16x73	1687	S[1345]	1721.5	370.5	16x73
1608	S[1424]	2590.5	280.5	16x73	1688	S[1344]	1710.5	190.5	16x73
1609	S[1423]	2579.5	370.5	16x73	1689	S[1343]	1699.5	280.5	16x73
1610	S[1422]	2568.5	190.5	16x73	1690	S[1342]	1688.5	370.5	16x73
1611	S[1421]	2557.5	280.5	16x73	1691	S[1341]	1677.5	190.5	16x73
1612	S[1420]	2546.5	370.5	16x73	1692	S[1340]	1666.5	280.5	16x73
1613	S[1419]	2535.5	190.5	16x73	1693	S[1339]	1655.5	370.5	16x73
1614	S[1418]	2524.5	280.5	16x73	1694	S[1338]	1644.5	190.5	16x73
1615	S[1417]	2513.5	370.5	16x73	1695	S[1337]	1633.5	280.5	16x73
1616	S[1416]	2502.5	190.5	16x73	1696	S[1336]	1622.5	370.5	16x73
1617	S[1415]	2491.5	280.5	16x73	1697	S[1335]	1611.5	190.5	16x73
1618	S[1414]	2480.5	370.5	16x73	1698	S[1334]	1600.5	280.5	16x73
1619	S[1413]	2469.5	190.5	16x73	1699	S[1333]	1589.5	370.5	16x73
1620	S[1412]	2458.5	280.5	16x73	1700	S[1332]	1578.5	190.5	16x73
1621	S[1411]	2447.5	370.5	16x73	1701	S[1331]	1567.5	280.5	16x73
1622	S[1410]	2436.5	190.5	16x73	1702	S[1330]	1556.5	370.5	16x73
1623	S[1409]	2425.5	280.5	16x73	1703	S[1329]	1545.5	190.5	16x73
1624	S[1408]	2414.5	370.5	16x73	1704	S[1328]	1534.5	280.5	16x73
1625	S[1407]	2403.5	190.5	16x73	1705	S[1327]	1523.5	370.5	16x73
1626	S[1406]	2392.5	280.5	16x73	1706	S[1326]	1512.5	190.5	16x73
1627	S[1405]	2381.5	370.5	16x73	1707	S[1325]	1501.5	280.5	16x73
1628	S[1404]	2370.5	190.5	16x73	1708	S[1324]	1490.5	370.5	16x73
1629	S[1403]	2359.5	280.5	16x73	1709	S[1323]	1479.5	190.5	16x73
1630	S[1402]	2348.5	370.5	16x73	1710	S[1322]	1468.5	280.5	16x73
1631	S[1401]	2337.5	190.5	16x73	1711	S[1321]	1457.5	370.5	16x73
1632	S[1400]	2326.5	280.5	16x73	1712	S[1320]	1446.5	190.5	16x73
1633	S[1399]	2315.5	370.5	16x73	1713	S[1319]	1435.5	280.5	16x73
1634	S[1398]	2304.5	190.5	16x73	1714	S[1318]	1424.5	370.5	16x73
1635	S[1397]	2293.5	280.5	16x73	1715	S[1317]	1413.5	190.5	16x73
1636	S[1396]	2282.5	370.5	16x73	1716	S[1316]	1402.5	280.5	16x73
1637	S[1395]	2271.5	190.5	16x73	1717	S[1315]	1391.5	370.5	16x73
1638	S[1394]	2260.5	280.5	16x73	1718	S[1314]	1380.5	190.5	16x73
1639	S[1393]	2249.5	370.5	16x73	1719	S[1313]	1369.5	280.5	16x73
1640	S[1392]	2238.5	190.5	16x73	1720	S[1312]	1358.5	370.5	16x73
1641	S[1391]	2227.5	280.5	16x73	1721	S[1311]	1347.5	190.5	16x73
1642	S[1390]	2216.5	370.5	16x73	1722	S[1310]	1336.5	280.5	16x73
1643	S[1389]	2205.5	190.5	16x73	1723	S[1309]	1325.5	370.5	16x73
1644	S[1388]	2194.5	280.5	16x73	1724	S[1308]	1314.5	190.5	16x73
1645	S[1387]	2183.5	370.5	16x73	1725	S[1307]	1303.5	280.5	16x73
1646	S[1386]	2172.5	190.5	16x73	1726	S[1306]	1292.5	370.5	16x73
1647	S[1385]	2161.5	280.5	16x73	1727	S[1305]	1281.5	190.5	16x73
1648	S[1384]	2150.5	370.5	16x73	1728	S[1304]	1270.5	280.5	16x73
1649	S[1383]	2139.5	190.5	16x73	1729	S[1303]	1259.5	370.5	16x73
1650	S[1382]	2128.5	280.5	16x73	1730	S[1302]	1248.5	190.5	16x73
1651	S[1381]	2117.5	370.5	16x73	1731	S[1301]	1237.5	280.5	16x73
1652	S[1380]	2106.5	190.5	16x73	1732	S[1300]	1226.5	370.5	16x73
1653	S[1379]	2095.5	280.5	16x73	1733	S[1299]	1215.5	190.5	16x73
1654	S[1378]	2084.5	370.5	16x73	1734	S[1298]	1204.5	280.5	16x73
1655	S[1377]	2073.5	190.5	16x73	1735	S[1297]	1193.5	370.5	16x73
1656	S[1376]	2062.5	280.5	16x73	1736	S[1296]	1182.5	190.5	16x73
1657	S[1375]	2051.5	370.5	16x73	1737	S[1295]	1171.5	280.5	16x73
1658	S[1374]	2040.5	190.5	16x73	1738	S[1294]	1160.5	370.5	16x73
1659	S[1373]	2029.5	280.5	16x73	1739	S[1293]	1149.5	190.5	16x73
1660	S[1372]	2018.5	370.5	16x73	1740	S[1292]	1138.5	280.5	16x73
1661	S[1371]	2007.5	190.5	16x73	1741	S[1291]	1127.5	370.5	16x73
1662	S[1370]	1996.5	280.5	16x73	1742	S[1290]	1116.5	190.5	16x73
1663	S[1369]	1985.5	370.5	16x73	1743	S[1289]	1105.5	280.5	16x73
1664	S[1368]	1974.5	190.5	16x73	1744	S[1288]	1094.5	370.5	16x73
1665	S[1367]	1963.5	280.5	16x73	1745	S[1287]	1083.5	190.5	16x73
1666	S[1366]	1952.5	370.5	16x73	1746	S[1286]	1072.5	280.5	16x73
1667	S[1365]	1941.5	190.5	16x73	1747	S[1285]	1061.5	370.5	16x73
1668	S[1364]	1930.5	280.5	16x73	1748	S[1284]	1050.5	190.5	16x73
1669	S[1363]	1919.5	370.5	16x73	1749	S[1283]	1039.5	280.5	16x73
1670	S[1362]	1908.5	190.5	16x73	1750	S[1282]	1028.5	370.5	16x73
1671	S[1361]	1897.5	280.5	16x73	1751	S[1281]	1017.5	190.5	16x73
1672	S[1360]	1886.5	370.5	16x73	1752	S[1280]	1006.5	280.5	16x73
1673	S[1359]	1875.5	190.5	16x73	1753	S[1279]	995.5	370.5	16x73
1674	S[1358]	1864.5	280.5	16x73	1754	S[1278]	984.5	190.5	16x73
1675	S[1357]	1853.5	370.5	16x73	1755	S[1277]	973.5	280.5	16x73
1676	S[1356]	1842.5	190.5	16x73	1756	S[1276]	962.5	370.5	16x73
1677	S[1355]	1831.5	280.5	16x73	1757	S[1275]	951.5	190.5	16x73
1678	S[1354]	1820.5	370.5	16x73	1758	S[1274]	940.5	280.5	16x73
1679	S[1353]	1809.5	190.5	16x73	1759	S[1273]	929.5	370.5	16x73
1680	S[1352]	1798.5	280.5	16x73	1760	S[1272]	918.5	190.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
1761	S[1271]	907.5	280.5	16x73	1841	DUMMY	27.5	190.5	16x73
1762	S[1270]	896.5	370.5	16x73	1842	DUMMY	16.5	280.5	16x73
1763	S[1269]	885.5	190.5	16x73	1843	DUMMY	5.5	370.5	16x73
1764	S[1268]	874.5	280.5	16x73	1844	DUMMY	-5.5	190.5	16x73
1765	S[1267]	863.5	370.5	16x73	1845	DUMMY	-16.5	280.5	16x73
1766	S[1266]	852.5	190.5	16x73	1846	DUMMY	-27.5	370.5	16x73
1767	S[1265]	841.5	280.5	16x73	1847	DUMMY	-38.5	190.5	16x73
1768	S[1264]	830.5	370.5	16x73	1848	DUMMY	-49.5	280.5	16x73
1769	S[1263]	819.5	190.5	16x73	1849	DUMMY	-60.5	370.5	16x73
1770	S[1262]	808.5	280.5	16x73	1850	DUMMY	-71.5	190.5	16x73
1771	S[1261]	797.5	370.5	16x73	1851	DUMMY	-82.5	280.5	16x73
1772	S[1260]	786.5	190.5	16x73	1852	DUMMY	-93.5	370.5	16x73
1773	S[1259]	775.5	280.5	16x73	1853	DUMMY	-104.5	190.5	16x73
1774	S[1258]	764.5	370.5	16x73	1854	DUMMY	-115.5	280.5	16x73
1775	S[1257]	753.5	190.5	16x73	1855	DUMMY	-126.5	370.5	16x73
1776	S[1256]	742.5	280.5	16x73	1856	S[1200]	-137.5	190.5	16x73
1777	S[1255]	731.5	370.5	16x73	1857	S[1199]	-148.5	280.5	16x73
1778	S[1254]	720.5	190.5	16x73	1858	S[1198]	-159.5	370.5	16x73
1779	S[1253]	709.5	280.5	16x73	1859	S[1197]	-170.5	190.5	16x73
1780	S[1252]	698.5	370.5	16x73	1860	S[1196]	-181.5	280.5	16x73
1781	S[1251]	687.5	190.5	16x73	1861	S[1195]	-192.5	370.5	16x73
1782	S[1250]	676.5	280.5	16x73	1862	S[1194]	-203.5	190.5	16x73
1783	S[1249]	665.5	370.5	16x73	1863	S[1193]	-214.5	280.5	16x73
1784	S[1248]	654.5	190.5	16x73	1864	S[1192]	-225.5	370.5	16x73
1785	S[1247]	643.5	280.5	16x73	1865	S[1191]	-236.5	190.5	16x73
1786	S[1246]	632.5	370.5	16x73	1866	S[1190]	-247.5	280.5	16x73
1787	S[1245]	621.5	190.5	16x73	1867	S[1189]	-258.5	370.5	16x73
1788	S[1244]	610.5	280.5	16x73	1868	S[1188]	-269.5	190.5	16x73
1789	S[1243]	599.5	370.5	16x73	1869	S[1187]	-280.5	280.5	16x73
1790	S[1242]	588.5	190.5	16x73	1870	S[1186]	-291.5	370.5	16x73
1791	S[1241]	577.5	280.5	16x73	1871	S[1185]	-302.5	190.5	16x73
1792	S[1240]	566.5	370.5	16x73	1872	S[1184]	-313.5	280.5	16x73
1793	S[1239]	555.5	190.5	16x73	1873	S[1183]	-324.5	370.5	16x73
1794	S[1238]	544.5	280.5	16x73	1874	S[1182]	-335.5	190.5	16x73
1795	S[1237]	533.5	370.5	16x73	1875	S[1181]	-346.5	280.5	16x73
1796	S[1236]	522.5	190.5	16x73	1876	S[1180]	-357.5	370.5	16x73
1797	S[1235]	511.5	280.5	16x73	1877	S[1179]	-370.5	190.5	16x73
1798	S[1234]	500.5	370.5	16x73	1878	S[1178]	-379.5	280.5	16x73
1799	S[1233]	489.5	190.5	16x73	1879	S[1177]	-390.5	370.5	16x73
1800	S[1232]	478.5	280.5	16x73	1880	S[1176]	-401.5	190.5	16x73
1801	S[1231]	467.5	370.5	16x73	1881	S[1175]	-412.5	280.5	16x73
1802	S[1230]	456.5	190.5	16x73	1882	S[1174]	-423.5	370.5	16x73
1803	S[1229]	445.5	280.5	16x73	1883	S[1173]	-434.5	190.5	16x73
1804	S[1228]	434.5	370.5	16x73	1884	S[1172]	-445.5	280.5	16x73
1805	S[1227]	423.5	190.5	16x73	1885	S[1171]	-456.5	370.5	16x73
1806	S[1226]	412.5	280.5	16x73	1886	S[1170]	-467.5	190.5	16x73
1807	S[1225]	401.5	370.5	16x73	1887	S[1169]	-478.5	280.5	16x73
1808	S[1224]	390.5	190.5	16x73	1888	S[1168]	-489.5	370.5	16x73
1809	S[1223]	379.5	280.5	16x73	1889	S[1167]	-500.5	190.5	16x73
1810	S[1222]	370.5	370.5	16x73	1890	S[1166]	-511.5	280.5	16x73
1811	S[1221]	357.5	190.5	16x73	1891	S[1165]	-522.5	370.5	16x73
1812	S[1220]	346.5	280.5	16x73	1892	S[1164]	-533.5	190.5	16x73
1813	S[1219]	335.5	370.5	16x73	1893	S[1163]	-544.5	280.5	16x73
1814	S[1218]	324.5	190.5	16x73	1894	S[1162]	-555.5	370.5	16x73
1815	S[1217]	313.5	280.5	16x73	1895	S[1161]	-566.5	190.5	16x73
1816	S[1216]	302.5	370.5	16x73	1896	S[1160]	-577.5	280.5	16x73
1817	S[1215]	291.5	190.5	16x73	1897	S[1159]	-588.5	370.5	16x73
1818	S[1214]	280.5	280.5	16x73	1898	S[1158]	-599.5	190.5	16x73
1819	S[1213]	269.5	370.5	16x73	1899	S[1157]	-610.5	280.5	16x73
1820	S[1212]	258.5	190.5	16x73	1900	S[1156]	-621.5	370.5	16x73
1821	S[1211]	247.5	280.5	16x73	1901	S[1155]	-632.5	190.5	16x73
1822	S[1210]	236.5	370.5	16x73	1902	S[1154]	-643.5	280.5	16x73
1823	S[1209]	225.5	190.5	16x73	1903	S[1153]	-654.5	370.5	16x73
1824	S[1208]	214.5	280.5	16x73	1904	S[1152]	-665.5	190.5	16x73
1825	S[1207]	203.5	370.5	16x73	1905	S[1151]	-676.5	280.5	16x73
1826	S[1206]	192.5	190.5	16x73	1906	S[1150]	-687.5	370.5	16x73
1827	S[1205]	181.5	280.5	16x73	1907	S[1149]	-698.5	190.5	16x73
1828	S[1204]	170.5	370.5	16x73	1908	S[1148]	-709.5	280.5	16x73
1829	S[1203]	159.5	190.5	16x73	1909	S[1147]	-720.5	370.5	16x73
1830	S[1202]	148.5	280.5	16x73	1910	S[1146]	-731.5	190.5	16x73
1831	S[1201]	137.5	370.5	16x73	1911	S[1145]	-742.5	280.5	16x73
1832	DUMMY	126.5	190.5	16x73	1912	S[1144]	-753.5	370.5	16x73
1833	DUMMY	115.5	280.5	16x73	1913	S[1143]	-764.5	190.5	16x73
1834	DUMMY	104.5	370.5	16x73	1914	S[1142]	-775.5	280.5	16x73
1835	DUMMY	93.5	190.5	16x73	1915	S[1141]	-786.5	370.5	16x73
1836	DUMMY	82.5	280.5	16x73	1916	S[1140]	-797.5	190.5	16x73
1837	DUMMY	71.5	370.5	16x73	1917	S[1139]	-808.5	280.5	16x73
1838	DUMMY	60.5	190.5	16x73	1918	S[1138]	-819.5	370.5	16x73
1839	DUMMY	49.5	280.5	16x73	1919	S[1137]	-830.5	190.5	16x73
1840	DUMMY	38.5	370.5	16x73	1920	S[1136]	-841.5	280.5	16x73
NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)

1921	S[1135]	-852.5	370.5	16x73	2001	S[1055]	-1732.5	280.5	16x73
1922	S[1134]	-863.5	190.5	16x73	2002	S[1054]	-1743.5	370.5	16x73
1923	S[1133]	-874.5	280.5	16x73	2003	S[1053]	-1754.5	190.5	16x73
1924	S[1132]	-885.5	370.5	16x73	2004	S[1052]	-1765.5	280.5	16x73
1925	S[1131]	-896.5	190.5	16x73	2005	S[1051]	-1776.5	370.5	16x73
1926	S[1130]	-907.5	280.5	16x73	2006	S[1050]	-1787.5	190.5	16x73
1927	S[1129]	-918.5	370.5	16x73	2007	S[1049]	-1798.5	280.5	16x73
1928	S[1128]	-929.5	190.5	16x73	2008	S[1048]	-1809.5	370.5	16x73
1929	S[1127]	-940.5	280.5	16x73	2009	S[1047]	-1820.5	190.5	16x73
1930	S[1126]	-951.5	370.5	16x73	2010	S[1046]	-1831.5	280.5	16x73
1931	S[1125]	-962.5	190.5	16x73	2011	S[1045]	-1842.5	370.5	16x73
1932	S[1124]	-973.5	280.5	16x73	2012	S[1044]	-1853.5	190.5	16x73
1933	S[1123]	-984.5	370.5	16x73	2013	S[1043]	-1864.5	280.5	16x73
1934	S[1122]	-995.5	190.5	16x73	2014	S[1042]	-1875.5	370.5	16x73
1935	S[1121]	-1006.5	280.5	16x73	2015	S[1041]	-1886.5	190.5	16x73
1936	S[1120]	-1017.5	370.5	16x73	2016	S[1040]	-1897.5	280.5	16x73
1937	S[1119]	-1028.5	190.5	16x73	2017	S[1039]	-1908.5	370.5	16x73
1938	S[1118]	-1039.5	280.5	16x73	2018	S[1038]	-1919.5	190.5	16x73
1939	S[1117]	-1050.5	370.5	16x73	2019	S[1037]	-1930.5	280.5	16x73
1940	S[1116]	-1061.5	190.5	16x73	2020	S[1036]	-1941.5	370.5	16x73
1941	S[1115]	-1072.5	280.5	16x73	2021	S[1035]	-1952.5	190.5	16x73
1942	S[1114]	-1083.5	370.5	16x73	2022	S[1034]	-1963.5	280.5	16x73
1943	S[1113]	-1094.5	190.5	16x73	2023	S[1033]	-1974.5	370.5	16x73
1944	S[1112]	-1105.5	280.5	16x73	2024	S[1032]	-1985.5	190.5	16x73
1945	S[1111]	-1116.5	370.5	16x73	2025	S[1031]	-1996.5	280.5	16x73
1946	S[1110]	-1127.5	190.5	16x73	2026	S[1030]	-2007.5	370.5	16x73
1947	S[1109]	-1138.5	280.5	16x73	2027	S[1029]	-2018.5	190.5	16x73
1948	S[1108]	-1149.5	370.5	16x73	2028	S[1028]	-2029.5	280.5	16x73
1949	S[1107]	-1160.5	190.5	16x73	2029	S[1027]	-2040.5	370.5	16x73
1950	S[1106]	-1171.5	280.5	16x73	2030	S[1026]	-2051.5	190.5	16x73
1951	S[1105]	-1182.5	370.5	16x73	2031	S[1025]	-2062.5	280.5	16x73
1952	S[1104]	-1193.5	190.5	16x73	2032	S[1024]	-2073.5	370.5	16x73
1953	S[1103]	-1204.5	280.5	16x73	2033	S[1023]	-2084.5	190.5	16x73
1954	S[1102]	-1215.5	370.5	16x73	2034	S[1022]	-2095.5	280.5	16x73
1955	S[1101]	-1226.5	190.5	16x73	2035	S[1021]	-2106.5	370.5	16x73
1956	S[1100]	-1237.5	280.5	16x73	2036	S[1020]	-2117.5	190.5	16x73
1957	S[1099]	-1248.5	370.5	16x73	2037	S[1019]	-2128.5	280.5	16x73
1958	S[1098]	-1259.5	190.5	16x73	2038	S[1018]	-2139.5	370.5	16x73
1959	S[1097]	-1270.5	280.5	16x73	2039	S[1017]	-2150.5	190.5	16x73
1960	S[1096]	-1281.5	370.5	16x73	2040	S[1016]	-2161.5	280.5	16x73
1961	S[1095]	-1292.5	190.5	16x73	2041	S[1015]	-2172.5	370.5	16x73
1962	S[1094]	-1303.5	280.5	16x73	2042	S[1014]	-2183.5	190.5	16x73
1963	S[1093]	-1314.5	370.5	16x73	2043	S[1013]	-2194.5	280.5	16x73
1964	S[1092]	-1325.5	190.5	16x73	2044	S[1012]	-2205.5	370.5	16x73
1965	S[1091]	-1336.5	280.5	16x73	2045	S[1011]	-2216.5	190.5	16x73
1966	S[1090]	-1347.5	370.5	16x73	2046	S[1010]	-2227.5	280.5	16x73
1967	S[1089]	-1358.5	190.5	16x73	2047	S[1009]	-2238.5	370.5	16x73
1968	S[1088]	-1369.5	280.5	16x73	2048	S[1008]	-2249.5	190.5	16x73
1969	S[1087]	-1380.5	370.5	16x73	2049	S[1007]	-2260.5	280.5	16x73
1970	S[1086]	-1391.5	190.5	16x73	2050	S[1006]	-2271.5	370.5	16x73
1971	S[1085]	-1402.5	280.5	16x73	2051	S[1005]	-2282.5	190.5	16x73
1972	S[1084]	-1413.5	370.5	16x73	2052	S[1004]	-2293.5	280.5	16x73
1973	S[1083]	-1424.5	190.5	16x73	2053	S[1003]	-2304.5	370.5	16x73
1974	S[1082]	-1435.5	280.5	16x73	2054	S[1002]	-2315.5	190.5	16x73
1975	S[1081]	-1446.5	370.5	16x73	2055	S[1001]	-2326.5	280.5	16x73
1976	S[1080]	-1457.5	190.5	16x73	2056	S[1000]	-2337.5	370.5	16x73
1977	S[1079]	-1468.5	280.5	16x73	2057	S[999]	-2348.5	190.5	16x73
1978	S[1078]	-1479.5	370.5	16x73	2058	S[998]	-2359.5	280.5	16x73
1979	S[1077]	-1490.5	190.5	16x73	2059	S[997]	-2370.5	370.5	16x73
1980	S[1076]	-1501.5	280.5	16x73	2060	S[996]	-2381.5	190.5	16x73
1981	S[1075]	-1512.5	370.5	16x73	2061	S[995]	-2392.5	280.5	16x73
1982	S[1074]	-1523.5	190.5	16x73	2062	S[994]	-2403.5	370.5	16x73
1983	S[1073]	-1534.5	280.5	16x73	2063	S[993]	-2414.5	190.5	16x73
1984	S[1072]	-1545.5	370.5	16x73	2064	S[992]	-2425.5	280.5	16x73
1985	S[1071]	-1556.5	190.5	16x73	2065	S[991]	-2436.5	370.5	16x73
1986	S[1070]	-1567.5	280.5	16x73	2066	S[990]	-2447.5	190.5	16x73
1987	S[1069]	-1578.5	370.5	16x73	2067	S[989]	-2458.5	280.5	16x73
1988	S[1068]	-1589.5	190.5	16x73	2068	S[988]	-2469.5	370.5	16x73
1989	S[1067]	-1600.5	280.5	16x73	2069	S[987]	-2480.5	190.5	16x73
1990	S[1066]	-1611.5	370.5	16x73	2070	S[986]	-2491.5	280.5	16x73
1991	S[1065]	-1622.5	190.5	16x73	2071	S[985]	-2502.5	370.5	16x73
1992	S[1064]	-1633.5	280.5	16x73	2072	S[984]	-2513.5	190.5	16x73
1993	S[1063]	-1644.5	370.5	16x73	2073	S[983]	-2524.5	280.5	16x73
1994	S[1062]	-1655.5	190.5	16x73	2074	S[982]	-2535.5	370.5	16x73
1995	S[1061]	-1666.5	280.5	16x73	2075	S[981]	-2546.5	190.5	16x73
1996	S[1060]	-1677.5	370.5	16x73	2076	S[980]	-2557.5	280.5	16x73
1997	S[1059]	-1688.5	190.5	16x73	2077	S[979]	-2568.5	370.5	16x73
1998	S[1058]	-1699.5	280.5	16x73	2078	S[978]	-2579.5	190.5	16x73
1999	S[1057]	-1710.5	370.5	16x73	2079	S[977]	-2590.5	280.5	16x73
2000	S[1056]	-1721.5	190.5	16x73	2080	S[976]	-2601.5	370.5	16x73

NO.	Name	X	Y	Bump size (um)	NO.	Name	X	Y	Bump size (um)
2081	S[975]	-2612.5	190.5	16x73	2161				
2082	S[974]	-2623.5	280.5	16x73	2162				
2083	S[973]	-2634.5	370.5	16x73	2163				
2084	S[972]	-2645.5	190.5	16x73	2164				
2085	S[971]	-2656.5	280.5	16x73	2165				
2086	S[970]	-2667.5	370.5	16x73	2166				
2087	S[969]	-2678.5	190.5	16x73	2167				
2088	S[968]	-2689.5	280.5	16x73	2168				
2089	S[967]	-2700.5	370.5	16x73	2169				
2090	S[966]	-2711.5	190.5	16x73	2170				
2091	S[965]	-2722.5	280.5	16x73	2171				
2092	S[964]	-2733.5	370.5	16x73	2172				
2093	S[963]	-2744.5	190.5	16x73	2173				
2094	S[962]	-2755.5	280.5	16x73	2174				
2095	S[961]	-2766.5	370.5	16x73	2175				
2096					2176				
2097					2177				
2098					2178				
2099					2179				
2100					2180				
2101					2181				
2102					2182				
2103					2183				
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2109					2189				
2110					2190				
2111					2191				
2112					2192				
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2160					2240				

15. REVISION HISTORY

Reversion	Content	Date
0.1	New SPEC	2015/04/22
0.2	Add bump information (p87~p89)	2015/07/29
0.3	Update bump information (p87~p89) Add Pad coordinates (p90~p101) Add revision history (p102)	2015/08/10
0.4	Modify VDDIO and VDDIO_IF voltage application range(p4)	2015/09/10
0.5	Add value of wiring resistance to each pin (p12)	2016/02/03
0.6	Add 480RGBx1280 resolution Modify power IC pump clock frequency value refers to EK79030 internal oscillation(p12)	2016/03/03