Display Future Ltd
www.displayfuture.com

LCD MODULE SPECIFICATION

Model: DF-GON0132WB-M1

This module uses ROHS materials

For customer acceptance

Customer		date
Approved		
Comments		

The standard product specification may change without prior notice in order to improve performance or quality. Please contact Display Future Ltd for updated specification and product status before design for the standard product or release of the order.	Revision	1.0
	Engineering	
	Date	01/06/18
	Our Reference	

REVISION RECORD

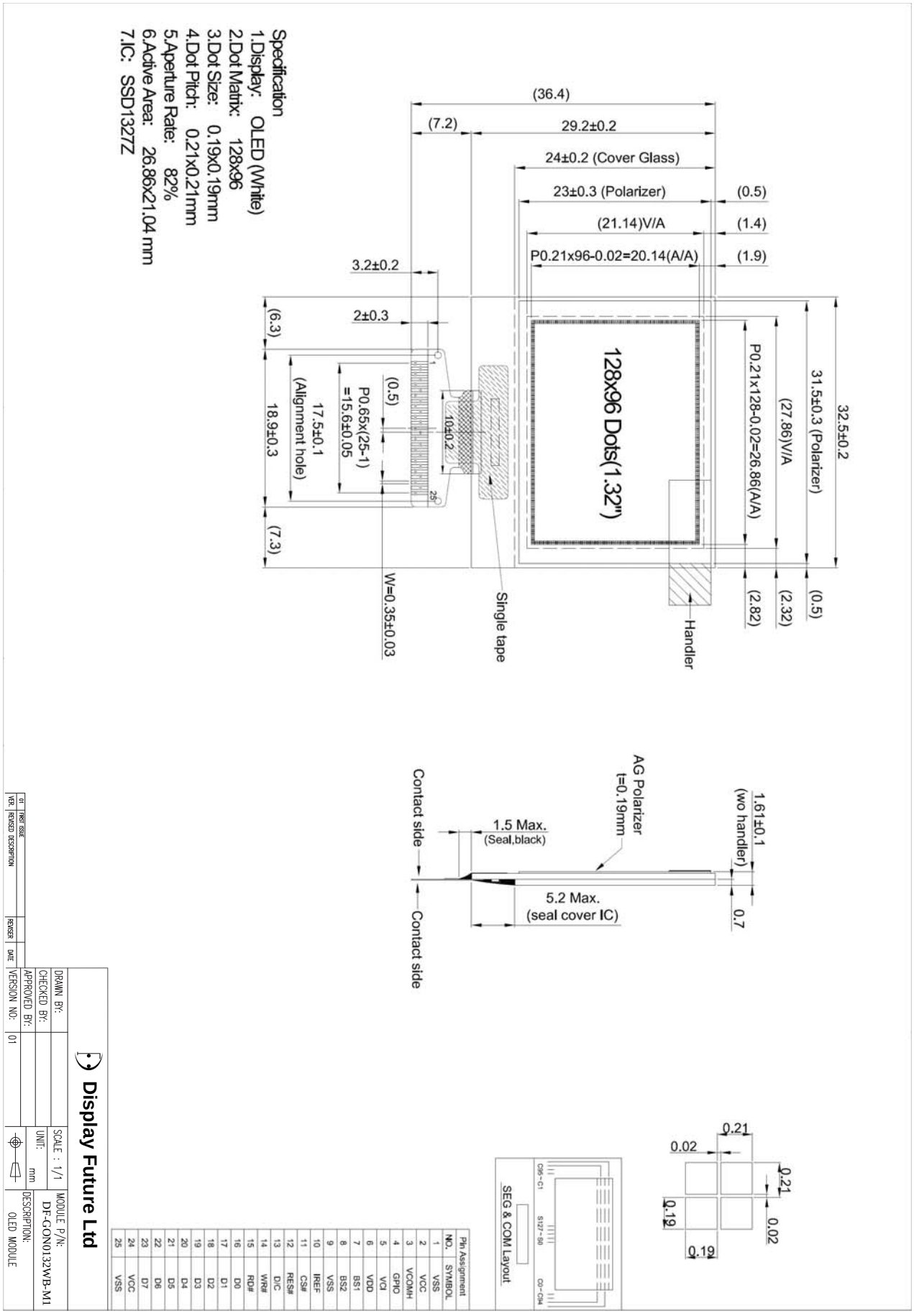
REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2018-05-25	First Release	

CONTENT

■ PHYSICAL DATA

No.	Items	Specification	Unit
1	Display Mode	Passive Matrix OLED	-
2	Display Color	Monochrome (White)	-
3	Duty	1/96	-
4	Resolution	128(H) x 96(V)	Pixel
5	Active Area	26.86 (W)x 20.14 (H)	mm^2
6	Outline Dimension	32.50 (W) x 29.20 (H) x 1.61(D)	mm^3
7	Pixel Pitch	0.21 (W) x 0.21 (H)	mm^2
8	Pixel Size	0.19 (W) x 0.19 (H)	mm^2
9	Driver IC	SSD1327	-
10	Interface	8-bit CPU, 4-wire SPI, I2C	-
11	Aperture Rate	82	%
12	Weight	3.10 ± 10%	g

■ EXTERNAL DIMENSIONS



■ ABSOLUTE MAXIMUM RATINGS

Items	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CI}	-0.3	4.0	V	
	V_{CC}	8	19.0	V	
Operating temperature	T_{OP}	-40	70	℃	2
Storage temperature	T_{ST}	-40	85	℃	2
Life time(100cd/m²)	-	13000	-	hour	3
Life time(80cd/m²)	-	16000	-	hour	4

Note:

1. Maximum ratings are those values beyond which damages to the OLED module may occur. The OLED functional operation should be restricted to the limits in the DC characteristics tables.
2. The defined temperature ranges do not include the polarizer.The maximum withstood temperature of the polarizer should be 80℃.

(A) Under Vcc=15.0V,Ta=25℃,50%RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(C) More command setting (Initial code), please see the application note.

3. Setting of 100 cd/m²:
   - Contrast setting : 0x5f
   - Frame rate : 105Hz
   - Duty setting : 1/96
4. Setting of 80 cd/m²:
   - Contrast setting : 0x4f
   - Frame rate : 105Hz
   - Duty setting : 1/96

■ ELECTRICAL CHARACTERISTICS

◆DC Characteristics

Items	Symbol	Conditions	Min	Typ.	Max	Unit
Driver power voltage	V_{CC}		14.5	15.0	15.5	V
Low voltage power supply	V_{CI}		2.6	-	3.5	V
High level input	V_{IH}	Iout=100uA	0.8 x V_{CI}	-	V_{CI}	V
Low level input	V_{IL}	Iout=100uA	0	-	0.2x V_{CI}	V
High level output	V_{OH}	Iout=100uA	0.9xV_{CI}	-	V_{CI}	V
Low level output	V_{OL}	Iout=100uA	0	-	0.1xV_{CI}	V
Vcc supply current	I_{CC}	V_{CI}=3.5V,Vcc=18V, Display ON, No panel attached, contrast=FF	Extrenal V_{DD}=2.5V	600	750	uA
			Internal V_{DD}=2.5V	600	750	uA
V_{CI} supply current	I_{CI}	V_{CI}=3.5V,Vcc=18V, Display ON, No panel attached, contrast=FF	Extrenal V_{DD}=2.5V	35	50	uA
			Internal V_{DD}=2.5V	95	120	uA
Segment output current setting V_{CC} =18.0V, IREF=10uA,	I_{SEG}	Contrast=FF	-	300	370	uA
		Contrast=AF	-	206	-	
		Contrast=7F	-	150	-	
		Contrast=3F	-	75	-	
		Contrast=1F	-	37.5	-	

◆AC Characteristics

1. 8080-Serial MCU Parallel Interface Timing Characteristics

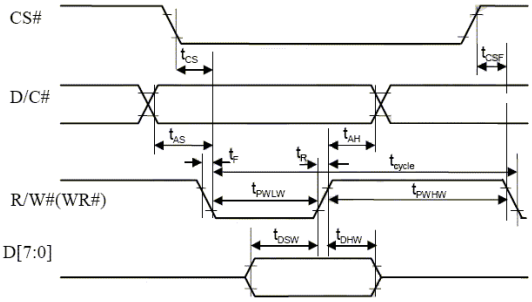
8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{CI} = 3.3V, T_A = 25°C)

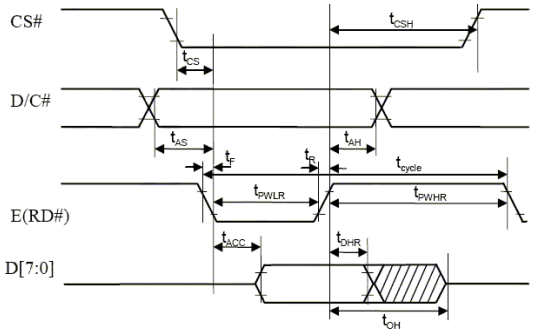
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics

Write cycle



Read cycle



2. Graphic Display Data Ram Address Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command " Set Re-map" A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 …D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:

- Command " Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 …D8191

GDDRAM address map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|									
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	

COM Outputs / Row Address (HEX)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command " Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Vertical Address Increment (A[2]=1)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 …D8191

GDDRAM address map 2

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]		D7936[3:0]	D7936[7:4]	D8064[3:0]	D8064[7:4]	(HEX)
COM1	01	D1[3:0]	D1[7:4]	D129[3:0]	D129[7:4]		D7937[3:0]	D7937[7:4]	D8065[3:0]	D8065[7:4]	
|	|									
COM126	7E	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]		D8062[3:0]	D8062[7:4]	D8190[3:0]	D8190[7:4]	
COM127	7F	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]		D8063[3:0]	D8063[7:4]	D8191[3:0]	D8191[7:4]	

COM Outputs / Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command " Set Re-map" A0h is set to:
  Enable Column Address Re-map (A[0]=1)
  Enable Nibble Re-map (A[1]=1)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 …D8191

GDDRAM address map 3

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		3F		3E			01		00	
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]
|	|									
COM126	7E	D8127[7:4]	D8127[3:0]	D8126[7:4]	D8126[3:0]		D8065[7:4]	D8065[3:0]	D8064[7:4]	D8064[3:0]
COM127	7F	D8191[7:4]	D8191[3:0]	D8190[7:4]	D8190[3:0]		D8129[7:4]	D8129[3:0]	D8128[7:4]	D8128[3:0]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=0)

Nibble re-map A[1]=1

The example in which the display start line registe r is set to 10h with the following condition:

- Command " Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 …D8191

GDDRAM address map 4

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM118	01	D1[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|									
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs
Column Address
(HEX)

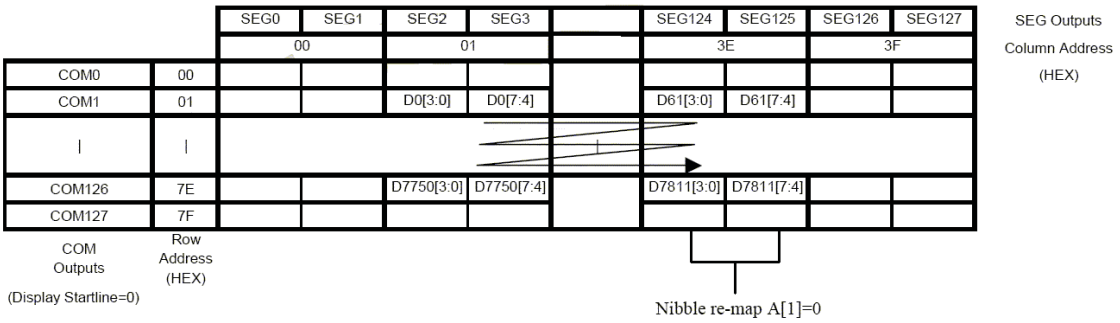
COM Outputs
Row Address (HEX)
(Display Startline=78H)

Nibble re-map A[1]=0

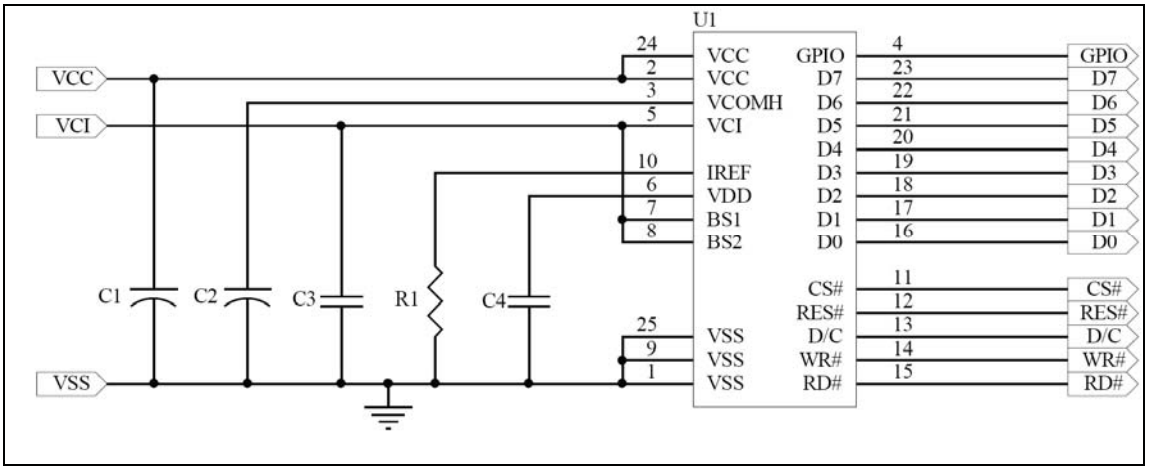
The GDDRAM map under the following condition:

- Command " Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 …D7811

GDDRAM address map 5



3. Application Circuit



Component:

C1, C2: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C3, C4: 1uF/16V(0603)

R1: 1M ohm (0603) 1%

This circuit is for 8080 8bits interface.

4. Command Table

Refer to IC Spec. : SSD1327

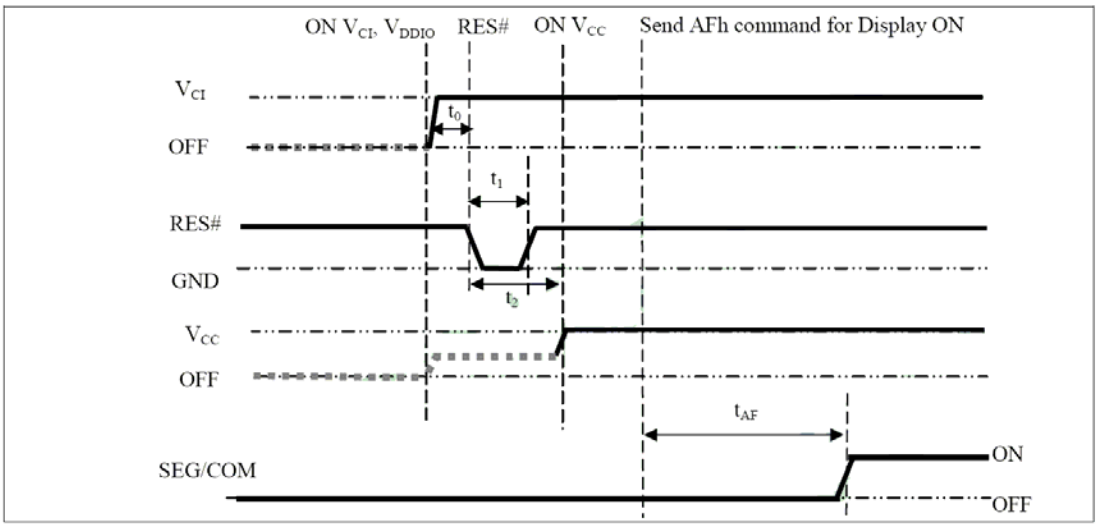
■ TIMING OF POWER SUPPLY

1. Power ON/OFF Sequence

Power ON sequence:

1. Power ON V_{CI}.
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1)[4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

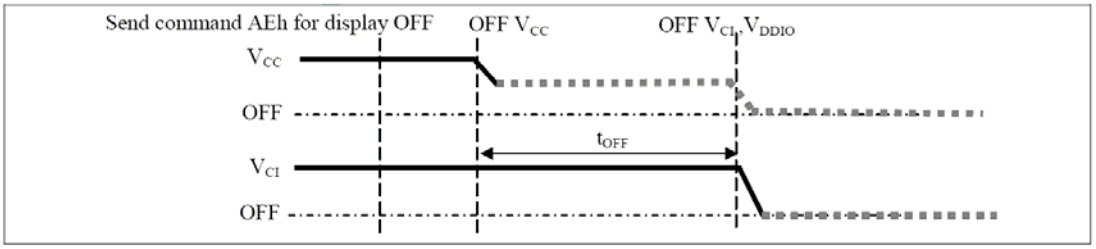
The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2], [3]
3. Wait for t_{OFF}. Power OFF V_{CI}.(where Minimum t_{OFF} =80ms[5], Typical t_{OFF} =100ms)

The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
(2) V_{CC} should be kept disable when it is OFF.
(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumsta nce.
(4) The register values are reset after t_1 .
(5) V_{CI} should not be Power OFF before V_{CC} Power OFF

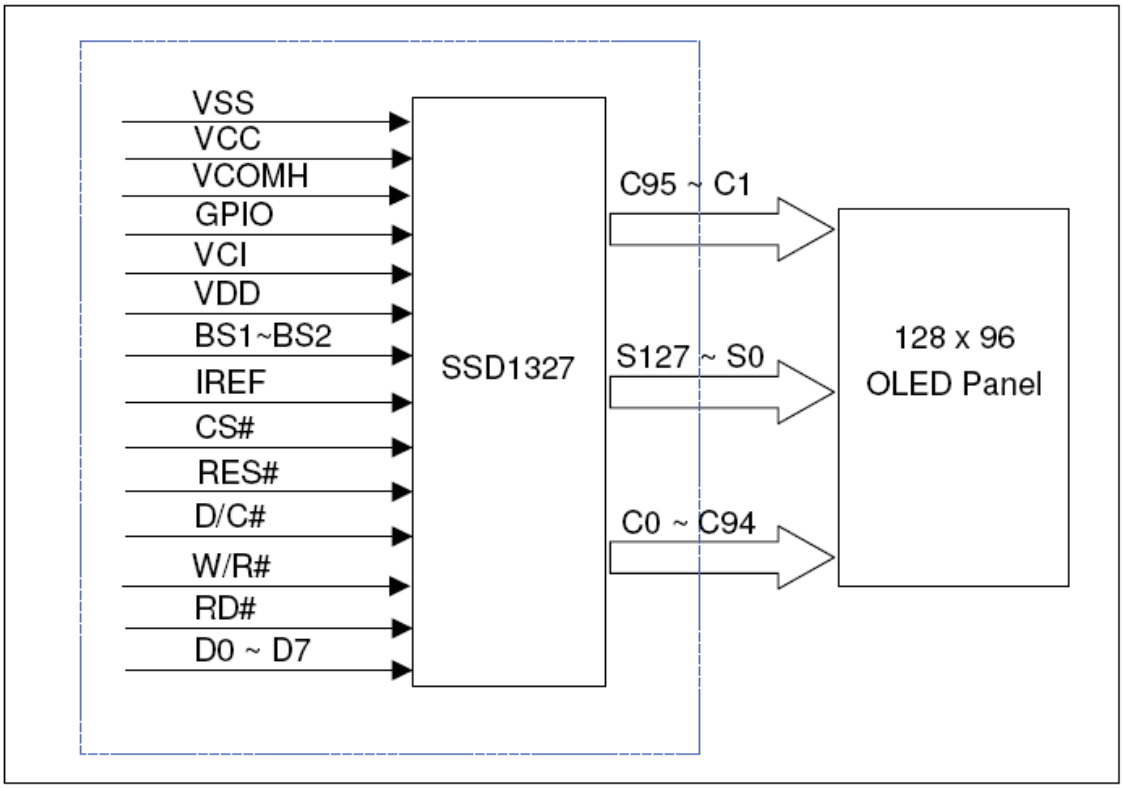
■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Pixel luminance		L	80	100	-	cd /m^2	Display average
Standby luminance		L	-	10	-	cd/m^2	
Response time		-	-	10	-	μs	
Normal mode current consumption		-	-	25.5	27.5	mA	All pixels on
Standby mode current consumption		-	-	1.0	2.0	mA	Standby mode 10% pixel on
Normal mode power consumption		-	-	382.5	412.5	mW	All pixels on
Standby mode power consumption		-	-	15.0	30.0	mW	Standby mode 10% pixel on
Color Coordinate	White	CIE x	0.24	0.28	0.32	CIE1931	Darkroom
		CIE y	0.28	0.32	0.36		
Contrast Ratio*		Cr	2000:1	-	-		Darkroom
Viewing Angle Uniformity		△ θ	160	-	-	Degree	-

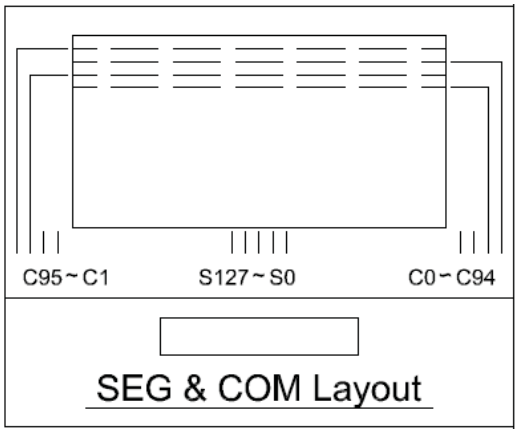
1. Normal mode condition:
   - Driving Voltage : 15.0V
   - Contrast setting : 0 x 5f
   - Frame rate : 105Hz
   - Duty setting : 1/96
2. Standby mode condition:
   - Driving Voltage : 15.0V
   - Contrast setting : 0 x 0a
   - Frame rate : 105Hz
   - Duty setting : 1/96

■ INTERFACE PIN CONNECTIONS

1. Function Block Diagram



2. Panel Layout Diagram



3. PIN Assignments

PIN NAME	PIN NO	DESCRIPTION
VSS	1	Ground
VCC	2	Power supply for analog circuit
VCOMH	3	Com Voltage Output. A capacitor should be connected between this pin and V_{SS}
GPIO	4	General I/O port.
VCI	5	Power supply for logic circuit
VDD	6	A capacitor should be connected between this pin and V_{SS}
BS1	7	Interface selection input.
BS2	8	
VSS	9	Ground.
IREF	10	Reference current input pin. A resistor should be connected between this pin and V_{SS}
CS#	11	Chip select input.
RES#	12	Reset signal input. When it’ s low, initialization of SSD1327 is executed.
D/C	13	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
WR#	14	This pin is used to receive the write data signal.
RD#	15	This pin is used to receive the read data signal.
D0	16	Data bus (for parallel interface)
D1	17	
D2	18	
D3	19	
D4	20	
D5	21	
D6	22	
D7	23	
VCC	24	Power supply for analog circuit.
VSS	25	Ground.

■ RELIABILITY TESTS

<table>
<tr><th colspan="2">Item</th><th>Condition</th><th>Criterion</th></tr>
<tr><td colspan="2">High Temperature Storage
(HTS)</td><td>85±2℃, 240 hours</td><td rowspan="6">1. After testing, the function test is ok.
2. After testing, no addition to the defect.
3. After testing, the change of luminance should be within +/- 50% of initial value.
4. After testing, the change for the mono and area color must be within (+/-0.02, +/-0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.
5. After testing, the change of total current consumption should be within +/- 50% of initial value.</td></tr>
<tr><td colspan="2">High Temperature Operating
(HTO)</td><td>70±2℃, 120 hours</td></tr>
<tr><td colspan="2">Low Temperature Storage
(LTS)</td><td>-40±2℃, 240 hours</td></tr>
<tr><td colspan="2">Low Temperature Operating
(LTO)</td><td>-40±2℃, 120 hours</td></tr>
<tr><td colspan="2">High Temperature / High Humidity Storage
(HTHHS)</td><td>65±3℃, 90%±3%RH, 120 hours</td></tr>
<tr><td colspan="2">Thermal Shock (Non-operation)
(TS)</td><td>-40±2℃ ~ 25℃ ~ 85±2℃
(30min) (5min) (30min)
100cycles</td></tr>
<tr><td>Vibration
(Packing)</td><td>Frequency:5~55Hz,0.5G
Scan rate: 1 oct/min
Time: 2 hrs/axis
Test axis: X,Y,Z.</td><td colspan="2" rowspan="2">1. One box for each test.
2. No addition to the cosmetic and the electrical defects.</td></tr>
<tr><td>Drop
(Packing)</td><td>Height : 120cm, each time for 6 sides, 3 edges, 1 angle</td></tr>
</table>

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).

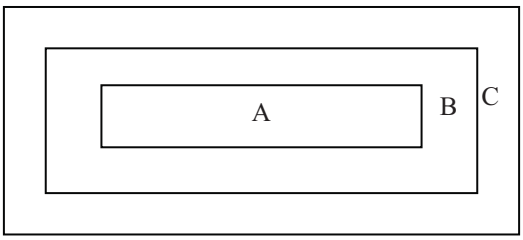
■OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1： 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.
2 Minor defect : The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area

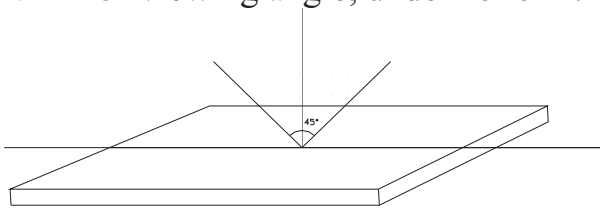
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



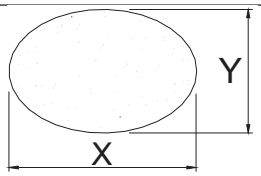
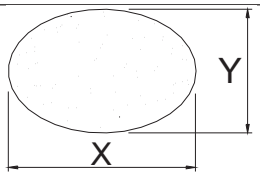
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

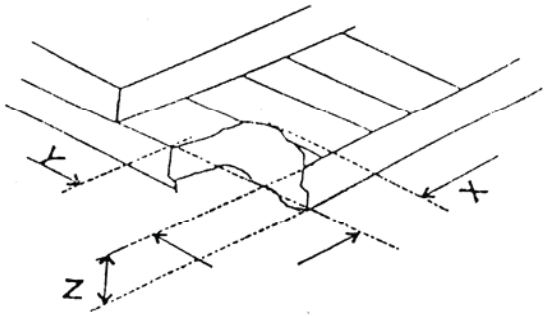
◆Inspection Criteria

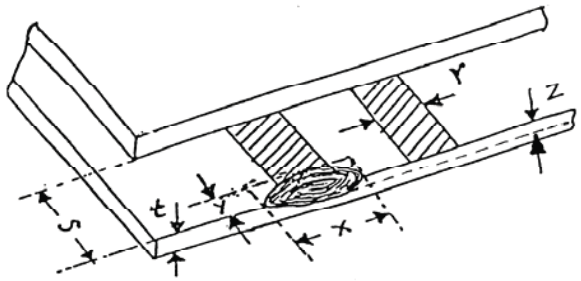
1 Major defect : AQL= 0.65

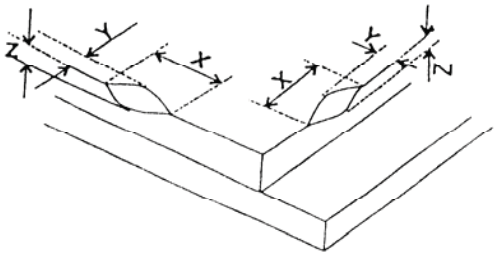
Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td colspan="2"></td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.10</td><td colspan="2">Ignored</td></tr>
<tr><td>0.10＜Φ≦0.15</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.15＜Φ≦0. 20</td><td>1</td></tr>
<tr><td>0.20＜Φ</td><td>0</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs.</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignore</td></tr>
<tr><td>5.0＜L≦10.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦5.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.50＜Φ≦0.80</td><td>1</td></tr>
<tr><td>0.80＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 

(mm)<table><tr><td>x</td><td>≤ 2.0</td></tr><tr><td>y</td><td>≤ S</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 

(mm)<table><tr><td>x</td><td>≤ a / 2</td></tr><tr><td>y</td><td>≤ s / 3</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 

(mm)<table><tr><td>x</td><td>≤ a / 5</td></tr><tr><td>y</td><td>≤ 1.0</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: V_{DD}(logic voltage) → V_{CC} (driving voltage), and power off sequence: V_{CC} (driving voltage) → V_{DD} (logic voltage).
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC

controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. If the module can not be used up in 3 months,make sure to seal the module in the vacuum bag with dessicant.
2. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
3. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
4. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless agreed between Display Future and customer, Display Future will replace or repair any of its OLED modules which are found to be functionally defective when inspected in accordance with Display Future OLED acceptance standards(copies available upon request)for a period of one year from date of production. Cosmetic/visual defects must be returned to Display Future manufacturing partner within 90 days of shipment. Confirmation of such date shall be based on data code on product. The warranty liability is limited to repair and/or replacement on the terms set forth above. Display Future will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

No warranty can be granted if the precautions stated above have been disregarded.The typical examples of violations are:

-Broken OLED glass.
-PCB eyelet is damaged or modified.
-PCB conductors damaged.
-Circuit modified in any way,including addition of components.
-PCB tampered with by grinding,engraving or painting varnish.
-Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement.Modules must be returned with sufficient description of the failures or defects.Any connectors or cable installed by the customer must be removed completely.

■ PRIOR CONSULT MATTER

1. ① For Display Future standard products,we keep the right to change material,process ... for the product property without notice on our customer.
   ② For OEM products,if any change needed which may affect the product property,we will consult with our customer in advance.
2. If you have special requirement about reliability condition,please let us know before you start the test on our samples.