SA3086

80 CH SEGMENT /COMMON DRIVER FOR DOT MATRIX LCD

Ver 2.1 1 July, 2000

INTRODUCTION

The SA3086 is an LCD driver LSI which is fabricated by low power CMOS high voltage process technology. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

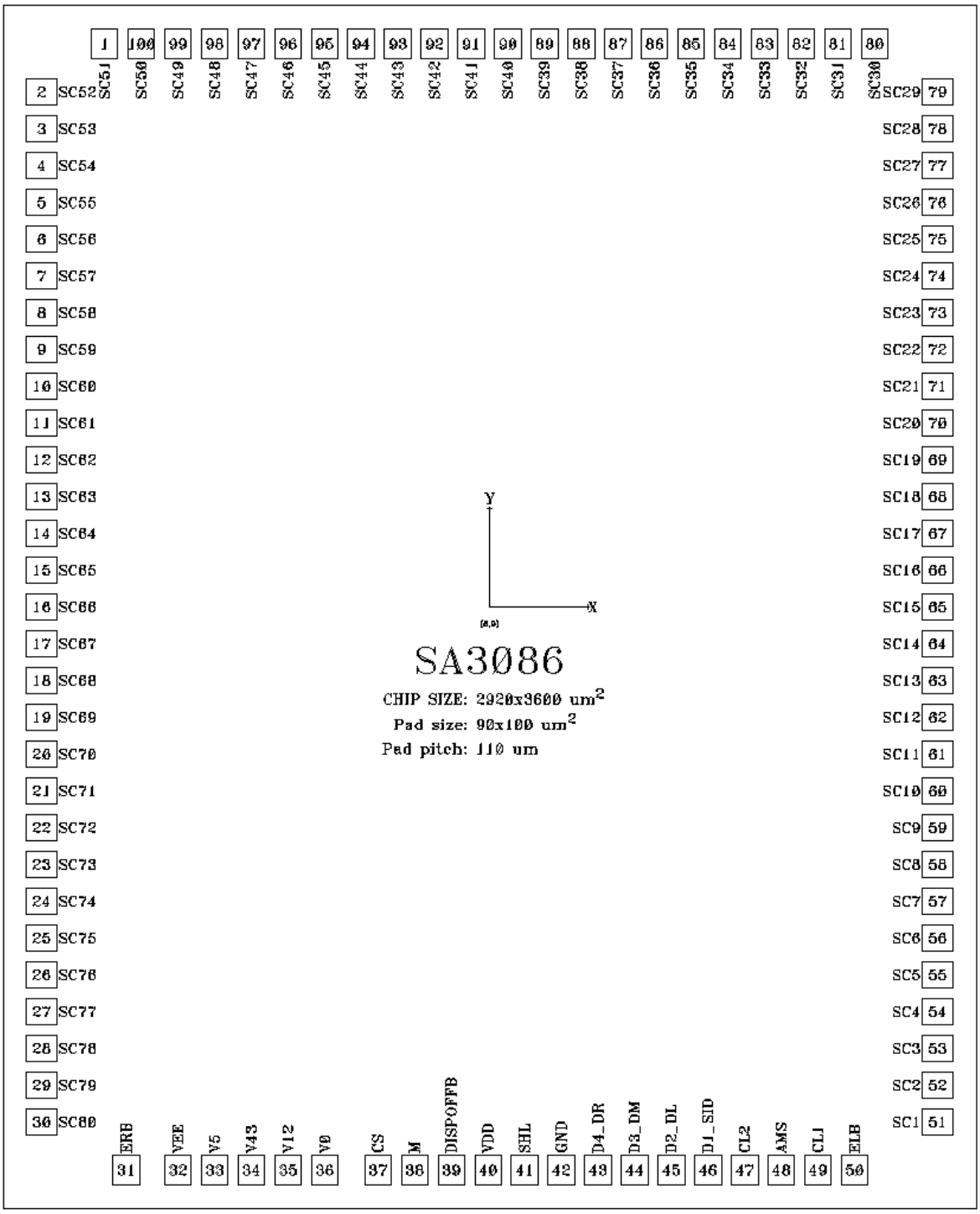
FEATURES

- Power supply voltage: + 5V ± 10 %, + 3V ± 10%
- Supply voltage for display: 6 to 28 V (V_{DD}- V_{EE})
- 4-bit parallel / 1-bit serial data processing (in segment mode)
- Single mode operation / dual mode operation (in common mode)
- Power down function (in segment mode)
- Applicable LCD duty 1/64 – 1/256
- Interface

DRIVERS	
COM (cascade)	SEG (cascade)
SA3086	SA3086

- High voltage CMOS process
- Bare die

PAD DIAGRAM


SA3086
CHIP SIZE: 2920x3600 um2
Pad size: 90x100 um2
Pad pitch: 110 um
Y
X
(0,0)
1 SC51
100 SC50
99 SC49
98 SC48
97 SC47
96 SC46
95 SC45
94 SC44
93 SC43
92 SC42
91 SC41
90 SC40
89 SC39
88 SC38
87 SC37
86 SC36
85 SC35
84 SC34
83 SC33
82 SC32
81 SC31
80 SC30
2 SC52
3 SC53
4 SC54
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9 SC59
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11 SC61
12 SC62
13 SC63
14 SC64
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24 SC74
25 SC75
26 SC76
27 SC77
28 SC78
29 SC79
30 SC80
SC29 79
SC28 78
SC27 77
SC26 76
SC25 75
SC24 74
SC23 73
SC22 72
SC21 71
SC20 70
SC19 69
SC18 68
SC17 67
SC16 66
SC15 65
SC14 64
SC13 63
SC12 62
SC11 61
SC10 60
SC9 59
SC8 58
SC7 57
SC6 56
SC5 55
SC4 54
SC3 53
SC2 52
SC1 51
ERB 31
VEE 32
V5 33
V43 34
V12 35
V0 36
CS 37
M 38
DISPOFFB 39
VDD 40
SHL 41
GND 42
D4_DR 43
D3_DM 44
D2_DL 45
D1_SID 46
CL2 47
AMS 48
CLI 49
ELB 50

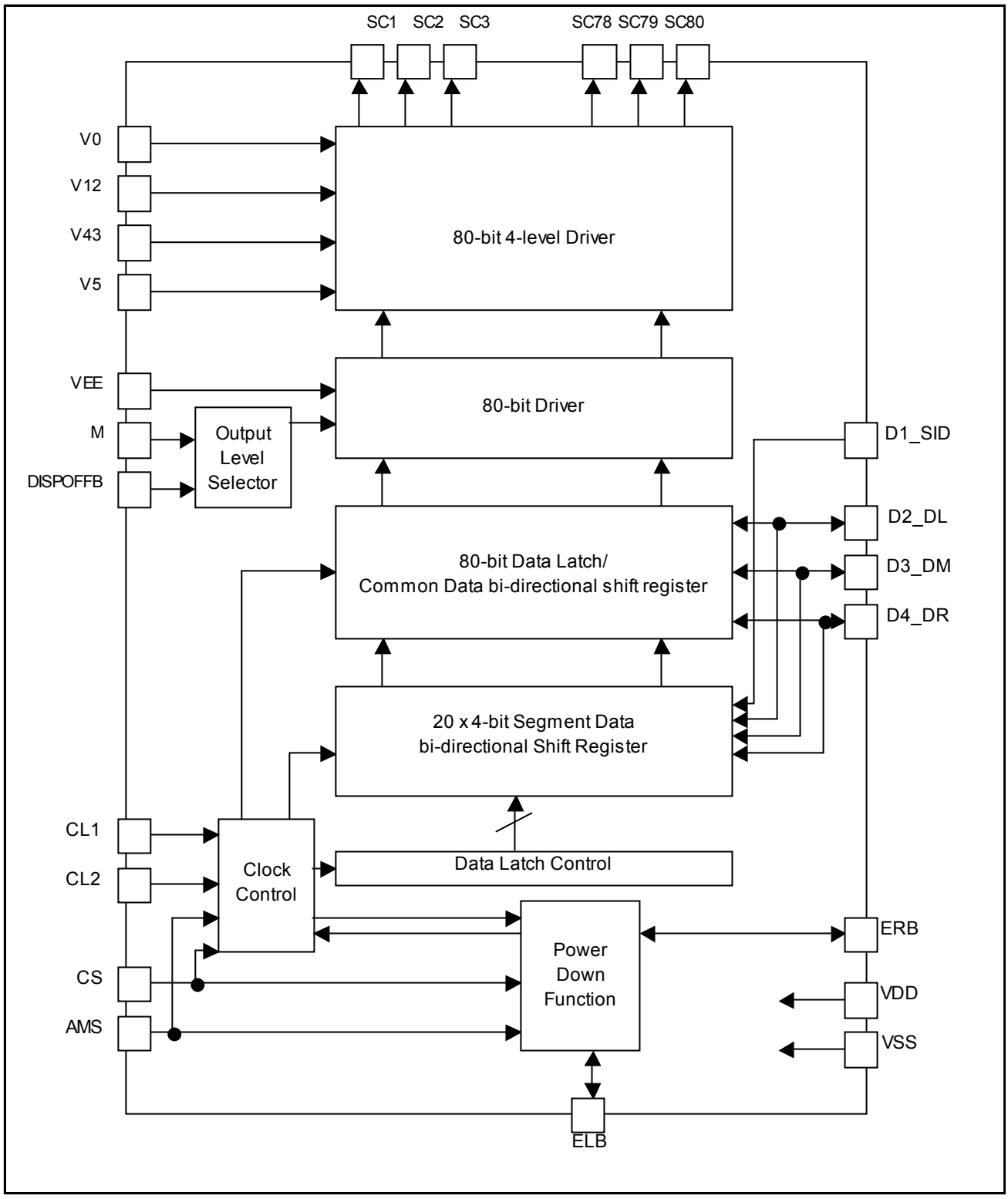
PAD LOCATION

No.	NAME	X	Y
1	SC51	-1155.00	1684.00
2	SC52	-1344.00	1540.00
3	SC53	-1344.00	1430.00
4	SC54	-1344.00	1320.00
5	SC55	-1344.00	1210.00
6	SC56	-1344.00	1100.00
7	SC57	-1344.00	990.00
8	SC58	-1344.00	880.00
9	SC59	-1344.00	770.00
10	SC60	-1344.00	660.00
11	SC61	-1344.00	550.00
12	SC62	-1344.00	440.00
13	SC63	-1344.00	330.00
14	SC64	-1344.00	220.00
15	SC65	-1344.00	110.00
16	SC66	-1344.00	0.00
17	SC67	-1344.00	-110.00
18	SC68	-1344.00	-220.00
19	SC69	-1344.00	-330.00
20	SC70	-1344.00	-440.00
21	SC71	-1344.00	-550.00
22	SC72	-1344.00	-660.00
23	SC73	-1344.00	-770.00
24	SC74	-1344.00	-880.00
25	SC75	-1344.00	-990.00
26	SC76	-1344.00	-1100.00
27	SC77	-1344.00	-1210.00
28	SC78	-1344.00	-1320.00
29	SC79	-1344.00	-1430.00
30	SC80	-1344.00	-1540.00
31	ERB	-1090.00	-1684.00
32	VEE	-934.40	-1684.00
33	V5	-824.40	-1684.00
34	V43	-714.40	-1684.00

No.	NAME	Y	Y
35	V12	-604.40	-1684.00
36	V0	-494.40	-1684.00
37	CS	-334.70	-1684.00
38	M	-224.70	-1684.00
39	DISPOFFB	-114.70	-1684.00
40	VDD	-4.70	-1684.00
41	SHL	105.30	-1684.00
42	GND	215.30	-1684.00
43	D4 DR	325.30	-1684.00
44	D3 DM	435.30	-1684.00
45	D2 DL	545.30	-1684.00
46	DI SID	655.30	-1684.00
47	CL2	765.30	-1684.00
48	AMS	875.30	-1684.00
49	CL1	985.30	-1684.00
50	ELB	1095.30	-1684.00
51	SC1	1344.00	-1540.00
52	SC2	1344.00	-1430.00
53	SC3	1344.00	-1320.00
54	SC4	1344.00	-1210.00
55	SC5	1344.00	-1100.00
56	SC6	1344.00	-990.00
57	SC7	1344.00	-880.00
58	SC8	1344.00	-770.00
59	SC9	1344.00	-660.00
60	SC10	1344.00	-550.00
61	SC11	1344.00	-440.00
62	SC12	1344.00	-330.00
63	SCI'3	1344.00	-220.00
64	SC14	1344.00	-110.00
65	SC15	1344.00	0.00
66	SC16	1344.00	110.00
67	SC17	1344.00	220.00
68	SC18	1344.00	330.00

No.	NAME	X	Y
69	SC19	1344.00	440.00
70	SC20	1344.00	550.00
71	SC21	1344.00	660.00
72	SC22	1344.00	770.00
73	SC23	1344.00	880.00
74	SC24	1344.00	990.00
75	SC25	1344.00	1100.00
76	SC26	1344.00	1210.00
77	SC27	1344.00	1320.00
78	SC28	1344.00	1430.00
79	SC29	1344.00	1540.00
80	SC30	1155.00	1684.00
81	SC31	1045.00	1684.00
82	SC32	935.00	1.684.00
83	SC33	825.00	1684.00
84	SC34	715.00	1684.00
85	SC35	605.00	1684.00
86	SC36	495.00	1684.00
87	SC37	385.00	1684.00
88	SC38	275.00	1684.00
89	SC39	165.00	1684.00
90	SC40	55.00	1684.00
91	SC41	-55.00	1684.00
92	SC42	-165.00	1684.00
93	SC43	-275.00	1684.00
94	SC44	-385.00	1684.00
95	SC45	-495.00	1684.00
96	SC46	-605.00	1684.00
97	SC47	-715.00	1684.00
98	SC48	-825.00	1684.00
99	SC49	-935.00	1684.00
100	SC50	-1045.00	1684.00

BLOCK DIAGRAM



BLOCK DESCRIPTION

Name	Function	COM/SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In case of common driver application, this block generates shift clock (LCK) for the common data bidirectional shift register.	COM/SEG
Data latch control	Determines the direction of segment data shift, and input data of each bidirectional shift register. In case of 4-bit segment data parallel transfer mode, data is shifted by 4-bit unit. In case of common driver application mode, data is transferred to the common data shift register directly, so this block is not work.	SEG
Power down function	Controls the clock enable state of current driver according to the input value of enable pin (ELB or ERB). If enable input value is "Low", every clock of the current driver is enabled and the clock control block works. But if enable input is "High", current driver is disabled and the input data value has no effect to the output level. So power consumption can be lowered.	SEG
Output level selector	Control the output voltage level according to the input control pin (M and DISPOFFB) (refer to PIN DESCRIPTION).	COM/SEG
20 x 4-bit segment data bidirectional shift register	Stores output data value by shifting the input values. When 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in case of 4-bit parallel transfer mode application, only 20 clocks makes the role. When common driver application mode, this block is not work.	SEG
80-bit data latch / common data bidirectional shift register	In case of segment driver application, the data from the 20x4-bit segment data shift register are latched for segment driver output. When single-type common driver application, 1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. When dual-type common application mode, 80-bit register are divided by two blocks and controlled independently (refer to NOTES).	COM/SEG
80-bit level shifter	Voltage level shifter block for high voltage part. the inputs of this block are logical voltage level and the outputs of this block are high voltage level value. And this value is input to the driver.	COM/SEG
80-bit 4-level driver	Selects the output voltage level according to the M and latched data value. If the data value is "High" the driver output is selected voltage level (V0 or V5), and in the reverse case the driver output value is non-selected level (V12 or V43). In case of segment driver application, non-selected output value is V2 or V3. And when common driver application, this value becomes V1 or V4.	COM/SEG

PIN DESCRIPTION

<table>
<tr><th>Pin (no)</th><th>Input output</th><th>Name</th><th>Description</th><th>Inter-face</th></tr>
<tr><td>V_{DD} (40)</td><td rowspan="3">Power</td><td rowspan="2">Operating Voltage</td><td>Logical "High" input port (+5V+ 10%, +3V+ 10%)</td><td rowspan="3">Power</td></tr>
<tr><td>V_{SS} (42)</td><td>0V (GND)</td></tr>
<tr><td>V_{EE} (32)</td><td>Driver Supply Voltage</td><td>Logical "Low" for high voltage part</td></tr>
<tr><td>VO,V12, V43 V5 (33-36)</td><td>Input</td><td>LCD driver output voltage level</td><td>Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source (refer to NOTE 2).</td><td>Power</td></tr>
<tr><td>SC1 ~ SC80 (1-30, 51-100)</td><td>Output</td><td>LCD driver output</td><td>Display data output pin which corresponds to the respective latch contents. One of V_0, V_{12}, V_{34} and V_5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to NOTE 1).</td><td>LCD</td></tr>
<tr><td>CL2 (47)</td><td>Input</td><td>Data shift clock</td><td>Clock pulse input for the bidirectional shift register.
• In case of segment driver application, the data is shifted to 20 x 4-bit segment data shift register at the falling edge of this clock pulse. The clock pulse, which was input when the enable bit (ELB/ERB) is not active condition, is invalid.
• In case of common driver application, the data is shifted to 80-bit common data bidirectional shift register by the CL1 clock. So this clock pin is not used (Open or connect this to VDD)</td><td>Controller</td></tr>
<tr><td>M(38)</td><td>Input</td><td>Alternate signal for LCD driver output</td><td>Alternate signal input pin for LCD driving. Normal frame inversion signal is input to this pin.</td><td>Controller</td></tr>
<tr><td>CL1(49)</td><td>Input</td><td>Data latch clock</td><td>• In case of segment driver application, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block. • In case of common driver application, CL1 is used as shifting clock of common output data.</td><td>Controller</td></tr>
<tr><td>DISPOFF B (39)</td><td>Input</td><td>Display oft control</td><td>Control input pin to fix the driver output (SC1™SC80) to VO level, during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.</td><td>Controller</td></tr>
<tr><td>CS (37)</td><td>Input</td><td>COM/SEG mode control</td><td>When CS = "Low", SA3086 is used as 80-bit segment driver.
When CS = "High", SA3086 is set to 80-bit common driver.</td><td>-</td></tr>
<tr><td>AMS (48)</td><td>Input</td><td>Application mode select</td><td>According to the input value of the AMS and the CS pin, application mode of SA3086 is different as below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application mode</th><th>COM/SEG</th></tr>
<tr><td>L</td><td>L</td><td>4-bit parallel interface mode</td><td rowspan="2">SEG</td></tr>
<tr><td>L</td><td>H</td><td>1-bit serial interface mode</td></tr>
<tr><td>H</td><td>L</td><td>single-type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>H</td><td>H</td><td>dual-type application mode</td></tr>
</table></td><td>Controller</td></tr>
</table>

PIN DESCRIPTION (continued)

<table>
<tr><th>Pin (NO)</th><th>Input/ Output</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr><td>D1 SID, D2DL, D3DM, D4 DR (43-46)</td><td>Input/ Output</td><td>Display data input / serial input data / left, right data input /output</td><td>• In case of segment driver application, these pins are used as 4-bit data input pin (when 4-bit parallel interface mode : AMS = "Low"), or D1SID is used as serial data input pin and other pins are not used. (Open or connect this to VDD) (when 1-bit serial interface mode : AMS = "High"). • In case of common driver application, the data are shifted from D2DL (D4DR) to D4DR (D2DL), when single-type application mode (AMS = "Low"). In dual-type application case, the data are shifted from D2DL and D3DM (D4DR and D3DM) to D4-DR (D2 DL). In each case the direction of data shift is determined by SHL input, (refer to NOTE 3, NOTE4)</td><td>controller</td></tr>
<tr><td>SHL(41)</td><td>Input</td><td>Shift direction control</td><td>When SHL = "Low", data is shifted from left to right When SHL = "High", the direction is reversed, (refer to NOTE 3)</td><td>-</td></tr>
<tr><td>ELB,ERB (50,31)</td><td>Input/ Output</td><td>Enable data input/output</td><td>• In case of segment driver application, only when enable input (ELB or ERB) is "Low", the internal operation is enabled (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. (refer to NOTE 4)
<table>
<tr><th rowspan="2">SHL</th><th colspan="2">SEGMENT DRIVER</th></tr>
<tr><th>ELB</th><th>ERB</th></tr>
<tr><td>L</td><td>Output (last open)</td><td>Input (first VSS)</td></tr>
<tr><td>H</td><td>Input (last VSS)</td><td>Output (first open)</td></tr>
</table>
• In case of common driver application, power down function is not used. (Open)</td><td>-</td></tr>
</table>

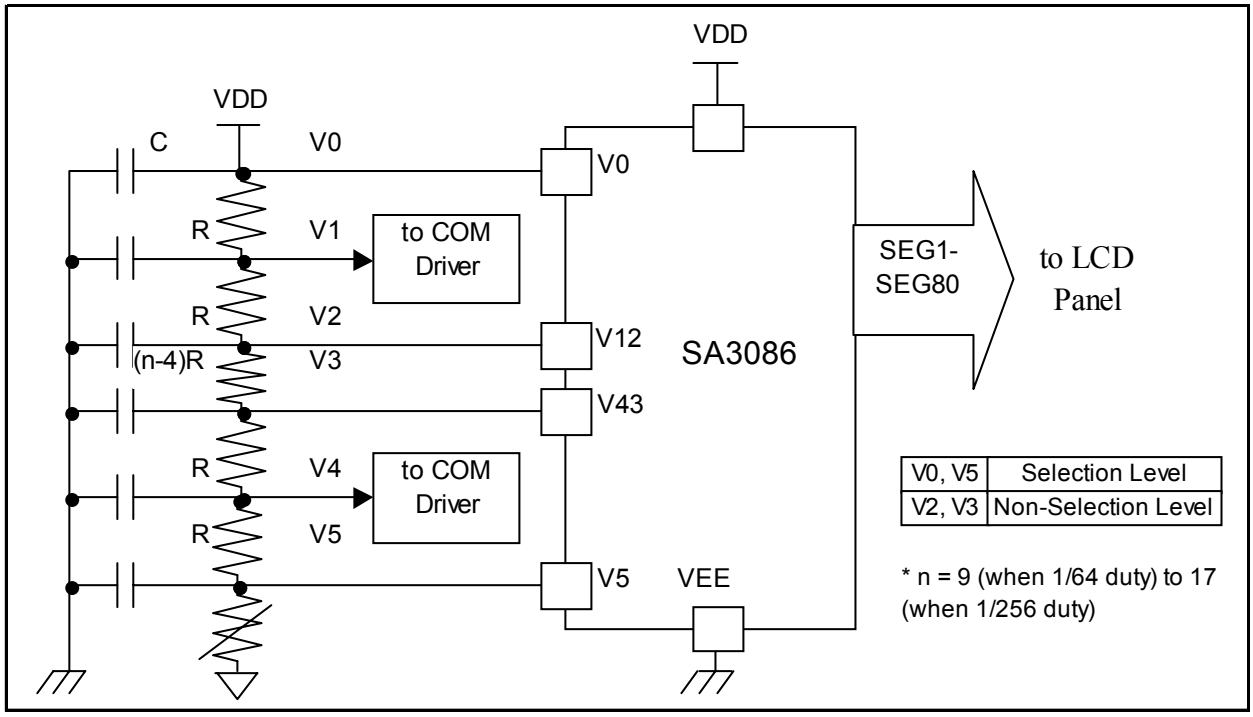
NOTE 1. Output level control

X: Don't care

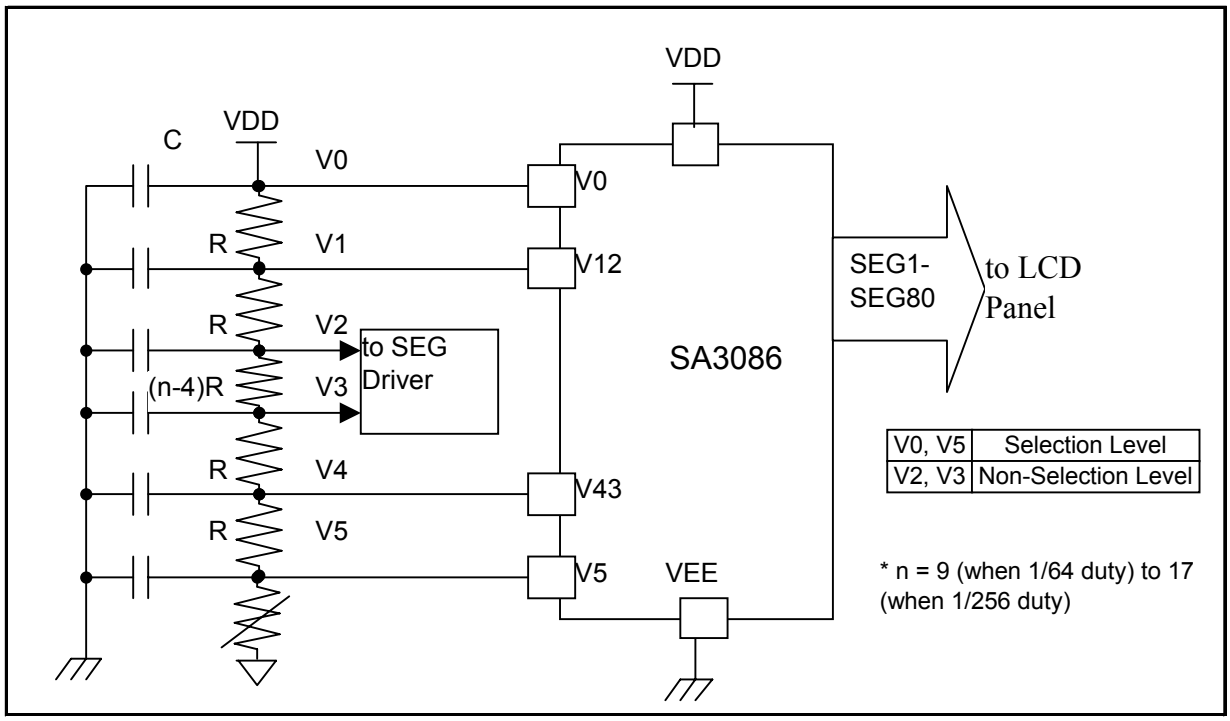
M	Latched data	DISPOFFB	Output level (SC1 ~ SC80)	
			SEG Mode	COM Mode
L	L	H	V12(V2)	V12(V1)
L	H	H	VO	V5
H	L	H	V43(V3)	V43(V4)
H	H	H	V5	VO
X	X	L	VO	VO

NOTE 2. LCD Driving Voltage Application Circuit

(1) Segment driver application (CS = “Low”)

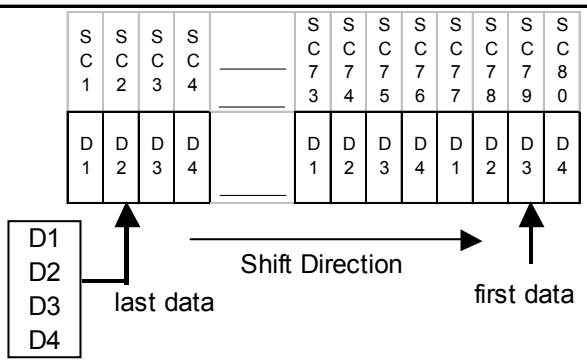
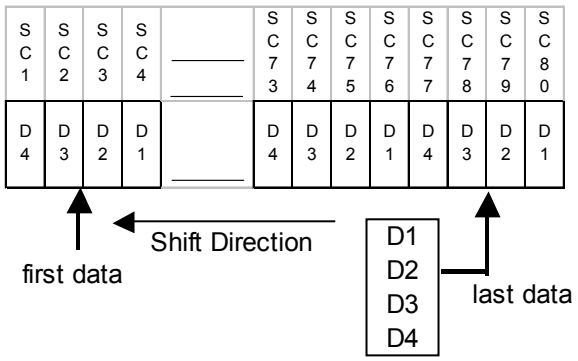
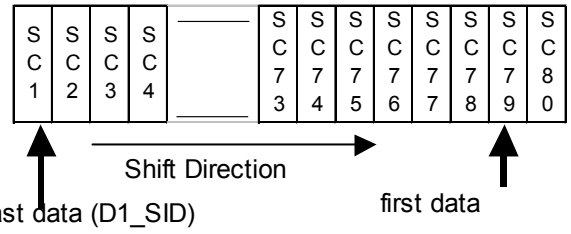
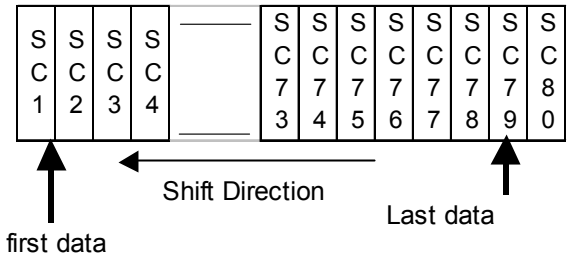


(2) Common driver application (CS= “High”)

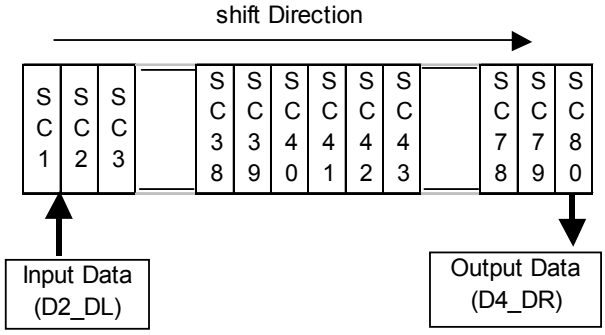
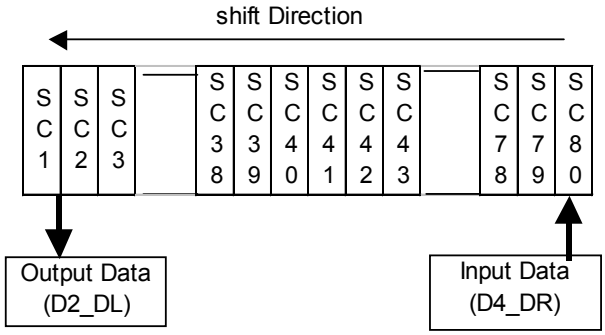
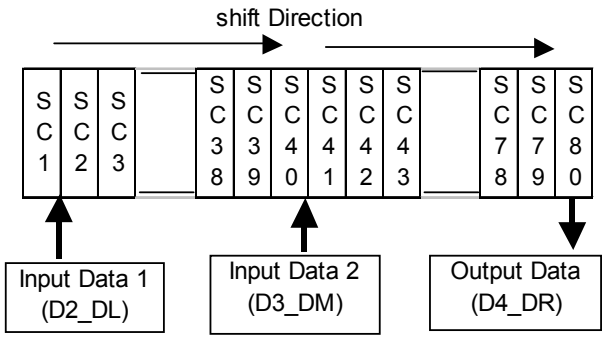
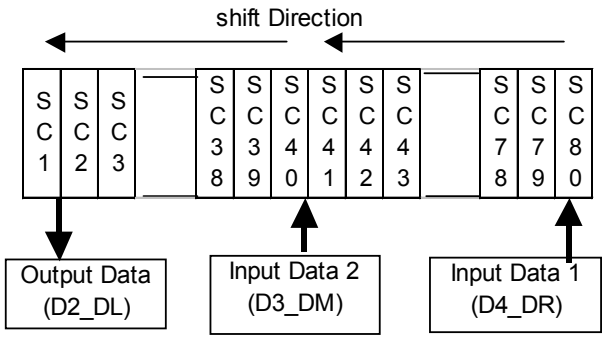


NOTE 3. Data Shift Direction according to Control Signals

(1) When CS = “Low” (segment driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	4-Bit Parallel Data Transfer Mode (SEG)		D1_SID, D2_DL, D3_DM D4_DR
	H			D1_SID
H	L	1-Bit Serial Data Transfer Mode (SEG)		
	H			

(2) When CS = “High” (common driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL, D3_DM
	H			D4_DR, D3_DM

NOTE 4. Usage of Data Pins

COM / SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS ="Low")	4-bit paralle interface mode (AMS = "Low")	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1-bit serial interface mode (AMS = "Low")	X	SID (input)	Connect to VDD		
COM (CS = "High")	single-type application mode (AMS = "Low")	L	open	DL (input)	Open	DR (output)
		H		DL (output)		DR (input)
	dual-type application mode (AMS = "High")	L	open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3 - +7.0	V
Driver supply voltage	V_{LCD}	0 - +30	
Input voltage	V_{IN}	-0.3 - V_{DD} +0.3	
Operating temperature	Topr	-30 - +85	°C
Storage temperature	Tstg	-55 - +150	

* **NOTE:** Voltage greater than above may do damage to the circuit.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(1) Segment Driver Application

(V_{SS} = 0V, Ta = - 30- +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating Voltage1	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	$V_{IN} = V_{DD} - V_{EE}$		6	-	28	
Input voltage (1)	V_{IH}	-		$0.8V_{DD}$	-	V_{DD}	
	V_{IL}	-		0	-	$0.2V_{DD}$	
Output voltage (2)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	$V_{IN} = V_{DD}$ to V_{SS}		-10	-	10	µA
Input leakage current 2 (3)	I_{IL2}	$V_{IN} = V_{DD}$ to V_{EE}		-25	-	25	
On resistance (4)	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current (5)	I_{STBY}	f_{CL1} = 32kHz M = V_{ss}	V_{ss} pin	-	-	100	µA
	I_{DD}	f_{CL1} = 32kHz f_M = 80 Hz	V_{DD} = 5V	-	-	5	mA
			V_{DD} = 3V	-	-	2	
	I_{EE}		V_{DD} = 5V	-	-	500	µA

NOTES:

1. Applied to CL1, CL2, ELB, ERB, D1_SID – D4_DR, SHL, DISPOFFB, M, CS, AMS pin
2. ELB, ERB pin
3. V0, V12, V43, V5 pin
4. $V_{LCD} = V_{DD} - V_{EE}$, V0 = V_{DD} = 5V, 5V= V_{EE} = -23 V
   V12 = V_{DD}-2/n(V_{LCD}), V43 = V_{EE}+2/n(V_{LCD}), n = 17 (1/256 duty, 1/17 bias)
5. V0 = V_{DD}, V12 = 1.71V(V_{DD} = 5V) or -0.06V (V_{DD} = 3V),
   V43 = -19.71 V(V_{DD} = 5V) or -19.94V (V_{DD} = 3V), V5 = V_{EE} = -23V, no-load condition (1/256 duty, 1/17 bias)
   4-bit parallel interface mode
   I_{STBY} : V_{DD} = 5V, f_{CL2} = 5.12MHz, SHL = V_{SS}, DISPOFFB = V_{DD}, M = V_{SS}, display data pattern = 0000
   I_{DD} : V_{DD} = 3V, f_{CL2} = 4MHz, display data pattern = 0101
   V_{DD} = 5 V, f_{CL2} = 5.12MHz, display data pattern = 0101
   I_{EE} : V_{DD} = 5V, f_{CL2} = 5.12MHz, display data pattern = 0101, V_{EE} pin

DC CHARACTERISTICS (CONTINUED)

(2) Common Driver Application

(V_{SS} = 0V, Ta = -30 - +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating Voltage1	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = V_{DD} - V_{EE}		6	-	28	
Input voltage (1)	V_{IH}	-		0.8V_{DD}	-	V_{DD}	
	V_{IL}	-		0	-	0.2V_{DD}	
Output voltage (3)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4Ma		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN} = V_{DD} to V_{SS}		-10	-	10	µA
Input leakage current 2 (2)	I_{IL2}	V_{IN} = 0V, V_{DD} = 5V (PULL UP)		-50	-125	-250	
Input leakage current 3 (4)	I_{IL3}	V_{IN} = V_{DD} to V_{SS}		-25	-	25	
On resistance (5)	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current (6)	I_{STBY}	f_{CL1} = 32kHz	V_{ss} pin	-	-	100	µA
	I_{DD}	f_{CL1} = 32kHz, f_M = 80 Hz	V_{DD} = 5V	-	-	200	
			V_{DD} = 3V	-	-	120	
	I_{EE}		V_{DD} = 5V	-	-	150	

NOTES:

1. Applied to CL1, D2_DL (SHL = LOW), D4_DR (SHL = HIGH), SHL, DISPOFFB, M, CS, AMS pin
2. Pull-up input pins : CL2, D1_SID, D3_DM (AMS = HIGH), ELB (SHL = LOW), ERB (SHL = HIGH)
3. D2_DL (SHL = HIGH) , D4_DR (SHL = LOW) pin
4. V0, V12, V43, V5 pin
5. V_{KCD} = V_{DD}-V_{EE}, V0 = V_{DD} = 5V, V5 = V_{EE} = -23V
   V12 = V_{DD}-1/n(V_{LCD}), V43 = V_{EE}+1/n(V_{LCD}), n = 17(1/256 duty, 1/17 bias)
6. V0 = V_{DD}, V12 = 3.35V (V_{DD} = 5V) or 1.47V (V_{DD} = 3V),
   V43 = -21.35V (V_{DD} = 5 V) or -21.47V (V_{DD} = 3 V), V5 = V_{EE} = -23 V, no-load condition (1/256 duty, 1/17 bias)
   single-type mode operation : AMS = V_{SS}, SHL = V_{SS}, DISPOFFB = V_{DD}
   D1_SID = D3_DM = V_{DD}, D4_DR = OPEN, ELB = ERB = OPEN,
   I_{STBY} : V_{DD} = 5V, M = V_{SS}, D2_DL = V_{SS}
   I_{DD} : f_M = 80Hz, D2_DL = V_{DD}
   V_{DD} = 3 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
   V_{DD} = 5 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
   I_{EE} : f_M = 80Hz, D2_DL = V_{DD}
   V_{DD} = 5V, current through V_{EE} Pin, display data pattern = 10000000..., 01000000...,
   00100000..., 00010000...

AC CHARACTERISTICS

(1) Segment Driver Application

(V_{SS} = 0V, Ta = - 30 - +85°C)

Characteristic	Symbol	Test Condition	(1) V_{DD} = 5V ± 10%			(2) V_{DD} = 3V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	125	-	-	250	-	-	Ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	ELB Output	-	-	60	-	-	125	
		ERB Output			60			125	
ELB, ERB set-up time	t_{PUS}	ELB Input	30	-	-	65	-	-	
		ERB Input	30			65			
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-		Ns
M – OUT propagation delay time	t_{PD1}	C_L = 15pF	-	-	1.0	-	-	1.2	µs
CL1 – OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	-s	

AC CHARACTERISTICS (CONTINUED)

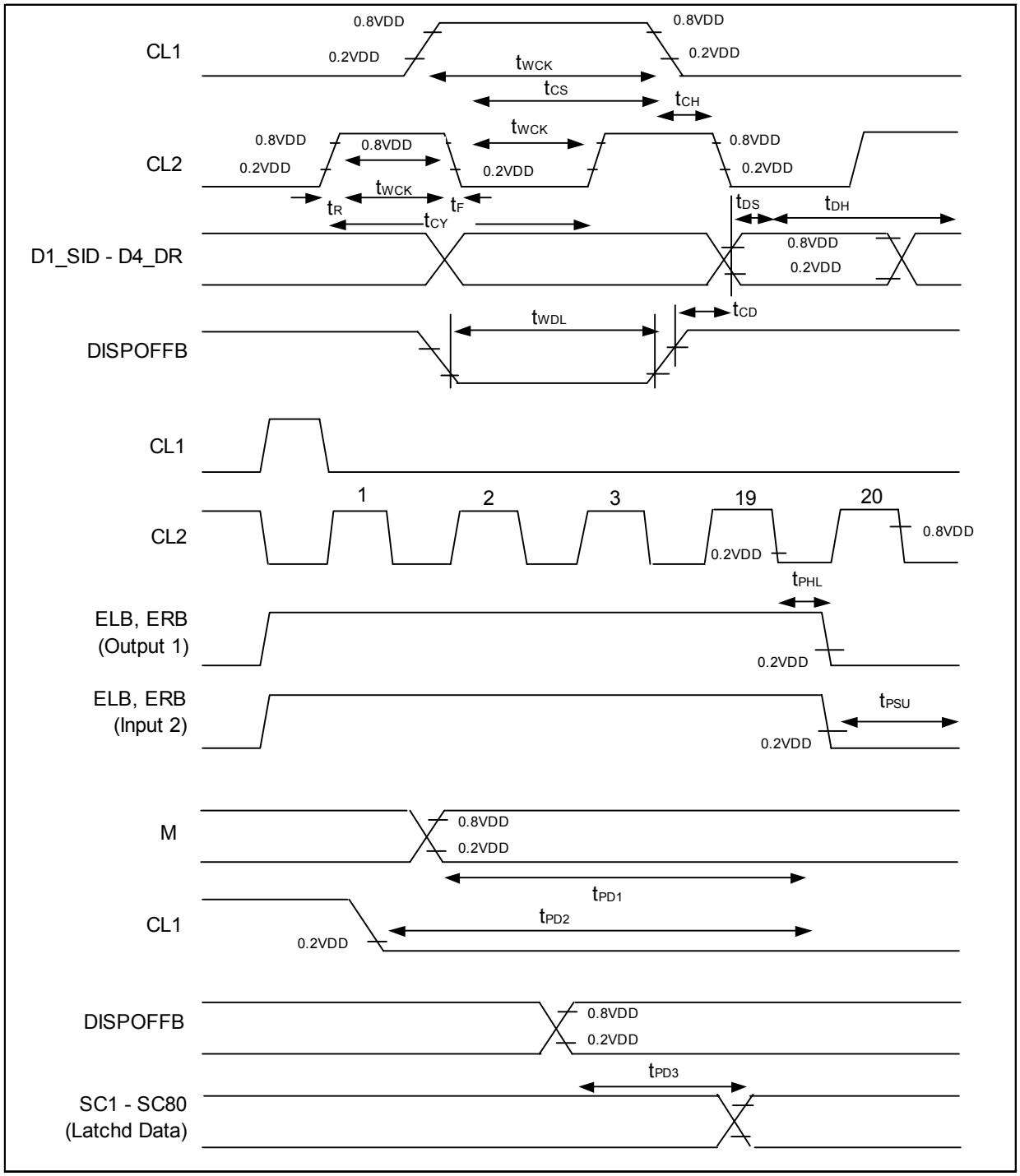
(2) Common Driver Application

(V_{SS} = 0V, Ta = - 30 - +85°C)

Characteristic	Symbol	Test Condition	(1) V_{DD} = 5V ± 10%			(2) V_{DD} = 3V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-		ns
Output delay time	t_{DL}	C_L = 15pF	-	-	200	-	-	250	
M – OUT propagation delay time	t_{PD1}		-	-	1.0			1.2	µs
CL1 – OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t_{PD3}				1.0			1.2	

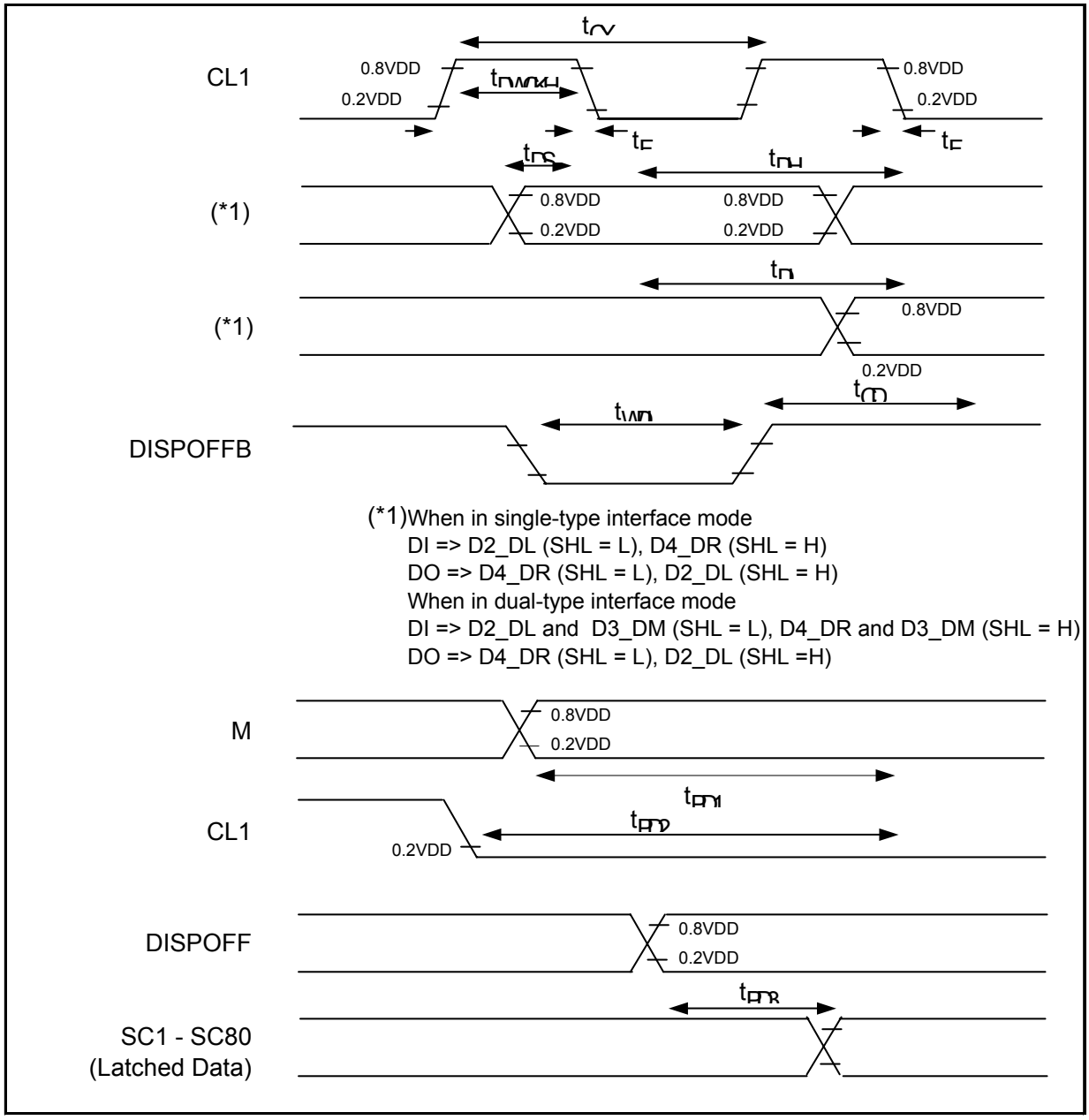
AC CHARACTERISTICS (CONTINUED)

(3) Segment Driver Application Timing



AC CHARACERISTICS (CONTINUED)

(4) Common Driver Application Timing



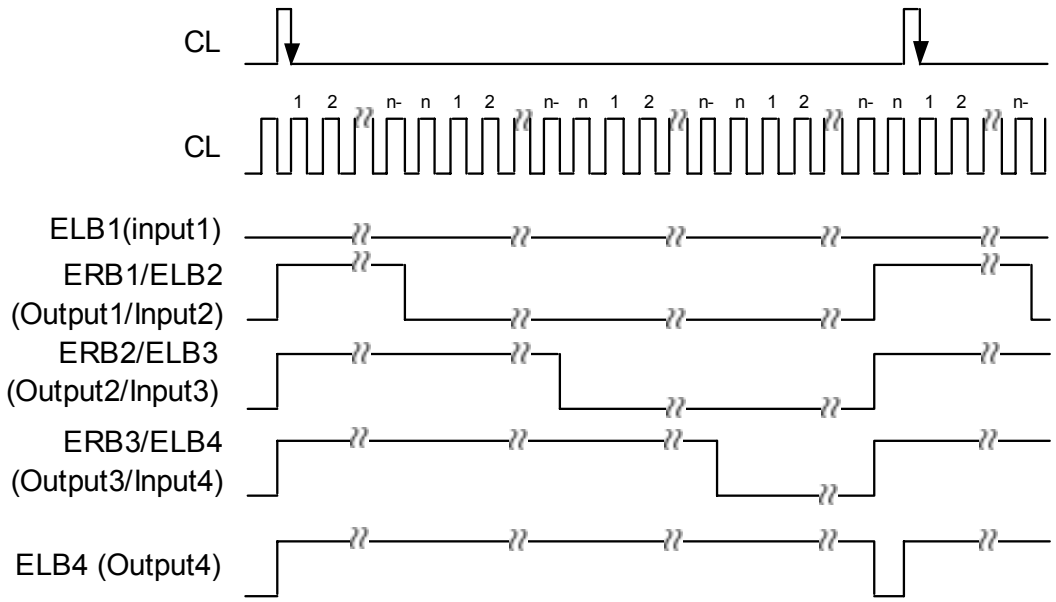
(*1)When in single-type interface mode
DI => D2_DL (SHL = L), D4_DR (SHL = H)
DO => D4_DR (SHL = L), D2_DL (SHL = H)
When in dual-type interface mode
DI => D2_DL and D3_DM (SHL = L), D4_DR and D3_DM (SHL = H)
DO => D4_DR (SHL = L), D2_DL (SHL =H)

POWER DOWN FUNCTION

In the case of cascade connection of segment mode drivers, S6B0086 has a “power down function” in order to reduce the power consumption.

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	ERB	ELB	While ERB =”Low”, current driver is enabled.	Disabled
H	ELB	ERB	While ELB =”Low”, current driver is enabled.	Disabled

* In the case of common driver application, power down function does not work.



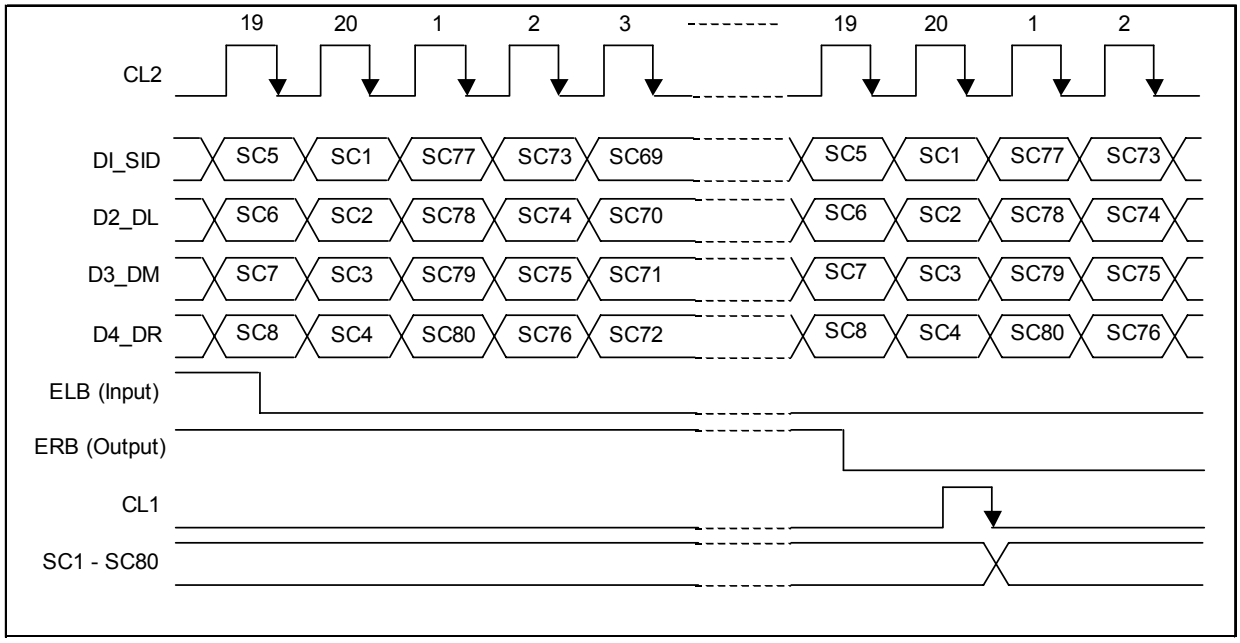
NOTES:

1. SHL = High (EBL = Input, ERB = Output)
   Current SA3086's ERB must be connected to the next SA3086's
2. When in 4-bit parallel interface mode: n = 20
   When in 1-bit serial interface mode: n = 80

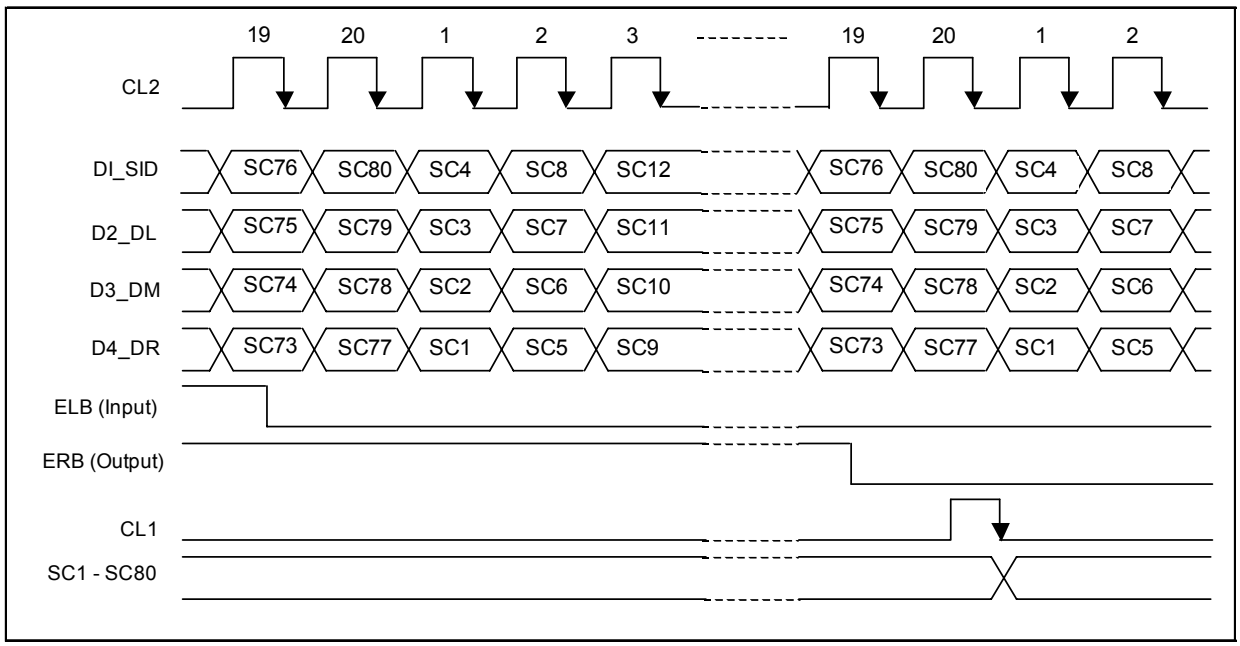
OPERATION TIMING DIAGRAM

(1) 4-BIT Parallel Mode Interface Segment Driver

- When SHL = “Low”

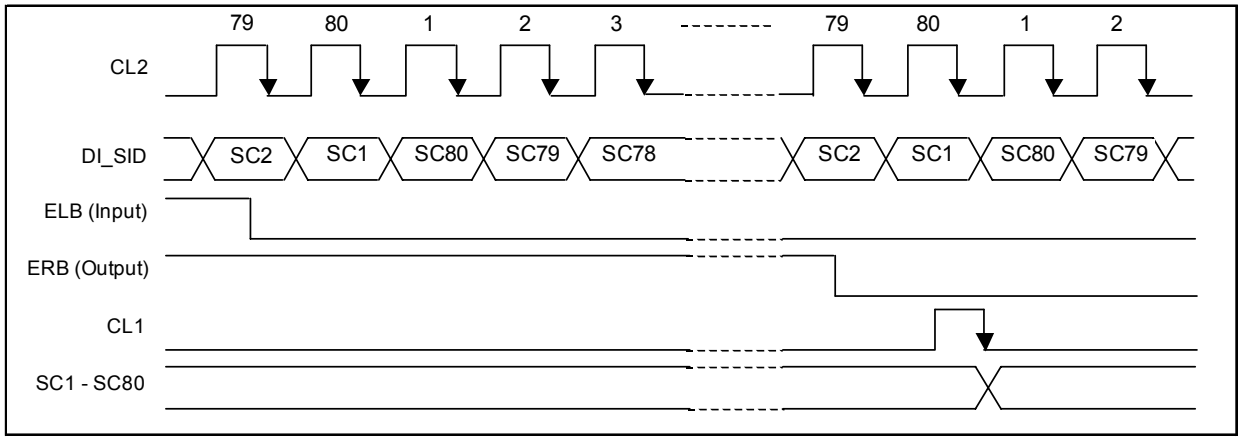


- When SHL = “High”

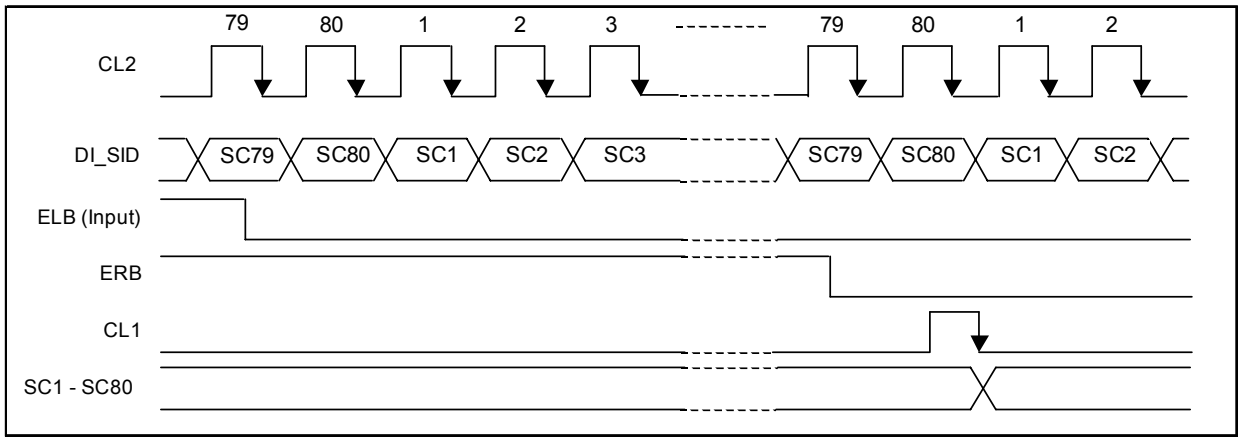


(2) 1-bit Serial Mode Interface Segment Driver

- When SHL = “Low”

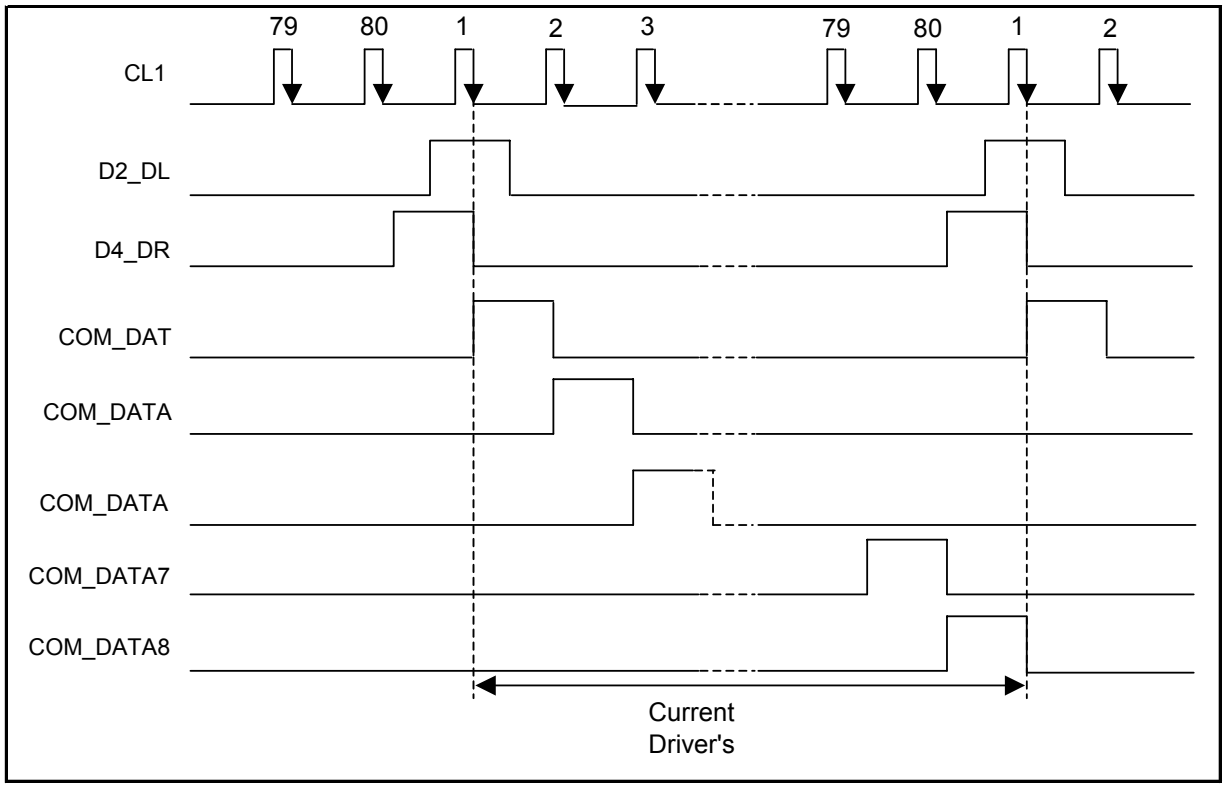


- When SHL = “High”

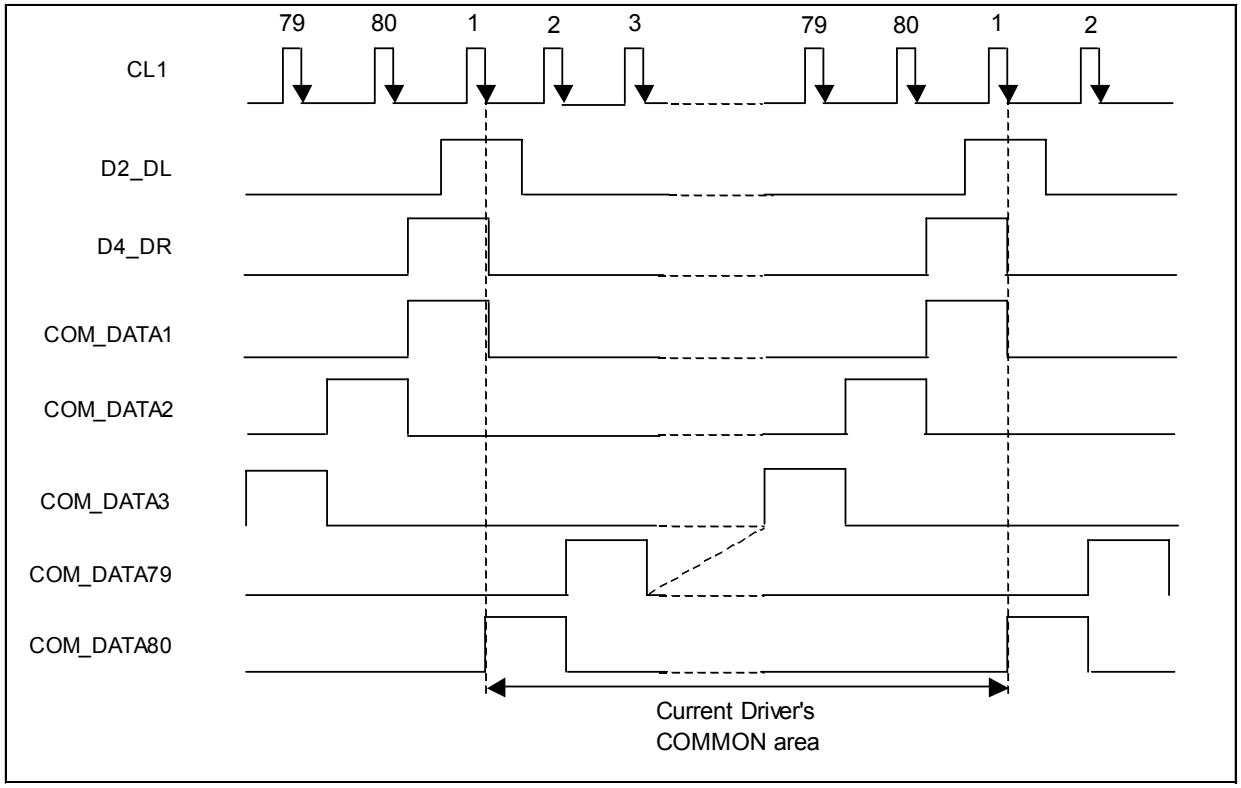


(3) Single-type Interface Mode Common Driver

- When SHL = “Low”

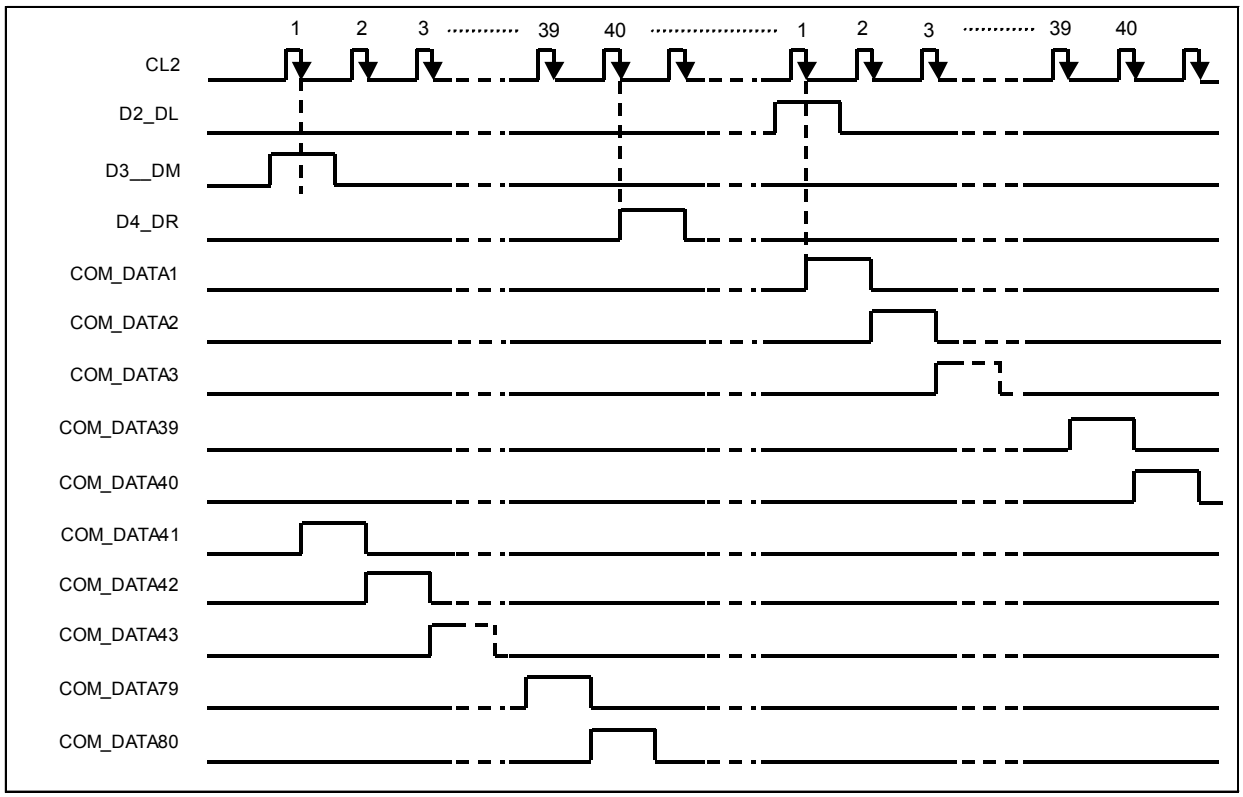


- When SHL = “High”

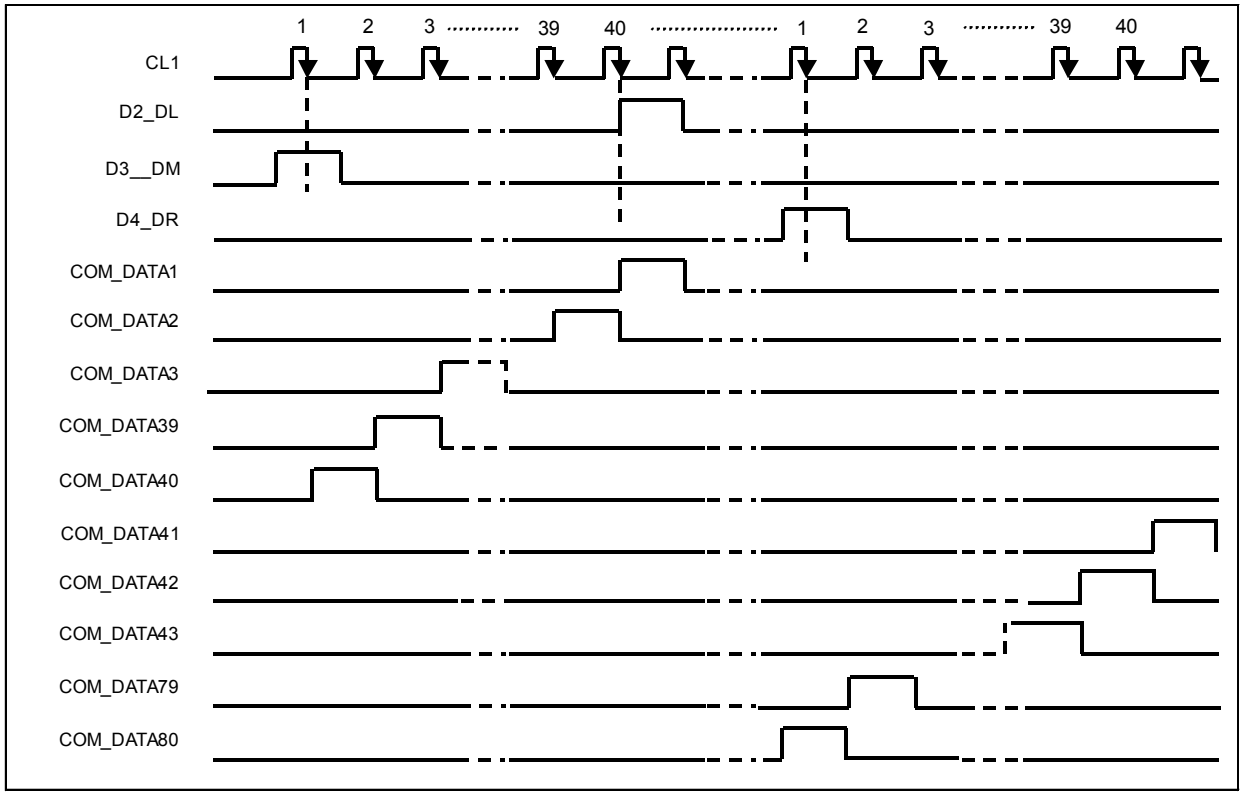


(4) Dual type interface mode driver

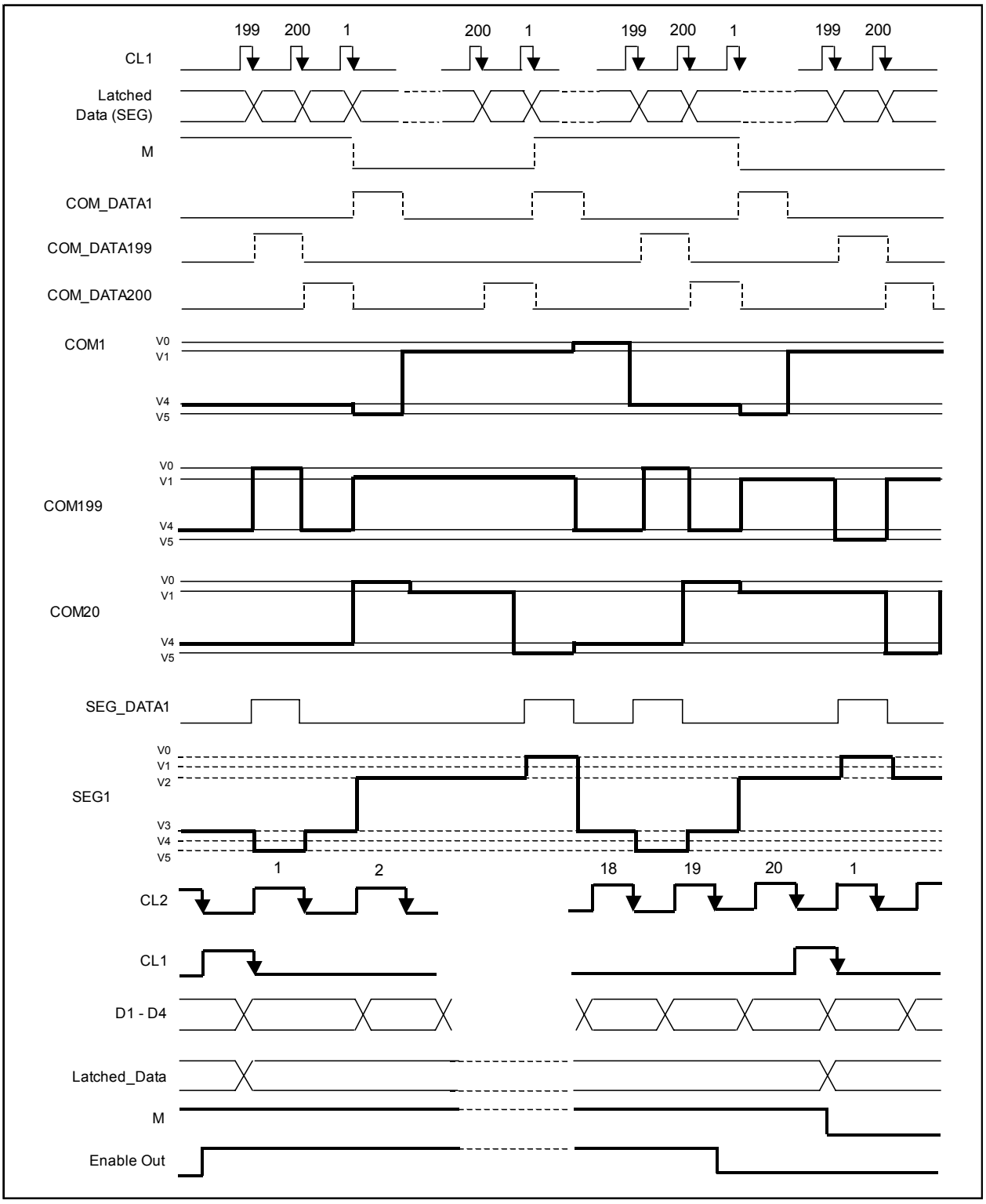
- When SHL = “Low”



- When SHL = “High”



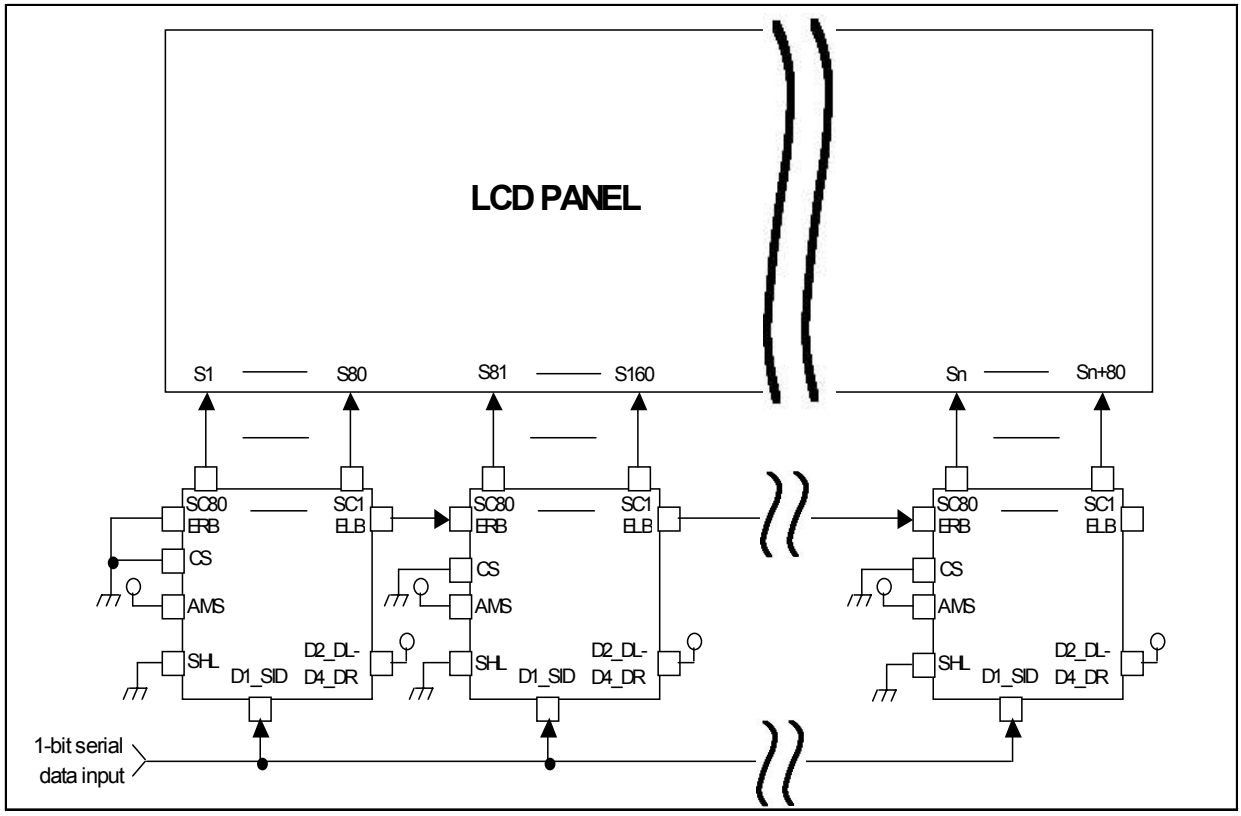
(5) Common / Segment Driver Timing (1/200 DUTY)



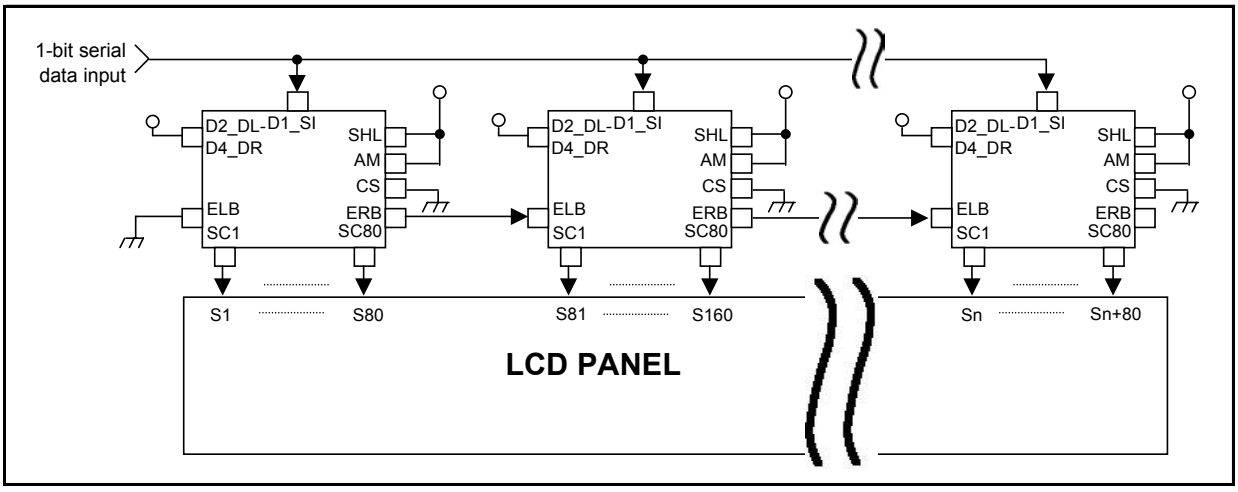
APPLICATION INFORMATION

1-bit Serial Interface (80-Ch. Segment Driver)

a) Lower View (SHL = L, AMS = H)

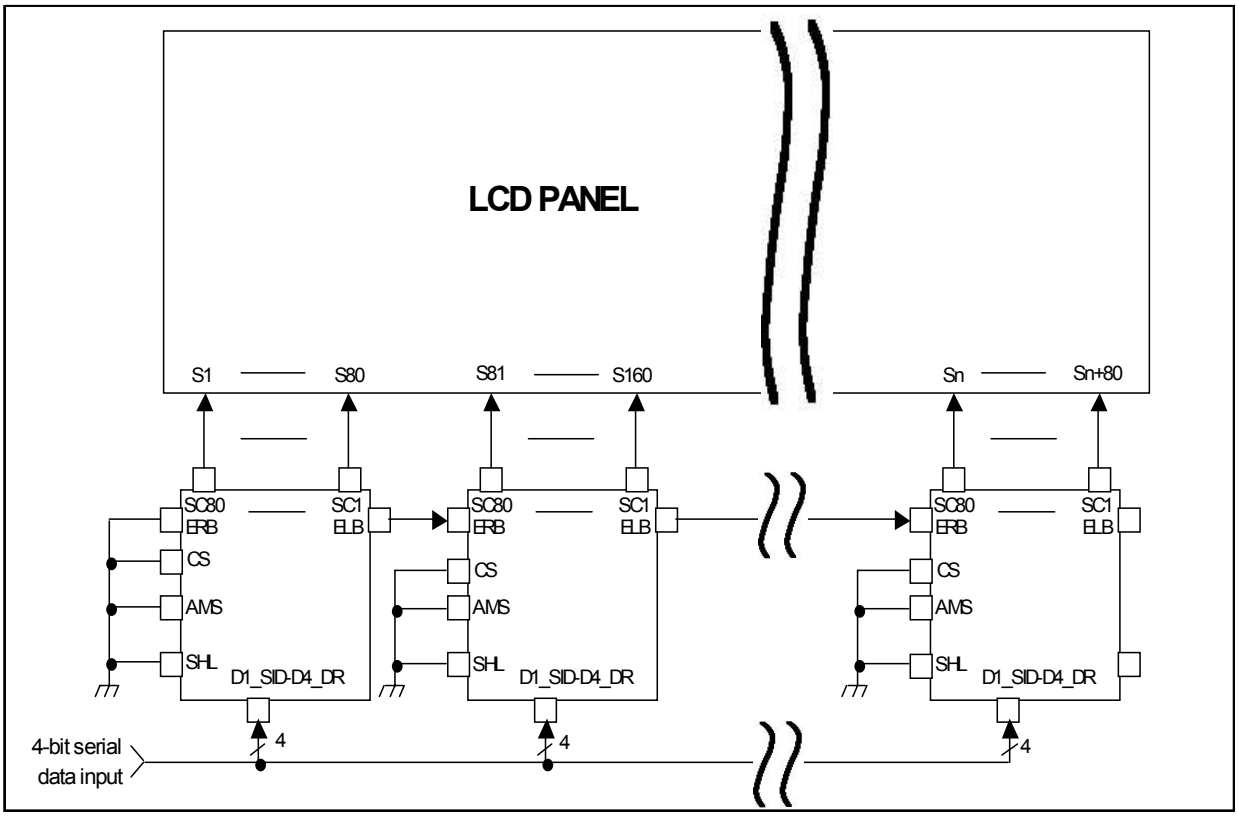


b) Upper View (SHL = H, AMS = H)

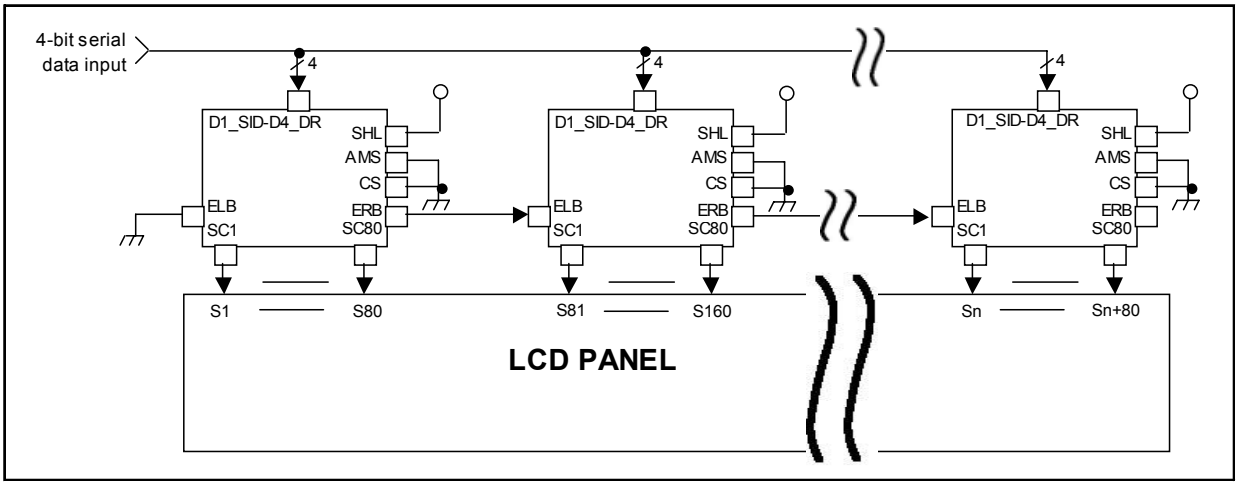


4-Bit Parallel Interface Mode (80 Ch. Segment Driver)

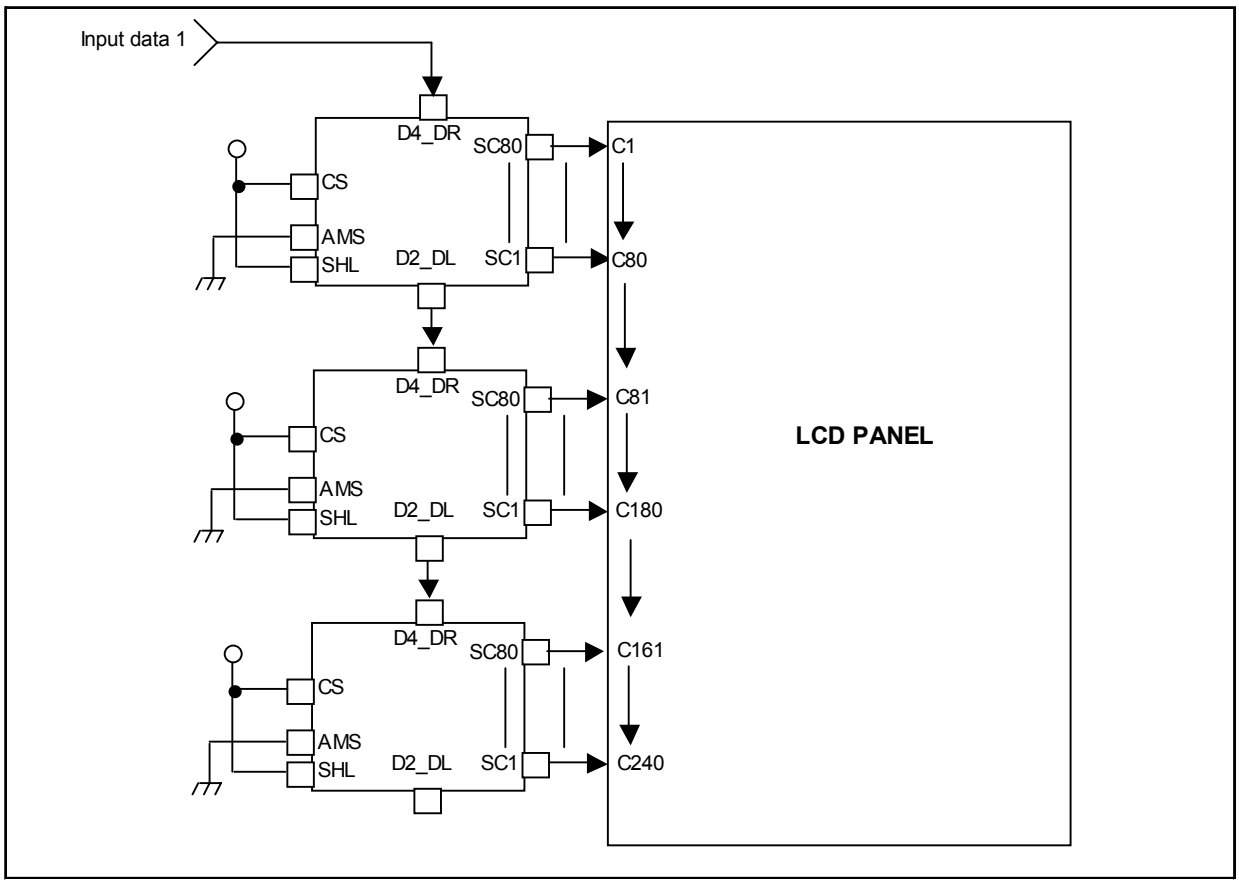
a) Lower View (SHL = L, AMS = L)



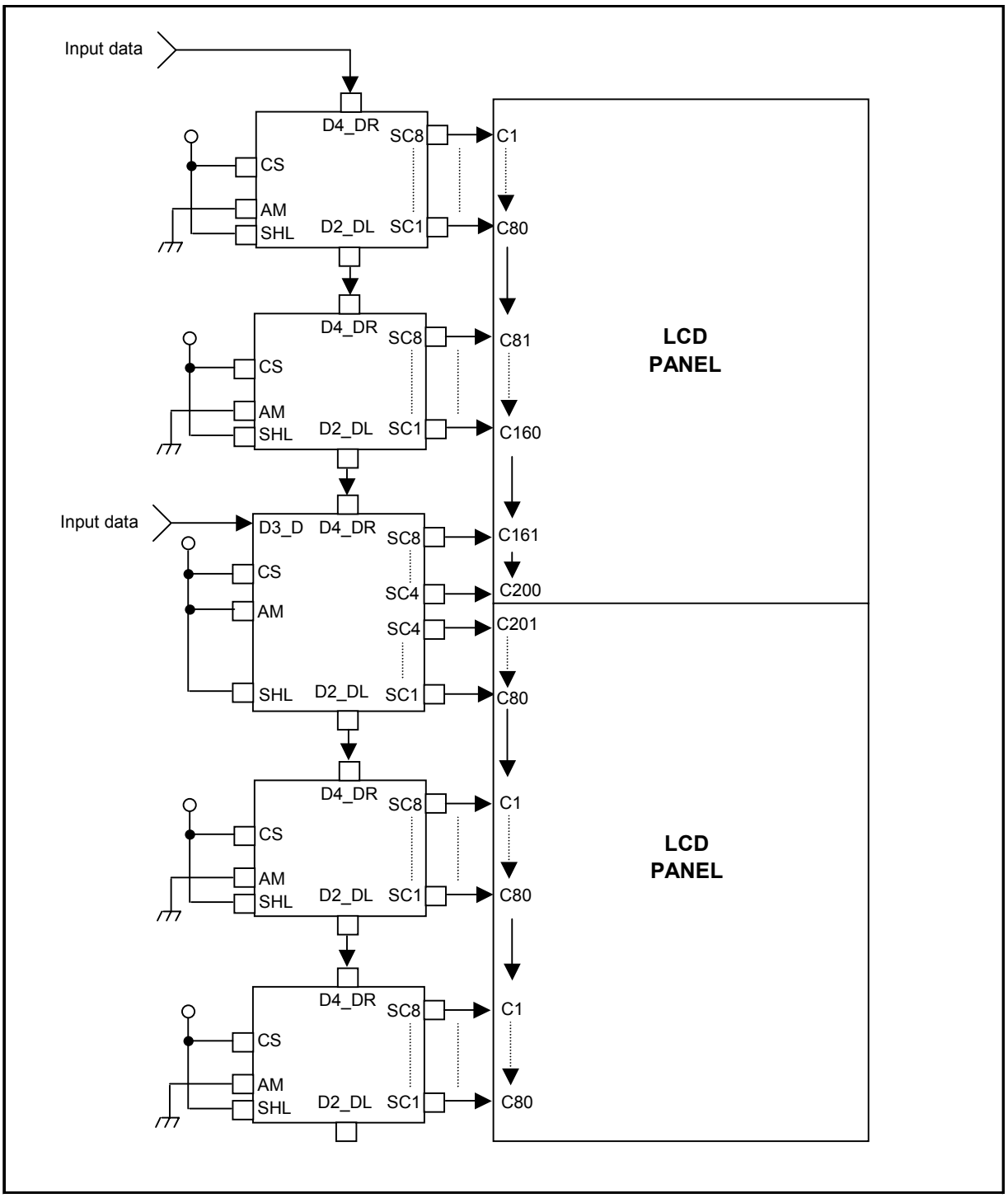
b) Upper View (SHL = H, AMS = L)



Single-type Interface Mode (80 Ch. Common Driver)



Dual-type Interface Mode (40 Ch. Common Driver)



NOTE: Using this application mode (dual-type common mode), the duty ratio can be reduced to half, In case, 1/200 duty can be used to drive the 400 common LCD panel.

APPLICATION CIRCUIT EXAMPLE