



Data Sheet

NT7532

132 X 65 RAM-Map STN LCD

Controller/Driver

V0.02

Preliminary

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Revision History

NT7532 Specification Revision History		
Version	Content	Data
0.01	Original	Jan. 2003
0.02	Cancel the function of the Temperature Coefficient setting	Jul. 2003

Features

- n 132 x 65-dot graphics display LCD controller/driver for black/white STN LCD
- n RAM capacity: 132 x 65 = 8,580 bits
- n 8-bit parallel bus interface for both 8080 and 6800 series,
4-wire Serial Peripheral Interface (SPI)
- n Direct RAM data display using the display data RAM.
When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed.
(At normal display)
- n Many command functions:
Read/Write display data, display ON/OFF, Normal/Reverse display, page address set, set display start line, set LCD bias, electronic contrast controls, V₀ voltage regulation internal resistor ratio set, read modify write, select segment driver direction, power save.
- n Power supply voltage:
 - VDD, VDD2 = 2.4 ~ 3.5 V
 - V₀ = 4.0 ~ 11.5 V
 - VOUT = 12.0 V Max.
- n 2X / 3X / 4X on chip DC-DC converter
- n On chip LCD driving voltage generator or external power supply selectable
- n 64-step contrast adjuster and on chip voltage follower
- n On chip oscillation and hardware reset

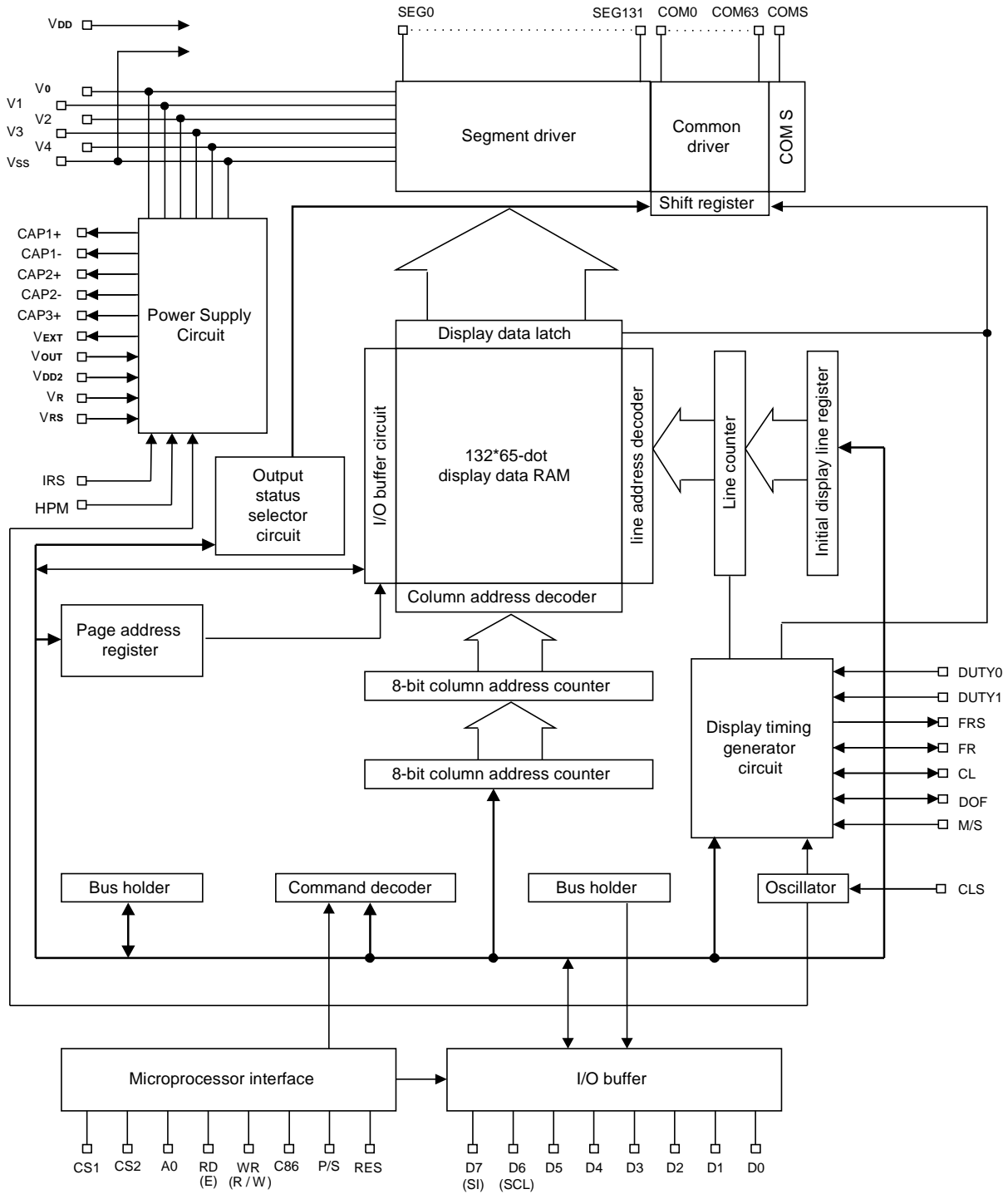
General Description

The NT7532 is a single-chip LCD driver for dot-matrix liquid crystal displays, which is directly connectable to a microcomputer bus. It accepts 8-bit parallel or serial display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates a LCD drive signal independent of the microprocessor clock.

The set of the on-chip display RAM of 65 X 132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom. The NT7532 contain 65 common output circuits and 132 segment output circuits, so that a single chip of NT7532 can make 65 X 132, 55 X 132, 49 X 132 and 33 X 132 dot displays with pad option (DUTY1, DUTY0).

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with minimum current consumption and the smallest LSI configuration.

Block Diagram



Pad Descriptions
Power Supply

Pad No.	Designation	I/O	Description																														
60 – 63	VDD	Supply	2.4 - 3.5V power supply input. These pads must be connected each other.																														
13,27,56,102,122,128,132	VDD	O	2.4 - 3.5V power supply output for pad option																														
64 – 67	VDD2	Supply	This is the power supply for the step-up voltage circuit for the LCD. These pads must be connected each other.																														
68 – 71	VSS	Supply	Ground. These pads must be connected each other.																														
72 – 75	VSS2	Supply	Ground. These pads must be connected each other.																														
6,20,58,99,120,121,125,130,134	VSS	O	Ground output for pad option.																														
115 – 117 103 – 105 106 – 108 109 – 111 112 – 114	V0 V1 V2 V3 V4	Supply	<p>LCD driver supplies voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship: $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{ss}$ When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command.</p> <table border="1"> <thead> <tr> <th>LCD bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/5 bias</td> <td>4/5V0</td> <td>3/5V0</td> <td>2/5V0</td> <td>1/5V0</td> </tr> <tr> <td>1/6 bias</td> <td>5/6V0</td> <td>4/6V0</td> <td>2/6V0</td> <td>1/6V0</td> </tr> <tr> <td>1/7 bias</td> <td>6/7V0</td> <td>5/7V0</td> <td>2/7V0</td> <td>1/7V0</td> </tr> <tr> <td>1/8 bias</td> <td>7/8V0</td> <td>6/8V0</td> <td>2/8V0</td> <td>1/8V0</td> </tr> <tr> <td>1/9 bias</td> <td>8/9V0</td> <td>7/9V0</td> <td>2/9V0</td> <td>1/9V0</td> </tr> </tbody> </table>	LCD bias	V1	V2	V3	V4	1/5 bias	4/5V0	3/5V0	2/5V0	1/5V0	1/6 bias	5/6V0	4/6V0	2/6V0	1/6V0	1/7 bias	6/7V0	5/7V0	2/7V0	1/7V0	1/8 bias	7/8V0	6/8V0	2/8V0	1/8V0	1/9 bias	8/9V0	7/9V0	2/9V0	1/9V0
LCD bias	V1	V2	V3	V4																													
1/5 bias	4/5V0	3/5V0	2/5V0	1/5V0																													
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1/7 bias	6/7V0	5/7V0	2/7V0	1/7V0																													
1/8 bias	7/8V0	6/8V0	2/8V0	1/8V0																													
1/9 bias	8/9V0	7/9V0	2/9V0	1/9V0																													

LCD Power Supply

Pad No.	Designation	I/O	Description
83 – 86	C1-	O	Capacitor 1- pad for internal DC/DC voltage converter.
87 – 90	C1+	O	Capacitor 1+ pad for internal DC/DC voltage converter.
95 – 98	C2-	O	Capacitor 2- pad for internal DC/DC voltage converter.
91 – 94	C2+	O	Capacitor 2+ pad for internal DC/DC voltage converter.
79 – 82	C3+	O	Capacitor 3+ pad for internal DC/DC voltage converter.
76 – 78	VOUT	O	DC/DC voltage converter output
118 – 119	VR	I	Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.
100	VEXT	I	This is the external input reference voltage (VREF) for the internal voltage regulator. It is valid only when external VREF is used. VEXT must be $\geq 2.4V$ and $\leq VDD2$. When using internal VREF, this pad must be NC.
101	VRS	I	Select the internal voltage regulator or external voltage regulator. VRS = 0: using the external VREF VRS = 1: using the internal VREF

System Bus Connection

Pad No.	Designation	I/O	Description
29 – 30 32 – 33 35 – 36 38 – 39 41 – 42 44 – 45 47 – 48 50 – 51	D0 D1 D2 D3 D4 D5 D6 (SCL) D7 (SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.
17 – 19	A0	I	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicate that D0 to D7 are display data A0 = "L": Indicates that D0 to D7 are control data
14 – 16	$\overline{\text{RES}}$	I	When $\overline{\text{RES}}$ is set to "L", the settings are initialized. The reset operation is performed by the $\overline{\text{RES}}$ signal level
7 – 9 10 – 12	$\overline{\text{CS1}}$ $\overline{\text{CS2}}$	I	This is the chip select signal. When $\overline{\text{CS1}}$ ="L" and $\overline{\text{CS2}}$ ="H", then the chip select becomes active, and data/command I/O is enabled.
24 – 26	$\overline{\text{RD}}$ (E)	I	When connected to an 8080 MPU, it is active LOW. This pad is connected to the $\overline{\text{RD}}$ signal of the 8080MPU, and the NT7532 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU
21 – 23	$\overline{\text{WR}}$ (R/ $\overline{\text{W}}$)	I	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU $\overline{\text{WR}}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{\text{WR}}$ signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/ $\overline{\text{W}}$ = "H": Read When R/ $\overline{\text{W}}$ = "L": Write
126	C86	I	This is the MPU interface switch terminal C86 = "H": 6800 Series MPU interface C86 = "L": 8080 MPU interface

System Bus Connection (continuous)

Pad No.	Designation	I/O	Description															
127	P/S	I	<p>This is the parallel data input/serial data input switch terminal P/S = "H": Parallel data input P/S = "L": Serial data input The following applies depending on the P/S status:</p> <table border="1"> <thead> <tr> <th>P/S</th> <th>Data/Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>A0</td> <td>D0 to D7</td> <td>\overline{RD}, \overline{WR}</td> <td>-</td> </tr> <tr> <td>"L"</td> <td>A0</td> <td>SI (D7)</td> <td>Write only</td> <td>SCL (D6)</td> </tr> </tbody> </table> <p>When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. \overline{RD} (E) and \overline{WR} (R/W) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.</p>	P/S	Data/Command	Data	Read/Write	Serial Clock	"H"	A0	D0 to D7	\overline{RD} , \overline{WR}	-	"L"	A0	SI (D7)	Write only	SCL (D6)
P/S	Data/Command	Data	Read/Write	Serial Clock														
"H"	A0	D0 to D7	\overline{RD} , \overline{WR}	-														
"L"	A0	SI (D7)	Write only	SCL (D6)														
124	CLS	I	<p>Terminal to select whether enable or disable the display clock internal oscillator circuit. CLS = "H": Internal oscillator circuit is enabled CLS = "L": Internal oscillator circuit is disabled (requires external input) When CLS = "L", input the display clock through the CL pad.</p>															
123	M/S	I	<p>This terminal selects the master/slave operation for the NT7532 chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.</p>															
4	CL	I/O	<p>This is the display clock input terminal. When the NT7532 chips are used in master/slave mode, the various CL terminals must be connected.</p>															
3	FR	I/O	<p>This is the liquid crystal alternating current signal I/O terminal M/S = "H": Output M/S = "L": Input When the NT7532 chip is used in master/slave mode, the various FR terminals must be connected.</p>															
5	\overline{DOF}	I/O	<p>This is the liquid crystal display blanking control terminal. M/S = "H": Output M/S = "L": Input When the NT7532 chip is used in master/slave mode, the various \overline{DOF} terminals must be connected.</p>															
2	FRS	O	<p>This is the output terminal for the static drive. This terminal is only enabled when the static indicator display is ON in master operation mode, and is used in conjunction with the FR terminal</p>															

System Bus Connection (continuous)

Pad No.	Designation	I/O	Description
131	IRS	I	<p>This terminal selects the resistors for the V0 voltage level adjustment.</p> <p>IRS = "H", Use the internal resistors IRS = "L", Do not use the internal resistors</p> <p>The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal. This pad is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected</p>
129	$\overline{\text{HPM}}$	I	<p>This is the power control terminal for the power supply circuit for liquid crystal drive.</p> <p>$\overline{\text{HPM}}$ = "H", Normal mode $\overline{\text{HPM}}$ = "L", High power mode</p> <p>This pad is enabled only when the master operation mode is selected and It is fixed to either "H" or "L" when the slave operation mode is selected.</p>

Liquid Crystal Drive Pads

Pad No.	Designation	I/O	Description
168 – 299	SEG0 - 131	O	Segment signal output for LCD display.
135 – 166 300 – 331	COM31 - 0 COM32 - 63	O	Common signal output for LCD display. When in master/slave mode, the same signal is output by both master and slave
167, 332	COMS	O	These are the COM output terminals for the indicator. Both terminals output the same signal. No connect these terminals if they are not used. When in master/slave mode, the same signal is output by both master and slave.

Configuration Pad

Pad No.	Designation	I/O	Description															
57 59	DUTY0 DUTY1	I	<p>Select the LCD driver duty</p> <table border="1"> <thead> <tr> <th>DUTY1</th> <th>DUTY0</th> <th>LCD driver duty</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1/33</td> </tr> <tr> <td>0</td> <td>1</td> <td>1/49</td> </tr> <tr> <td>1</td> <td>0</td> <td>1/55</td> </tr> <tr> <td>1</td> <td>1</td> <td>1/65</td> </tr> </tbody> </table>	DUTY1	DUTY0	LCD driver duty	0	0	1/33	0	1	1/49	1	0	1/55	1	1	1/65
DUTY1	DUTY0	LCD driver duty																
0	0	1/33																
0	1	1/49																
1	0	1/55																
1	1	1/65																

Test Pad

Pad No.	Designation	I/O	Description
28	TEST0	I	Test pads, and must be connected to VDD.
1,31,34,37, 40,43,46,49, 52–55,133	NC	-	NC pads, no connection for user.

Functional Descriptions

Microprocessor Interface

Interface Type Selection

The NT7532 can transfer data via 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI). When high or low is selected for the parity of P/S pad either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data cannot be read out.

Table. 1

P/S	Type	$\overline{CS1}$	CS2	A0	\overline{RD}	\overline{WR}	C86	D7	D6	D0 to D5
H	Parallel Input	$\overline{CS1}$	CS2	A0	\overline{RD}	\overline{WR}	C86	D7	D6	D0 to D5
L	Serial Input	$\overline{CS1}$	CS2	A0	-	-	-	SI	SCL	(HZ)

“-” Must always be high or low

Parallel Interface

When the NT7532 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pad to go high or low as shown in Table 2.

Table. 2

C86	Type	$\overline{CS1}$	CS2	A0	\overline{RD}	\overline{WR}	D0 to D7
H	6800 microprocessor bus	$\overline{CS1}$	CS2	A0	E	R/ \overline{W}	D0 to D7
L	8080 microprocessor bus	$\overline{CS1}$	CS2	A0	\overline{RD}	\overline{WR}	D0 to D7

Data Bus Signals

The NT7532 identifies the data bus signal according to A0, E, R/ \overline{W} (\overline{RD} , \overline{WR}) signals.

Table. 3

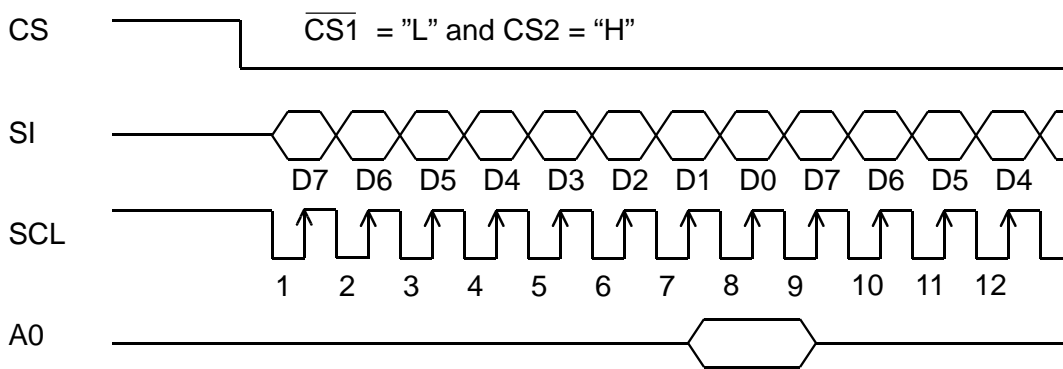
Common	6800 processor (R/ \overline{W})	8080 processor		Function
		\overline{RD}	\overline{WR}	
A0				
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Reads status
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface

When the serial interface has been selected (P/S = “L”), then when the chip is in active state ($\overline{CS1}$ = “L” and CS2 = “H”), the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data in the rising edge of eighth serial clock for processing.

The A0 input is used to determine whether or the serial data input is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is the serial interface signal chart.

Figure. 1



Note:

1. When the chip is not active, the shift registers and the counters are reset to their initial states.
2. Reading is not possible while in serial interface mode.
3. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

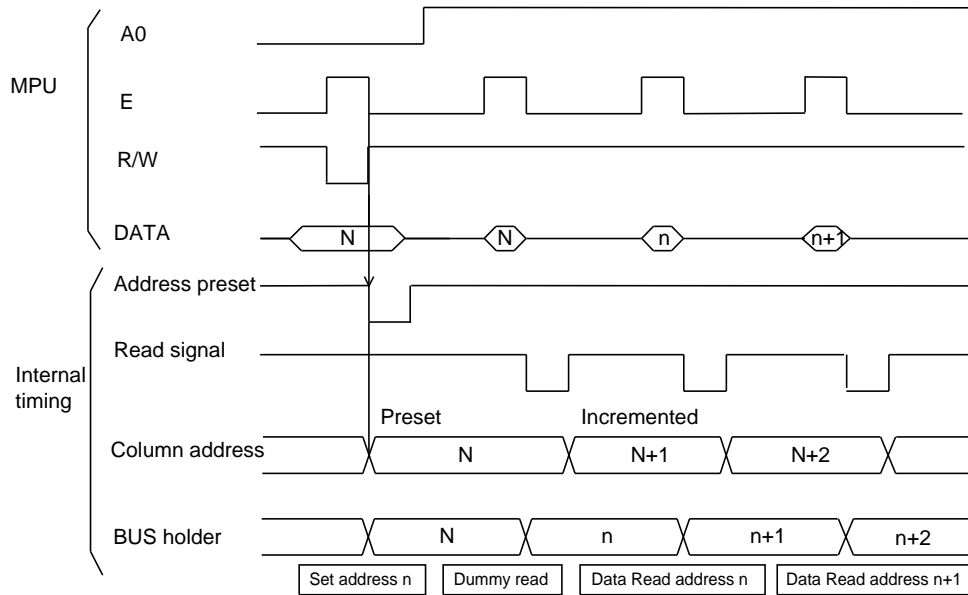
Chip Select Inputs

The NT7532 has two chips select pads. $\overline{CS1}$ and CS2 can interface to a microprocessor when $\overline{CS1}$ is low and CS2 is high. When these pads are set to any other combination. D0 to D7 are high impedance and A0, E and $\overline{R/W}$ inputs are disabled. When serial input interface is selected. the shift register and counter are reset.

Access to Display Data RAM and Internal Registers

The NT7532 can perform a series of pipeline processing between LSI's using the bus holder of the internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in the bus holder, and outputs it onto system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in the bus holder, and stores it in display RAM until the next data write cycle starts.

When viewed from the microprocessor, the NT7532 access speed greatly depends on the cycle time rather than access time to the display RAM (t_{acc}). This view shows the data transfer speed to / from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during the second data read. A single dummy read must be inserted after address setup and after the write cycle (refer to Figure2).

Figure. 2


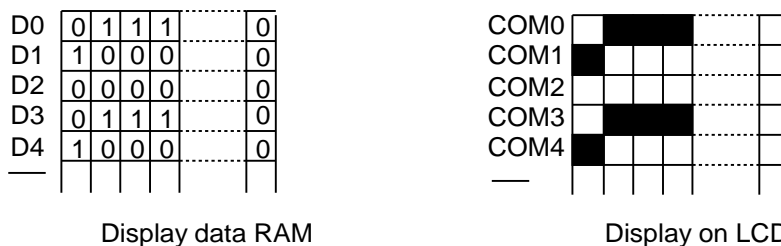
Busy Flag

When the busy flag is "1" it indicates that the NT7532 chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pad with the read instruction. If the cycle time (t_{cyc}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

Display Data RAM

The display data RAM is RAM that stores the dot data for the display. It has a $65(8 \text{ page} * 8 \text{ bit} + 1) * 132$ bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display common direction, and there are few constraints at the time of display data transfer when multiple NT7532 chips are used, thus display structures can be created easily and with a high degree of freedom.

Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

Figure. 3


The Page Address Circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address8 (D3, D2, D1, D0 = 1, 0, 0, 0,) is the page for the RAM region used; only display data D0 is used.

The Column Address

As shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read / write command. This allows the MPU display data to be accessed continuously. Moreover, the incrimination of column addresses stops with 83H, because the column address is independent of the page address. Thus, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to respecify both the page address and the column address.

Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table. 4

SEG Output	SEG0	SEG131
ADC "0"	0 (H)à	Column Address à 83 (H)
(ADC) "1"	83 (H)ß	Column Address ß0 (H)

The Line Address Circuit

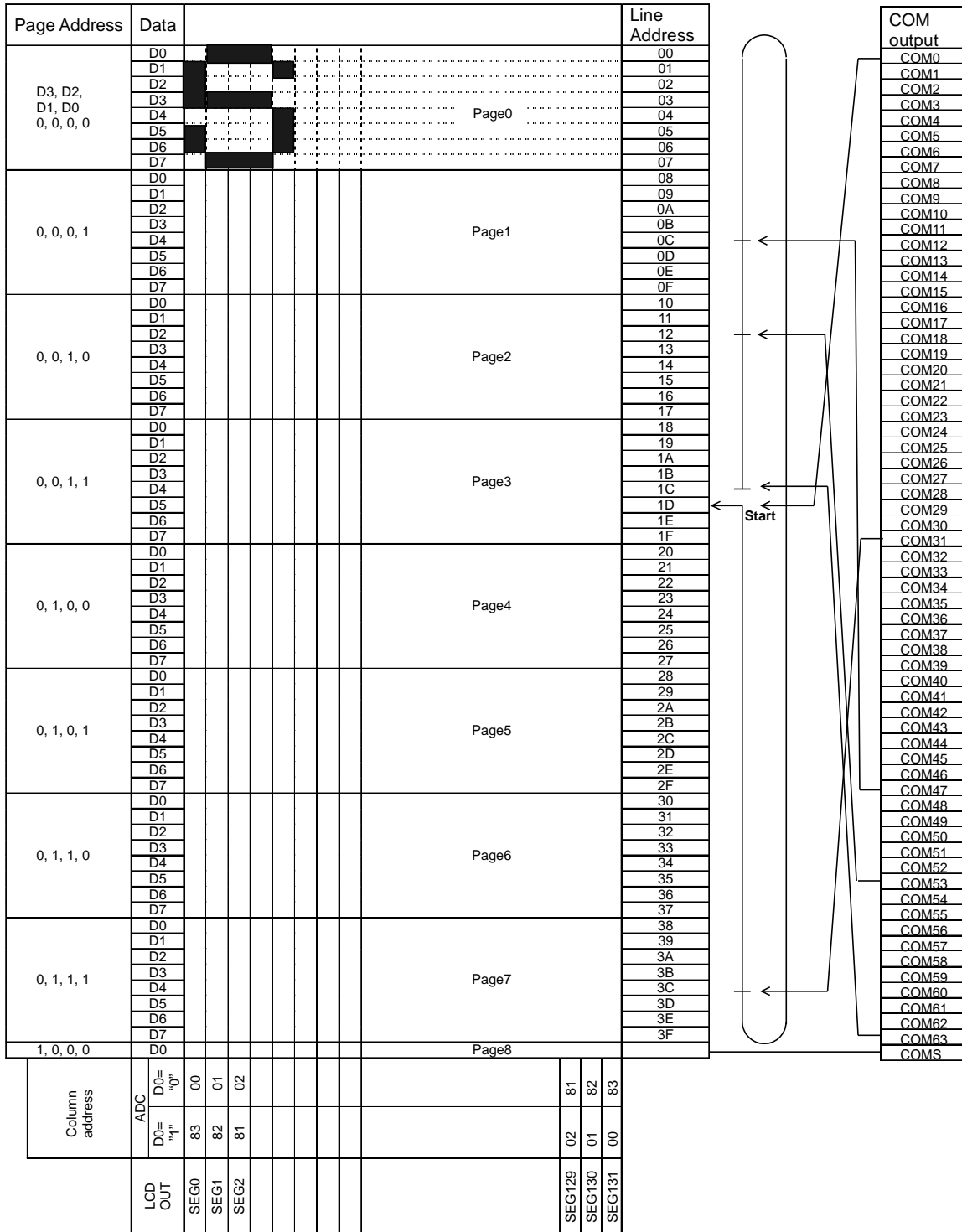
The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal and the COM63 output for NT7532, when the common output mode is reversed. The display area is a 65-line area for the NT7532 from the display start line address. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = "H" and CLS = "H". When CLS = "L" the oscillation stops, and the display clock is input through the CL terminal.

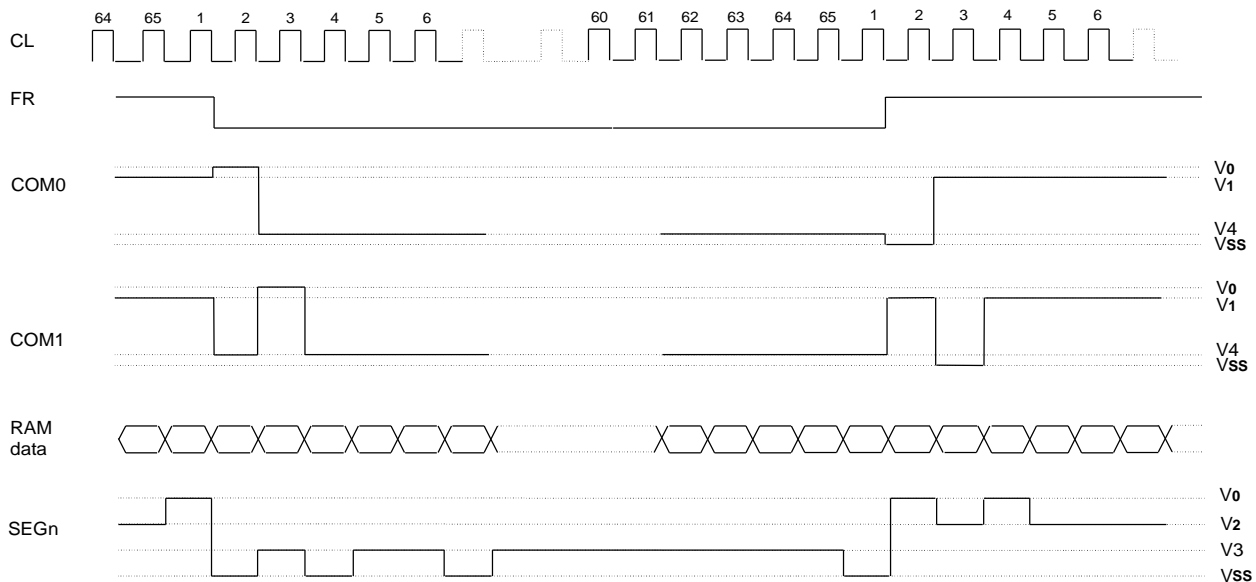
Figure. 4 Relationship between display data RAM and address. (if initial display line is 1DH)


Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of access to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive waveform using a 2 frames alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Figure. 5



When multiple NT7532 chips are used, the slave chips must be supplied with the display timing signals (FR, CL, \overline{DOF}) from the master chip[s]. Table 5 shows the status of the FR, CL, and \overline{DOF} signals.

Table. 5

Operating Mode		FR	CL	\overline{DOF}
Master (M/S = "H")	The internal oscillator circuit is enabled (CLS = "H")	Output	Output	Output
	The internal oscillator circuit is disabled (CLS = "L")	Output	Input	Output
Slave (M/S = "L")	The internal oscillator circuit is disabled (CLS = "H")	Input	Input	Input
	The internal oscillator circuit is disabled (CLS = "L")	Input	Input	Input

Table 6 shows the relationship between oscillation frequency and frame frequency.

Table. 6

Duty	Item	f _{CL}	f _{FR}
1/65	On-chip oscillator is used	f _{osc} /6	f _{CL} /(2 X 65)
	On-chip oscillator is not used	External input f _{CL}	f _{CL} /(2 X 65)
1/55	On-chip oscillator is used	f _{osc} /8	f _{CL} /(2 X 55)
	On-chip oscillator is not used	External input f _{CL}	f _{CL} /(2 X 55)
1/49	On-chip oscillator is used	f _{osc} /8	f _{CL} /(2 X 49)
	On-chip oscillator is not used	External input f _{CL}	f _{CL} /(2 X 49)
1/33	On-chip oscillator is used	f _{osc} /12	f _{CL} /(2 X 33)
	On-chip oscillator is not used	External input f _{CL}	f _{CL} /(2 X 33)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads.

Table. 7

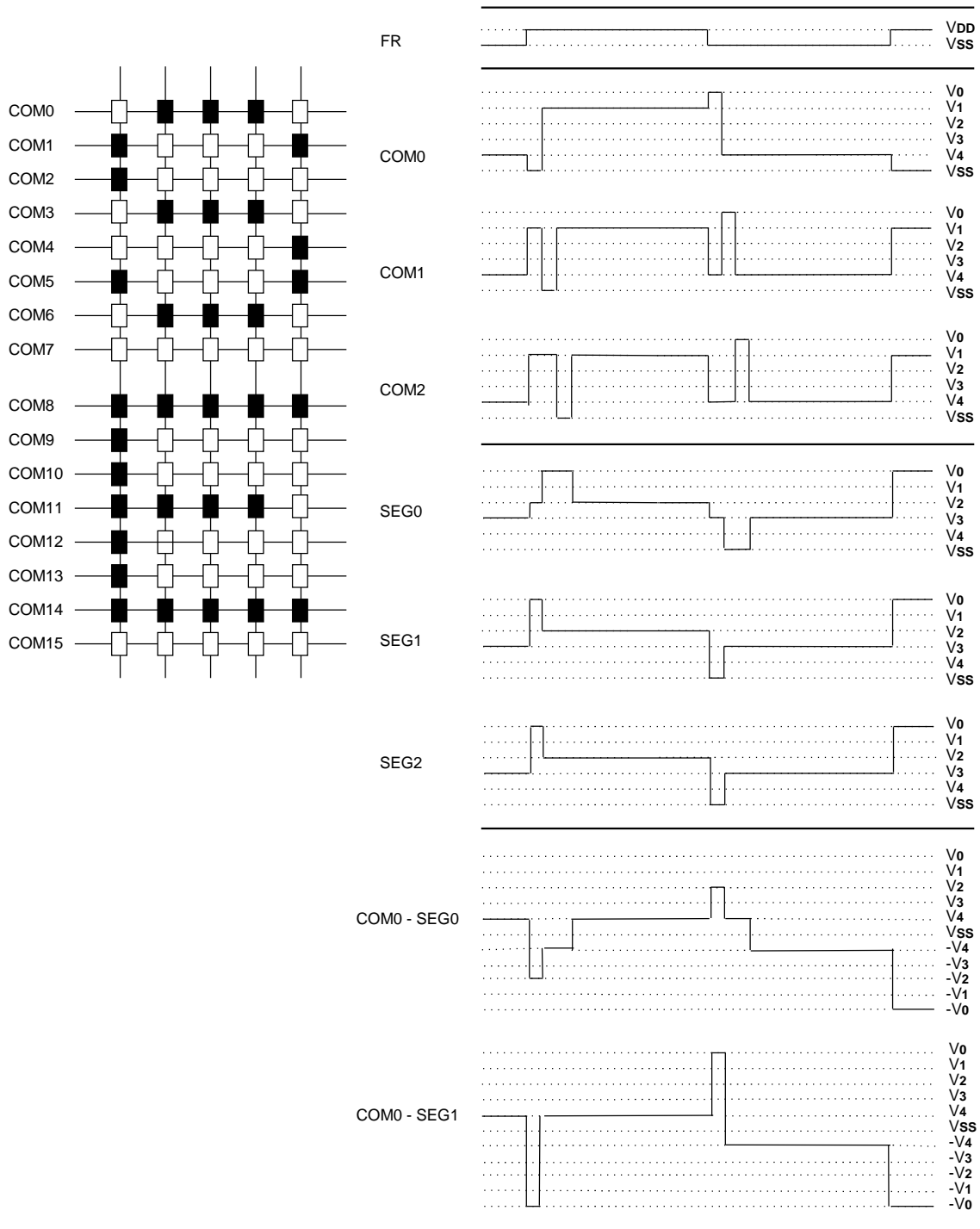
Duty	Status	Common output pads								
		COM [0-15]	COM [16-23]	COM [24-26]	COM [27-36]	COM [37-39]	COM [40-47]	COM [48-63]	COMS	
1/33	Normal	COM[0-15]	NC					COM[16-31]	COMS	
	Reverse	COM[31-16]	NC					COM[15-0]		
1/49	Normal	COM[0-23]		NC			COM[24-47]		COMS	
	Reverse	COM[47-24]		NC			COM[23-0]			
1/55	Normal	COM[0-26]			NC	COM[27-53]			COMS	
	Reverse	COM[53-27]			NC	COM[26-0]				
1/65	Normal	COM[0-63]								COMS
	Reverse	COM[63-0]								

The combination of the display data, the COM scan signals, and the FR signal produces the liquid crystal drive voltage output. Figure 6 shows example of the SEG and COM output waveform.

Configuration Setting

The NT7532 has two optional configurations, configured by DUTY0, DUTY1.

DUTY1 DUTY0	Common	Segment	V1	V2	V3	V4
1, 1	65	132	8/9V0, 6/7V0	7/9V0, 5/7V0	2/9V0, 2/7 V0	1/9V0, 1/7V0
1, 0	55	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 1	49	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 0	33	132	5/6V0, 4/5V0	4/6V0, 3/5V0	2/6 V0, 2/5V0	1/6V0, 1/5V0

Figure. 6


The Power Supply Circuit

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control functions, and Table 8 shows reference combinations.

Table. 8

Item	Status	
	"1"	"0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table. 9

Use Settings	D2	D1	D0	Step-up Circuit	Voltage regulator circuit	V/F circuit	External voltage input	Step-up voltage system terminal
Only the internal power supply is used	1	1	1	O	O	O	VDD2	Used
Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	VOUT, VDD2	Open
Only the V/F circuit is used	0	0	1	X	X	O	V0, VDD2	Open
Only the external power supply is used	0	0	0	X	X	X	V0 to V4	Open

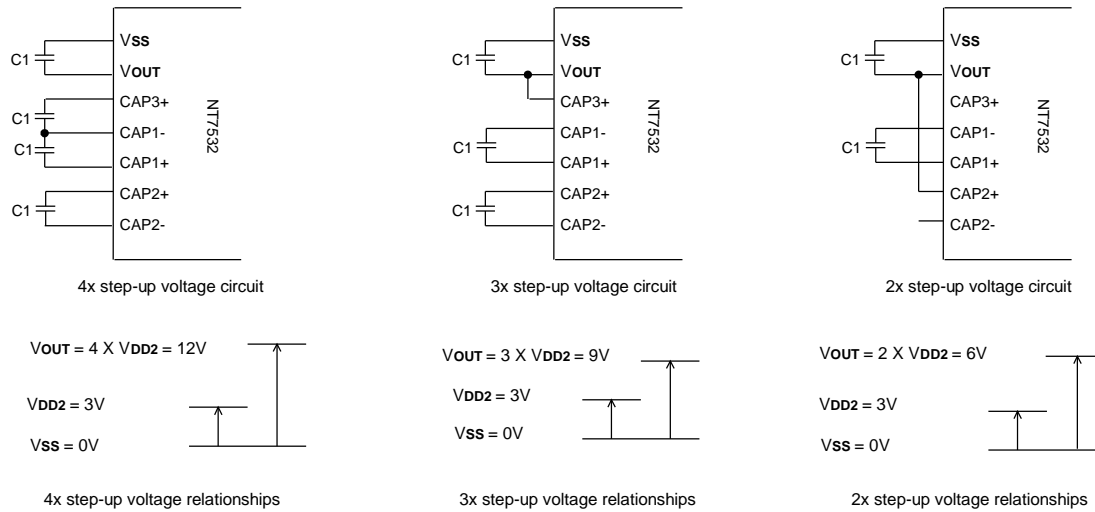
*The "step-up system terminals" refer CAP1+, CAP1-, CAP2+, CAP2- and CAP3+.

*While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits within the NT7532 chips it is possible to product 4X, 3X, 2X step-ups of the VDD2-VSS2 voltage levels.

Figure. 7



The Voltage Regulator Circuit

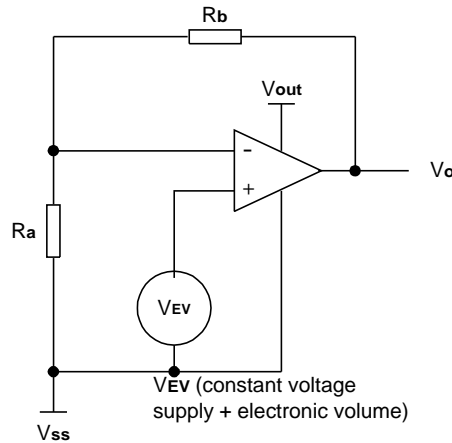
The step-up voltage generated at V_{out} outputs the liquid crystal driver voltage V_0 through the voltage regulator circuit. Because the NT7532 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

Moreover, in the NT7532, two types of thermal gradients have been prepared as VREG options:
 (1) approximately $-0.05\%/^{\circ}C$ and (2) external input (supplied to the VEXT terminal).

When the V0 Voltage Regulator Internal Resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where $|V0| < |VOUT|$.

$$V0 = (1+Rb/Ra)*V_{EV} = (1+Rb/Ra)* (1-(63-\alpha)/162)*VREG \quad (\text{Equation A-1})$$



VREG is the IC internal fixed voltage supply, and its voltage at $T_a = 25^\circ\text{C}$ is as shown in Table 10.

Table. 10

Equipment Type	VRS	Thermal Gradient	Units	VREG
Internal Power Supply	1	-0.05	%/°C	2.1
External Input	0	-	-	VEXT

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for α depending on the electronic volume register settings. Ra/Rb is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The $(1+Rb/Ra)$ ratio assumes the values shown in Table11 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

Table. 11

D5	D4	D3	D2	D1	D0	α	V0
0	0	0	0	0	0	0	Minimum
0	0	0	0	0	1	1	:
0	0	0	0	1	0	2	:
		:			:	:	:
1	0	0	0	0	0	32 (default)	:
		:			:	:	:
1	1	1	1	1	0	62	:
1	1	1	1	1	1	63	Maximum

V0 voltage regulator internal resistance ratio register value and (1+ Rb/Ra) ratio (Reference value)

Table. 12

Register			Equipment Type by Thermal Gradient [Units:%/°C]	
D2	D1	D0	-0.05	VREG External Input
0	0	0	3.0	1.5
0	0	1	3.5	2.0
0	1	0	4.0	2.5
0	1	1	4.5	3.0
1	0	0	5.0	3.5
1	0	1	5.5	4.0
1	1	0	6.0	4.5
1	1	1	6.4	5.0

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta=25°C and V0=7V for a NT7532 model on which the temperature compensation is internal, using the equation A-1, the following setup is enable.

Table. 13

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V0 voltage regulator	-	-	-	0	1	0
Electronic Volume	1	0	0	1	0	1

- When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
- The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L"). When the V0 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the VR terminal is left open.
- Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The Liquid Crystal Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3, and V4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for NT7532 can be selected.

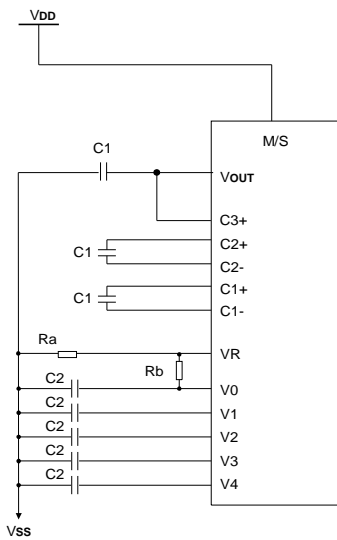
High Power Mode

The power supply circuit equipped in the NT7532 chips has very low power consumption (normal mode: $\overline{\text{HPM}} = \text{"H"}$). However for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the $\overline{\text{HPM}}$ terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.

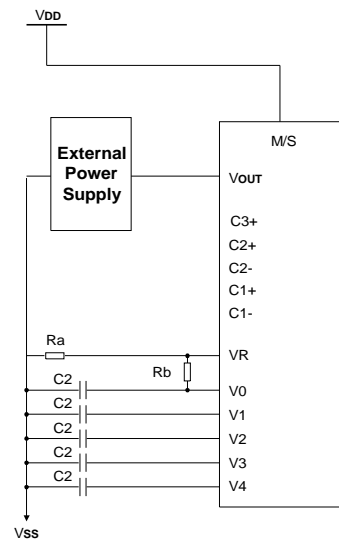
Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a Command Sequence when Built-in Power Supply is turned OFF. To turn off the built-in power supply, follow the command sequence as shown below to turn it off after making the system enter standby mode.

Reference Power Supply Circuit for Driving LCD Panel

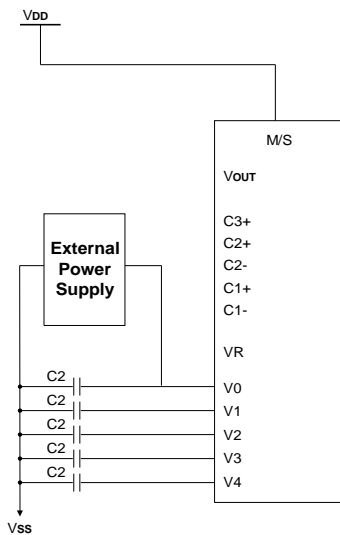
-When using all LCD power circuits
(Voltage converter regulator and follower)
(In case of 3X boosting circuit)



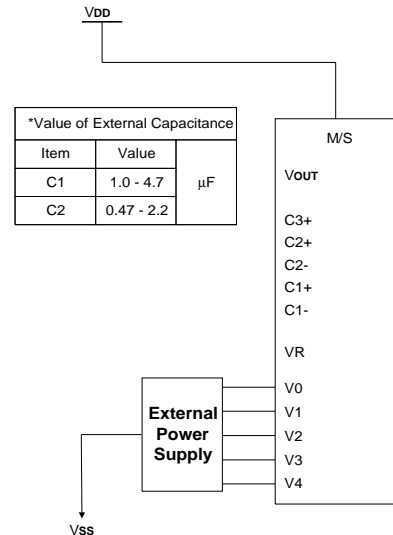
-When not using voltage booster circuits



-When only using voltage follower



-When not using internal LCD power supply circuits



Reset Circuit

When the $\overline{\text{RES}}$ input falls to “L”, these LSIs reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = “L”)
4. Power control register (D2, D1, D0) = (0, 0, 0,)
5. Register data clear in serial interface
6. LCD power supply bias ratio 1/9 (1/65 duty), 1/8 (1/55, 1/49 duty), 1/6 (1/33 duty)
7. Read modify write OFF
8. Static indicator: OFF
Static indicator register: (D1, D2) = (0, 0)
9. Display start line register set at first line
10. Column address counter set at address0
11. Page address register set at page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear:
V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear
Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Test mode clear
16. All-indicator-lamps-on OFF (All-indicator-lamps ON/OFF command D0 = “L”)
17. Output condition of COM, SEG
COM: V1
SEG: V2

On the other hand, when the reset command is used, only default settings 7 to 15 above are put into effect.

The MPU interface (Reference Example)”, the $\overline{\text{RES}}$ terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the $\overline{\text{RES}}$ terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition; therefore, take measures to prevent the input terminal from entering a high impedance state.

In the NT7532, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply an “L” signal to the $\overline{\text{RES}}$ terminal when the external liquid crystal power supply is applied. Even though the oscillator circuit operates while the $\overline{\text{RES}}$ terminal is “L,” the display timing generator circuit is stopped, and the FR, FRS, and $\overline{\text{DOF}}$ terminals are fixed to “H,” and the CL pin is fixed to “H” only when the internal oscillator circuit is used. There is no influence on the D0 to D7 terminals.

Commands

The NT7532 uses a combination of A0, \overline{RD} (E) and \overline{WR} (R/ \overline{W}) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the \overline{RD} pad and a write status when a low pulse is input to the \overline{WR} pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/ \overline{W} pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, \overline{RD} (E) becomes 1(high) when the 6800 series microprocessor interface reads status of display data. This is the only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands are explained below. When the serial interface is selected, input data starting from D7 in sequence.

1. Display ON/OFF

Alternatively turns the display on and off.

A0	\overline{E} \overline{RD}	$\overline{R/\overline{W}}$ \overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	1	1	AFh	Display ON
										0	AEh	Display OFF

When the display OFF command is executed when in the display all points ON mode, power save mode is entered. See the section on the power saver for details.

2. Set Display Start Line

Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. The higher number of lines in ascending order, corresponding to the duty cycle follows it. When this command changes the line address, smooth scrolling or a page change takes place.

A0	\overline{E} \overline{RD}	$\overline{R/\overline{W}}$ \overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	A5	A4	A3	A2	A1	A0	40h to 7Fh

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator, and only D0 is valid for data change.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	1	1	A3	A2	A1	A0	B0h to BFh

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
		:		:
1	1	1	0	7
1	1	1	1	8

4. Set Column Address

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access the display RAM, the column address counter is incremental by during each access until address 132 is accessed. The page address is not changed during this time.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	0	1	A7	A6	A5	A4	10h to 1Fh
						0	A3	A2	A1	A0	00h to 0Fh

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	1
0	0	0	1	0	1	1	0	2
			:					:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

5. Read Status

This command is used to control the output status of signal SYNC, PM, CL and FR.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Busy: When high, the NT7532 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address "131-n" corresponds to segment driver n. when high, the display is normal and column address corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When low, the display turns on. When high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by \overline{RES} signal or by reset command. When low, the display is on. When high, the chip is being reset.

6. Write Display Data

Write 8-bit data in display RAM. As the column address automatically increments by 1 after each write, the microprocessor can continue to write data of multiple words.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address automatically increments by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads could be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure4. When display data is written or read, the column address is incremented by 1 as shown in Figure4.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	0	0	0	A0h	Normal
										1	A1h	Reverse

9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	1	0	A6h	RAM Data "H" LCD ON voltage (normal)
										1	A7h	RAM Data "L" LCD ON voltage (reverse)

10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	0	0	A4h	Normal display mode
										1	A5h	Display all points ON

When D0 is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power save mode. Refer to the Power Save section for details.

11. Set LCD Bias

This command selects the voltage bias ratio required for the liquid crystal display.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Duty			
												1/33	1/49	1/55	1/65
0	1	0	1	0	1	0	0	0	1	0	A2h	1/6 bias	1/8 bias	1/8 bias	1/9 bias
										1	A3h	1/5 bias	1/6 bias	1/6 bias	1/7 bias

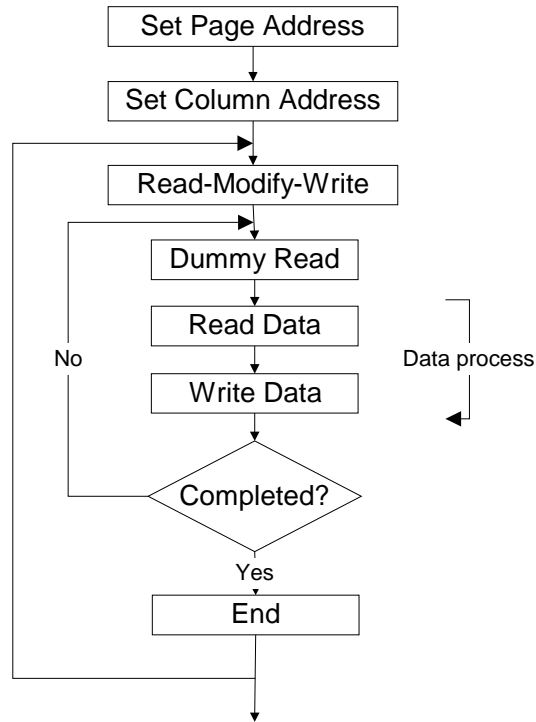
12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or other events.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	0	0	E0h

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

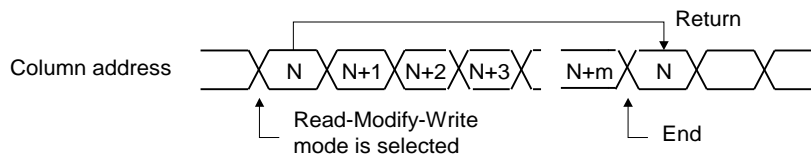
Cursor display sequence



13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued)

A0	E	R/ \overline{W}	D7	D6	D5	D4	D3	D2	D1	D0	Hex
	\overline{RD}	\overline{WR}									
0	1	0	1	1	1	0	1	1	1	0	Eh



14. Reset

This command resets the Display Start Line register, Column Address counter, Page Address register, and Common output mode register, the V0 voltage regulator internal resistor ratio register, the Electronic Volume register, the static indicator mode register, the read-modify-write mode register, and the test mode. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
0	1	0	1	1	1	0	0	0	0	1	0	E2h

The Reset command cannot initialize LCD power supply. Only the Reset signal to the \overline{RES} pad can initialize the supplies.

15. Output Status Select Register

When D3 is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	0	0	0	*	*	*	C0h to C7h
			1	1	0	0	1				C8h to CFh

*: Invalid bit

D3 = 0: Normal (COM0 → COM63/53/47/31)

D = 1: Reverse (COM63/53/47/31 → COM0)

16. Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	1	A2	A1	A0	28h to 2Fh

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.
 When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.
 When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

17. V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under “The Power Supply Circuits”.

A0	$\frac{E}{RD}$	$\frac{R/\bar{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	20h	Small
								0	0	1	21h	
								0	1	0	22h	
									:		:	
								1	1	0	26h	
								1	1	1	27h	Large

18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. It is a two bytes command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

(1) The Electronic Volume Mode Set

When this command is input, the electronic volume register set command is enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	$\frac{E}{RD}$	$\frac{R/\bar{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	0	0	1	81h

(2) Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	$\frac{E}{RD}$	$\frac{R/\bar{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Hex	V0
0	1	0	*	*	0	0	0	0	0	1	XX	Small
					0	0	0	0	1	0	XX	
					0	0	0	0	1	1	XX	
									:		:	
					1	1	1	1	1	0	XX	
					1	1	1	1	1	1	XX	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double bytes command paired with the static indicator register set command, and thus command must be executed one after the other. (The static indicator OFF command is a single byte command)

(1) Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	0	0	ACh	Static Indicator OFF
										1	ADh	Static Indicator ON

(2) Static Indicator Register Set

This command sets two bits of data into the static indicator register and used to set the static indicator into a blinking mode.

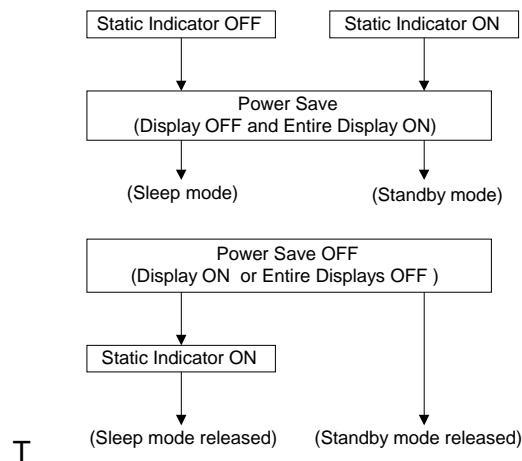
A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Indicator Display Status
0	1	0	*	*	*	*	*	*	0	0	XX	OFF
									0	1	XX	ON (blinking at approximately 1 second intervals)
									1	0	XX	ON (blinking at approximately 0.5 second intervals)
									1	1	XX	ON (constantly on)

20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce current consumption.

If the static indicator is off, the Power Save command makes the system enter sleep mode. If the static indicator is on, this command makes the system enter standby mode.

Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

- (1) Stops the oscillator circuit and LCD power supply circuit.
- (2) Stops the LCD driver and outputs the VSS level as the segment/common driver output.
- (3) Holds the display data and operation mode provided before the start of the sleep mode.
- (4) The MPU can access the built-in display data RAM.

Standby Mode

Stops the operation of the duty LCD displays system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive. The ON operation of the static drive system indicates that the NT7532 is in standby mode. The internal status in the standby mode is as follows:

- (1) Stops the LCD power supply circuit.
- (2) Stops the LCD drive and outputs the VSS level as the segment / common driver output.
However, the static drive system still operates.
- (3) Holds the display data and operation mode provided before the start of the standby mode.
- (4) The MPU can access the built-in display data RAM.

When the Reset command is issued in the standby mode, the sleep mode is set.

- When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7532 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7532 to go to the sleep mode or standby mode.

21. NOP

Non-Operation Command.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	1	1	E3h

22. Test Command

This is the dedicated IC chip test command. It must not be used for normal operation. If the Test command is issued inadvertently set the \overline{RES} input to low or issue the Reset command to release the test mode.

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	1	*	*	*	*	F0h to FFh

*: Invalid bit

Cautions: The NT7532 maintains an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. Users must consider how to suppress noise on the package and system or to prevent ambient noise insertion. To prevent a spike in noise, built-in software for periodical status refreshment is recommended. The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

Table 14. Command Table

Command	A0	RD	WR	Code									Hex	Function
				D7	D6	D5	D4	D3	D2	D1	D0			
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0	1	AEh AFh	Turn on LCD panel when goes high, and turn off when goes low
(2) Set Display Start Line	0	1	0	0	1	Display Start Address					40h to 7Fh	Specifies RAM display line for COM0		
(3) Set Page Address	0	1	0	1	0	1	1	Page Address				B0h to BFh	Set the display data RAM page in Page Address register	
(4) Set Column Address	0	1	0	0	0	0	1	Higher Column Address				00h to 1Fh	Set 4 higher bits and 4 lower bits of column address of display data RAM in register	
	0	1	0	0	0	0	0	Lower Column Address						
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information	
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM	
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM	
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0	1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0	1	A6h A7h	Normal indication when low, but full indication when high
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	A4h A5h	Selects normal display (0) or entire display on
(11) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0	1	A2h A3h	Sets LCD driving voltage bias ratio
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	0	E0h	Increments column address counter during each write
(13) End	0	1	0	1	1	1	0	1	1	1	0	0	EEh	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	0	E2h	Resets internal functions
(15) Common Output Mode Select	0	1	0	1	1	0	0	0	1	*	*	*	C0h to CFh	Selects COM output scan direction *: invalid data
(16) Set Power Control	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Selects the power circuit operation mode	
(17) V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Selects internal resistor ratio Rb/Ra mode	
(18) Electronic Volume mode Set Electronic Volume Register Set	0	1	0	1	0	0	0	0	0	0	1	81h		
	0	1	0	*	*	Electronic Control Value					XX	Sets the V0 output voltage electronic volume register		
(19) Set Static indicator ON/OFF Set Static Indicator Register	0	1	0	0	0	1	0	1	0	1	0	1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode	
(20) Power Save	0	1	0	-	-	-	-	-	-	-	-	-		Compound command of Display OFF and Entire Display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation	
(22) Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!	
(23) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset	

Note: Do not use any other command, or system malfunction may result.

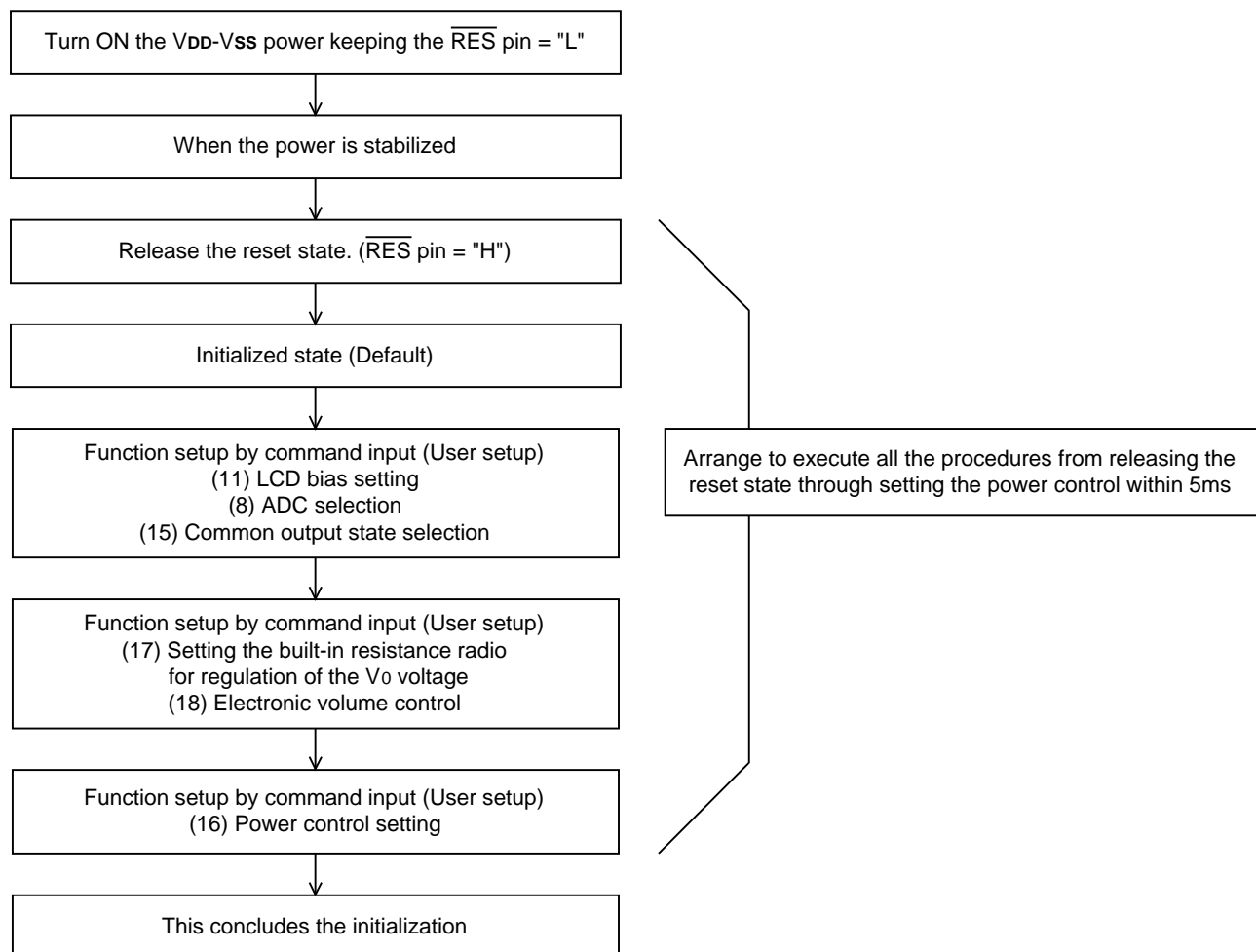
Command Description

Instruction Setup: Reference

1. Initialization

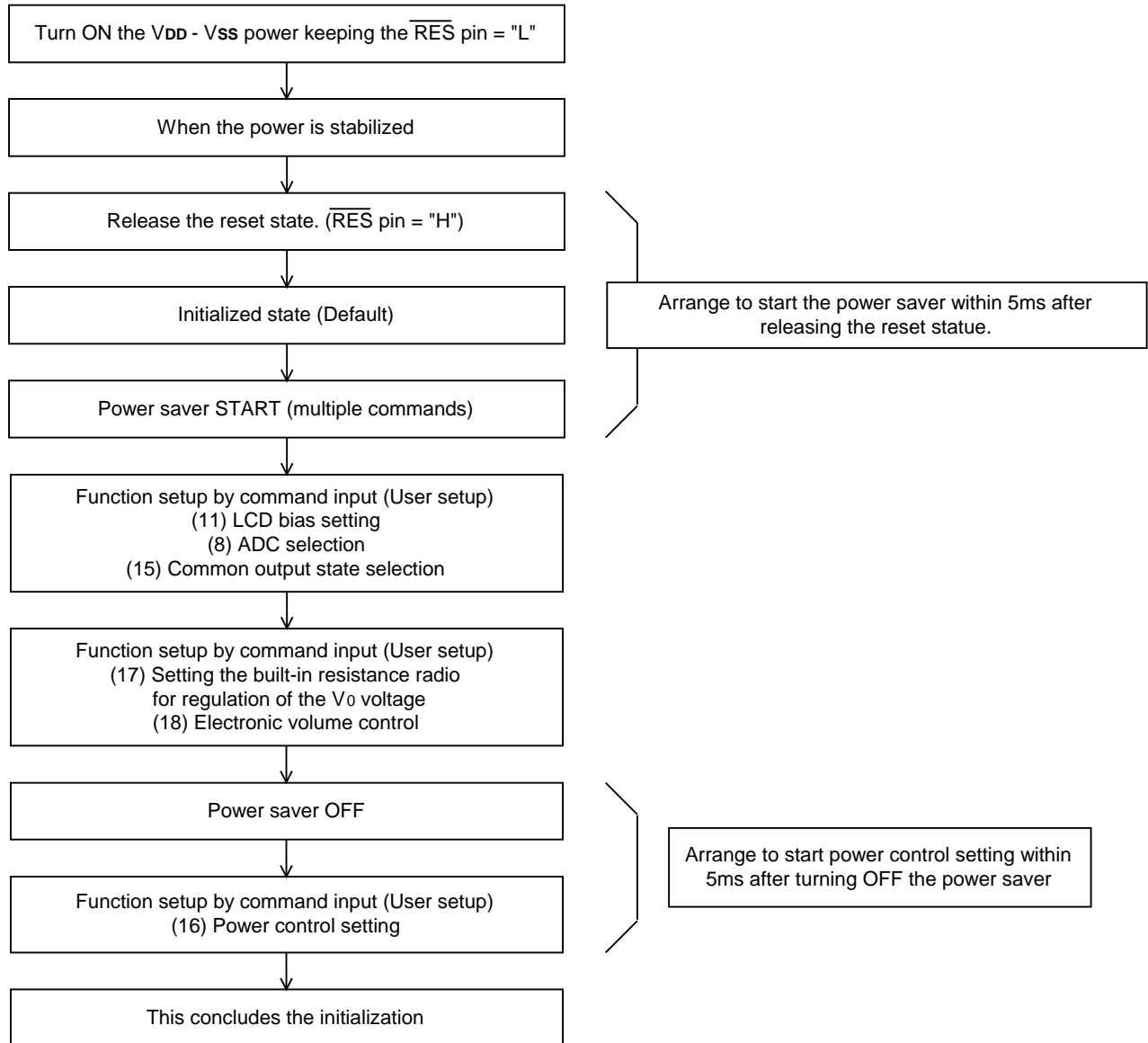
Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 - V4) and the VDD pin, the picture on the display may instantaneously become totally dark when the power is turned on. To avoid such failure, we recommend the following flow sequence when turning on the power.

1.1. When the built-in power is being used immediately after turning on the power:



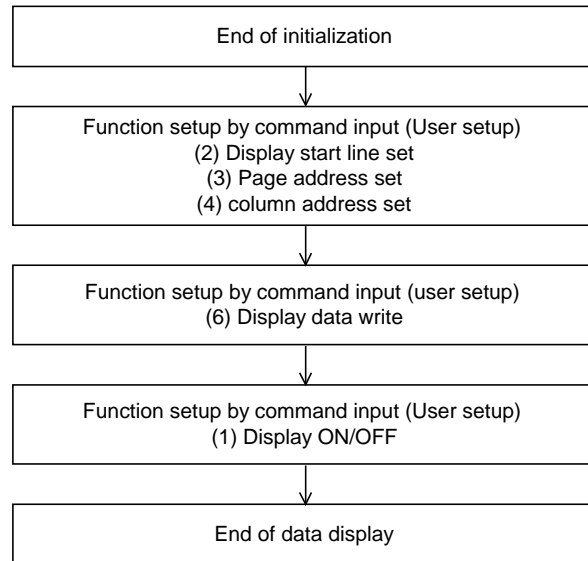
The target time of 5ms will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

1.2. When the built-in power is not being used immediately after turning on the power

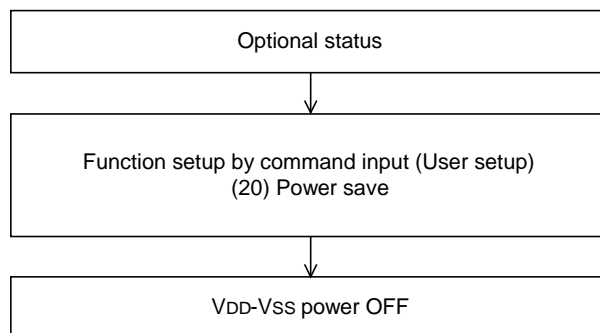


The target time of 5ms will vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct and operation check using the actual equipment.

2. Data Display



3. Power OFF



The target time of 5ms will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Absolute Maximum Rating

DC Supply Voltage (VDD, VDD2)	-0.3V to +3.6V
DC Supply Voltage (VOUT)	-0.3V to +14.0V
DC Supply Voltage (V0)	-0.3V to +13.5V
Input Voltage (Vin)	-0.3V to VDD+0.3V
Operating Ambient Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

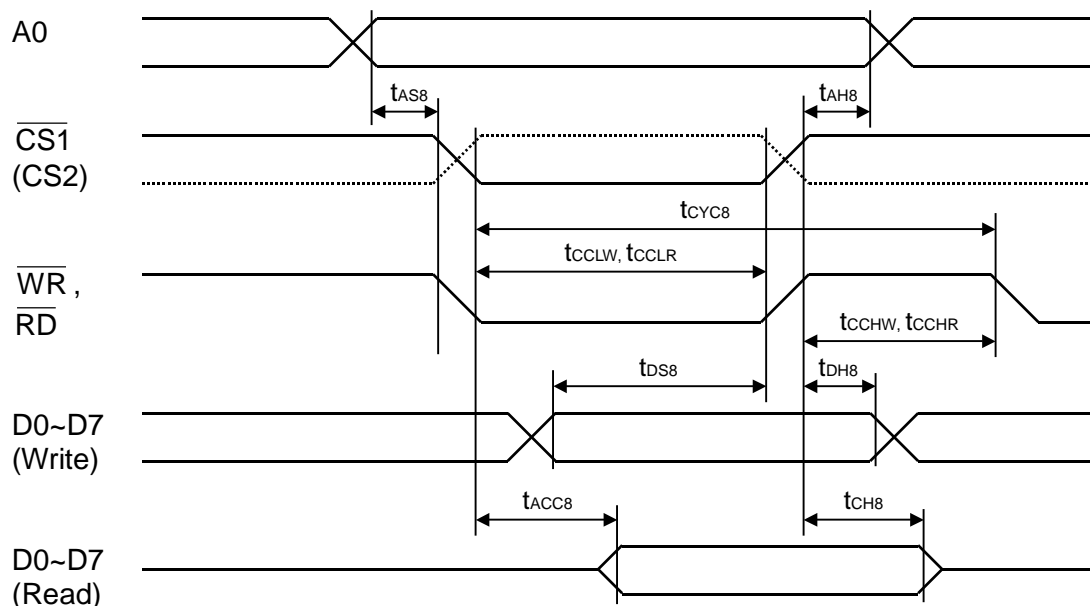
DC Characteristics (VSS = 0V, VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.4	-	3.5	V	
VDD2	Operating Voltage	2.4	-	3.5	V	
VOUT	Booster Output Voltage	6.0	-	12.0	V	
V0	Voltage Regulator Operating Voltage	4.5	-	11.5	V	
VREG	Reference Voltage	2.04	2.10	2.16	V	Ta = 25°C, -0.05%/°C
IDD1	Dynamic Current Consumption 1	-	21	35	μA	VDD = 3V, V0 = 11V, built-in power supply off, display on, display data = checker and no access, Ta = 25°C
IDD2	Dynamic Current Consumption 2	-	96	160	μA	4X boosting, VDD, VDD2 = 3V, V0 = 11V, built-in power supply on, display on, display data = checker and no access, temperature gradient is -0.05%/°C, Ta = 25°C, when V0 voltage internal resistor is used, normal mode.
IDD3	Dynamic Current Consumption 3	-	153	255	μA	4X boosting, VDD, VDD2 = 3V, V0 = 11V, built-in power supply on, display on, display data = checker and no access, temperature gradient is -0.05%/°C, Ta = 25°C, when V0 voltage internal resistor is used, high power mode.
ISP	Sleep Mode Current Consumption	-	0.01	5	μA	During sleep, Ta = 25°C
ISB	Standby Mode Current Consumption	-	4	8	μA	During standby, Ta = 25°C

DC Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VIHC	High-Level Input Voltage	0.8 X VDD	-	VDD	V	A0, D0 - D7, \overline{RD} (E), \overline{WR} (R/ \overline{W}), $\overline{CS1}$, $\overline{CS2}$, CLS, CL, FR, M/S, C86, P/S, \overline{DOF} , \overline{RES} , VRS, IRS and \overline{HPM}
VILC	Low-Level Input Voltage	VSS	-	0.2 X VDD	V	
VOHC	High-Level Output Voltage	0.8 X VDD	-	VDD	V	IOH = -0.5mA (D0 - D7, FR, FRS, \overline{DOF} , and CL)
VOLC	Low -Level Output Voltage	VDD	-	0.2 X VDD	V	IOL = 0.5mA (D0 - D7, FR, FRS, \overline{DOF} , and CL)
ILI	Input Leakage Current	-1.0	-	1.0	μ A	Vin = VDD or VSS (A0, \overline{RD} (E), \overline{WR} (R/ \overline{W}), $\overline{CS1}$, $\overline{CS2}$, CLS, M/S, C86, P/S, IRS, VRS and \overline{RES})
IHZ	HZ Leakage Current	-3.0	-	3.0	μ A	When the D0 - D7, FR, CL, and \overline{DOF} are in high impedance
RON1	LCD Driver ON Resistance	-	2.0	3.5	K Ω	V1IN=3.3V, VMIN=1.65V, V0IN=0V, Iload=100 μ A, Ta=25°C
RON2	LCD Driver ON Resistance	-	3.2	5.4	K Ω	
CIN	Input Pad Capacity	-	5.0	8.0	pF	Ta = 25°C, f = 1MHz
fOSC	Oscillation Frequency	27	33	39	kHz	Ta = 25°C

Notes: 1. Voltages $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$ must always be satisfied.

AC Characteristics
1. System Buses Read/Write Characteristics (for 8080 Series MPU)


(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

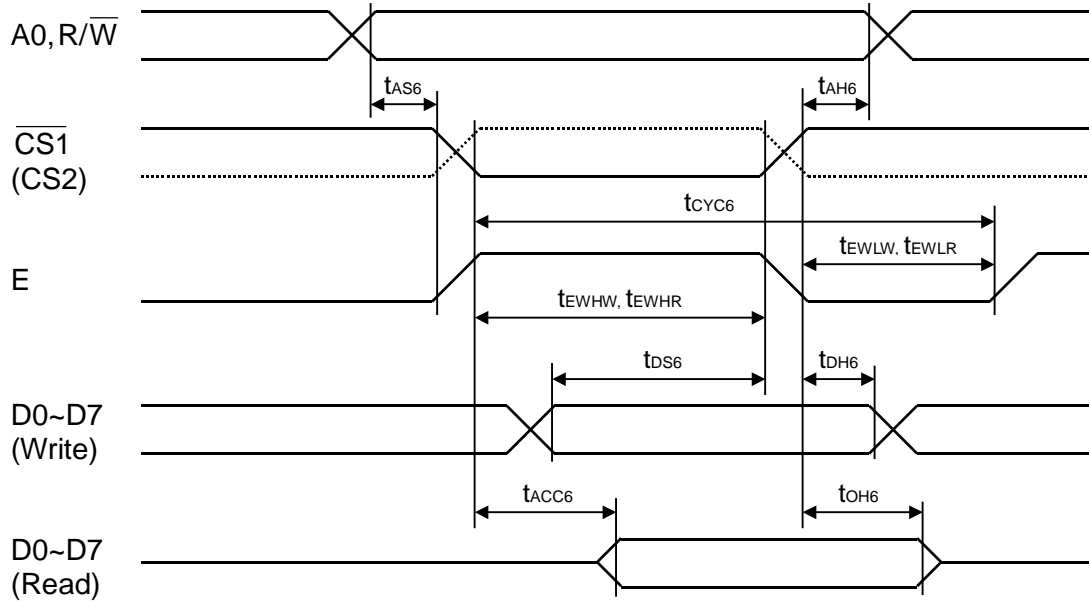
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t _{AH8}	Address hold time	0	-	-	ns	A0
t _{AS8}	Address setup time	0	-	-	ns	
t _{CYC8}	System cycle time	300	-	-	ns	
t _{CCLW}	Control low pulse width (write)	90	-	-	ns	\overline{WR}
t _{CCLR}	Control low pulse width (read)	120	-	-	ns	\overline{RD}
t _{CCHW}	Control high pulse width (write)	120	-	-	ns	\overline{WR}
t _{CCHR}	Control high pulse width (read)	60	-	-	ns	\overline{RD}
t _{DS8}	Data setup time	40	-	-	ns	D0~D7
t _{DH8}	Data hold time	15	-	-	ns	
t _{ACC8}	\overline{RD} access time	-	-	140	ns	D0~D7, CL = 100pF
t _{CH8}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (t_r , t_f) is specified at 15ns or less.

($t_r + t_f$) < ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for write, ($t_r + t_f$) < ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) for read.

*2. All timing is specified using 20% and 80% of VDD as the reference.

*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when $\overline{CS1}$ is low (CS2 is high) and \overline{WR} or \overline{RD} is low.

2. System Buses Read/Write Characteristics (for 6800 Series MPU)


(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t _{AH6}	Address hold time	0	-	-	ns	A0
t _{AS6}	Address setup time	0	-	-	ns	
t _{CYC6}	System cycle time	300	-	-	ns	
t _{EWHW}	Control low pulse width (write)	90	-	-	ns	\overline{WR}
t _{EWHR}	Control low pulse width (read)	120	-	-	ns	\overline{RD}
t _{EWLW}	Control high pulse width (write)	120	-	-	ns	\overline{WR}
t _{EWLR}	Control high pulse width (read)	60	-	-	ns	\overline{RD}
t _{DS6}	Data setup time	40	-	-	ns	D0~D7
t _{DH6}	Data hold time	15	-	-	ns	
t _{ACC6}	\overline{RD} access time	-	-	140	ns	D0~D7, CL = 100pF
t _{OH6}	Output disable time	10	-	100	ns	

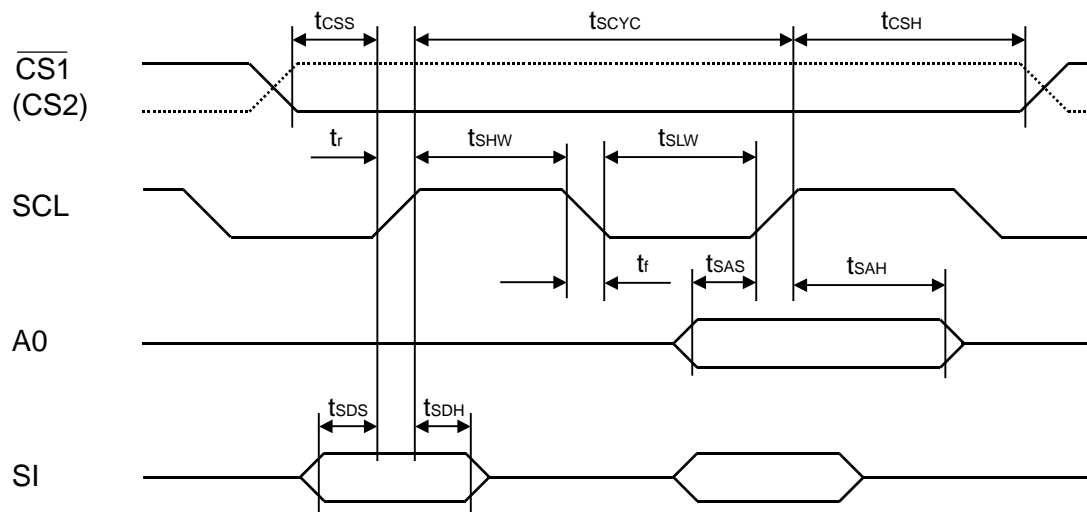
*1. The input signal rise time and fall time (t_r , t_f) is specified at 15ns or less.

($t_r + t_f$) < (t_{CYC6} - t_{EWLW} - t_{EWHW}) for write, ($t_r + t_f$) < (t_{CYC6} - t_{EWLR} - t_{EWHR}) for read.

*2. All timing is specified using 20% and 80% of VDD as the reference.

*3. t_{EWLW} and t_{EWLR} are specified as the overlap interval when $\overline{CS1}$ is low (CS2 is high) and E is high.

3. Serial Interface Timing



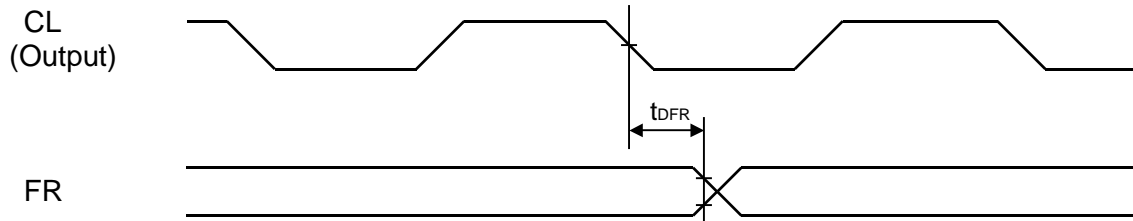
(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tscyc	Serial clock cycle	250	-	-	ns	SCL
tshw	Serial clock H pulse width	100	-	-	ns	SCL
tslw	Serial clock L pulse width	100	-	-	ns	SCL
tsAS	Address setup time	150	-	-	ns	D/I
tsAH	Address hold time	150	-	-	ns	D/I
tSDS	Data setup time	100	-	-	ns	SDI
tSDH	Data hold time	100	-	-	ns	SDI
tcss	Chip select setup time	150	-	-	ns	$\overline{\text{CS1}}$, CS2
tcsH	Chip select hold time	150	-	-	ns	$\overline{\text{CS1}}$, CS2

*1. The input signal rise time and fall time (t_r , t_f) is specified at 15ns or less.

*2. All timing is specified using 20% and 80% of VDD as the standard.

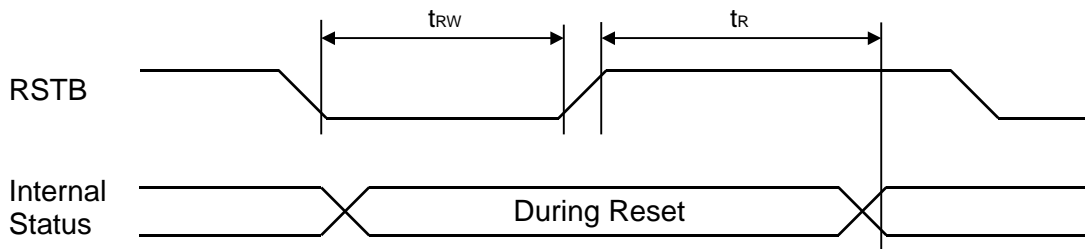
4. Display Control Timing



(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

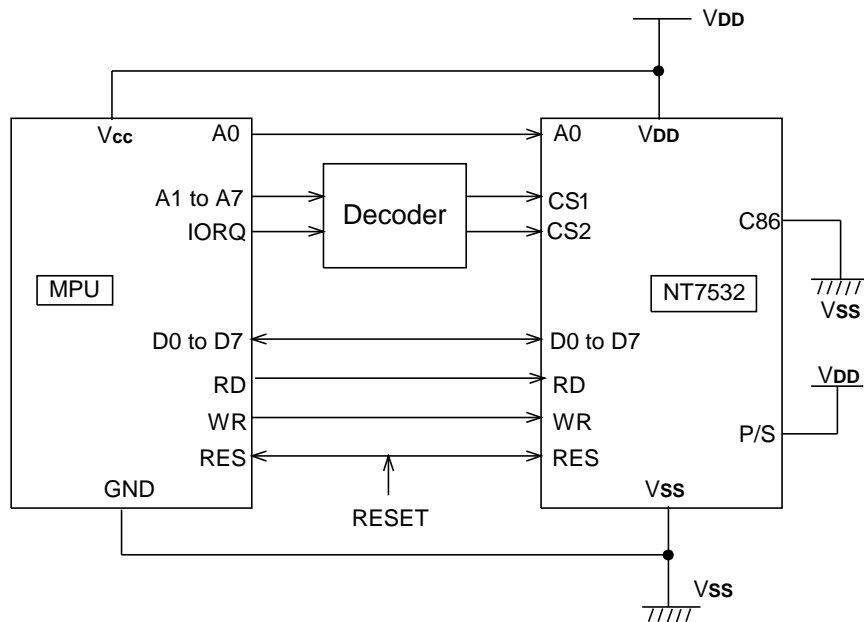
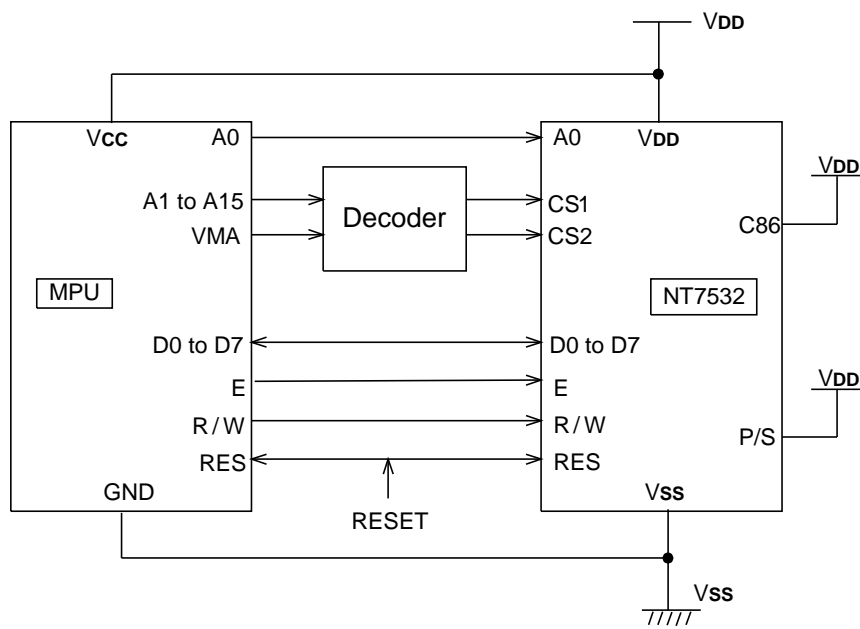
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{dFR}	FR delay time	-	20	80	ns	CL = 50 pF

5. Reset Timing



(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_r	Reset Time	-	-	1.0	μ s	
t_{rw}	Reset low pulse width	1.0	-	-	μ s	\overline{RES}

Microprocessor Interface (for reference only)
8080-series microprocessors

Figure. 8
6800-series microprocessors

Figure. 9

Connections between LCD Drivers (for reference only)

The liquid crystal display area can be enlarged with ease through the use of multiple NT7532 chips. Use same equipment type.

NT7532 (master) ↔ NT7532 (slave)

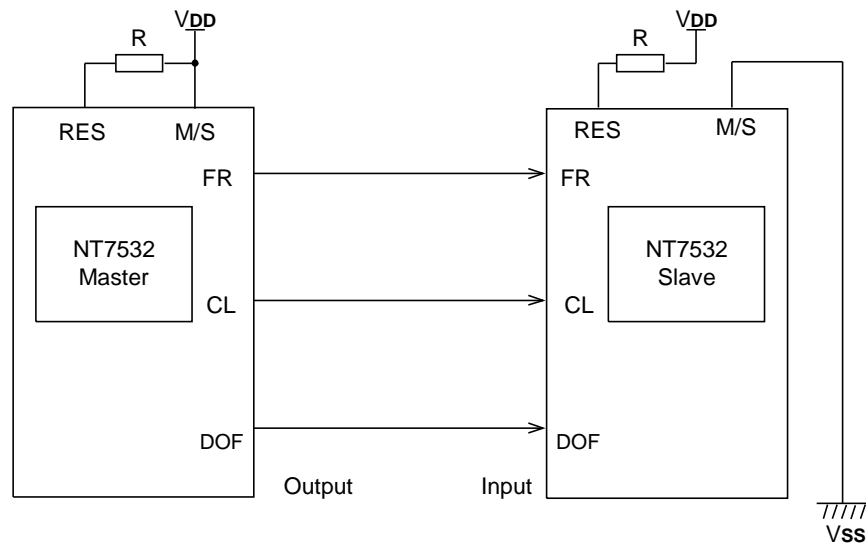
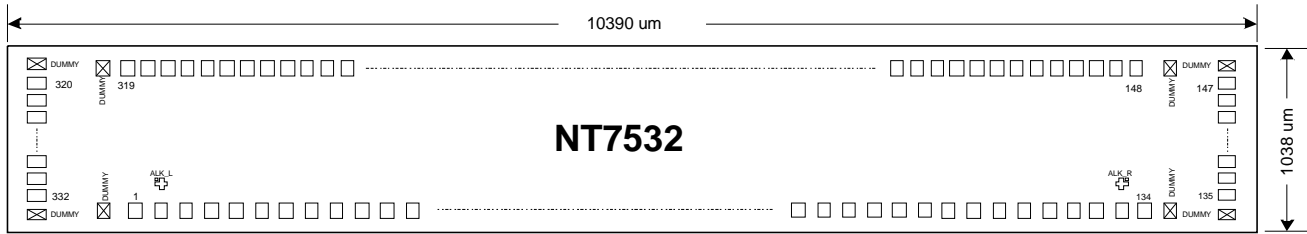


Figure. 10

Bonding Diagram


Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	NC	-4655.0	-379.0	30	D0	-2625.0	-379.0
2	FRS	-4585.0	-379.0	31	NC	-2555.0	-379.0
3	FR	-4515.0	-379.0	32	D1	-2485.0	-379.0
4	CL	-4445.0	-379.0	33	D1	-2415.0	-379.0
5	/DOF	-4375.0	-379.0	34	NC	-2345.0	-379.0
6	VSS	-4305.0	-379.0	35	D2	-2275.0	-379.0
7	/CS1	-4235.0	-379.0	36	D2	-2205.0	-379.0
8	/CS1	-4165.0	-379.0	37	NC	-2135.0	-379.0
9	/CS1	-4095.0	-379.0	38	D3	-2065.0	-379.0
10	CS2	-4025.0	-379.0	39	D3	-1995.0	-379.0
11	CS2	-3955.0	-379.0	40	NC	-1925.0	-379.0
12	CS2	-3885.0	-379.0	41	D4	-1855.0	-379.0
13	VDD	-3815.0	-379.0	42	D4	-1785.0	-379.0
14	/RES	-3745.0	-379.0	43	NC	-1715.0	-379.0
15	/RES	-3675.0	-379.0	44	D5	-1645.0	-379.0
16	/RES	-3605.0	-379.0	45	D5	-1575.0	-379.0
17	A0	-3535.0	-379.0	46	NC	-1505.0	-379.0
18	A0	-3465.0	-379.0	47	D6	-1435.0	-379.0
19	A0	-3395.0	-379.0	48	D6	-1365.0	-379.0
20	VSS	-3325.0	-379.0	49	NC	-1295.0	-379.0
21	/WR	-3255.0	-379.0	50	D7	-1225.0	-379.0
22	/WR	-3185.0	-379.0	51	D7	-1155.0	-379.0
23	/WR	-3115.0	-379.0	52	NC	-1085.0	-379.0
24	/RD	-3045.0	-379.0	53	NC	-1015.0	-379.0
25	/RD	-2975.0	-379.0	54	NC	-945.0	-379.0
26	/RD	-2905.0	-379.0	55	NC	-875.0	-379.0
27	VDD	-2835.0	-379.0	56	VDD	-805.0	-379.0
28	TEST0	-2765.0	-379.0	57	DUTY0	-735.0	-379.0
29	D0	-2695.0	-379.0	58	VSS	-665.0	-379.0

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
59	DUTY1	-595.0	-379.0	93	CAP2+	1785.0	-379.0
60	VDD	-525.0	-379.0	94	CAP2+	1855.0	-379.0
61	VDD	-455.0	-379.0	95	CAP2-	1925.0	-379.0
62	VDD	-385.0	-379.0	96	CAP2-	1995.0	-379.0
63	VDD	-315.0	-379.0	97	CAP2-	2065.0	-379.0
64	VDD2	-245.0	-379.0	98	CAP2-	2135.0	-379.0
65	VDD2	-175.0	-379.0	99	VSS	2205.0	-379.0
66	VDD2	-105.0	-379.0	100	VEXT	2275.0	-379.0
67	VDD2	-35.0	-379.0	101	VRS	2345.0	-379.0
68	VSS	35.0	-379.0	102	VDD	2415.0	-379.0
69	VSS	105.0	-379.0	103	V1	2485.0	-379.0
70	VSS	175.0	-379.0	104	V1	2555.0	-379.0
71	VSS	245.0	-379.0	105	V1	2625.0	-379.0
72	VSS2	315.0	-379.0	106	V2	2695.0	-379.0
73	VSS2	385.0	-379.0	107	V2	2765.0	-379.0
74	VSS2	455.0	-379.0	108	V2	2835.0	-379.0
75	VSS2	525.0	-379.0	109	V3	2905.0	-379.0
76	VOUT	595.0	-379.0	110	V3	2975.0	-379.0
77	VOUT	665.0	-379.0	111	V3	3045.0	-379.0
78	VOUT	735.0	-379.0	112	V4	3115.0	-379.0
79	CAP3+	805.0	-379.0	113	V4	3185.0	-379.0
80	CAP3+	875.0	-379.0	114	V4	3255.0	-379.0
81	CAP3+	945.0	-379.0	115	V0	3325.0	-379.0
82	CAP3+	1015.0	-379.0	116	V0	3395.0	-379.0
83	CAP1-	1085.0	-379.0	117	V0	3465.0	-379.0
84	CAP1-	1155.0	-379.0	118	VR	3535.0	-379.0
85	CAP1-	1225.0	-379.0	119	VR	3605.0	-379.0
86	CAP1-	1295.0	-379.0	120	VSS	3675.0	-379.0
87	CAP1+	1365.0	-379.0	121	VSS	3745.0	-379.0
88	CAP1+	1435.0	-379.0	122	VDD	3815.0	-379.0
89	CAP1+	1505.0	-379.0	123	M/S	3885.0	-379.0
90	CAP1+	1575.0	-379.0	124	CLS	3955.0	-379.0
91	CAP2+	1645.0	-379.0	125	VSS	4025.0	-379.0
92	CAP2+	1715.0	-379.0	126	C86	4095.0	-379.0

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
127	PS	4165.0	-379.0	163	COM3	3877.5	379.0
128	VDD	4235.0	-379.0	164	COM2	3822.5	379.0
129	/HPM	4305.0	-379.0	165	COM1	3767.5	379.0
130	VSS	4375.0	-379.0	166	COM0	3712.5	379.0
131	IRS	4445.0	-379.0	167	COMS	3657.5	379.0
132	VDD	4515.0	-379.0	168	SEG0	3602.5	379.0
133	NC	4585.0	-379.0	169	SEG1	3547.5	379.0
134	VSS	4655.0	-379.0	170	SEG2	3492.5	379.0
135	COM31	5059.0	-330.0	171	SEG3	3437.5	379.0
136	COM30	5059.0	-275.0	172	SEG4	3382.5	379.0
137	COM29	5059.0	-220.0	173	SEG5	3327.5	379.0
138	COM28	5059.0	-165.0	174	SEG6	3272.5	379.0
139	COM27	5059.0	-110.0	175	SEG7	3217.5	379.0
140	COM26	5059.0	-55.0	176	SEG8	3162.5	379.0
141	COM25	5059.0	0.0	177	SEG9	3107.5	379.0
142	COM24	5059.0	55.0	178	SEG10	3052.5	379.0
143	COM23	5059.0	110.0	179	SEG11	2997.5	379.0
144	COM22	5059.0	165.0	180	SEG12	2942.5	379.0
145	COM21	5059.0	220.0	181	SEG13	2887.5	379.0
146	COM20	5059.0	275.0	182	SEG14	2832.5	379.0
147	COM19	5059.0	330.0	183	SEG15	2777.5	379.0
148	COM18	4702.5	379.0	184	SEG16	2722.5	379.0
149	COM17	4647.5	379.0	185	SEG17	2667.5	379.0
150	COM16	4592.5	379.0	186	SEG18	2612.5	379.0
151	COM15	4537.5	379.0	187	SEG19	2557.5	379.0
152	COM14	4482.5	379.0	188	SEG20	2502.5	379.0
153	COM13	4427.5	379.0	189	SEG21	2447.5	379.0
154	COM12	4372.5	379.0	190	SEG22	2392.5	379.0
155	COM11	4317.5	379.0	191	SEG23	2337.5	379.0
156	COM10	4262.5	379.0	192	SEG24	2282.5	379.0
157	COM9	4207.5	379.0	193	SEG25	2227.5	379.0
158	COM8	4152.5	379.0	194	SEG26	2172.5	379.0
159	COM7	4097.5	379.0	195	SEG27	2117.5	379.0
160	COM6	4042.5	379.0	196	SEG28	2062.5	379.0
161	COM5	3987.5	379.0	197	SEG29	2007.5	379.0
162	COM4	3932.5	379.0	198	SEG30	1952.5	379.0

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
199	SEG31	1897.5	379.0	235	SEG67	-82.5	379.0
200	SEG32	1842.5	379.0	236	SEG68	-137.5	379.0
201	SEG33	1787.5	379.0	237	SEG69	-192.5	379.0
202	SEG34	1732.5	379.0	238	SEG70	-247.5	379.0
203	SEG35	1677.5	379.0	239	SEG71	-302.5	379.0
204	SEG36	1622.5	379.0	240	SEG72	-357.5	379.0
205	SEG37	1567.5	379.0	241	SEG73	-412.5	379.0
206	SEG38	1512.5	379.0	242	SEG74	-467.5	379.0
207	SEG39	1457.5	379.0	243	SEG75	-522.5	379.0
208	SEG40	1402.5	379.0	244	SEG76	-577.5	379.0
209	SEG41	1347.5	379.0	245	SEG77	-632.5	379.0
210	SEG42	1292.5	379.0	246	SEG78	-687.5	379.0
211	SEG43	1237.5	379.0	247	SEG79	-742.5	379.0
212	SEG44	1182.5	379.0	248	SEG80	-797.5	379.0
213	SEG45	1127.5	379.0	249	SEG81	-852.5	379.0
214	SEG46	1072.5	379.0	250	SEG82	-907.5	379.0
215	SEG47	1017.5	379.0	251	SEG83	-962.5	379.0
216	SEG48	962.5	379.0	252	SEG84	-1017.5	379.0
217	SEG49	907.5	379.0	253	SEG85	-1072.5	379.0
218	SEG50	852.5	379.0	254	SEG86	-1127.5	379.0
219	SEG51	797.5	379.0	255	SEG87	-1182.5	379.0
220	SEG52	742.5	379.0	256	SEG88	-1237.5	379.0
221	SEG53	687.5	379.0	257	SEG89	-1292.5	379.0
222	SEG54	632.5	379.0	258	SEG90	-1347.5	379.0
223	SEG55	577.5	379.0	259	SEG91	-1402.5	379.0
224	SEG56	522.5	379.0	260	SEG92	-1457.5	379.0
225	SEG57	467.5	379.0	261	SEG93	-1512.5	379.0
226	SEG58	412.5	379.0	262	SEG94	-1567.5	379.0
227	SEG59	357.5	379.0	263	SEG95	-1622.5	379.0
228	SEG60	302.5	379.0	264	SEG96	-1677.5	379.0
229	SEG61	247.5	379.0	265	SEG97	-1732.5	379.0
230	SEG62	192.5	379.0	266	SEG98	-1787.5	379.0
231	SEG63	137.5	379.0	267	SEG99	-1842.5	379.0
232	SEG64	82.5	379.0	268	SEG100	-1897.5	379.0
233	SEG65	27.5	379.0	269	SEG101	-1952.5	379.0
234	SEG66	-27.5	379.0	270	SEG102	-2007.5	379.0

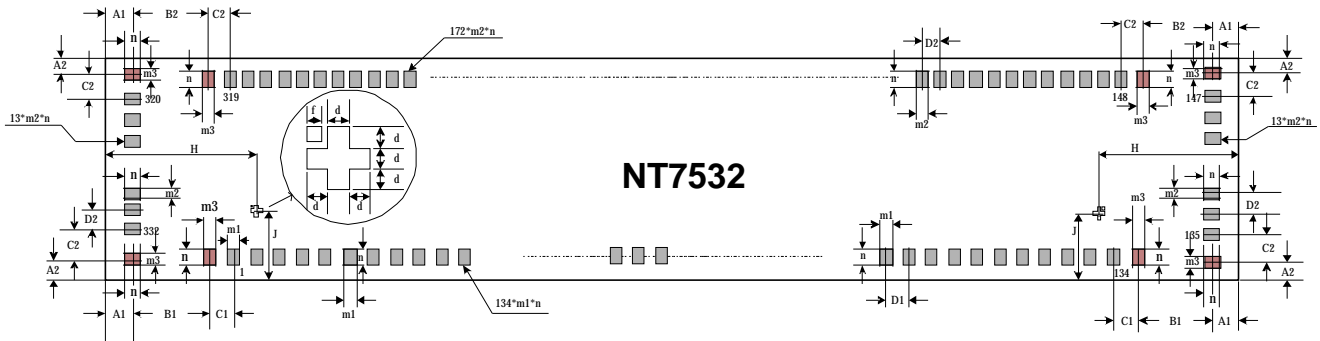
Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
271	SEG103	-2062.5	379.0	302	COM34	-3767.5	379.0
272	SEG104	-2117.5	379.0	303	COM35	-3822.5	379.0
273	SEG105	-2172.5	379.0	304	COM36	-3877.5	379.0
274	SEG106	-2227.5	379.0	305	COM37	-3932.5	379.0
275	SEG107	-2282.5	379.0	306	COM38	-3987.5	379.0
276	SEG108	-2337.5	379.0	307	COM39	-4042.5	379.0
277	SEG109	-2392.5	379.0	308	COM40	-4097.5	379.0
278	SEG110	-2447.5	379.0	309	COM41	-4152.5	379.0
279	SEG111	-2502.5	379.0	310	COM42	-4207.5	379.0
280	SEG112	-2557.5	379.0	311	COM43	-4262.5	379.0
281	SEG113	-2612.5	379.0	312	COM44	-4317.5	379.0
282	SEG114	-2667.5	379.0	313	COM45	-4372.5	379.0
283	SEG115	-2722.5	379.0	314	COM46	-4427.5	379.0
284	SEG116	-2777.5	379.0	315	COM47	-4482.5	379.0
285	SEG117	-2832.5	379.0	316	COM48	-4537.5	379.0
286	SEG118	-2887.5	379.0	317	COM49	-4592.5	379.0
287	SEG119	-2942.5	379.0	318	COM50	-4647.5	379.0
288	SEG120	-2997.5	379.0	319	COM51	-4702.5	379.0
289	SEG121	-3052.5	379.0	320	COM52	-5059.0	330.0
290	SEG122	-3107.5	379.0	321	COM53	-5059.0	275.0
291	SEG123	-3162.5	379.0	322	COM54	-5059.0	220.0
292	SEG124	-3217.5	379.0	323	COM55	-5059.0	165.0
293	SEG125	-3272.5	379.0	324	COM56	-5059.0	110.0
294	SEG126	-3327.5	379.0	325	COM57	-5059.0	55.0
295	SEG127	-3382.5	379.0	326	COM58	-5059.0	0
296	SEG128	-3437.5	379.0	327	COM59	-5059.0	-55.0
297	SEG129	-3492.5	379.0	328	COM60	-5059.0	-110.0
298	SEG130	-3547.5	379.0	329	COM61	-5059.0	-165.0
299	SEG131	-3602.5	379.0	330	COM62	-5059.0	-220.0
300	COM32	-3657.5	379.0	331	COM63	-5059.0	-275.0
301	COM33	-3712.5	379.0	332	COMS	-5059.0	-330.0

Dummy Pad Location (Total: 8 pins)

NO	X	Y	NO	X	Y	NO	X	Y
0	-4745.0	-379.0	3	5059.0	390.0	6	-5059.0	390.0
1	4745.0	-379.0	4	4762.5	379.0	7	-5059.0	-390.0
2	5059.0	-390.0	5	-4762.5	379.0			

Alignment Mark Location (Total: 2 pins)

NO	X	Y
L	-4581.0	-143.0
R	4581.0	-143.0

Package Information

Chip Outline Dimensions unit: μm

Symbol	Dimensions in mm	Symbol	Dimensions in mm
A1	136	D2	55
A2	129	m1	42
B1	314	m2	35
B2	296.5	m3	45
C1	90	n	90
C2	60	d	30
D1	70	f	20

Bump Area:

1. Input (pad 1 ~ pad 134) = $42\mu\text{m} \times 90\mu\text{m}$
2. Output (pad 135 ~ pad 332) = $35\mu\text{m} \times 90\mu\text{m}$
3. Dummy (0 ~ 7) = $45\mu\text{m} \times 90\mu\text{m}$

Bump Height:
15 +/- 3 μm

Ordering Information

Part No.	Packages
NT7532H-BDT	Gold Bump on Chip Tray