LG4525B

528-Channel, 262,144-Color One-Chip Driver with RAM, Power Supply and Gate Circuits for Amorphous TFT-LCD Panels

Ver 0.30
2009-03-04

Description

The LG4525B is a one-chip liquid crystal controller driver LSI, comprising RAM of 176 RGB x 220 dots at maximum, a source driver, a gate driver and a power supply circuit. For effective data transfer, the LG4525B supports high-speed 8-/9-/16-/18-bit bus interfaces as a system interface to microcomputer and high-speed RAM write mode.
As a moving picture interface, the LG4525B supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0).
Also, the LG4525B incorporates step-up circuits and voltage follower circuits to generate TFT liquid crystal panel drive voltages.
The LG4525B's power management functions such as 8-color display and deep standby and so on make this LSI an ideal driver for the medium or small sized portable products with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- A one-chip controller driver incorporating a gate circuit and a power supply circuit for 176RGB x220 dots graphics display on an amorphous TFT panel in 262k colors
- System interface
  - High-speed interfaces via 8-, 9-, 16-, 18-bit parallel ports
  - Serial interface
- Interface for moving picture display
  - 6-, 16-, 18-bit bus RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  - VSYNC interface (System interface + VSYNC)
  - FLM interface (System interface + FLM)
- Window address function to specify a rectangular area on the internal RAM to write data
- Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
  - Resizing function (x 1/2, x 1/4)
- Abundant color display and drawing functions
  - Programmable γ -correction function for 262k-color display
  - Partial display function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
  - Standby, Deep standby, sleep function
  - 8-color display function
  - Input power supply voltages: VCI = 2.5V ~ 3.3V (logic analog circuit power supply)
VDD3 = 1.65V ~ 3.3V (interface I/O power supply)
VCI ≥ VDD3
- Incorporates a liquid crystal drive power supply circuit
  - Source/Vcom power supply: AVDD = (GVDD+0.5)V ~ 6.0V
VCI-VCL ≤ 6.0V
  - Gate drive power supply: VGH > (AVDD+0.5)V
VGL < (VCL-0.6)V
VGH-VGL ≤ 32V
  - Vcom drive power supply: VCOMH = (VCI-0.5)V ~ (AVDD-0.5)V
VCOML = (VCL+0.5)V ~ 0V
VCOMH-VCOML ≤ 6.0V
- Liquid crystal power supply startup sequence
- TFT storage capacitance: Cst only (common VCOM formula)
- 87,120-byte internal RAM
- Internal 528-channel source driver and 220-channel gate driver
- Configures a COG module with one chip by arranging gate lines on both sides

Block Diagram

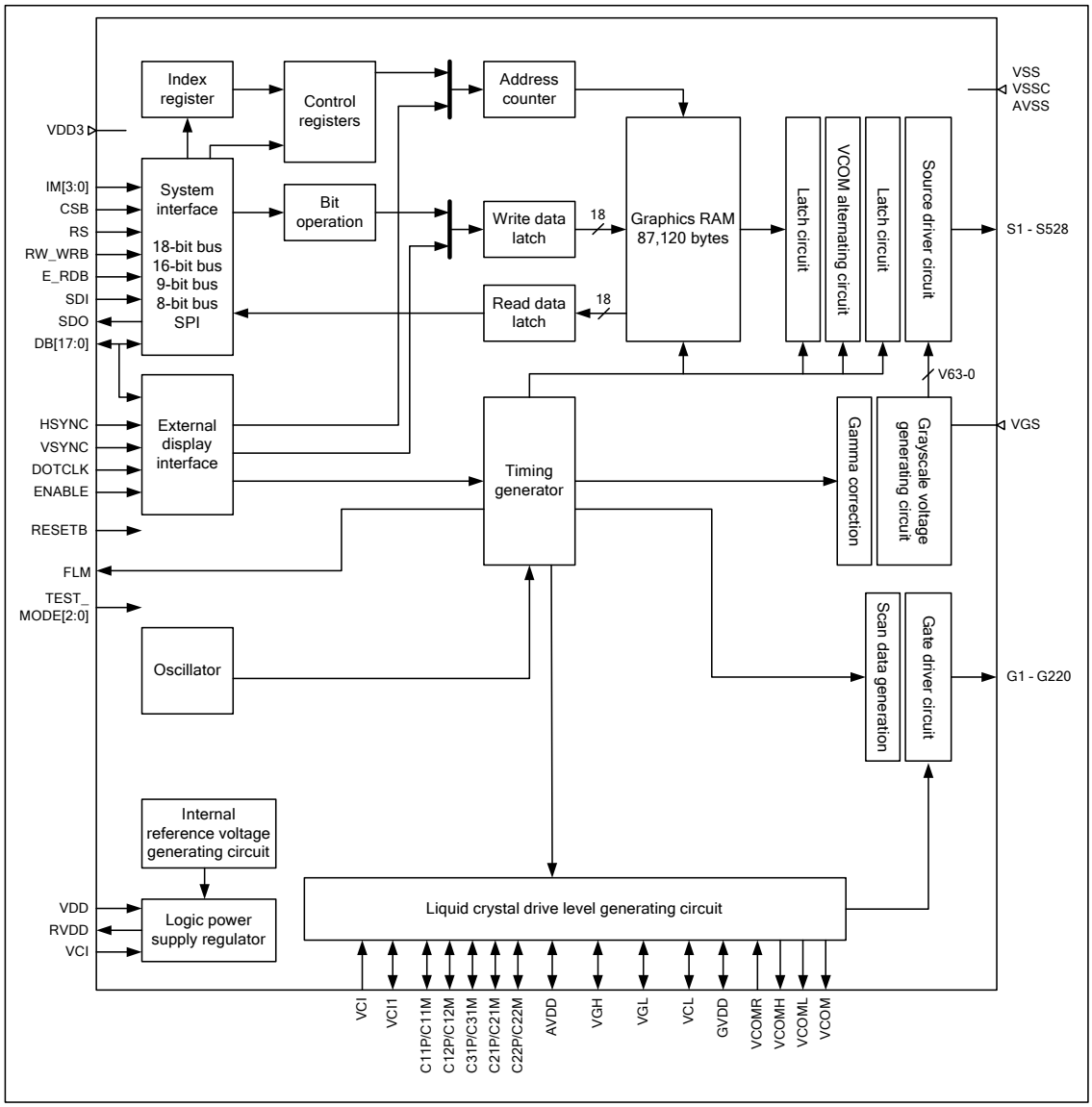


Figure 1

Pin Function

Table 1 Interface Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>IM<3:1>, IM0/ID, TEST_MODE<1></td><td>I</td><td>GND or VDD3</td><td>Select a mode to interface to an MPU. In SPI mode, the IM0 pin is used to set the ID of device code.
<table>
<tr><th>TEST_MODE<1></th><th>IM<3:0></th><th>Interface Mode</th><th>DB Pins</th></tr>
<tr><td>0</td><td>0000</td><td>68-system 16-bit interface</td><td>DB<17:10>, DB<8:1></td></tr>
<tr><td>0</td><td>0001</td><td>68-system 8-bit interface 1</td><td>DB<17:10></td></tr>
<tr><td>0</td><td>0010</td><td>80-system 16-bit interface</td><td>DB<17:10>, DB<8:1></td></tr>
<tr><td>0</td><td>0011</td><td>80-system 8-bit interface 1</td><td>DB<17:10></td></tr>
<tr><td>0</td><td>010/ID</td><td>Serial peripheral interface(SPI)</td><td>SDI, SDO</td></tr>
<tr><td>0</td><td>1000</td><td>68-system 18-bit interface</td><td>DB<17:0></td></tr>
<tr><td>0</td><td>1001</td><td>68-system 9-bit interface 1</td><td>DB<17:9></td></tr>
<tr><td>0</td><td>1010</td><td>80-system 18-bit interface</td><td>DB<17:0></td></tr>
<tr><td>0</td><td>1011</td><td>80-system 9-bit interface 1</td><td>DB<17:9></td></tr>
<tr><td>1</td><td>0001</td><td>68-system 8-bit interface 2</td><td>DB<8:1></td></tr>
<tr><td>1</td><td>1001</td><td>68-system 9-bit interface 2</td><td>DB<8:0></td></tr>
<tr><td>1</td><td>0011</td><td>80-system 8-bit interface 2</td><td>DB<8:1></td></tr>
<tr><td>1</td><td>1011</td><td>80-system 9-bit interface 2</td><td>DB<8:0></td></tr>
</table></td></tr>
<tr><td>CSB</td><td>I</td><td>MPU</td><td>Chip select signal (active low).
Low: LG4525B is selected and accessible.
High: LG4525B is not selected and not accessible.
Fix to the GND level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal.
Low: selects the index/status register.
High: selects a control register.</td></tr>
<tr><td>RW_WRB</td><td>I</td><td>MPU</td><td>Write strobe (active low) in 80-system bus interface mode.
Serial clock input in SPI mode.</td></tr>
<tr><td>E_RDB</td><td>I</td><td>MPU</td><td>Read strobe (active low) in 80-system bus interface mode. Fix to either VDD3 or GND level in SPI mode.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>Serial data input in SPI mode.
Data are input on the rising edge of the SCL signal. Fix to either VDD3 or GND level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU</td><td>Serial data output in SPI mode.
Data are output on the falling edge of the SCL signal. Leave the pin open when not in use.</td></tr>
<tr><td>DB<0> ~ DB<17></td><td>I/O</td><td>MPU</td><td>Parallel bidirectional data bus.
Unused pins must be fixed either VDD3 or GND level.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU</td><td>Data enable signal in RGB interface mode.
Low: select (accessible).
High: not select (inaccessible).
The EPL bit inverts the polarity of the ENABLE signal. Fix to either VDD3 or GND level when not in use.</td></tr>
</table>

VSYNC	I	MPU	Frame synchronization signal. When VSPL = “0”, it is active low. When VSPL = “1”, it is active high. Fix to either VDD3 or GND level when not in use.
HSYNC	I	MPU	Line synchronization signal. When HSPL = “0”, it is active low. When HSPL = “1”, it is active high. Fix to either VDD3 or GND level when not in use.
DOTCLK	I	MPU	Dot clock signal. When DPL = “0”, input data on the rising edge of DOTCLK. When DPL = “1”, input data on the falling edge of DOTCLK. Fix to either VDD3 or GND level when not in use.
RESETB	I	MPU or External RC circuit	Hardware reset (active low). Be sure to execute a power-on reset after supplying power.
FLM	O	MPU	Frame head pulse signal. This is used when writing RAM data in synchronization with display frame. Leave the pin open when not in use.

Table 2 Power Supply Pins

Signal	I/O	Connected to	Function
VCI	-	Power supply	Power supply to generate the internal logic power supply. Supply voltage to the analog circuit. Connect to an external power supply of 2.5 to 3.3V.
VCI1	-	Power supply	Internal reference voltage level of amplitude VCI−GND. Place a stabilizing capacitor between GND. Reference voltage input to the step-up circuit 1. When not using the internal reference voltage, connect to an external power supply up to 2.75V.
VDD	-	Power supply	Generated power supply to the internal logic. VDD = 1.7 to 1.9V
RVDD	-	Power supply	Internal logic regulator output.
VDD3	O	Stabilizing capacitor	Power supply to the interface pins: VDD3 = 1.65 to 3.3V. VDD3 and the internal logic voltage VDD must be supplied in the same condition. In case of COG, connect to VDD on the FPC if VDD3 = VDD to prevent noise.
VSS, AVSS, VSSC	-	Power supply	Circuit ground : GND = 0V.

Table 3 Step-Up Circuit

Signal	I/O	Connected to	Function

AVDD	I	Stabilizing capacitor, Schottky diode	Output voltage from the step-up circuit 1. Place a stabilizing capacitor between GND. Place a schottky diode between VGH. AVDD = 4.5 to 5.5V (twice the VCI1 level).Power supply to the source driver's LCD output unit and an input voltage to the step-up circuit 2.
VGH	I	Stabilizing capacitor, Schottky diode	An output voltage from the step-up circuit 2. The step-up rate is set with the BT bits. Place a stabilizing capacitor between GND. Place a schottky diode between AVDD. VGH = max 16.5V (4 to 6 times the VCI1 level) A supply voltage to drive gate lines of the TFT panel.
VGL	I	Stabilizing capacitor, Schottky diode	An output voltage from the step-up circuit 2. The step-up rate is set with the BT bits. Place a stabilizing capacitor between GND. Place a schottky diode between GND. VGL = min −16.5V (−3 to −5 times the VCI1 level) A supply voltage to drive gate lines of the TFT panel.
VCL	I	Stabilizing capacitor	An output voltage from the step-up circuit 2. Place a stabilizing capacitor between GND. VCL = 0 to −3.3V (−1 times the VCI1 level) A supply voltage to generate the VCOML level.
C11P, C11M	I/O	Step-up capacitor	Pins to connect a capacitor for the internal step-up circuit 1.
C12P, C12M	I/O	Step-up capacitor or GND or OPEN	Pins to connect a capacitor when using the dual mode step-up1 circuit. Leave the pins open or connect to GND, when not using the dual mode step-up1 circuit.
C31P, C31M C21P, C21M C22P, C22M	I/O	Step-up capacitor	Pins to connect capacitors for the internal step-up circuit 2. Connect capacitors according to step-up rate. Leave the pins open when not using the circuit.

Table 4 LCD Drive

Signal	I/O	Connected to	Function
GVDD	O	Stabilizing capacitor	A voltage level of AVDD−GND, generated from the reference level of VCI−GND according to the rate set with the VRH bits. GVDD is (1) a source driver grayscale reference voltage VDH, (2) a VCOMH level reference voltage, and (3) a VCOM amplitude reference voltage. Connect to a stabilizing capacitor. GVDD = 3.0 to (AVDD – 0.5) V. When using a variable resistor for VCOMH(VCOMR), place the resister between GVDD and GND.
VCOM	O	TFT panel common electrode	Supply voltage to the common electrode of TFT panel. VCOM is AC voltages alternating between the VCOMH and VCOML levels. The alternating cycle is set by M signal. Connect to the common electrode of TFT panel. All outputs come from the same node.

VCOMH	O	Stabilizing capacitor	The high level of VCOM AC voltage. Connect to a stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The low level of VCOM AC voltage. Adjust the VCOML level with the VDV bits. Connect to a stabilizing capacitor. To fix the VCOML level to GND, set VCOMG to “0”. In this case, capacitor connection is not necessary.
VCOMR	I	Variable resistor or open	Reference level to generate the VCOMH level either with an externally connected variable resistor or by setting the register of the LG4525B. When using a variable resistor, halt the internal VCOMH adjusting circuit by setting the register and place the resister between GVDD and GND. When generating the VCOMH level by setting the register, leave this pin open.
VGS	I	GND or external resistor	Reference level for the grayscale voltage generation circuit. The VGS level can be changed by connecting to an external resistor.
S1 ~ S528	O	LCD	Source line outputs to LCD.
G1 ~ G220	O	LCD	Gate line outputs to LCD.

Table 5 Others (Test, Dummy Pins)

Signal	I/O	Connected to	Function
VREF	I/O	OPEN or stabilizing capacitor	Reference voltage pin for test.
CL1	O	OPEN	Output Pin for test purpose.
EN_EXCLK	I	OPEN	Dummy pin.
EXCLK	I	OPEN	Dummy pin.
TEST_MODE <0>	I	GND	Input Pins for test purpose.
TEST_MODE <2>	I	OPEN	Dummy pin.
TEST_MUX< 2:0>	I	VDD3, GND or OPEN	Dummy pins.
TEST_DA	I	VDD3, GND or OPEN	Dummy pin.
M	-	VDD3, GND or OPEN	Dummy pin.
CONTACT	-	-	Dummy pins.
DUMMY1~37	-	-	Dummy pins.

PAD Arrangement

- Chip size : 13798um X 602um
- Chip thickness : T.B.D
- PAD Coordination : PAD center
- Coordination origin : Chip center

- Au BUMP size
(1) 40.00um x 50.00um
No.1 - No.215

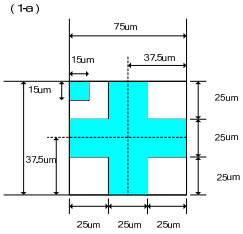
(2) 16.00um x 118.00um
No.216 - No.988

- Au BUMP pitch : see PAD coordination Table
- Au BUMP height : 12um (typ)
- No. in the figure corresponds to No. in the PAD coordination Table

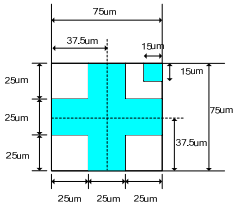
- Alignment mark

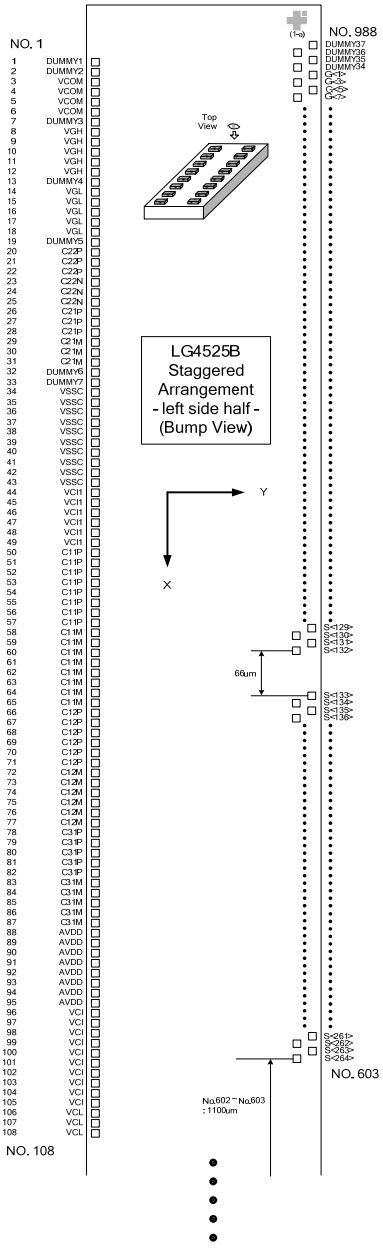
Alignment mark	X	Y
1-a (Left)	-6852.5	254.5
1-b (Right)	6852.5	254.5

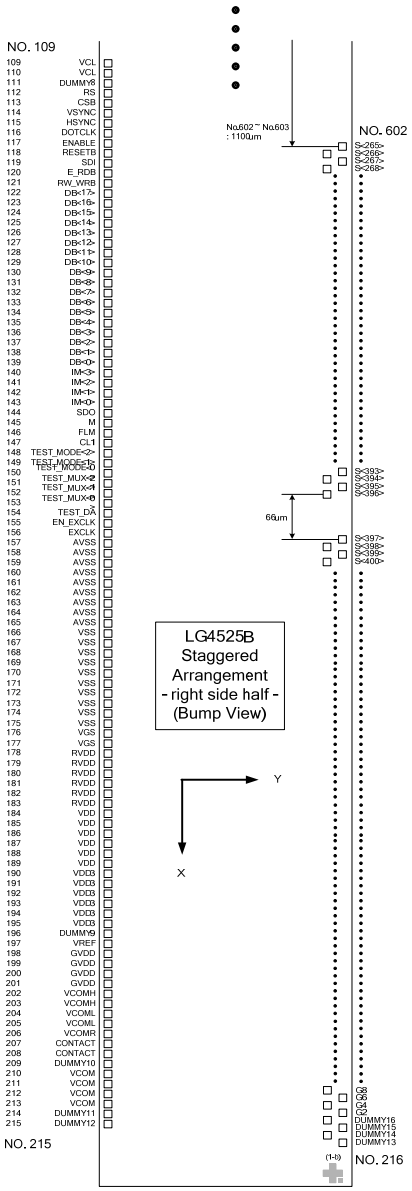
(1-a)



(1-b)







PAD Coordinate

Pad # .	PAD Name	X	Y
1	DUMMY1	-6695	-267
2	DUMMY2	-6635	-267
3	VCOM	-6575	-267
4	VCOM	-6515	-267
5	VCOM	-6455	-267
6	VCOM	-6395	-267
7	DUMMY3	-6335	-267
8	VGH	-6275	-267
9	VGH	-6215	-267
10	VGH	-6155	-267
11	VGH	-6095	-267
12	VGH	-6035	-267
13	DUMMY4	-5975	-267
14	VGL	-5915	-267
15	VGL	-5855	-267
16	VGL	-5795	-267
17	VGL	-5735	-267
18	VGL	-5675	-267
19	DUMMY5	-5615	-267
20	C22P	-5555	-267
21	C22P	-5495	-267
22	C22P	-5435	-267
23	C22M	-5375	-267
24	C22M	-5315	-267
25	C22M	-5255	-267
26	C21P	-5195	-267
27	C21P	-5135	-267
28	C21P	-5075	-267
29	C21M	-5015	-267
30	C21M	-4955	-267
31	C21M	-4895	-267
32	DUMMY6	-4835	-267
33	DUMMY7	-4775	-267
34	VSSC	-4715	-267
35	VSSC	-4655	-267
36	VSSC	-4595	-267
37	VSSC	-4535	-267
38	VSSC	-4475	-267
39	VSSC	-4415	-267
40	VSSC	-4355	-267
41	VSSC	-4295	-267
42	VSSC	-4235	-267
43	VSSC	-4175	-267
44	VCI1	-4115	-267
45	VCI1	-4055	-267
46	VCI1	-3995	-267
47	VCI1	-3935	-267
48	VCI1	-3875	-267
49	VCI1	-3815	-267
50	C11P	-3755	-267
51	C11P	-3695	-267
52	C11P	-3635	-267
53	C11P	-3575	-267
54	C11P	-3515	-267
55	C11P	-3455	-267
56	C11P	-3395	-267
57	C11P	-3335	-267
58	C11M	-3275	-267
59	C11M	-3215	-267
60	C11M	-3155	-267
61	C11M	-3095	-267
62	C11M	-3035	-267
63	C11M	-2975	-267
64	C11M	-2915	-267
65	C11M	-2855	-267
66	C12P	-2795	-267
67	C12P	-2735	-267
68	C12P	-2675	-267
69	C12P	-2615	-267
70	C12P	-2555	-267
71	C12P	-2495	-267
72	C12M	-2435	-267
73	C12M	-2375	-267
74	C12M	-2315	-267
75	C12M	-2255	-267
76	C12M	-2195	-267
77	C12M	-2135	-267
78	C31P	-2075	-267
79	C31P	-2015	-267
80	C31P	-1955	-267
81	C31P	-1895	-267
82	C31P	-1835	-267
83	C31M	-1775	-267
84	C31M	-1715	-267

Pad # .	PAD Name	X	Y
85	C31M	-1655	-267
86	C31M	-1595	-267
87	C31M	-1535	-267
88	AVDD	-1475	-267
89	AVDD	-1415	-267
90	AVDD	-1355	-267
91	AVDD	-1295	-267
92	AVDD	-1235	-267
93	AVDD	-1175	-267
94	AVDD	-1115	-267
95	AVDD	-1055	-267
96	VCI	-995	-267
97	VCI	-935	-267
98	VCI	-875	-267
99	VCI	-815	-267
100	VCI	-755	-267
101	VCI	-695	-267
102	VCI	-635	-267
103	VCI	-575	-267
104	VCI	-515	-267
105	VCI	-455	-267
106	VCL	-395	-267
107	VCL	-335	-267
108	VCL	-275	-267
109	VCL	-215	-267
110	VCL	-155	-267
111	DUMMY8	-95	-267
112	RS	-35	-267
113	CSB	25	-267
114	VSYNC	85	-267
115	HSYNC	145	-267
116	DOTCLK	205	-267
117	ENABLE	265	-267
118	RESETB	325	-267
119	SDI	385	-267
120	E_RDB	445	-267
121	RW_WRB	505	-267
122	DB<17>	565	-267
123	DB<16>	650	-267
124	DB<15>	735	-267
125	DB<14>	820	-267
126	DB<13>	905	-267
127	DB<12>	990	-267
128	DB<11>	1075	-267
129	DB<10>	1160	-267
130	DB<9>	1245	-267
131	DB<8>	1330	-267
132	DB<7>	1415	-267
133	DB<6>	1500	-267
134	DB<5>	1585	-267
135	DB<4>	1670	-267
136	DB<3>	1755	-267
137	DB<2>	1840	-267
138	DB<1>	1925	-267
139	DB<0>	2010	-267
140	IM<3>	2095	-267
141	IM<2>	2155	-267
142	IM<1>	2215	-267
143	IM<0>	2275	-267
144	SDO	2335	-267
145	M	2420	-267
146	FLM	2505	-267
147	CL1	2590	-267
148	TEST_MODE<2>	2675	-267
149	TEST_MODE<1>	2735	-267
150	TEST_MODE<0>	2795	-267
151	TEST_MUX<2>	2855	-267
152	TEST_MUX<1>	2915	-267
153	TEST_MUX<0>	2975	-267
154	TEST_DA	3035	-267
155	EN_EXCLK	3095	-267
156	EXCLK	3155	-267
157	AVSS	3215	-267
158	AVSS	3275	-267
159	AVSS	3335	-267
160	AVSS	3395	-267
161	AVSS	3455	-267
162	AVSS	3515	-267
163	AVSS	3575	-267
164	AVSS	3635	-267
165	AVSS	3695	-267
166	VSS	3755	-267
167	VSS	3815	-267
168	VSS	3875	-267

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169	VSS	3935	-267
170	VSS	3995	-267
171	VSS	4055	-267
172	VSS	4115	-267
173	VSS	4175	-267
174	VSS	4235	-267
175	VSS	4295	-267
176	VGS	4355	-267
177	VGS	4415	-267
178	RVDD	4475	-267
179	RVDD	4535	-267
180	RVDD	4595	-267
181	RVDD	4655	-267
182	RVDD	4715	-267
183	RVDD	4775	-267
184	VDD	4835	-267
185	VDD	4895	-267
186	VDD	4955	-267
187	VDD	5015	-267
188	VDD	5075	-267
189	VDD	5135	-267
190	VDD3	5195	-267
191	VDD3	5255	-267
192	VDD3	5315	-267
193	VDD3	5375	-267
194	VDD3	5435	-267
195	VDD3	5495	-267
196	DUMMY9	5555	-267
197	VREF	5615	-267
198	GVDD	5675	-267
199	GVDD	5735	-267
200	GVDD	5795	-267
201	GVDD	5855	-267
202	VCOMH	5915	-267
203	VCOMH	5975	-267
204	VCOML	6035	-267
205	VCOML	6095	-267
206	VCOMR	6155	-267
207	CONTACT	6215	-267
208	CONTACT	6275	-267
209	DUMMY10	6335	-267
210	VCOM	6395	-267
211	VCOM	6455	-267
212	VCOM	6515	-267
213	VCOM	6575	-267
214	DUMMY11	6635	-267
215	DUMMY12	6695	-267
216	DUMMY13	6772	233
217	DUMMY14	6756	80
218	DUMMY15	6740	233
219	DUMMY16	6724	80
220	G<2>	6708	233
221	G<4>	6692	80
222	G<6>	6676	233
223	G<8>	6660	80
224	G<10>	6644	233
225	G<12>	6628	80
226	G<14>	6612	233
227	G<16>	6596	80
228	G<18>	6580	233
229	G<20>	6564	80
230	G<22>	6548	233
231	G<24>	6532	80
232	G<26>	6516	233
233	G<28>	6500	80
234	G<30>	6484	233
235	G<32>	6468	80
236	G<34>	6452	233
237	G<36>	6436	80
238	G<38>	6420	233
239	G<40>	6404	80
240	G<42>	6388	233
241	G<44>	6372	80
242	G<46>	6356	233
243	G<48>	6340	80
244	G<50>	6324	233
245	G<52>	6308	80
246	G<54>	6292	233
247	G<56>	6276	80
248	G<58>	6260	233
249	G<60>	6244	80
250	G<62>	6228	233
251	G<64>	6212	80
252	G<66>	6196	233

Pad # .	PAD Name	X	Y
253	G<68>	6180	80
254	G<70>	6164	233
255	G<72>	6148	80
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856	S<11>	-4652	233
857	S<10>	-4668	80
858	S<9>	-4684	233
859	S<8>	-4700	80
860	S<7>	-4716	233
861	S<6>	-4732	80

Pad # .	PAD Name	X	Y
862	S<5>	-4748	233
863	S<4>	-4764	80
864	S<3>	-4780	233
865	S<2>	-4796	80
866	S<1>	-4812	233
867	DUMMY26	-4828	80
868	DUMMY27	-4844	233
869	DUMMY28	-4860	80
870	DUMMY29	-4876	233
871	DUMMY30	-4892	80
872	DUMMY31	-4908	233
873	DUMMY32	-4924	80
874	DUMMY33	-4940	233
875	G<219>	-4956	80
876	G<217>	-4972	233
877	G<215>	-4988	80
878	G<213>	-5004	233
879	G<211>	-5020	80
880	G<209>	-5036	233
881	G<207>	-5052	80
882	G<205>	-5068	233
883	G<203>	-5084	80
884	G<201>	-5100	233
885	G<199>	-5116	80
886	G<197>	-5132	233
887	G<195>	-5148	80
888	G<193>	-5164	233
889	G<191>	-5180	80
890	G<189>	-5196	233
891	G<187>	-5212	80
892	G<185>	-5228	233
893	G<183>	-5244	80
894	G<181>	-5260	233
895	G<179>	-5276	80
896	G<177>	-5292	233
897	G<175>	-5308	80
898	G<173>	-5324	233
899	G<171>	-5340	80
900	G<169>	-5356	233
901	G<167>	-5372	80
902	G<165>	-5388	233
903	G<163>	-5404	80
904	G<161>	-5420	233
905	G<159>	-5436	80
906	G<157>	-5452	233
907	G<155>	-5468	80
908	G<153>	-5484	233
909	G<151>	-5500	80
910	G<149>	-5516	233
911	G<147>	-5532	80
912	G<145>	-5548	233
913	G<143>	-5564	80
914	G<141>	-5580	233
915	G<139>	-5596	80
916	G<137>	-5612	233
917	G<135>	-5628	80
918	G<133>	-5644	233
919	G<131>	-5660	80
920	G<129>	-5676	233
921	G<127>	-5692	80
922	G<125>	-5708	233
923	G<123>	-5724	80
924	G<121>	-5740	233
925	G<119>	-5756	80
926	G<117>	-5772	233
927	G<115>	-5788	80
928	G<113>	-5804	233
929	G<111>	-5820	80
930	G<109>	-5836	233
931	G<107>	-5852	80
932	G<105>	-5868	233
933	G<103>	-5884	80
934	G<101>	-5900	233
935	G<99>	-5916	80
936	G<97>	-5932	233
937	G<95>	-5948	80
938	G<93>	-5964	233
939	G<91>	-5980	80
940	G<89>	-5996	233
941	G<87>	-6012	80
942	G<85>	-6028	233
943	G<83>	-6044	80
944	G<81>	-6060	233
945	G<79>	-6076	80
946	G<77>	-6092	233
947	G<75>	-6108	80
948	G<73>	-6124	233

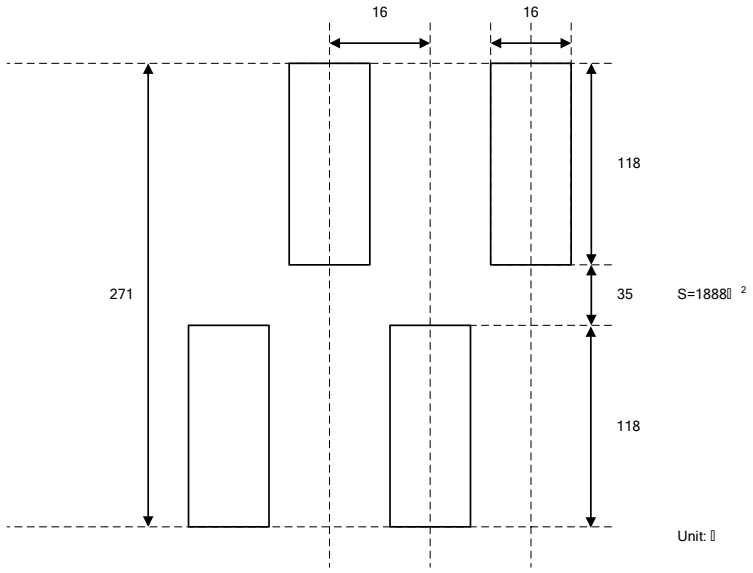
Pad # .	PAD Name	X	Y
949	G<71>	-6140	80
950	G<69>	-6156	233
951	G<67>	-6172	80
952	G<65>	-6188	233
953	G<63>	-6204	80
954	G<61>	-6220	233
955	G<59>	-6236	80
956	G<57>	-6252	233
957	G<55>	-6268	80
958	G<53>	-6284	233
959	G<51>	-6300	80
960	G<49>	-6316	233
961	G<47>	-6332	80
962	G<45>	-6348	233
963	G<43>	-6364	80
964	G<41>	-6380	233
965	G<39>	-6396	80
966	G<37>	-6412	233
967	G<35>	-6428	80
968	G<33>	-6444	233
969	G<31>	-6460	80
970	G<29>	-6476	233
971	G<27>	-6492	80
972	G<25>	-6508	233
973	G<23>	-6524	80
974	G<21>	-6540	233
975	G<19>	-6556	80
976	G<17>	-6572	233
977	G<15>	-6588	80
978	G<13>	-6604	233
979	G<11>	-6620	80
980	G<9>	-6636	233
981	G<7>	-6652	80
982	G<5>	-6668	233
983	G<3>	-6684	80
984	G<1>	-6700	233
985	DUMMY34	-6716	80
986	DUMMY35	-6732	233
987	DUMMY36	-6748	80
988	DUMMY37	-6764	233

Alignment mark	X	Y
1-a (Left)	-6852.5	254.5
1-b (Right)	6852.5	254.5

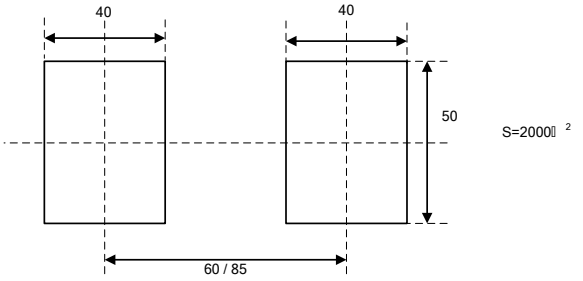
Bump Arrangement

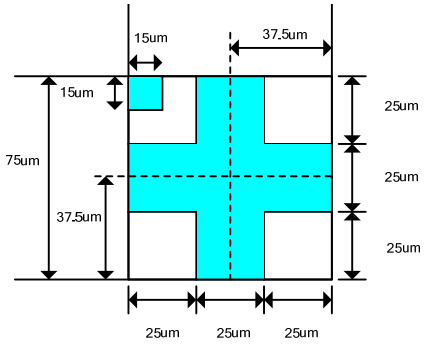
S1 ~ S528
G1 ~ G220

(No. 216 ~ No. 988)

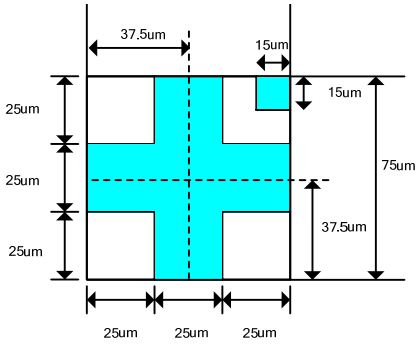


I/O PINS
(No. 1 ~ No. 215)





Alignment Mark Left (1-a)
(-6852.5 , 254.5)



Alignment Mark Right (1-b)
(6852.5 , 254.5)

Block Function

System Interface

The LG4525B supports 2-system high-speed interfaces: 80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and a Serial Peripheral Interface (SPI). The interface mode is selected by setting the IM[2:0] pins.

The LG4525B has a 16-bit index register (IR); an 18-bit write-data register (WDR); and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the LG4525B read the first data from the internal GRAM. Valid data are read out after the LG4525B performs the second read operation.

Instructions are written consecutively as the instruction execution time except starting oscillator takes 0 clock cycle.

Table 6 Register Selection (80-system 8-/9-/16-/18-bit Parallel Interface)

80-system I/F			Function
WRB	RDB	RS	
0	1	0	Write an index to IR
1	0	0	Read an internal status
0	1	1	Write to control registers or the internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 7 Register Selection (Serial Peripheral Interface)

Start Byte (SPI)		Function
R/W	RS	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

External Display Interface

The LG4525B supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB[17:0]) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section.

The LG4525B allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 87,120 (176 x 220x 18bit) bytes, using 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Register" section.

Timing Generator

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

LG4525B generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

LCD Driver Circuit

The LCD driver circuit of the LG4525B consists of a 528-output source driver (S1 ~ S528) and a 220-output gate driver (G1~G220). Display pattern data are latched when the 528th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels GVDD, VGH, VGL and VCOM for driving an LCD.

Internal logic power supply regulator

The internal logic power supply regulator generates internal logic power supply VDD.

GRAM Address MAP

Table 8 GRAM address and display panel position (SS = “0”, BGR = “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	…	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G220	“0000”H			“0001”H			“0002”H			“0003”H			…	“00AC”H			“00AD”H			“00AE”H			“00AF”H		
G2	G219	“0100”H			“0101”H			“0102”H			“0103”H			…	“01AC”H			“01AD”H			“01AE”H			“01AF”H		
G3	G218	“0200”H			“0201”H			“0202”H			“0203”H			…	“02AC”H			“02AD”H			“02AE”H			“02AF”H		
G4	G217	“0300”H			“0301”H			“0302”H			“0303”H			…	“03AC”H			“03AD”H			“03AE”H			“03AF”H		
G5	G216	“0400”H			“0401”H			“0402”H			“0403”H			…	“04AC”H			“04AD”H			“04AE”H			“04AF”H		
G6	G215	“0500”H			“0501”H			“0502”H			“0503”H			…	“05AC”H			“05AD”H			“05AE”H			“05AF”H		
G7	G214	“0600”H			“0601”H			“0602”H			“0603”H			…	“06AC”H			“06AD”H			“06AE”H			“06AF”H		
G8	G213	“0700”H			“0701”H			“0702”H			“0703”H			…	“07AC”H			“07AD”H			“07AE”H			“07AF”H		
G9	G212	“0800”H			“0801”H			“0802”H			“0803”H			…	“08AC”H			“08AD”H			“08AE”H			“08AF”H		
G10	G211	“0900”H			“0901”H			“0902”H			“0903”H			…	“09AC”H			“09AD”H			“09AE”H			“09AF”H		
G11	G210	“0A00”H			“0A01”H			“0A02”H			“0A03”H			…	“0AAC”H			“0AAD”H			“0AAE”H			“0AAF”H		
G12	G209	“0B00”H			“0B01”H			“0B02”H			“0B03”H			…	“0BAC”H			“0BAD”H			“0BAE”H			“0BAF”H		
G13	G208	“0C00”H			“0C01”H			“0C02”H			“0C03”H			…	“0CAC”H			“0CAD”H			“0CAE”H			“0CAF”H		
G14	G207	“0D00”H			“0D01”H			“0D02”H			“0D03”H			…	“0DAC”H			“0DAD”H			“0DAE”H			“0DAF”H		
G15	G206	“0E00”H			“0E01”H			“0E02”H			“0E03”H			…	“0EAC”H			“0EAD”H			“0EAE”H			“0EAF”H		
G16	G205	“0F00”H			“0F01”H			“0F02”H			“0F03”H			…	“0FAC”H			“0FAD”H			“0FAE”H			“0FAF”H		
G17	G204	“1000”H			“1001”H			“1002”H			“1003”H			…	“10AC”H			“10AD”H			“10AE”H			“10AF”H		
G18	G203	“1100”H			“1101”H			“1102”H			“1103”H			…	“11AC”H			“11AD”H			“11AE”H			“11AF”H		
G19	G202	“1200”H			“1201”H			“1202”H			“1203”H			…	“12AC”H			“12AD”H			“12AE”H			“12AF”H		
G20	G201	“1300”H			“1301”H			“1302”H			“1303”H			…	“13AC”H			“13AD”H			“13AE”H			“13AF”H		
:	:	:			:			:			:			…	:			:			:			:		
:	:	:			:			:			:			…	:			:			:			:		
G213	G8	“D400”H			“D401”H			“D402”H			“D403”H			…	“D4AC”H			“D4AD”H			“D4AE”H			“D4AF”H		
G214	G7	“D500”H			“D501”H			“D502”H			“D503”H			…	“D5AC”H			“D5AD”H			“D5AE”H			“D5AF”H		
G215	G6	“D600”H			“D601”H			“D602”H			“D603”H			…	“D6AC”H			“D6AD”H			“D6AE”H			“D6AF”H		
G216	G5	“D700”H			“D701”H			“D702”H			“D703”H			…	“D7AC”H			“D7AD”H			“D7AE”H			“D7AF”H		
G217	G4	“D800”H			“D801”H			“D802”H			“D803”H			…	“D8AC”H			“D8AD”H			“D8AE”H			“D8AF”H		
G218	G3	“D900”H			“D901”H			“D902”H			“D903”H			…	“D9AC”H			“D9AD”H			“D9AE”H			“D9AF”H		
G219	G2	“DA00”H			“DA01”H			“DA02”H			“DA03”H			…	“DAAC”H			“DAAD”H			“DAAE”H			“DAAF”H		
G220	G1	“DB00”H			“DB01”H			“DB02”H			“DB03”H			…	“DBAC”H			“DBAD”H			“DBAE”H			“DBAF”H		

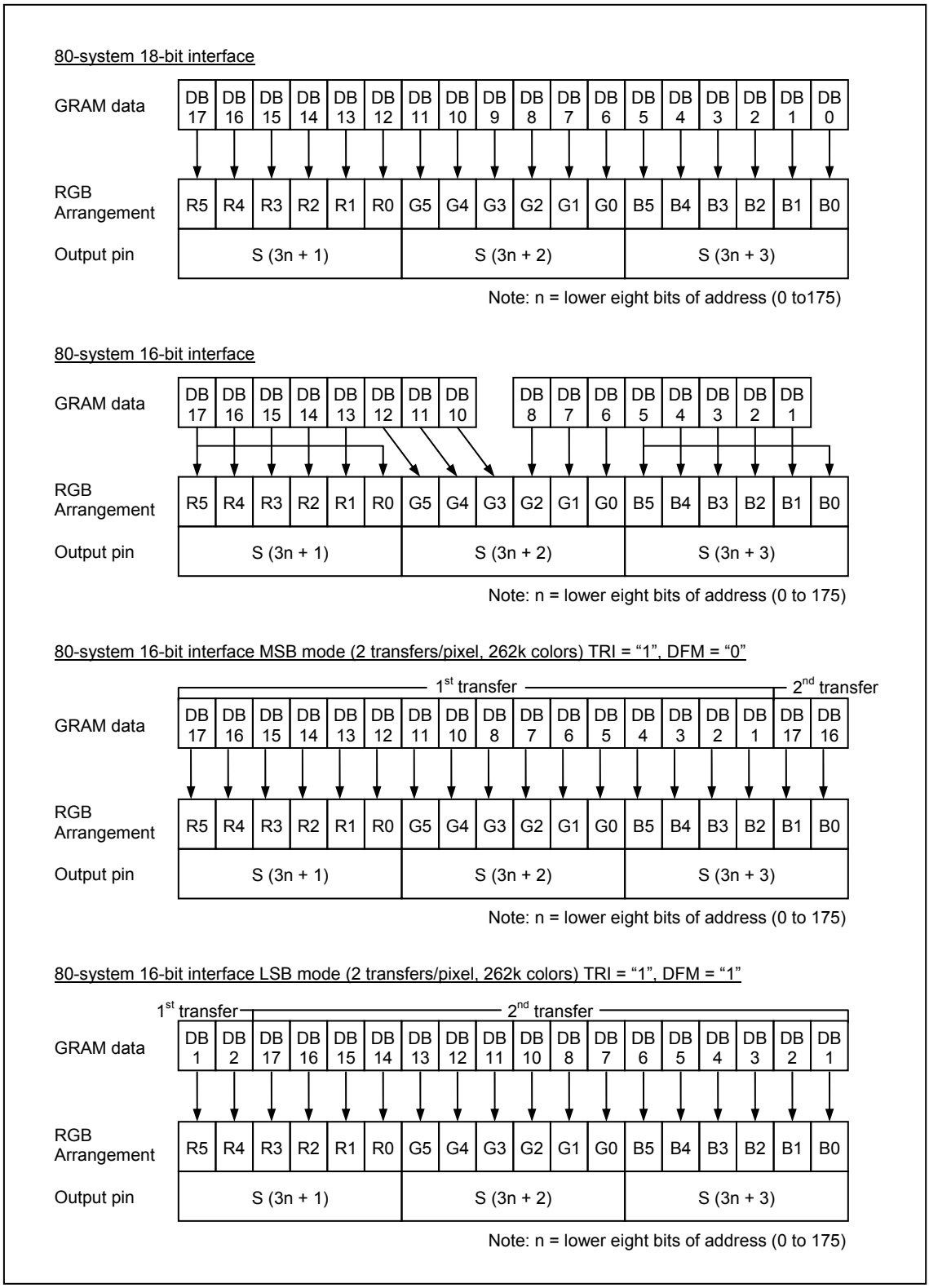


Figure 2 GRAM data and display data: system interface (SS = "0", BGR = "0")

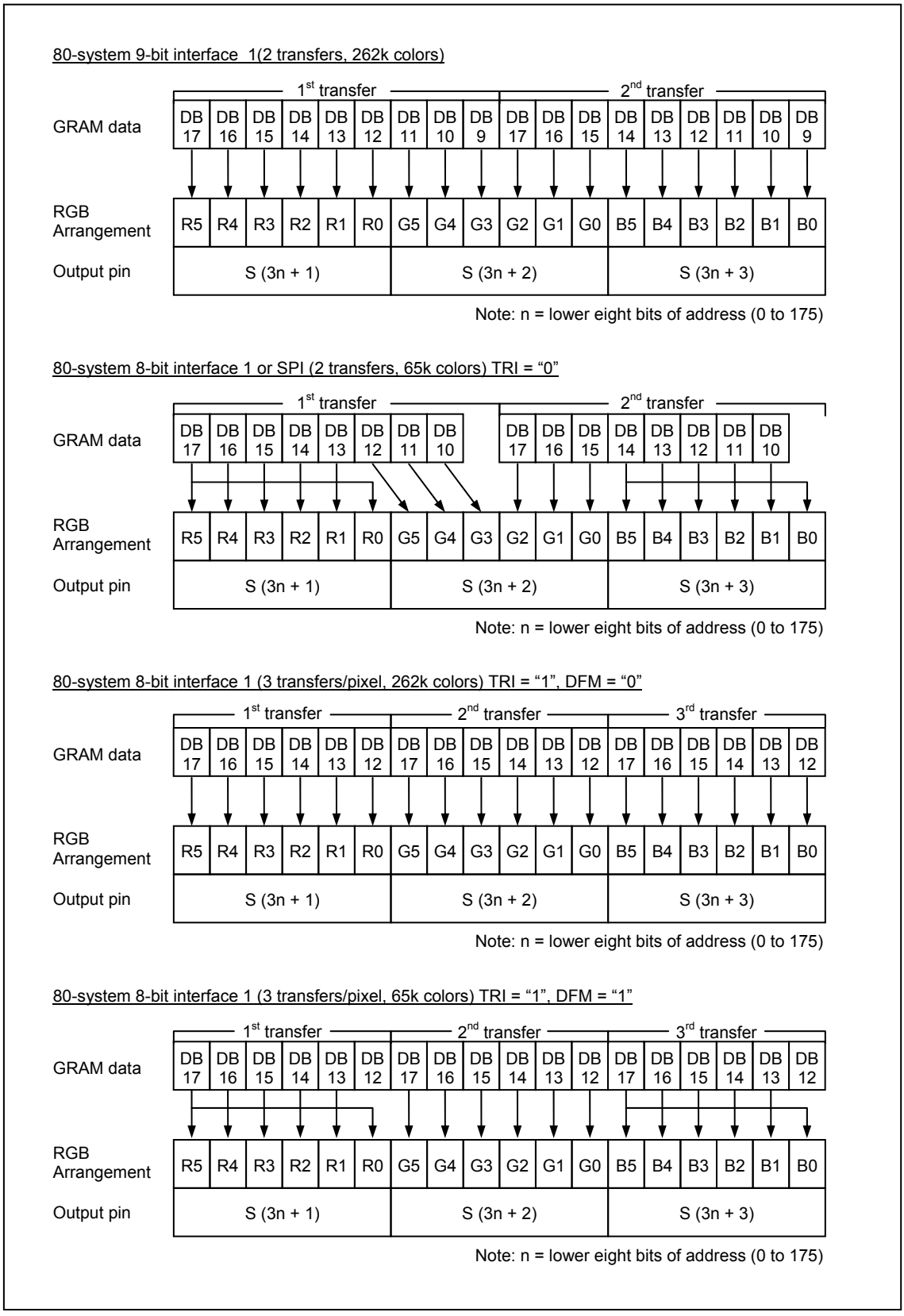
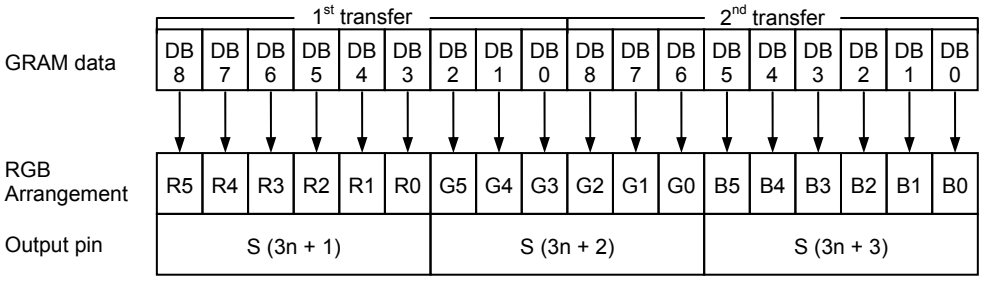


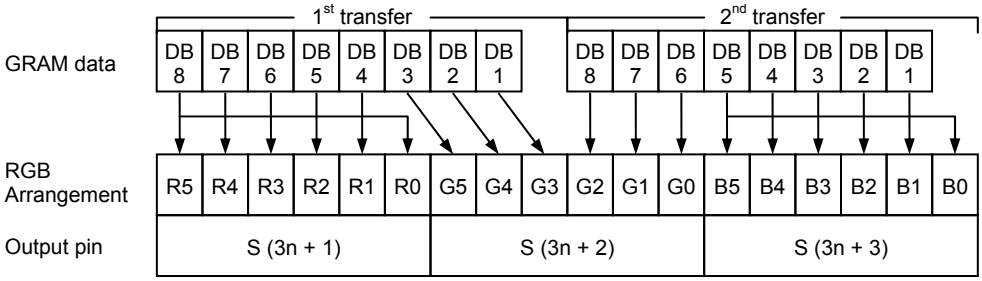
Figure 3 GRAM data and display data: system interface (SS = "0", BGR = "0")

80-system 9-bit interface 2(2 transfers, 262k colors)



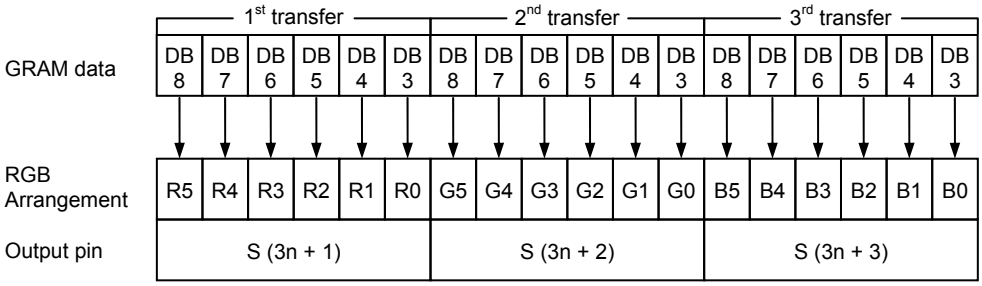
Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface 2 (2 transfers, 65k colors) TRI = "0"



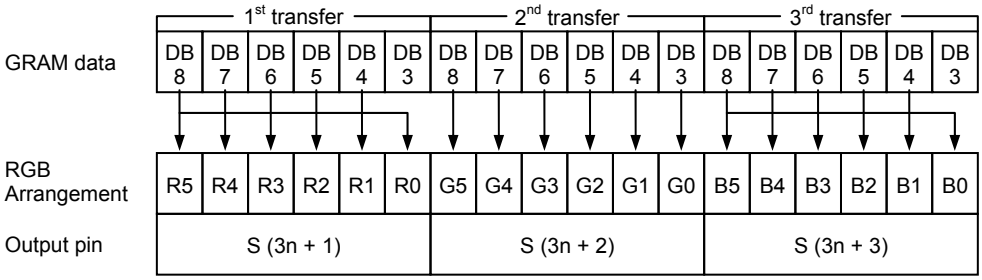
Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface 2 (3 transfers/pixel, 262k colors) TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface 2 (3 transfers/pixel, 65k colors) TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

Figure 4 GRAM data and display data: system interface (SS = "0", BGR = "0")

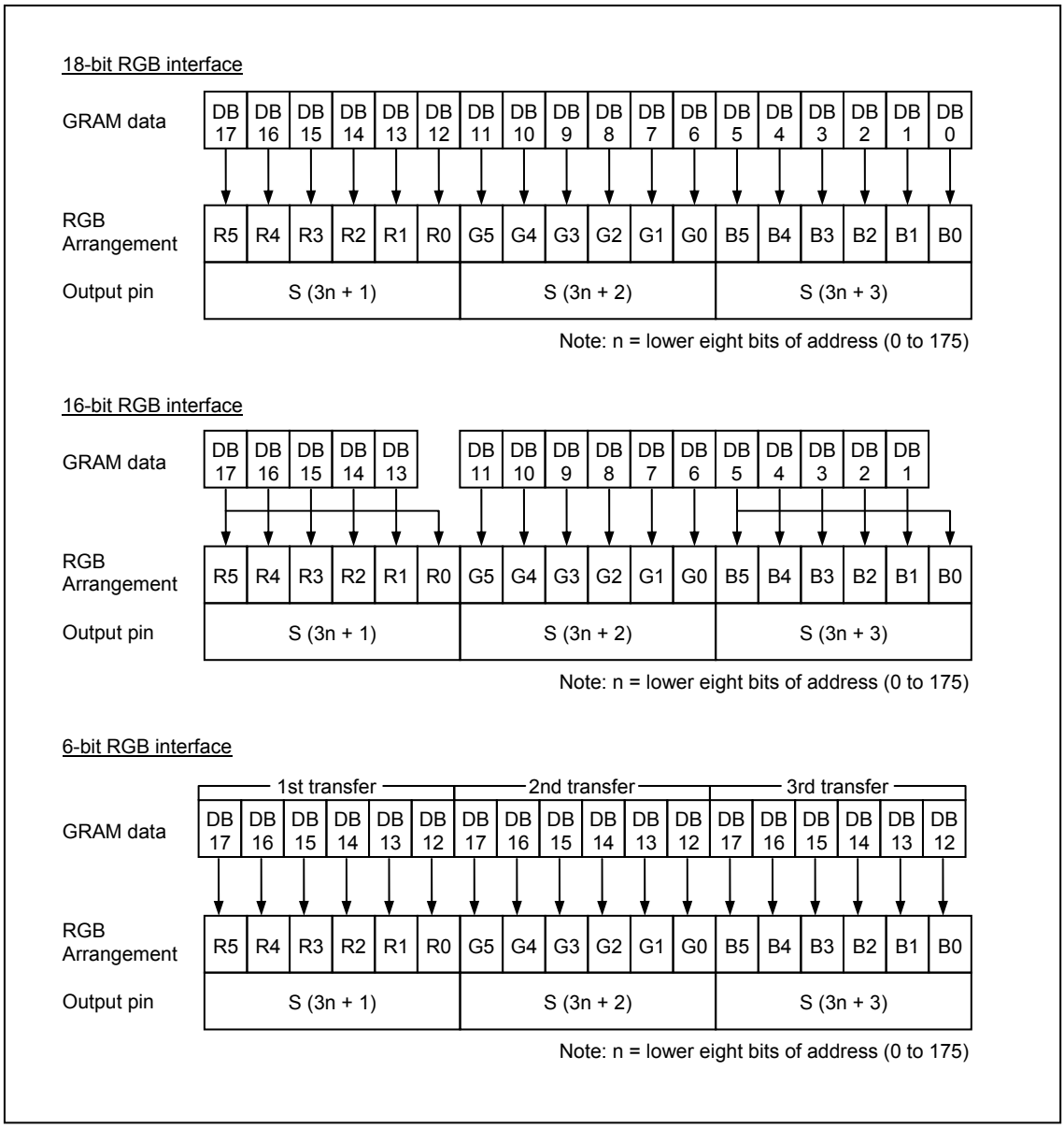


Figure 5 GRAM data and display data: system interface (SS = "0", BGR = "0")

Table 9 GRAM address and display panel position (SS = "1", BGR = "1")

S/G pin		S528	S527	S526	S525	S524	S523	S522	S521	S520	S519	S518	S517	…	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G220	"0000"H			"0001"H			"0002"H			"0003"H			…	"00AC"H			"00AD"H			"00AE"H			"00AF"H		
G2	G219	"0100"H			"0101"H			"0102"H			"0103"H			…	"01AC"H			"01AD"H			"01AE"H			"01AF"H		
G3	G218	"0200"H			"0201"H			"0202"H			"0203"H			…	"02AC"H			"02AD"H			"02AE"H			"02AF"H		
G4	G217	"0300"H			"0301"H			"0302"H			"0303"H			…	"03AC"H			"03AD"H			"03AE"H			"03AF"H		
G5	G216	"0400"H			"0401"H			"0402"H			"0403"H			…	"04AC"H			"04AD"H			"04AE"H			"04AF"H		
G6	G215	"0500"H			"0501"H			"0502"H			"0503"H			…	"05AC"H			"05AD"H			"05AE"H			"05AF"H		
G7	G214	"0600"H			"0601"H			"0602"H			"0603"H			…	"06AC"H			"06AD"H			"06AE"H			"06AF"H		
G8	G213	"0700"H			"0701"H			"0702"H			"0703"H			…	"07AC"H			"07AD"H			"07AE"H			"07AF"H		
G9	G212	"0800"H			"0801"H			"0802"H			"0803"H			…	"08AC"H			"08AD"H			"08AE"H			"08AF"H		
G10	G211	"0900"H			"0901"H			"0902"H			"0903"H			…	"09AC"H			"09AD"H			"09AE"H			"09AF"H		
G11	G210	"0A00"H			"0A01"H			"0A02"H			"0A03"H			…	"0AAC"H			"0AAD"H			"0AAE"H			"0AAF"H		
G12	G209	"0B00"H			"0B01"H			"0B02"H			"0B03"H			…	"0BAC"H			"0BAD"H			"0BAE"H			"0BAF"H		
G13	G208	"0C00"H			"0C01"H			"0C02"H			"0C03"H			…	"0CAC"H			"0CAD"H			"0CAE"H			"0CAF"H		
G14	G207	"0D00"H			"0D01"H			"0D02"H			"0D03"H			…	"0DAC"H			"0DAD"H			"0DAE"H			"0DAF"H		
G15	G206	"0E00"H			"0E01"H			"0E02"H			"0E03"H			…	"0EAC"H			"0EAD"H			"0EAE"H			"0EAF"H		
G16	G205	"0F00"H			"0F01"H			"0F02"H			"0F03"H			…	"0FAC"H			"0FAD"H			"0FAE"H			"0FAF"H		
G17	G204	"1000"H			"1001"H			"1002"H			"1003"H			…	"10AC"H			"10AD"H			"10AE"H			"10AF"H		
G18	G203	"1100"H			"1101"H			"1102"H			"1103"H			…	"11AC"H			"11AD"H			"11AE"H			"11AF"H		
G19	G202	"1200"H			"1201"H			"1202"H			"1203"H			…	"12AC"H			"12AD"H			"12AE"H			"12AF"H		
G20	G201	"1300"H			"1301"H			"1302"H			"1303"H			…	"13AC"H			"13AD"H			"13AE"H			"13AF"H		
:	:	:			:			:			:			…	:			:			:			:		
:	:	:			:			:			:			…	:			:			:			:		
G213	G8	"D400"H			"D401"H			"D402"H			"D403"H			…	"D4AC"H			"D4AD"H			"D4AE"H			"D4AF"H		
G214	G7	"D500"H			"D501"H			"D502"H			"D503"H			…	"D5AC"H			"D5AD"H			"D5AE"H			"D5AF"H		
G215	G6	"D600"H			"D601"H			"D602"H			"D603"H			…	"D6AC"H			"D6AD"H			"D6AE"H			"D6AF"H		
G216	G5	"D700"H			"D701"H			"D702"H			"D703"H			…	"D7AC"H			"D7AD"H			"D7AE"H			"D7AF"H		
G217	G4	"D800"H			"D801"H			"D802"H			"D803"H			…	"D8AC"H			"D8AD"H			"D8AE"H			"D8AF"H		
G218	G3	"D900"H			"D901"H			"D902"H			"D903"H			…	"D9AC"H			"D9AD"H			"D9AE"H			"D9AF"H		
G219	G2	"DA00"H			"DA01"H			"DA02"H			"DA03"H			…	"DAAC"H			"DAAD"H			"DAAE"H			"DAAF"H		
G220	G1	"DB00"H			"DB01"H			"DB02"H			"DB03"H			…	"DBAC"H			"DBAD"H			"DBAE"H			"DBAF"H		

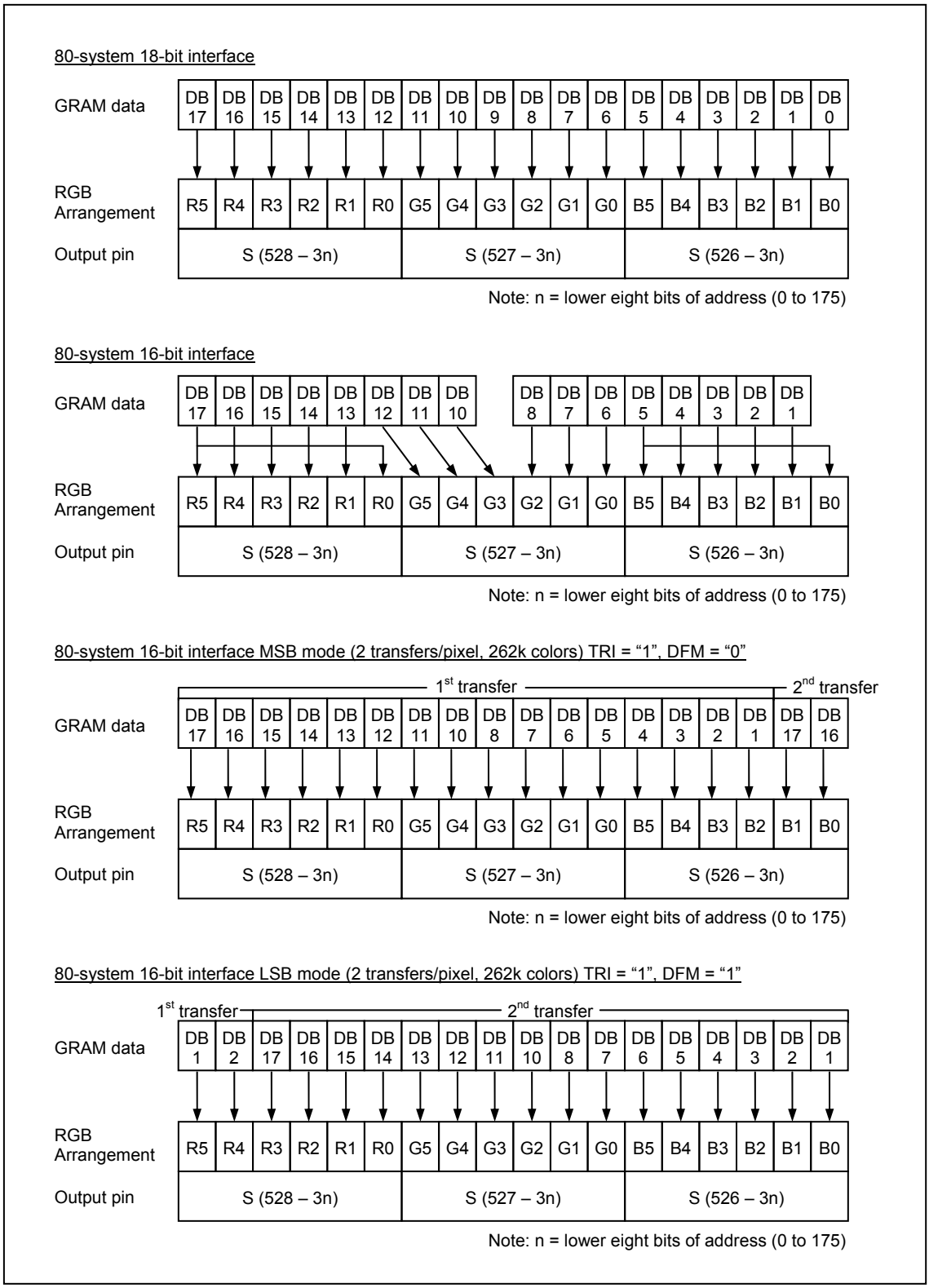
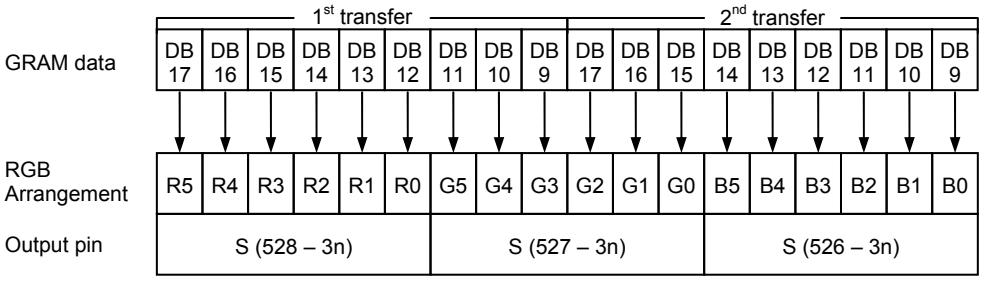


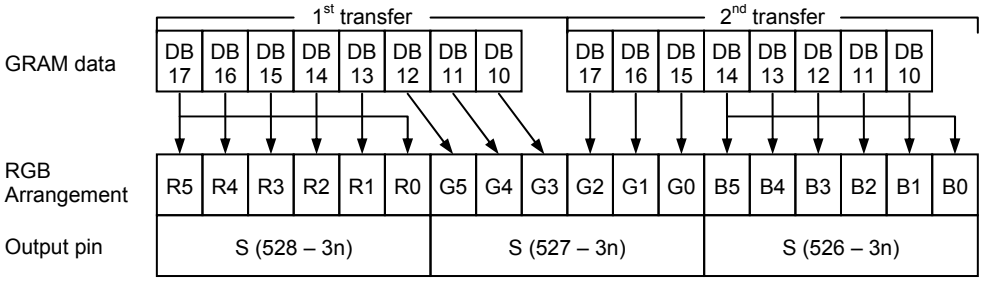
Figure 6 GRAM data and display data: system interface (SS = "1", BGR = "1")

80-system 9-bit interface 1(2 transfers, 262k colors)



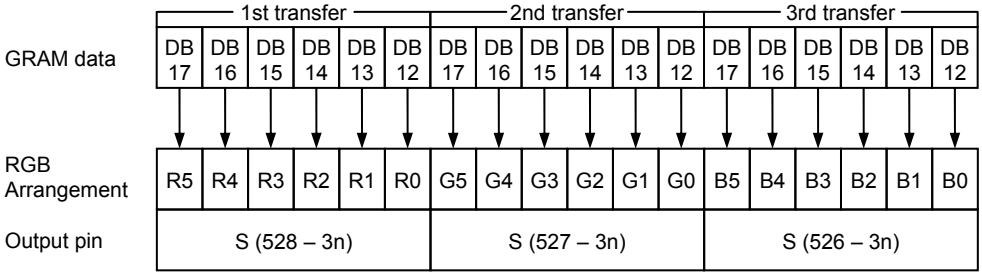
Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface 1 or SPI (2 transfers, 65k colors) TRI =



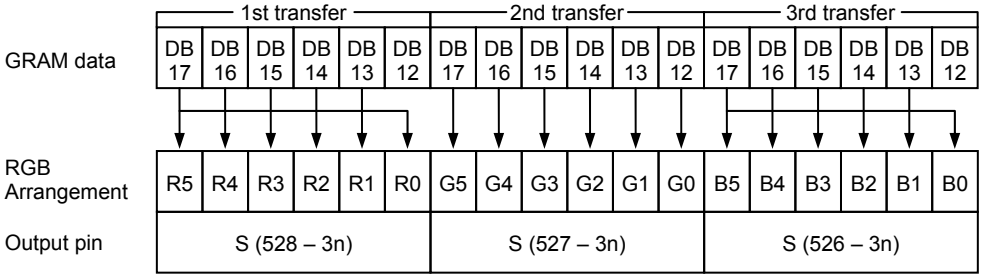
Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface 1 (3 transfers/pixel, 262k colors) TRI = “1”, DFM = “0”



Note: n = lower eight bits of address (0 to 175)

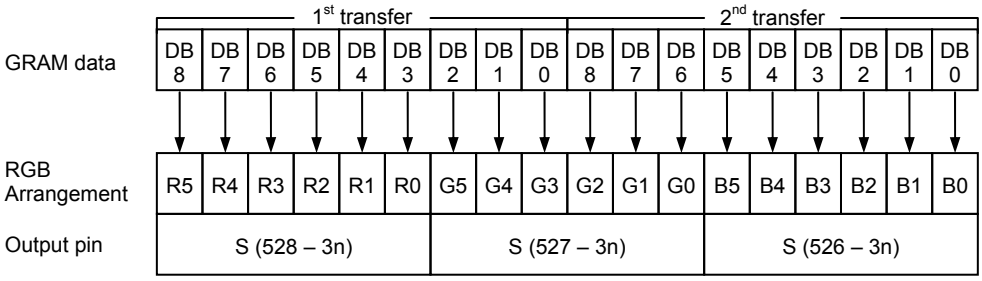
80-system 8-bit interface 1 (3 transfers/pixel, 65k colors) TRI = “1”, DFM = “1”



Note: n = lower eight bits of address (0 to 175)

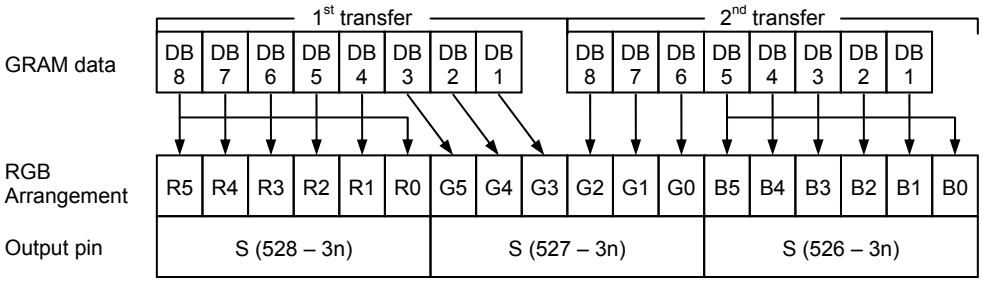
Figure 7 GRAM data and display data: system interface (SS = “1”, BGR = “1”)

80-system 9-bit interface 2(2 transfers, 262k colors)



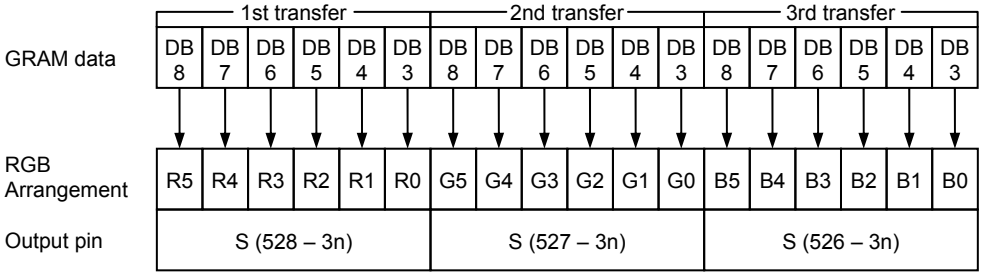
Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface 2 (2 transfers, 65k colors) TRI = "0"



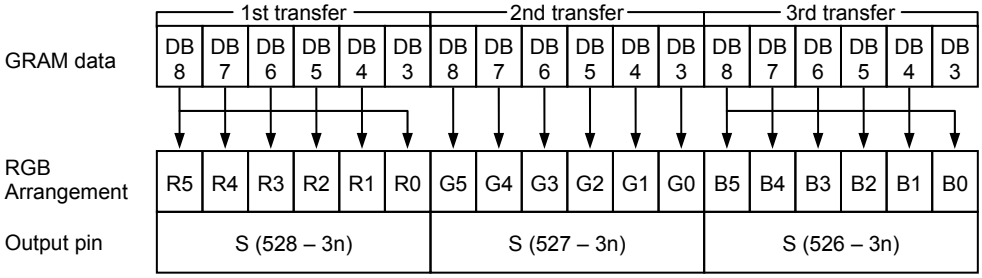
Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface 2 (3 transfers/pixel, 262k colors) TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface 2 (3 transfers/pixel, 65k colors) TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

Figure 8 GRAM data and display data: system interface (SS = "1", BGR = "1")

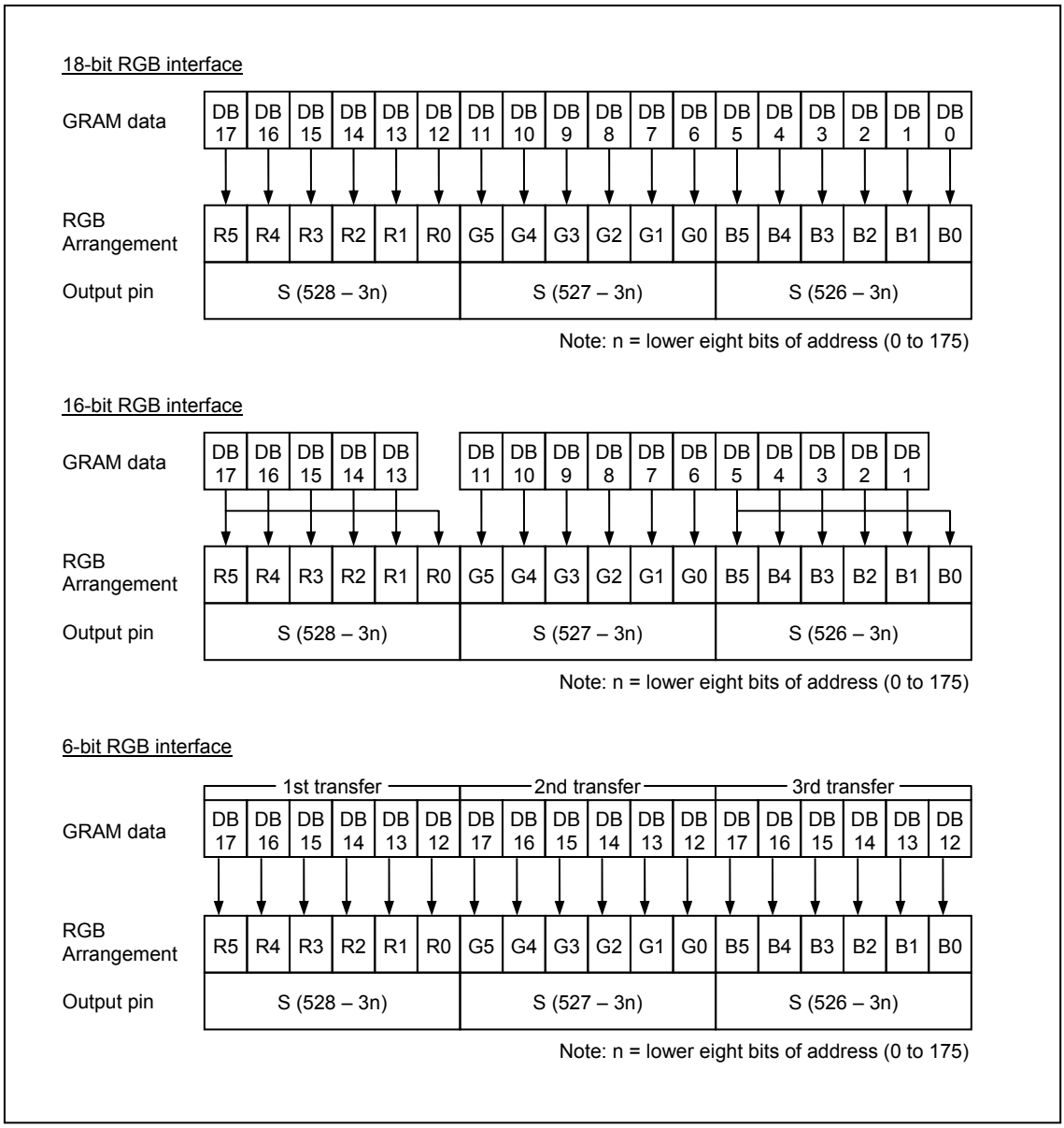


Figure 9 GRAM data and display data: system interface (SS = "1", BGR = "1")

Instructions

Outline

The LG4525B adopts 18-bit bus architecture to interface to a high-performance microcomputer. The LG4525B starts internal processing after storing control information of externally sent 18-, 16-, 9-, 8-bit data in the instruction register (IR) and the data register (DR). Since internal operations of the LG4525B are controlled by the signals sent from the microcomputer, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 to IB0) are called instructions. The LG4525B use the 18-bit format internally for operations involving internal GRAM access. The instructions of the LG4525B are categorized into the following groups.

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

Normally, the instruction for writing data to the internal GRAM is used the most often. Since the LG4525B can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there is less load on the program in the microcomputer. Since instructions are executed in 0 cycles, it is possible to write instructions consecutively.

Instruction Data Format

Note that as the following figure shows, the assignment of 16 instruction bits(IB15-0) to the data bus differs in different interface operations. Write instruction according to the data transfer format of the interface in use.

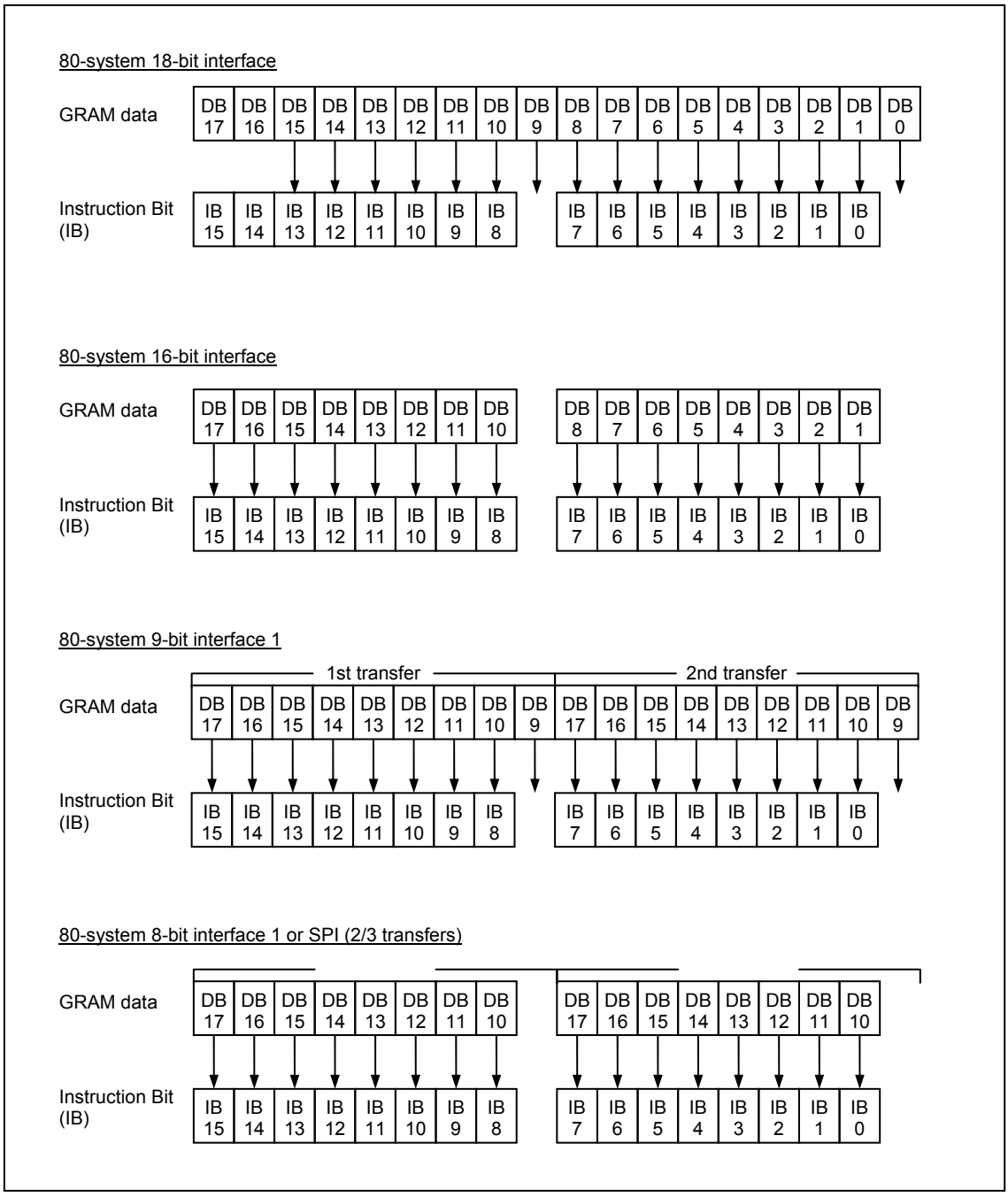


Figure 10 Instruction bits

Instruction Description

The following are detailed explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h – R7Fh) of a control register or RAM control to be accessed using binary numbers “000_0000” to “111_1111”. An access to the register as well as instruction bits contained in it is disabled unless its index is represented in this register.

Status Read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L[7:0]								0	0	0	0	0	0	0	0

The SR bits represent an internal status of the LG4525B.
L[7:0] – Indicates the positon of the line that is currently driving liquid crystal.

Device code read (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	0	1	0	0	1	0	1	1	0	1	1

The device code “025B”H is read out when reading out this register forcibly.

Driver output control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL[4:0]				

NL[4:0] – Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set with NL[4:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 10

NL[4:0]	Number of Lines	NL[4:0]	Number of Lines
5’h00	8	5’h0F	128
5’h01	16	5’h10	136
5’h02	24	5’h11	144
5’h03	32	5’h12	152
5’h04	40	5’h13	160
5’h05	48	5’h14	168
5’h06	56	5’h15	176
5’h07	64	5’h16	184

5'h08	72	5'h17	192
5'h09	80	5'h18	200
5'h0A	88	5'h19	208
5'h0B	96	5'h1A	216
5'h0C	104	5'h1B	220
5'h0D	112	5'h1C-5'h1F	Setting disabled
5'h0E	120		

SS – Selects the shift direction of outputs from the source pins.

If SS = "0", the source pins output from S1 to S528.
If SS = "1", the source pins output from S528 to S1.

The combination of SS and BGR bits controls the order of assigning RGB dots to the source driver pins S1 to S528.

If SS = "0" and BGR = "0", RGB dots are assigned interchangeably from S1 to S528.
If SS = "1" and BGR = "1", RGB dots are assigned interchangeably from S528 to S1.

When changing SS or BGR bits, RAM data must be rewritten.

GS – Set the direction of scan by the gate driver. Set the GS bit in combination with SM and SS bits to optimize scan method to the LCD module.

SM – Sets gate driver assignment in combination with the GS bit according to the LC module. See "Scan mode setting".

DPL – Sets the signal polarity of DOTCLK pin.

DPL = 0 : input data on the rising edge of DOTCLK
DPL = 1 : input data on the falling edge of DOTCLK

EPL – Sets the signal polarity of ENABLE pin.

EPL = 0 : writes data DB[17:0] when ENABLE = 0 and disables data write operation when ENABLE = 1.
EPL = 1 : writes data DB[17:0] when ENABLE = 1 and disables data write operation when ENABLE = 0.

HSPL – Sets the signal polarity of HSYNC pin.
HSPL = 0 : Low active
HSPL = 1 : High active

VSPL – Sets the signal polarity of VSYNC pin.
VSPL = 0 : Low active
VSPL = 1 : High active

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD[1:0]		BC0	EOR	0	0	NW[5:0]					

NW[5:0] – Specify n, the number of raster-rows from 1 to 64, where alternations occurs every n+1 raster-rows when C-pattern waveform is generated(BC0=1).

EOR – When EOR=1, alternation occurred by applying EOR(Exclusive OR) operation to an odd/even frame selecting signal and n-raster-row inversion signal while a C-pattern waveform is generated(BC0=1). This instruction is used when liquid crystal alternation drive is not available due to combination of numbers of LCD raster-rows and the value of "x n". For details, see n-raster-row Inversion Alternating Drive.

BC0 – Selects the liquid crystal drive waveform VCOM. See "Line Inversion AC Drive" for details.
BC0 = 0: frame inversion waveform is selected.
BC0 = 1: Line inversion waveform is selected.
In either liquid crystal drive method, the polarity inversion is halted in blank periods (back and front porch periods).

FLD[1:0] – Set the number of fields for n-field interlaced scan. See "Interlaced Scan" for details. The FLD bits are disabled in external display interface mode. When using the external display interface, set FLD[1:0] = "01"

Table 11

FLD[1:0]	Number of fields
2'h00	Setting disabled
2'h01	1 field (= 1 frame)
2'h02	Setting disabled
2'h03	3 fields

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D[1:0]		AM	0	EPF[1:0]	

The LG4525B modifies data sent from a microcomputer before writing them to the internal GRAM in order to write the GRAM data in high speed and reduce software processing load on the microcomputer. See "Graphics Operation Function" for details.

EPF[1:0] – Set the data format when 16bpp(R,G and B) to 18bpp(r, g and b) is stored in internal RAM. EPF settings are effective when :

1. 80-system 16-bit interface, TRI = 0
2. 80-system 8-bit interface, TRI = 0
3. Clock synchronous serial interface

Table 12

EPF	Expand 16bpp(R,G,B) to 18bpp(r,g,b)
2'h0	Same value as MSB is inputted to LSB of R and B r[5:0] = {R[4:0], R[4]} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], B[4]}
2'h1	"0" is inputted to LSB of r and b r[5:0] = {R[4:0], 1'b0} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 1'b0} Except. R[4:0], B[4:0] = 5'h1F -> r,b[5:0] = 6'h3F G[5:0] = 6'h3F -> g[5:0] = 6'h3F

2'h2	"1" is inputted to LSB of r and b r[5:0] = {R[4:0], 1'b1} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 1'b1} Except. R[4:0], B[4:0] = 5'h00 -> r,b[5:0] = 6'h00 G[5:0] = 6'h00 -> g[5:0] = 6'h00
2'h3	Setting disabled

TRI – Selects the RAM data transfer mode in 80-system 8-bit/16-bit bus interface operation.
In 8-bit interface operation,
TRI = 0: 16-bit RAM data is transferred in two transfers.
TRI = 1: 18-bit RAM data is transferred in three transfers.
In 16-bit bus interface operation,
TRI = 0: 16-bit RAM data is transferred in one transfer.
TRI = 1: 18-bit RAM data is transferred in two transfers.
Make sure TRI = 0 when not using either 16-bit or 8-bit interface. Also, set TRI = 0 during read operation.

DFM – Sets the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.

Table 13

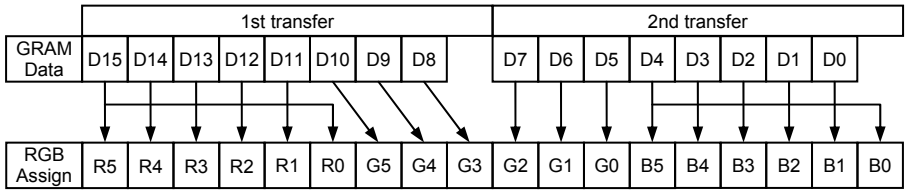
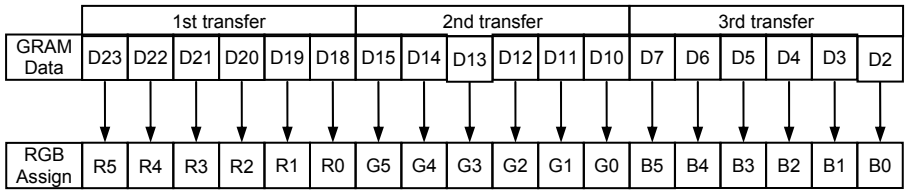
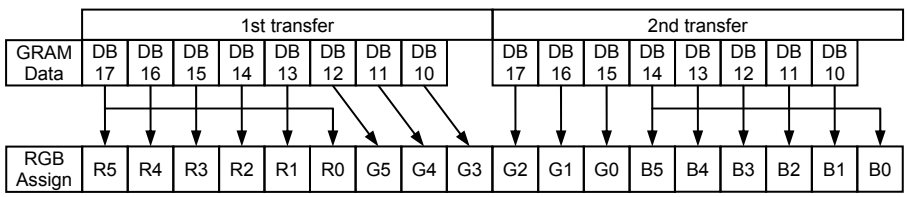
TRI	DFM	RAM write data transfer via serial peripheral interface (SPI)
0	*	SPI (2 transfers/pixel) – 65k colors available 
1	0	SPI (3 transfers/pixel) – 262k colors available 
1	1	Setting disabled

Table 14

TRI	DFM	RAM write data transfer via 8-bit interface 1
0	*	80-system 8-bit interface (2 transfers/pixel) – 65k colors 

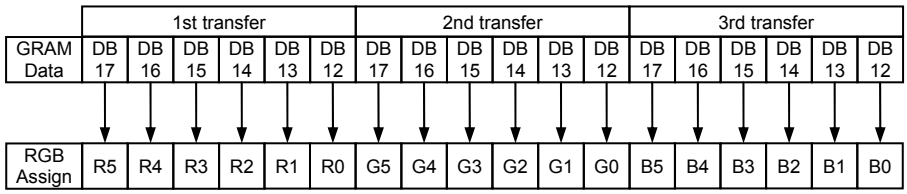
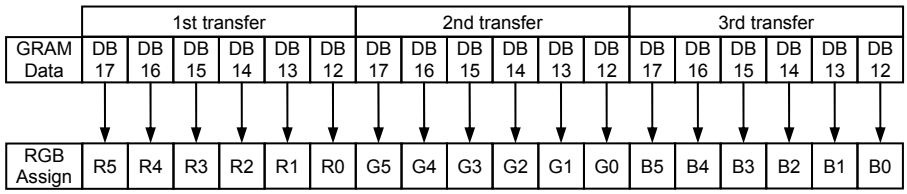
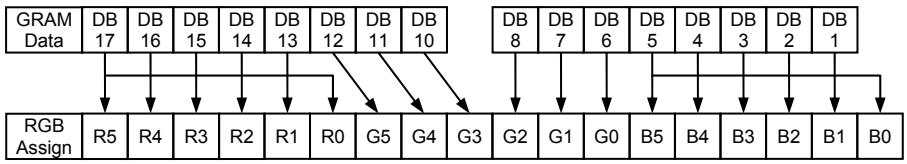
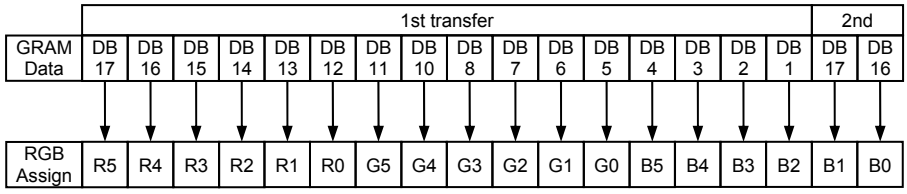
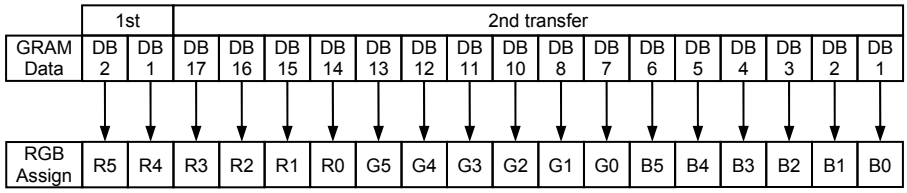
1	0	80-system 8-bit interface (3 transfers/pixel) – 262k colors 
1	1	80-system 8-bit interface (3 transfers/pixel) – 65k colors 

Table 15

TRI	DFM	RAM write data transfer via 16-bit interface
0	*	80-system 16-bit interface (1 transfers/pixel) – 65k colors 
1	0	80-system 16-bit interface MSB mode(2 transfers/pixel) – 262k colors available 
1	1	80-system 16-bit interface LSB mode(2 transfers/pixel) – 262k colors available 

BGR – Reverses the order of RGB dots to BGR when writing 18-bit pixel data to the internal GRAM.
BGR = 0 : Write source data in order of R-G-B.
BGR = 1 : Change the order with B-G-R.

I/D[1:0] – The address counter is automatically incremented by 1 as writing data to the internal GRAM when I/D[1:0] = "1". The address counter is automatically decremented by 1 as writing data to the internal GRAM when I/D[1:0] = "0". The increment/decrement can be set separately to each upper (AD[15:8]) / lower (AD[7:0]) byte of address. The transition direction of address (vertical/horizontal) when writing data to the internal GRAM is set with the AM bit.

AM – Sets the direction of automatically updating address for writing data to the internal RAM in the address counter (AC). When AM = "0", the address is updated in horizontal writing direction. When AM = "1", the address is updated in vertical writing direction. When a window address area is set, data are written only to the GRAM area specified with window address in the writing direction set with I/D[1:0] and AM bits.

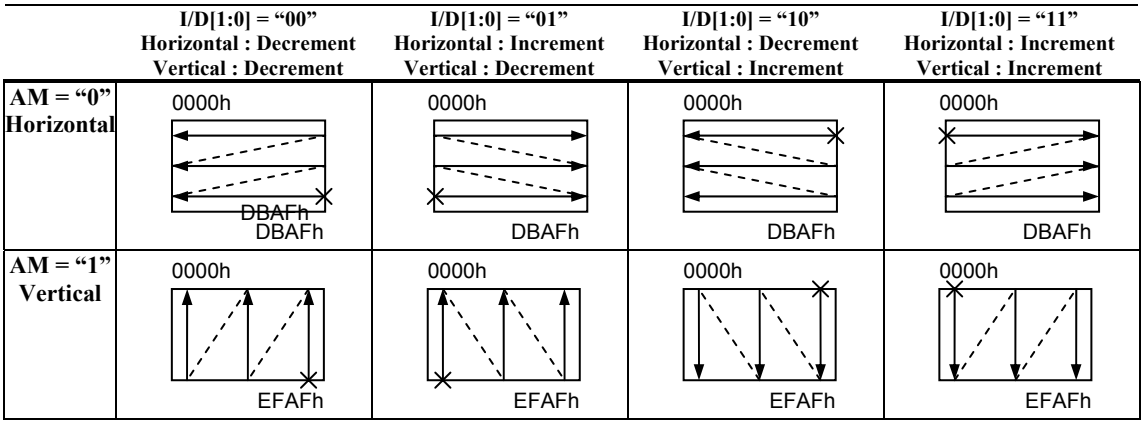


Figure 11 Automatic address update (AM, I/D)

Resizing Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV[1:0]		0	0	RCH[1:0]		0	0	RSZ[1:0]	

RSZ[1:0] – Sets the resizing factor. When the RSZ bits are set for resizing, the LG4525B writes the data of the resized image in both horizontal and vertical directions according to the resizing factor on the internal GRAM. See "Resizing function".

RCH[1:0] – Sets the number of pixels made as the remainder in horizontal direction as a result of resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ=2'h0) or there are no remainder pixels.

RCV[1:0] – Sets the number of pixels made as the remainder in vertical direction as a result of resizing a picture. By specifying the number of remainder pixels with RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ=2'h0) or there are no remainder pixels.

Table 16

RSZ[1:0]	Resizing scale
2'h0	No resizing (x1)
2'h1	x 1/2
2'h2	Setting disabled
2'h3	x 1/4

Table 17

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Table 18

RCV[1:0]	Number of remainder Pixels in Vertical Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTS[2:0]			VLE[1:0]		SPT	0	0	GON	DTE	COL	REV	D[1:0]	

D[1:0] – A graphics display appears on the screen when D[1] = "1", and is turned off upon setting D[1] = "0". When setting D[1] = "0", the graphics display data are retained in the internal GRAM and the display appears instantly on the screen upon setting D[1] to "1". When the D[1] bit is "0", i.e. while no display is shown on the screen, all source outputs are at the GND level to reduce charging/discharging current on liquid crystal cells, which is generated during liquid crystal AC drive.

When the display is turned off by setting D[1:0] = 2'h1, the LG4525B continues internal display operation. When the display is turned off by setting D[1:0] = 2'h0, the LG4525B's internal display operation is halted completely. In combination with GON bit, the D[1:0] bits control ON/OFF of graphics display. For details, see "Instruction setting".

Table 19

D[1:0]	Source Output (S1-720)	FLM signal	Internal Operation
2'h0	GND	Halt	Halt
2'h1	GND	Operation	Operation
2'h2	Non-display	Operation	Operation
2'h3	Base-image display	Operation	Operation

Notes: 1. The data write operation from the microcomputer is not affected by the setting in the D[1:0] bits.
2. The PTS bits set the source output level for "non-lit display"

REV – The grayscale level corresponding to the GRAM data can be reversed by setting REV = 1. This enables the LG4525B to display the same image form a same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

Table 20

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000 : 18'h3FFFF	V63 : V0	V0 : V63
1	18'h00000 : 18'h3FFFF	V0 : V63	V63 : V0

COL – When COL = "1", the 8-color display mode is selected. For details, see the "8-color Display Mode" section. The 8-color display mode is not available in external interface mode.

Table 21

COL	Operating amplifier	Display color
1'h0	64	262,144
1'h1	2	8

Note: When COL=1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

GON, DTE – The combination of settings in GON and DTE bits sets the output level form gate lines(G1-G320). When GON=0, the VCOM output level becomes the GND level.

Table 22

GON	DTE	G1-G320
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

SPT – When SPT = "1", the LCD is driven in 2 split screens. For details, see the "Partial Display Function" section

VLE[1:0] – When VLE[0] = "1", the first display is scrolled up in vertical direction. When VLE[1] = "1", the second display is scrolled up in vertical direction. The first and second displays cannot be scrolled simultaneously. This function is not available with the external display interface. In this case, set VLE to "00".

Table 23

VLE[1:0]	2nd display image	1st display image
2'h0	Fixed	Fixed
2'h1	Fixed	Scroll up
2'h2	Scroll up	Fixed
2'h3	Setting disabled	

PTS[2:0] – Set the source output in non-display drive period.

Table 24

PTS[2:0]	Source output level		Grayscale amplifier In operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3h0	V63	V0	V0 to V63	Register setting(DC0,DC1)
3h1	Setting disabled	Setting disabled	-	-
3h2	GND	GND	V0 to V63	Register setting(DC0,DC1)
3h3	Hi-Z	Hi-Z	V0 to V63	Register setting(DC0,DC1)
3'h4	V63	V0	V0 and V63	Register setting(DC0,DC1)
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0 and V63	Register setting(DC0,DC1)
3'h7	Hi-Z	Hi-Z	V0 and V63	Register setting(DC0,DC1)

Notes: 1.The gate output level in non-display drive period is controlled by the PTG setting(off-scan mode).

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	FP[7:0]								BP[7:0]							

FP[7:0]/BP[7:0] – Sets the blank period made at the beginning and the end of a display (front porch and back porch, respectively). The FP[7:0] and BP[7:0] bits specify the number of lines for the front and back porch periods, respectively. In setting, be sure:

FP ≥ 2 lines
BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal.

Table 25

FP[7:0]/BP[7:0]	Number of lines for the front/back porches
8'h00	Setting disabled
8'h01	Setting disabled
8'h02	2 lines
8'h03	3 lines
8'h04	4 lines
8'h05	5 lines
8'h06	6 lines
8'h07	7 lines
8'h08	8 lines
:	:
8'hED	253 lines
8'hFE	254 lines
8'hFF	255 lines

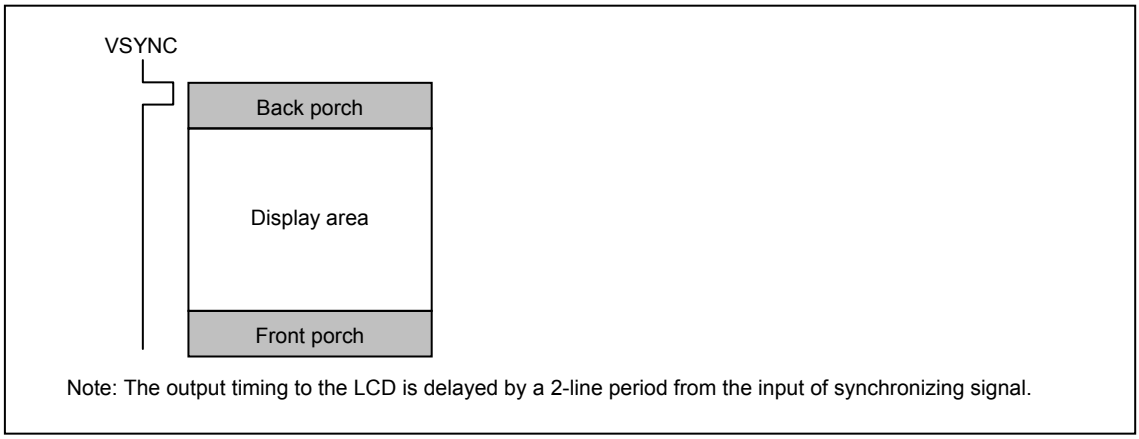


Figure 12 Back/front porches

Set the BP[7:0], FP[7:0] bits as follows in each operation mode.

Table 26

Internal clock operation	BP ≥ 2 lines	FP ≥ 2 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	PTG[1:0]		ISC[3:0]			

ISC[3:0] – Set the interval of scan when PTG[1:0] sets the interval scan. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal is inverted in the same cycle as the interval scan.

Table 27

ISC[3:0]	Scan cycle	Time for interval when(fFLM)=60Hz
4'h0	Setting disabled	-
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTG[1:0] – Set the scan mode in non-display area, which is made between partial display periods of the first and the second images, or turning off both base and partial images(full-screen non display). The setting is commonly applied to all non-display drive period.

Table 28

PTG[1:0]	Gate drive operation In non-display area	Source output level In non-display area	VCOM output
2'h0	Normal scan	PTS[2:0] setting	VCOMH/VCOML amplitude
2'h1	Setting disabled	-	-
2'h2	Interval scan	PTS[2:0] setting	VCOMH/VCOML amplitude
2'h3	Setting disabled	-	-

Note: Select frame-inversion AC drive when setting interval scan.

Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
MCP	1	EQ[3:0]				SEQ[3:0]				SDT[3:0]				MCP[3:0]			

MCP[3:0] – Set the vcom output delay from the falling edge of gate output .

Table 29

MCP[3:0]	Vcom output delay	
	Internal operation (internal oscillator)	RGB I/F operation (DOTCLK)
4'h0	0 clock	0 clocks
4'h1	2 clocks	8 clocks
4'h2	4 clocks	16 clocks
4'h3	6 clocks	24 clocks
:	:	:
4'hC	24 clocks	96 clocks
4'hD	26 clocks	104 clocks
4'hE	28 clocks	112 clocks
4'hF	30 clocks	120 clocks

SDT[3:0] – Set the source output delay from the falling edge of gate output .

Table 30

SDT[3:0]	Source output delay	
	Internal operation (internal oscillator)	RGB I/F operation (DOTCLK)
4'h0	0 clock	0 clocks
4'h1	2 clocks	8 clocks
4'h2	4 clocks	16 clocks
4'h3	6 clocks	24 clocks
:	:	:
4'hC	24 clocks	96 clocks
4'hD	26 clocks	104 clocks
4'hE	28 clocks	112 clocks
4'hF	30 clocks	120 clocks

SEQ[3:0] – Sets Source equalization period.

Table 31

SEQ[3:0]	Source equalization period	
	Internal operation (internal oscillator)	**RGB I/F operation (DOTCLK)**
4'h0	0 clock	0 clocks
4'h1	1 clock	4 clocks
4'h2	2 clocks	8 clocks
4'h3	3 clocks	12 clocks
:	:	:
4'hC	12 clocks	48 clocks
4'hD	13 clocks	52 clocks
4'hE	14 clocks	56 clocks
4'hF	15 clocks	60 clocks

EQ[3:0] – Set the vcom equalization period.

Table 32

EQ[3:0]	Vcom equalization period	
	Internal operation (internal oscillator)	**RGB I/F operation (DOTCLK)**
4'h0	0 clock	0 clocks
4'h1	1 clock	4 clocks
4'h2	2 clocks	8 clocks
4'h3	3 clocks	12 clocks
:	:	:
4'hC	12 clocks	48 clocks
4'hD	13 clocks	52 clocks
4'hE	14 clocks	56 clocks
4'hF	15 clocks	60 clocks

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
MCP	1	NO[3:0]				0	0	DIV[1:0]		0	RTN[6:1]						0

RTN[6:1] – Set the 1H (1line) period in internal oscillator cycles. RTN[6:0] should be greater than or equal to 44 (= 2Ch)

Table 33 clocks per line (internal clock operation 1 clock = 1 OSC)

RTNI[6:0]	Clock per Line
7'h00 – 7'h2A	Setting disabled
7'h2C	44 clocks
7'h2E	46 clocks
7'h30	48 clocks
7'h32	50 clocks
…….	
7'h7C	124 clocks
7'h7E	126 clocks

DIV[1:0] – The internal oeration is synchronized with the clock, which is divided with the division ratio set with the DIV bits. Set the RTN and DIV bits to adjust frame frequency. If the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. See “Frame Frequency Adjustmemnt Function”. In RGB interface mode, the DIV bits are disabled.

DIV[1:0]	Division ratio	**Internal operation clock frequecy**
2’h0	1	Fosc/1
2’h1	2	Fosc/2
2’h2	4	Fosc/4
2’h3	8	Fosc/8

Formula to calculate frame frequency

$$Frame\ frequency = \frac{Fosc}{(Clock\ cycles\ per\ line * Division\ ratio * (Active\ line + BP + FP))}$$

Where,

fosc = frequency of RC oscillation,
Active line = number of active lines for driving liquid crystal (NL bits),
Division ratio = DIV bits,
Clock cycles per line = RTN bits,
FP = the number of lines for the front porch period and
BP = the number of lines for the back porch period.

NO[3:0] – Set the non-overlap period of outputs from adjacent gate lines .

Table 34

NO[3:0]	**Gate non-overlap time**	
	Internal operation (internal oscillator)	**RGB I/F operation (DOTCLK)**
4’h0	0 clock	0 clocks
4’h1	2 clocks	8 clocks
4’h2	4 clocks	16 clocks
4’h3	6 clocks	24 clocks
:	:	:
4’hC	24 clocks	96 clocks
4’hD	26 clocks	104 clocks
4’hE	28 clocks	112 clocks
4’hF	30 clocks	120 clocks

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	

RM – Selects the interface to access the LG4525B’s internal GRAM. The RAM access is possible only via the interface selected with the RM bit. Set RM to “1” when writing display data via the RGB interface. The LG4525B allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = “0” even while display operations are performed via the RGB interface.

Table 35 RM bit

RM	Interface for RAM access
1'h0	System interface/VSYNC interface
1'h1	RGB interface

RIM[1:0] – Selects one of the following RGB interface modes when the RGB interface mode is selected with the RM and DM bits. Make this setting before display operation via external display interface. Do not make changes to the setting during display operation.

Table 36 RIM[1:0] bits

RIM[1:0]	RGB interface mode
2'h00	18-bit RGB interface (1 transfer/pixel)
2'h01	16-bit RGB interface (1 transfer/pixel)
2'h10	6-bit RGB interface (3 transfers/pixel)
2'h11	Setting disabled

DM[1:0] – Sets the display operation mode. By setting DM[1:0] as follows, it is possible to switch between the internal clock operation mode and the external display interface mode. Do not switch between different external interface modes (RGB interface and VSYNC interface).

Table 37 DM[1:0] bits

DM[1:0]	Display operation mode
2'h00	Internal clock operation
2'h01	RGB interface
2'h10	VSYNC interface
2'h11	Setting disabled

Notes:
1. Instructions are set only via the system interface.
2. Be sure that data transfer and dot clock input is performed in units of RGB dots in 6-bit RGB interface mode.

As the following table, the optimum interface for the state of display can be selected by setting the external display interface mode.

Table 38

Display State	Operation mode	RAM access (RM)	Display mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 01)
Rewrite still picture area while display moving pictures	RGB interface (2)	System interface (RM = 0)	RGB interface (DM = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM = 10)

Notes:
1. Instructions are set only via the system interface.
2. The RGB-I/F and the VSYNC-I/F are not used simultaneously.
3. Do not make changes to the RGB-I/F mode setting (RIM) while the RGB I/F is in operation.
4. See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.

Internal clock operation mode

All display operations are synchronized with the signals generated from the internal operating clock in this mode. None of inputs via the external display interface are valid. The internal RAM is accessible only via the system interface.

RGB interface mode (1)

In RGB interface mode, display operations are synchronized with the frame synchronizing signal (VSYNC), the line synchronizing signal (HSYNC), and the dot clock (DOTCLK). These signals must be supplied through a display period using the RGB interface.

Display data are transferred in units of pixels via the DB[17:0] pins. All display data are stored in the internal RAM. The combined use of the high-speed RAM write mode and the widow address function enables not only displaying data in moving picture area and data in the internal RAM in other than the moving picture area at a time but also minimizing data transfer by transferring data only when rewriting screen.

The front porch (FP) and back porch (BP) periods, and the display duration period (NL) are automatically calculated inside the LG4525B by internally counting the number of line synchronizing signal clocks (HSYNC) from the falling edge of the frame synchronizing signal (VSYNC). Take this into consideration when transferring RGB data via the DB[17:0] pins.

RGB interface mode (2)

The LG4525B enables rewriting RAM data via the system interface while the RGB interface is selected for display operation. In this case, be sure to write RAM data while display data are not being transferred via the RGB interface (ENABLE = High). To return to the display data transfer mode via the RGB interface, change the ENABLE bit first and then set a new address (AD[15:0]) in the AC and the index register to R22h.

VSYNC interface mode

In VSYNC interface mode, internal display operations are synchronized with the frame synchronizing signal (VSYNC). In this mode, a moving picture can be displayed via the system interface by writing data to the internal RAM at more than the minimum speed from the falling edge of frame synchronizing signal (VSYNC). In this case, there are constraints in the RAM writing speed and method. For details, see “External Display Interface”.
No external signal input except VSYNC input is accepted in VSYNC interface mode.

The timings and durations of front porch (FP), back porch (BP) periods and display duration period (NL) are automatically calculated from the falling edge of the frame synchronization signal (VSYNC) according to the instructions set in the relevant registers.

Frame Rate Control (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	OHZ	0	0	0	FRS[4:0]				

FRS[4:0] – Set the frame rate when the internal resistor is used for oscillator circuit.
Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation via RGB interface.

Table 39

FRS[4:0]	Ratio of frequency	FRS[4:0]	Ratio of frequency
5'h00	x 0.32	5'h10	x 1.83
5'h01	x 0.42	5'h11	x 1.92
5'h02	x 0.52	5'h12	x 2.02
5'h03	x 0.62	5'h13	x 2.10
5'h04	x 0.71	5'h14	x 2.20
5'h05	x 0.81	5'h15	x 2.29
5'h06	x 0.90	5'h16	x 2.38
5'h07	x 1.00 (default)	5'h17	x 2.46
5'h08	x 1.09	5'h18	x 2.56
5'h09	x 1.19	5'h19	x 2.64
5'h0A	x 1.28	5'h1A	x 2.75
5'h0B	x 1.38	5'h1B	x 2.84
5'h0C	x 1.47	5'h1C	x 2.90
5'h0D	x 1.56	5'h1D	x 2.98
5'h0E	x 1.66	5'h1E	x 3.09
5'h0F	x 1.74	5'h1F	x 3.16

Note : When the default OSC frequency(FRS[4:0]=5'h07) is 0.92MHz and the register setting is FRS[4:0]=5'h04 , then OSC frequency = 0.92MHz x 0.71 = 0.66MHz

OHZ – Set the test mode

OHZ = 0 – FLM pin is normal output..

OHZ = 1 – FLM pin is clock input for test.

Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	SAP[2:0]				BT[2:0]			0	AP[2:0]			DK	DSTB	SLP	STB

STB – When STB = "1", the LG4525B enters the standby mode. In standby mode, the display operation completely halts, and the internal operation, including internal RC oscillation and reception of external clock pulses, completely halts. Only instructions to release the LG4525B from the standby mode (STB = "0") and to start oscillators are accepted during the standby mode. To set the standby mode, follow the sequence of standby mode setting.

SLP – When SLP = 1, the LG4525B enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change of GRAM data or instruction is accepted in sleep mode. The GRAM data and the instruction bits remain unchanged.

DSTB – When DSTB = 1, the LG4525B enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and the instruction bit setting are destroyed and must be reset after exiting deep standby mode.

DK – Activates AVDD. When DK = 0, AVDD activates at the same timing as VGH. When DK = 1, AVDD activates separately from VGH.

Table 40

DK	Step-up Cycle in Step-up Circuit 1
1'h0	Startup AVDD simultaneously with VGH. Startup step-up circuit 1 (AVDD output) according to AP[2:0]
1'h1	Halt step-up circuit 1 (AVDD). (Default)

AP[2:0] – Adjusts the constant current in the operation amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0]=3'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.
Adjust the amount of fixed current from the fixed-current source in the internal operational amplifier circuit. VGH operates when AP is not 000. Complete setting AP before setting PON = 1. (While setting PON = 1, setting of AP bit cannot be changed.) For the details of sequences, refer to Flow of "Power Supply Setting".

Table 41

AP[2:0]	LCD power supply circuits	Grayscale voltage generating circuit
3'h0	Halt operation	Halt operation
3'h1	Setting disabled	Setting disabled
3'h2	Normal operation	0.5
3'h3	Normal operation	0.75
3'h4	Normal operation	1
3'h5	Normal operation	1.25
3'h6	Normal operation	1.5
3'h7	Setting disabled	Setting disabled

Note: In this table, the constant current in operational amplifiers is shown by the ratio to the constant current when AP[1:0] is set to 2'h3.

BT[2:0] – Sets the factor used in the step-up circuits. Use an optimal step-up factor for the voltage in use. To reduce power consumption, set a smaller factor.

Table 42 Step up factor and output voltage level

BT[2:0]	AVDD	VGH	VGL	Capacitor connection Pins
3'h0	VCI1 x 2 [x 2]	AVDD x 3 [x 6]	–(VCI1 + AVDD x 2) [x –5]	AVDD, VGH, VGL, C11±, C12±, C13±, C21±, C22±
3'h1			–(AVDD x 2) [x –4]	AVDD, VGH, VGL, C11±, C12±, C21±, C22±
3'h2			–(VCI1 + AVDD) [x –3]	AVDD, VGH, VGL, C11±, C12±, C13±, C21±, C22±
3'h3		VCI1 + AVDD x 2 [x 5]	–(VCI1 + AVDD x 2) [x –5]	AVDD, VGH, VGL, C11±, C12±, C13±, C21±, C22±
3'h4			–(AVDD x 2) [x –4]	AVDD, VGH, VGL, C11±, C12±, C21±, C22±
3'h5			–(VCI1 + AVDD) [x –3]	AVDD, VGH, VGL, C11±, C12±, C13±, C21±, C22±
3'h6		AVDD x 2 [x 4]	–(AVDD x 2) [x –4]	AVDD, VGH, VGL, C11±, C12±, C21±, C22±
3'h7			–(VCI1 + AVDD) [x –3]	AVDD, VGH, VGL, C11±, C12±, C13±, C21±, C22±

Note: 1. The step-up factor from VCI1 are shown in the brackets [ ].
2. Connect capacitors where required when using AVDD, VGH, VGL voltages.
3. Set the following voltages within the respective ranges:
AVDD = (GVDD+0.5)V~6.0V, VGH-VGL≤32V, VGH>AVDD+0.5V, VGL<VCL-0.6V

SAP[2:0] – Adjust the constant current for the operational amplifier circuit in the source driver. A larger constant current stabilizes the operational amplifier circuit, but current consumption increases. Adjust the constant current taking the display quality-current consumption trade-off into account. During a period showing no display, set SAP = 0 to halt the operational amplifier circuit to reduce current consumption.

Table 43

SAP[2:0]	Constant current (ratio to 3)
3'h0	Halt operational amplifier
3'h1	Constant current (ratio to 3) : 0.65
3'h2	Constant current (ratio to 3) : 0.8
3'h3	Constant current (ratio to 3) : 1.00
3'h4	Constant current (ratio to 3) : 1.35
3'h5	Constant current (ratio to 3) : 1.60
3'h6	Setting disabled
3'h7	Setting disabled

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	DSEN	0	DC1[2:0]			0	DC0[2:0]			0	VC[2:0]		

DSEN – This bit enables the operation of clock synchronization mode.
DSEN = 0: Step-up is operated by divided oscillator clock.
DSEN = 1: Step-up is operated by synchronized line or frame clock.

Table 44 Step-up frequency (Step-up Circuit 1)

DC0[2:0]	Step-up circuit 1 : step-up frequency (f_{DCDC1})	
	DSEN = 0	**DSEN = 1**
3'h0	fosc/2	Internal clock / 2
3'h1	fosc/4	Internal clock / 4
3'h2	fosc/8	Internal clock / 8
3'h3	fosc/16	Internal clock / 16
3'h4	fosc/32	Internal clock / 32
3'h5	fosc/64	Internal clock / 64
3'h6	Halt step-up circuit 1	
3'h7	fosc/128	Internal clock / 128

Note : 1. Make sure to set DC0 and DC1 to maintain $f_{DCDC1} \geq f_{DCDC2}$.
2. Make sure to set DC0 to maintain RTN[6:0] ≥ division ratio for f_{DCDC1}

Table 45 Step-up frequency (Step-up Circuit 2)

DC1[2:0]	Step-up circuit 2 : step-up frequency (f_{DCDC2})	
	DSEN = 0	**DSEN = 1**
3'h0	fosc/16	Setting disable
3'h1	fosc/32	Line frequency / 2
3'h2	fosc/64	Line frequency / 4
3'h3	fosc/128	Line frequency / 8
3'h4	fosc/256	Line frequency / 16
3'h5	fosc/512	Line frequency / 32
3'h6	Halt step-up circuit 2	
3'h7	fosc/1024	Line frequency / 64

Note : Make sure to set DC0 and DC1 to maintain $f_{DCDC1} \geq f_{DCDC2}$.

Table 46 VCI1 output level

VC[2:0]	VCI1 (Reference Voltage) (VCI1 Voltage)
3'h0	1.00 x VCI
3'h1	0.93 x VCI
3'h2	0.88 x VCI
3'h3	0.82 x VCI
3'h4	0.78 x VCI
3'h5	0.74 x VCI
3'h6	0.70 x VCI
3'h7	Setting disabled

Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH[3:0]			

VRH[3:0] – Sets the factor to generate GVDD from VCI.

Table 47 GVDD

VRH[3:0]	GVDD Voltage
4'h0	Halt
4'h1	Halt
4'h2	Halt
4'h3	Halt
4'h4	Halt
4'h5	Halt
4'h6	Halt
4'h7	Halt
4'h8	VCI1 x 1.38
4'h9	VCI1 x 1.45
4'hA	VCI1 x 1.53
4'hB	VCI1 x 1.60
4'hC	VCI1 x 1.68
4'hD	VCI1 x 1.75
4'hE	VCI1 x 1.83
4'hF	Setting disabled

Note: Set the VC and VRH bits to maintain the GVDD voltage at (AVDD – 0.5) V or less.

PON – Controls the operation to generate VGL. In setting the PON bit, follows the power-supply startup sequence.

PON = 0 : Halts the step-up operation to generate VGL.
PON = 1 : Starts the step-up operation to generate VGL.

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV[4:0]					0	VCM[6:0]						

VCM[6:0] – Sets the VCOMH level (the higher voltage of VCOM alternating drive). VCM[6:0] specifies the voltage by GVDD x n, where n is a discrete number from 0.400 to 0.875. To halt internal volume and adjust VCOMH with an external resistor from VCOMR, set VCM[6:0] = "1111111".

Table 48

VCM [6:0]	VCOMH	VCM [6:0]	VCOMH	VCM [6:0]	VCOMH	VCM [6:0]	VCOMH
7'h00	GVDD x 0.400	7'h20	GVDD x 0.560	7'h40	GVDD x 0.720	7'h60	GVDD x 0.880
7'h01	GVDD x 0.405	7'h21	GVDD x 0.565	7'h41	GVDD x 0.725	7'h61	GVDD x 0.885
7'h02	GVDD x 0.410	7'h22	GVDD x 0.570	7'h42	GVDD x 0.730	7'h62	GVDD x 0.890
7'h03	GVDD x 0.415	7'h23	GVDD x 0.575	7'h43	GVDD x 0.735	7'h63	GVDD x 0.895
7'h04	GVDD x 0.420	7'h24	GVDD x 0.580	7'h44	GVDD x 0.740	7'h64	GVDD x 0.900
7'h05	GVDD x 0.425	7'h25	GVDD x 0.585	7'h45	GVDD x 0.745	7'h65	GVDD x 0.905
7'h06	GVDD x 0.430	7'h26	GVDD x 0.590	7'h46	GVDD x 0.750	7'h66	GVDD x 0.910
7'h07	GVDD x 0.435	7'h27	GVDD x 0.595	7'h47	GVDD x 0.755	7'h67	GVDD x 0.915
7'h08	GVDD x 0.440	7'h28	GVDD x 0.600	7'h48	GVDD x 0.760	7'h68	GVDD x 0.920
7'h09	GVDD x 0.445	7'h29	GVDD x 0.605	7'h49	GVDD x 0.765	7'h69	GVDD x 0.925
7'h0A	GVDD x 0.450	7'h2A	GVDD x 0.610	7'h4A	GVDD x 0.770	7'h6A	GVDD x 0.930
7'h0B	GVDD x 0.455	7'h2B	GVDD x 0.615	7'h4B	GVDD x 0.775	7'h6B	GVDD x 0.935
7'h0C	GVDD x 0.460	7'h2C	GVDD x 0.620	7'h4C	GVDD x 0.780	7'h6C	GVDD x 0.940
7'h0D	GVDD x 0.465	7'h2D	GVDD x 0.625	7'h4D	GVDD x 0.785	7'h6D	GVDD x 0.945
7'h0E	GVDD x 0.470	7'h2E	GVDD x 0.630	7'h4E	GVDD x 0.790	7'h6E	GVDD x 0.950
7'h0F	GVDD x 0.475	7'h2F	GVDD x 0.635	7'h4F	GVDD x 0.795	7'h6F	GVDD x 0.955
7'h10	GVDD x 0.480	7'h30	GVDD x 0.640	7'h50	GVDD x 0.800	7'h70	GVDD x 0.960
7'h11	GVDD x 0.485	7'h31	GVDD x 0.645	7'h51	GVDD x 0.805	7'h71	GVDD x 0.965
7'h12	GVDD x 0.490	7'h32	GVDD x 0.650	7'h52	GVDD x 0.810	7'h72	GVDD x 0.970
7'h13	GVDD x 0.495	7'h33	GVDD x 0.655	7'h53	GVDD x 0.815	7'h73	GVDD x 0.975
7'h14	GVDD x 0.500	7'h34	GVDD x 0.660	7'h54	GVDD x 0.820	7'h74	GVDD x 0.980
7'h15	GVDD x 0.505	7'h35	GVDD x 0.665	7'h55	GVDD x 0.825	7'h75	Setting disabled
7'h16	GVDD x 0.510	7'h36	GVDD x 0.670	7'h56	GVDD x 0.830	7'h76	Setting disabled
7'h17	GVDD x 0.515	7'h37	GVDD x 0.675	7'h57	GVDD x 0.835	7'h77	Setting disabled
7'h18	GVDD x 0.520	7'h38	GVDD x 0.680	7'h58	GVDD x 0.840	7'h78	Setting disabled
7'h19	GVDD x 0.525	7'h39	GVDD x 0.685	7'h59	GVDD x 0.845	7'h79	Setting disabled
7'h1A	GVDD x 0.530	7'h3A	GVDD x 0.690	7'h5A	GVDD x 0.850	7'h7A	Setting disabled
7'h1B	GVDD x 0.535	7'h3B	GVDD x 0.695	7'h5B	GVDD x 0.855	7'h7B	Setting disabled
7'h1C	GVDD x 0.540	7'h3C	GVDD x 0.700	7'h5C	GVDD x 0.860	7'h7C	Setting disabled
7'h1D	GVDD x 0.545	7'h3D	GVDD x 0.705	7'h5D	GVDD x 0.865	7'h7D	Setting disabled
7'h1E	GVDD x 0.550	7'h3E	GVDD x 0.710	7'h5E	GVDD x 0.870	7'h7E	Setting disabled
7'h1F	GVDD x 0.555	7'h3F	GVDD x 0.715	7'h5F	GVDD x 0.875	7'h7F	Halt internal volume.

Note : Set the VcomH voltage from (VCI - 0.5)V to (AVDD - 0.5)V

VDV[4:0] – Sets the alternating amplitudes of VCOM AC voltage. These bits amplify VCOM by from 0.6 to 1.23 times the GVDD voltage. If VCOMG = 0, VDV[4:0] bits are disabled.

Table 49

VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude
5'h00	GVDD x 0.60	5'h10	GVDD x 1.05
5'h01	GVDD x 0.63	5'h11	GVDD x 1.08
5'h02	GVDD x 0.66	5'h12	GVDD x 1.11
5'h03	GVDD x 0.69	5'h13	GVDD x 1.14
5'h04	GVDD x 0.72	5'h14	GVDD x 1.17
5'h05	GVDD x 0.75	5'h15	GVDD x 1.20
5'h06	GVDD x 0.78	5'h16	GVDD x 1.23
5'h07	GVDD x 0.81	5'h17	GVDD x 1.26
5'h08	GVDD x 0.84	5'h18	GVDD x 1.29
5'h09	GVDD x 0.87	5'h19	GVDD x 1.32
5'h0A	GVDD x 0.90	5'h1A	GVDD x 1.35
5'h0B	GVDD x 0.93	5'h1B	GVDD x 1.38
5'h0C	GVDD x 0.96	5'h1C	GVDD x 1.41
5'h0D	GVDD x 0.99	5'h1D	GVDD x 1.44
5'h0E	GVDD x 1.02	5'h1E	GVDD x 1.47
5'h0F	Setting disabled	5'h1F	GVDD x 1.50

Note : Set the VCOML voltage from (VCL + 0.5)V to 0V

VCOMG – When VCOMG = 1, the LG4525B can output a negative voltage level for VCOML (0V ~ -(VCL + 0.5V) Max.). When VCOMG = 0, the output of VCOML is fixed to GND level, and setting of the VDV[4:0] bits become invalid. And LG4525B halts the amplifier for negative voltage to save power. In this case, adjust the amplitude of (VCOMH-VCOML) voltage only with VCM[6:0] bits.
VCOMG = 1 is valid only when PON = 1. So set PON = 1 ahead, before setting VCOMG = 1.

Regulator Control 1 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RSET			0	RI[2:0]			0	RV[2:0]			0	RCONT[2:0]		

RCONT[2:0] – These bits control the input voltage of main bias op_amp.

Table 50

RCONT[2:0]	Input voltage
3'h0	VCI x 0.25
3'h1	Setting disabled
3'h2	Open
3'h3	VCI x 0.30
3'h4	Setting disabled
3'h5	Setting disabled
3'h6	VCI x 0.20
3'h7	Setting disabled

RV[2:0] – These bits control the output voltage of internal logic regulator.

Table 51

RV [2:0]	Vdd voltage
3'h0	VCI x 0.80
3'h1	VCI x 0.75
3'h2	VCI x 0.70
3'h3	VCI x 0.65
3'h4	VCI x 0.60
3'h5	VCI x 0.55
3'h6	VCI x 0.50
3'h7	VCI x 0.45

RI[2:0] – These bits control the bias current of internal logic regulator.

Table 52

RI [2:0]	Logic regulator bias current
3'h0	x 1
3'h1	x 2
3'h2	x 3
3'h3	x 4
3'h4	x 5
3'h5	x 6
3'h6	x 7
3'h7	x 8

Note : In this table, the constant current is shown by the ratio to the constant current when RI[2:0] is set to 3'h3.

RSET[2:0] – These bits control the main bias.

Table 53

RSET[2:0]	Main bias current
3'h0	x 0.39
3'h1	x 0.43
3'h2	x 0.48
3'h3	x 0.56
3'h4	x 0.65
3'h5	x 0.79
3'h6	x 1.00 (default)
3'h7	x 1.36

Regulator Control 2 (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0

W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S_MULTI

S_MULTI – It controls output size of Amp used for source output. Recommend.

Gamma Select Control (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	EN_MA	0	0	0	PS

PS – This bit specifies the VA mode enable signal.

Table 54

PS	Mode
1'h0	TN mode
1'h1	VA mode

EN_MA – This bit specify the PFN0-5/PFP0-1/PMN/PMP registers Manual setting enable signal

Table 55

		EN_MA	PS
Auto	TN mode	0	0
	VA mode	0	1
Manual	User setting	1	x

RAM Address Set (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD[15:0]															

AD[15:0] – A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as data is written to the internal GRAM in order to write data consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM='1'), the address AD[15:0] is set in the address counter every frame on the falling edge of VSYNC.
Note 2: In internal clock operation and VSYNC interface operation (RM='0'), the address AD[15:0] is set when executing the instruction.

Table 56

AD[15:0]	GRAM Data Setting
16'h0000 – 16'h00AF	Bitmap data on the first line
16'h0100 – 16'h01AF	Bitmap data on the second line
16'h0200 – 16'h02AF	Bitmap data on the third line
:	:
16'hD900 – 16'hD9AF	Bitmap data on the 218th line
16'hDA00 – 16'hDAAF	Bitmap data on the 219th line
16'hDB00 – 16'hDBAF	Bitmap data on the 220th line

Write Data to RAM (R22h)

R/W	RS	The bit assignment between RAM write data WD[17:0] and DB[17:0] differs according to the selected interface.
W	1	WD[17:0]

WD[17:0] – The LG4525B writes data to the internal GRAM by expanding into 18 bits internally. The data expansion format into 18 bits differs according to the interface.

The GRAM data represents the grayscale level. The LG4525B automatically updates the address according to AM and I/D[1:0] as it writes data in the GRAM. In standby mode, the GRAM is not accessible. The data in 16-bit format is developed into 18 bits according to the register setting (DFM) in 8-/16-bit interface operation.

Note : When writing data in the GRAM via system interface while using the RGB interface, make sure that write operation via two interface do not conflict.

Table 57 GRAM data and corresponding LCD Grayscale level (REV = 1)

GRAM data RGB	Grayscale level	
	Negative	Positive
6'h00	V63	V0
6'h01	V62	V1
6'h02	V61	V2
6'h03	V60	V3
6'h04	V59	V4
6'h05	V58	V5
6'h06	V57	V6
6'h07	V56	V7
6'h08	V55	V8
6'h09	V54	V9
6'h0A	V53	V10
6'h0B	V52	V11
6'h0C	V51	V12
6'h0D	V50	V13
6'h0E	V49	V14
6'h0F	V48	V15
6'h10	V47	V16
6'h11	V46	V17
6'h12	V45	V18
6'h13	V44	V19
6'h14	V43	V20
6'h15	V42	V21
6'h16	V41	V22
6'h17	V40	V23
6'h18	V39	V24
6'h19	V38	V25
6'h1A	V37	V26
6'h1B	V36	V27
6'h1C	V35	V28
6'h1D	V34	V29
6'h1E	V33	V30
6'h1F	V32	V31

GRAM data RGB	Grayscale level	
	Negative	Positive
6'h20	V31	V32
6'h21	V30	V33
6'h22	V29	V34
6'h23	V28	V35
6'h24	V27	V36
6'h25	V26	V37
6'h26	V25	V38
6'h27	V24	V39
6'h28	V23	V40
6'h29	V22	V41
6'h2A	V21	V42
6'h2B	V20	V43
6'h2C	V19	V44
6'h2D	V18	V45
6'h2E	V17	V46
6'h2F	V16	V47
6'h30	V15	V48
6'h31	V14	V49
6'h32	V13	V50
6'h33	V12	V51
6'h34	V11	V52
6'h35	V10	V53
6'h36	V9	V54
6'h37	V8	V55
6'h38	V7	V56
6'h39	V6	V57
6'h3A	V5	V58
6'h3B	V4	V59
6'h3C	V3	V60
6'h3D	V2	V61
6'h3E	V1	V62
6'h3F	V0	V63

Table 58 GRAM data and corresponding LCD Grayscale level (REV = 0)

GRAM data RGB	Grayscale level	
	Negative	Positive
6'h00	V0	V63
6'h01	V1	V62
6'h02	V2	V61
6'h03	V3	V60
6'h04	V4	V59
6'h05	V5	V58
6'h06	V6	V57
6'h07	V7	V56
6'h08	V8	V55
6'h09	V9	V54
6'h0A	V10	V53
6'h0B	V11	V52
6'h0C	V12	V51
6'h0D	V13	V50
6'h0E	V14	V49
6'h0F	V15	V48
6'h10	V16	V47
6'h11	V17	V46
6'h12	V18	V45
6'h13	V19	V44
6'h14	V20	V43
6'h15	V21	V42
6'h16	V22	V41
6'h17	V23	V40
6'h18	V24	V39
6'h19	V25	V38
6'h1A	V26	V37
6'h1B	V27	V36
6'h1C	V28	V35
6'h1D	V29	V34
6'h1E	V30	V33
6'h1F	V31	V32
6'h20	V32	V31
6'h21	V33	V30
6'h22	V34	V29
6'h23	V35	V28
6'h24	V36	V27
6'h25	V37	V26
6'h26	V38	V25
6'h27	V39	V24
6'h28	V40	V23
6'h29	V41	V22
6'h2A	V42	V21
6'h2B	V43	V20
6'h2C	V44	V19
6'h2D	V45	V18
6'h2E	V46	V17
6'h2F	V47	V16
6'h30	V48	V15
6'h31	V49	V14
6'h32	V50	V13
6'h33	V51	V12
6'h34	V52	V11
6'h35	V53	V10
6'h36	V54	V9
6'h37	V55	V8
6'h38	V56	V7
6'h39	V57	V6
6'h3A	V58	V5
6'h3B	V59	V4
6'h3C	V60	V3
6'h3D	V61	V2
6'h3E	V62	V1
6'h3F	V63	V0

Read Data from RAM (R22h)

R/W	RS	The bit assignment between RAM write data RD[17:0] and DB[17:0] differs according to the selected interface.
R	1	RD[17:0]

RD[17:0] – 18-bit data read from the GRAM. The bit assignment between RD[17:0] and DB[17:0] (data on the data bus) differs according to the selected interface.

When the LG4525B read data from the GRAM to the microcomputer, the first word read immediately after RAM address set is taken in the internal read-data latch and invalid data is sent to the data bus DB[17:0]. Valid data is sent to the data bus as the LG4525B reads out the second and subsequence words.

When either 8-bit or 16-bit interface is selected, the LSB of R and B dot data are not read out.

Note : This register is not available in RGB interface operation.

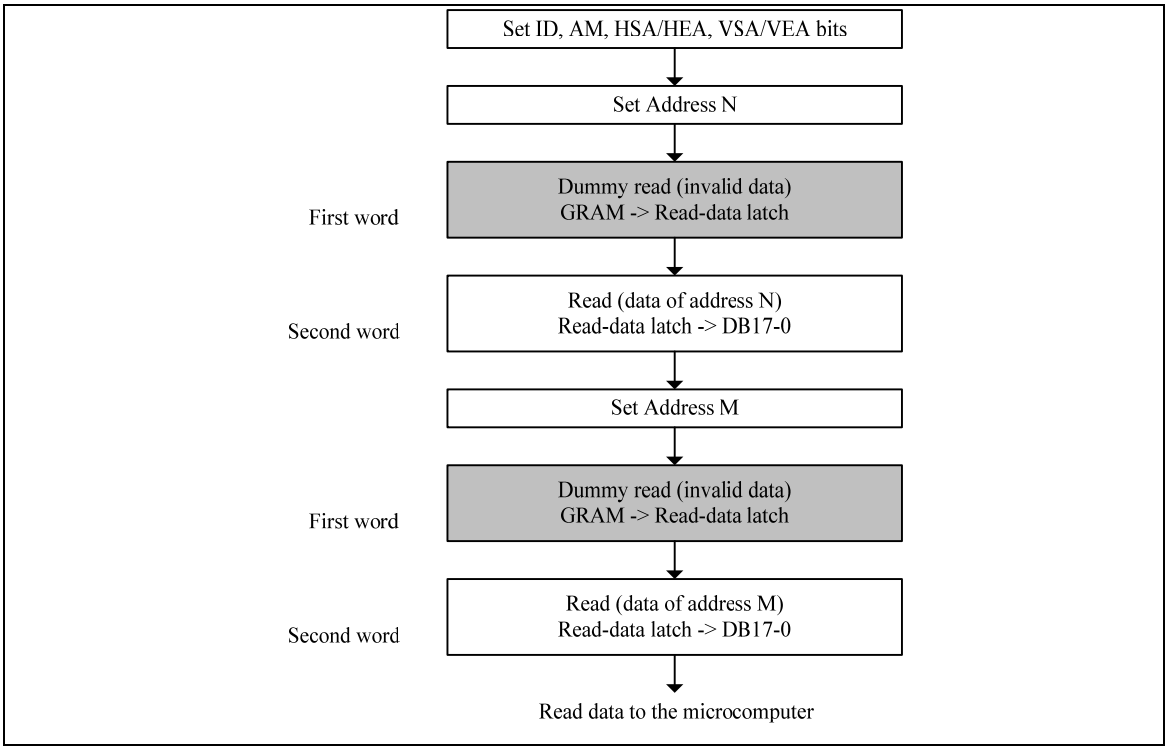


Figure 13

Sortware Reset (R28h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST

SRST – When SRST=1, software is reset.
When SRST=0, software reset is canceled.

Gamma Control 1-16 (R30h to R3Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				
W	1						PFP1[2:0]								PFP0[2:0]		
W	1						PFP3[2:0]								PFP2[2:0]		
W	1						PFN1[2:0]								PFN0[2:0]		
W	1						PFN3[2:0]								PFN2[2:0]		
W	1														PMP[2:0]		
W	1														PMN[2:0]		

PKP5-0[2 :0] – γ fine-adjustment register for positive polarity
PRP1-0[2 :0] – γ gradient-adjustment register for positive polarity
VRP0[3:0], VRP1[4 :0] – γ amplitude-adjustment register for positive polarity

PKN5-0[2 :0] – γ fine-adjustment register for negative polarity
PRN1-0[2 :0] – γ gradient-adjustment register for negative polarity
VRN0[3:0], VRN1[4 :0] – γ amplitude-adjustment register for negative polarity

PFP3-0[2:0] – γ fine adjustment register bits for positive polarity
PFN3-0[2:0] – γ fine adjustment register bits for negative polarity
PMP[2:0] – γ fine adjustment register bits for positive polarity
PMN[2:0] – γ fine adjustment register bits for negative polarity

For details, see "γ-Correction Function" section

Gate Scan Position (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	SCN[4:0]					

SCN[4:0] – Specifies the gate line where the gate driver starts scan.

Table 59

SCN[4:0]	**Gate line No (Scan start position)**			
	SM = 0		**SM = 1**	
	GS = 0	**GS = 1**	**GS = 0**	**GS = 1**
5'h00	G1	G220	G1	G220
5'h01	G9	G212	G17	G204
5'h02	G17	G204	G33	G188
5'h03	G25	G196	G49	G172
5'h04	G33	G188	G65	G156
5'h05	G41	G180	G81	G140
5'h06	G49	G172	G97	G124
5'h07	G57	G164	G113	G108
5'h08	G65	G156	G129	G92
5'h09	G73	G148	G145	G76
5'h0A	G81	G140	G161	G60
5'h0B	G89	G132	G177	G44
5'h0C	G97	G124	G193	G28
5'h0D	G105	G116	G209	G12
5'h0E	G113	G108	G2	G219
5'h0F	G121	G100	G18	G203
5'h10	G129	G92	G34	G187
5'h11	G137	G84	G50	G171
5'h12	G145	G76	G66	G155
5'h13	G153	G68	G82	G139
5'h14	G161	G60	G98	G123
5'h15	G169	G52	G114	G107
5'h16	G177	G44	G130	G91
5'h17	G185	G36	G146	G75
5'h18	G193	G28	G162	G59
5'h19	G201	G20	G178	G43
5'h1A	G209	G12	G194	G27
5'h1B	G217	G4	G210	G11
5'h1C – 5'h1F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Vertical Scroll Control (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VL[7:0]							

VL[7:0] – Sets the amount of scrolling the base image by the number of lines. The RAM data in the start line address is displayed on the line, which is shifted from the first line of the liquid crystal panel by the number of lines set with VL[7:0]. In setting VL[7:0], make sure VL ≤ 220

First screen position (R42h)

Second screen position (R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE1[7:0]								SS1[7:0]							
W	1	SE2[7:0]								SS2[7:0]							

SS1[7:0] – Sets the position of the start line from which the first display starts. The gate driver starts scan from the line of the number set with the SS1 bits + 1.

SE1[7:0] – Sets the position of the end line at which the first display ends. The gate driver ends scan at the line of the number set with the SE1 bits + 1. For instance, when SS1 = 07h and SE1 = 10h, the first display is shown on the gate lines from G8 to G17, and gate lines G1 to G7 and G18 thereafter are driven to show a blank screen. Be sure that SS1 ≤ SE1 ≤ DBh. For details, see the “Partial Display Timing” section.

SS2[7:0] – Sets the position of the start line from which the second display starts. The gate driver starts scan from the line of the number set with the SS2 bits + 1. The second display is shown when SPT = “1”.

SE2[7:0] – Sets the position of the end line at which the second display ends. The gate driver ends scan at the line of the number set with the SE2 bits + 1. For instance, when SPT = “1”, and SS2 = 20h, SE2 = 4Fh, the second display is shown on the gate lines from G33 to G80.

Be sure that SS1 ≤ SE1 < SS2 ≤ SE2 ≤ DBh. For details, see the “Partial Display Timing” section

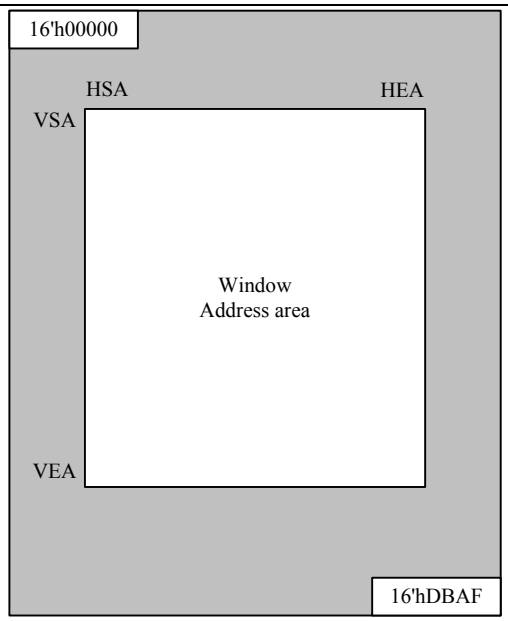
Horizontal RAM Address (R44h)

Vertical RAM Address (R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA[7:0]								HSA[7:0]							
W	1	VEA[7:0]								VSA[7:0]							

HSA[7:0]/HEA[7:0] – HSA[7:0] and HEA[7:0] represent the addresses at the start and end of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the range on the GRAM to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8’h00 ≤ HSA < HEA ≤ 8’hAF.

VSA[7:0]/VEA[7:0] – VSA[7:0] and VEA[7:0] represent the addresses at the start and end of the window address area in vertical direction, respectively. VSA[7:0] and VEA[7:0] specify the range on the GRAM to write data. Set VSA[7:0] and VEA[7:0] before starting RAM write operation. In setting, make sure that 8’h000 ≤ VSA < VEA ≤ 8’hDB.



Window address area
8'h00 <= HSA < HEA <= 8'hAF
8'h00 <=VSA < VEA <= 8'hDB

Note 1) Make an window address area within the GRAM address area.
Note 2) Make sure to set AD15-0 an address and the start of line within the window address area.

Figure 14

EPROM Control Register 1 (R50h)

EPROM programming control. See "EPROM Control" section.

PDIN[7:0] – Data input. This corresponds to VCM[6:0] bits of R13h.

PA[1:0] – address input. This selects one of four banks of the EPROM.

Table 60

PA[1:0]	Write Data Input	Write OPT Cell
2'h0	PDIN[6:0]	Cell[6:0]
2'h1	PDIN[6:0]	Cell[14:8]
2'h2	PDIN[6:0]	Cell[22:16]
2'h3	PDIN[6:0]	Cell[30:24]

PWE – Write enable.

PPROG – Program mode enable.

VPP – Power switch control for the VPP pin of the embedded EPROM. When VPP = "1", the internal VPP is set to 7.2V; otherwise it is set to 1.8V.

POR – Pulse for read operation.

PTM[1:0] – Pins for enabling test mode

EPROM Control Register 2 (R51h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0										AUTOWR	RA[1:0]		VCMSEL[1:0]	

EPROM programming control. See “EPROM Control” section.

VCMSEL[1:0] – With VCMSEL pin, sets VcomH level from either the register R13h or the EPROM

Table 61

VCMSEL[1:0]	VcomH Level adjustment
00	VCM[6:0] of the register R13h
01	EPROM data at first if EPROM has data. Otherwise,VCM[6:0] of the register R13h
1x	EPROM data selected by RA[1:0]

RA[1:0] – Read address input. This selects one of four banks of the EPROM.

AUTOWR – Select the methoe of write operation
If AUTOWR=’1’, write address is PA.
Else AUTOWR=’0’, write address is auto select address.

Note : If the VCMSEL=”01”, “10” or “11”, you must set and reset the POR register to make the stable reading of data from the EPROM.
That is, you must run the following sequence before entering the “LCD Power Supply ON sequence”. Otherwise, the abnormal reading from the EPROM can make the image quality wrong.
Also, in the case that AUTOWR=’1’, you must run the following sequence before entering the writing sequence of the EPROM. See “Power Supply Instrunction Setting”

EPROM Control Register 3 (R52h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0								PDOUT[7:0]						

PDOUT[7:0] – EPROM Read Data output.

Test Register 1 (R71h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	OV	0	0	0	MWRM	0	T8CL	TVCOM[1:0]		0	0	TOSC	TDFN

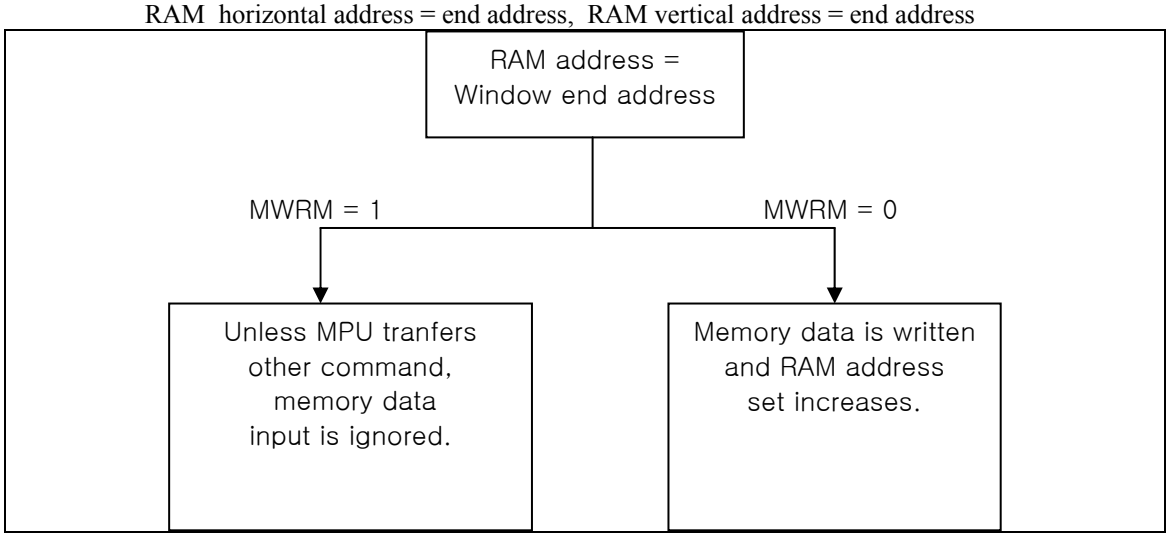
TDFN – Sets for the function test.
TOSC – Sets for the oscillator test.
TVCOM[1:0] – Sets the VCOM output level for test.

Table 62

TVCOM [1:0]	VCOM Level
2’h0	modulation
2’h1	modulation
2’h2	VCOML
2’h3	VCOMH

T8CL – Sets power saving for particular images. T8CL = "1", that means it has a chance to reserve power and "0" means it operates normally when images are displayed.

MWRM – Set Memory Write Mode.
RAM horizontal address = end address, RAM vertical address = end address



OV – Set data overwrite enable.
OV = 1 : data overwrite disable
OV = 0 : data overwrite enable.

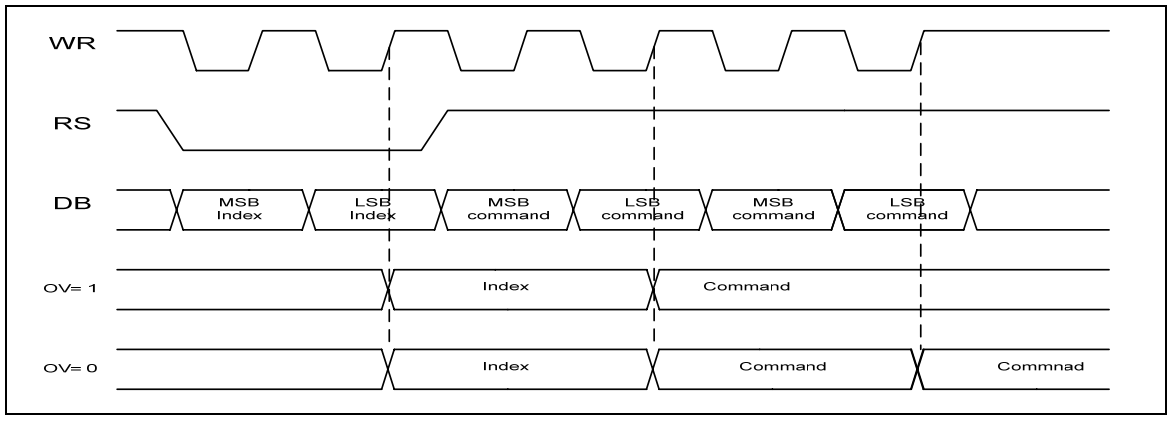


Figure 15

Test Register 2 (R72h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	REG ULPD	0	0	0	S_HIZ	0	0	0	0	0	0	0	MULTIVCOM

REGULPD – Sets
S_HIZ – stepup2
MULTIVCOM – Used for Device test.

Test Register 3 (R73h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	TDLY[1:0]		0	0	0	0	0	0	RDSM[1:0]		0	0	WRPW[1:0]	

WRPW[1:0] – Used for memory write pulse width test.
RDSM[1:0] – Used for memory read sensing margin test.
TDLY[1:0] – Sets for the delay time test

Test Register 4 (R74h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	TSAP	0	0	0	TSHZ	0	0	0	TVON	0	HaltVreg	0	SBC

SBC – Source Bias control Used for memory write pulse width test.
HaltVreg – Used for Device test.
TVON – Used for Device test.
TSHZ – Sets
TSAP – Sets

Instruction List

Index	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	Start oscillation																1
01h	Driver output control 1		VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	SM (0)	GS (0)	SS (0)				NL[4:0] (1B)				
02h	LCD Driving Wave Control					FLD[1:0] (01)		BC0 (0)	EOR (0)			NW[5:0] (000000)					
03h	Entry mode	TRI (0)	DFM (0)		BGR (0)							I/D[1:0] (11)		AM (0)		EPF[1:0] (00)	
04h	Resizing Control							RCV[1:0] (00)				RCH[1:0] (00)				RSZ[1:0] (00)	
07h	Display Control 1			PTS[2:0] (000)			VLE[1:0] (000)		SPT (0)			GON (0)	DTE (0)	COL (0)	REV (0)	D[1:0] (00)	
08h	Display Control 2	FP[7:0] (00001000)								BP[7:0] (00001000)							
09h	Display Control 3											PTG[1:0] (00)		ISC[3:0] (0000)			
0Ah	Display Control 4	EQ[3:0] (0000)				SEQ[3:0] (0000)				SDT[3:0] (0000)				MCP[3:0] (0000)			
0Bh	Frame cycle adjustment	NO[3:0] (0000)						DIV[1:0] (00)			RTN[6:1] (010110)						
0Ch	External display Interface Control								RM (0)			DM[1:0] (00)				RIM[1:0] (00)	
0Fh	Oscillation Control								OHZ (0)				FRS[4:0] (00111)				
10h	Power Control 1		SAP[2:0] (000)				BT[2:0] (0000)				AP[2:0] (000)			DK (1)	DSTB (0)	SLP (0)	STB (0)
11h	Power Control 2				DSEN (0)		DC1[2:0] (110)				DC0[2:0] (110)				VC[2:0] (000)		
12h	Power Control 3												PON (0)	VRH[3:0] (0000)			
13h	Power Control 4			VCOMG (0)	VDV[4:0] (00000)						VCM[6:0] (0000000)						
14h	Regulator Control 1		RSET[2:0] (110)				RI[2:0] (000)				RV[2:0] (011)				RCONT (000)		
15h	Regulator Control 2																S_MULTI (0)
16h	Gamma Select Control												EN_MA (0)				PS (0)
21h	RAM Address Set	AD[15:0] (0000000000000000)															
22h	RAM Data	WD[17:0] or RD[17:0]															
28h	Software Reset																SRST (0)
30h	Gamma Control 1						PKP1[2:0] (000)								PKP0[2:0] (000)		
31h	Gamma Control 2						PKP3[2:0] (000)								PKP2[2:0] (000)		
32h	Gamma Control 3						PKP5[2:0] (000)								PKP4[2:0] (000)		
33h	Gamma Control 4						PRP1[2:0] (000)								PRP0[2:0] (000)		
34h	Gamma Control 5						PKN1[2:0] (000)								PKN0[2:0] (000)		
35h	Gamma Control 6						PKN3[2:0] (000)								PKN2[2:0] (000)		
36h	Gamma Control 7						PKN5[2:0] (000)								PKN4[2:0] (000)		
37h	Gamma Control 8						PRN1[2:0] (000)								PRN0[2:0] (000)		
38h	Gamma Control 9				VRP1[4:0] (00000)								VRP0[4:0] (00000)				
39h	Gamma Control 10				VRN1[4:0] (00000)								VRN0[4:0] (00000)				
3Ah	Gamma Control 11						PFP1[2:0] (001)								PFP0[2:0] (001)		
3Bh	Gamma Control 12						PFP3[2:0] (001)								PFP2[2:0] (001)		
3Ch	Gamma Control 13						PFN1[2:0] (001)								PFN0[2:0] (001)		
3Dh	Gamma Control 14						PFN3[2:0] (001)								PFN2[2:0] (001)		
3Eh	Gamma Control 15														PMP[2:0] (001)		

3Fh	Gamma Control 16													PMN[2:0] (001)	
40h	Gate scan start position												SCN[4:0] (00000)		
41h	Vertical scroll control									VL[7:0] (00000000)					
42h	Frist Screen position	SE1[7:0] (11111111)								SS1[7:0] (00000000)					
43h	Second Screen position	SE2[7:0] (11111111)								SS2[7:0] (00000000)					
44h	Horizontal RAM Address	HEA[7:0] (10101111)								HSA[7:0] (00000000)					
45h	Vertical RAM Address	VEA[7:0] (11011011)								VSA[7:0] (00000000)					
50h	EPROM Control 1	PTM[1:0] (00)		POR (0)	VPP (0)	PPROG (0)	PWE (0)	PA[1:0] (00)		PDIN[7:0] (00000000)					
51h	EPROM Control 2												AUTOWR (0)	RA[1:0] (00)	VCMSEL[1:0] (00)
52h	EPROM Control 3									PDOUT[7:0] (11111111)					
71h	Test register 1				OV (0)				MWRM (0)		T&CL (0)	TVCOM[1:0] (00)			TOSC (0) TDFN (0)
72h	Test register 2				REGULPD (0)				S_HIZ (0)						MULTIVCOM (1)
73h	Test register 3			TDLY[1:0] (00)								RDSM[1:0] (00)			WRPW[1:0] (00)
74h	Test register 4				TSAP (0)				TSHZ (0)				TVON (0)	HaltVreg (0)	SBC (0)

Reset Function

The LG4525B is initialized with a RESET input. During a reset period, the LG4525B is in a busy state and neither instruction nor access to the GRAM data from the MPU is accepted. The LG4525B's internal power supply circuit unit is initialized also with a RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, neither access to the internal GRAM nor initial setting of instruction bits is accepted.

1. Initial state of instruction bits (default)
See the instruction list. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization
The RAM data is not automatically initialized with a RESET input and must be initialized by software in a display-off period (D1-0 = "00").

3. Output pin initial state *See note

1. LCD driver S1~S528	: GND
G1~G220	: VGL (= GND)
2. VCOM	: GND
3. VCOMR	: Hi-Z
4. VCOMH	: Hi-Z
5. VCOML	: GND
6. GVDD	: Hi-Z
7. VCI1	: VCI
8. AVDD	: VCI
9. VGH	: AVDD (= VCI)
10. VGL	: GND
11. VCL	: GND
12. VDD	: VDD
13. FLM	: GND
14. SDO	: GND

4. Initial state of input/output pins* See note

1. C11P	: VCI1
2. C11M	: GND
3. C12P	: VCI1
4. C12M	: GND
5. C31P	: VCI1
6. C31M	: GND
7. C21P	: AVDD (= VCI)
8. C21M	: GND
9. C22P	: AVDD (= VCI)
10. C22M	: GND

Note: The above-mentioned initial states of output and input pins are the ones when the LG4525B's power supply circuit is connected as exemplified in "Wiring example".

5. Note on Reset function

(1) When a RESET input is entered into the LG4525B while it is in deep standby mode, the LG4525B starts up the inside logic regulator and makes a transition to the initial state. During this period, the interface pins may be under an unstable condition. For this reason, do not enter a RESET input in deep standby mode.

(2) When transferring instruction using either two or three transfer mode via 8-/9-/16-bit interface, make sure to execute data transfer synchronization after executing a reset operation.

Basic Mode operation of the LG4525B

The basic operation modes of the LG4525B are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

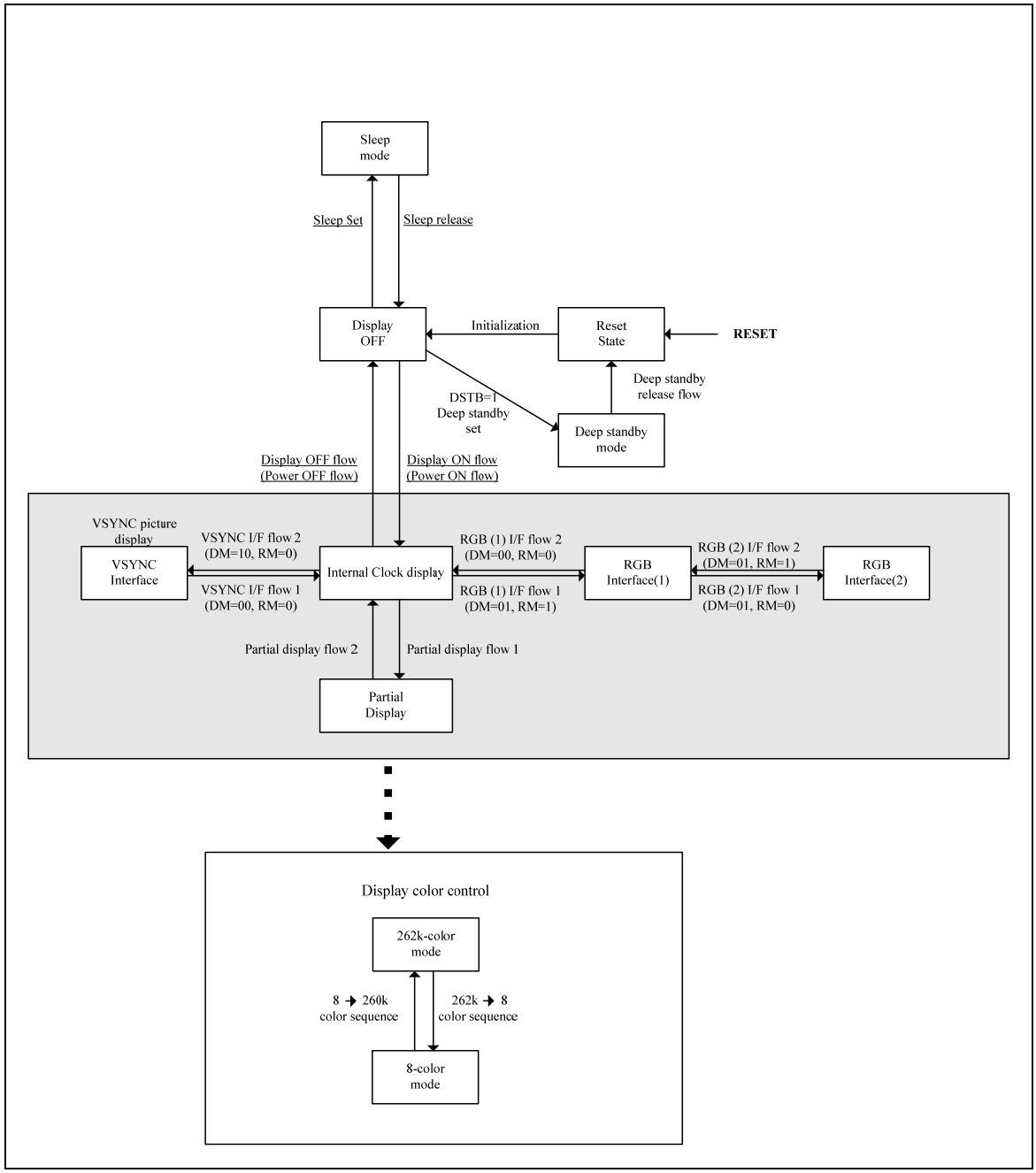


Figure 16

Interface and data format

The LG4525B supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The LG4525B allows selecting an optimum interface according to the kind of display (moving or still picture) in order to transfer data efficiently.

As external display interface, the LG4525B supports RGB interface and VSYNC interface, both enabling data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the LG4525B writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the LG4525B's GRAM in order to minimize the data transfer by transferring data only when it is necessary to switch the moving picture frames. The window address function specifies the RAM area where data is rewritten for moving picture display and enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display using system interface by writing data to the GRAM at more than a certain speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in speed and methods of writing data to the internal RAM.

The LG4525B can operate in either one of the following four modes according to the state of display. The display operation mode is determined by setting the external interface control register. When switching between different modes, make sure to refer to mode switching sequence.

Table 63

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM[1:0]) while RGB interface is in operation.
4. See the "External Display Interface" section for the mode transition sequence.

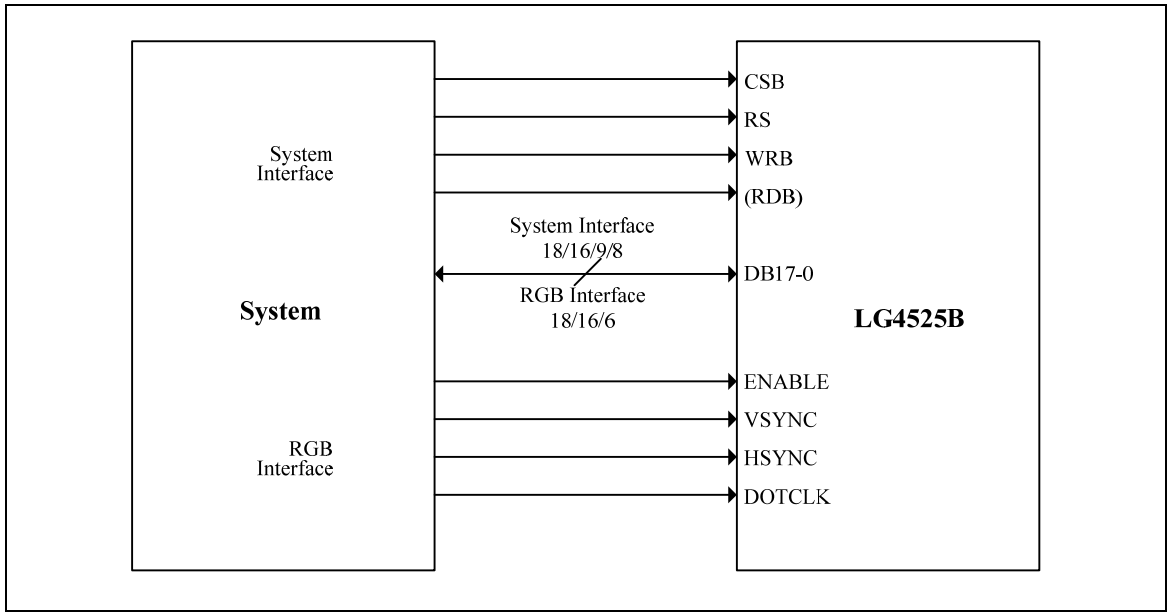


Figure 17 LG4525B's Interface

Internal clock operation
The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. Any input via external display interface is invalid in this operation. The internal RAM is accessible only via system interface.

RGB interface operation (1)
The display operation is synchronized with the frame synchronous signal (VSYNC), the line synchronous signal (HSYNC), and the dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied throughout the display period using RGB interface.
The LG4525B transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function enables the LG4525B to display a moving picture and the data in other than the moving picture RAM area simultaneously and transferring only data to be overwritten in the moving picture RAM area when7 rewriting the moving picture RAM area. This structure can minimize the total number of data transfer.
The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the LG4525B by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with these settings.

RGB interface operation (2)
This mode enables the LG4525B to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first and then set a new address and the index register to R22h.

VSYNC interface operation
The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the LG4525B to display a moving picture using system interface by writing data to the internal RAM at more than a minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are constraints in speed and methods of writing RAM data. For details, see the "VSYNC Interface" section. As an external input, only VSYNC signal input is valid in this mode. Any other input via external display interface is invalid.
The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) according to the register settings inside the LG4525B.

System Interface

The following are the kinds of system interfaces available with the LG4525B. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 64

TEST_MODE[1]	IM[3:0]	Interface Mode with MPU	DB pins	Colors
0	0000	68-system 16-bit interface	DB[17:10], DB[8:1]	262,144 *see Note 1
0	0001	68-system 8-bit interface 1	DB[17:10]	262,144 *see Note 2
0	0010	80-system 16-bit interface	DB15-0	262,144 *see Note 1
0	0011	80-system 8-bit interface 1	DB7-0	262,144 *see Note 2
0	010*	Clock synchronous serial interface	SDI,SDO	65,536
0	1000	68-system 18-bit interface	DB[17:0]	262,144
0	1001	68-system 9-bit interface 1	DB[17:9]	262,144
0	1010	80-system 18-bit interface	DB[17:0]	262,144
0	1011	80-system 9-bit interface 1	DB[17:9]	262,144
1	0001	68-system 8-bit interface 2	DB[8:1]	262,144 *see Note 2
1	1001	68-system 9-bit interface 2	DB[8:0]	262,144
1	0011	80-system 8-bit interface 2	DB[8:1]	262,144 *see Note 2
1	1011	80-system 9-bit interface 2	DB[8:0]	262,144

Notes: 1. 65,536 colors in 16-bit signal transfer mode.
2. 65,536 colors in 8-bit 2-transfer mode.

80-system 18-bit Bus Interface

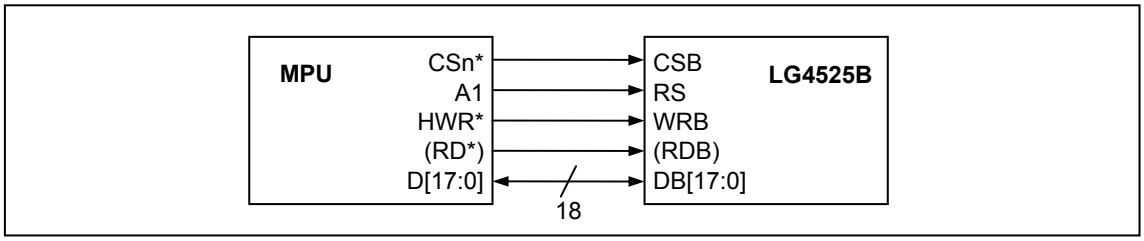


Figure 18 18-bit Interface

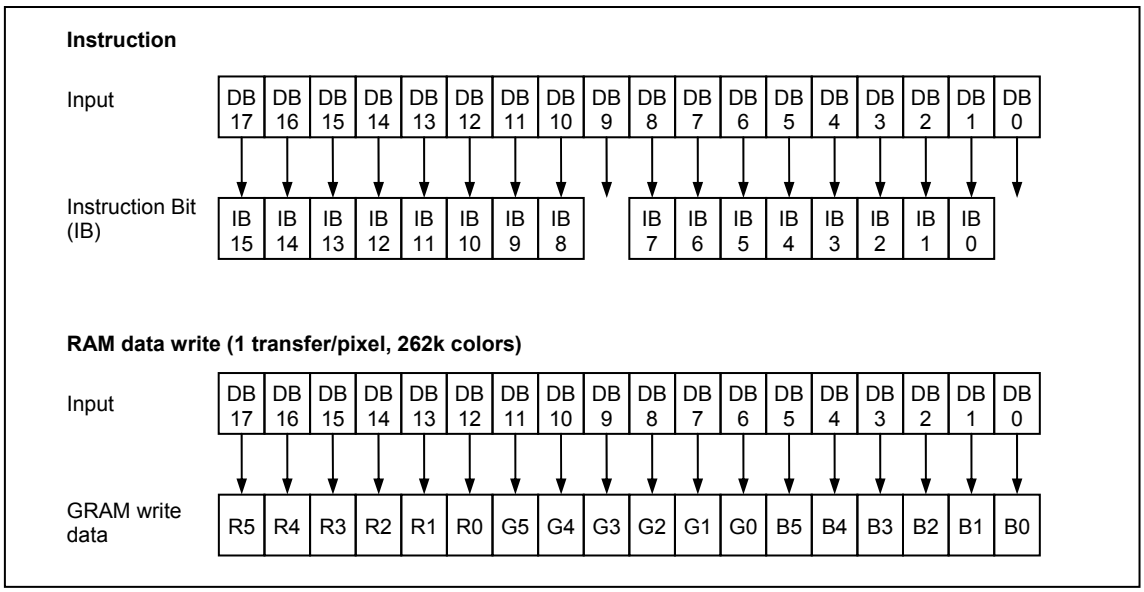


Figure 19 Data format for 18-bit interface

80-system 16-bit Bus Interface

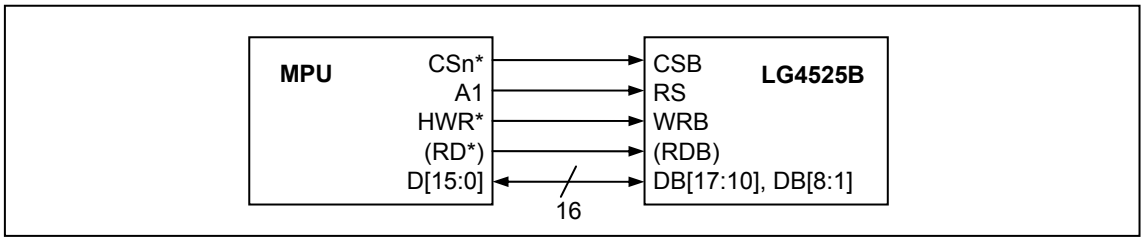


Figure 20 16-bit Interface

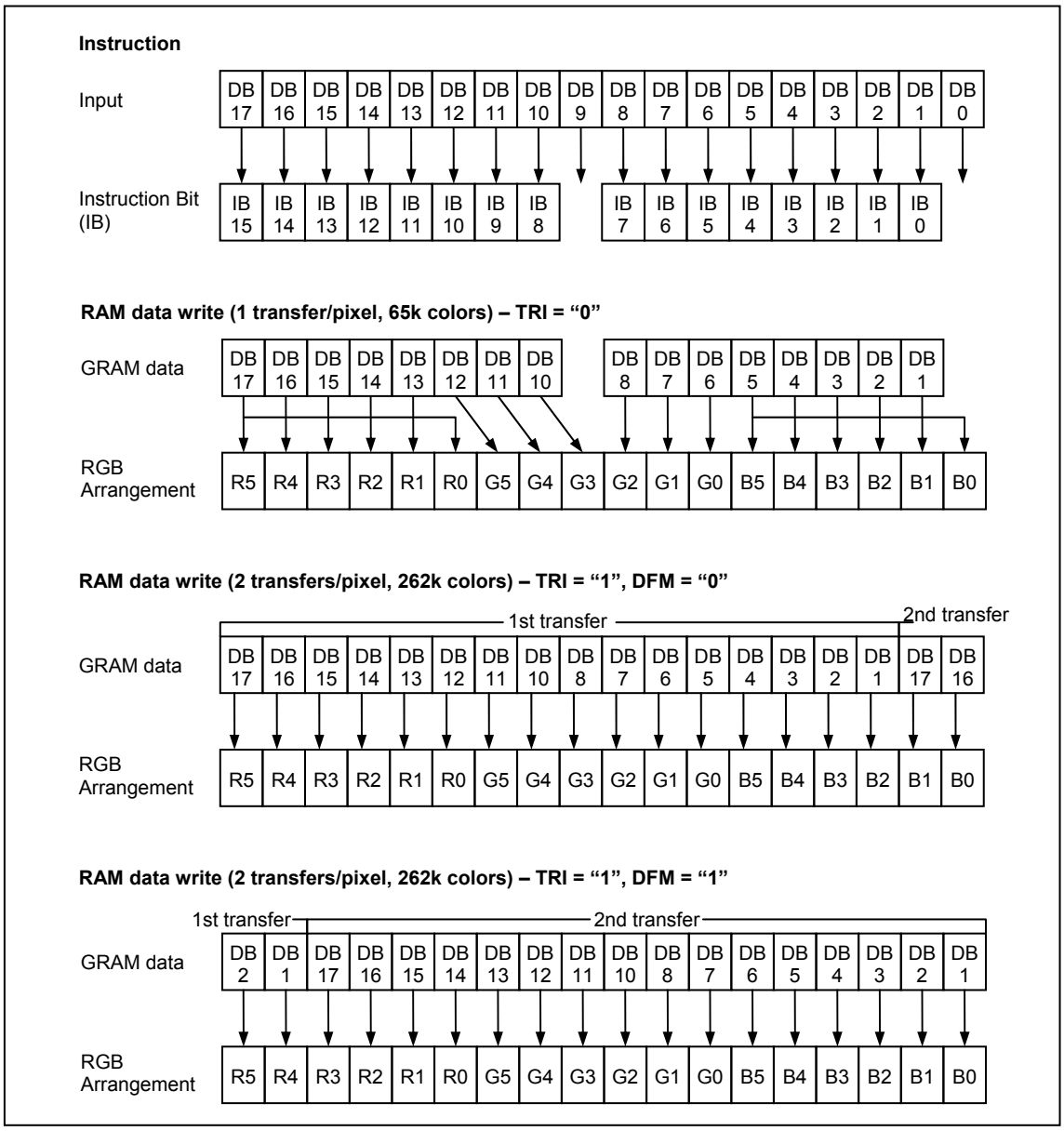


Figure 21 Data format for 16-bit interface

Data Transfer Synchronous in 16-bit Bus Interface operation

The LG4525B supports a data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 2/16 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

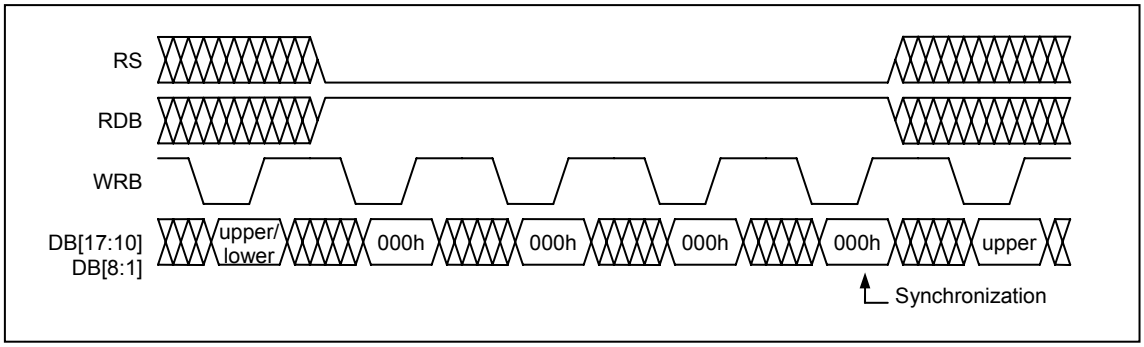


Figure 22 16-bit Data Transfer Synchronization

80-system 9-bit Bus Interface 1

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into the upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either the VDD3 or GND level. When writing to the index register, the upper byte (8 bits) must be written.

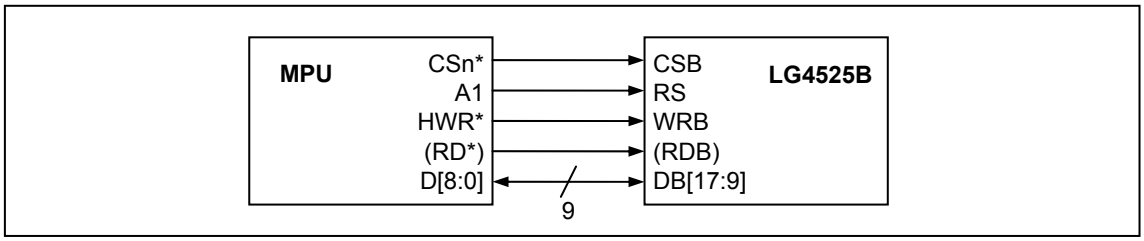


Figure 23 9-bit Interface

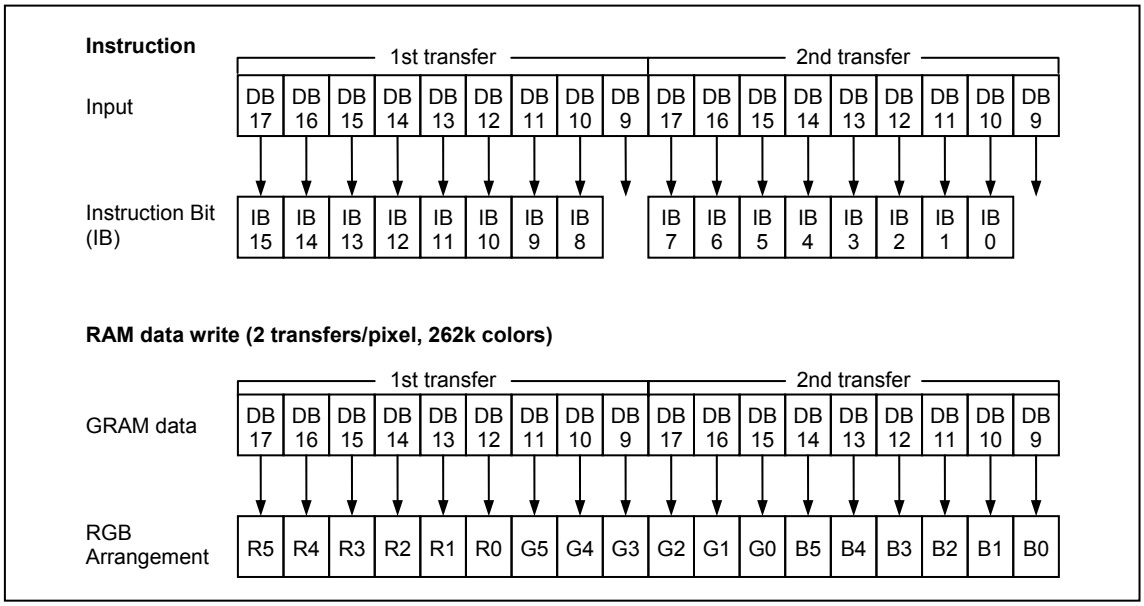


Figure 24 9-bit Interface Data Format

80-system 9-bit Bus Interface 2

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first (the MSB is not used). The RAM write data is also divided into the upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either the VDD3 or GND level. When writing to the index register, the upper byte (8 bits) must be written.

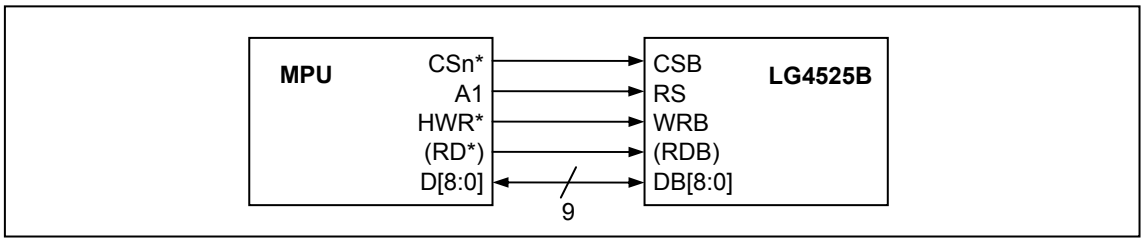


Figure 25 9-bit Interface

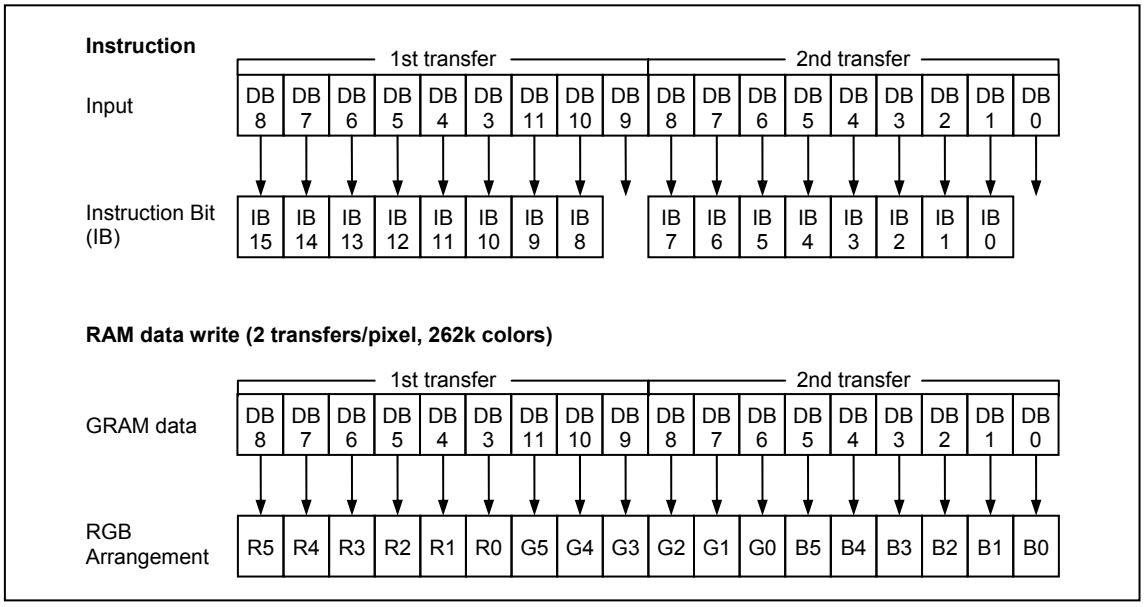


Figure 26 9-bit Interface Data Format

Data Transfer Synchronous in 9-bit Bus Interface operation

The LG4525B supports a data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 9 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

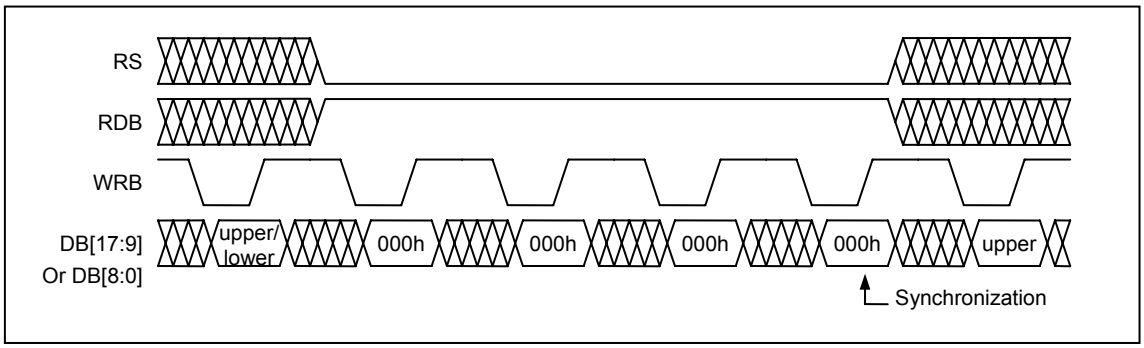


Figure 27 9-bit Data Transfer Synchronization

80-system 8-bit Bus Interface 1

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either the VDD3 or GND level. When writing the index register, the upper byte (8 bits) must be written.

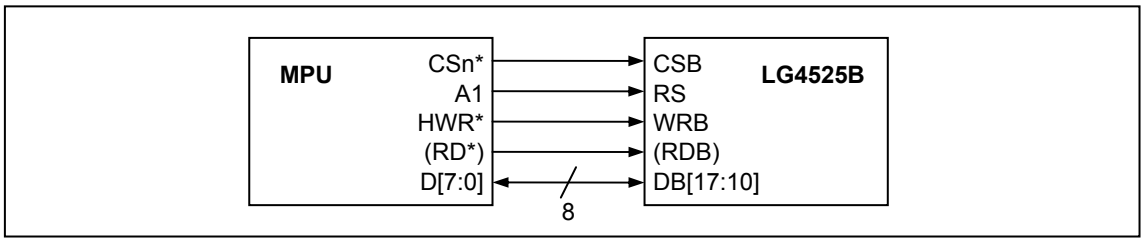


Figure 28 8-bit Interface

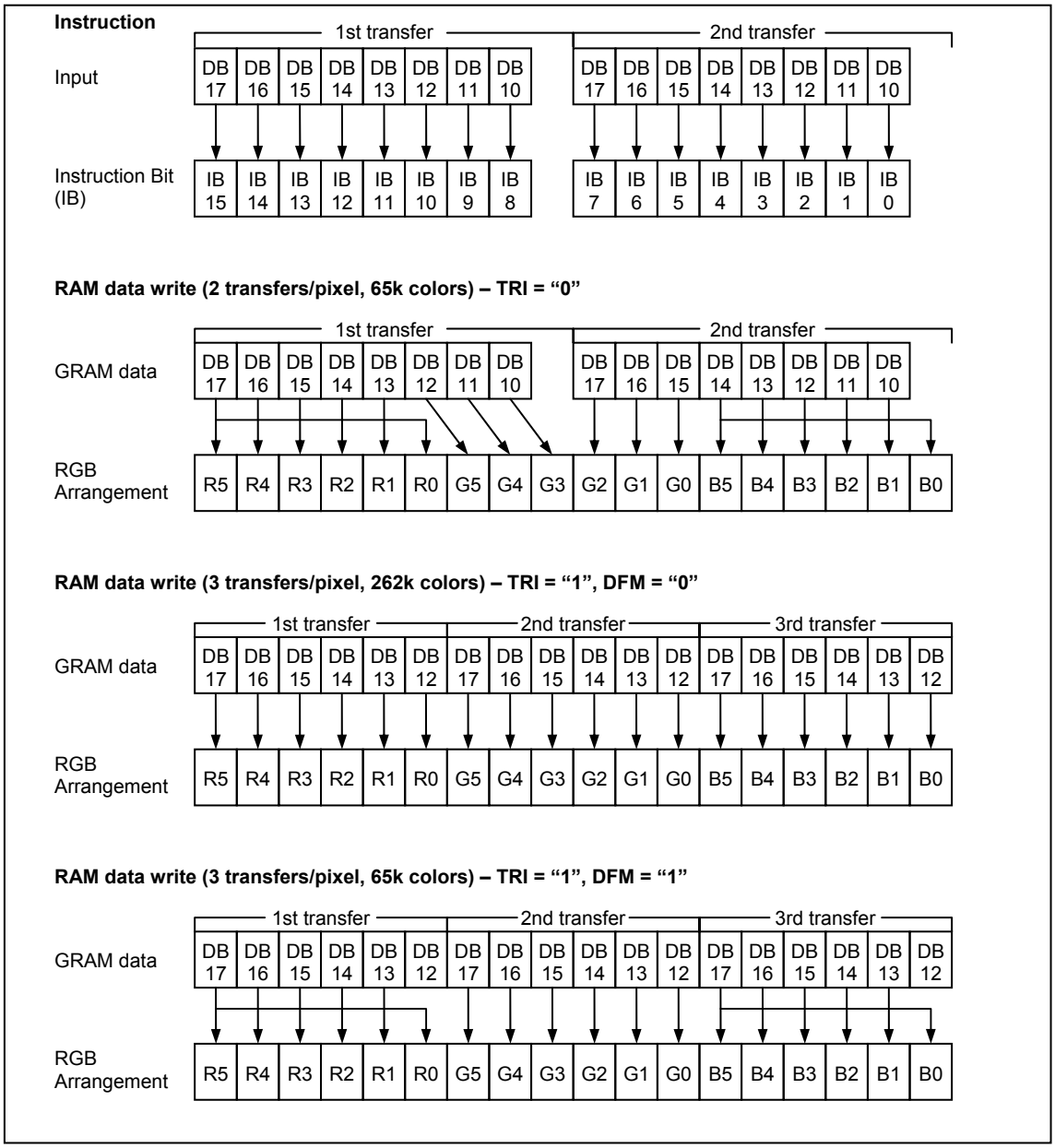


Figure 29 8-bit Interface Data Format

80-system 8-bit Bus Interface 2

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either the VDD3 or GND level. When writing the index register, the upper byte (8 bits) must be written.

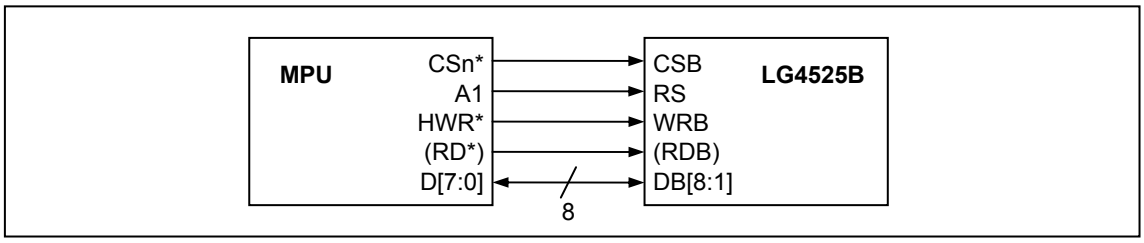


Figure 30 8-bit Interface

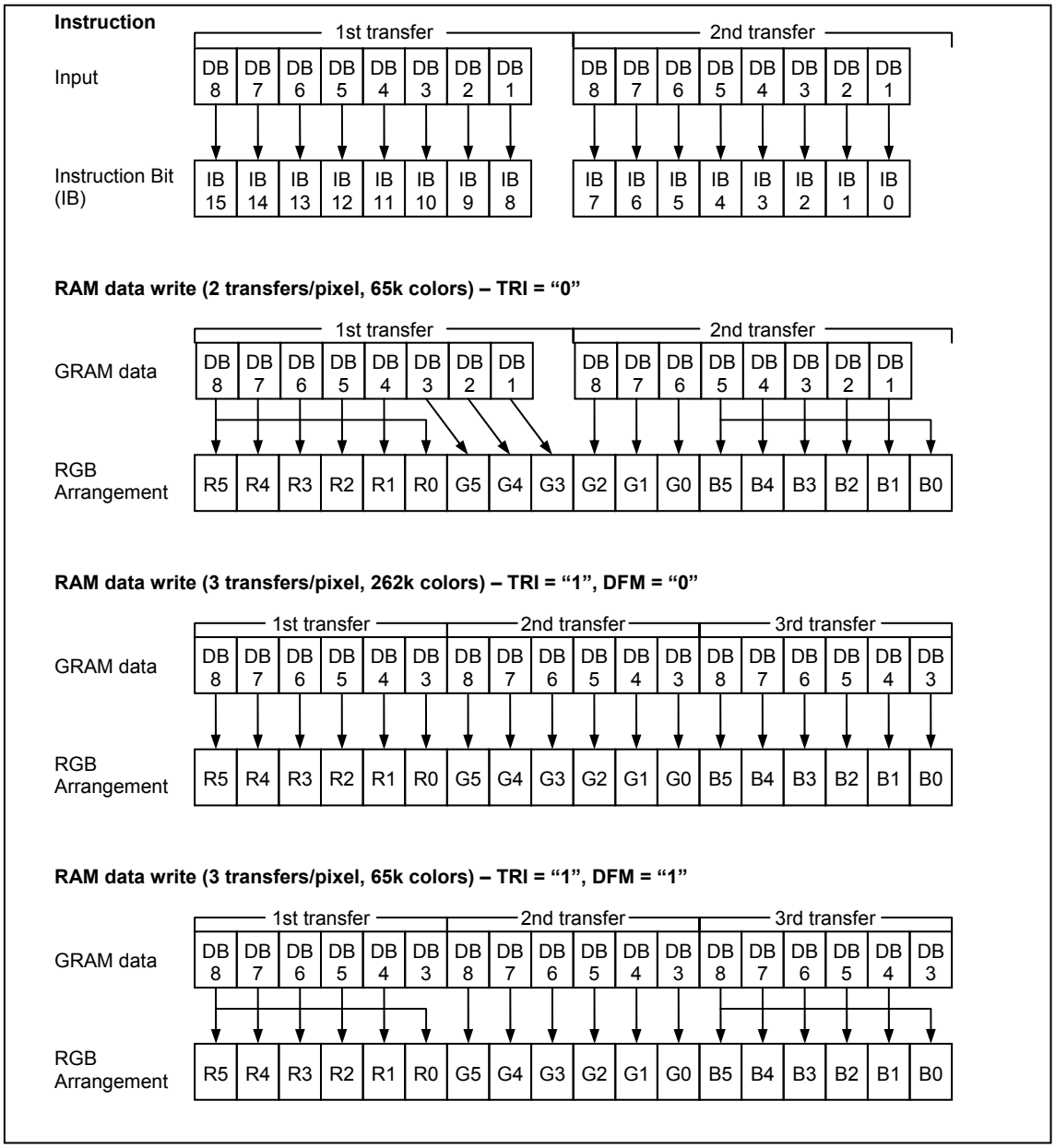


Figure 31 8-bit Interface Data Format

Data Transfer Synchronous in 8-bit Bus Interface operation

The LG4525B supports a data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 8 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

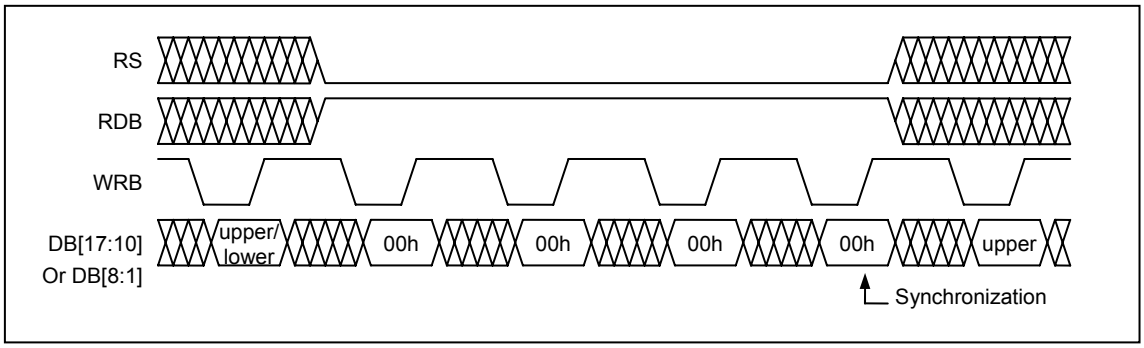


Figure 32 8-bit Data Transfer Synchronization

Serial Interface

The serial interface is selected by setting the IM2 pin to the VDD3 levels. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either VDD3 or GND level.

The LG4525B recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The LG4525B is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LG4525B are compared and both 6-bit data match, and then the LG4525B starts taking in data. The least significant bit of the device identification code is set with the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the LG4525B because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, an index register write operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). The LG4525B receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The LG4525B writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the LG4525B starts transferring or receiving data in units of bytes. The LG4525B executes data transfer from the MSB. The LG4525B's instruction takes 16-bit format and they are executed inside after it is transferred in two bytes (16 bits: DB15-0) from the MSB (The LG4525B expands RAM write data into 18-bit format when writing them to the internal GRAM). The first byte received by the LG4525B following the start byte is always the upper eight bits of instruction and the second byte is the lower 8 bits of instruction.

In case of reading data from the GRAM, the LG4525B does not transfer valid data until first five bytes of data are read from the GRAM following the start byte. The LG4525B starts sending valid data as it reads the sixth and subsequent byte data.

Table 65 Start byte format

Transferred bits	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

Note: ID bit is selected by setting the IM0/ID pin.

Table 66

RS	**R/W**	**Function**
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

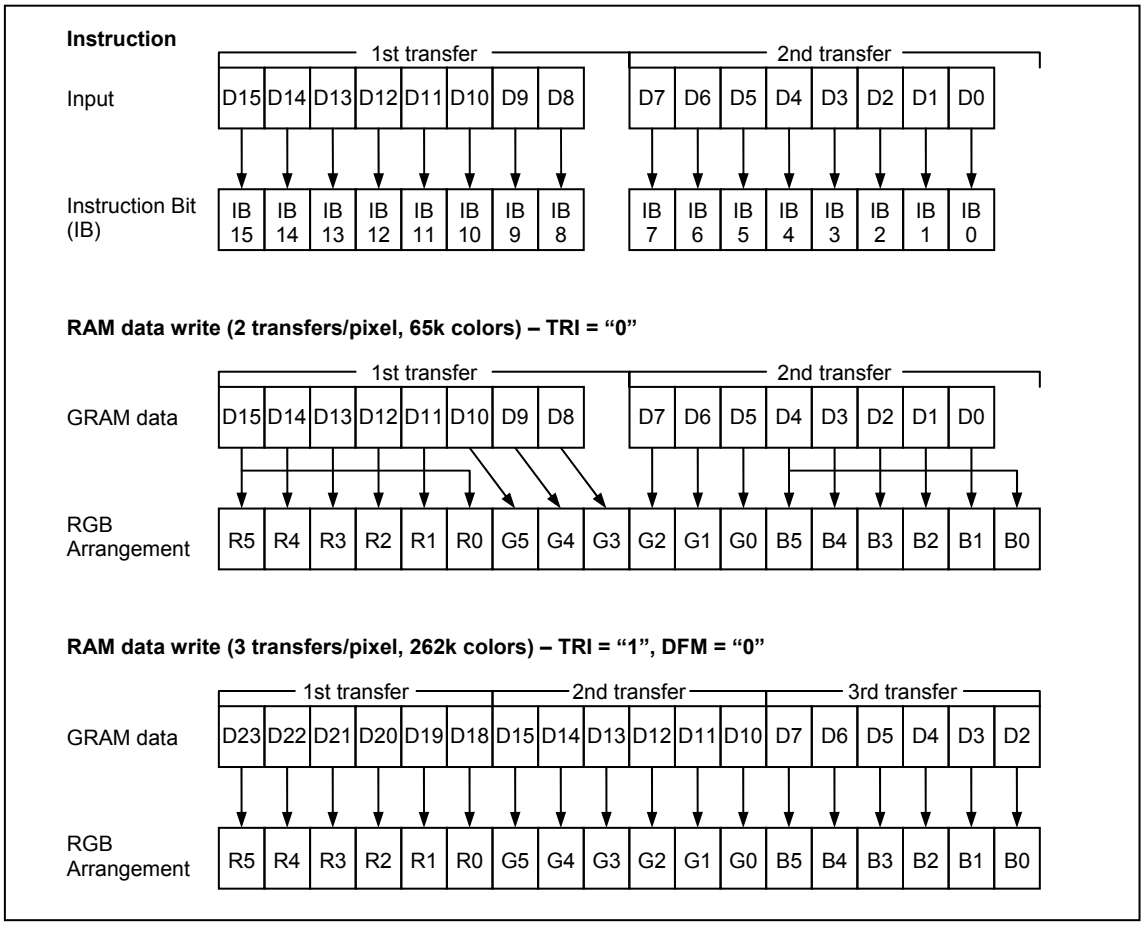


Figure 33 Data format for SPI

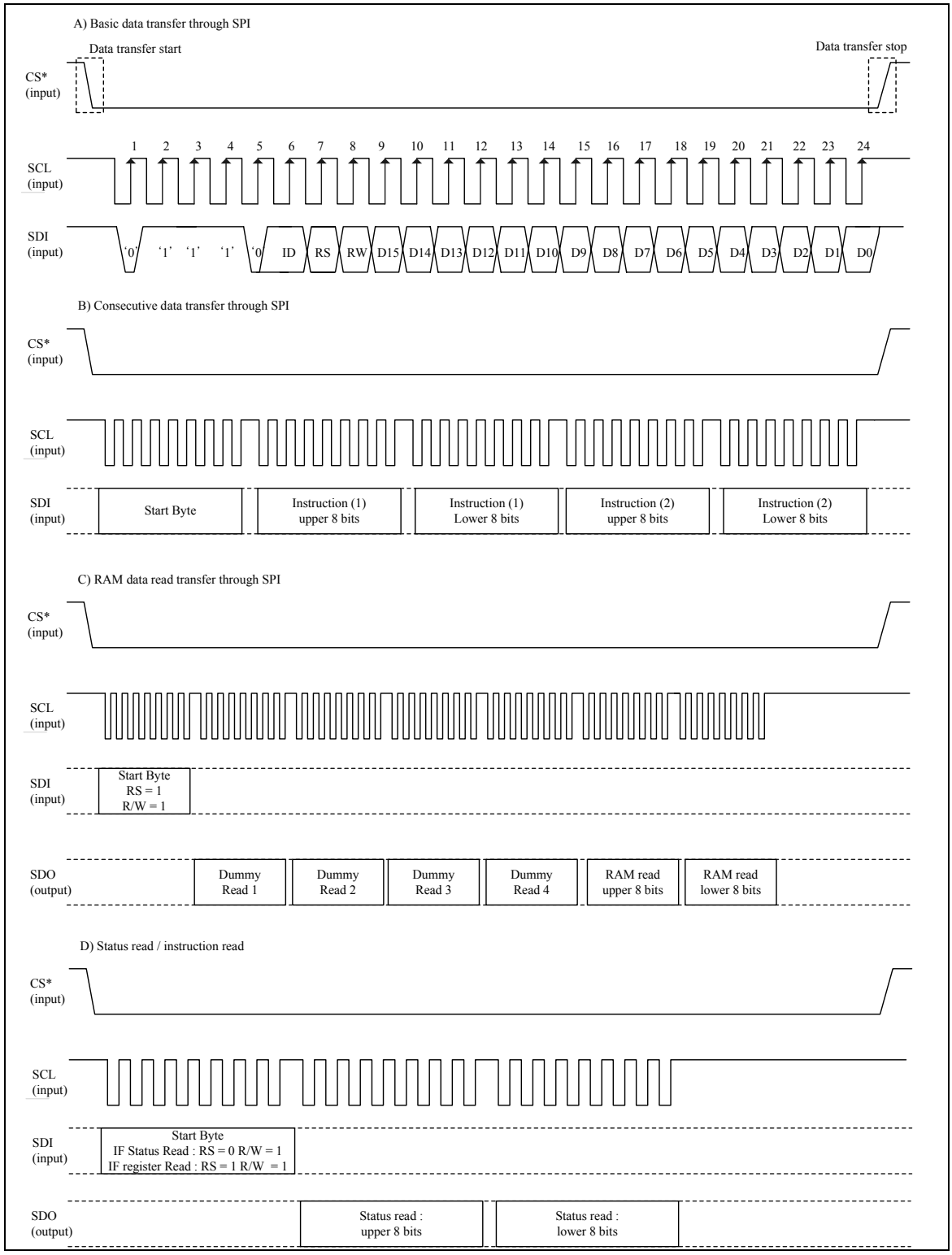


Figure 34 Data Transfer in Serial interface

VSYNC Interface

The LG4525B supports VSYNC interface, enabling the LG4525B to display a moving picture with minimum modifications to the existing system, using system interface and the frame synchronization signal (VSYNC).

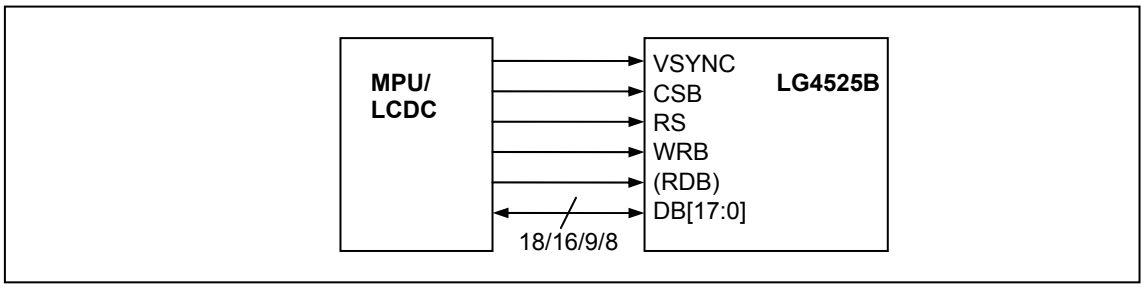


Figure 35 VSYNC Interface

The VSYNC interface is selected by setting DM[1:0] = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at a speed faster to a certain degree than the internal display operation speed, it becomes possible to rewrite data without flickering the moving picture on display and enables the LG4525B to display a moving picture using a system interface.

The LG4525B performs the display operation with the internal clock signal generated from the internal oscillator and the VSYNC signal in this mode. In VSYNC mode, the data displayed on the screen are written to the internal RAM in order to transfer only the data to be written over the moving picture RAM area and thereby minimize the total data transfer required for moving picture display.

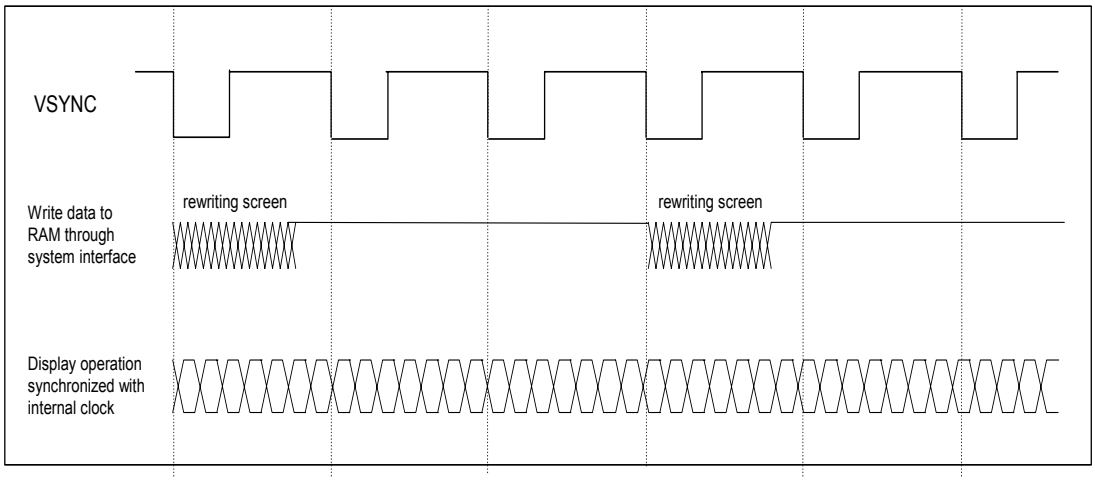


Figure 36 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum speed of writing data to the internal RAM via the system interface and the minimum internal clock frequency, which are calculated from the following formulae.

Internal clock frequency (fosc) [Hz]
= FrameFrequency × (DisplayLines (NL) + FrontPorch (FP) + BackPorch (BP)) × 60 clocks × variance

$$RAMWriteSpeed > \frac{176 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 60\ clocks \times \frac{1}{fosc}}$$

Note: When the RAM write operation does not start on the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum RAM writing speed and internal clock frequency in VSYNC interface mode is as follows.

[Example]

Display size	176 RGB × 220 lines
Lines	220 lines
Back/front porch	14/2 lines (BP = 1110/FP = 0010)
Frame frequency	70 Hz

Internal clock frequency (fosc)
= 70 Hz × (220 + 2 + 14) lines × 44 Clocks × 1.1 / 0.9 = 888 kHz

When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±10% for variances and ensures to complete the display operation within one VSYNC cycle.

In this example, variances attributed to the fabrication process of LSI and room temperature are counted in. Other possible causes of variances, such as differences in external resistors or voltage changes are not in consideration. It is necessary to allow for an enough margin if these factors must be incorporated.

Minimum speed for RAM writing
176 × 220 / {((14 + 220 - 2) lines × 44 clock) /0.89 MHz} = 3.376MHz

The above theoretical value is calculated on the premise that the LG4525B starts writing data to the internal RAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line where display operation is performed and the RAM line address where data write operation is performed.

The RAM write speed of 3.376MHz or more on the falling edge of VSYNC will guarantee the completion of RAM write operation before the LG4525B starts displaying the RAM data on the screen, enabling rewriting the entire screen without flicker.

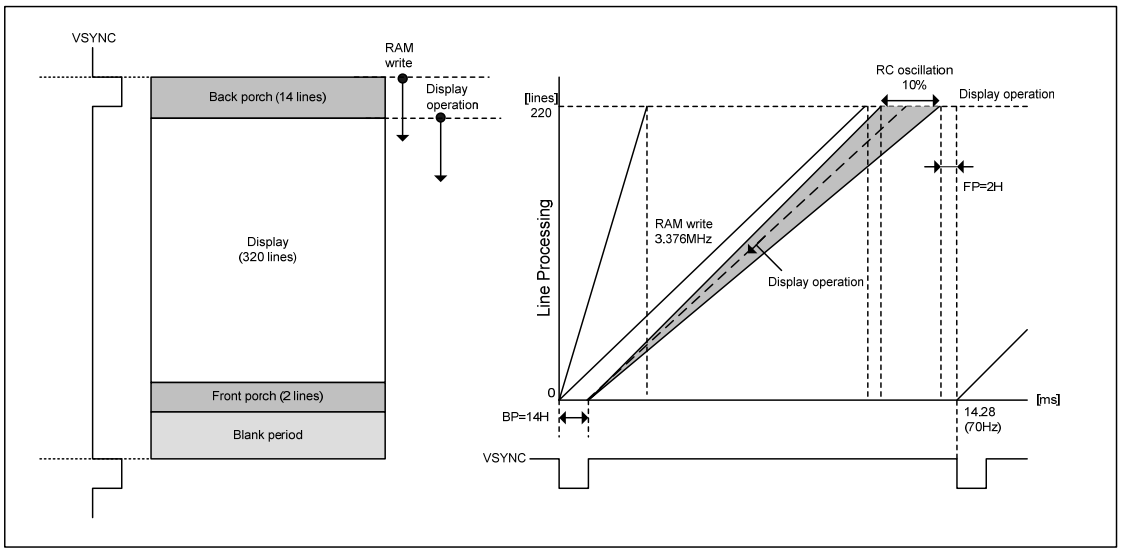


Figure 37 Write/Display Operation Timing via VSYNC Interface

Notes in using the VSYNC interface

1. The above example of calculation gives a theoretical value. In the actual setting, other possible causes of variances not counted in the above example such as differences in internal oscillators should also be taken into consideration. It is strongly recommended to allow for an enough margin in setting a RAM writing speed.

2. The above example of calculation gives a minimum value in case of rewriting the entire screen. If the moving picture display area is smaller than that, the range for setting a minimum RAM writing speed can have extra margins.

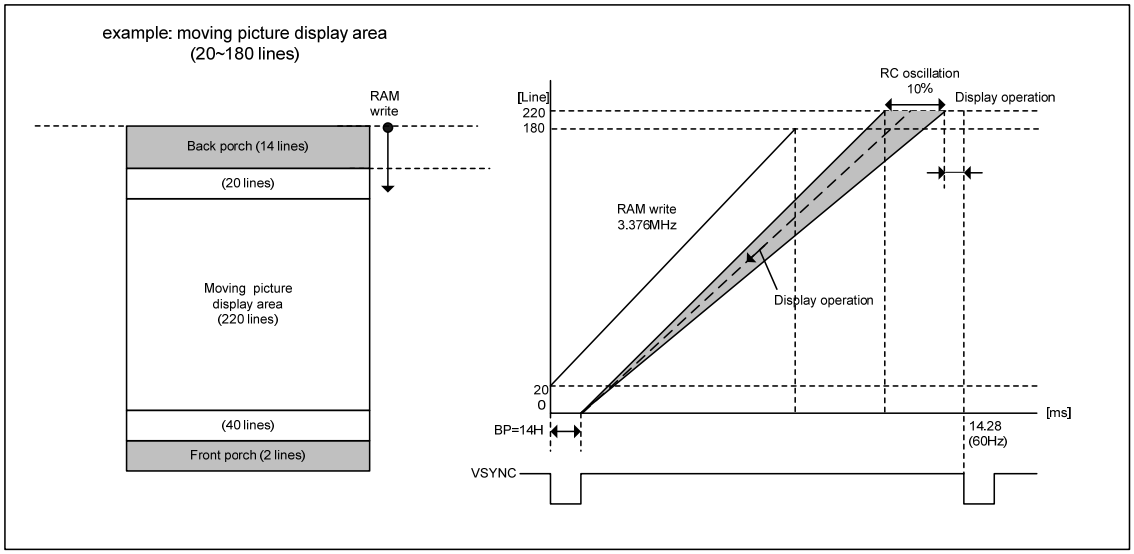


Figure 38 RAM write margin

3. After drawing 1 frame, a front porch period continues until the next input of VSYNC is detected.

4. When switching from the internal clock operation mode (DM1-0 = “00”) to the VSYNC interface mode, or the other way around, it is enabled from the next VSYNC cycle, i.e. after completing the display of the frame, which the LG4525B was internally processing when switching the modes.

5. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

6. In VSYNC interface mode, set the AM bit to “0” to transfer display data in the method mentioned above.

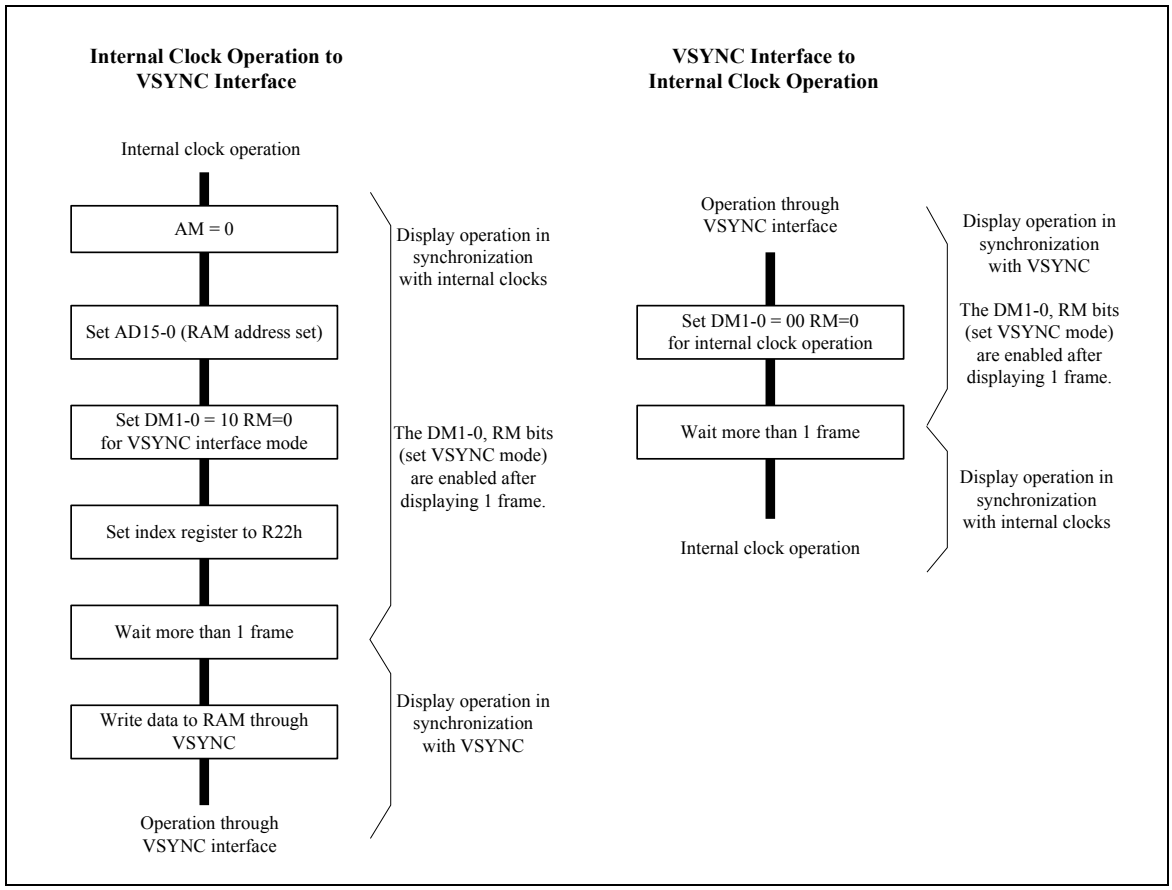


Figure 39 Sequences to Switch between VSYNC and Internal Clock Operation Modes

External Display Interface

The following RGB interfaces are available with the LG4525B. The interface operation is set with the RIM[1:0] bits. The RGB interface is used for RAM access.

Table 67

RIM[1:0]	RGB Interface	DB Pin
00	18-bit RGB interface	DB[17:0]
01	16-bit RGB interface	DB[17:10], DB[8:1]
10	6-bit RGB interface	DB[17:12]
11	Setting disabled	-

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface in combination with the window address function enables minimizing data transfer by rewriting data in high-speed with low power consumption only within the RAM area where data must be updated. In RGB interface operation, it is necessary to set back and front porch periods before and after the display period, respectively.

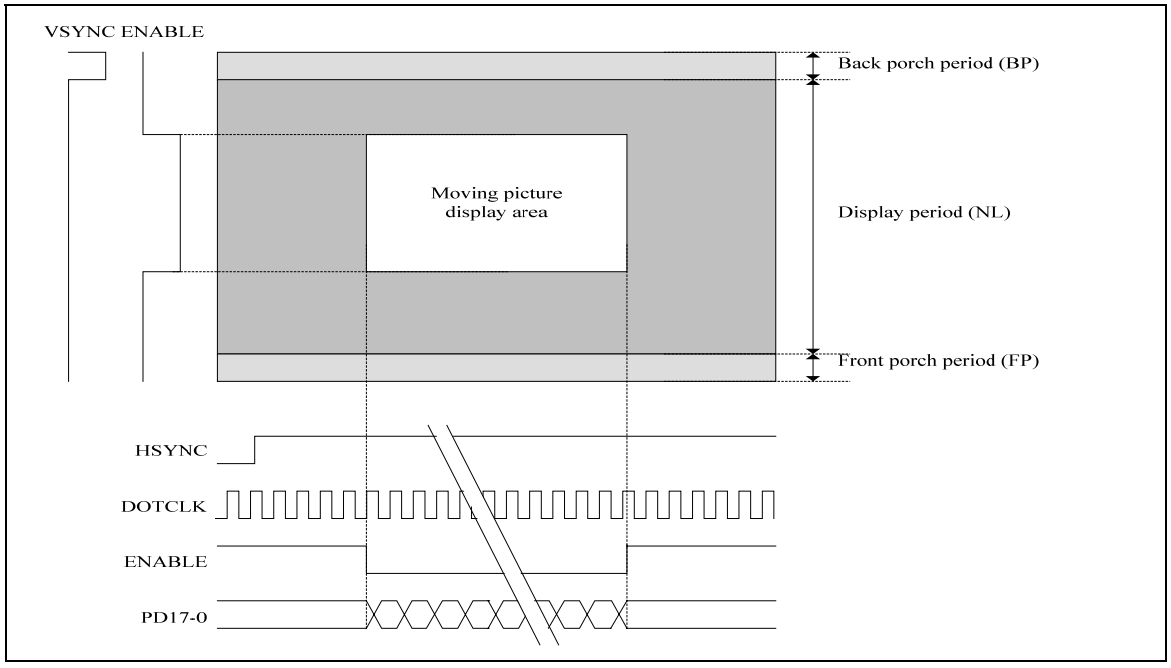


Figure 40 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals are changeable by setting the DPL, EPL, HSPL, and VSPL bits, respectively according to the system configuration.

RGB Interface Timing

The timing relationships of signals in RGB interface operation area as follows.

16-18-bit RGB Interface Timing

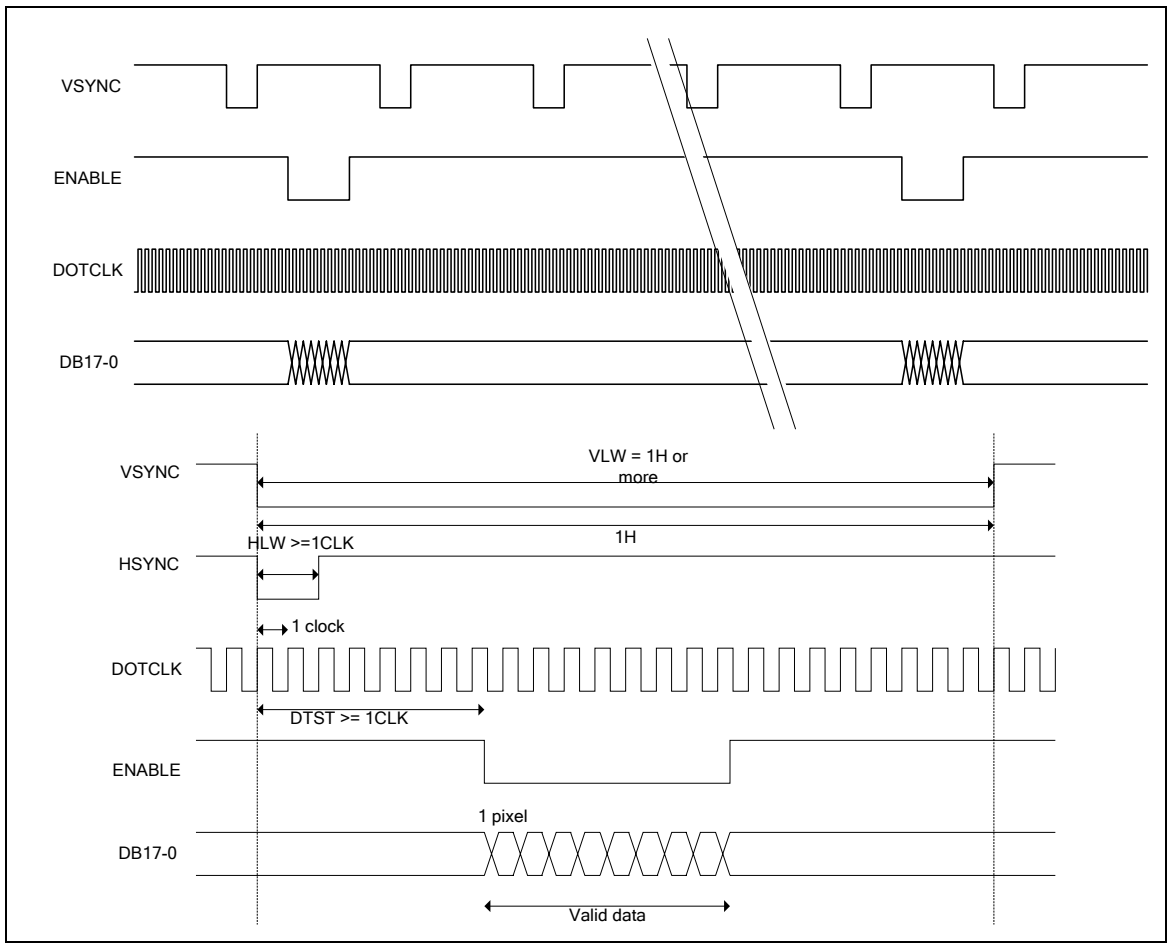


Figure 41

Notes: 1. VLW : VSYNC Low period
HLW : HSYNC Low period
DTST : data transfer setup time

6-bit RGB Interface Timing

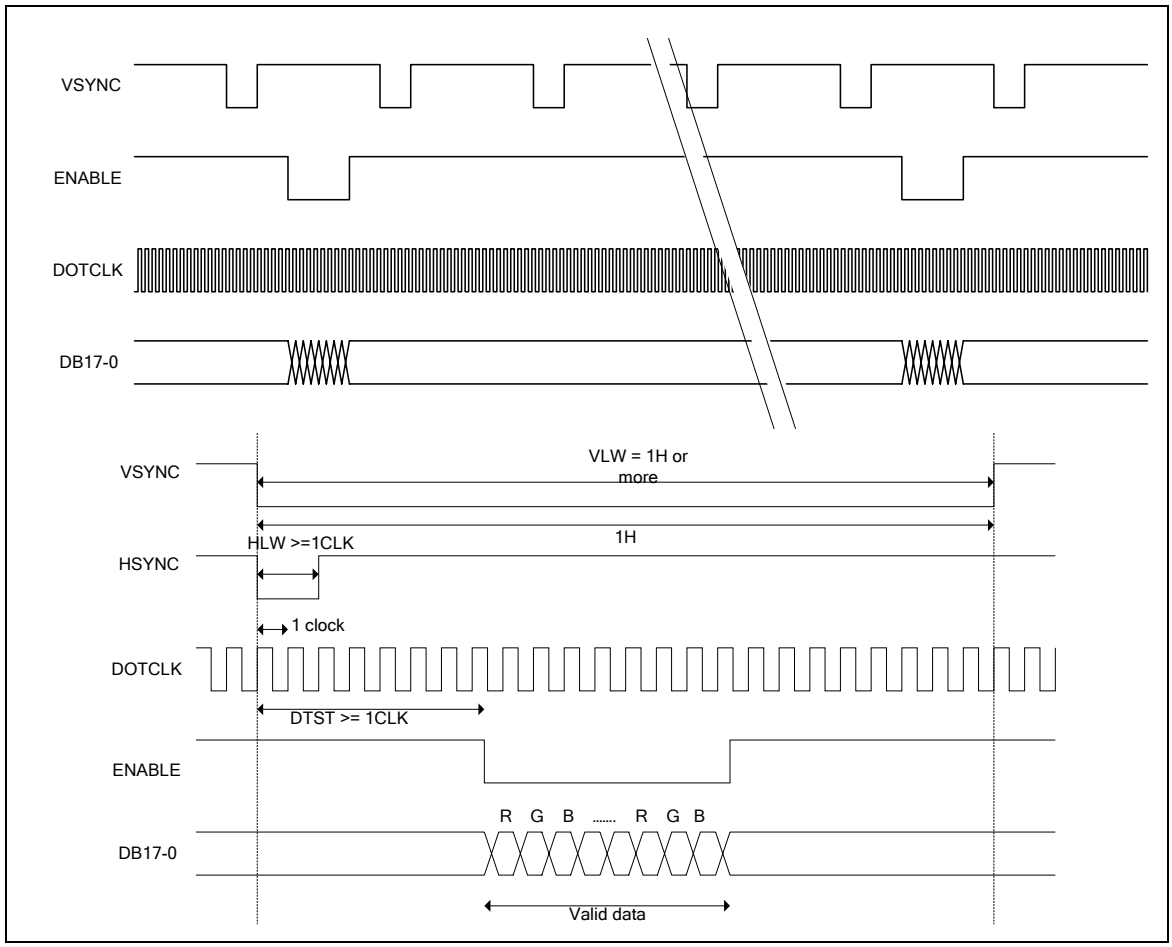


Figure 42

Notes: 1. VLW : VSYNC Low period
HLW : HSYNC Low period
DTST : Data transfer setup time
2. In 6-bit RGB interface operation, set the cycles of VSYNC, HSYNC, ENABLE, DOTCLK so that one pixel is transferred in units of three DOTCLKs via DB17-12 (DB5-0).

Moving Picture Display with the RGB Interface

The LG4525B supports RGB interfaces for displaying a moving picture and RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function can minimize data transfer by specifying a moving picture RAM area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. The data transfer is limited to a moving picture RAM area.
4. The reduction in data transfer contributes to the reduction in power consumption by the entire system
5. The combined use with system interface allows updating data in the still picture area, such as icons, while displaying a moving picture via RGB interface

RAM access via system interface in RGB interface operation

The LG4525B allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the RAM via system interface, set ENABLE "High" to stop writing data via RGB interface. Then set RM = "0" to enable RAM access via system interface. When reverting to the RGB interface operation, wait for a time for a read/write bus cycle. Then, set RM = "1" and the index register to R22h to start accessing RAM via RGB interface. A conflict between RAM accesses via two different interfaces will not guarantee write operation.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

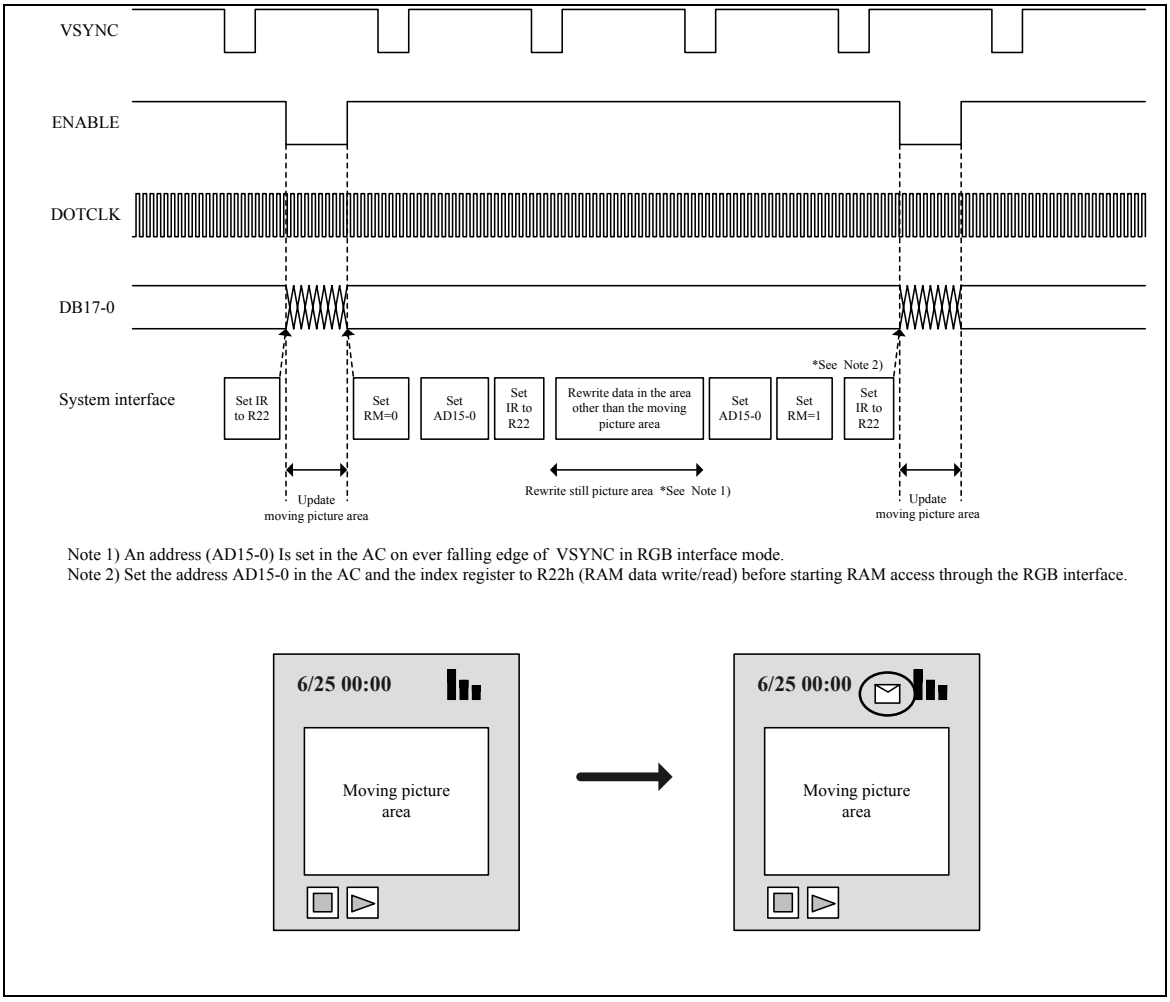


Figure 43 Updating the Still Picture Area while Displaying Moving Picture

6-bit RGB Interface

The 6-bit RGB interface is selected by setting RIM[1:0] = 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus according to data enable signal (ENABLE). Unused pins DB[11:0] must be fixed at either VDD3 or GND level.

The instructions are set only via system interface.

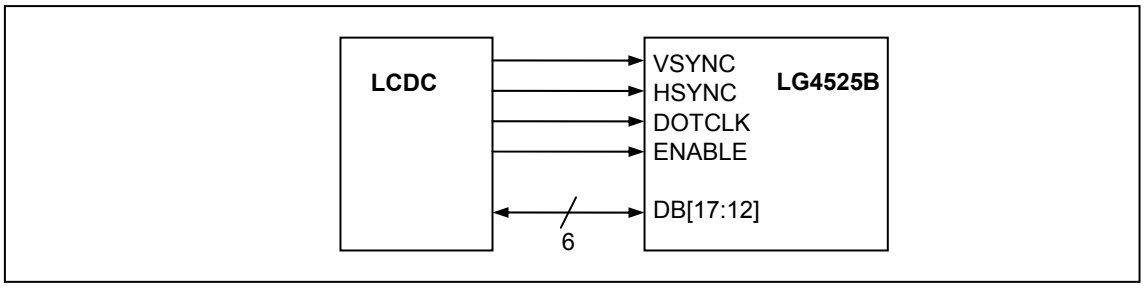


Figure 44 6-bit RGB interface

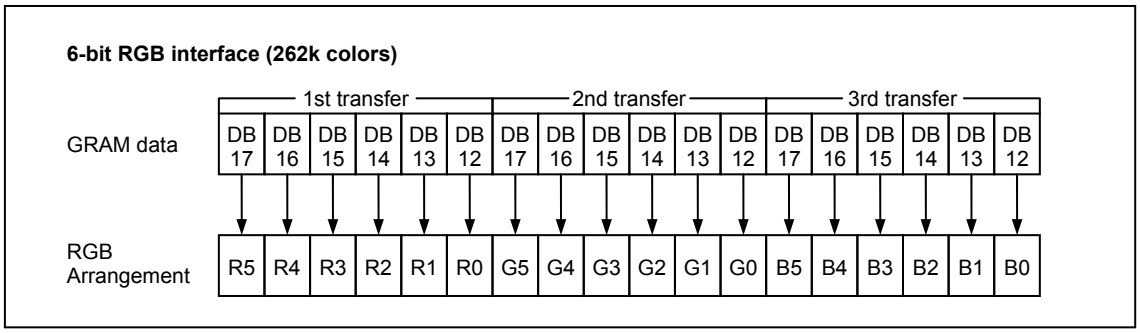


Figure 45 Data format for 6-bit interface

Data Transfer Synchronization in 6-bit Bus Interface operation

The LG4525B has data transfer counters to count the first, second, and third 6-bit data transfers in 6-bit RBG interface operation. The transfer counters are always reset to the first data transfer on the falling edge of VSYNC. If there is a mismatch in the number of data transfers, the counters are reset to the first data transfer at the start of each frame (on the falling edge of VSYNC) and data transfer can be restarted in correct order from the next frame. In case of displaying a moving picture, which requires consecutive data transfer, this function can minimize the effect from the data transfer mismatch and help recover the display system to a normal state.

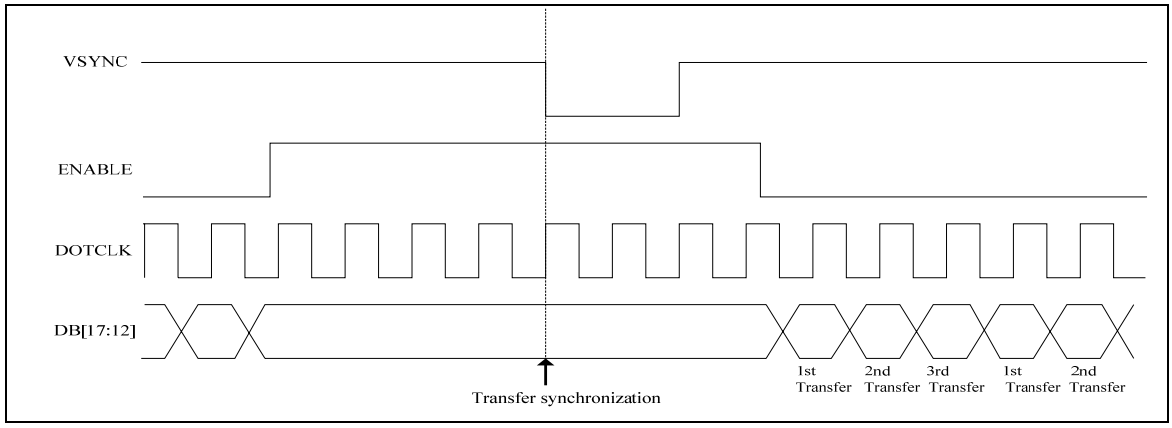


Figure 46 6-bit Transfer Synchronization

16-bit RGB Interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus according to data enable signal (ENABLE).

The instructions are set only via system interface.

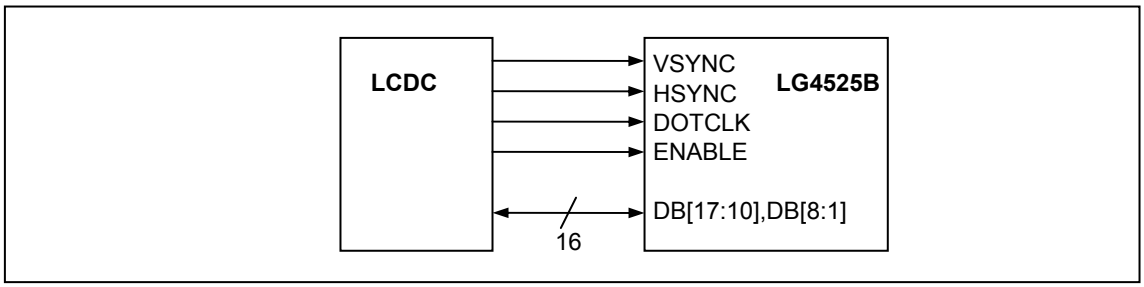


Figure 47 16-bit RGB interface

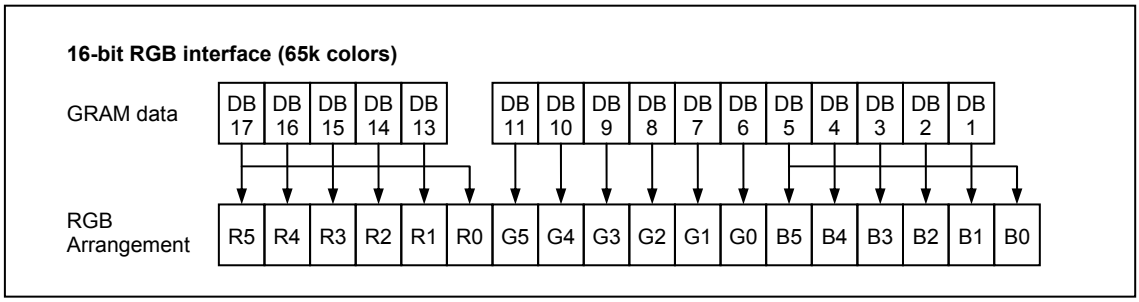


Figure 48 Data format for 16-bit interface

18-bit RGB Interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB17-0) according to data enable signal (ENABLE).

The instructions are set only via system interface.

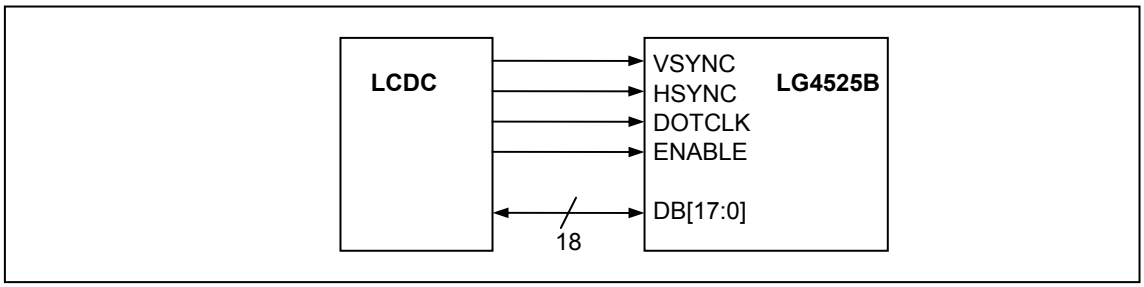


Figure 49 18-bit RGB interface

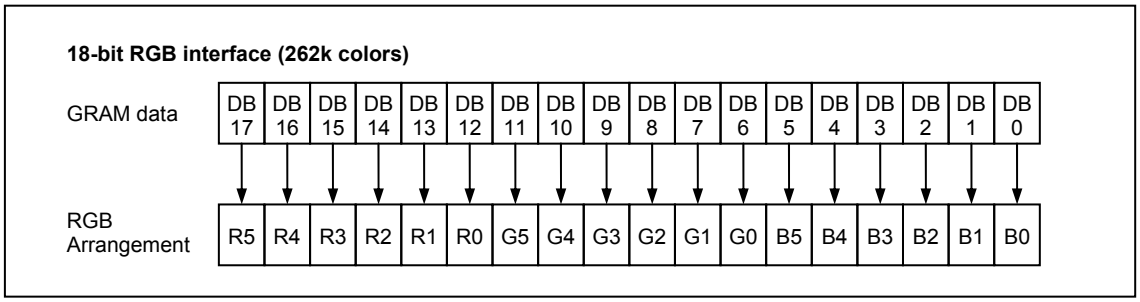


Figure 50 Data format for 18-bit interface

Notes on Using the External Display Interface

1. The following functions are not available in external display interface operation.

Table 68 Functions Not Available in External Display Interface operation

Function	External Display Interface	Internal Display Interface
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied throughout the display operation.

3. The reference clock for generating liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.

4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel.

5. In 6-bit RGB interface operation, each 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. Take this into consideration and make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE, and data transfer via DB17-12 so that data transfer is completed in units of pixels.

6. When switching between the internal operation mode and the external display interface operation, follow the sequences in Figure 46 RGB and Internal Clock Operation Mode switching sequences.

7. In RGB interface operation, a front porch period continues until the next VSYNC input is detected after the end of each frame period.

8. In RGB interface operation, RAM address AD15-0 is set in the address counter every frame on the falling edge of VSYNC.

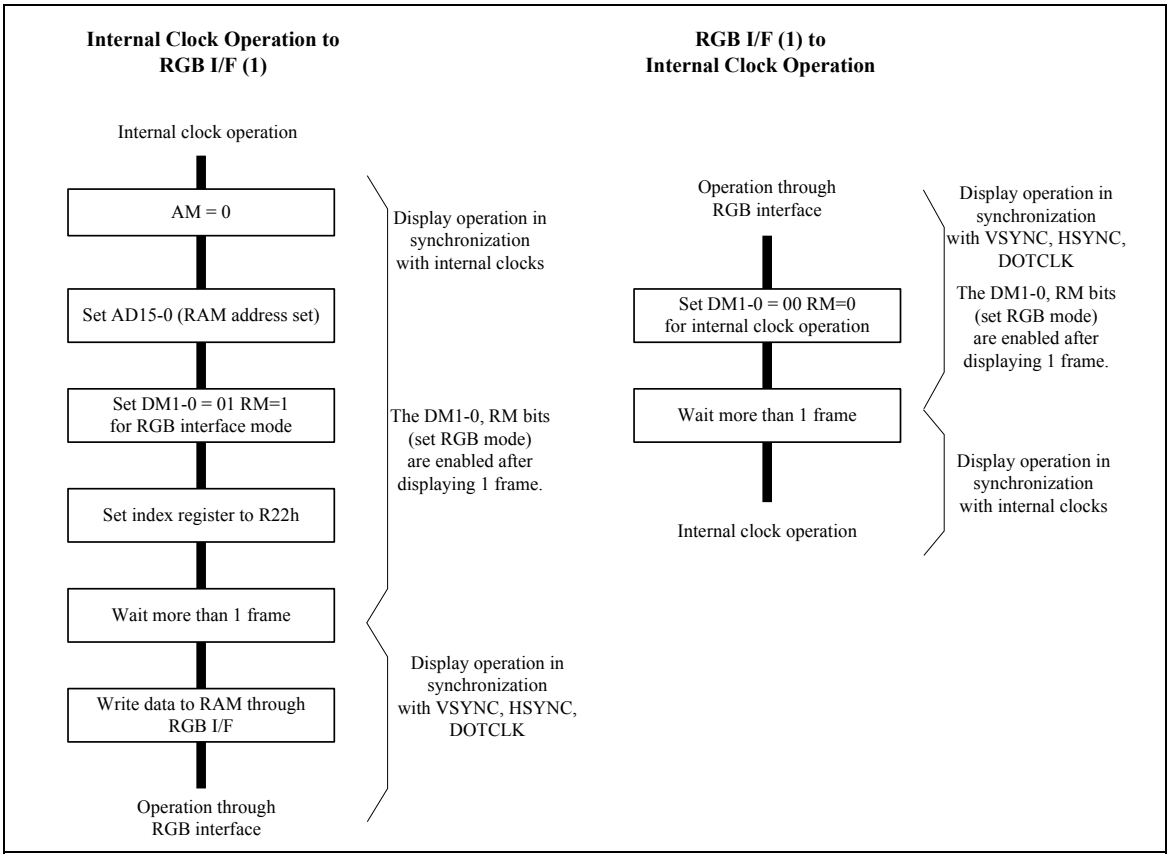


Figure 51 RGB and Internal Clock Operation Mode switching sequences

Resizing function

The LG4525B supports resizing function (x 1/2, x 1/4), which is executed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit representing the contraction factor (x1/2 or x1/4) of the image. This function enables the LG4525B to write the resized image data directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system just to transfer data as usual even when resizing of the image is required. This feature makes a resized image easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The LG4525B processes the contraction of an image simply by selecting pixels. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.

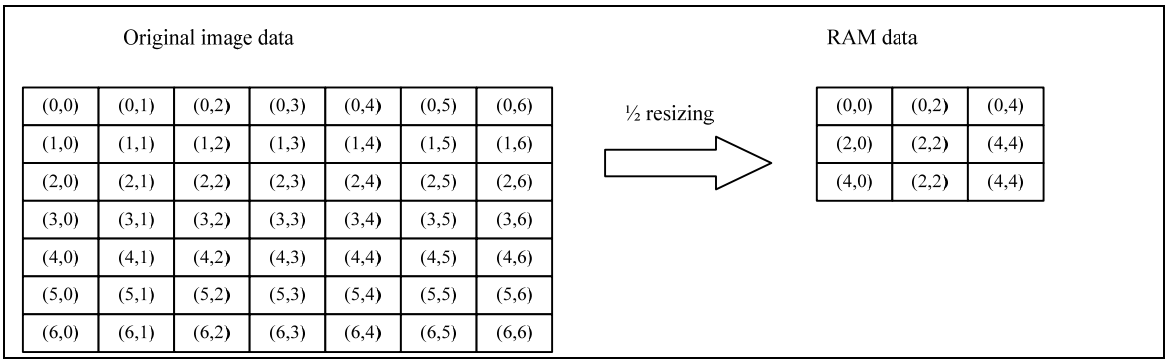


Figure 52 Data transfer in resizing

Table 69

Origianl image size (X x Y)	Resized image Size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
352x288(CIF)	176x144	88x72
320x240(QVGA)	160x120	80x60
176x144(QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44

Resizing setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting the RAM area using the window address function, the window address area must be just the size of the resized picture. If resizing creates surplus pixels, which are calculated from the following equations, set them with the RCV, RCH bits before writing data to the internal RAM.

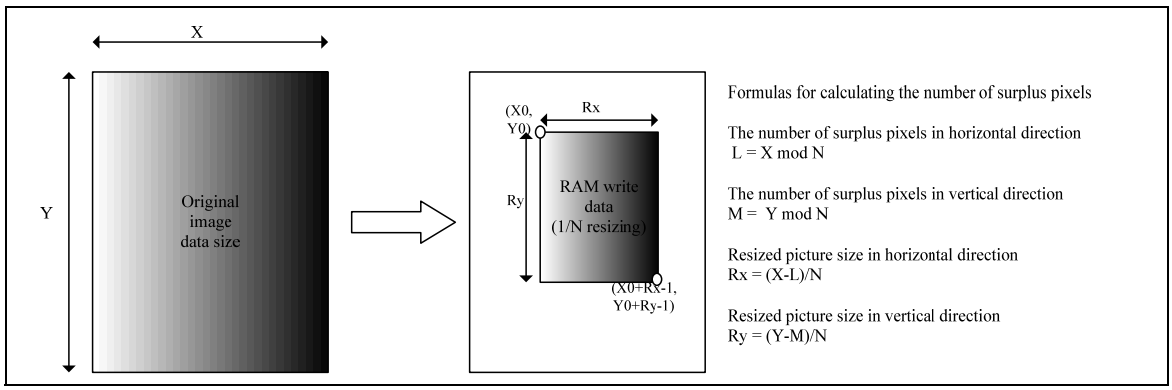


Figure 53 Resizing Setting, surplus pixel calculation

Table 70

Image (before resizing)		
Number of data in horizontal direction	X	
Number of data in vertical direction	Y	
Resizing ratio	1/N	

Resizing setting in the LG4525B		
Resizing setting	RSZ	N-1
Number of data in horizontal direction	RCH	L
Number of data in vertical direction	RCV	M
RAM writing start address	AD	(X0,Y0)
RAM window address	HAS	X0
	HEA	X0+Rx-1
	VSA	Y0
	VEA	Y0+Ry-1

Notes to Resizing function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are remainder pixels. Otherwise (if RSZ = 2'h0), set RCH = RCV = 2'h0.

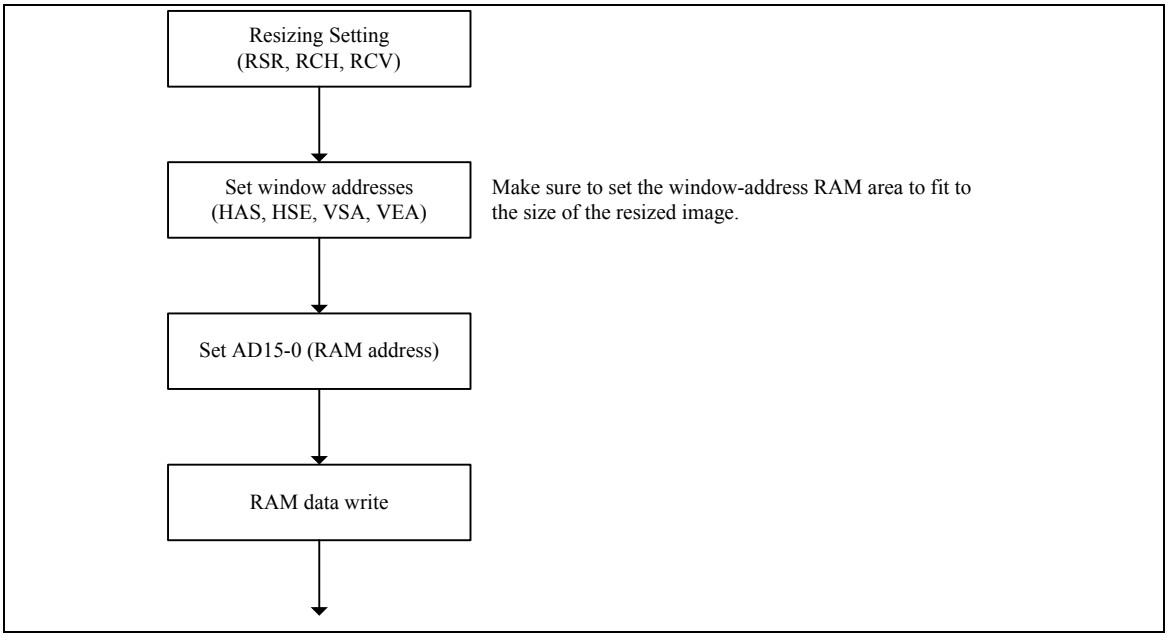


Figure 54 RAM write operation sequence in resizing

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA7-0, end: VEA7-0 bits). The AM and I/D bits set the transition direction of the RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the LG4525B to write data including image data consecutively without taking data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area setting range]
(Horizontal direction) 8'h00 ≤ HSA ≤ HEA ≤ 8'hAF
(Vertical direction) 8'h00 ≤ VSA ≤ VEA ≤ 8'hDB
[RAM Address setting range]
(RAM address) HSA ≤ AD7-0 ≤ HEA
VSA ≤ AD15-8 ≤ VEA

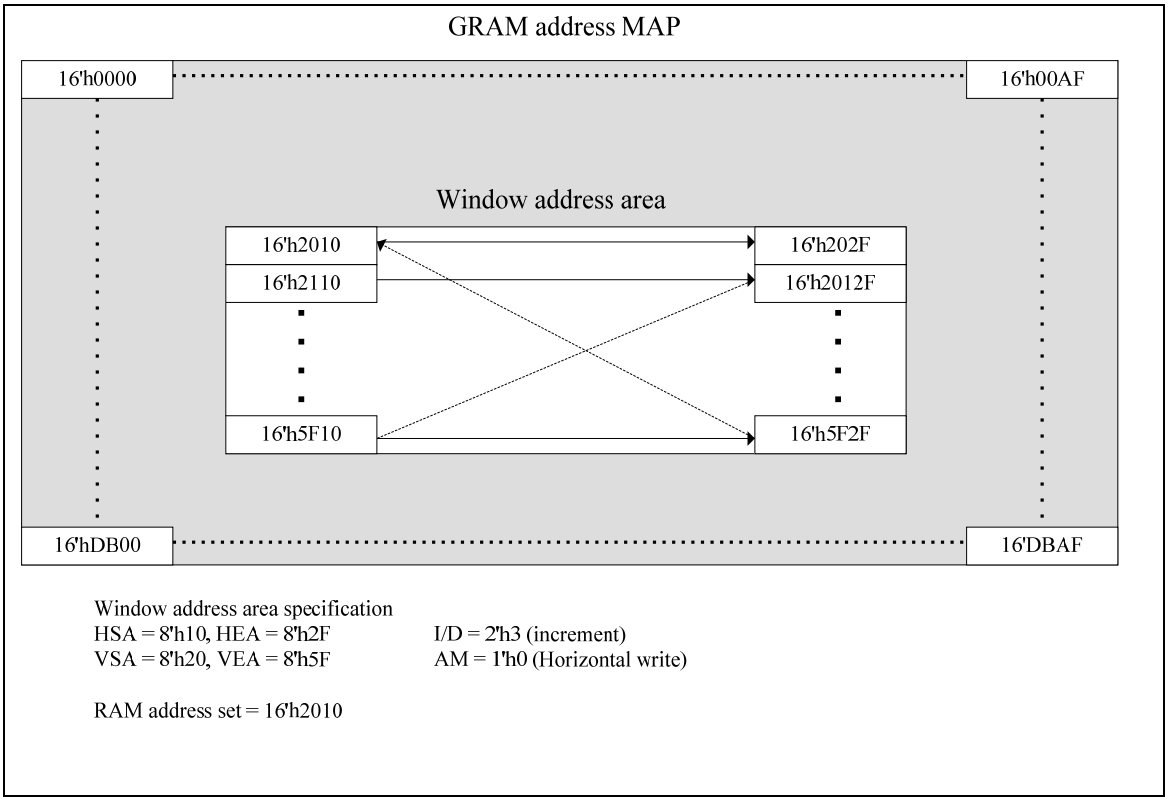


Figure 55 Automatic address update within a Window Address Area

EPROM Control

LG4525B has an embedded EPROM which is a 32-bit one-time programmable (OTP) IP from eMemory Technology Inc. (EO01X32KCV6).
EO01X32KCV6 is a CMOS, 1bit (1-bit) program OTP logic device. The main memory block is organized as 8-bits by 4 banks. See the data sheet of EO01X32KCV6.
The pins of the embedded EPROM can be controlled using the EPROM control 1 (R50h) register as shown below.

Table 71

EO01X32KCV6	Bit fields of register R40h
PTM = 0V/1.8V	PTM[1:0] = 00/11
POR = 0V/1.8V	POR = 0/1
VPP = 1.8V/7.2V	VPP = 0/1
PPROG = 0V/1.8V	PPROG = 0/1
PWE = 0V/1.8V	PWE = 0/1
PA[1:0] = 0V/1.8V	PA[1:0] = 0/1
PDIN[7:0] = 0V/1.8V	PDIN[7:0] = 0/1

The RA[1:0] of register R41h selects one of four EPROM bytes.
Accessing EPROM control registers, follow the timing requirements of read and program cycles.

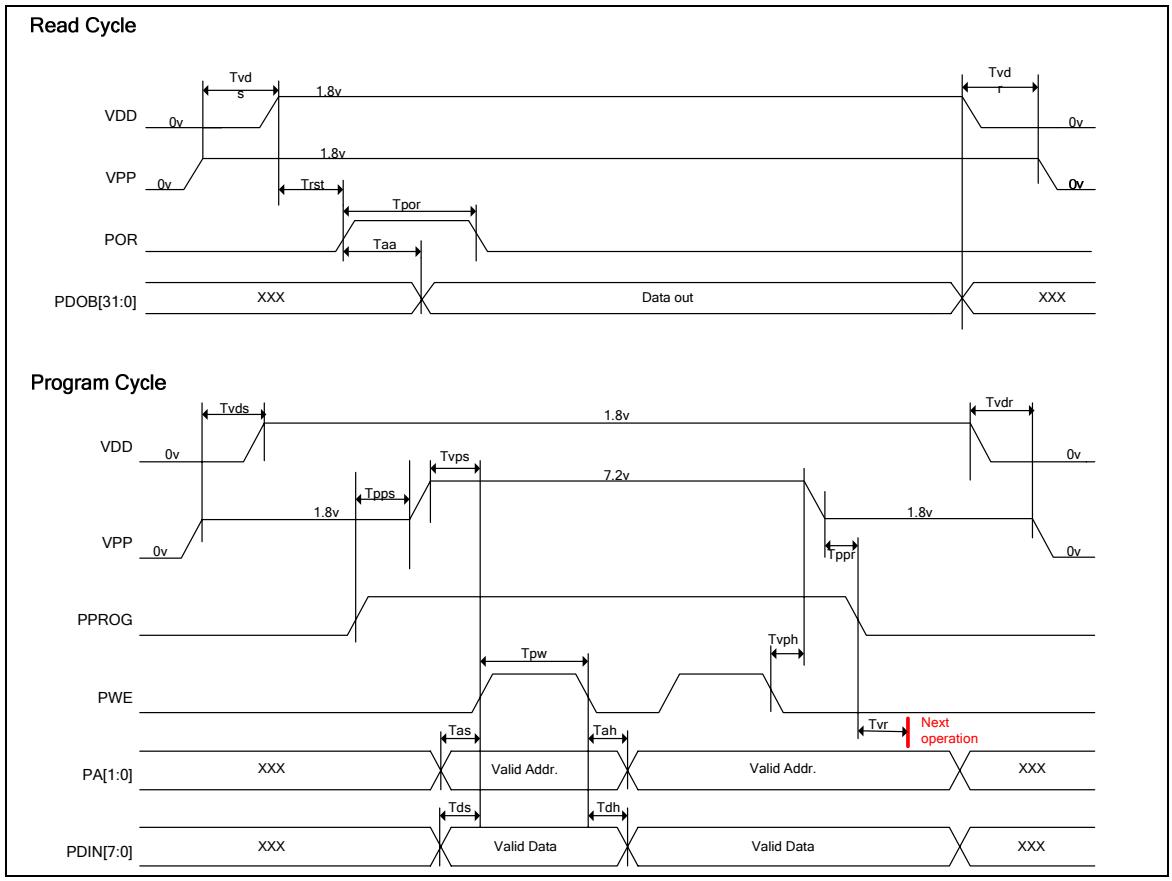


Figure 56 EPROM timings

Table 72

Parameter	Symbol	EO01X32KCV6		Unit
		Min	Max	
Risimg Time / Fallimg Time	T_r / T_f	-	1	ns
Data Access Time	T_{aa}	-	70	ns
Power-on Pulse Width Time	T_{por}	200	-	ns
Address / Data Setup Time	T_{as} / T_{ds}	4	-	ns
Address / Data Hold Time	T_{ah} / T_{dh}	9	-	ns
External VPP Setup Time	T_{vps}	0	-	ns
External VPP Hold Time	T_{vph}	0	-	ns
Program Recovery Time	T_{vr}	10	-	us
Program Pulse Width	T_{pw}	300	350	us
VDD Setup Time	T_{vds}	0	-	ms
VDD Recovery Time	T_{vdr}	0	-	ms
PPROG Setup Time	T_{pps}	10	-	ns
PPROG Recovery Time	T_{ppr}	10	-	ns
Power on Read Time	T_{rst}	20	-	ns

Notes
1. All electrical and timing parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.
2. All program signals that align together in the timing diagrams should be derived from the rising clock edge.
3. All timing measurements are from the 50% of the input to 50% of the output.
4. All input waveforms have rising time (t_r) and falling time (t_f) of 1ns from 10% to 90% of the input waveforms.
5. For capacitive loads greater than 1pF, access time will increase by 1ns per pF of additional loading.
6. Program time means one byte program time in user mode

Scan Mode Setting

The LG4525B allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the LG4525B and the LCD panel.

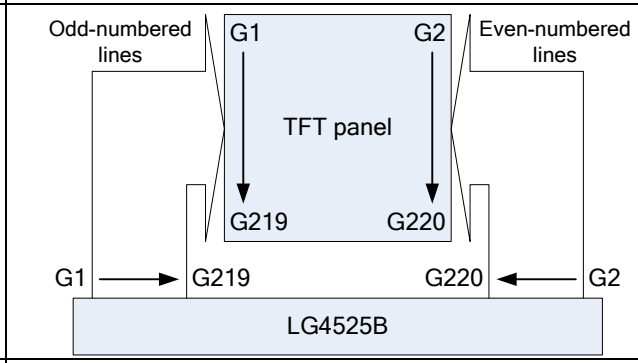
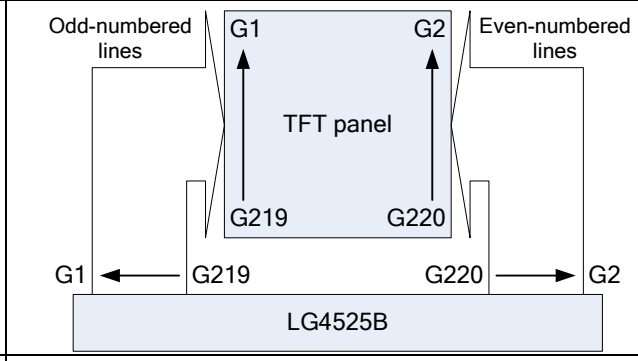
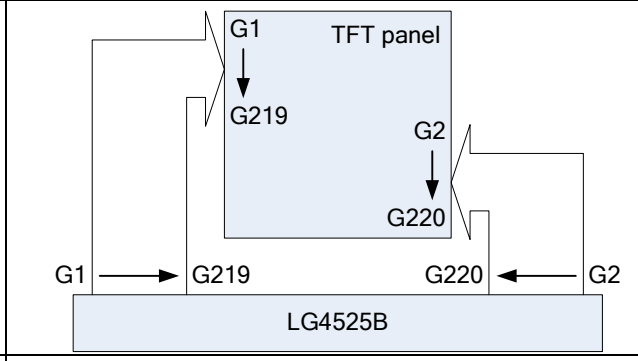
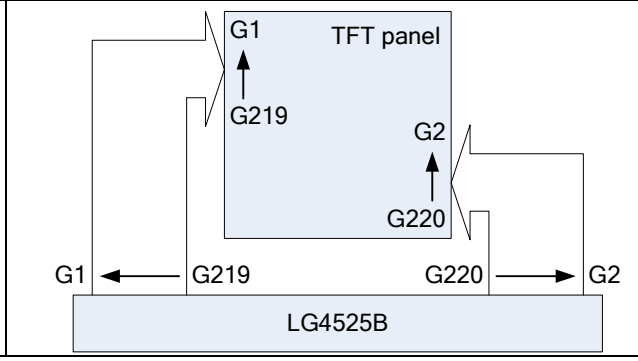
SM	GS	Scan direction	
0	0		G1, G2, G3, G4, …, G218, G219, G220
0	1		G220, G219, G218, …, G4, G3, G2, G1
1	0		G1, G3, G5, …, G217, G219, G2, G4, G6, …, G218, G220
1	1		G220, G218, G216, …, G6, G4, G2, G219, G217, G215, …, G5, G3, G1

Figure 57

n-Line Inversion AC Drive

The LG4525B, in addition to the frame-inversion liquid crystal AC drive, supports the n-line inversion AC drive, in which the polarity of liquid crystal is inverted in units of n lines, where n takes a number from 1 to 64. The quality of display will be improved by using n-line inversion AC drive.
In determining n (the value set with the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells .

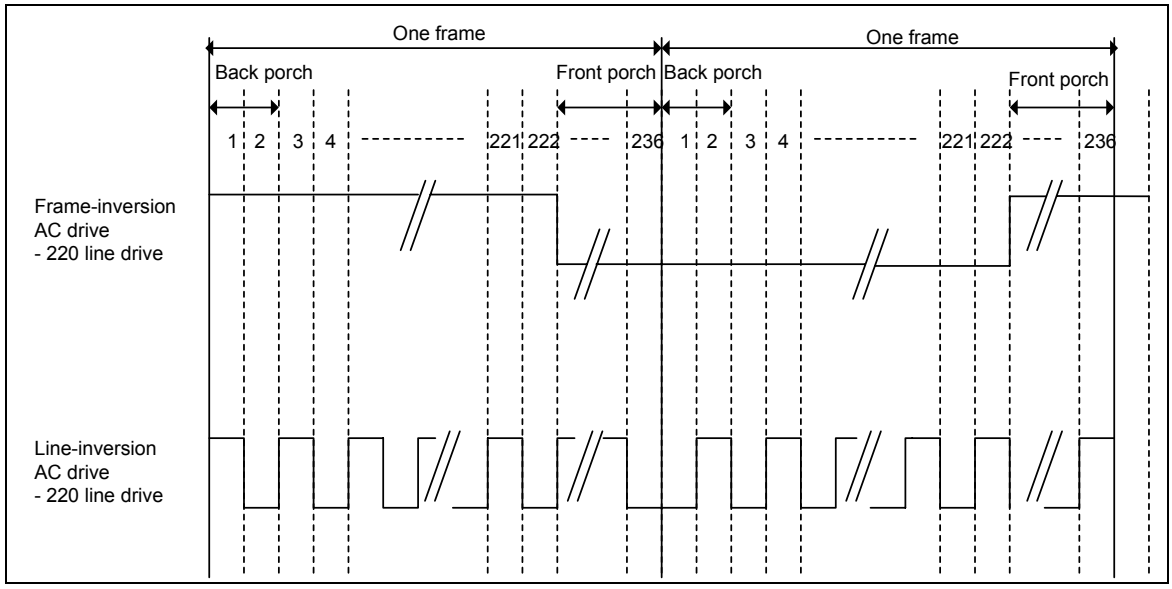


Figure 58 Example of Alternating Signals for n-line Inversion

Interlaced Scan

The LG4525B supports interlaced scan for driving a frame by splitting it into n field in order to prevent flicker.

To determine the number of fields (n : value set with the FLD bits), check the quality of display on the liquid crystal panel in use. The following table shows the scanned(gate) lines in each field. When FLD[1:0] = “01”, the number of fields in one frame is one. When FLD[1:0] = “11”, the number of fields in one frame is three. The figure illustrates the output waveforms of 3-field interlaced scan.

Table 73 Interlaced scan (GS = “0”)

FLD[1:0]	**01**		**11**	
		1	2	3
G1	*	*		
G2	*		*	*
G3	*			
G4	*	*		
G5	*		*	
G6	*			*
G7	*	*		
G8	*		*	
:				
G217	*	*		
G218	*		*	
G219	*			*
G220	*	*		

Table 74 Interlaced scan (GS = “1”)

FLD[1:0]	**01**		**11**	
		1	2	3
G220	*	*		
G219	*		*	*
G218	*			
G217	*	*		
G216	*		*	
G215	*			*
G214	*	*		
G213	*		*	
:				
G4	*	*		
G3	*		*	
G2	*			*
G1	*	*		

*: scaned gate lines

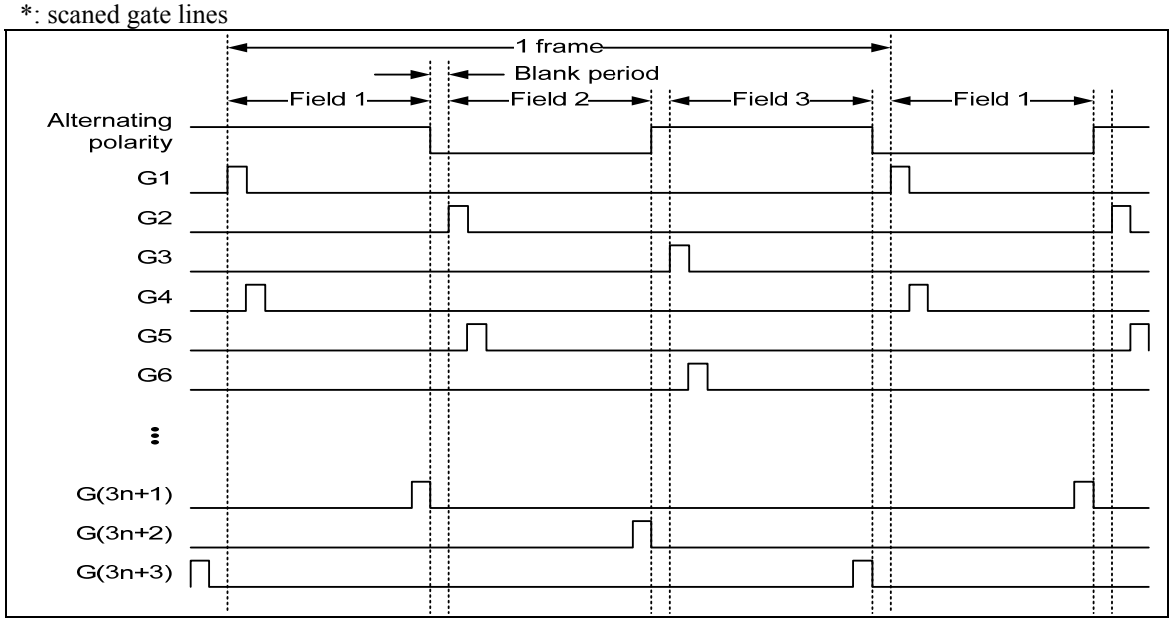


Figure 59 Gate output timing of 3-field interlaced scan

Frame-Frequency Adjustment Function

The LG4525B supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting the DIV, RTN bits without changing the oscillation frequency.

To switch frame frequencies according to whether displaying a moving picture or displaying a still picture, set a high oscillation frequency in advance. Then, set a low frame frequency to save power consumption when displaying a still picture. When displaying a moving picture, set the frequency high.

Relationship between the liquid crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be adjusted by setting the 1H period adjustment (RTNI/E) bit and the operation clock division (DIVI/E) bit.

Equation for calculating frame frequency

$$Frame\ Frequency = \frac{Fosc}{Number\ Of\ Clocks\ Per\ Line \times Division\ Ratio \times (Line + FP + BP)}$$

Fosc	: RC oscillation frequency
Number of Clocks per line	: RTNI/E bit
Division Ratio	: DIVI/E bit
Line	: number of lines to drive the LCD (NL bit)
FP	: Number of lines for front porch
BP	: Number of lines for back porch

Example of Calculation : when maximum frame frequency = 70Hz

Number of lines : 220 lines
1H period : 44 Clock cycles (RTN[6:0] = “0101100”)
Division ratio of operating clock : 1/1
Front porch : 2 lines
Back porch : 14 lines

Fosc = 70 (Hz) x 44 (clocks) x 1/1 x (220 + 2 + 14) (Lines) = 726.9(KHz)

In this case, the RC oscillation frequency is to set to 726.9KHz. Adjust the value of the external resistor connected to the RC oscillator so that RC oscillation frequency becomes 726.9KHz.

Partial Display Function

The LG4525B is provided with a function that allows sections within the panel to be displayed separately (partial display mode) .The LG4525B can select and drive two screens at any position with the screen-driving position registers (R42h and R43h).

Any two screens required for display are selectively driven and hence leads to a reduction in LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS1[7:0]) and end line (SE1[7:0]) are specified by the 1st screen-driving position register (R42h).

For the 2nd division screen, start line (SS2[7:0]) and end line (SE2[7:0]) are specified by the 2nd screen-driving position register (R43h).

The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value. The address of selection-driving lines for the 1st and 2nd screens must be specified within the NL5-0 register setting value (LCD-driving duty set value).

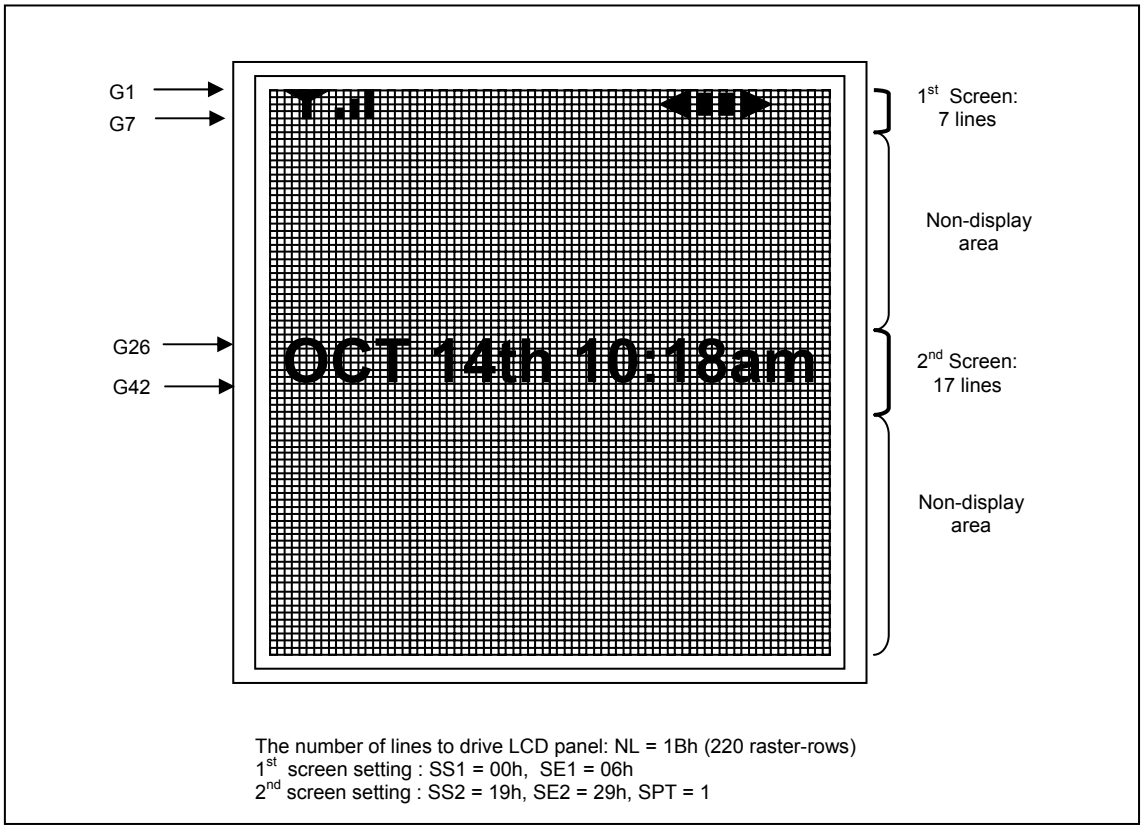


Figure 60

Constraints in setting the 1st/2nd Screen Drive Position Registers

The following restrictions must be satisfied when setting the start line (SS1[7:0]) and end line (SE1[7:0]) of the 1st screen driving position register (R42h) and the start line (SS2[7:0]) and end line (SE2[7:0]) of the 2nd screen driving position register (R43h) for the LG4525B.
Note that incorrect display may occur if the restrictions are not satisfied.

Table 75 One screen drive (SPT = 0)

Register Settings	Display Operation
(SE1[7:0])- (SS1[7:0]) = NL	Full screen display Normally displays (SE1[7:0]) to (SS1[7:0])
(SE1[7:0]) – (SS1[7:0]) < NL	Partial display Normally displays (SE1[7:0]) to (SS1[7:0]) White display for all other times (RAM data is not related at all)
(SE1[7:0]) – (SS1[7:0]) > NL	Setting disabled

Liquid crystal panel interface timing

The relationships between RGB interface signals and liquid crystal panel control signals in internal operation and RGB interface operations are as follows.

Internal clock operation

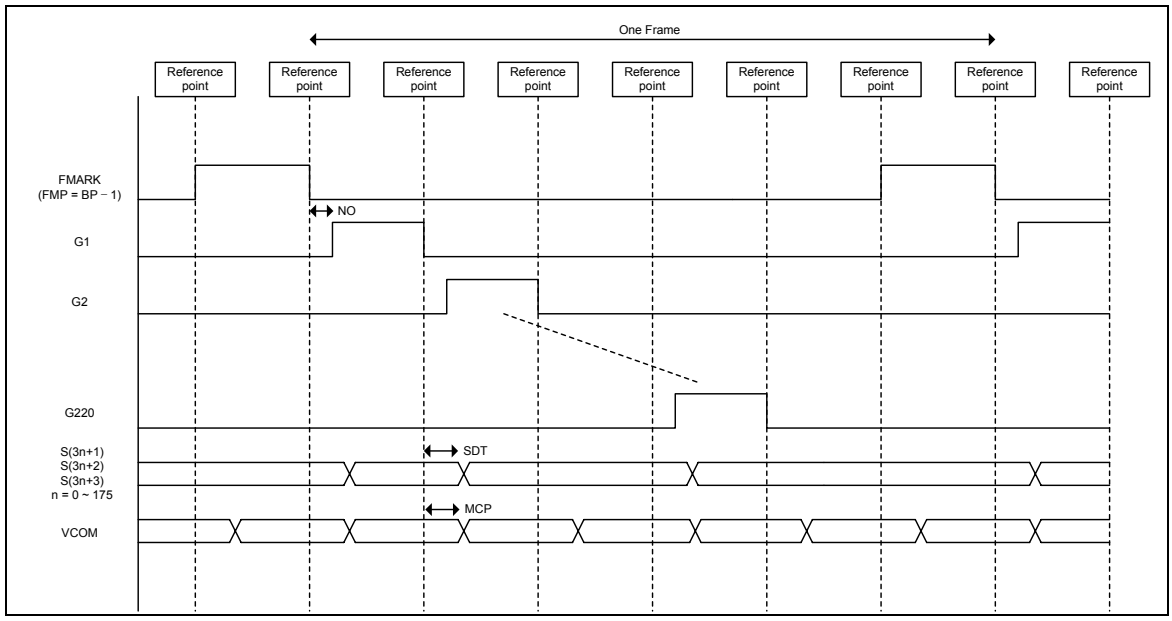


Figure 61

RGB Interface operation

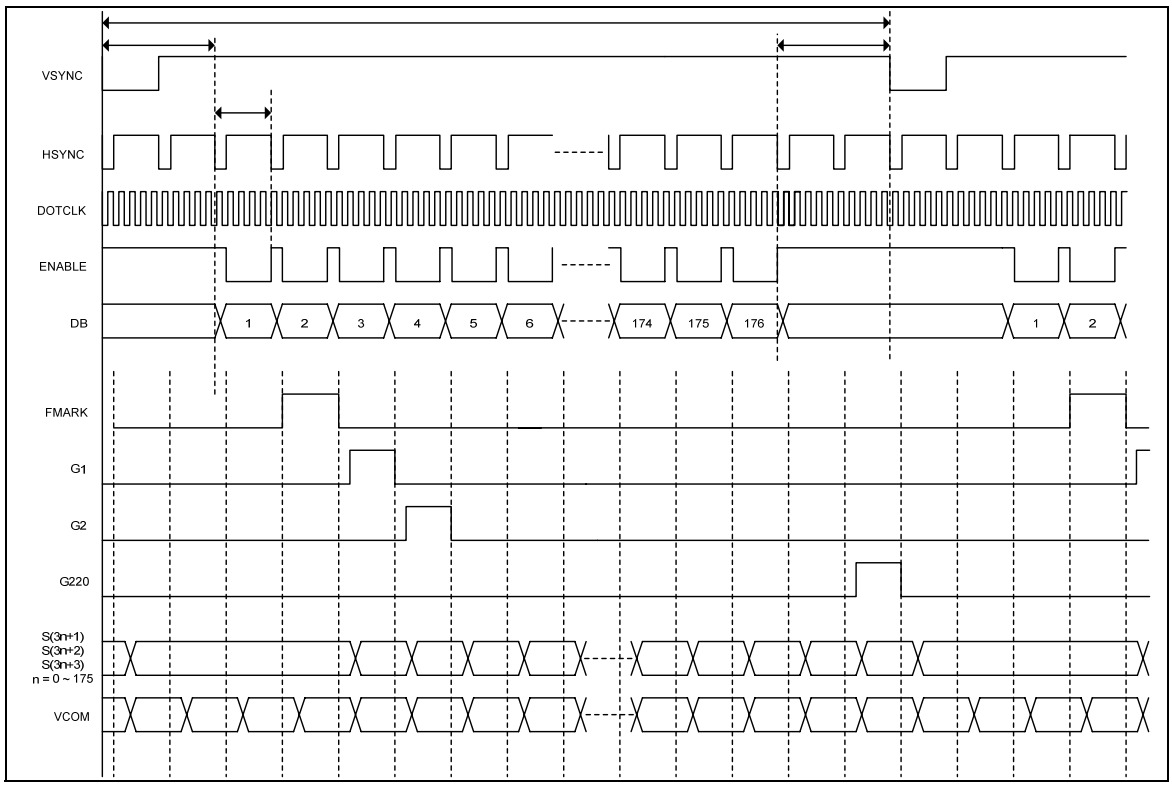


Figure 62

γ-Correction Function

The LG4525B has the γ-correction function to display in 262,144 colors simultaneously. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LG4525B available with liquid crystal panels of various characteristics.

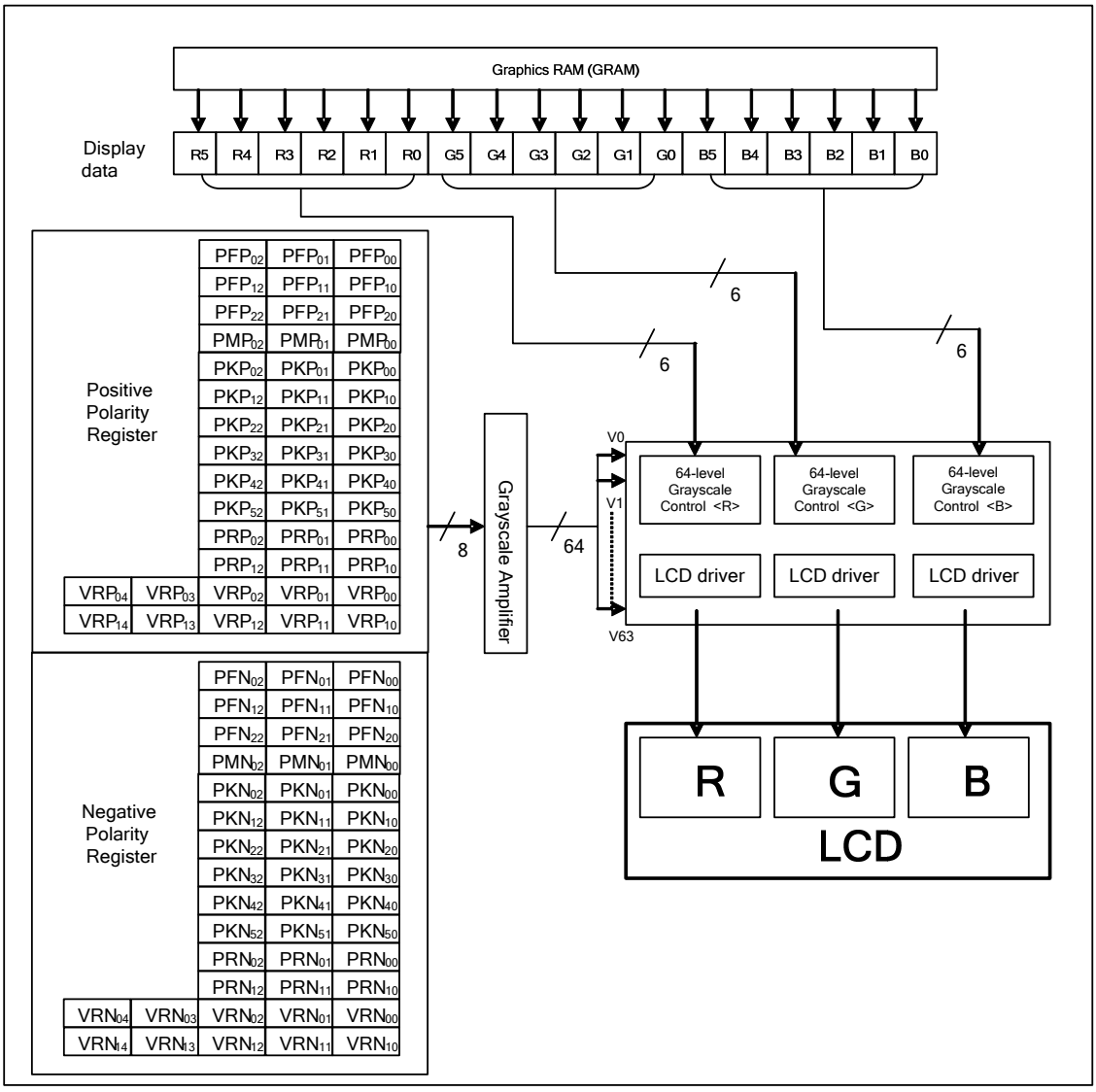


Figure 63 Grayscale control

Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the LG4525B.

To generate 64 grayscale voltages (V0 to V63), the LG4525B first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

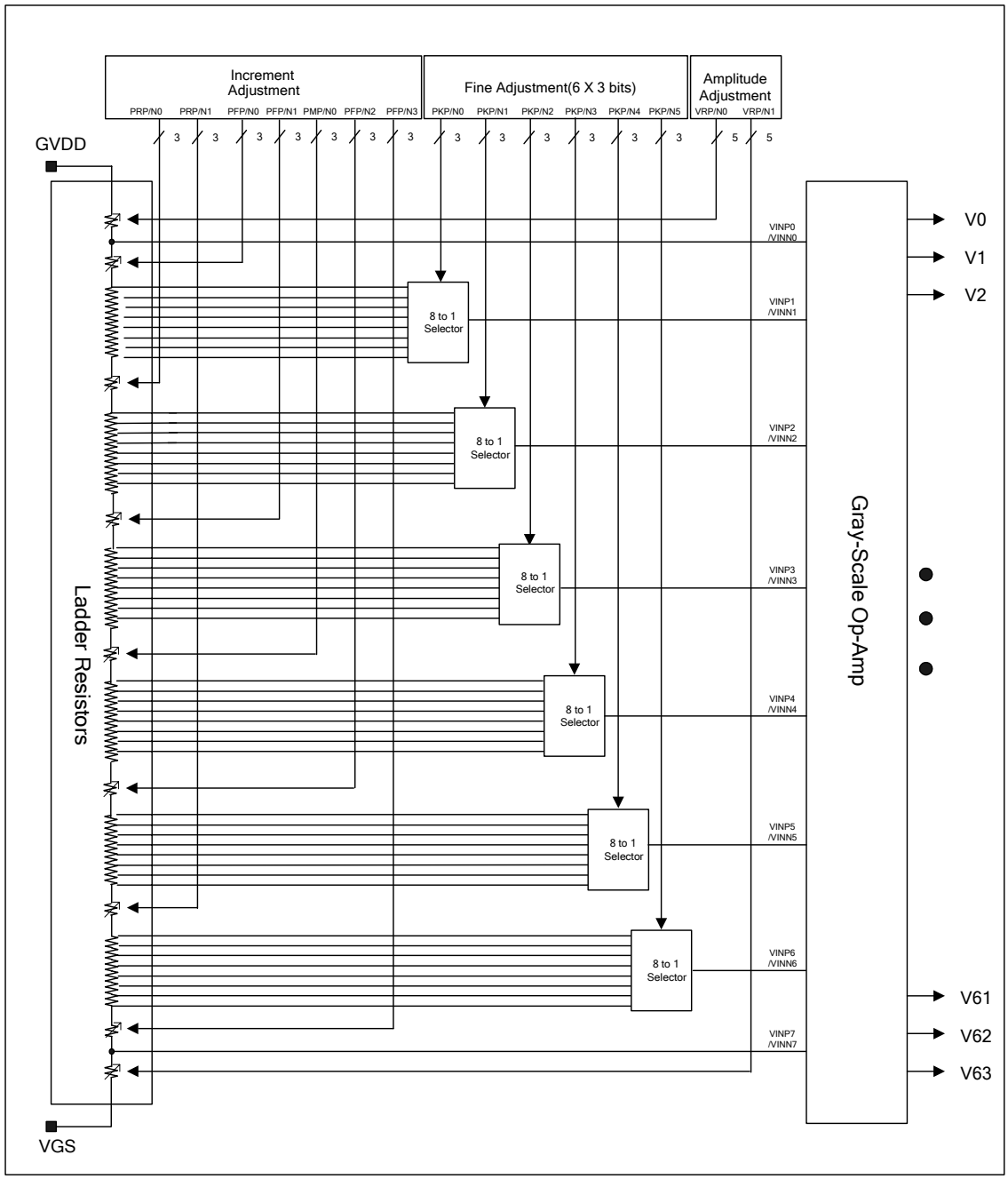


Figure 64 Grayscale amplifier unit

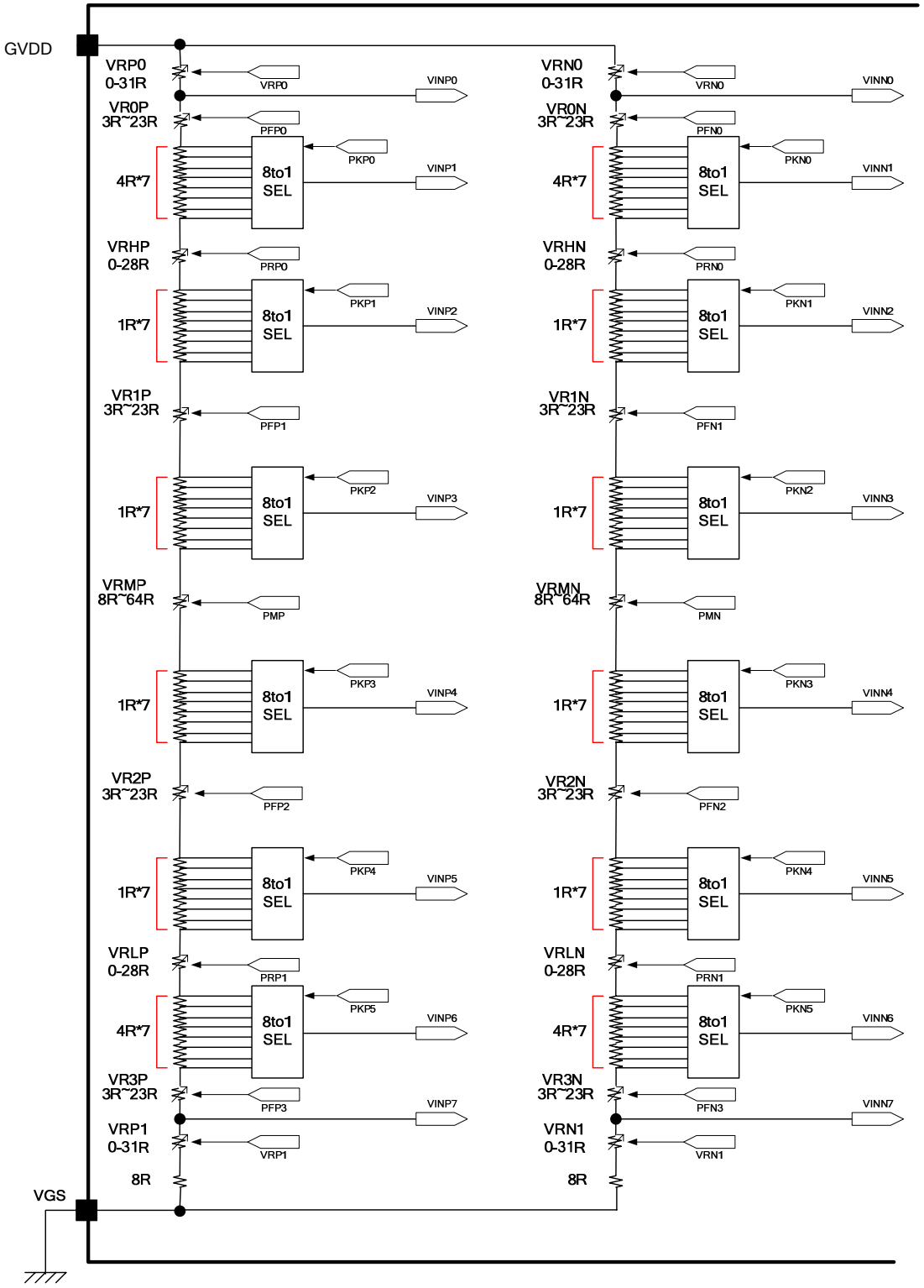


Figure 65 Ladder resistor units and 8-to-1 selectors

γ-Correction Register

The γ-correction registers of the LG4525B consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for γ-characteristics of a liquid crystal panel. These γ-correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.

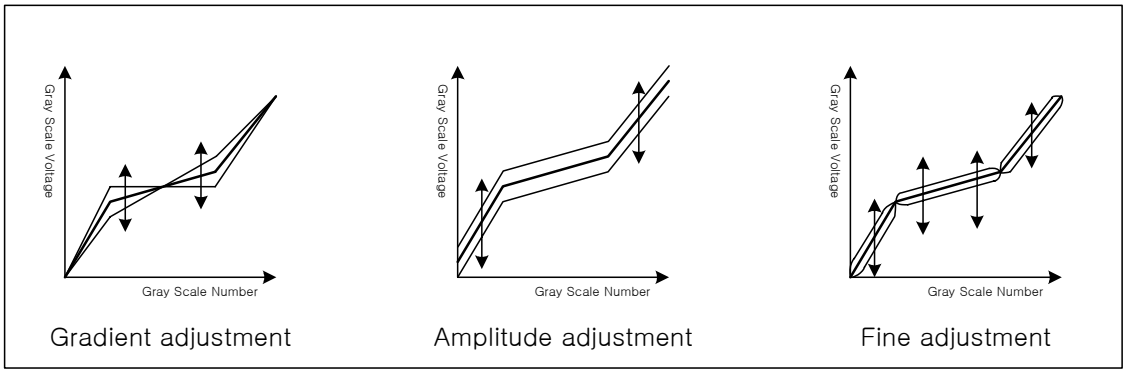


Figure 66

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 76 List of registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
	PFP0[2:0]	PFN0[2:0]	Variable resistor VR0P(N)
	PFP1[2:0]	PFN1[2:0]	Variable resistor VR1P(N)
	PFP2[2:0]	PFN2[2:0]	Variable resistor VR2P(N)
	PFP3[2:0]	PFN3[2:0]	Variable resistor VR3P(N)
	PMP[2:0]	PMN[2:0]	Variable resistor VRMP(N)
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder Resistors and 8-to-1 Selector

Block Configuration

The reference voltage generating unit as illustrated in figure 66 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LG4525B uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)/VR0~4P(N)/VRMP(N)) and amplitude adjustment (VRP(N)0~1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 77 Gradient adjustment

Contents of register PRP(N)0/1[2:0]	Resistance VRHP(N) VRLP(N)	Contents of register PFP(N)0/1/2/3[2:0]	Resistance VR0/1P(N) VR2/3P(N)	Contents of register PMP(N)[2:0]	Resistance VRMP(N)
000	0R	000	3R	000	8R
001	4R	001	5R	001	16R
010	8R	010	9R	010	24R
011	12R	011	11R	011	32R
100	16R	100	15R	100	40R
101	20R	101	17R	101	48R
110	24R	110	21R	110	56R
111	28R	111	23R	111	64R

.

Table 78 Amplitude adjustment

Contents of register VRP(N)0[4:0]	Resistance VRP(N)0 VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages

Table 79 Fine adjustment registers and selected voltage

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
3'h0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
3'h1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
3'h2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3'h3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
3'h4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
3'h5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
3'h6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
3'h7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formula.

Table 80 Formula for calculating voltage (1)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	GVDD - ΔV x VRP0/SUMRP	-	VINP0
KVP1	GVDD - ΔV x (VRP0+VR0P+0R)/SUMRP	PKP0= 3'h0	VINP1
KVP2	GVDD - ΔV x (VRP0+VR0P+4R)/SUMRP	PKP0= 3'h1	
KVP3	GVDD - ΔV x (VRP0+VR0P+8R)/SUMRP	PKP0= 3'h2	
KVP4	GVDD - ΔV x (VRP0+VR0P+12R)/SUMRP	PKP0= 3'h3	
KVP5	GVDD - ΔV x (VRP0+VR0P+16R)/SUMRP	PKP0= 3'h4	
KVP6	GVDD - ΔV x (VRP0+VR0P+20R)/SUMRP	PKP0= 3'h5	
KVP7	GVDD - ΔV x (VRP0+VR0P+24R)/SUMRP	PKP0= 3'h6	
KVP8	GVDD - ΔV x (VRP0+VR0P+28R)/SUMRP	PKP0= 3'h7	
KVP9	GVDD - ΔV x (VRP0+VR0P+28R+VRHP)/SUMRP	PKP1= 3'h0	VINP2
KVP10	GVDD - ΔV x (VRP0+VR0P+29R+VRHP)/SUMRP	PKP1= 3'h1	
KVP11	GVDD - ΔV x (VRP0+VR0P+30R+VRHP)/SUMRP	PKP1= 3'h2	
KVP12	GVDD - ΔV x (VRP0+VR0P+31R+VRHP)/SUMRP	PKP1= 3'h3	
KVP13	GVDD - ΔV x (VRP0+VR0P+32R+VRHP)/SUMRP	PKP1= 3'h4	
KVP14	GVDD - ΔV x (VRP0+VR0P+33R+VRHP)/SUMRP	PKP1= 3'h5	
KVP15	GVDD - ΔV x (VRP0+VR0P+34R+VRHP)/SUMRP	PKP1= 3'h6	
KVP16	GVDD - ΔV x (VRP0+VR0P+35R+VRHP)/SUMRP	PKP1= 3'h7	
KVP17	GVDD - ΔV x (VRP0+VR0/1P+35R+VRHP)/SUMRP	PKP2= 3'h0	VINP3
KVP18	GVDD - ΔV x (VRP0+VR0/1P+36R+VRHP)/SUMRP	PKP2= 3'h1	
KVP19	GVDD - ΔV x (VRP0+VR0/1P+37R+VRHP)/SUMRP	PKP2= 3'h2	
KVP20	GVDD - ΔV x (VRP0+VR0/1P+38R+VRHP)/SUMRP	PKP2= 3'h3	
KVP21	GVDD - ΔV x (VRP0+VR0/1P+39R+VRHP)/SUMRP	PKP2= 3'h4	
KVP22	GVDD - ΔV x (VRP0+VR0/1P+40R+VRHP)/SUMRP	PKP2= 3'h5	
KVP23	GVDD - ΔV x (VRP0+VR0/1P+41R+VRHP)/SUMRP	PKP2= 3'h6	
KVP24	GVDD - ΔV x (VRP0+VR0/1P+42R+VRHP)/SUMRP	PKP2= 3'h7	
KVP25	GVDD - ΔV x (VRP0+VR0/1P+42R+VRHP +VRMP)/SUMRP	PKP3= 3'h0	VINP4
KVP26	GVDD - ΔV x (VRP0+VR0/1P+43R+VRHP +VRMP)/SUMRP	PKP3= 3'h1	
KVP27	GVDD - ΔV x (VRP0+VR0/1P+44R+VRHP +VRMP)/SUMRP	PKP3= 3'h2	
KVP28	GVDD - ΔV x (VRP0+VR0/1P+45R+VRHP +VRMP)/SUMRP	PKP3= 3'h3	
KVP29	GVDD - ΔV x (VRP0+VR0/1P+46R+VRHP +VRMP)/SUMRP	PKP3= 3'h4	
KVP30	GVDD - ΔV x (VRP0+VR0/1P+47R+VRHP +VRMP)/SUMRP	PKP3= 3'h5	
KVP31	GVDD - ΔV x (VRP0+VR0/1P+48R+VRHP +VRMP)/SUMRP	PKP3= 3'h6	
KVP32	GVDD - ΔV x (VRP0+VR0/1P+49R+VRHP +VRMP)/SUMRP	PKP3= 3'h7	
KVP33	GVDD - ΔV x (VRP0+VR0/1/2P+49R+VRHP +VRMP)/SUMRP	PKP4= 3'h0	VINP5
KVP34	GVDD - ΔV x (VRP0+VR0/1/2P+50R+VRHP +VRMP)/SUMRP	PKP4= 3'h1	
KVP35	GVDD - ΔV x (VRP0+VR0/1/2P+51R+VRHP +VRMP)/SUMRP	PKP4= 3'h2	
KVP36	GVDD - ΔV x (VRP0+VR0/1/2P+52R+VRHP +VRMP)/SUMRP	PKP4= 3'h3	
KVP37	GVDD - ΔV x (VRP0+VR0/1/2P+53R+VRHP +VRMP)/SUMRP	PKP4= 3'h4	
KVP38	GVDD - ΔV x (VRP0+VR0/1/2P+54+VRHP +VRMP)/SUMRP	PKP4= 3'h5	
KVP39	GVDD - ΔV x (VRP0+VR0/1/2P+55R+VRHP +VRMP)/SUMRP	PKP4= 3'h6	
KVP40	GVDD - ΔV x (VRP0+VR0/1/2P+56R+VRHP +VRMP)/SUMRP	PKP4= 3'h7	
KVP41	GVDD - ΔV x (VRP0+VR0/1/2P+56R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h0	VINP6
KVP42	GVDD - ΔV x (VRP0+VR0/1/2P+60R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h1	
KVP43	GVDD - ΔV x (VRP0+VR0/1/2P+64R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h2	
KVP44	GVDD - ΔV x (VRP0+VR0/1/2P+68R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h3	
KVP45	GVDD - ΔV x (VRP0+VR0/1/2P+72R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h4	

KVP46	GVDD - ΔV x (VRP0+VR0/1/2P+76R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h5	
KVP47	GVDD - ΔV x (VRP0+VR0/1/2P+80R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h6	
KVP48	GVDD - ΔV x (VRP0+VR0/1/2P+84R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h7	
KVP49	GVDD - ΔV x (VRP0+VR0/1/2/3P+84R+VRHP+VRMP +VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors = 92R+VRHP+VRLP+VRP0+VRP1+VR0P+VR1P+VR2P +VR3P+VRMP

ΔV : Difference in electrical potential between GVDD and VGS

Table 81 Formula for calculating voltage (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	VINP2+(VINP1-VINP2) x (30/48)
V3	VINP2+(VINP1-VINP2) x (23/48)
V4	VINP2+(VINP1-VINP2) x (16/48)
V5	VINP2+(VINP1-VINP2) x (12/48)
V6	VINP2+(VINP1-VINP2) x (8/48)
V7	VINP2+(VINP1-VINP2) x (4/48)
V8	VINP2
V9	VINP3+(VINP2-VINP3) x (22/24)
V10	VINP3+(VINP2-VINP3) x (20/24)
V11	VINP3+(VINP2-VINP3) x (18/24)
V12	VINP3+(VINP2-VINP3) x (16/24)
V13	VINP3+(VINP2-VINP3) x (14/24)
V14	VINP3+(VINP2-VINP3) x (12/24)
V15	VINP3+(VINP2-VINP3) x (10/24)
V16	VINP3+(VINP2-VINP3) x (8/24)
V17	VINP3+(VINP2-VINP3) x (6/24)
V18	VINP3+(VINP2-VINP3) x (4/24)
V19	VINP3+(VINP2-VINP3) x (2/24)
V20	VINP3
V21	VINP4+(VINP3-VINP4) x (22/23)
V22	VINP4+(VINP3-VINP4) x (21/23)
V23	VINP4+(VINP3-VINP4) x (20/23)
V24	VINP4+(VINP3-VINP4) x (19/23)
V25	VINP4+(VINP3-VINP4) x (18/23)
V26	VINP4+(VINP3-VINP4) x (17/23)
V27	VINP4+(VINP3-VINP4) x (16/23)
V28	VINP4+(VINP3-VINP4) x (15/23)
V29	VINP4+(VINP3-VINP4) x (14/23)
V30	VINP4+(VINP3-VINP4) x (13/23)
V31	VINP4+(VINP3-VINP4) x (12/23)

Grayscale voltage	Formula
V32	VINP4+(VINP3-VINP4) x (11/23)
V33	VINP4+(VINP3-VINP4) x (10/23)
V34	VINP4+(VINP3-VINP4) x (9/23)
V35	VINP4+(VINP3-VINP4) x (8/23)
V36	VINP4+(VINP3-VINP4) x (7/23)
V37	VINP4+(VINP3-VINP4) x (6/23)
V38	VINP4+(VINP3-VINP4) x (5/23)
V39	VINP4+(VINP3-VINP4) x (4/23)
V40	VINP4+(VINP3-VINP4) x (3/23)
V41	VINP4+(VINP3-VINP4) x (2/23)
V42	VINP4+(VINP3-VINP4) x (1/23)
V43	VINP4
V44	VINP5+(VINP4-VINP5) x (22/24)
V45	VINP5+(VINP4-VINP5) x (20/24)
V46	VINP5+(VINP4-VINP5) x (18/24)
V47	VINP5+(VINP4-VINP5) x (16/24)
V48	VINP5+(VINP4-VINP5) x (14/24)
V49	VINP5+(VINP4-VINP5) x (12/24)
V50	VINP5+(VINP4-VINP5) x (10/24)
V51	VINP5+(VINP4-VINP5) x (8/24)
V52	VINP5+(VINP4-VINP5) x (6/24)
V53	VINP5+(VINP4-VINP5) x (4/24)
V54	VINP5+(VINP4-VINP5) x (2/24)
V55	VINP5
V56	VINP6+(VINP5-VINP6) x (44/48)
V57	VINP6+(VINP5-VINP6) x (40/48)
V58	VINP6+(VINP5-VINP6) x (36/48)
V59	VINP6+(VINP5-VINP6) x (32/48)
V60	VINP6+(VINP5-VINP6) x (25/48)
V61	VINP6+(VINP5-VINP6) x (18/48)
V62	VINP6
V63	VINP7

Note: Make sure AVDD-V0 > 0.5V

Relationship between RAM Data and Voltage Output Levels
The relationship between RAM data and source output voltage levels is as follows.

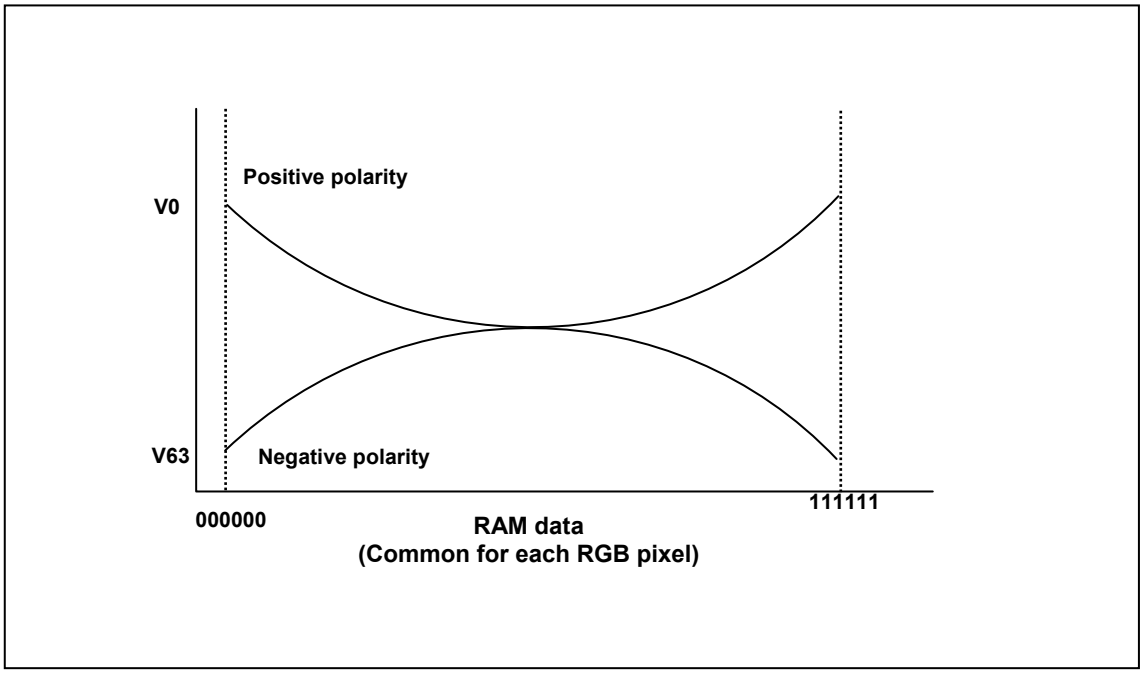


Figure 67 RAM data and the output voltage (REV = "1")

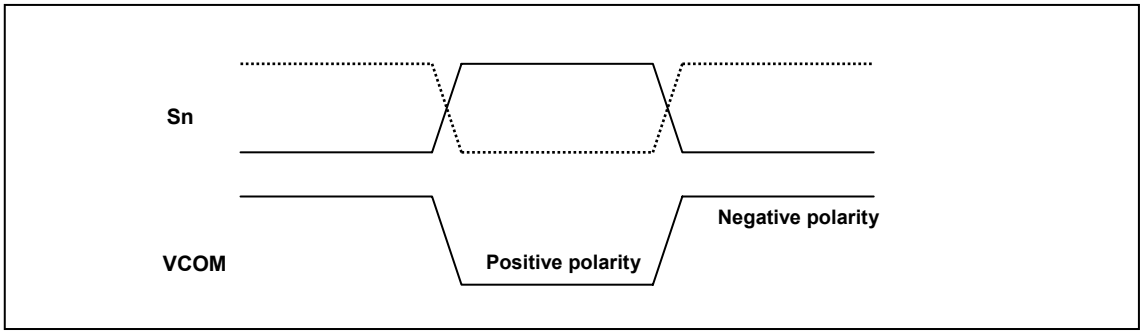


Figure 68 Source output and VCOM

8-Color Display Mode

The LG4525B has a function to display in 8colors. In 8-color mode, available grayscale levels are V0 and V63, and the power supplies of other grayscales (V1 to V62) are halted to reduce power consumption.

In 8-color display mode, the MSBs of the respective dot data (R5, G5, B5) are written to the rest of the dot data in order to display in 8 colors without rewriting the RAM data.

The γ- correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.

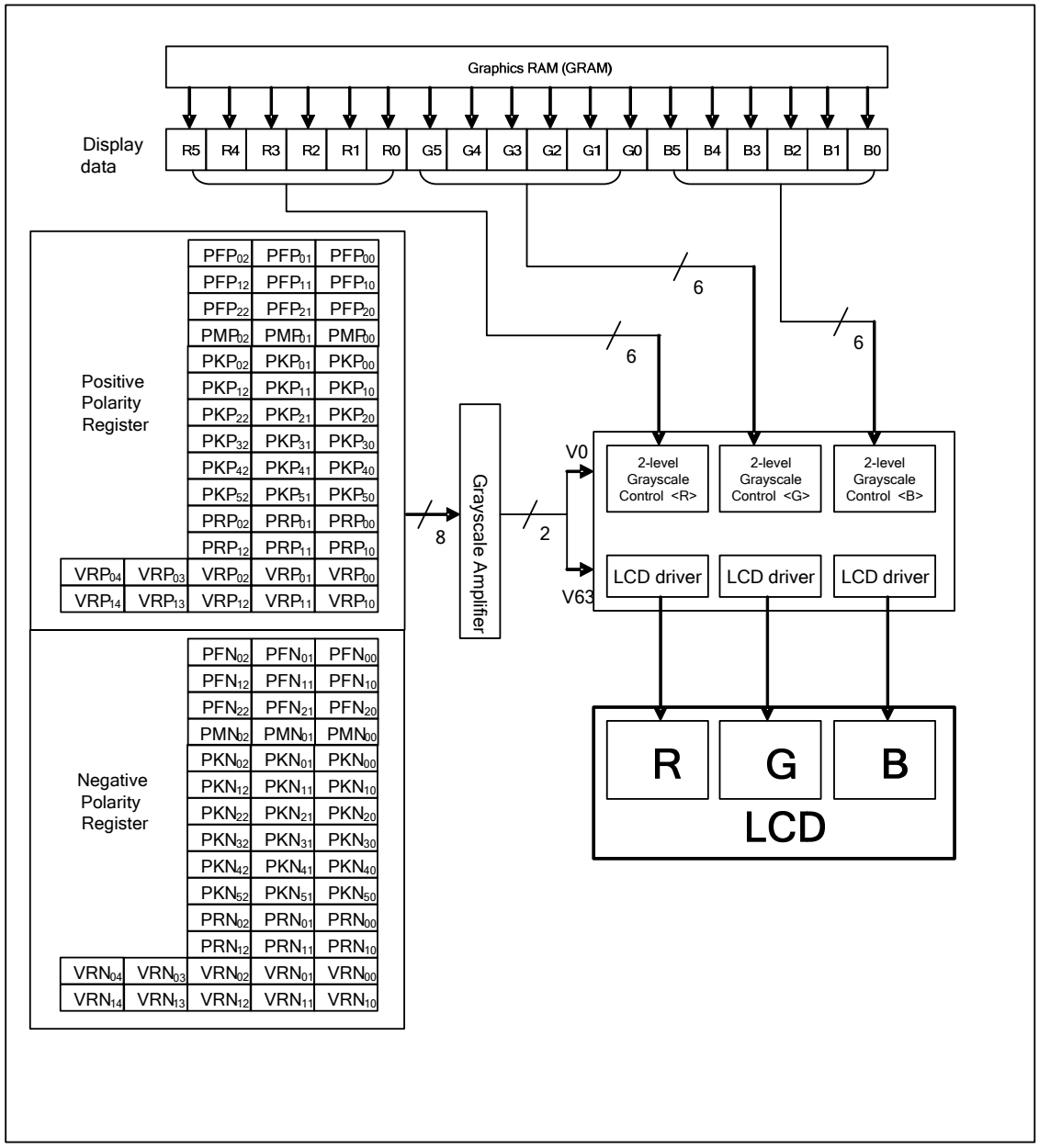


Figure 69 8-color display mode

To switch between the 262,144-color mode and 8-color mode, follow the sequence below.

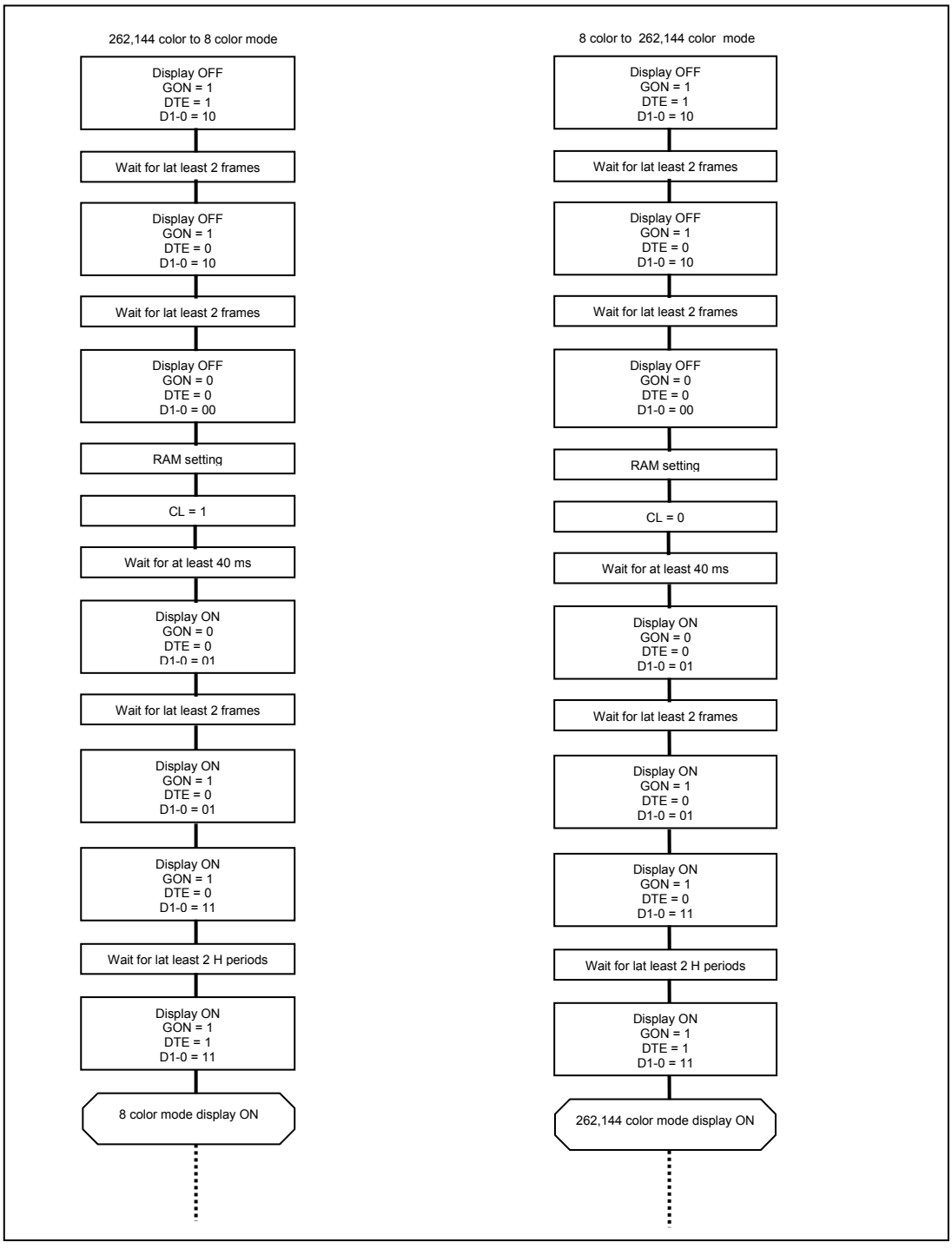


Figure 70

Power-supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the LG4525B.

Power supply circuit connection example 1 (VCI1 = VCI1 AMP)

In the following example, the VCI1 level is adjusted internally with the VCI1 output circuit.

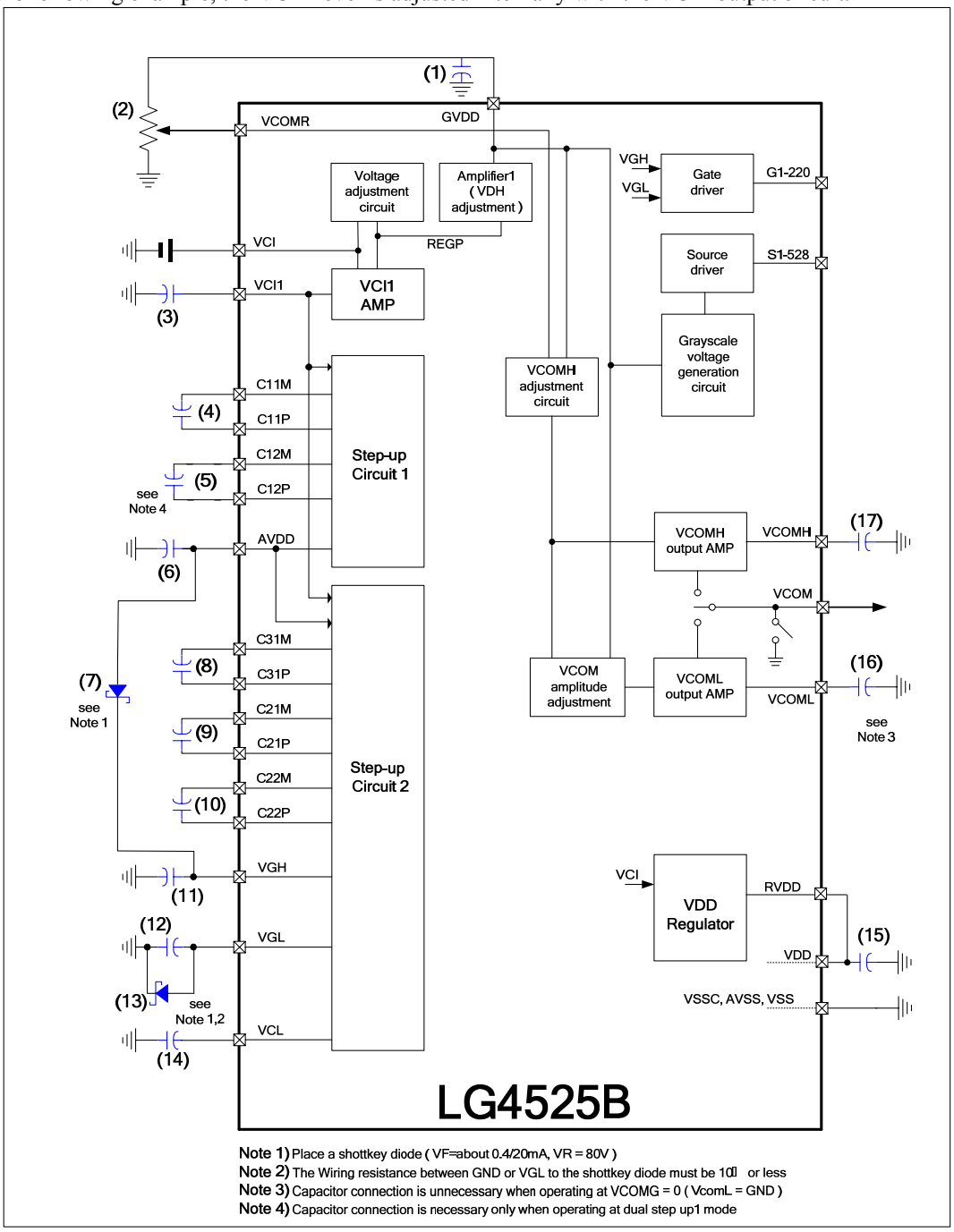


Figure 71

Note: The wiring resistance between the schottky diode and GND/VGL must be 10-Ohm or less.

Power supply circuit connection example2 (VCI1 = VCI direct input)

In the following example, the electrical VCI is directly applied to VCI1. In this case, the VCI1 level cannot be adjusted internally but step-up operation becomes more effective

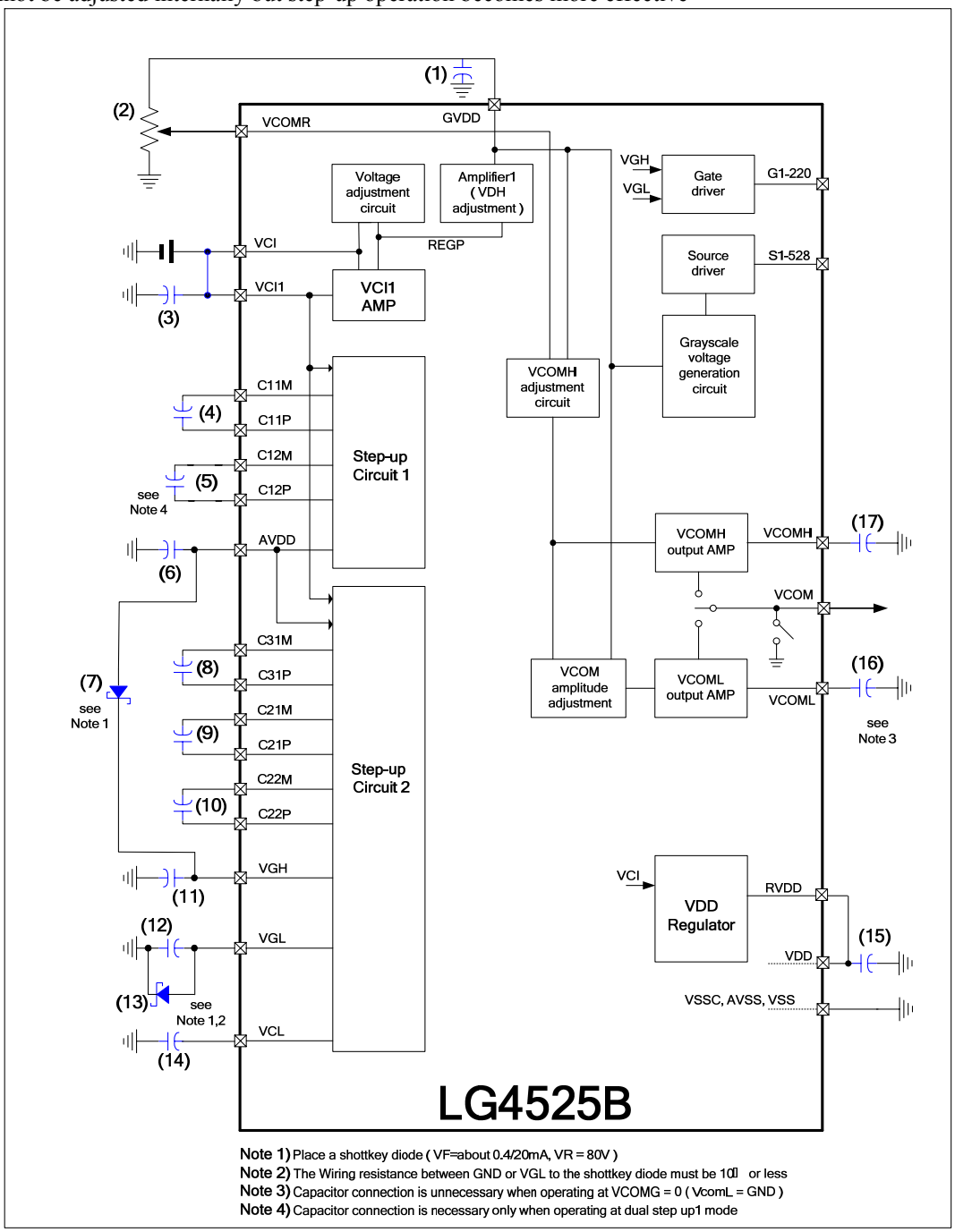


Figure 72

Note: The wiring resistance between the schottky diode and GND/VGL must be 10-Ohm or less.
When directly applying the VCI level to VCI1, set VC=3'h0.

Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the LG4525B are as follows.

Table 82 Capacitor

Capacitance	Voltage proof	Pin Connection
1uF (B characteristics)	6V	(1)GVDD, (3)VCI1, (4) C11M/P, (5) C12M/P, (8) C31M/P, (14) VCL, (15) VDD, (16) VCOML, (17) VCOMH
	10V	(6) AVDD, (9) C21M/P, (10) C22M/P
	25V	(11) VGH, (12) VGL

Notes: 1. Check with the LC module.
2. The numbers in the parentheses corresponds to the numbers of the elements in Figure 71, Figure 72 .

Table 83 Schottky Diode

Specification	Pin Connection
VF<0.4 V/20 mA@25℃, VR ≥ 30V	(7) AVDD-VGH (13) GND-VGL

Table 84 Variable Resistor

Specification	Pin Connection
>200kΩ	(2) VCOMR

Application of Power-supply Circuit

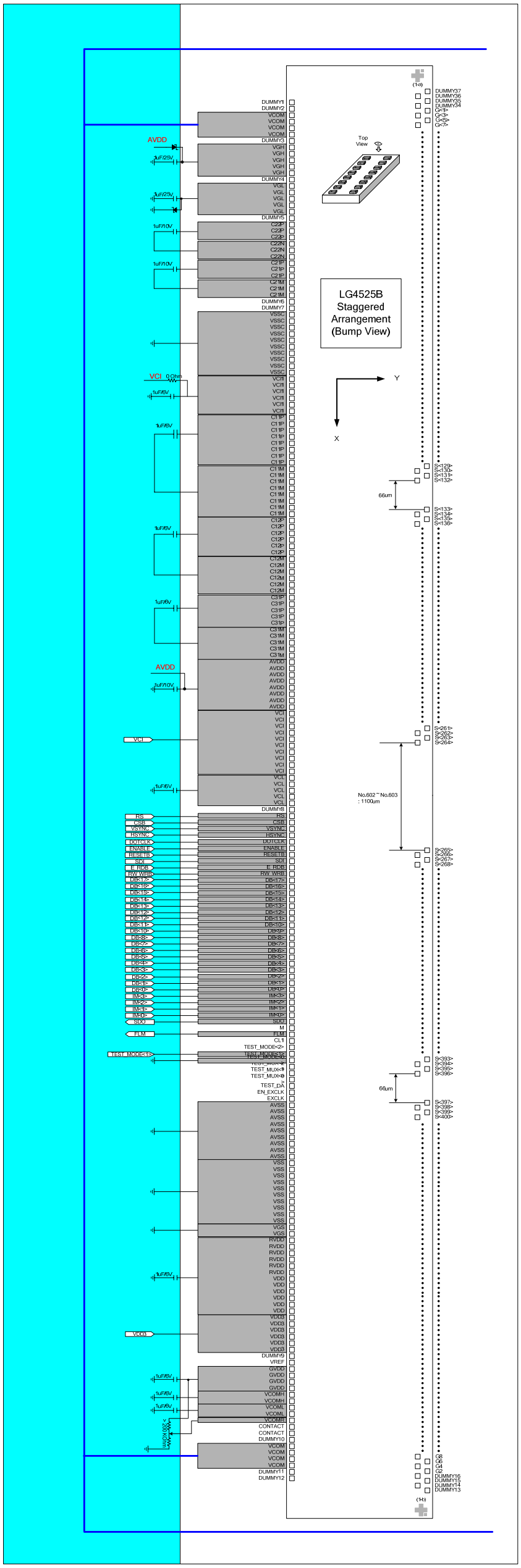


Figure 73

Voltage Setting Pattern Diagram

The pattern diagram of voltage setting and waveforms of the liquid crystal application voltages are as follows.

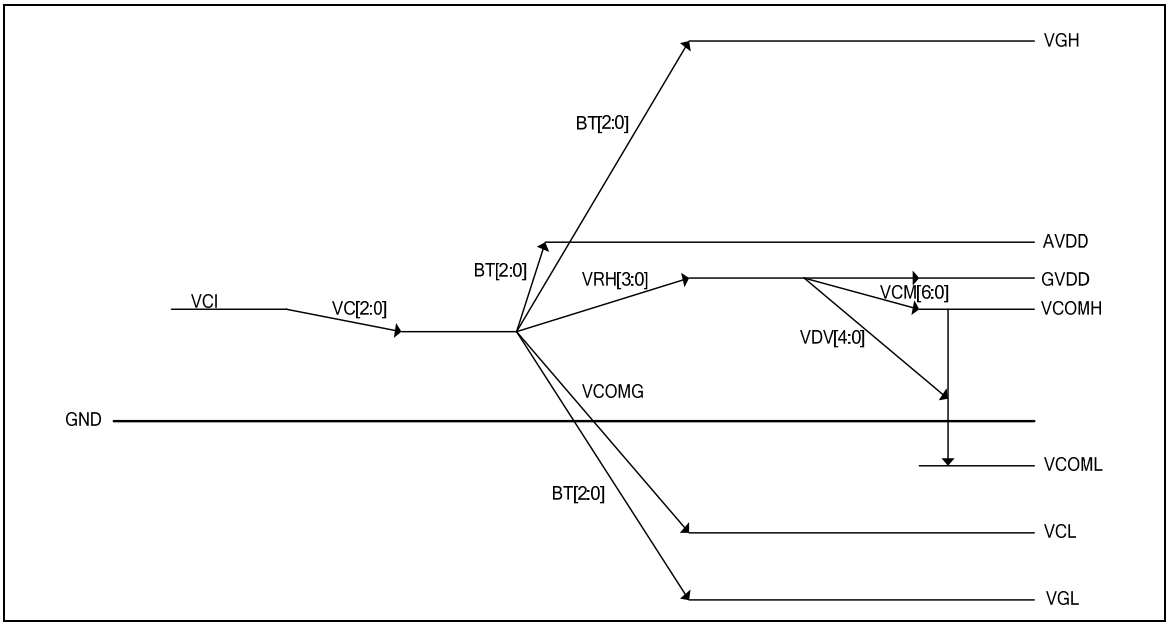


Figure 74 Pattern Diagram for Voltage Setting

Note Output voltages of AVDD, VGH, VGL, and VCL drop from setting voltage(idea voltage) depending on the current consumption at output. (AVDD – GVDD) > 0.5V is the relation to the actual voltage. When using the voltage in the large current consumption at the fast VCOM2 cycle(such as line-by-line inversion), check the voltage value

Power Supply Instruction Setting

The followings are the sequences for setting power supply ON/OFF. Make power supply ON/OFF settings according to the following sequences in Display ON/OFF, Standby set/exit, Sleep set/exit sequences.

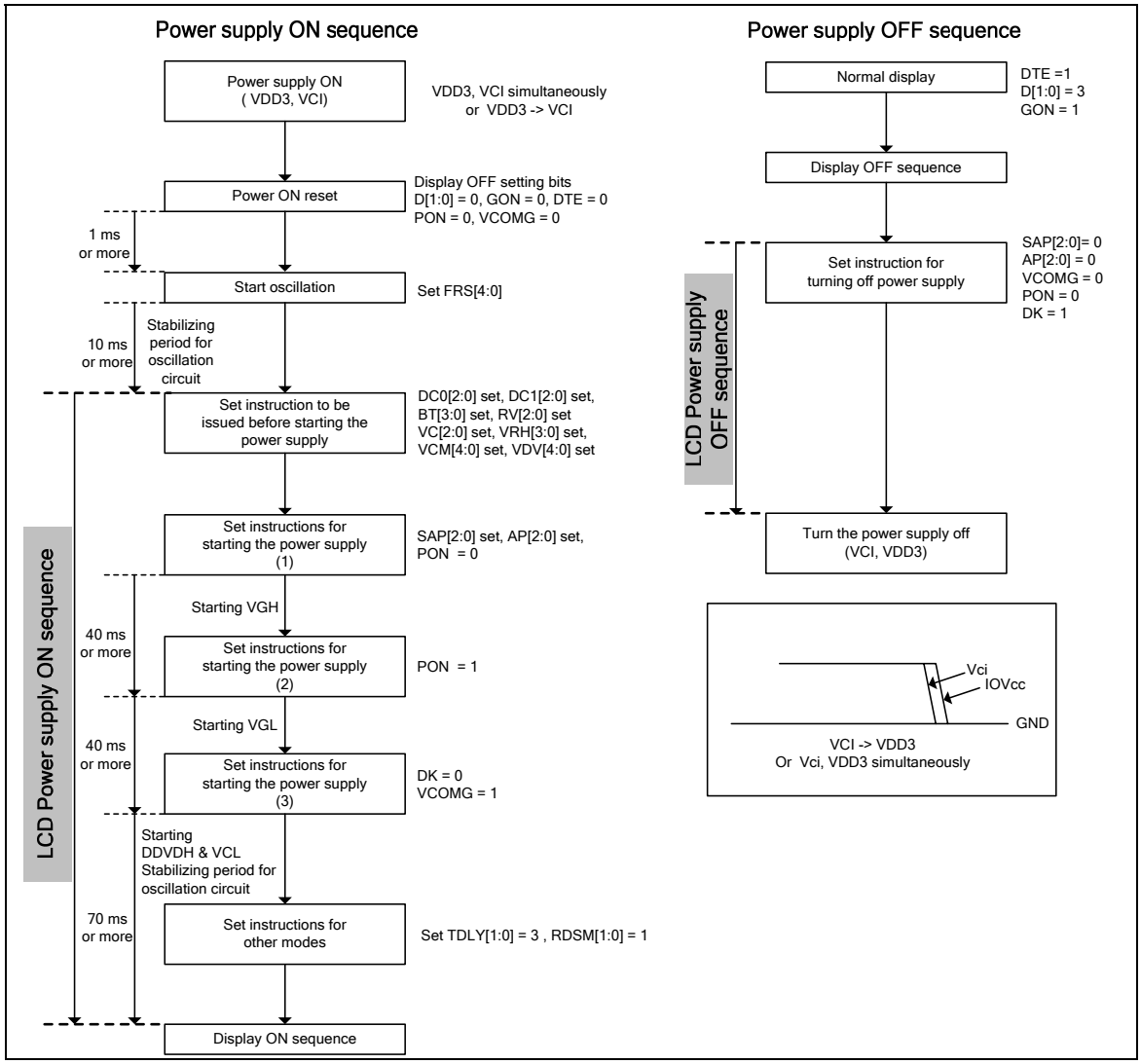


Figure 75

Instruction Setting

The following are the sequences for various instruction settings with the LG4525B. When making the following instruction settings, follow the respective sequences below.

Display ON/OFF sequence

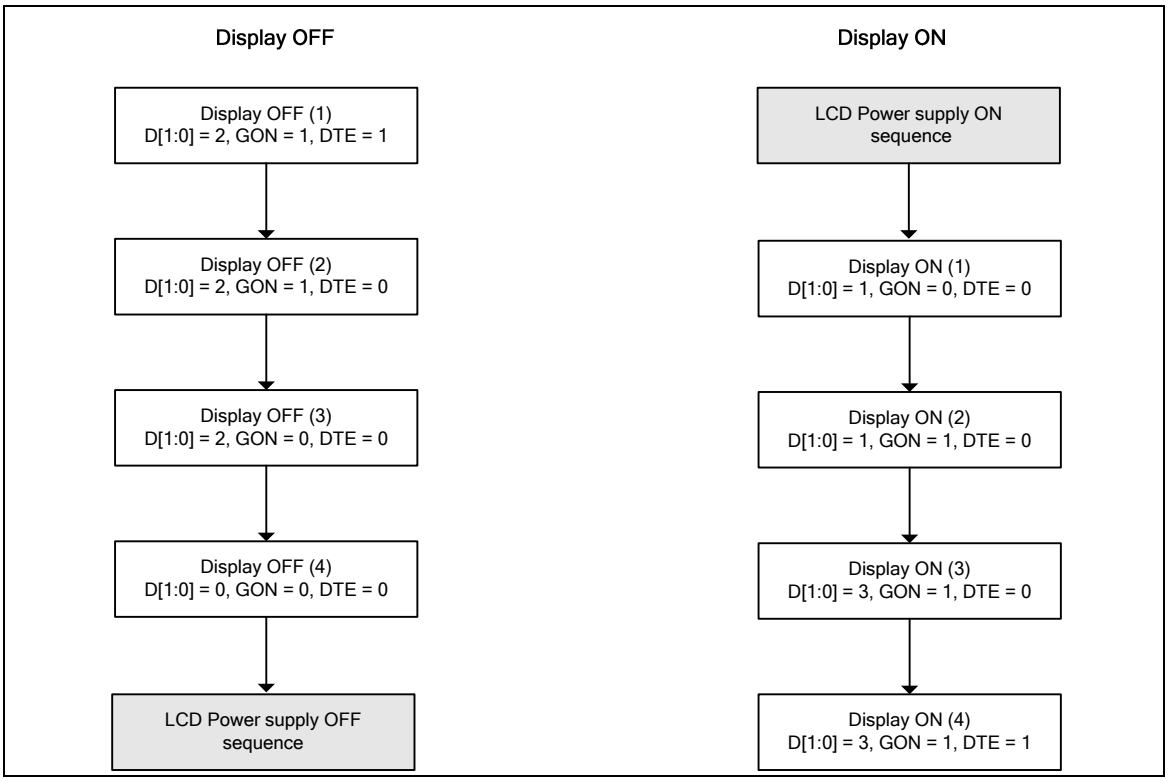


Figure 76

Standby / Sleep mode SET/EXIT sequences

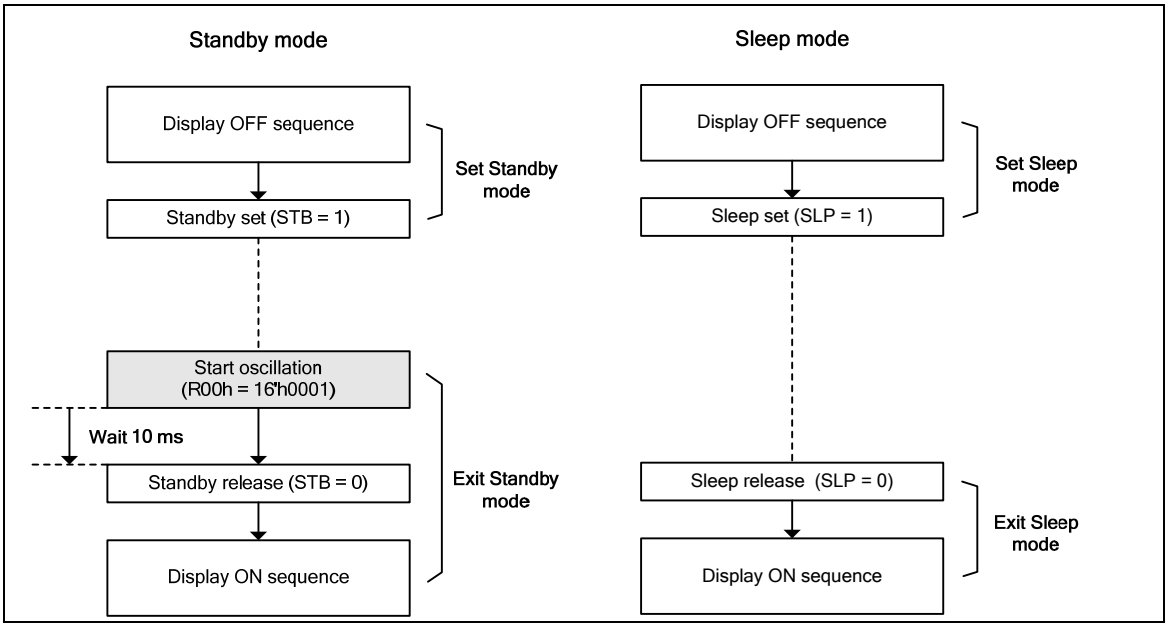


Figure 77

Note : “Display ON/OFF” sequences include “LCD Power Supply ON/OFF” sequences respectively. See “Display ON/OFF sequence” section.

Deep standby mode IN/EXIT sequences

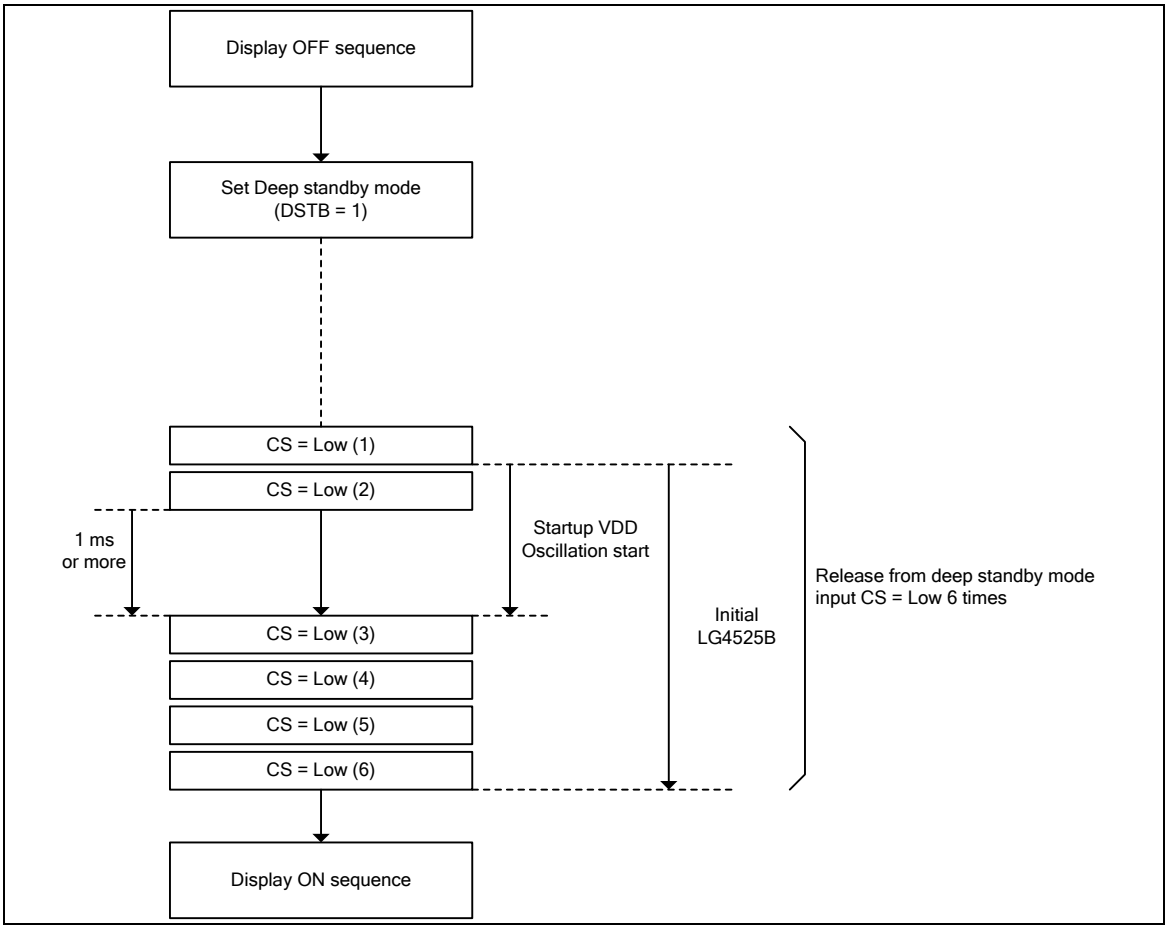


Figure 78

Note : “Display ON/OFF” sequences include “LCD Power Supply ON/OFF” sequences respectively.
See “Display ON/OFF sequence” section.

8-color mode setting

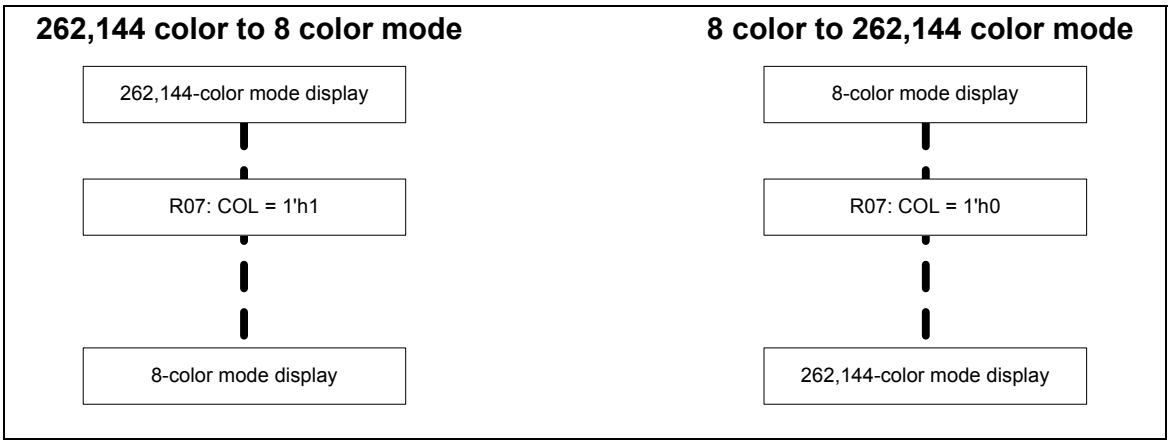


Figure 79

Partial Display setting

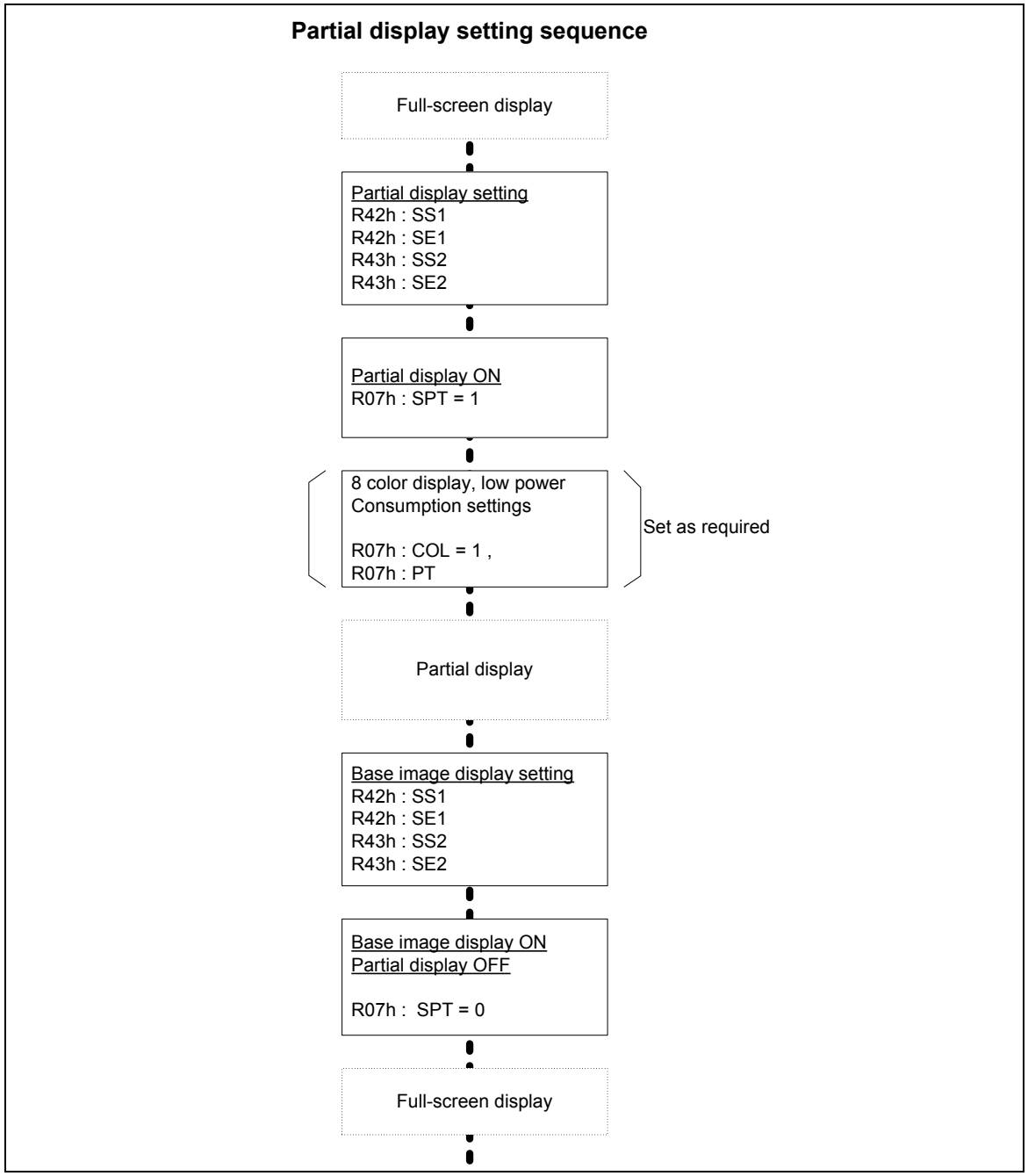


Figure 80

Absolute Maximum Ratings

Table 85

Item	Symbol	Unit	value	Notes
Power supply voltage (1)	VCI, VDD3	V	-0.3 ~ +4.5	1, 2
Power supply voltage (2)	VCI – AGND	V	-0.3 ~ +4.5	1, 3
Power supply voltage (3)	AVDD – AGND	V	-0.3 ~ +8.0	1, 4
Power supply voltage (4)	AGND – VCL	V	-0.3 ~ +4.5	1
Power supply voltage (5)	AVDD –VCL	V	-0.3 ~ +8.0	1, 5
Power supply voltage (6)	VGH – AGND	V	-0.3 ~ +18	1, 6
Power supply voltage (7)	AGND – VGL	V	-0.3 ~ +18	1, 7
Input voltage	Vi	V	-0.3~VDD3+0.3	1
Operating temperature	Topr	˚C	-40 ~ +85	1, 8
Storage temperature	Tstg	˚C	-55 ~ +125	1

Note 1) If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.
Note 2) Make sure (High) VDD3 ≥ GND (Low).
Note 3) Make sure (High) VCI ≥ GND (Low).
Note 4) Make sure (High) AVDD ≥ AGND (Low).
Note 5) Make sure (High) AVDD ≥ VCL (Low).
Note 6) Make sure (High) VGH ≥ AGND (Low).
Note 7) Make sure (High) AGND ≥ VGL (Low).
Note 8) The DC/AC characteristics of die and wafer products is guaranteed at 85 ℃.

Electrical Characteristics

DC Characteristics

Table 86

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Notes
Input high-level voltage	VIH	V	VDD3 = 1.65 ~ 3.3V	0.8VDD3		VDD3	2,3
Input low-level voltage	VIL	V	VDD3 = 1.65 ~ 3.3V	0		0.2VDD3	2,3
Output high-level voltage (1) (DB17-0, SDO, FLM)	VOH	V	VDD3 = 1.65 ~ 3.3V IOH = 0.1mA	0.8VDD3			2
Output lowlevel voltage (1) (DB17-0, SDO, FLM)	VOL	V	VDD3 = 1.65~ 3.3V IOL = 0.1mA			0.2VDD3	2
I/O leakage current	I_{li}	µA	Vin = 0 ~ VDD3	-1		1	4
Current consumption : Deep standby mode	I_{ST}	µA	VDD3 = VCI = 2.8V , Ta ≈ 25°C		1	10	5

Note : Operating temperature = -40°C ~ 80°C

80-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 87 See Figure 82 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	tCYCW	ns	T.B.D.	-	-
		Read	tCYCR	ns	T.B.D.	-	-
Write “Low” level pulse width Read “Low” level pulse width		Write	PWLW	ns	T.B.D.	-	-
		Read	PWLR	ns	T.B.D.	-	-
Write “High” level pulse width Read “High” level pulse width		Write	PWHW	ns	T.B.D.	-	-
		Read	PWHR	ns	T.B.D.	-	-
Write/Read rise/fall time			tWRr,tWRF	ns		-	T.B.D.
Setup time	Write (RS to CSB/ WRB)		tAS	ns	T.B.D.	-	-
	Read (RS to CSB/ RDB)				T.B.D.	-	-
Address hold time			tAH	ns	T.B.D.	-	-
Write data setup time			tDSW	ns	T.B.D.	-	-
Write data hold time			tH	ns	T.B.D.	-	-
Read data delay time			tDDR	ns	-	-	T.B.D.
Read data hold time			tDHR	ns	T.B.D.	-	-

80-System Bus Interface Timing Characteristics (8/9-Bit Bus)

Table 88 See Figure 82 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	tCYCW	ns	T.B.D.	-	-
		Read	tCYCR	ns	T.B.D.	-	-
Write “Low” level pulse width Read “Low” level pulse width		Write	PWLW	ns	T.B.D.	-	-
		Read	PWLR	ns	T.B.D.	-	-
Write “High” level pulse width Read “High” level pulse width		Write	PWHW	ns	T.B.D.	-	-
		Read	PWHR	ns	T.B.D.	-	-
Write/Read rise/fall time			tWRr,tWRF	ns	-	-	T.B.D.
Setup time	Write (RS to CSB/ WRB)		tAS	ns	T.B.D.	-	-
	Read (RS to CSB/ RDB)				T.B.D.	-	-
Address hold time			tAH	ns	T.B.D.	-	-
Write data setup time			tDSW	ns	T.B.D.	-	-
Write data hold time			tH	ns	T.B.D.	-	-
Read data delay time			tDDR	ns	-	-	T.B.D.
Read data hold time			tDHR	ns	T.B.D.	-	-

Serial Peripheral Interface Timing Characteristics

Table 89 See Figure 83 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	tSCYC	ns	T.B.D.	-	-
	Read (transmitted)	tSCYC	ns	T.B.D.	-	-
Serial clock “High” level pulse width	Write (received)	tSCH	ns	T.B.D.	-	-
	Read (transmitted)	tSCH	ns	T.B.D.	-	-
Serial clock “Low” level pulse width	Write (received)	tSCL	ns	T.B.D.	-	-
	Read (transmitted)	tSCL	ns	T.B.D.	-	-
Serial clock rise/fall time		tscr,tscf	ns	-	-	T.B.D.
Chip select setup time		tCSU	ns	T.B.D.	-	-
Chip select hold time		tCH	ns	T.B.D.	-	-
Serial input data setup time		tSISU	ns	T.B.D.	-	-
Serial input data hold time		tSIH	ns	T.B.D.	-	-
Serial output data delay time		tSOD	ns	-	-	T.B.D.
Serial output data hold time		tSOH	ns	T.B.D.	-	-

RGB Interface Timing Characteristics

Table 90 See Figure 84 (18/16-bit I/F, VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	ns	T.B.D.	-	-
ENABLE setup time	tENS	ns	T.B.D.	-	-
ENABLE hold time	tENH	ns	T.B.D.	-	-
DOTCLK “Low” level pulse width	PWDL	ns	T.B.D.	-	-
DOTCLK “High” level pulse width	PWDH	ns	T.B.D.	-	-
DOTCLK cycle time	tCYCD	ns	T.B.D.	-	-
Data setup time	tPDS	ns	T.B.D.	-	-
Data hold time	tPDH	ns	T.B.D.	-	-
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	-	-	T.B.D.

Reset Timing Characteristics

Table 91 See Figure 85 & Figure 86 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset wait time	**tRW**	**ms**	1	**-**	**-**
Reset “Low” level width	**tRES**	**ms**	1	-	-
Reset rise time	**trRES**	**us**	-	-	10
Reset time	**tRT**	**ms**	-	-	10

Oscillator Clock Characteristics

Table 92 (Condition: VDD3=VCI=2.8V, Ta=25°C, R14h=16’h6030, R0Fh=16’h0007)

Item	Symbol	Unit	Min	Typ	Max
Oscillator Frequency	fosc	KHz	T.B.D.	T.B.D.	T.B.D.

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following are the configurations of I pin, I/O pin, and O pin.

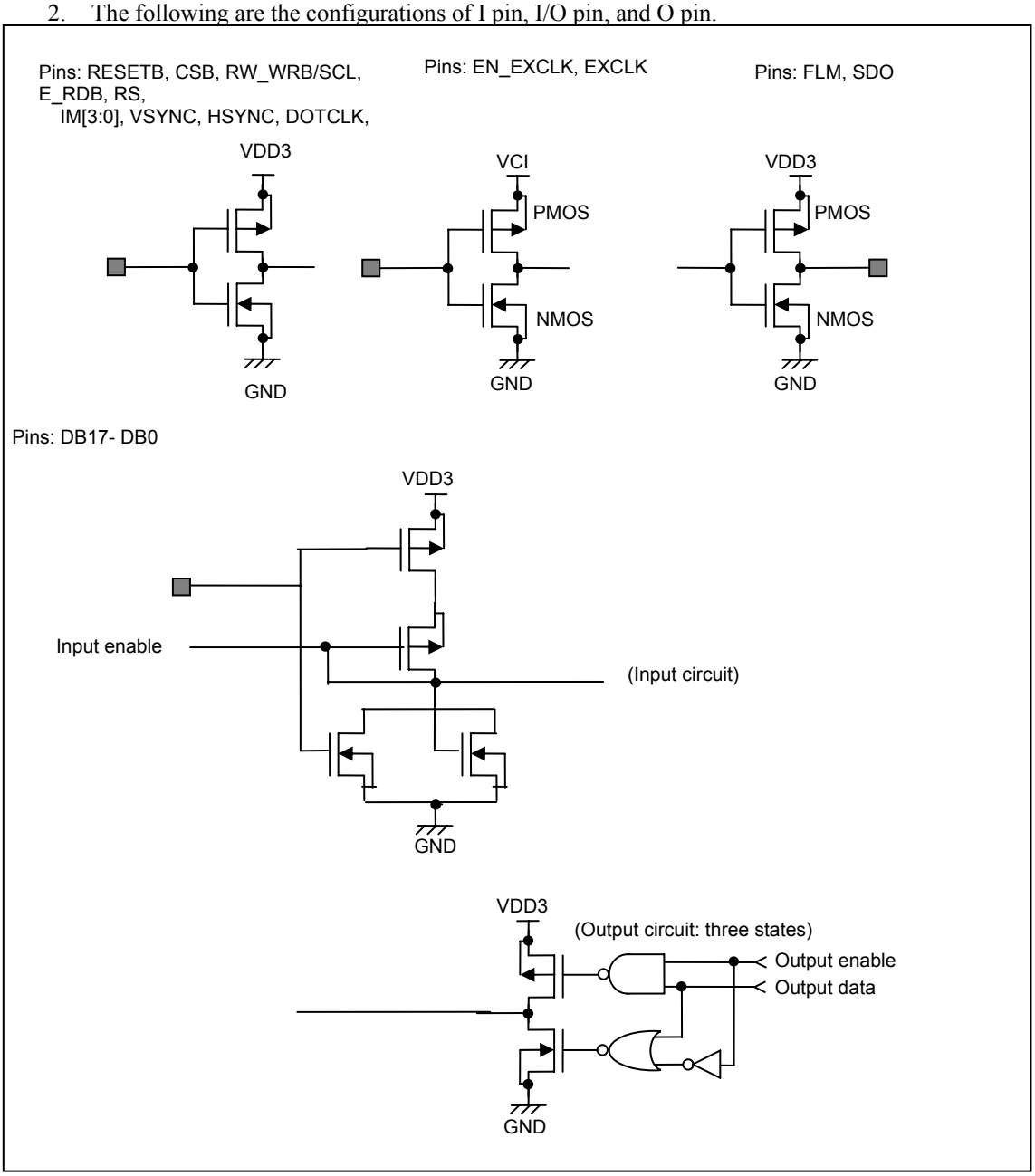


Figure 81

3. The TEST1 pin must be grounded (GND). The IM[3:0] pins must be fixed at either GND or the VDD3 level.
4. This excludes currents though the output drive MOS.
5. This excludes currents flowing through input/output units. Be sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CSB pin is set to “High” or “Low”.

Timing characteristic diagram

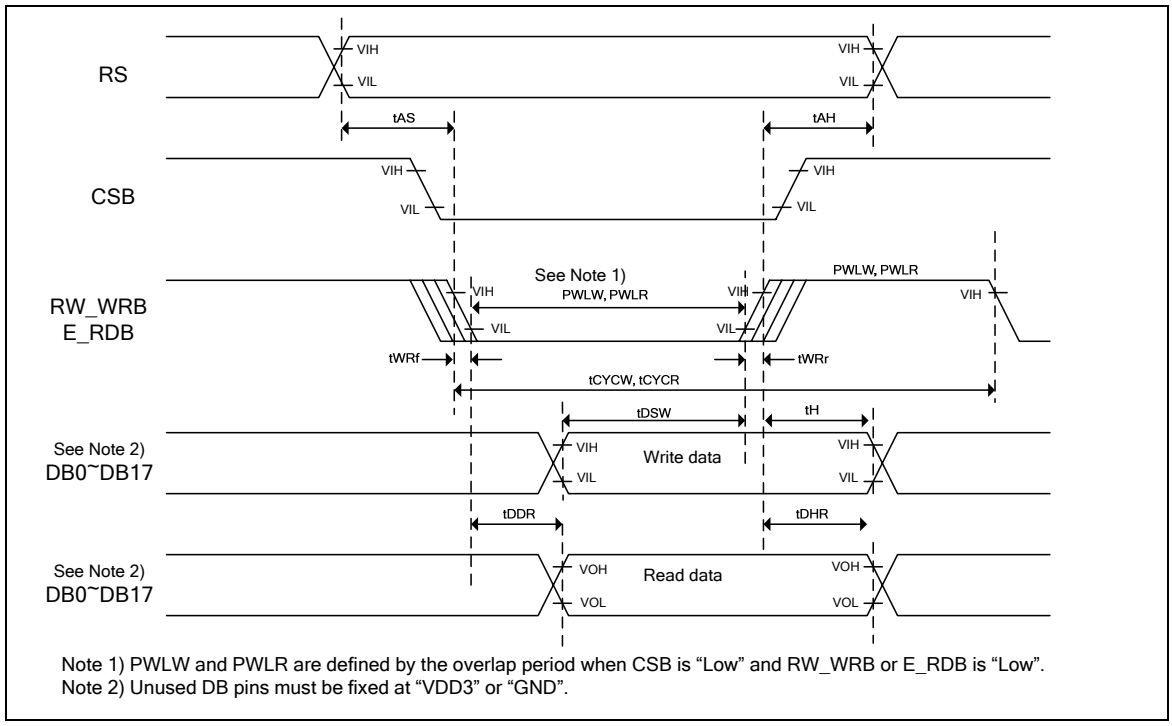


Figure 82 80-system bus interface operation

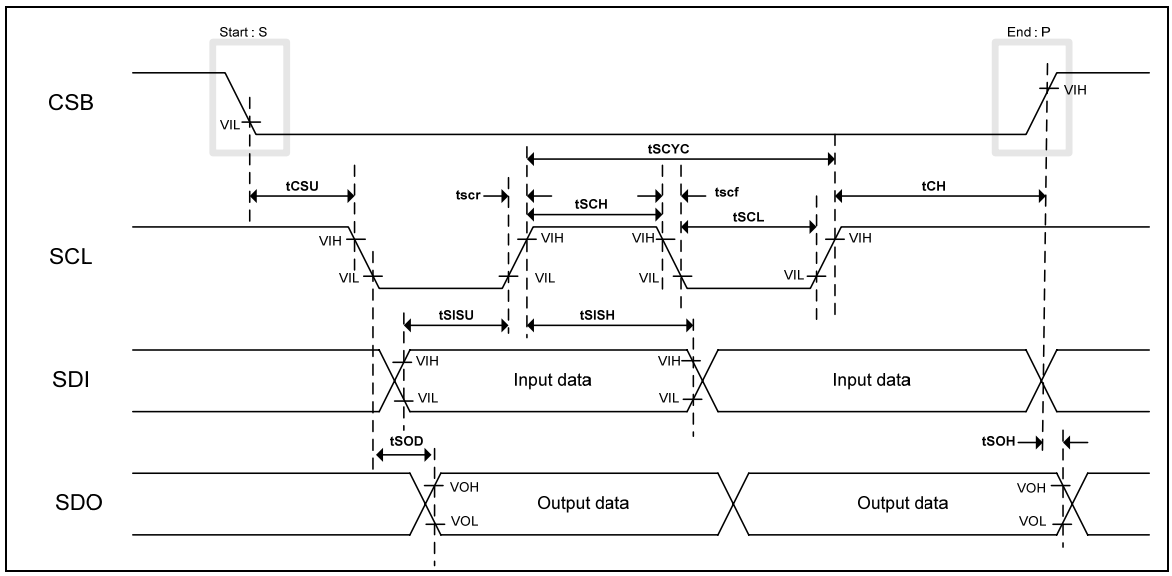


Figure 83 Serial Peripheral Interface operation

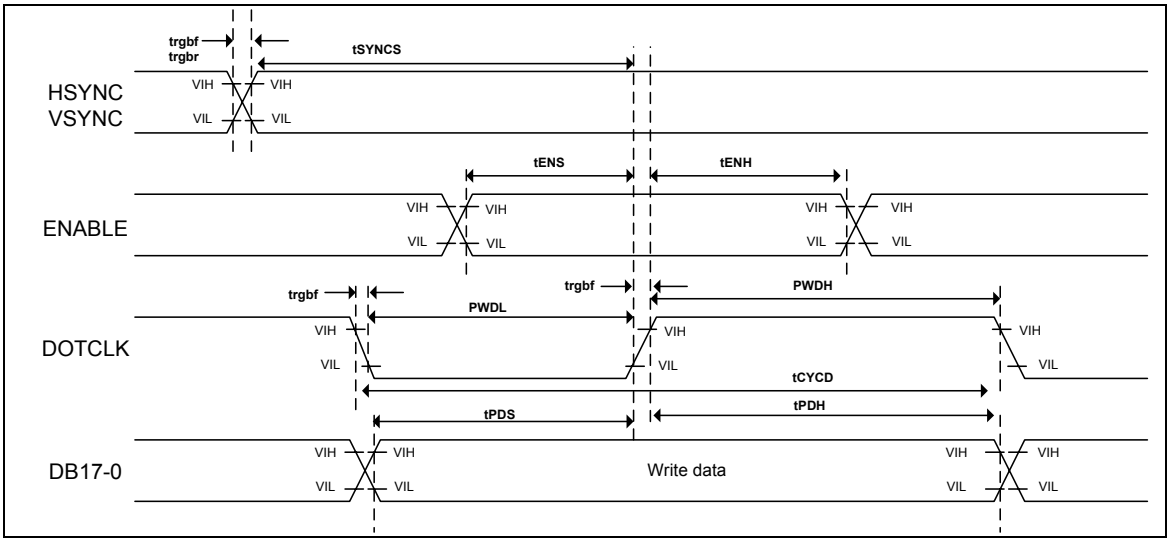


Figure 84 RGB interface operation

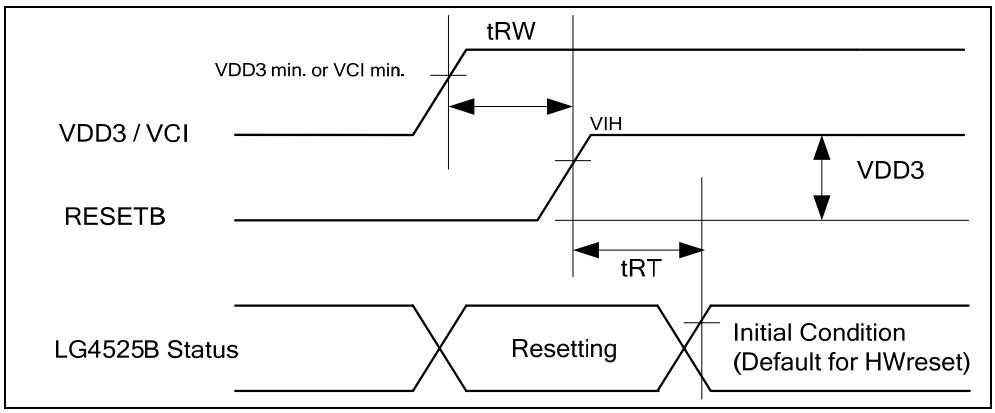


Figure 85 Reset timing when power supply is input

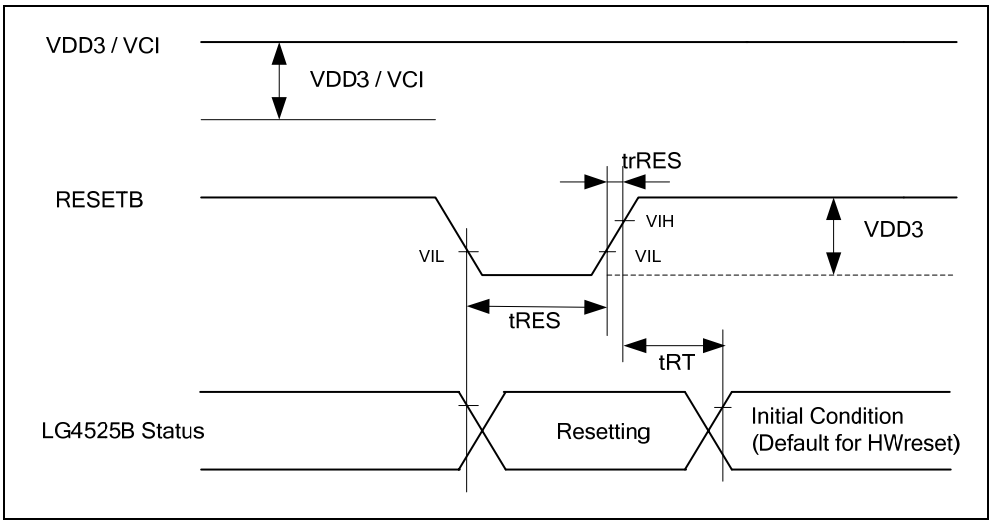


Figure 86 Reset timing during normal operation

Revision History

Ver.	Date	Revision Description	Revised by
0.10	2009.01.03	Preliminary release	S.H. Koh
0.20	2009.01.21	Revised Block Diagram and Pin Function : p.6 ~ 10	D.H. Kim
0.20	2009.01.21	Revised Power supply circuit connection and external elements : p.127 ~ 129	D.H. Kim
0.20	2009.01.21	Revised the descriptions of interface : p.7	S.H. Koh
0.30	2009.03.04	Revised <Figure 34 Data Transfer in Serial interface> : p.86	S.H. Koh
0.30	2009.03.04	Revised the Application of Power Supply Circuit : p.130 <Figure 73>	D.H. Kim
0.30	2009.03.04	Corrected the function of TEST_MODE<2> : p.10 <Table 5>	D.H. Kim