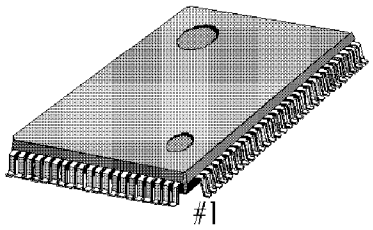
INTRODUCTION

The KS0086 is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology.
In case of segment driver, it can be interfaced as 1-bit serial or 4-bit parallel by controller. In case of common driver, dual type mode can be applicable. And in case of segment mode application, power down function saves power consumption.

100QFP-1420C



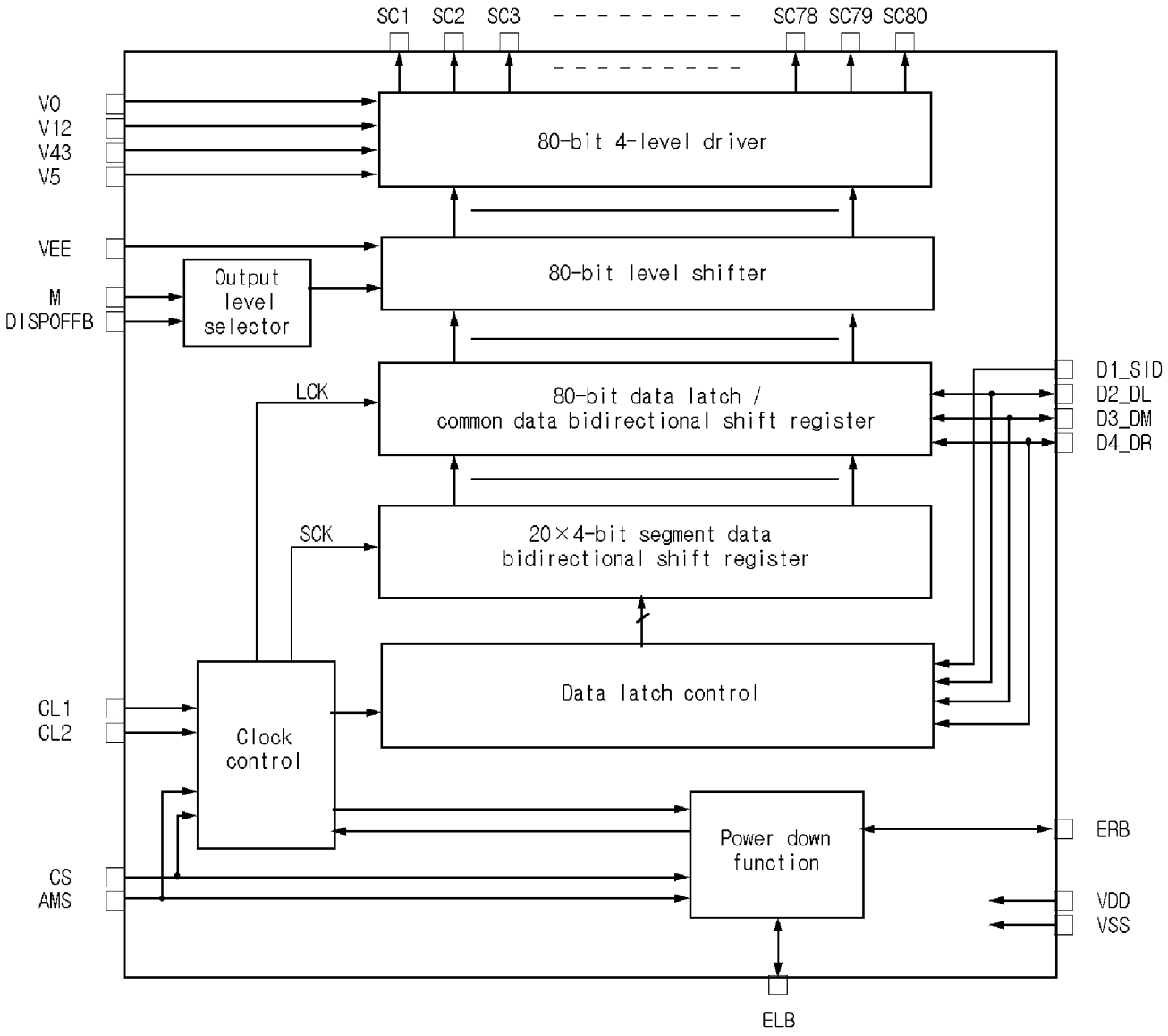
FEATURES

- Power supply voltage : +5V ± 10%, + 3V ± 10%
- Supply voltage for display : 6 ~ 28V (VDD-VEE)
- 4-bit parallel / 1-bit serial data processing (In segment mode)
- Single mode operation / Dual mode operation (In common mode)
- Power down function (In segment mode)
- Applicable LCD duty : 1/64 ~ 1/256
- Interface

Driver	
COM (cascade)	SEG (cascade)
KS0086	Another KS0086

- High voltage CMOS process
- 100 QFP and bare chip available

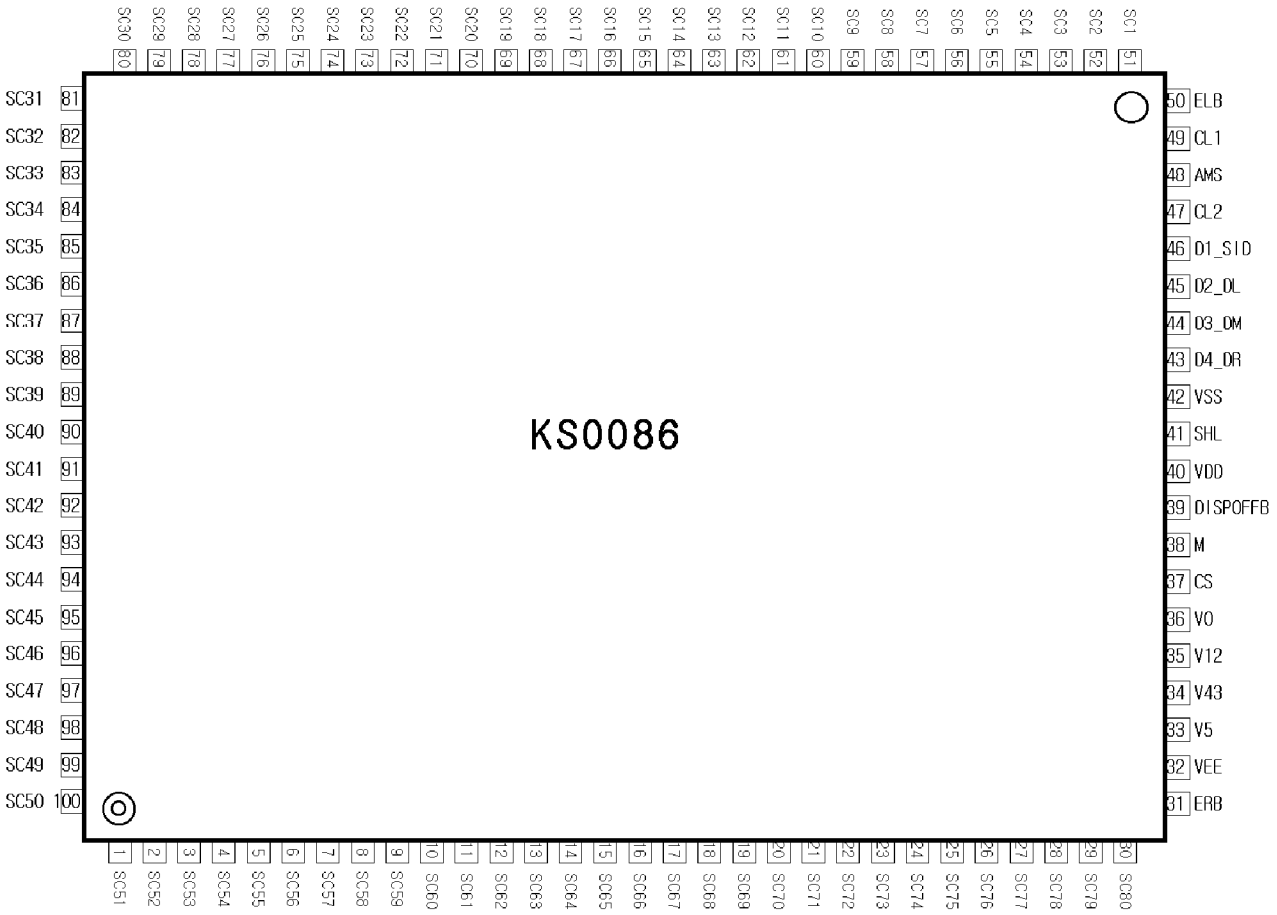
BLOCK DIAGRAM



BLOCK DESCRIPTION

Name	Function	COM/SEG
Clock control	Generates latch clock(LCK), shift clock(SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In case of common driver application, this block generates shift clock(LCK) for the common data bidirectional shift register.	COM/SEG
Data latch control	Determines the direction of segment data shift, and input data of each bidirectional shift register. In case of 4-bit segment data parallel transfer mode, data is shifted by 4-bit unit. In case of common driver application mode, data is transferred to the common data shift register directly, so this block is not work.	SEG
Power down function	Controls the clock enable state of current driver according to the input value of enable pin(ELB or ERB). If enable input value is "Low", every clock of the current driver is enabled and the clock control block works. But if enable input is "High", current driver is disabled and the input data value has no effect to the output level. So power consumption can be lowered.	SEG
Output level selector	Control the output voltage level according to the input control pin(M and DISPOFFB)(refer to PIN DESCRIPTION).	COM/SEG
20 × 4-bit segment data bidirectional shift register	Stores output data value by shifting the input values. When 1-bit serial interface mode application, all 80 shift clocks(SCK) are needed to store all the display data. But in case of 4-bit parallel transfer mode application, only 20 clocks makes the role. When common driver application mode, this block is not work.	SEG
80-bit data latch / common data bidirectional shift register	In case of segment driver application, the data from the 20x4-bit segment data shift register are latched for segment driver output. When single-type common driver application, 1-bit input data(from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. When dual-type common application mode, 80-bit register are divided by two blocks and controlled independently(refer to NOTE3).	COM/SEG
80-bit level shifter	Voltage level shifter block for high voltage part. the inputs of this block are logical voltage level and the outputs of this block are high voltage level value. And this value is input to the driver.	COM/SEG
80-bit 4-level driver	Selects the output voltage level according to the M and latched data value. If the data value is "High" the driver output is selected voltage level(V0 or V5), and in the reverse case the driver output value is non-selected level(V12 or V43). In case of segment driver application, non-selected output value is V2 or V3. And when common driver application, this value becomes V1 or V4.	COM/SEG

PIN CONFIGURATION



PIN DESCRIPTION

PIN (NO)	INPUT OUTPUT	NAME	DESCRIPTION	INTERFACE
VDD (40)	Power	Operating Voltage	Logical "High" input port(+5V ± 10%, +3V ± 10%)	Power
VSS (42)			0V (GND)	
VEE (32)		Driver Supply Voltage	Logical "Low" for high voltage part	
V0,V12,V43 V5 (33-36)	Input	LCD driver output voltage level	Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source(refer to NOTE 2).	Power
SC1 ~ SC80 (1-30, 51-100)	Output	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to NOTE 1).	LCD
CL2 (47)	Input	Data shift clock	Clock pulse input for the bidirectional shift register. • In case of segment driver application, the data is shifted to 20 x 4-bit segment data shift register at the falling edge of this clock pulse. The clock pulse, which was input when the enable bit (ELB/ERB) is not active condition, is invalid. • In case of common driver application, the data is shifted to 80-bit common data bidirectional shift register by the CL1 clock. So this clock pin is not used(Open or connect this to VDD)	Controller
M (38)	Input	Alternate signal for LCD driver output	Alternate signal input pin for LCD driving. Normal frame inversion signal is input to this pin.	Controller
CL1(49)	Input	Data latch clock	• In case of segment driver application, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block. • In case of common driver application, CL1 is used as shifting clock of common output data.	Controller
DISPOFFB (39)	Input	Display off control	Control input pin to fix the driver output(SC1~SC80) to V0 level, during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.	Controller
CS (37)	Input	COM/SEG mode dontrol	When CS = "Low", KS0086 is used as 80-bit segment driver. When CS = "High", KS0086 is set to 80-bit common driver.	-
AMS (48)	Input	Application mode select	According to the input value of the AMS and the CS pin, application mode of KS0086 is different as below.	Controller

CS	AMS	Application mode	COM/SEG
L	L	4-bit parallel interface mode	SEG
L	H	1-bit serial interface mode	
H	L	single-type application mode	COM
H	H	dual-type application mode	

PIN DESCRIPTION (continued)

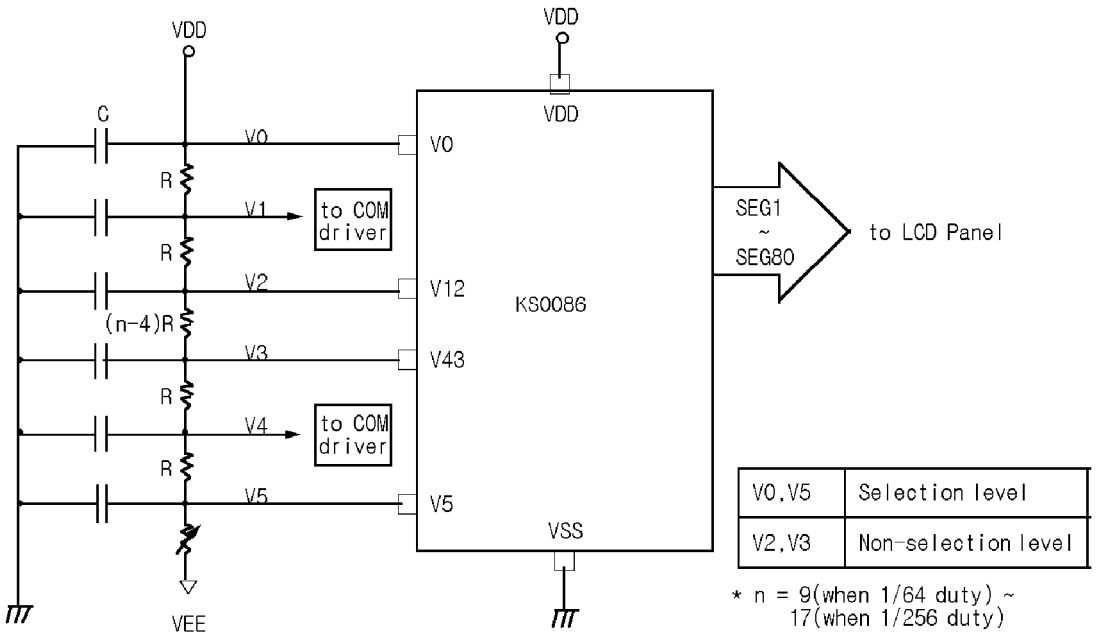
PIN (NO)	INPUT OUTPUT	NAME	FUNCITON	INTERFACE
D1_SID, D2_DL, D3_DM, D4_DR (43-46)	Input/ Output	Display data input / serial input data / left,right data input · output	• In case of segment driver application, these pins are used as 4-bit data input pin (when 4-bit parallel interface mode : AMS = "Low"), or D1_SID is used as serial data input pin and other pins are not used. (Open or connect this to VDD) (when 1-bit serial interface mode : AMS = "High"). • In case of common driver application, the data are shifted from D2_DL(D4_DR) to D4_DR(D2_DL), when single-type application mode (AMS = "Low"). In dual-type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4-DR (D2_DL). In each case the direction of data shift is determined by SHL input. (refer to NOTE 3, NOTE4)	controller
SHL (41)	Input	Shift direction control	When SHL = "Low", data is shifted from left to right When SHL = "High", the direction is reversed. (refer to NOTE 3)	-
ELB, ERB (50, 31)	Input/ Output	Enable data input/output	• In case of segment driver application, only when enable input (ELB or ERB) is "Low", the internal operation is enabled (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. (refer to NOTE 4) • In case of common driver application, power down function is not used. (Open)	-

NOTE 1. Output level control X:Don't care

M	Latched data	DISPOFFB	Output level (SC1 ~ SC80)	
			SEG Mode	COM Mode
L	L	H	V12(V2)	V12(V1)
L	H	H	V0	V5
H	L	H	V43(V3)	V43(V4)
H	H	H	V5	V0
X	X	L	V0	V0

NOTE 2. LCD driving voltage application circuit

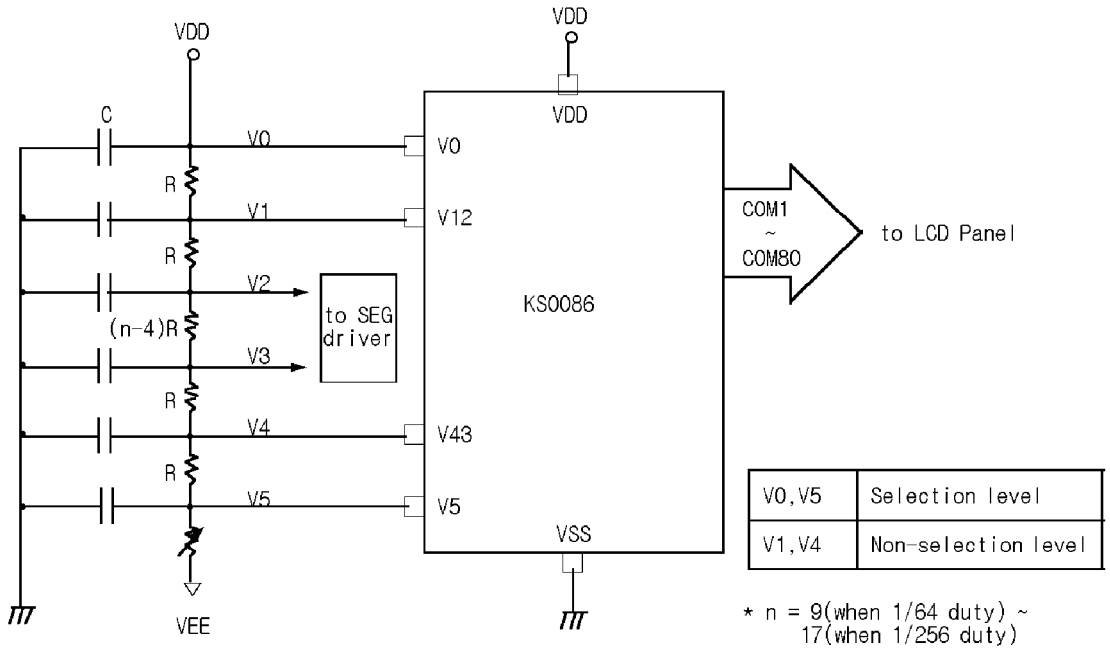
(1) Segment driver application (CS="Low")



V0,V5	Selection level
V2,V3	Non-selection level

* n = 9(when 1/64 duty) ~ 17(when 1/256 duty)

(2)Common driver application (CS="High")

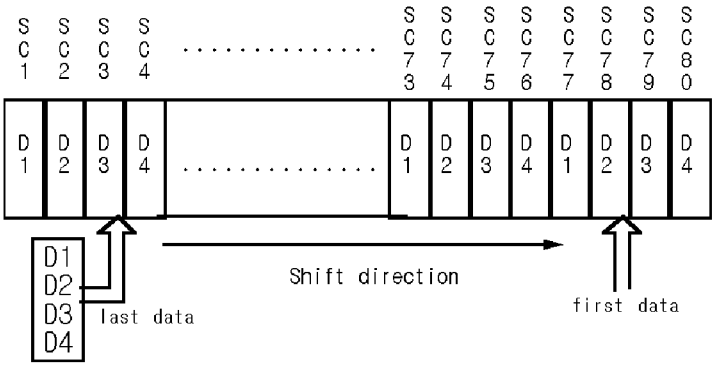
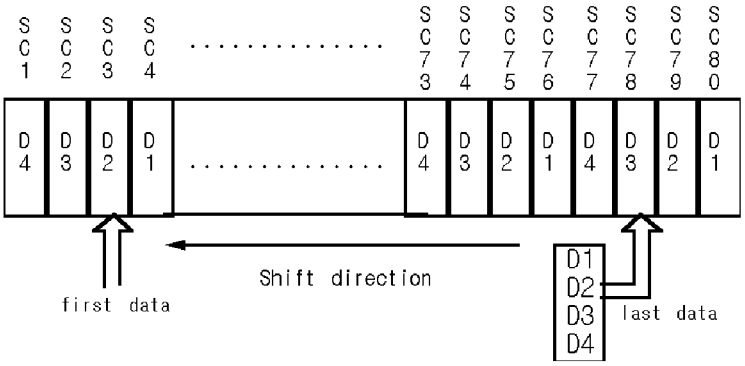
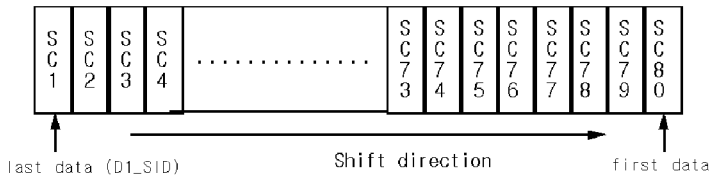
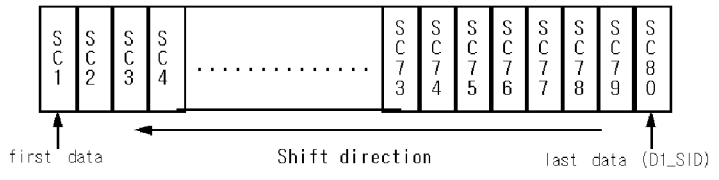


V0,V5	Selection level
V1,V4	Non-selection level

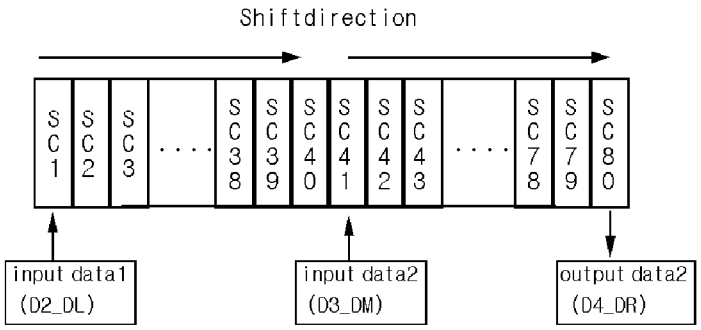
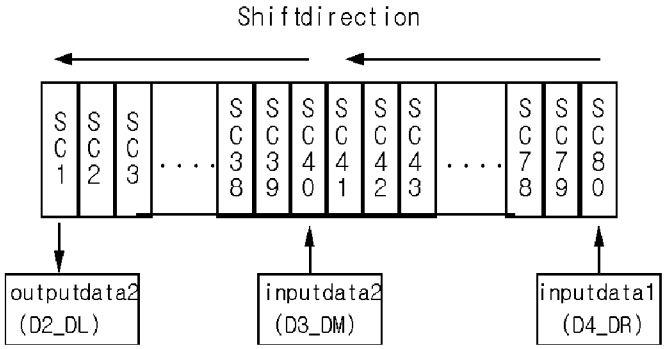
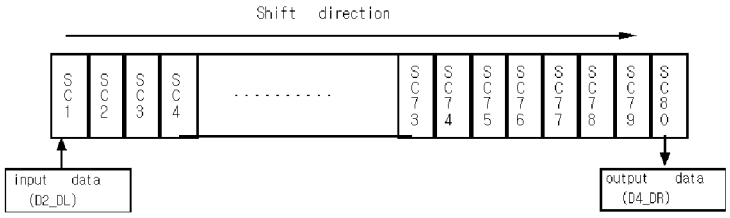
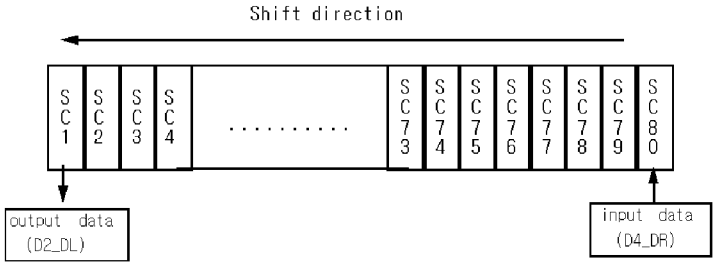
* n = 9(when 1/64 duty) ~ 17(when 1/256 duty)

NOTE 3. Data shift direction according to control signals

(1) When CS = "Low" (segment driver application)

AMS	SHL	Application mode	Data direction	Input pin
L	L	4-bit patallel data transfer mode (SEG)		D1_SID D2_DL, D3_DM, D4_DR
	H			
H	L	1-bit serial data transfer mode (COM)		D1_SID
	H			

(2) When CS="High" (common driver application)

AMS	SHL	Application mode	Data direction	Input pin
H	L	dual-type application mode (COM)		D2_DL, D3_DM,
	H			D4_DR, D3_DM
L	L	single-type application mode (COM)		D2_DL
	H			D4_DR

NOTE 4. Usage of data pins

COM/SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS = "L")	4-bit parallel interface mode (AMS = "L")	X	D1 (input 1)	D2 (input 2)	D3 (input 3)	D4 (input 4)
	1-bit serial interface mode (AMS = "H")	X	SID (input)	open		
COM (CS = "H")	single-typ application mode (AMS = "L")	L	open	DL (input)	open	DR (output)
		H		DL (output)		DR (input)
	dual-type application mode (AMS = "H")	L	open	DL (input 1)	DM (input 2)	DR (output 2)
		H		DL (output 2)	DM (input 2)	DR (input 1)

* X = dont't care

MAXIMUM ABSOLUTE LIMIT

Characteristics	Symbol	Value	Unit
OperatingVoltage	V_{DD}	-0.3 ~ +7.0	V
Driver Supply Voltage	V_{LCD}	0 ~ +30	
Input Voltage	V_{IN}	-0.3 ~ VDD +0.3	
Operating Temperature	T_{OPR}	-30 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +150	

Voltage greater than above may result in damage to the circuit.

ELECTRICAL CHARACTERISTICS
DC Characteristics

(1) SEGMENT DRIVER APPLICATION (VSS = 0V, Ta = -30 ~ +85°C)

Charateristics	Symbol	Condition		Min	Typ	Max	Unit
Operating Voltage 1	VDD	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = VDD-VEE		6	-	28	
Input Voltage (*1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output Voltage (*2)	V_{OH}	I_{OH} = -0.4mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input Leakage Current 1 (*1)	I_{LKG1}	V_{IN} = VDD ~ VSS		-10	-	10	μA
Input Leakage Current 2(*3)	I_{LKG2}	V_{IN} = VDD ~ VEE		-25	-	25	
On Resistance (*4)	R_{ON}	I_{ON} = 100μA		-	2	4	KΩ
Supply Current (*5)	I_{STB}	f_{CL1} = 32KHz, f_M = 80Hz	VSS	-	-	100	μA
	I_{DD}		VDD=5V	-	-	5	mA
			VDD=3V	-	-	2	
	I_{EE}		VDD=5V	-	-	500	μA

NOTES
(*1) Applied to CL1, CL2, ELB, ERB, D1_SID ~ D4_DR, SHL, DISPOFFB, M, CS, AMS
(*2) ELB, ERB
(*3) V0, V12, V43, V5
(*4) V_{LCD}=VDD-VEE, V0=VDD=5V, V5=VEE=-23V
V12=VDD-2/n(V_{LCD}), V43=VEE+2/n(V_{LCD}), n = 17 (1/256 duty, 1/17 bias)
(*5) V0=VDD, V12=1.71V(VDD=5V) or -0.06 V(VDD=3V),
V43=-19.71V(VDD=5V) or -19.94V(VDD=3V), V5=VEE=-23V, no-load condition (1/256 duty, 1/17 bias)
4-bit parallel interface mode
ISTBY : VDD=5V, fCL2=5.12MHz, SHL=VSS, DISPOFFB=VDD, M=VSS, display data pattern = 0000
IDD : VDD=3V, fCL2=4MHz, display data pattern = 0101
VDD=5V, fCL2=5.12MHz, display data pattern = 0101
IEE : VDD=5V, fCL2=5.12MHz, display data pattern = 0101, VEE

DC Characteristics (continued)

(2) COMMON DRIVER APPLICATION (VSS = 0V, Ta = -30 ~ +85°C)

Charateristics	Symbol	Condition		Min	Typ	Max	Unit
Operating Voltage 1	VDD	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = VDD-VEE		6	-	28	
Input Voltage (*1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output Voltage (*2)	V_{OH}	I_{OH} = -0.4mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input Leakage Current 1 (*1)	I_{LKG1}	V_{IN} = VDD ~ VSS		-10	-	10	μA
Input Leakage Current 2(*3)	I_{LKG2}	V_{IN} = VDD ~ VEE		-25	-	25	
On Resistance (*4)	R_{ON}	I_{ON} = 100μA		-	2	4	KΩ
Supply Current (*5)	I_{STB}	f_{CL1} = 32KHz, f_M = 80Hz	VSS pin	-	-	100	μA
	I_{DD}		VDD=5V	-	-	200	
			VDD=3V	-	-	120	
	I_{EE}		VDD=5V	-	-	150	

NOTES
(*1) Applied to CL1, D2_DL1~D4-DR, SHL, DISPOFFB, M, CS, AMS
(*2) D2_DL1,D4_DR pin
(*3) V0, V12, V43, V5 pin
(*4) V_{LCD}=VDD-VEE, V0=VDD=5V, V5=VEE=-23V
V12=VDD-1/n(V_{LCD}), V43=VEE+1/n(V_{LCD}), n = 17(1/256 duty, 1/17 bias)
(*5) V0=VDD, V12=3.35V(VDD=5V) or 1.47V(VDD=3V),
V43=-21.35V(VDD=5V) or -21.47V(VDD=3V), V5=VEE=-23V, no-load condition (1/256 duty, 1/17 bias)
single-type mode operation.
ISTBY : VDD=5V, SHL=VSS, DISPOFFB=VDD, M=VSS, display data pattern = 0000
IDD : VDD=3V, display data pattern = 0101
VDD=5V, display data pattern = 0101
IEE : VDD=5V, display data pattern = 0101, VEE

AC Characteristics

(1) SEGMENT DRIVER APPLICATION

(VSS = 0V, Ta = -30 ~ +85°C)

Characteristics	Symbol	Conditions	VDD=5V ± 10%			VDD=3V ± 10%			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
Clock Cycle Time	t_{CY}	Duty = 50%	125	-	-	250	-	-	ns
Clock Pulse Width	t_{WCK}	-	45	-	-	95	-	-	
Clock Rise/Fall Time	t_R/t_F	-	-	-	30	-	-	30	
Data Set-Up Time	t_{DSU}	-	30	-	-	65	-	-	
Data Hold Time	t_{DH}	-	30	-	-	65	-	-	
Clock Set-Up Time	t_{CSU}	-	80	-	-	120	-	-	
Clock Hold Time	t_{CH}	-	80	-	-	120	-	-	
Propagation Delay Time	t_D	ELB Output	-	-	60	-	-	125	
		ERB Output			60			125	
ELB, ERB Set-Up Time	t_{SU}	ELB Input	30	-	-	65	-	-	
		ERB Input	30			65			
DISPOFFB Low Pulse Time	t_{WL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB Clear Time	t_{CD}	-	100	-	-	100	-	-	ns
M- OUT Propagation Delay Time	t_{PD1}	C_L = 15pF	-	-	1.0	-	-	1.2	µs
CL1-OUT Propagation Delay Time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB-OUT Propagation Delay Time	t_{PD3}		-	-	1.0	-	-	1.2	

AC Characteristics (continued)

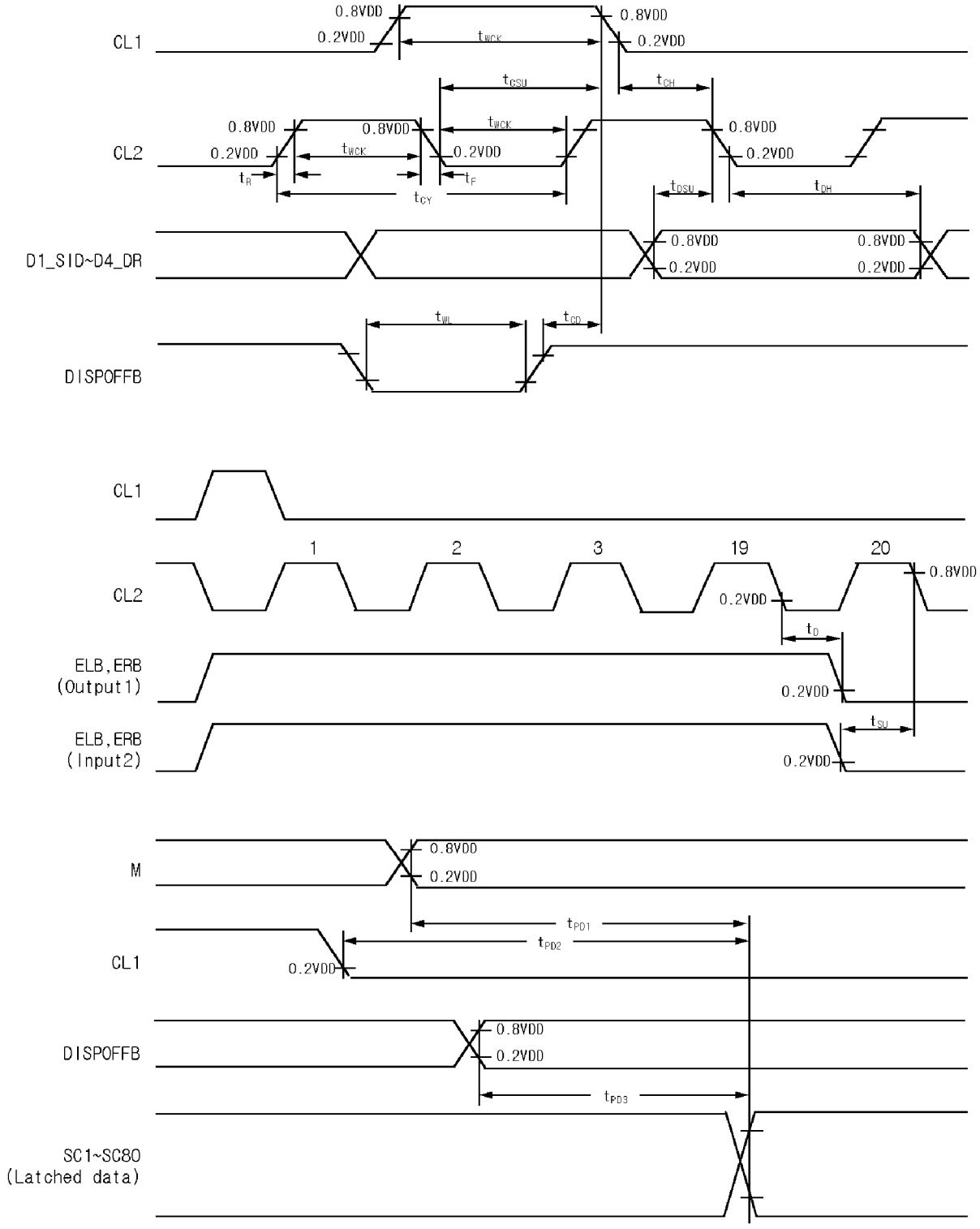
(2) COMMON DRIVER APPLICATION

(VSS = 0V, Ta = -30 ~ +85°C)

Characteristics	Symbol	Conditions	VDD=5V ± 10%			VDD=3V ± 10%			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
Clock Cycle Time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock Pulse Width	t_{WCKH}	-	45	-	-	95	-	-	
Clock Rise/Fall Time	t_R/t_F	-	-	-	50	-	-	50	
Data Set-Up Time	t_{DSU}	-	30	-	-	65	-	-	
Data Hold Time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB Low Pulse Width	t_{WL}	-	1.2	-	-	1.2	-	-	μs
DISPOFFB Clear Time	t_{CD}	-	100	-	-	100	-	-	ns
Output Delay Time	t_{DL}	C_L = 15pF	-	-	200	-	-	250	μs
M- OUT Propagation Delay Time	t_{PD1}		-	-	1.0	-	-	1.2	
CI1-OUT Propagation Delay Time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB-OUT Propagation Delay Time	t_{PD3}		-	-	1.0	-	-	1.2	

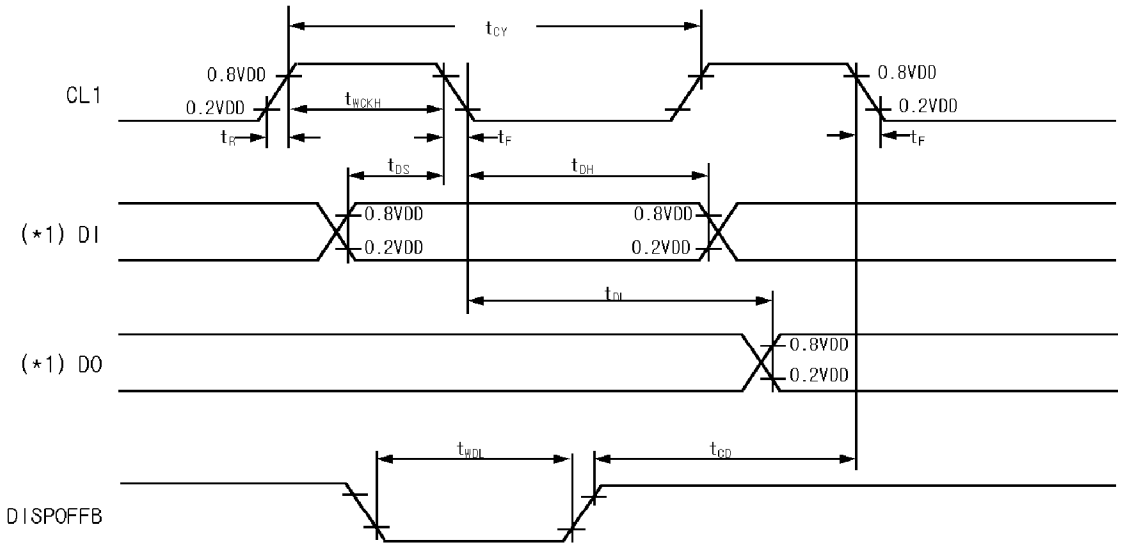
AC Characteristics (continued)

(3) SEGMENT DRIVER APPLICATION TIMING

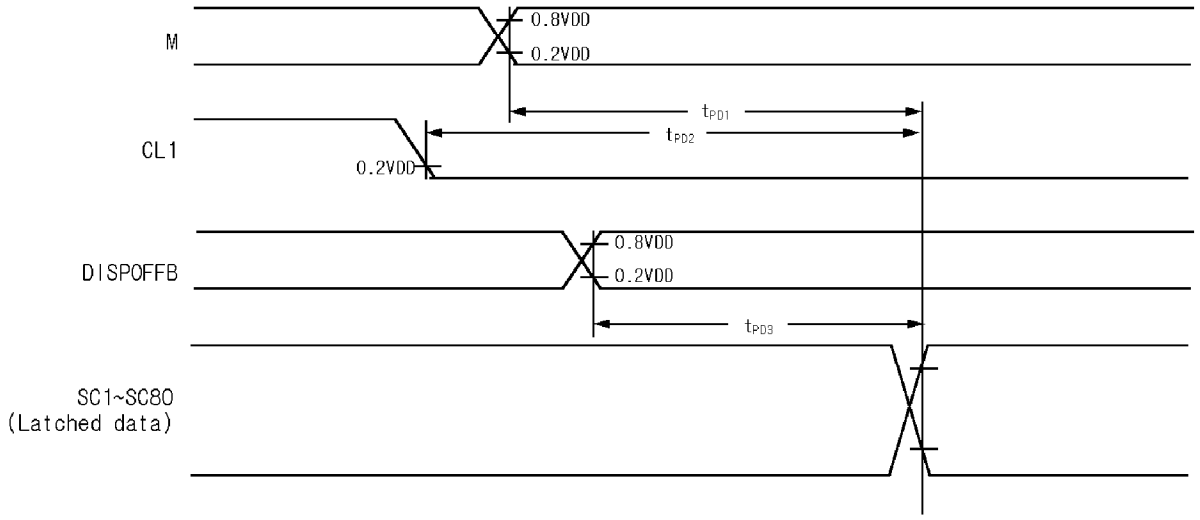


AC Characteristics (continued)

(4) COMMON DRIVER APPLICATION TIMING



(*1) When single-type interface mode
DI => D2_DL(SHL="L"), D4_DR(SHL="H")
DO => D4_DR(SHL="L"), D2_DL(SHL="H")
When dual-type interface mode
DI => D2_DL and D3_DM(SHL="L"), D4_DR and D3_DM(SHL="H")
DO => D4_DR(SHL="L"), D2_DL(SHL="H")

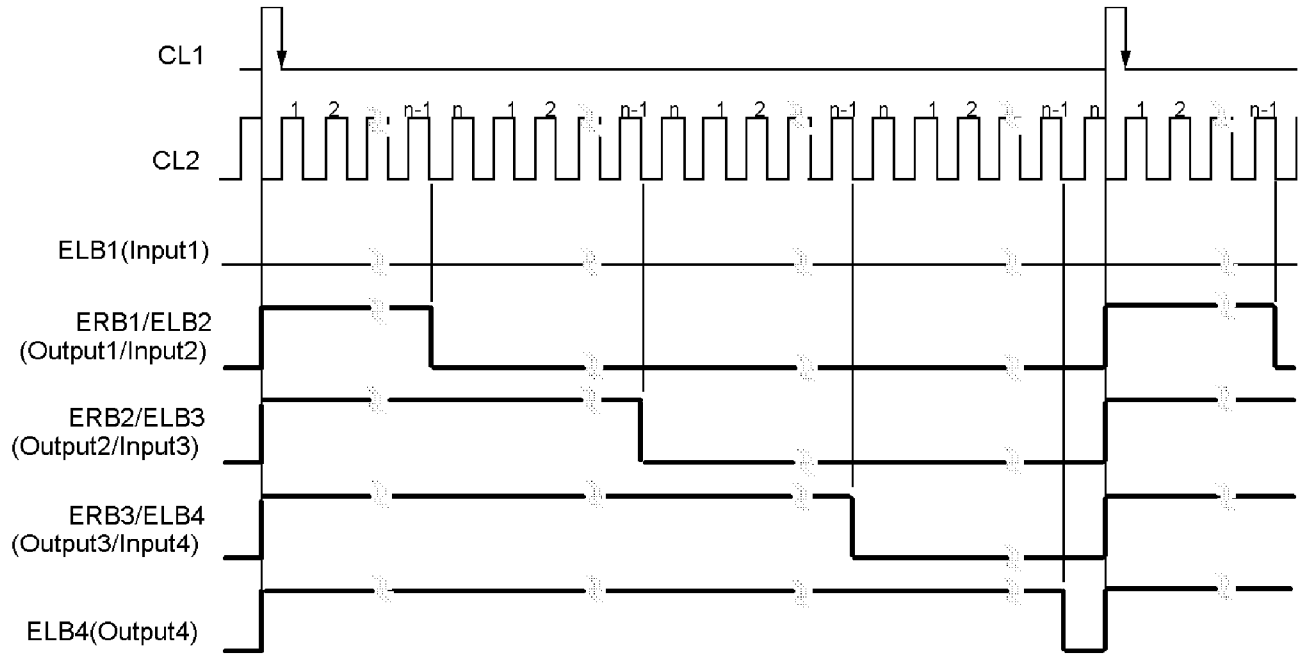


POWER DOWN FUNCTION

In order to reduce the power consumption, in case of cascade connection of segment mode drivers, KS0086 has a “power down function”.

SHL	Enable input	Enable output	Current driver staus	The other drivers staus
L	ERB	ELB	While ERB = “Low”, current driver is enabled.	Disabled
H	ELB	ERB	While ELB = “Low”, current driver is enabled.	Disabled

* In case of common driver application, power down function does not work.

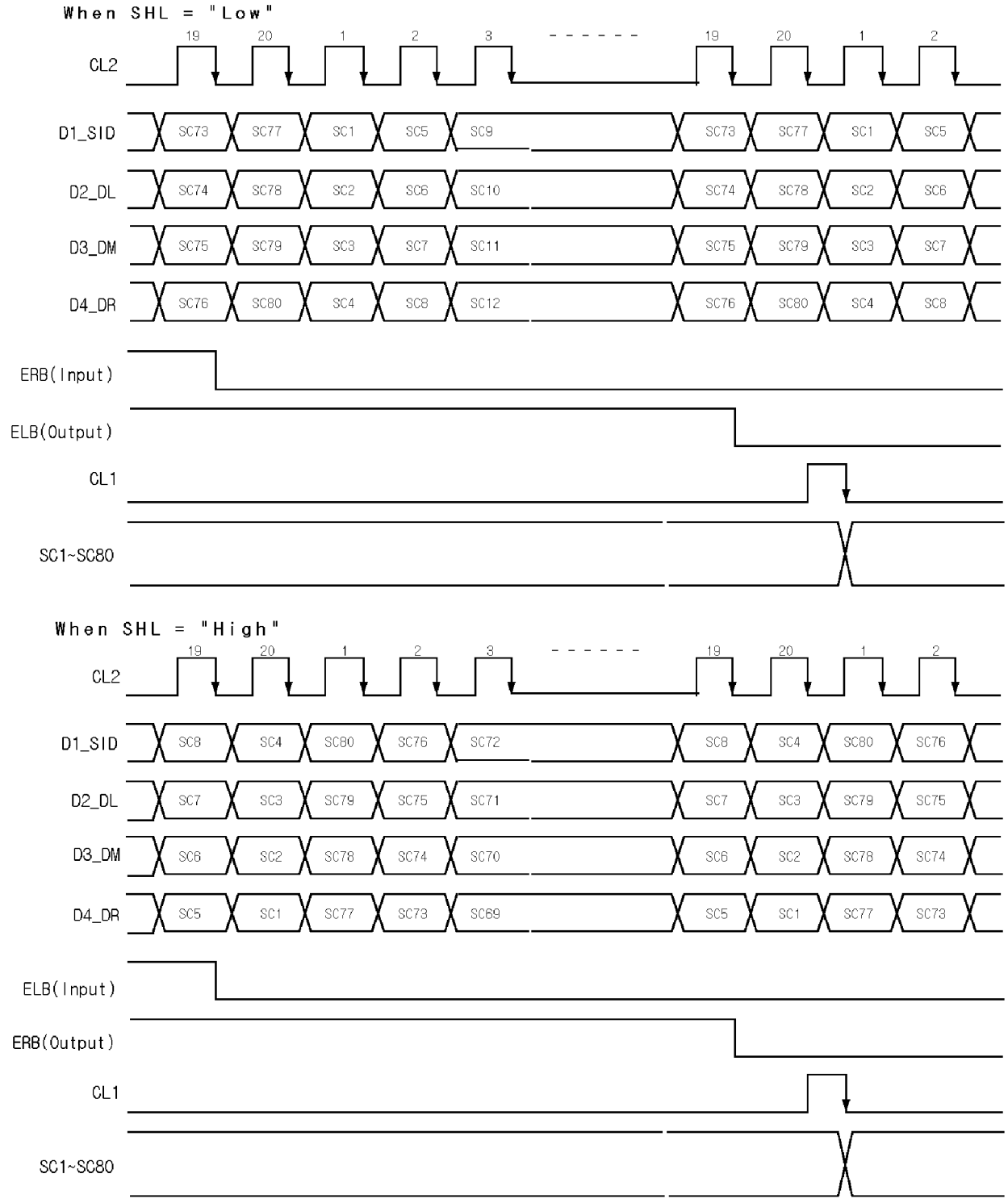


NOTE 1) SHL = "High" (ELB = Input, ERB = Output)
Current KS0086's ERB must be connected to the next KS0086's ELB.

2) When 4-bit parallel interface mode : n = 20
When 1-bit serial interface mode : n = 80

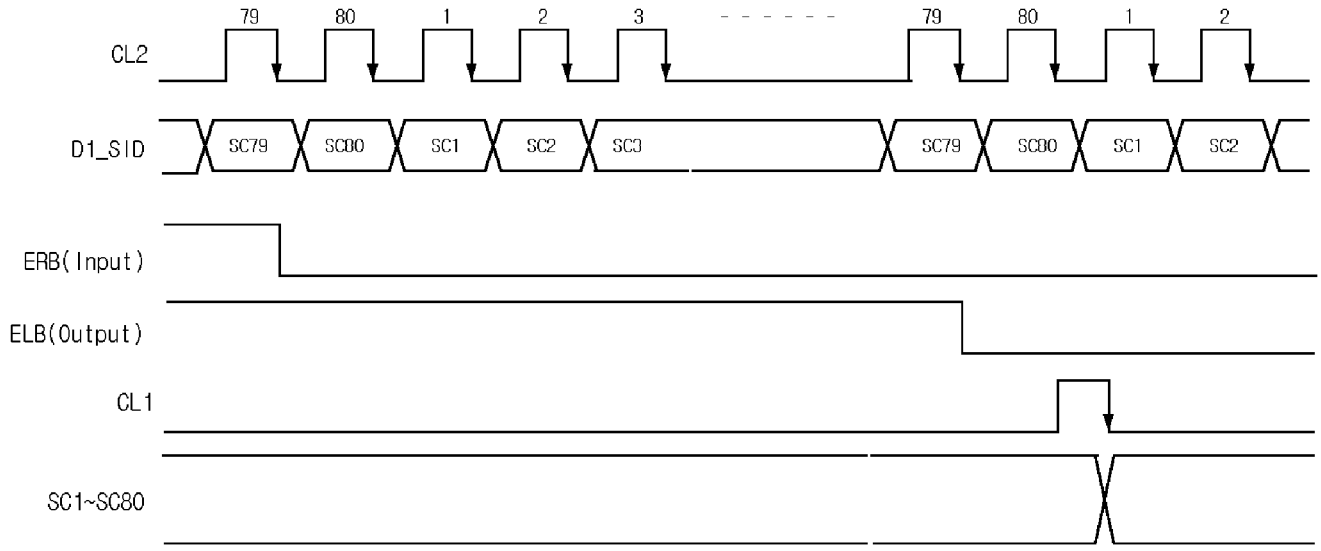
TIMING DIAGRAM

(1) 4-bit PARALLEL MODE INTERFACE SEGMENT DRIVER

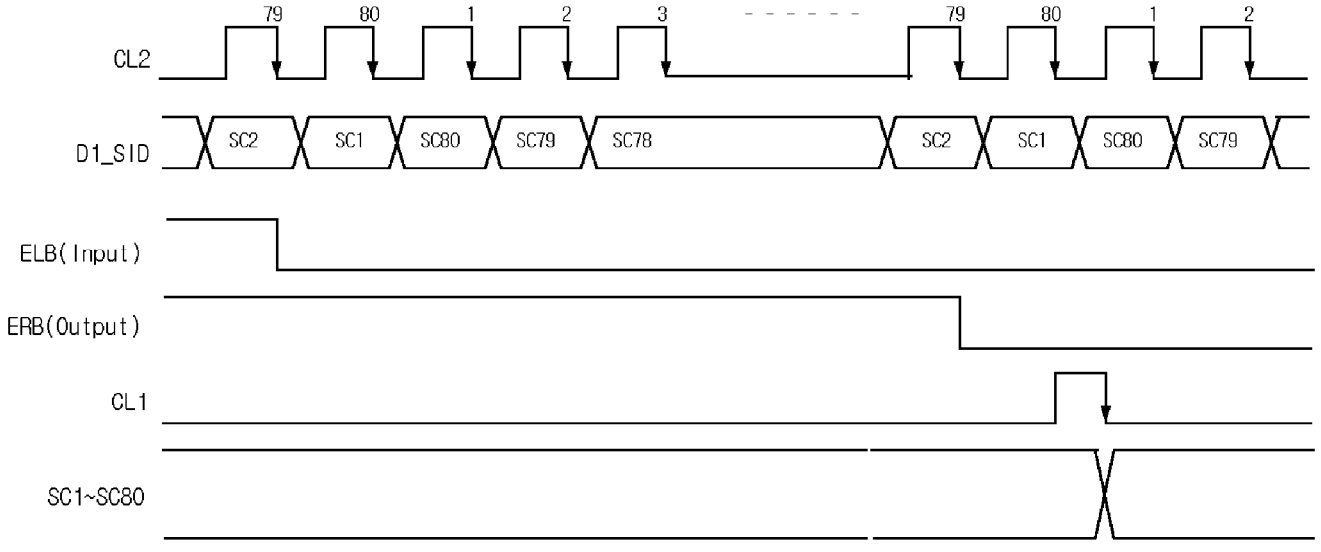


(2) 1-BIT SERIAL MODE INTERFACE SEGMENT DRIVER

When SHL = "Low"

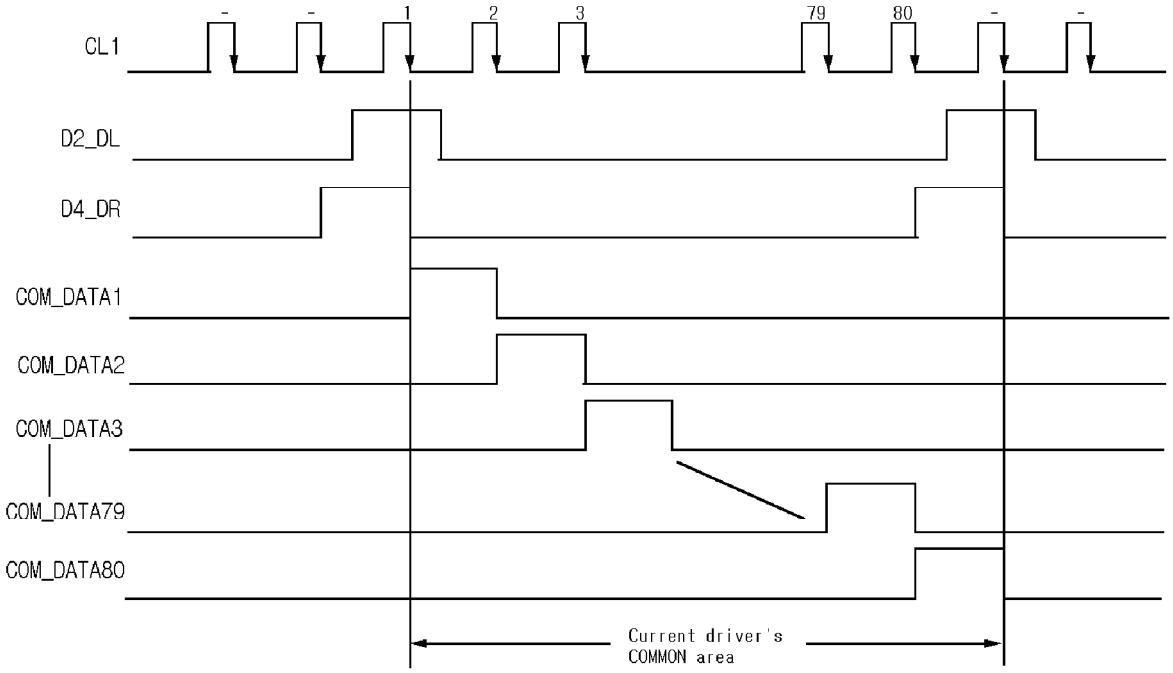


When SHL = "High"

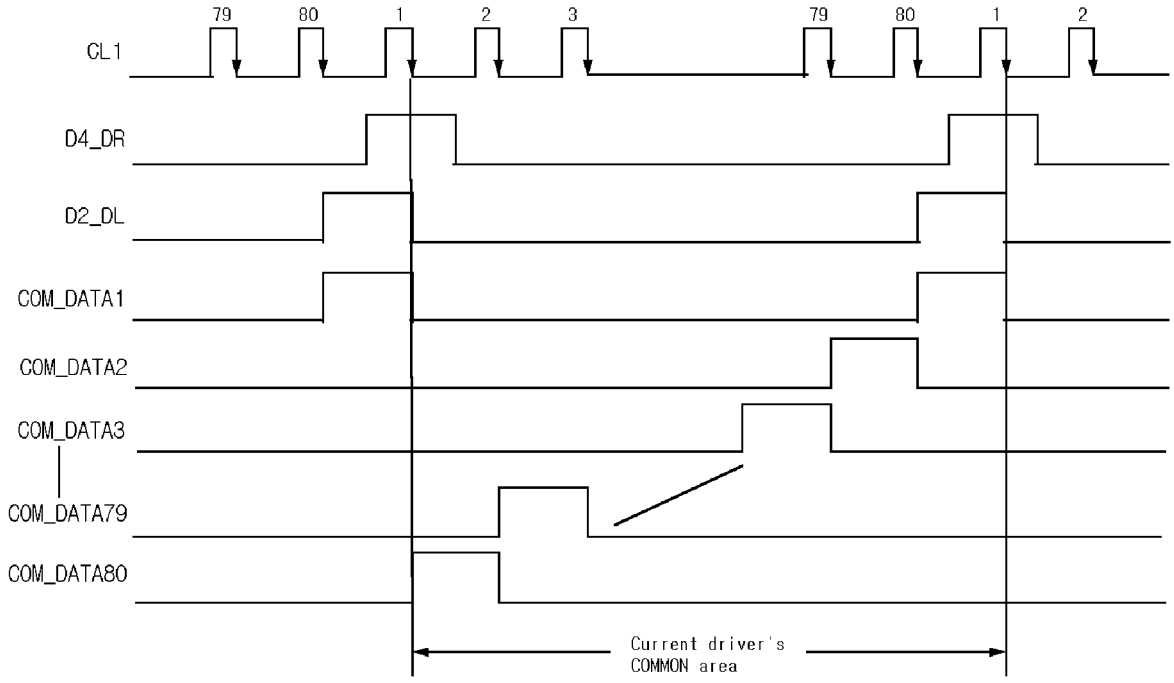


(3) SIGNAL-TYPE INTEFACE MODE COMMON DRIVER

When SHL = "Low"

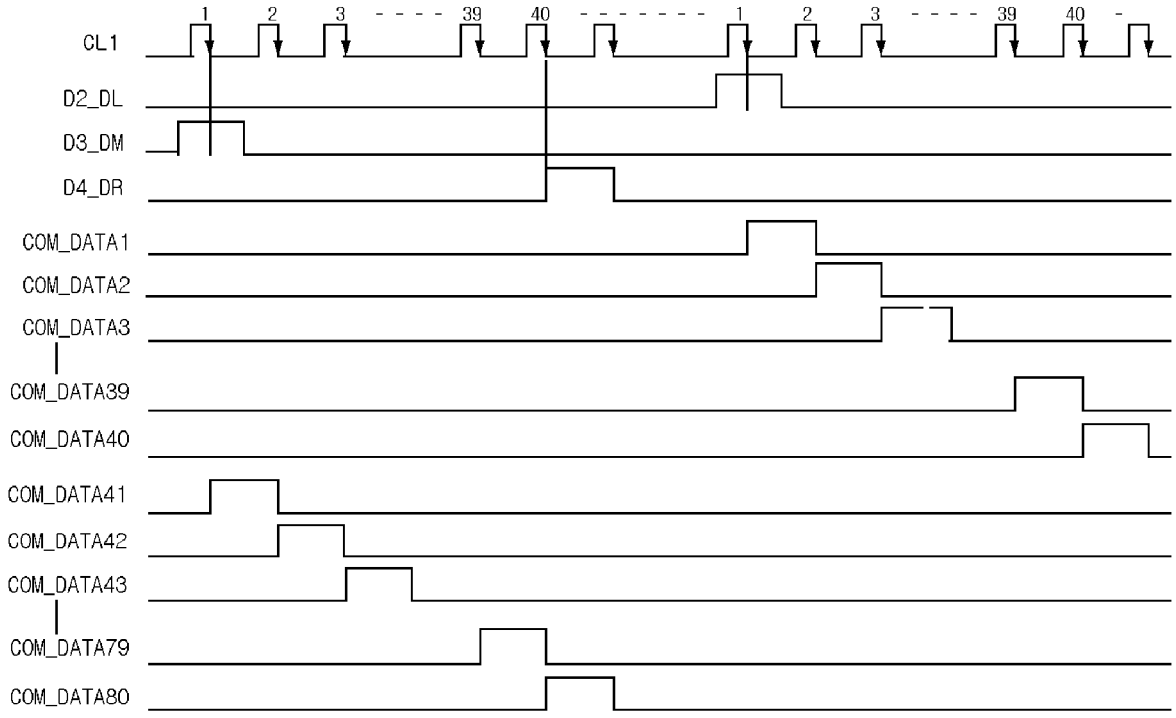


When SHL = "High"

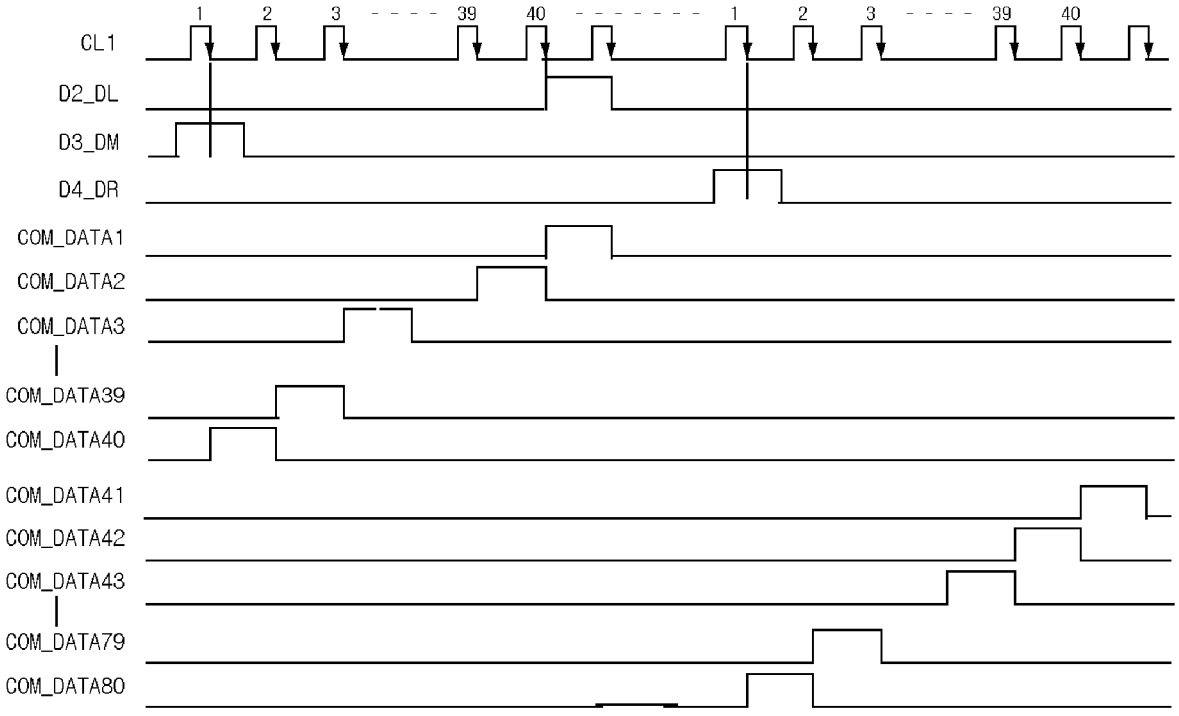


(4) DUAL-TYPE INTERFACE MODE COMMON DRIVER

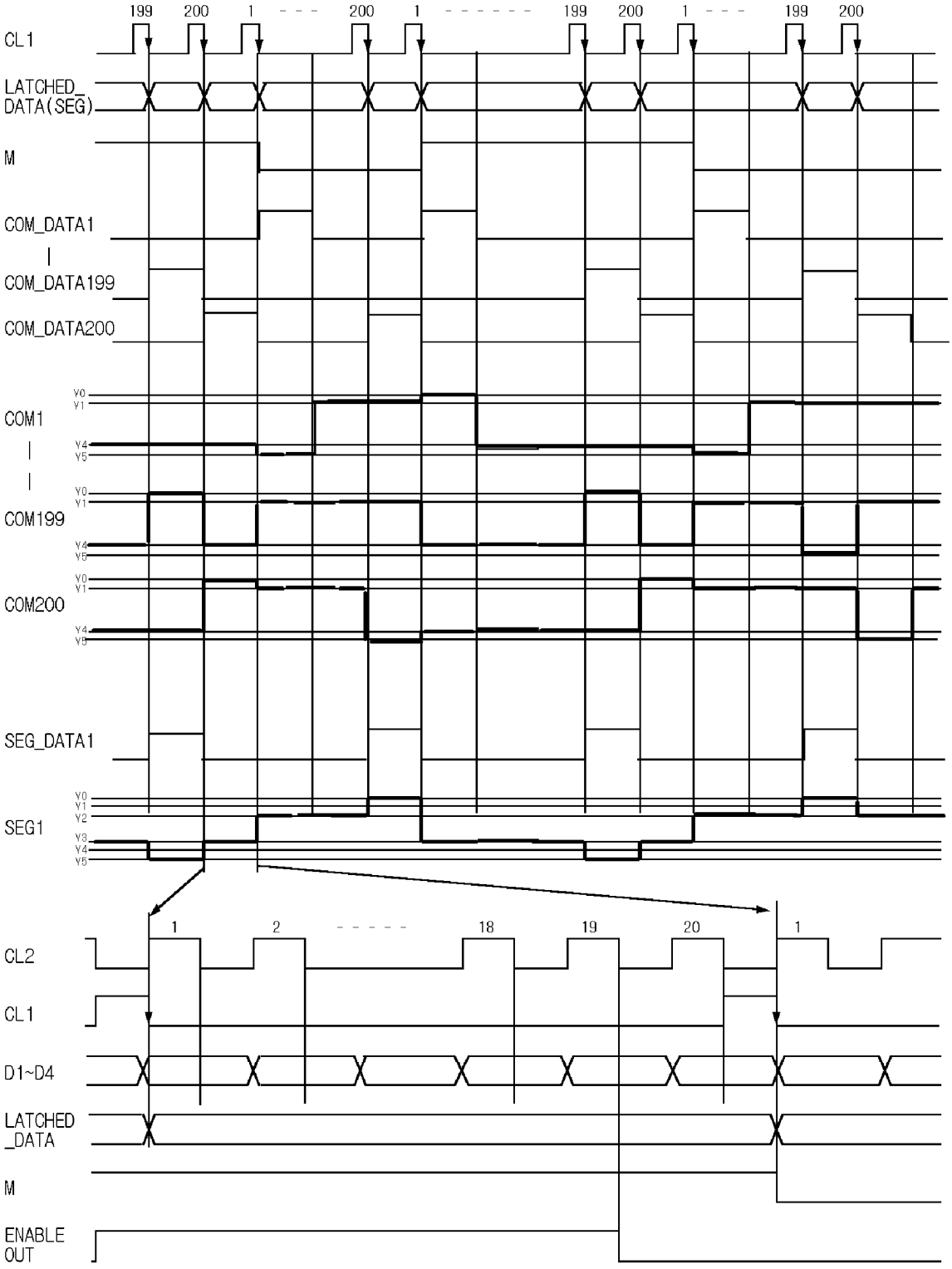
When SHL = "Low"



When SHL = "High"

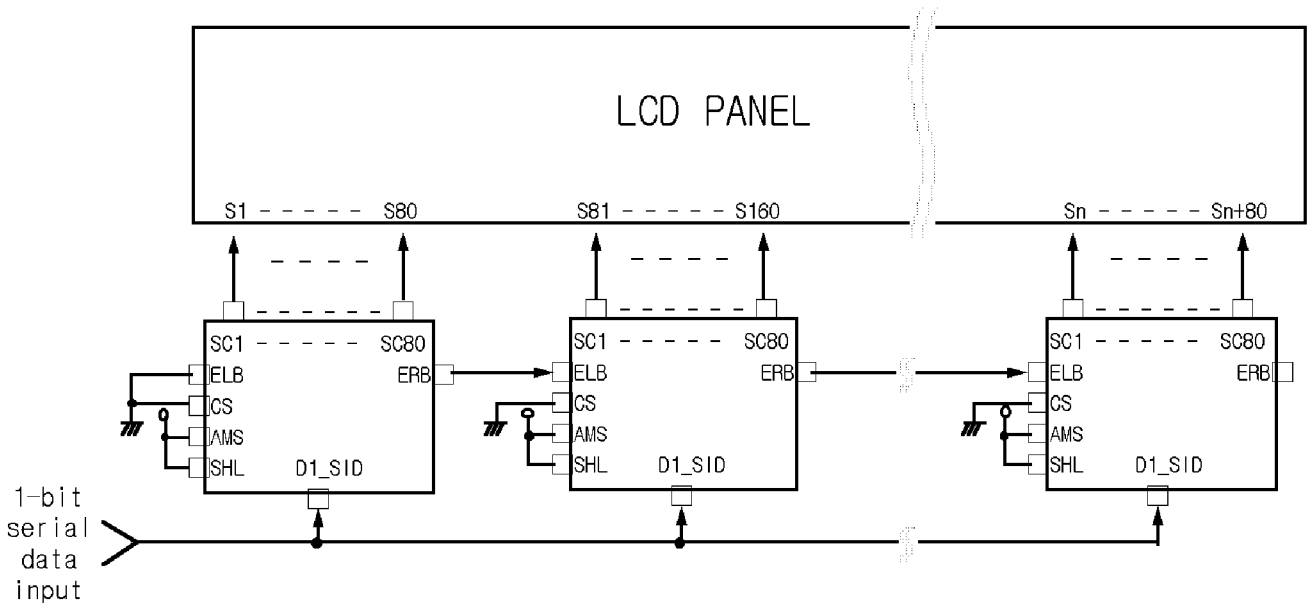


(5) COMMON / SEGMENT DRIVER TIMING (1 / 200 DUTY)

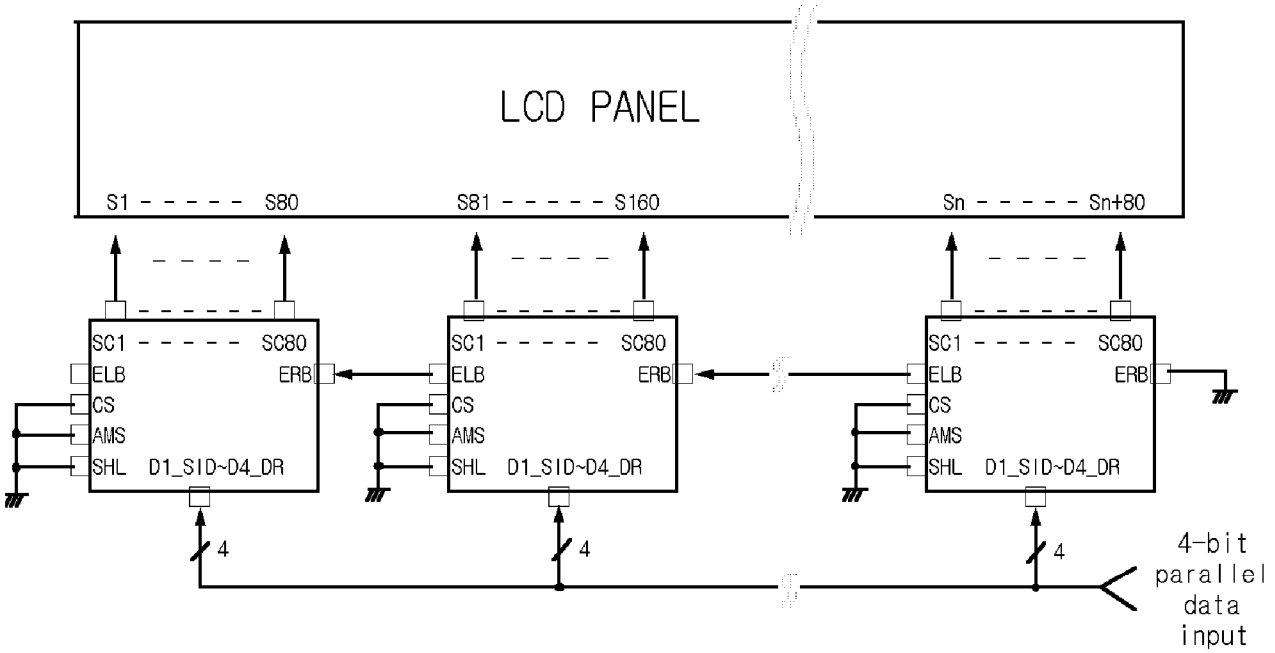


APPLICATION INFORMATION

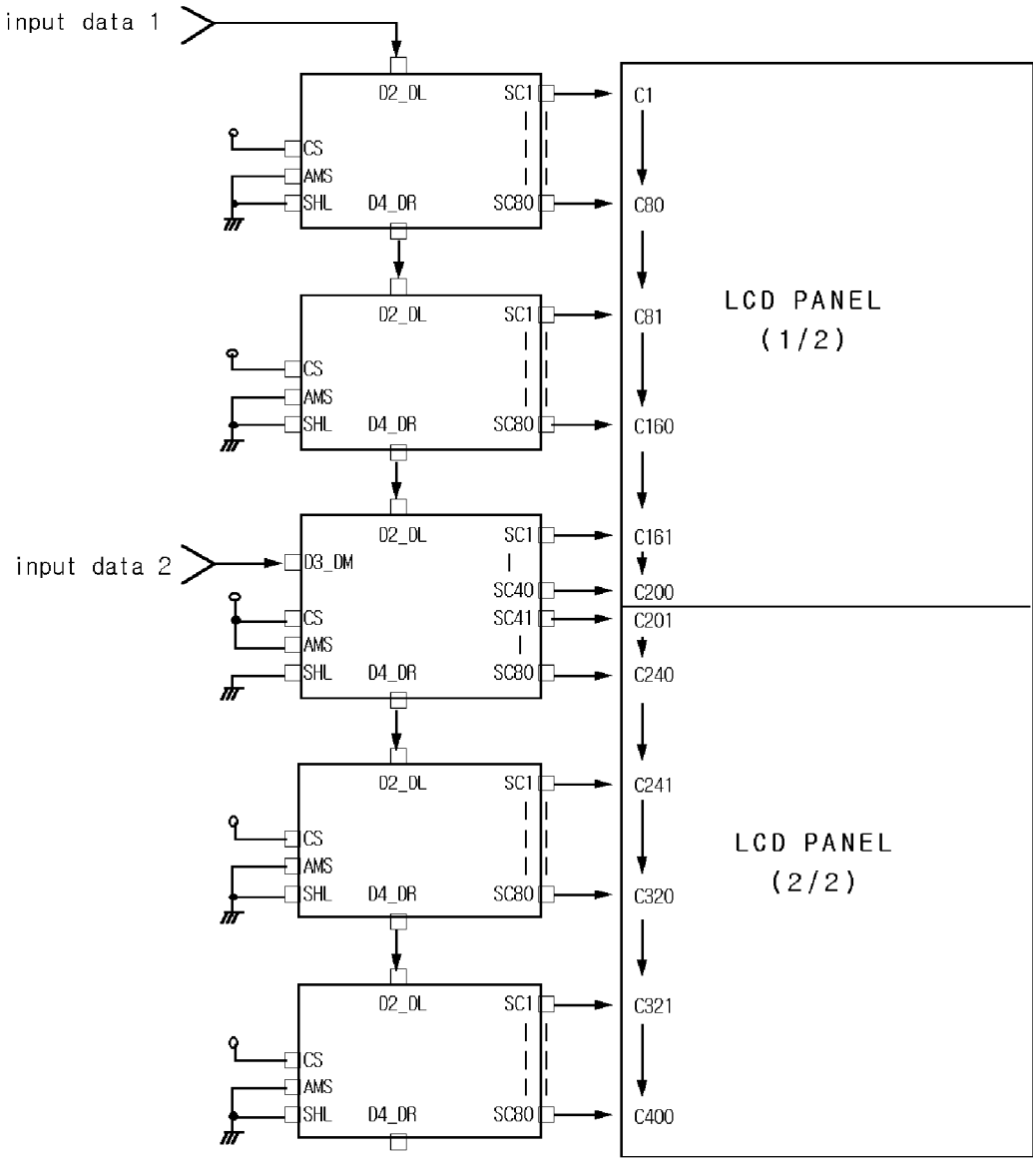
(1) 1-BIT SERIAL INTERFACE MODE (80-CH SEGMENT DRIVER)



(2) 4-BIT PARALLEL INTERFACE MODE (80-CH SEGMENT DRIVER)



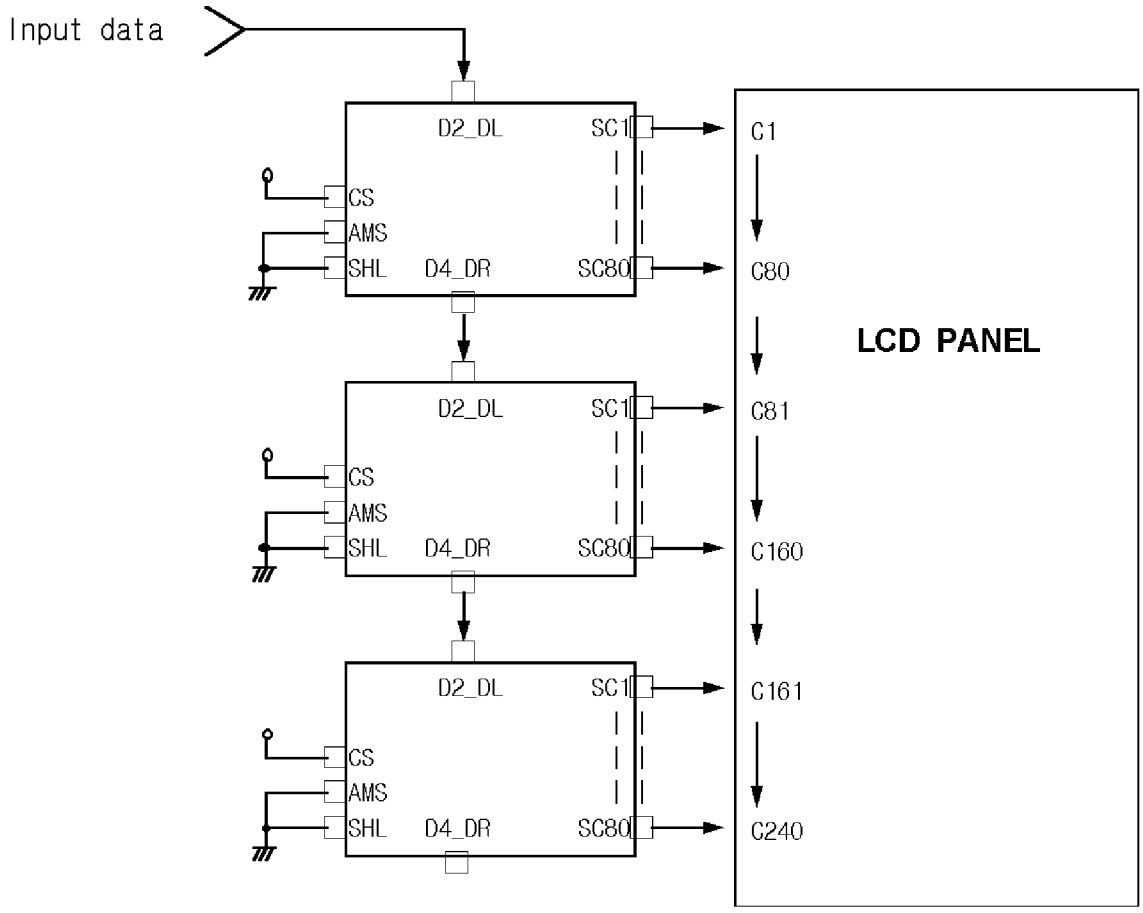
(3) DUAL-TYPE INTERFACE MODE (40CH + 40CH COMMON DRIVER)

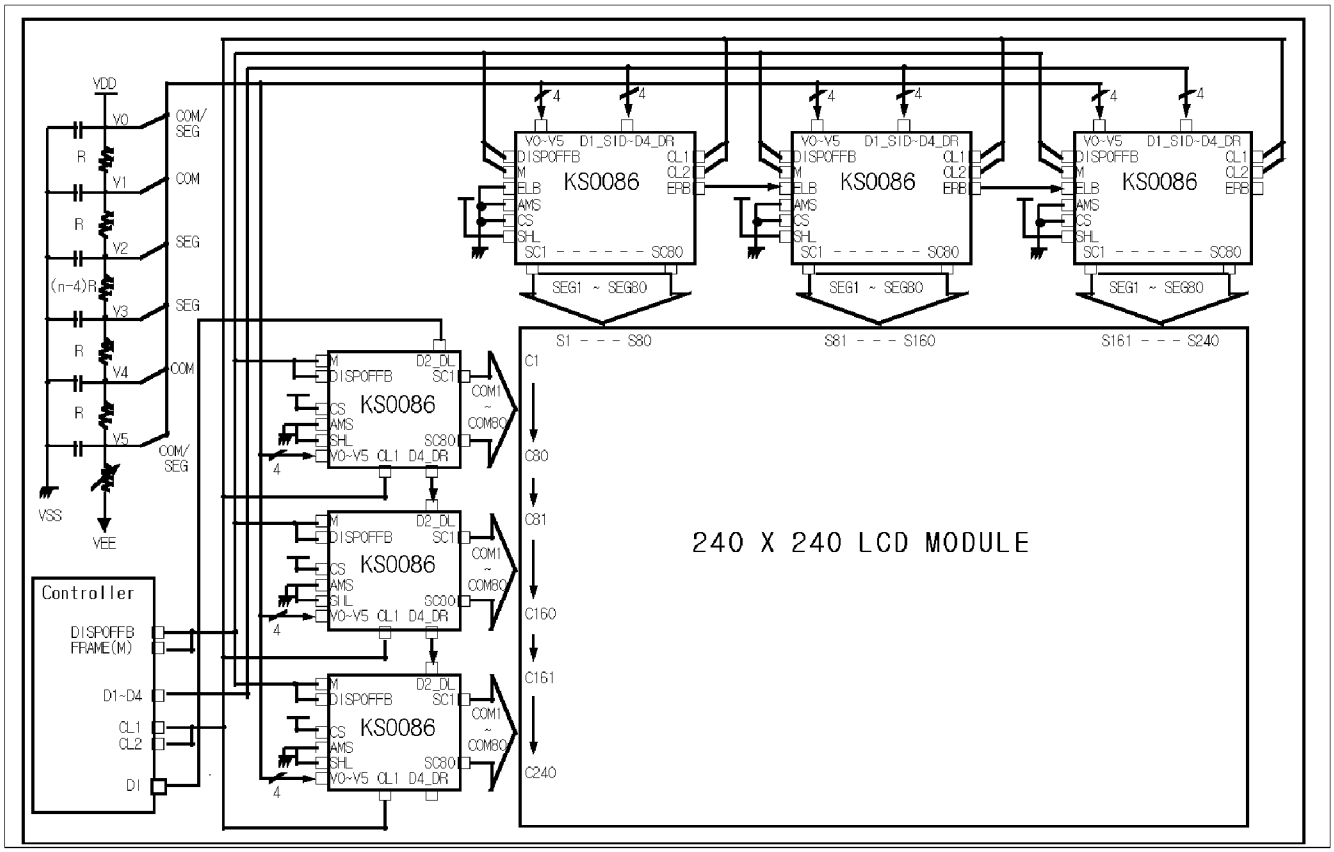


*NOTE

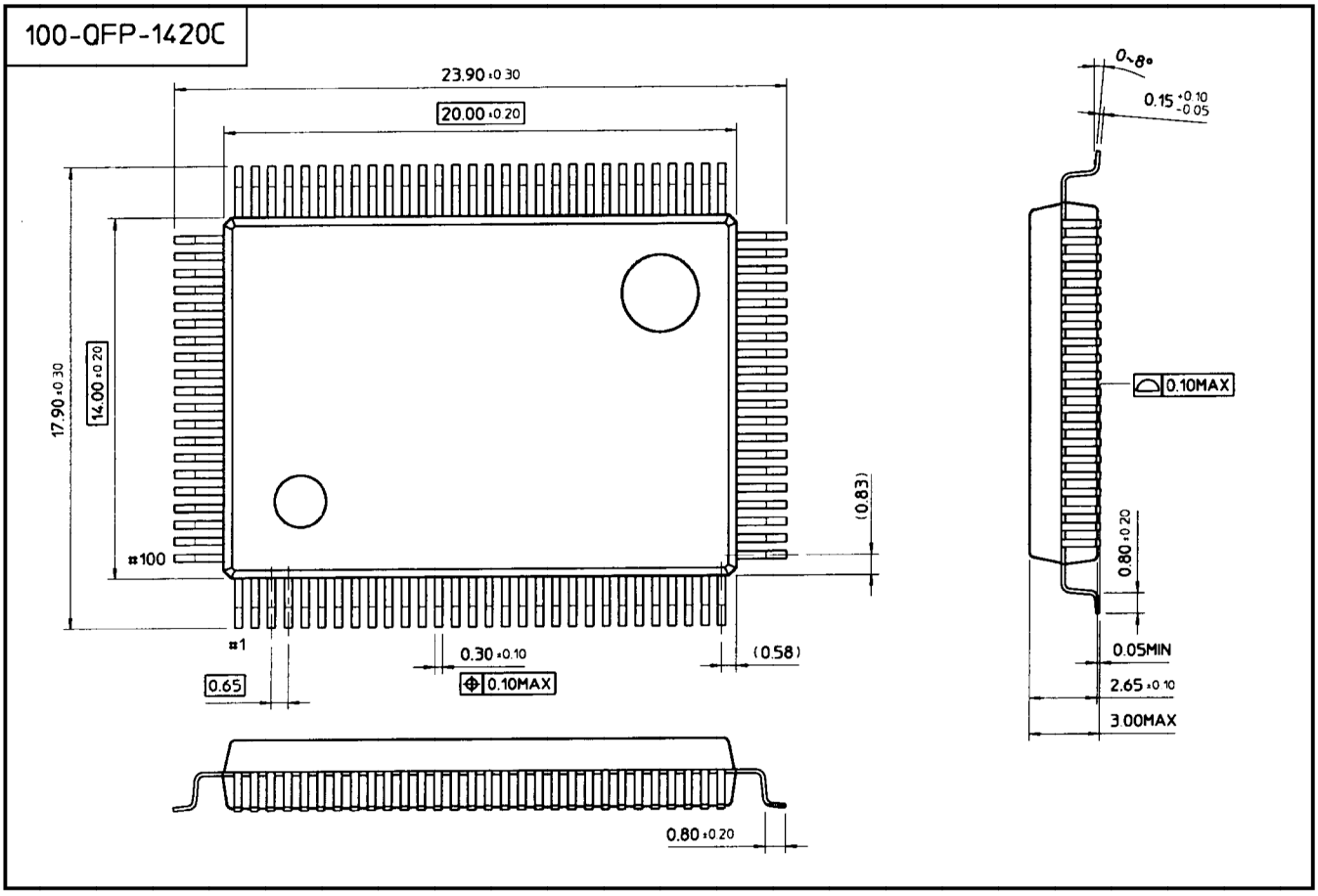
Using this application mode (dual-type common mode), duty ratio can be reduced to half. In upper case 1/200 duty can be used to drive 400 common LCD panel. If single -type application mode is used to this LCD panel, 1/400 duty ratio must be used.

(4) SIGNAL-TYPE INTERFACE MODE (80CH COMMON DRIVER)





Dimensions in Milimeters



Dimensions in Milimeters

100-QFP-1414