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LCD MODULE SPECIFICATION

PART NO.: UP-G128128ACTLWW1.44

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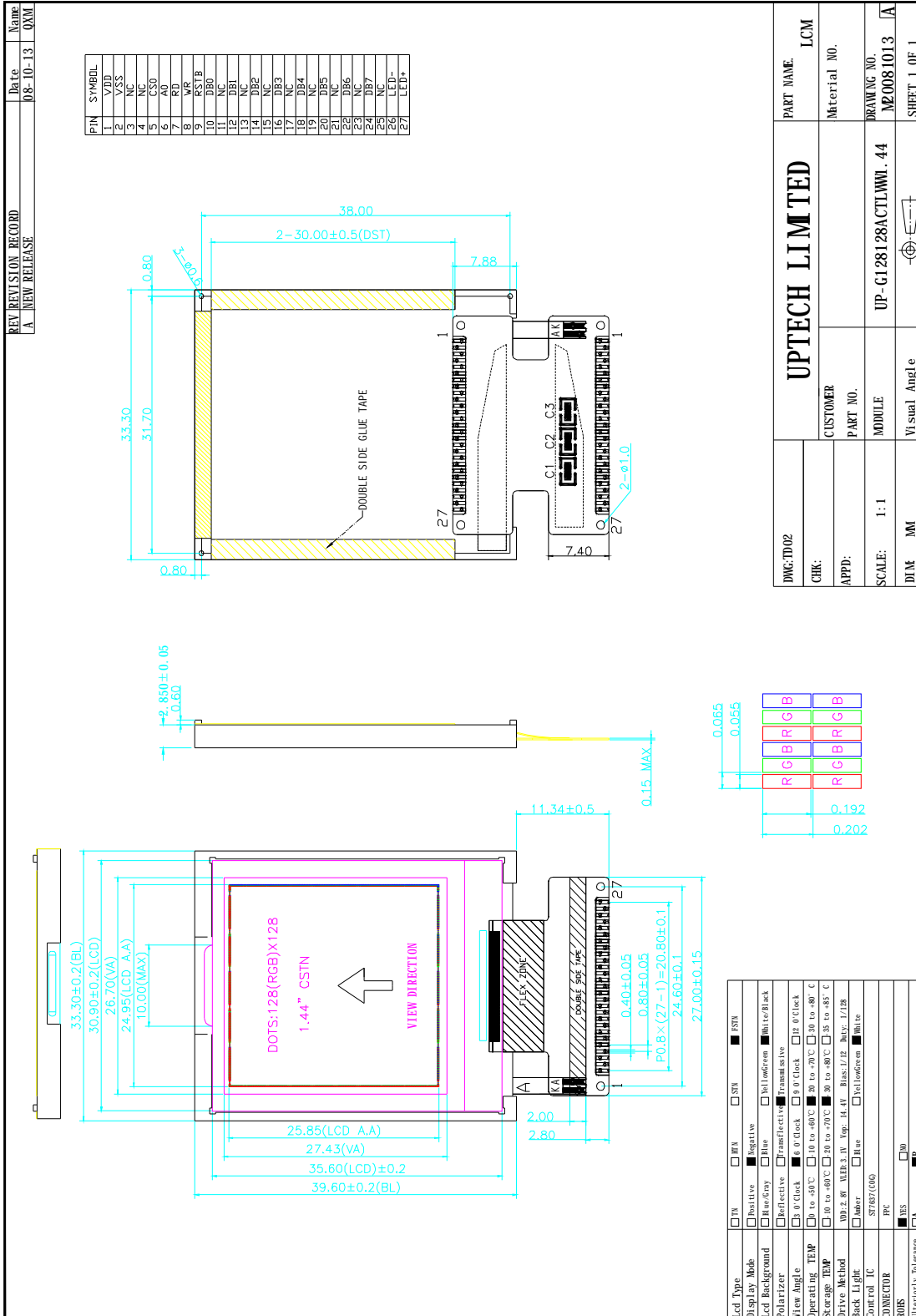


GENERAL SPECIFICATION

Outline Size(mm)	33.3(L)×39.6(W) ×3.45(T)MAX
LCD Type	CSTN, TRANSMISSIVE, Negative
Display type	128(RGB)×128 DOTS
View Area(mm)	26.7×27.43
Display Area(mm)	24.95×25.846
Dots size(mm)	0.055W×0.192H
Dots pitch(mm)	0.065W×0.202H
Controller& driver	ST7637 (Support 65K colors)
View Direction	6 O'CLOCK
Interface mode	8080 serial 8-Bit parallel interface
VDD&V _{LCD} (Type)	VDD=2.8V & V _{LCD} =14.4V,
Drive Method	1/128Duty, 1/12Bias
Backlight(Type)	White LED Side B/L
Operation Temp.(°C)	-20~+70
Storage Temp.(°C)	-30~+80



LCD MODULE DRAWING





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ABSOLUTE MAXIMUM RATING

ELECTRICAL ABSOLUTE MAXIMUM RATING.

ITEM	SYMBOL	MIN	MAX	UNIT	COMMENT
POWER SUPPLY FOR LOGIC	VDD -VSS	-0.3	3.0	V	
POWER SUPPLY FOR BOOSTER	VDD - VSS	-0.3	4.2	V	
POWER SUPPLY FOR LCD DRIVE	V _{LCD} - VSS	-0.3	18.0	V	
INPUT VOLTAGE	VI	VSS	VDD+0.5	V	
POWER SUPPLY FOR LED	VA-VK	--	3.3	V	

ENVIRONMENTAL ABSOLUTE MAXIMUM RATING.

ITEM	OPERATING		STORAGE		COMMENT
AMBIENT TEMPERATURE(°C)	-20	+70	-30	+80	
HUMIDITY	NOTE (1)		NOTE (1)		WITHOUT CONDENSATION
VIBRATION (M/S ²)	/	/	/	/	SEE "ITEMS OF RELIABILITY"
TEMPERATURE CYCLING TEST	/	/	/	/	SEE "ITEMS OF RELIABILITY"
CORROSIVE GAS	Not Acceptable		Not Acceptable		

NOTE(1):Ta≤40°C:90% RH MAX

Ta>40°C:ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90%RH AT 40°C.



ELECTRICAL CHARACTERISTICS (VSS=0V)

Item	Symbol	Condition	Min.	Typ	Max.	Unit	note
Power Supply for Logic	VDD -VSS	T _a =-20~+70°C	2.6	2.8	3.0	Volt	
Input Voltage	V _{IL}	VDD=2.8V	VSS		0.3 VDD	Volt	
	V _{IH}		0.7 VDD	-	VDD	Volt	
Output Voltage	V _{OL}	VDD=2.8 I _{OL} =+1mA I _{OH} =-1mA	VSS	-	0.2 VDD	Volt	
	V _{OH}		0.8 VDD	-	VDD	Volt	
LCD drive Voltage (recommended Voltage)	V _{LCD} -VSS				-	Volt	
		T _a =25°C	-	14.4	-		
					-		
Power Supply Current for LCM	I _{DD}	VDD =2.8V T _a =25°C Full Display Normal Operation	-	1.2	3.0	mA	-
	I _{LED}		-	15	20		

**INTERFACE PIN ASSIGNMENT**

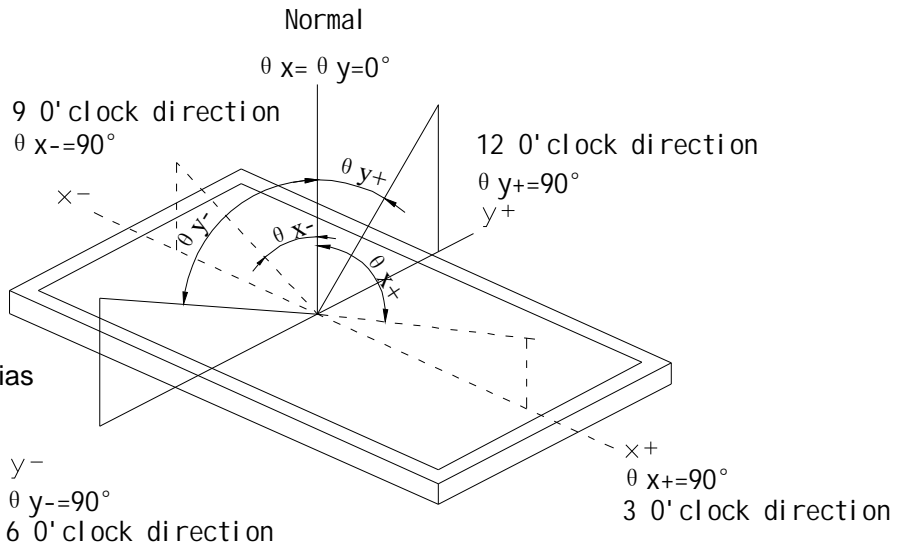
Pin No.	Pin Out	Description
1	VDD	Power Supply for LCD
2	VSS	Power Ground
3	NC	NO Connect
4	NC	NO Connect;
5	CS0	Chip select input pin; Command / data I/O is enable when /CS is LOW.
6	A0	Data / Instruction select input pin RS=L, BIT0 to BIT7 are instruction data RS=H, BIT0 to BIT7 are display data
7	RD	Read enable clock input pin. The data on D0 to D8 are latched at the rising edge of the RD signal.
8	WR	Write enable clock input pin. The data on D0 to D8 are latched at the rising edge of the WR signal.
9	RSTB	Reset input pin When /RESET is "L", initialization is executed
10	DB0	Data bus bit0;
11	NC	NO Connect;
12	DB1	Data bus bit1;
13	NC	NO Connect;
14	DB2	Data bus bit2;
15	NC	NO Connect;
16	DB3	Data bus bit3;
17	NC	NO Connect;
18	DB4	Data bus bit4;
19	NC	NO Connect;
20	DB5	Data bus bit5;
21	NC	NO Connect;
22	DB6	Data bus bit6;
23	NC	NO Connect;
24	DB7	Data bus bit7;
25	NC	NO Connect;
26	LED-	LED backlight input (Cathode);
27	LED+	LED backlight input (Anode);



ELECTRO-OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ	Max.	Unit	note
Viewing angle range	$\theta_{x+}+\theta_{x-}$	$T_a=25^\circ\text{C}$	105	129	--	Deg	K=2 A,B
	$\theta_{y+}+\theta_{y-}$		57	71	--		
Rise Time	T_r	$T_a=25^\circ\text{C}$	--	320	420	Msec	$\theta=0$ $\Phi=0$ $f_F=70\text{HZ}$ VOP=14.4V 1/128D,1/12B
		$T_a=0^\circ\text{C}$	--	--	--		
Fall Time	T_f	$T_a=25^\circ\text{C}$	--	110	145		
		$T_a=0^\circ\text{C}$	--	--	--		
Contrast	Cr	$T_a=25^\circ\text{C}$	24	36	--	--	$\theta=0$ $\Phi=0$ $f_F=70\text{HZ}$ VOP=14.4V 1/128D,1/12B

A. Definition of viewing angle (θ & Φ)



Condition:

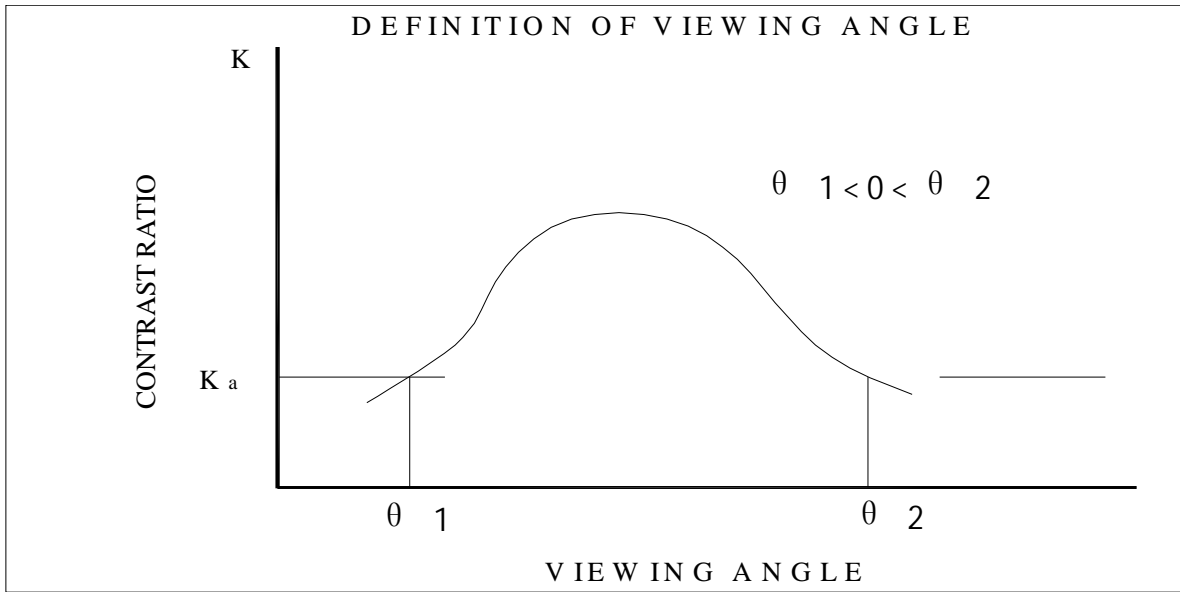
Operating voltage: V_{LCD}

Applying wave form: 1/N Duty, 1/a Bias

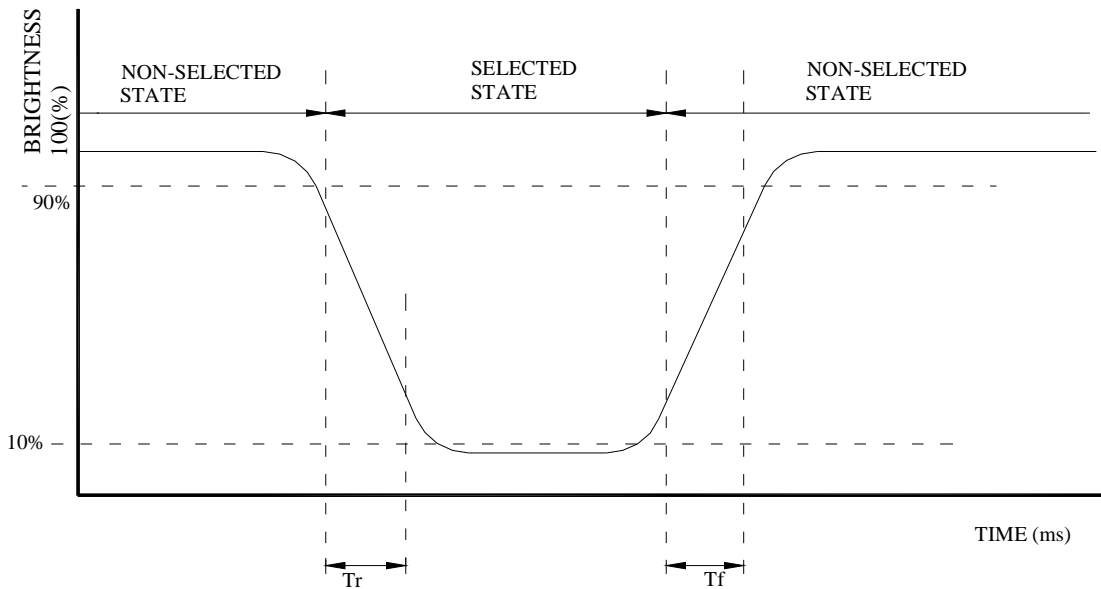
Contrast ratio: ≥ 2



B. Definition of viewing angle (θ_1 & θ_2)



C. Definition of Response Time (T_r , T_f)



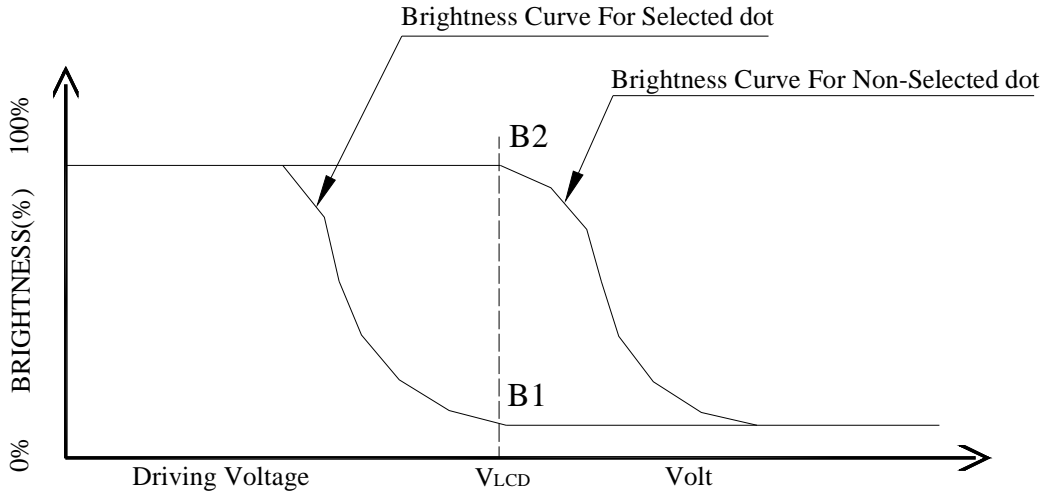


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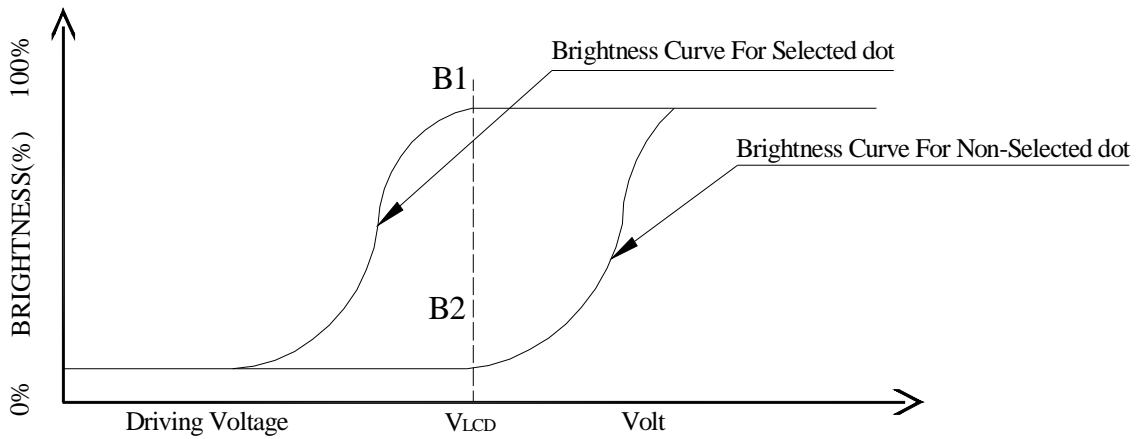


D. Definition of contrast ratio Cr (1) Mode: Positive



$$Cr = \frac{\text{Brightness of Non-selected dot (B2)}}{\text{Brightness of selected dot (B1)}}$$

(2) Mode: Negative



$$Cr = \frac{\text{Brightness of selected dot (B1)}}{\text{Brightness of Non-selected dot (B2)}}$$



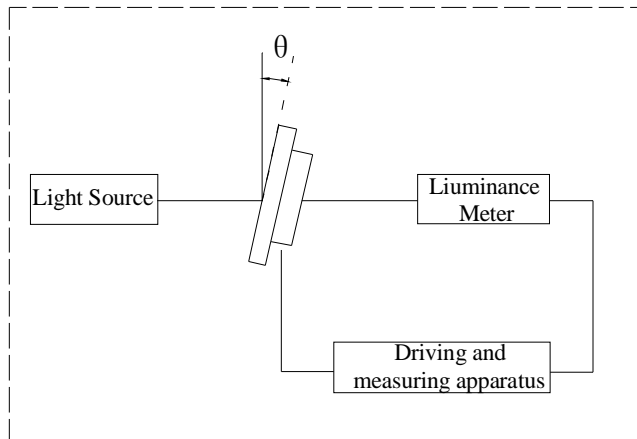
Description of Measuring Equipment

Light Source: Halogen LAMP

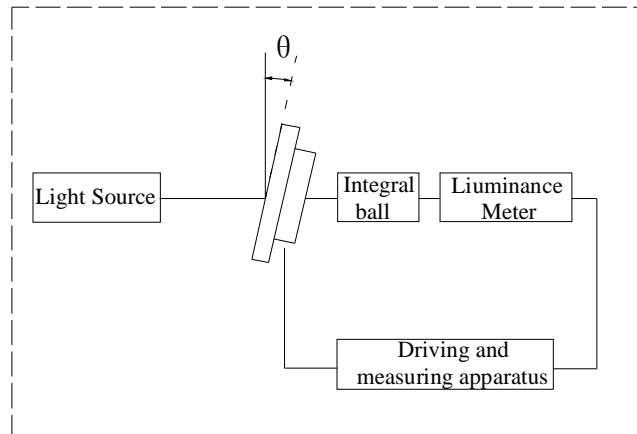
Measurement conditions: Luminance measurement spot

Diameter: 4mm Φ

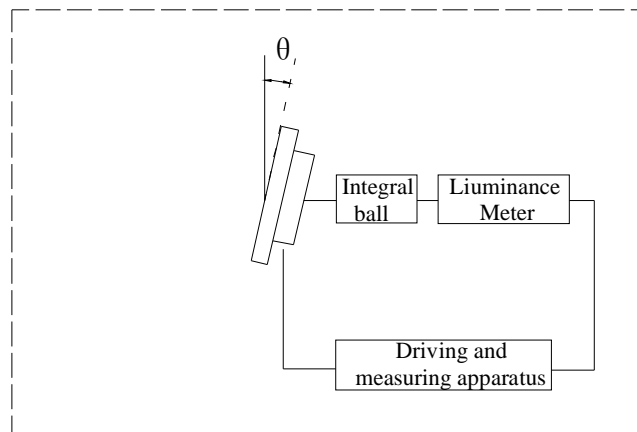
Mode: Transmissive



Mode: Transflective

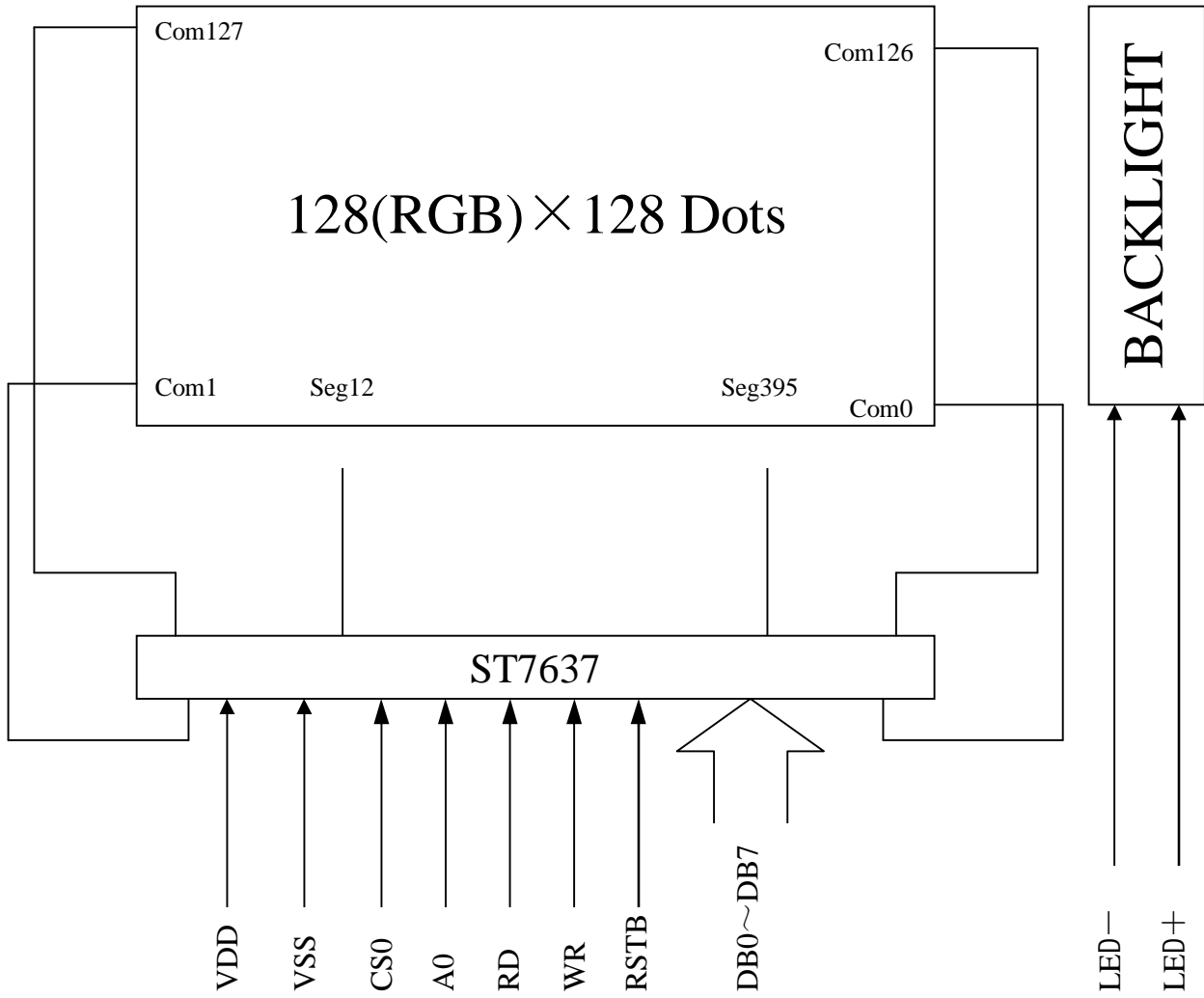


Mode: Reflective





(1) BLOCK DIAGRAM

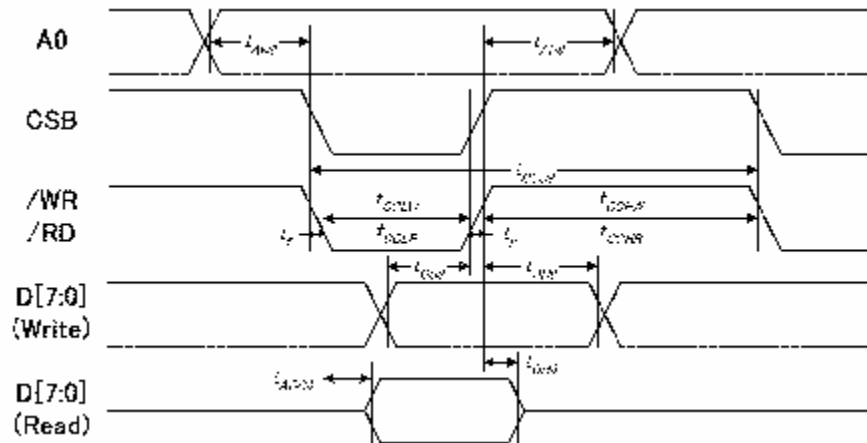




SCHEDULING

ST7367 Scheduling

- Read/Write Characteristics (8080 Serial Parallel Mode)



(VDD=2.8V, Ta=25°C, die)

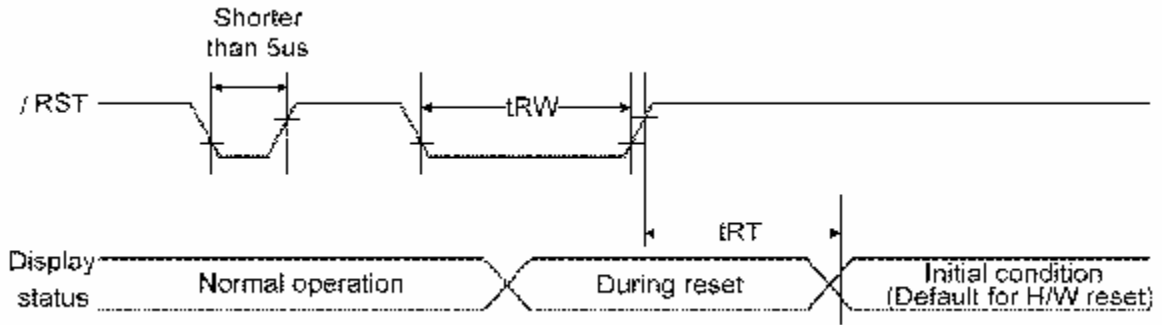
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t _{AH0}		15	—	ns
Address setup time		t _{AWB}		15	—	
System cycle time (WRITE)	WR	t _{CYC0}		170	—	ns
/WR L pulse width (WRITE)		t _{CCLW}		50	—	
/WR H pulse width (WRITE)	t _{CCHW}		100	—		
System cycle time (READ)	RD (ID)	t _{CYC0}	When read ID data	60	—	
/RD L pulse width (READ)		t _{CCLR}		40	—	
/RD H pulse width (READ)		t _{CCHR}		20	—	
System cycle time (READ)	RD (FM)	t _{CYC0}	When read from frame memory	350	—	
/RD L pulse width (READ)		t _{CCLR}		100	—	
/RD H pulse width (READ)		t _{CCHR}		250	—	
WRITE data setup time	D0 to D7	t _{DSS}		50	—	
WRITE data hold time		t _{DHB}		10	—	
READ access time (ID)		t _{ACCB (ID)}		—	50	
READ access time (FM)		t _{ACCB (FM)}	CL = 30 pF	—	70	
READ Output disable time		t _{OH0}	CL = 30 pF		60	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.



● Resetting timing



(VDD=2.8V, Ta=25°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Reset "L" pulse width	/RST	tRW		10	—	µs
Reset time		tRT		—	5 (*note 5)	ms
					—	120 (*note 6,7)

Notes:

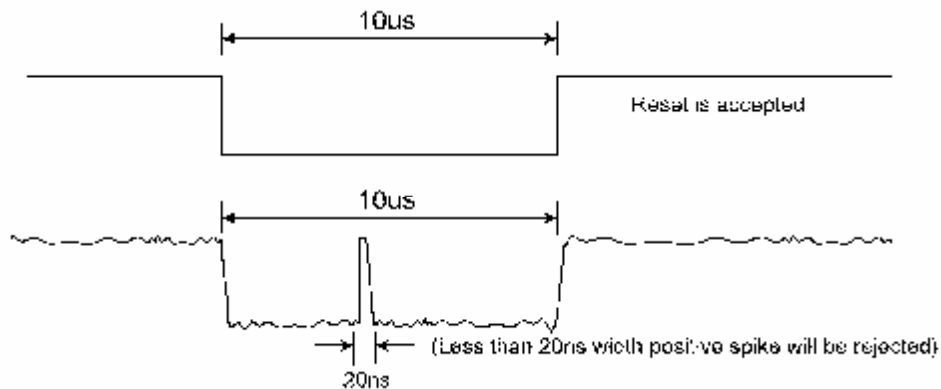
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RST.

2. Spike due to an electrostatic discharge on RST line does not cause irregular system reset according to the table below:

RST Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 120msec.



DISPLAY COMMANDS

The display commands shown below control the internal state of the LCD driver ICs. Commands are sent from CPU to LCD module for the display control.

Command Table-1 , /EXT= H , L , or floating														
Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
{00h}	NO ²	0	1	0	0	0	0	0	0	0	0	0	No Operation	3.1.1
{01h}	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	3.1.2
{04h}	RDDID	0	1	0	0	0	0	0	0	1	0	0	Read Display ID	3.1.3
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID1 read (D23-D16)	
-		1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID2 read (D15-D8)	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	ID3 read (D7-D0)	
{09h}	RDDST	0	1	0	0	0	0	0	0	0	0	1	Read Display Status	3.1.4
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	(D31-D24)	
-		1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(D23-D16)	
-		1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(D15-D8)	
-		1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(D7-D0)	
{0Ah}	RDDPM	0	1	0	0	0	0	0	0	0	1	0	Read Display Power Mode	3.1.5
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	D2	0	0	-	
{0Bh}	RDDMADCTR	0	1	0	0	0	0	0	0	0	1	1	Read Display MADCTR	3.1.6
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	0	0	0		
{0Ch}	RDDCOLMGR	0	1	0	0	0	0	0	0	1	0	0	Read Display Pixel Format	3.1.7
-		1	0	1									Dummy read	
-		1	0	1	0	0	0	0	0	D2	D1	D0	-	
{0Dh}	RDDIM	0	1	0	0	0	0	0	0	1	0	1	Read Display Image Mode	3.1.8
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	0	D5	D4	D3	0	0	0	-	
{0Eh}	RDDSM	0	1	0	0	0	0	0	0	1	1	0	Read Display Image Mode	3.1.9
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	0	0	0	0	0	0	-	
{0Fh}	RDDSDI?	0	1	0	0	0	0	0	0	1	1	1	Read Display Self-diagnostic result	3.1.10
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	1	1	1	D4	0	0	0	0		



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(10h)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in & booster off	9.1.11
(11h)	SLPOLT	0	1	0	0	0	0	1	0	0	0	1	Sleep out & booster on	9.1.12
(12h)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	9.1.13
(13h)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off (Normal)	9.1.14
(20h)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inverts on/off (normal)	9.1.15
(21h)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inverts on/on	9.1.15
(22h)	APOFF	0	1	0	0	0	1	0	0	0	0	1	All pixel off (Only for test purpose)	9.1.16
(23h)	AFON	0	1	0	0	0	1	0	0	0	0	1	All pixel on (Only for test purpose)	9.1.16
(25h)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	9.1.19
-		1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	Ev = 0 to 127	
(28h)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	9.1.20
(29h)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	9.1.20
(2Ah)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	9.1.22
		1	1	0	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	X_ADDR start: 0 ≤ XS ≤ 83h
		1	1	0	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	X_ADDR end: XS ≤ XE ≤ 83h
(2Bh)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	9.1.23
		1	1	0	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Y_ADDR start: 0 ≤ YS ≤ 83h
		1	1	0	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Y_ADDR end: YS ≤ YE ≤ 83h
(2Ch)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write	9.1.24
		1	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data
(2Dh)	RGBSET	0	1	0	0	0	1	0	1	1	0	1	Color set for 256 or 4k color display	9.1.25
-		1	1	0	-	-	-	R4	R3	R2	R1	R0	Red tone (0000)	
-		1	1	0	:	:	:	:	:	:	:	:	:-	
-		1	1	0	-	-	-	R4	R3	R2	R1	R0	Red tone (1111)	
-		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (00000)	
		1	1	0	-	-	-	-	-	-	-	-	-	
		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (11111)	
		1	1	0	-	-	-	B4	B3	B2	B1	B0	Blue tone (0000)	
		1	1	0	-	-	-	-	-	-	-	-	-	
		1	1	0	-	-	-	B4	B3	B2	B1	B0	Blue tone (1111)	
(2Eh)	RAMRD	0	1	0	0	0	1	0	1	1	1	0	Memory Read	9.1.26
		1	1	0	-	-	-	-	-	-	-	-	Dummy read	
		1	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
(30h)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial start/end address set	9.1.27



-		1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Start address (0~131)	
-		1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	End address (0~131)	
(33h)	SCRLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll Area	9.1.25
-		1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA=0~132	
-		1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA=0~132	
-		1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA=0~132	
(34h)	TEOFF	0	1	0	0	0	1	1	0	1	0	0	Tearing effect line of	9.1.26
(35h)	ILON	0	1	0	0	0	1	1	0	1	0	1	Tearing effect mode set & on	9.1.27
-		1	1	0	-	-	-	-	-	-	-	M	'0': mode1, '1': mode2	
(36h)	MADCTR	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	9.1.31
-		1	1	0	MY	MX	MV	ML	RGB	-	-	-	-	
(37h)	VSCSAL	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of RAM	9.1.32
		1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA = 0~131	
(38h)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	9.1.33
(39h)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	9.1.34
(3Ah)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	9.1.35
-		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	
(DAh)	RDID1	0	1	0	1	1	0	1	1	0	1	0	Read ID1	9.1.36
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	(D7-D0)	
(DBh)	RDID2	0	1	0	1	1	0	1	1	0	1	1	Read ID2	9.1.37
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	(D7-D0)	
(DCh)	RDID3	0	1	0	1	1	0	1	1	1	0	0	Read ID3	9.1.38
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	(D7-D0)	

Note 1: When /EXT connects to H or floating, commands which are not defined in "Command Table-1" are treated as NOP (00H) command.

Note 2: Commands 10H, 12H, 13H, 20H, 21H, 25H, 28H, 29H, 30H, 36H (Bit ML only), 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects.

During Sleep In mode, these commands are updated immediately.

Read status (09H), Read Display Power Mode (0AH), Read Display MADCTR (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode



Command Table-2 , /EXT= L or command D7h[7] enable														
Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(B0h)	DutySe:	0	1	0	1	0	1	1	0	0	0	0	Display Duty setting	9 1.36
		1	1	0	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0		
(B1h)	FirstCom	0	1	0	1	0	1	1	0	0	0	1	First Com. Page address	9 1.40
		1	1	0	--	F6	F5	F4	F3	F2	F1	F0		
(B3h)	OscDiv	0	1	0	1	0	1	1	0	0	1	1	HOSC divider	9 1.41
		1	1	0	-	-	-	-	-	-	CLD1	CLD0		
(B5h)	NI InvRet	0	1	0	1	0	1	1	0	1	0	1	N-line control	9 1.42
		1	1	0	M	N6	N5	N4	N3	N2	N1	N0		
(B7h)	ComScanDir	0	1	0	1	0	1	1	0	1	1	1	Com/Seg Scan Direction for Glass layout	9 1.43
		1	1	0	0	SMX	0	0	SS3R	0				
(B8h)	RmwIn	0	1	0	1	0	1	1	1	0	0	0	reac modify write control IN	9 1.44
(B9h)	RmwOut	0	1	0	1	0	1	1	1	0	0	1	reac modify write control Out	9 1.45
(C0h)	VopSet	0	1	0	1	1	0	0	0	0	0	0	Vop setting	9 1.46
		1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0		
		1	1	0	-	-	-	-	-	-	-	VopB		
(C1h)	VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	-40mw/self	9 1.47
(C2h)	VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	-40mw/self	9 1.46
(C3h)	BiasSel	0	1	0	1	1	0	0	0	0	1	1	Bias selection	9 1.48
		1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0		
(C4h)	Bs.BmpXSel	0	1	0	1	1	0	0	0	1	0	0	Booster setting	9 1.50
		1	1	0	-	-	-	-	-	BST2	BST1	BST0		
(C5h)	Bs:EffSe	0	1	0	1	1	0	0	0	1	0	1	Booster efficiency selection	9 1.51
		1	1	0	-	-	-	-	-	-	BTF1	BTF0		
(C7h)	VopOffse:	0	1	0	1	1	0	0	0	1	1	1		9 1.52
		1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0		
		1	1	0	-	-	-	-	-	-	-	VOS8		
(CBh)	VgBorcSe	0	1	0	1	1	0	0	1	0	1	1	UV3 with Booster x2 control	9 1.53
		1	1	0	-	-	-	-	-	-	-	2BT0		
(CCh)	ID ⁺ Set	0	1	0	1	1	0	0	1	1	0	0	ID ⁺ setting	9 1.54
		1	1	0	ID ⁺ _7	ID ⁺ _6	ID ⁺ _5	ID ⁺ _4	ID ⁺ _3	ID ⁺ _2	ID ⁺ _1	ID ⁺ _0		
(CDh)	ID2Sel	0	1	0	1	1	0	0	1	1	0	1	ID2 setting	9 1.55



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		1	0	1	ID2_6	ID2_5	ID2_4	ID2_3	ID2_2	ID2_1	ID2_0		
(CEh)	ID3Set	0	1	0	1	0	0	1	1	1	0	ID3 setting	§.1.56
		1	0	0	ID3_7	ID3_6	ID3_5	ID3_4	ID3_3	ID3_2	ID3_1	ID3_0	
(D0h)	ANASET	0	1	0	1	0	1	0	0	0	0	Analog circuit setting	§.1.57
		1	0	0	0	0	1	1	1	0	1		
(D7h)	AutoLoadSel	0	1	0	1	0	1	0	1	1	1	mask rom data auto re-load control	§.1.58
		1	0	0	EXTC	OTPCF	-	ARD	1	1	1		
(DEh)	RDTsISatus	0	1	0	1	0	1	1	1	1	0	read IC status	§.1.59
		1	0	1	-	-	-	-	-	-	-	Dummy Read	
(E0h)	EPCTIN	0	1	0	1	1	0	0	0	0	0	Control OTP WR/RD	§.1.60
		1	0	0	0	0	WR :XRD	0	0	0	0		
(E1h)	EPCTCLT	0	1	0	1	1	1	0	0	0	0	OTP control cancel	§.1.61
(E2h)	EPMWR	0	1	0	1	1	1	0	0	0	1	Write to OTP	§.1.62
(E3h)	EPMRD	0	1	0	1	1	1	0	0	0	1	Read from OTP	§.1.63
(E4h)	OTPSSEL	0	1	0	1	1	1	0	0	1	0	Select OTP	§.1.64
		1	0	0	MS1	MS0	0	1	1	0	0		
(E5h)	ROMSET	0	1	0	1	1	1	0	0	1	0	Programmable rom setting	§.1.65
		1	0	0	0	0	0	0	1	1	0		
(E7h)		0	1	0	1	1	1	0	0	1	1	Low voltage mode setting	§.1.66
		1	0	0	0	0	1	0	0	0	1		
(E8h)		0	1	0	1	1	1	0	1	0	0		
		1	0	0	0	0	1	1	0	1	1		
		1	0	0	0	0	0	0	0	0	1		
		1	0	0	0	0	0	1	1	1	1		
(EBh)	HPVSET	0	1	0	1	1	1	0	1	0	1	High power mode setting	§.1.67
		1	0	0	0	0	0	0	0	0	0		
		1	0	0	0	0	0	0	0	0	1		
(F0h)	FRMSEL	0	1	0	1	1	1	1	0	0	0	Frame Freq. in Temp range A,B,C and D	§.1.68
		1	0	0	-	-	-	FA4	FA3	FA2	FA1	FA0	
		1	0	0	-	-	-	FB4	FB3	FB2	FB1	FB0	
		1	0	0				FC4	FC3	FC2	FC1	FC0	
		1	0	0	-	-	-	FD4	FD3	FD2	FD1	FD0	



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(F1h)	FRMSEL	0	1	0	1	1	1	1	0	0	0	1	Frame Freq. in Temp range A,B,C and D (idle)	9.1.69
		1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0		
		1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0		
		1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0		
		1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0		
(F2h)	TMPRNG	0	1	0	1	1	1	1	0	0	1	0	Temp range A,B and C	9.1.70
		1	1	0		TA6	TA5	TA4	TA3	TA2	TA1	TA0		
		1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0		
		1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0		
(F3h)	TMPHYS	0	1	0	1	1	1	1	0	0	1	1	Hysteresis value set	9.1.71
		1	1	0	-	-	-	-	TH3	TH2	TH1	TH0		
(F4h)	TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	TEMPSEL	9.1.72
		1	1	0	MT13	MT12	MT11	MT10	MT09	MT08	MT07	MT06		
		1	1	0	MT33	MT32	MT31	MT30	MT29	MT28	MT27	MT26		
		1	1	0	MT53	MT52	MT51	MT50	MT49	MT48	MT47	MT46		
		1	1	0	MT73	MT72	MT71	MT70	MT69	MT68	MT67	MT66		
		1	1	0	MT93	MT92	MT91	MT90	MT89	MT88	MT87	MT86		
		1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0		
		1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0		
		1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0		
(F7h)	TIYS	0	1	0	1	1	1	1	0	1	1	1	Temperature detection threshold	9.1.73
		1	1	0	IHYS7	IHYS6	IHYS5	IHYS4	IHYS3	IHYS2	IHYS1	IHYS0		
(F9h)	Frame Set	0	1	0	1	1	1	1	1	0	0	1	Set Frame RGB value	9.1.74
		1	1	0	-	-	-	P14	P13	P12	P11	P10		
		1	1	0	-	-	-	P24	P23	P22	P21	P20		
		:	:	:	:	:	:	:	:	:	:	:		
		1	1	0	-	-	-	P151	P153	P152	P151	P150		
		1	1	0	-	-	-	P164	P163	P162	P161	P160		



LCD Product Quality Standard & Reliability Test.

Inspection conditions

ENVIRONMENTAL CONDITIONS

The environmental conditions for inspection shall be as follows:

Room temperature: 22±3°C; Humidity: 50±10%RH

The external visual inspection

The inspection shall be performed by using a single 20W fluorescent lamp for illumination and the distance from LCD to eyes of the inspector should be 30cm or more.

Classification of defects

A major defect

A major defect refers to A defect which may substantially degrade usability for product applications.

Minor defect

A Minor defect refers to A defect which is not considered to substantially degrade product application or A defect which deviates from existing standards almost unrelated to the effective use of the product or its operation

Sampling procedures for each items acceptance level table

Defect type	Sampling procedures	AQL
Major defect	MIL-STD-105D Inspection level1 normal inspection Single sample inspection	1.0
Minor defect	MIL-STD-105D Inspection level1 normal inspection Single sample inspection	2.5

Life time

50,000Hrs (25°C in the room without ray of sun)

ITEMS OF RELIABILITY

ITEM	CONDITIONS	CRITERION
High temperature operation test	+70°C \ 120 hours	1. It judged at room temperature after 1 hours to be good as appearance and electrical test is normal after the experiment. 2. Current consumption should within the specification of Approval sheet Electro-optical characteristics
Low temperature operation test	-20°C \ 120 hours	5-10pcs



High temperature/humidity storage test	+80°C, 80%±10% RH \ 120 hours	
High temperature storage test	+80°C \ 120 hours	
Low temperature storage test	-30°C \ 120 hours	
Temperature cycling test	<p>-20°C (30 min) ↓↑ 25°C (5 min) ↓↑ 70°C (30 min)</p> <p>CYCLES: 10</p>	
Vibration	<p>Random Wave: 10 ~ 50 Hz Each Direction (x, y, z): 30MIN.</p>	

Cosmetic criteria of LCD screen

DEFECT	JUDGEMENT CRITERION		
	Size d (mm)	Acceptable quantity in active area	
Spots	d ≤ 0.1	Disregard	
	0.1 < d ≤ 0.2	6	
	0.2 < d ≤ 0.3	2	
	d > 0.3	0	
Note: d = (Length + Width)/2			
Polarizer Bubbles	d ≤ 0.3	Disregard	
	0.3 < d ≤ 1.0	3	
	1.0 < d ≤ 1.5	1	
	d > 1.5	0	
Note: d = (Length + Width)/2			
Lines	Width W (mm) Length L (mm)	Acceptable quantity in active area	
	W ≤ 0.02	Disregard	
	0.02 < W ≤ 0.05	L ≤ 5.0	6
		L > 5.0	0
	0.05 < W ≤ 0.1	L ≤ 2.0	6
L > 2.0		0	
W > 0.1	See criteria for spots		
Testing conditions: 20W fluorescent lamp at 30 cm distance at normal viewing angle			



PRECAUTIONS

Safety

1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

Static charge

Since this LCD module contains CMOS LSI that are sensitive to static charge, care must be taken when handling it.

Power on sequence

1. Input signals should not be applied to the LCD module before the logic system voltage has reached the specified voltage. If the above sequence is not kept, the LCD module might be permanently damaged.
2. When connecting the power supply, connect the LCD bias voltage after connecting the logic system voltage.
3. When disconnecting the power supply, disconnect the logic system voltage after the LCD bias voltage.
4. It is recommended to connect a serial resistor or fuse to the LCD bias power supply of the system as a current limiter. The value of the resistor depends on the kind of LCD used, but is typically 50~100Ω

Operation

1. It is essential to drive the LCD within the specified voltage limits, since a higher driving voltage than allowed causes a shorter LCD lifetime. Under these circumstances, electrochemical reactions will result in undesirable deterioration of the LCD.
2. The response time of the LC fluid is considerably longer at low temperature than in the normal operating temperature range. On the other hand, the LCD will show a dark blue color at high temperatures. Those phenomena do not indicate a malfunction or defect of the LCD. Back at normal temperatures, the LCD will return to its original behavior.
3. If the display area is pressed hard during operation, some abnormal display patterns might appear. However, the display will resume normal operation after turning the module off and on.
4. Moisture on the terminals could cause an electrochemical reaction resulting in an open terminal connection. If the environmental temperature is higher than 50°C, it is required that the relative humidity is 50% or less.

Long-time storage

For long-term storage the following methods are highly recommended:

1. Store the product in a polyethylene bag with a sealed opening to prevent fresh air entering from the outside. Placing it with a desiccant is not necessary.
2. Store the product in a dark place, with the temperature in the range from -10°C to 60°C.
3. Keep the sensitive polarizer surface of the LCD panels clear of any contact. We recommend using the container that was used by Uptech to deliver the products.

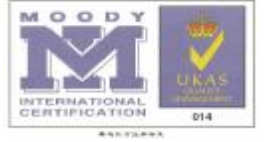
Cleaning of product

To clean the product makes sure to use absorbent cotton cloth or other soft material like chamois. Make sure to rub it gently and do not use chemicals when cleaning.

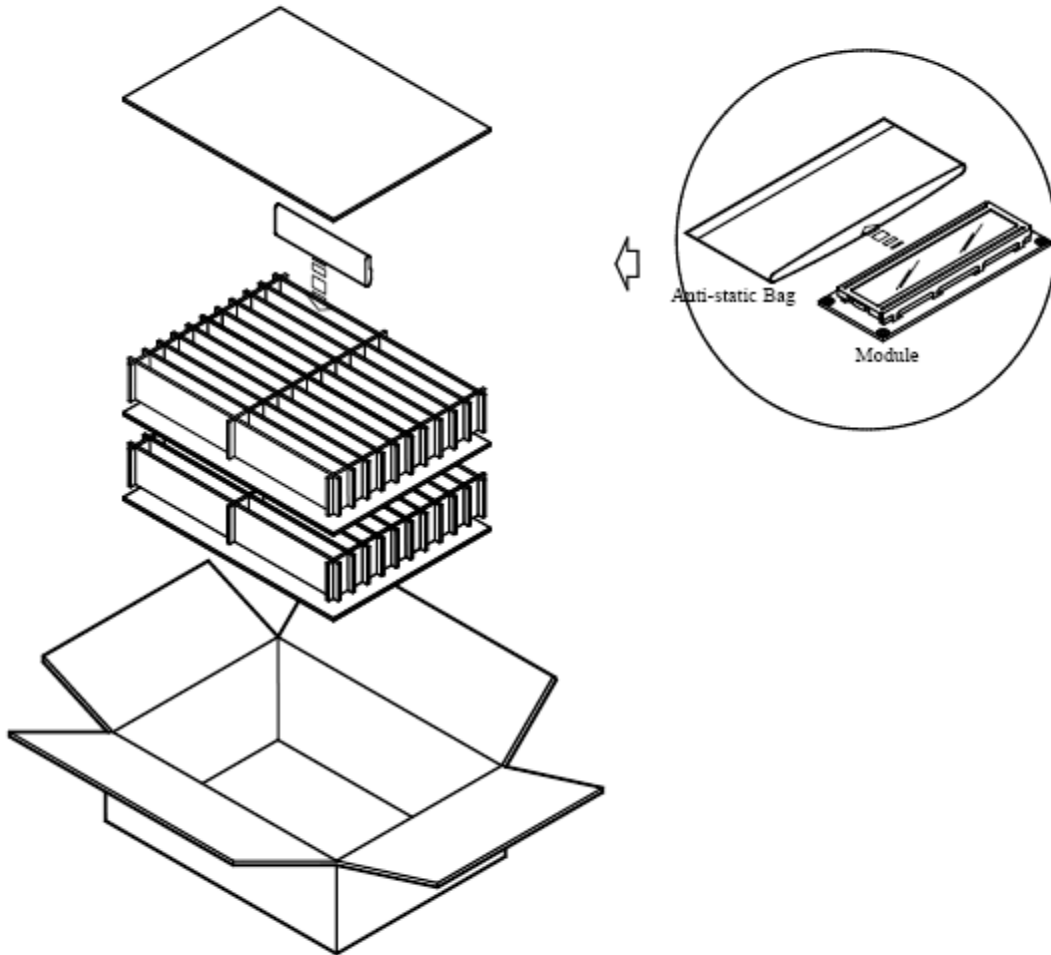


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PACKAGE INFORMATION





Code System :

UP—G 128 128 A C T L W W – X.XX
 1 2 3 4 5 6 7 8 9 10

- 1: Module type: S-SEGMENT,
C-CHARACTER;
G-GRAPHIC;
- 2,3: Display type: LINE *ROW ;
- 4: Serial number: A~Z;
- 5: Lcd mode: C- CSTN;
G-GRAY/STN;
Y-YELLOW-GREEN/STN;
T-TN,HTN;
F-FSTN;
S-BLUE/STN;
- 6: Polarizer mode: A~D: REFLECTIVE;
I,J,F,K: TRANSFLECTIVE;
M,N,L,O: TRANSMISSIVE;
T,U,P,Q: NEGATIVE;
- 7: Backlight mode: L-LED BACKLIGHT;
E-EL BACKLIGHT;
C-CCFL;
- 8: Backlight color: Y-YELLOW GREEN;
B-BLUE;
W-WHITE;
A-AMBER;
E-ORANGE;
- 9: Temperature range: W-WIDE TEMP.
BLANK-NORMAL TEMP.
- 10: Display size : X.XX inches