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ILI9488

a-Si TFT LCD Single Chip Driver 320(RGB) x 480 Resolution, 16.7M-color With Internal GRAM

Specification

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1. Introduction

The ILI9488 is a 16.7M single-chip SoC driver for a-Si TFT liquid crystal display panels with a resolution of 320(RGB) x 480 dots. The ILI9488 is comprised of a 960-channel source driver, a 480-channel gate driver, 345,600 bytes GRAM for graphic data of 320 (RGB) x 480 dots, and power supply circuit.

The ILI9488 supports parallel DBI Type B 8-/9-/16-/18-/24-bit data bus interfaces and DBI Type C 3-/4-line serial peripheral interfaces (SPI) to input commands. The ILI9488 supports DPI (16-/18-/24-bit) data bus for video image display. For MIPI*-DSI* high-speed interface mode, the ILI9488 also provides one data lane and one clock lane that can support up to 500Mbps on MIPI-DSI link.

The ILI9488 can operate with 1.65V I/O interface voltage and supports a wide range of analog power supplies. The ILI9488 supports 8-colors display and sleep mode power management functions, ideal for portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics displays.

Notes:

- MIPI: Mobile Industry Processor Interface
- DSI: Display Serial Interface

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2. Features

- Display resolution: 320 (RGB) (H) x 480 (V)
- Display color modes:
  - Full color modes:
    16.7M colors with dithering function (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)
  - Reduced color modes:
    262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)
    65K colors(16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)
    8 colors (3-bit data, R: 1-bit, G: 1-bit, B: 1-bit)
- Display module:
  - On-chip Frame Memory size 345,600 bytes, 320 (RGB) (H) x 480 (V) x 18 bits
  - Supports 960 source channel outputs
  - Supports up to a maximum of 480 gate lines
  - Supports 24-bits input image function
  - Supports column/1-/2-dot inversion
  - On-module DC VCOM control (-2 to 0V common electrode output voltage range)
  - Source/VCOM/Gate power supply voltage
    - DDVDH – GND = 4.5 to 6V
    - DDVDL – GND = -6 to -4.5V
    - VCL – GND = -3 to -2V
    - DC VCOM – GND = -2 to 0V, a step = 16mV
    - VREG1OUT – GND = 3.625 to 5.5 V
    - VREG2OUT – GND = -5.5 to -3.625V
    - VGH – GND = 10 to 20V
    - VGL – GND = -15 to -5V
- Display Interface types:
  - MIPI-DBI (Display Bus Interface)
    - Type B (i-80 system), 8-/9-/16-/18-/24-bit bus
    - Type C (Serial data transfer interface, 3/4-line SPI)
  - MIPI-DPI (Display Pixel Interface)
    - Supports 24 bit/pixel (R: 8-bit, G: 8-bit, B: 8-bit)
    - Supports 18 bit/pixel (R: 6-bit, G: 6-bit, B: 6-bit)
    - Supports 16 bit/pixel (R: 5-bit, G: 6-bit, B: 5-bit)
  - MIPI-DSI (Display Serial Interface)
    - Supports one data lane/maximum speed 500Mbps
    - Supports DSI version 1.01
    - Supports D-PHY version 1.00
- Input power
  - Low operating power supplies
    - IOVCC = 1.65 to 3.3V (Interface I/O)
    - VCI = 2.5 to 3.3V (Analog)
    - OTP programming voltage (DDVDH Pad) = 7V
- Power saving modes:
  - Deep-standby mode
  - Sleep mode

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- Other on-chip functions/Miscellaneous
  - Supports partial display mode
  - Supports inversion mode
  - Oscillator for display clock generation
  - LVD function (GAS bit) prevents image sticking for abnormal power off
  - Supports DC VCOM driving
  - DC VCOM voltage generator and adjustment
  - OTP memory store initialization register settings (MATCDL, VRH1, VRH2 and BT)
  - MTP (provides 4 times OTP to store DC VCOM setting, ID1/ID2/ID3 setting)
  - Supports CABC function
  - Supports 3-Gamma DGC function
  - Supports dither function. (The dither function is only available in Bypass mode of DPI 24-bit and MIPI-DSI.)
  - Supports color enhancement function

Notes:

- CABC: Content Adaptive Brightness Control
- DGC: Digital Gamma Correction
- LVD: Low Voltage Detection
- MTP: Multiple Time Programming
- OTP: One Time Programming

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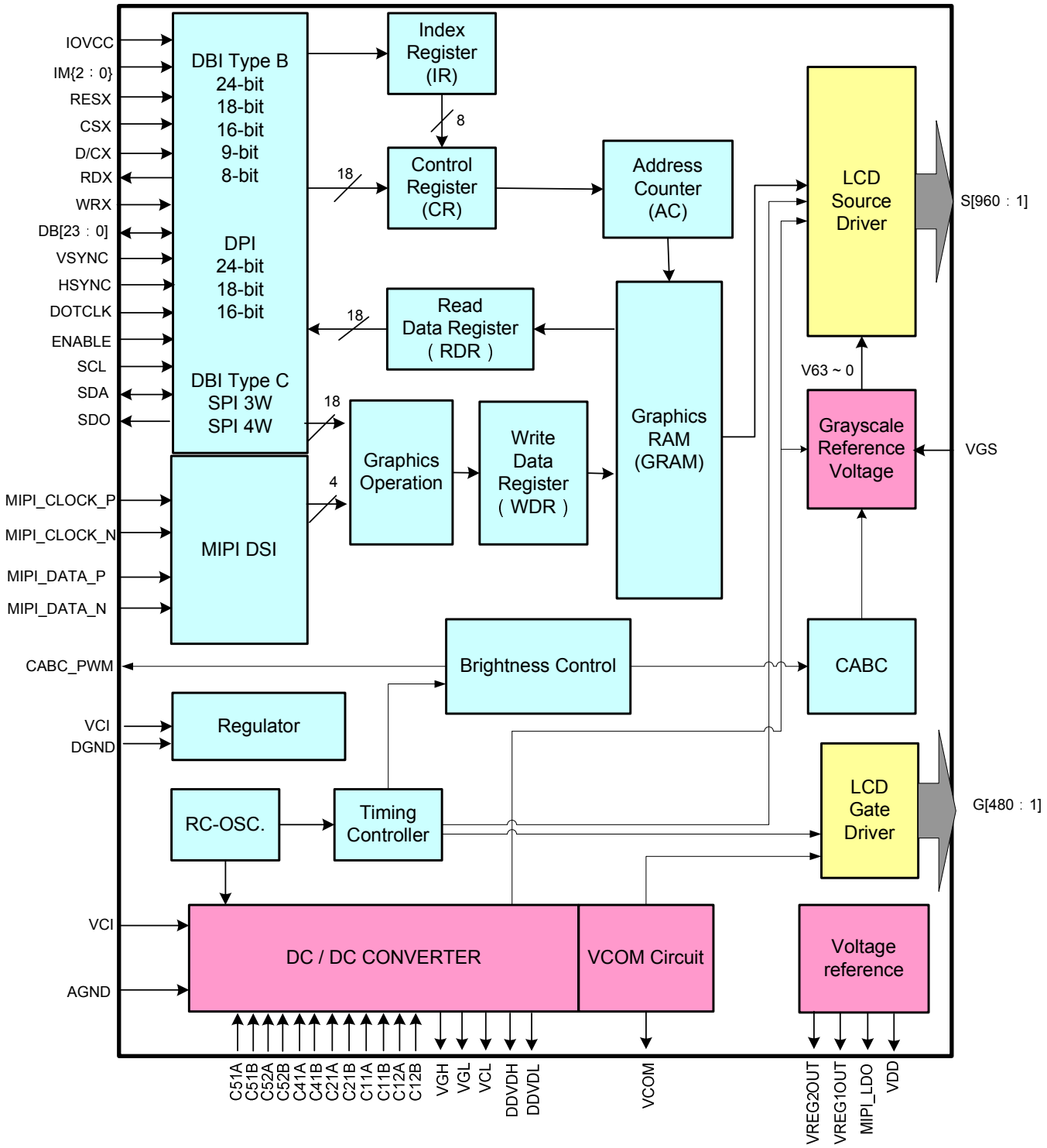
3. Device Overview

3.1.Block Diagram



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3.2. Block Function Description

3.2.1. System Interface

The interface operating mode (DBI, DPI or DSI) is selected by hardware pins IM [2:0], as shown in **Table 1** below.

Table 1: MIPI-DBI Operating Mode

MIPI-DBI Type B				
IM2	**IM1**	**IM0**	**Interface**	**Data Pin in Use**
0	0	0	24-bit bus (DB_EN=1)	DB [23:0]
0	0	0	18-bit bus (DB_EN=0)	DB [17:0]
0	0	1	9-bit bus	DB [8:0]
0	1	0	16-bit bus	DB [15:0]
0	1	1	8-bit bus	DB [7:0]
MIPI-DBI Type C				
1	0	1	Option1 (3-line SPI)	SDA,SDO
1	1	1	Option3 (4-line SPI)	SDA,SDO

Table 2: MIPI-DSI Operating Mode

IM [2:0]			Interface	Data Pin in Use
IM2	**IM1**	**IM0**		
1	1	0	MIPI-DSI	MIPI_DATA_P MIPI_DATA_N MIPI_CLOCK_P MIPI_CLOCK_N

The ILI9488 supports MIPI DBI Type B (8-/9-/16-/18-/24-bits) that uses command method which has an 8-bit index register (IR) and an 8-bit control register (CR). The ILI9488 also has an 18-bit write-data register (WDR) and read-data register (RDR). The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in the internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9488 reads the first data from the internal GRAM. Valid data are read out after the ILI9488 performs the second read operation.

MIPI-DBI Type B			Operation
D/CX	**RDX**	**WRX**	
“L”	“H”	↑	Write command
“H”	↑	“H”	Read parameter
“H”	“H”	↑	Write parameter

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3.2.2. Video Image Interface (TE-Signal and DPI)

When the DBI is selected, display data is written in synchronization with the TE signal which is generated from the internal clock to prevent flicker on the panel.

When the DPI is selected, externally supplied VSYNC, HSYNC, and DOTCLK signals will drive the chip. Display Data (DB [23:0]) is written in synchronization with those synchronous signals after Data Enable (ENABLE). This enables updating image data without flicker on the panel.

3.2.3. Address Counter (AC)

The Address Counter (AC) assigns an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. When writing data to the internal GRAM, the address in the AC is automatically increased/decreased by 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

3.2.4. Graphic RAM (GRAM)

The GRAM is used to store the display pattern data with a maximum of 345,600 bytes for 320 (RGB) x 480 display resolution.

3.2.5. Grayscale Voltage Generating Circuit

The Grayscale Voltage Generating Circuit generates a liquid crystal drive voltage that corresponds to the grayscale level setting in the Gamma correction register. The ILI9488 can display 262k colors at maximum.

3.2.6. Power Supply Circuit

The LCD drive power supply circuit generates VREG1OUT, VREG2OUT, VGH, VGL, and DC VCOM levels to drive the TFT LCD panel.

3.2.7. Timing Generating

The Timing Generator generates timing signals for internal circuits, such as the internal GRAM. Timing for display operation, such as RAM read operation, and timing for internal operations, such as RAM access by the MCU, is outputted separately so that they do not interfere with each other.

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3.2.8. Oscillator

The ILI9488 includes an RC oscillator circuit. Command settings are used to change the frame frequency.

3.2.9. Panel Driver Circuit

The LCD Driver Circuit has a 960-channel source driver (S1~S960) and a maximum of 480 gate lines (G1~G480). When 320 (RGB) pixels of data are input, the display pattern data is latched. The voltage is output from the source driver according to the latched data.

3.2.10. MIPI-DSI Controller Circuit

The MIPI-DSI Controller Circuit consists of a D-PHY controller, Protocol Control Unit (PCU), Packet Processing Unit (PPU), ECC generating circuit, internal data/command buffer, and analog transceiver. The D-PHY controls communication with the analog block, and the ECC generating circuit generates the ECC to check the outgoing data stream for accuracy of the receiving data packet. The PCU controls outgoing and incoming data streams, and the PPU controls packet distribution and merging. The internal data/command buffer is used for temporary storage of incoming commands and display data.

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3.3. Pin Descriptions

<table>
<tr><th colspan="4">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM2, IM1, IM0</td><td>I</td><td>Digital Input</td><td>Select the interface mode
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MIPI-DBI Type B 24-bit bus (DB_EN = 1)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MIPI-DBI Type B 18-bit bus (DB_EN = 0)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MIPI-DBI Type B 9-bit bus</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MIPI-DBI Type B 16-bit bus</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MIPI-DBI Type B 8-bit bus</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MIPI-DBI Type C Option 1 (3-line SPI)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI DSI</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>MIPI-DBI Type C Option 3 (4-line SPI)</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>Digital Input</td><td>Reset input signal
Initialize the chip with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>CSX</td><td>I</td><td>Digital Input</td><td>DBI Type B: Chip select input signal
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to IOVCC level when not in use.</td></tr>
<tr><td>D/CX</td><td>I</td><td>Digital Input</td><td>DBI Type B: Data/Command Selection pin
Low: Command
High: Parameter
Fix to IOVCC level when not in use.</td></tr>
<tr><td>WRX/SCL</td><td>I</td><td>Digital Input</td><td>DBI Type B: WRX pin, serves as a write signal
DBI Type C: SCL pin as Serial Clock when operates in the serial interface
Fix to IOVCC level when not in use.</td></tr>
<tr><td>RDX</td><td>I</td><td>Digital Input</td><td>DBI Type B: serve as a read signal
Fix to IOVCC level when not in use.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Digital I/O</td><td>DBI Type C
DIN/SDA: serial data input/output bi-direction pin
Fix to DGND level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td>Digital Output</td><td>DBI Type C
SDO: Serial data output
Leave the pin open when not in use.</td></tr>
<tr><td>TE</td><td>O</td><td>Digital Output</td><td>Serve as a TE (Tearing Effect) output signal
Leave the pin open when not in use.</td></tr>
<tr><td>CABC_PWM</td><td>O</td><td>Digital Output</td><td>The PWM frequency output for LED driver control</td></tr>
</table>

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			Leave the pin open when not in use.
MIPI_CLOCK_P	I	MIPI-DSI Input	DSI Positive polarity of low voltage differential clock signal ***Leave the pin open when not in use.***
MIPI_CLOCK_N	I	MIPI-DSI Input	DSI Negative polarity of low voltage differential clock signal ***Leave the pin open when not in use.***
MIPI_DATA_P	I/O	MIPI-DSI I/O	DSI Positive polarity of low voltage differential data signal ***Leave the pin open when not in use.***
MIPI_DATA_N	I/O	MIPI-DSI I/O	DSI Negative polarity of low voltage differential data signal ***Leave the pin open when not in use.***
DB [23:0]	I/O	Digital I/O	<table><tr><th>Interface Mode</th><th>Data Pin in Use</th></tr><tr><td>MIPI-DBI Type B 24-bit bus (DB_EN = 1)</td><td>DB [23:0]</td></tr><tr><td>MIPI-DBI Type B 18-bit bus (DB_EN = 0)</td><td>DB [17:0]</td></tr><tr><td>MIPI-DBI Type B 16-bit bus</td><td>DB [15:0]</td></tr><tr><td>MIPI-DBI Type B 9-bit bus</td><td>DB [8:0]</td></tr><tr><td>MIPI-DBI Type B 8-bit bus</td><td>DB [7:0]</td></tr><tr><td>MIPI-DPI 24-bit</td><td>DB [23:0]</td></tr><tr><td>MIPI-DPI 18-bit</td><td>DB [17:0]</td></tr><tr><td>MIPI-DPI 16-bit</td><td>DB [15:0]</td></tr></table>***Fix to DGND level when not in use.***
VSYNC	I	Digital Input	DPI: Frame synchronizing signal ***Fix to DGND level when not in use.***
HSYNC	I	Digital Input	DPI: Line synchronizing signal ***Fix to DGND level when not in use.***
ENABLE	I	Digital Input	DPI: A data ENABLE input signal ***Fix to DGND level when not in use.***
DOTCLK	I	Digital Input	DPI: Dot clock signal ***Fix to DGND level when not in use.***

LCD Driving Signals			
Pin Name	I/O	Type	Descriptions
S960~S1	O	Source Output	Source output voltage signals applied to the liquid crystal ***Leave the pin open when not in use.***

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G480~G1	O	Gate Output	Gate driver output pins VGH: the level selecting gate lines VGL: the level not selecting gate lines ***Leave the pin open when not in use.***
VCOM	O	LCD Output	The common voltage in DC VCOM driving The voltage range is set between -2V to 0V.
VGS	I	Power GND	Reference level for grayscale generating circuit ***Fix to GND level***

Charge-pump and Regulator Circuit			
Pin Name	I/O	Type	Descriptions
DDVDH	O	Charge Pump Output	Power supply for the source driver and VCOM driver. Input voltage from the set-up circuit (4.5 to 6V). ***Connect to a stabilizing capacitor between DDVDH and GND.***
DDVDL	O	Charge Pump Output	Power supply for the source driver and VCOM driver. Input voltage from the set-up circuit (-6 to -4.5V). ***Connect to a stabilizing capacitor between DDVDL and GND.***
VGH	O	Charge Pump Output	Power supply for the gate driver ***Connect to a stabilizing capacitor between VGH and GND.***
VGL	O	Charge Pump Output	Power supply for the gate driver ***Connect to a stabilizing capacitor between VGL and GND.***
VCL	O	Charge Pump Output	VCL = -VCI ~ -2 ***Connect to a stabilizing capacitor between VCL and GND.***
MIPI_LDO	O	LDO Output	MIPI DSI core power pad ***Connect to a stabilizing capacitor between MIPI_LDO and GND when operating in the MIPI DSI Interface.*** ***Leave the pin open when not in use.***
C52A, C52B C51A, C51B C41A, C41B C11A, C11B C12A, C12B	O	Analog Output	Capacitor connection pins for the step-up circuit 1 ***Connect to a stabilizing capacitor between C51A and C51B.*** ***Connect to a stabilizing capacitor between C52A and C52B.*** ***Connect to a stabilizing capacitor between C41A and C41B.*** ***Connect to a stabilizing capacitor between C11A and C11B.*** ***Connect to a stabilizing capacitor between C12A and C12B.***
C21A, C21B	O	Analog Output	Capacitor connection pins for the step-up circuit 2. ***Connect to a stabilizing capacitor between C21A and C21B.***

Power Pads			
Pin Name	I/O	Type	Descriptions

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VCI	P	Power Supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V. ***Connect to a stabilizing capacitor between VCI and GND.***
IOVCC	P	Power Supply	A supply voltage to the digital circuit. Connect to an external power supply of 1.65 ~ 3.3V.
VDD (VCORE)	O	Power Supply	Internal logic voltage output ***Connect to a stabilizing capacitor between VDD and GND.***
DGND	P	Power GND	Ground for the internal logic: DGND = 0V ***When using COG, connect to GND on the FPC to prevent noise.***
AGND	P	Power GND	AGND for the analog side: AGND = 0V ***When using COG, connect to GND on the FPC to prevent noise.***

Test Pads			
Pin Name	I/O	Type	Descriptions
DUMMY	-	-	Dummy pad ***Leave the pin open when not in use.***
TS [2:0]	I	-	Test pins, these pins are internal weak pull low. ***Leave the pin open when not in use.***
TESTP	I	Power GND	Test pins. ***Leave the pin open when not in use.***

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3.4. Pad Assignment

Chip Size: 22828um x 758um

Chip thickness : 280um (typ.)

Pad Location: Pad Center.

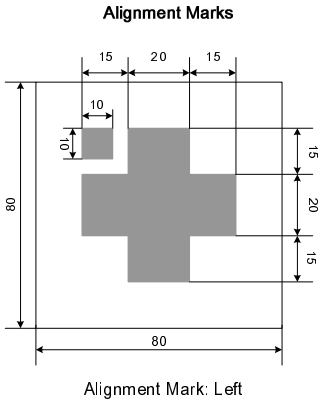
Coordinate Origin: Chip center location

Au bump height: 9um (typ.)

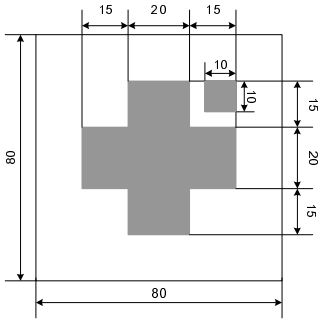
Au Bump Size:

1. 15um x 100um
   Gate: G1 ~ G480
   Source: S1 ~ S960

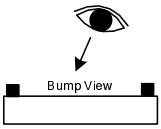
2. 50um x 80um
   Input Pads
   Pad 1 to 320.

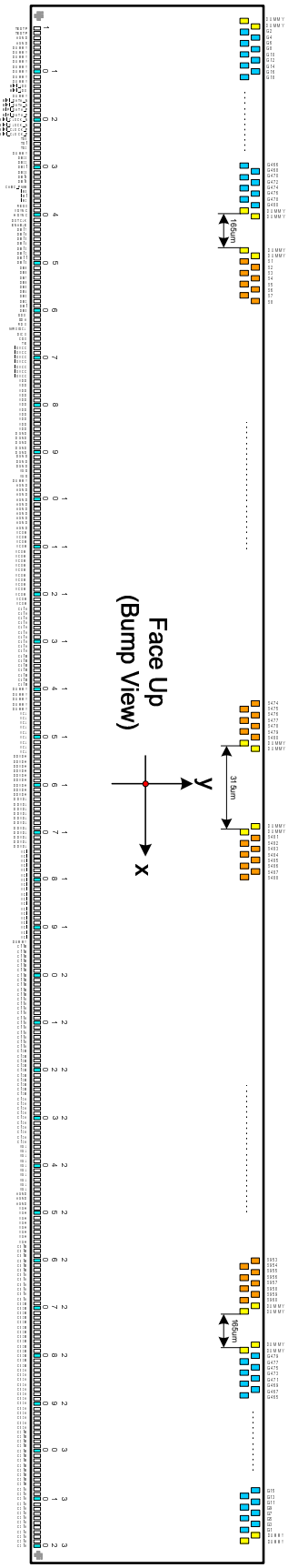


Alignment Mark: Left



Alignment Mark: Right





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3.5.Pad Coordination

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	TESTP	-11165	-279	49	DB11	-7805	-279	97	AGND	-4445	-279
2	TESTP	-11095	-279	50	DB10	-7735	-279	98	AGND	-4375	-279
3	AGND	-11025	-279	51	DB9	-7665	-279	99	AGND	-4305	-279
4	AGND	-10955	-279	52	DB8	-7595	-279	100	AGND	-4235	-279
5	DUMMY	-10885	-279	53	DB7	-7525	-279	101	AGND	-4165	-279
6	DUMMY	-10815	-279	54	DB6	-7455	-279	102	AGND	-4095	-279
7	DUMMY	-10745	-279	55	DB5	-7385	-279	103	AGND	-4025	-279
8	DUMMY	-10675	-279	56	DB4	-7315	-279	104	AGND	-3955	-279
9	DUMMY	-10605	-279	57	DB3	-7245	-279	105	AGND	-3885	-279
10	DUMMY	-10535	-279	58	DB2	-7175	-279	106	AGND	-3815	-279
11	DUMMY	-10465	-279	59	DB1	-7105	-279	107	VCOM	-3745	-279
12	DUMMY	-10395	-279	60	DB0	-7035	-279	108	VCOM	-3675	-279
13	MIPI_LDO	-10325	-279	61	SDO	-6965	-279	109	VCOM	-3605	-279
14	MIPI_LDO	-10255	-279	62	SDA	-6895	-279	110	VCOM	-3535	-279
15	DUMMY	-10185	-279	63	RDX	-6825	-279	111	VCOM	-3465	-279
16	MIPI_DATA_N	-10115	-279	64	WRX/SCL	-6755	-279	112	VCOM	-3395	-279
17	MIPI_DATA_N	-10045	-279	65	D/CX	-6685	-279	113	VCOM	-3325	-279
18	MIPI_DATA_P	-9975	-279	66	CSX	-6615	-279	114	VCOM	-3255	-279
19	MIPI_DATA_P	-9905	-279	67	TE	-6545	-279	115	VCOM	-3185	-279
20	MIPI_CLOCK_N	-9835	-279	68	IOVCC	-6475	-279	116	VCOM	-3115	-279
21	MIPI_CLOCK_N	-9765	-279	69	IOVCC	-6405	-279	117	VCOM	-3045	-279
22	MIPI_CLOCK_P	-9695	-279	70	IOVCC	-6335	-279	118	VCOM	-2975	-279
23	MIPI_CLOCK_P	-9625	-279	71	IOVCC	-6265	-279	119	VCOM	-2905	-279
24	TS0	-9555	-279	72	IOVCC	-6195	-279	120	VCOM	-2835	-279
25	TS1	-9485	-279	73	IOVCC	-6125	-279	121	VCOM	-2765	-279
26	TS2	-9415	-279	74	IOVCC	-6055	-279	122	VCOM	-2695	-279
27	DUMMY	-9345	-279	75	VDD	-5985	-279	123	C41A	-2625	-279
28	DB23	-9275	-279	76	VDD	-5915	-279	124	C41A	-2555	-279
29	DB22	-9205	-279	77	VDD	-5845	-279	125	C41A	-2485	-279
30	DB21	-9135	-279	78	VDD	-5775	-279	126	C41A	-2415	-279
31	DB20	-9065	-279	79	VDD	-5705	-279	127	C41A	-2345	-279
32	DB19	-8995	-279	80	VDD	-5635	-279	128	C41A	-2275	-279
33	DB18	-8925	-279	81	VDD	-5565	-279	129	C41A	-2205	-279
34	CABC_PWM	-8855	-279	82	VDD	-5495	-279	130	C41A	-2135	-279
35	IM0	-8785	-279	83	VDD	-5425	-279	131	C41A	-2065	-279
36	IM1	-8715	-279	84	VDD	-5355	-279	132	C41A	-1995	-279
37	IM2	-8645	-279	85	VDD	-5285	-279	133	C41B	-1925	-279
38	RESX	-8575	-279	86	DGND	-5215	-279	134	C41B	-1855	-279
39	VSYNC	-8505	-279	87	DGND	-5145	-279	135	C41B	-1785	-279
40	HSYNC	-8435	-279	88	DGND	-5075	-279	136	C41B	-1715	-279
41	DOTCLK	-8365	-279	89	DGND	-5005	-279	137	C41B	-1645	-279
42	ENABLE	-8295	-279	90	DGND	-4935	-279	138	C41B	-1575	-279
43	DB17	-8225	-279	91	DGND	-4865	-279	139	C41B	-1505	-279
44	DB16	-8155	-279	92	DGND	-4795	-279	140	DUMMY	-1435	-279
45	DB15	-8085	-279	93	DGND	-4725	-279	141	DUMMY	-1365	-279
46	DB14	-8015	-279	94	VGS	-4655	-279	142	DUMMY	-1295	-279
47	DB13	-7945	-279	95	VGS	-4585	-279	143	DUMMY	-1225	-279
48	DB12	-7875	-279	96	DUMMY	-4515	-279	144	DUMMY	-1155	-279

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
145	VCL	-1085	-279	195	C11B	2415	-279	245	VGL	5915	-279	295	C52A	9415	-279
146	VCL	-1015	-279	196	C11B	2485	-279	246	AGND	5985	-279	296	C21B	9485	-279
147	VCL	-945	-279	197	C11B	2555	-279	247	AGND	6055	-279	297	C21B	9555	-279
148	VCL	-875	-279	198	C11B	2625	-279	248	AGND	6125	-279	298	C21B	9625	-279
149	VCL	-805	-279	199	C11B	2695	-279	249	VGH	6195	-279	299	C21B	9695	-279
150	VCL	-735	-279	200	C11B	2765	-279	250	VGH	6265	-279	300	C21B	9765	-279
151	VCL	-665	-279	201	C11B	2835	-279	251	VGH	6335	-279	301	C21B	9835	-279
152	VCL	-595	-279	202	C11B	2905	-279	252	VGH	6405	-279	302	C21B	9905	-279
153	VCL	-525	-279	203	C11B	2975	-279	253	VGH	6475	-279	303	C21B	9975	-279
154	DDVDH	-455	-279	204	C11B	3045	-279	254	VGH	6545	-279	304	C21B	10045	-279
155	DDVDH	-385	-279	205	C11A	3115	-279	255	VGH	6615	-279	305	C21B	10115	-279
156	DDVDH	-315	-279	206	C11A	3185	-279	256	VGH	6685	-279	306	C21B	10185	-279
157	DDVDH	-245	-279	207	C11A	3255	-279	257	C51B	6755	-279	307	C21B	10255	-279
158	DDVDH	-175	-279	208	C11A	3325	-279	258	C51B	6825	-279	308	C21A	10325	-279
159	DDVDH	-105	-279	209	C11A	3395	-279	259	C51B	6895	-279	309	C21A	10395	-279
160	DDVDH	-35	-279	210	C11A	3465	-279	260	C51B	6965	-279	310	C21A	10465	-279
161	DDVDH	35	-279	211	C11A	3535	-279	261	C51B	7035	-279	311	C21A	10535	-279
162	DDVDH	105	-279	212	C11A	3605	-279	262	C51B	7105	-279	312	C21A	10605	-279
163	DDVDL	175	-279	213	C11A	3675	-279	263	C51A	7175	-279	313	C21A	10675	-279
164	DDVDL	245	-279	214	C11A	3745	-279	264	C51A	7245	-279	314	C21A	10745	-279
165	DDVDL	315	-279	215	C11A	3815	-279	265	C51A	7315	-279	315	C21A	10815	-279
166	DDVDL	385	-279	216	C12B	3885	-279	266	C51A	7385	-279	316	C21A	10885	-279
167	DDVDL	455	-279	217	C12B	3955	-279	267	C51A	7455	-279	317	C21A	10955	-279
168	DDVDL	525	-279	218	C12B	4025	-279	268	C51A	7525	-279	318	C21A	11025	-279
169	DDVDL	595	-279	219	C12B	4095	-279	269	C52B	7595	-279	319	C21A	11095	-279
170	DDVDL	665	-279	220	C12B	4165	-279	270	C52B	7665	-279	320	C21A	11165	-279
171	DDVDL	735	-279	221	C12B	4235	-279	271	C52B	7735	-279	321	DUMMY	11205	164
172	DDVDL	805	-279	222	C12B	4305	-279	272	C52B	7805	-279	322	DUMMY	11190	289
173	DDVDL	875	-279	223	C12B	4375	-279	273	C52B	7875	-279	323	G1	11175	164
174	VCI	945	-279	224	C12B	4445	-279	274	C52B	7945	-279	324	G3	11160	289
175	VCI	1015	-279	225	C12B	4515	-279	275	C52B	8015	-279	325	G5	11145	164
176	VCI	1085	-279	226	C12A	4585	-279	276	C52B	8085	-279	326	G7	11130	289
177	VCI	1155	-279	227	C12A	4655	-279	277	C52B	8155	-279	327	G9	11115	164
178	VCI	1225	-279	228	C12A	4725	-279	278	C52B	8225	-279	328	G11	11100	289
179	VCI	1295	-279	229	C12A	4795	-279	279	C52B	8295	-279	329	G13	11085	164
180	VCI	1365	-279	230	C12A	4865	-279	280	C52B	8365	-279	330	G15	11070	289
181	VCI	1435	-279	231	C12A	4935	-279	281	C52B	8435	-279	331	G17	11055	164
182	VCI	1505	-279	232	C12A	5005	-279	282	C52B	8505	-279	332	G19	11040	289
183	VCI	1575	-279	233	C12A	5075	-279	283	C52A	8575	-279	333	G21	11025	164
184	VCI	1645	-279	234	C12A	5145	-279	284	C52A	8645	-279	334	G23	11010	289
185	VCI	1715	-279	235	C12A	5215	-279	285	C52A	8715	-279	335	G25	10995	164
186	VCI	1785	-279	236	VGL	5285	-279	286	C52A	8785	-279	336	G27	10980	289
187	VCI	1855	-279	237	VGL	5355	-279	287	C52A	8855	-279	337	G29	10965	164
188	VCI	1925	-279	238	VGL	5425	-279	288	C52A	8925	-279	338	G31	10950	289
189	VCI	1995	-279	239	VGL	5495	-279	289	C52A	8995	-279	339	G33	10935	164
190	VCI	2065	-279	240	VGL	5565	-279	290	C52A	9065	-279	340	G35	10920	289
191	VCI	2135	-279	241	VGL	5635	-279	291	C52A	9135	-279	341	G37	10905	164
192	VCI	2205	-279	242	VGL	5705	-279	292	C52A	9205	-279	342	G39	10890	289
193	DUMMY	2275	-279	243	VGL	5775	-279	293	C52A	9275	-279	343	G41	10875	164
194	C11B	2345	-279	244	VGL	5845	-279	294	C52A	9345	-279	344	G43	10860	289

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
345	G45	10845	164	395	G145	10095	164	445	G245	9345	164	495	G345	8595	164
346	G47	10830	289	396	G147	10080	289	446	G247	9330	289	496	G347	8580	289
347	G49	10815	164	397	G149	10065	164	447	G249	9315	164	497	G349	8565	164
348	G51	10800	289	398	G151	10050	289	448	G251	9300	289	498	G351	8550	289
349	G53	10785	164	399	G153	10035	164	449	G253	9285	164	499	G353	8535	164
350	G55	10770	289	400	G155	10020	289	450	G255	9270	289	500	G355	8520	289
351	G57	10755	164	401	G157	10005	164	451	G257	9255	164	501	G357	8505	164
352	G59	10740	289	402	G159	9990	289	452	G259	9240	289	502	G359	8490	289
353	G61	10725	164	403	G161	9975	164	453	G261	9225	164	503	G361	8475	164
354	G63	10710	289	404	G163	9960	289	454	G263	9210	289	504	G363	8460	289
355	G65	10695	164	405	G165	9945	164	455	G265	9195	164	505	G365	8445	164
356	G67	10680	289	406	G167	9930	289	456	G267	9180	289	506	G367	8430	289
357	G69	10665	164	407	G169	9915	164	457	G269	9165	164	507	G369	8415	164
358	G71	10650	289	408	G171	9900	289	458	G271	9150	289	508	G371	8400	289
359	G73	10635	164	409	G173	9885	164	459	G273	9135	164	509	G373	8385	164
360	G75	10620	289	410	G175	9870	289	460	G275	9120	289	510	G375	8370	289
361	G77	10605	164	411	G177	9855	164	461	G277	9105	164	511	G377	8355	164
362	G79	10590	289	412	G179	9840	289	462	G279	9090	289	512	G379	8340	289
363	G81	10575	164	413	G181	9825	164	463	G281	9075	164	513	G381	8325	164
364	G83	10560	289	414	G183	9810	289	464	G283	9060	289	514	G383	8310	289
365	G85	10545	164	415	G185	9795	164	465	G285	9045	164	515	G385	8295	164
366	G87	10530	289	416	G187	9780	289	466	G287	9030	289	516	G387	8280	289
367	G89	10515	164	417	G189	9765	164	467	G289	9015	164	517	G389	8265	164
368	G91	10500	289	418	G191	9750	289	468	G291	9000	289	518	G391	8250	289
369	G93	10485	164	419	G193	9735	164	469	G293	8985	164	519	G393	8235	164
370	G95	10470	289	420	G195	9720	289	470	G295	8970	289	520	G395	8220	289
371	G97	10455	164	421	G197	9705	164	471	G297	8955	164	521	G397	8205	164
372	G99	10440	289	422	G199	9690	289	472	G299	8940	289	522	G399	8190	289
373	G101	10425	164	423	G201	9675	164	473	G301	8925	164	523	G401	8175	164
374	G103	10410	289	424	G203	9660	289	474	G303	8910	289	524	G403	8160	289
375	G105	10395	164	425	G205	9645	164	475	G305	8895	164	525	G405	8145	164
376	G107	10380	289	426	G207	9630	289	476	G307	8880	289	526	G407	8130	289
377	G109	10365	164	427	G209	9615	164	477	G309	8865	164	527	G409	8115	164
378	G111	10350	289	428	G211	9600	289	478	G311	8850	289	528	G411	8100	289
379	G113	10335	164	429	G213	9585	164	479	G313	8835	164	529	G413	8085	164
380	G115	10320	289	430	G215	9570	289	480	G315	8820	289	530	G415	8070	289
381	G117	10305	164	431	G217	9555	164	481	G317	8805	164	531	G417	8055	164
382	G119	10290	289	432	G219	9540	289	482	G319	8790	289	532	G419	8040	289
383	G121	10275	164	433	G221	9525	164	483	G321	8775	164	533	G421	8025	164
384	G123	10260	289	434	G223	9510	289	484	G323	8760	289	534	G423	8010	289
385	G125	10245	164	435	G225	9495	164	485	G325	8745	164	535	G425	7995	164
386	G127	10230	289	436	G227	9480	289	486	G327	8730	289	536	G427	7980	289
387	G129	10215	164	437	G229	9465	164	487	G329	8715	164	537	G429	7965	164
388	G131	10200	289	438	G231	9450	289	488	G331	8700	289	538	G431	7950	289
389	G133	10185	164	439	G233	9435	164	489	G333	8685	164	539	G433	7935	164
390	G135	10170	289	440	G235	9420	289	490	G335	8670	289	540	G435	7920	289
391	G137	10155	164	441	G237	9405	164	491	G337	8655	164	541	G437	7905	164
392	G139	10140	289	442	G239	9390	289	492	G339	8640	289	542	G439	7890	289
393	G141	10125	164	443	G241	9375	164	493	G341	8625	164	543	G441	7875	164
394	G143	10110	289	444	G243	9360	289	494	G343	8610	289	544	G443	7860	289

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
545	G445	7845	164	595	S932	6945	164	645	S882	6195	164	695	S832	5445	164
546	G447	7830	289	596	S931	6930	289	646	S881	6180	289	696	S831	5430	289
547	G449	7815	164	597	S930	6915	164	647	S880	6165	164	697	S830	5415	164
548	G451	7800	289	598	S929	6900	289	648	S879	6150	289	698	S829	5400	289
549	G453	7785	164	599	S928	6885	164	649	S878	6135	164	699	S828	5385	164
550	G455	7770	289	600	S927	6870	289	650	S877	6120	289	700	S827	5370	289
551	G457	7755	164	601	S926	6855	164	651	S876	6105	164	701	S826	5355	164
552	G459	7740	289	602	S925	6840	289	652	S875	6090	289	702	S825	5340	289
553	G461	7725	164	603	S924	6825	164	653	S874	6075	164	703	S824	5325	164
554	G463	7710	289	604	S923	6810	289	654	S873	6060	289	704	S823	5310	289
555	G465	7695	164	605	S922	6795	164	655	S872	6045	164	705	S822	5295	164
556	G467	7680	289	606	S921	6780	289	656	S871	6030	289	706	S821	5280	289
557	G469	7665	164	607	S920	6765	164	657	S870	6015	164	707	S820	5265	164
558	G471	7650	289	608	S919	6750	289	658	S869	6000	289	708	S819	5250	289
559	G473	7635	164	609	S918	6735	164	659	S868	5985	164	709	S818	5235	164
560	G475	7620	289	610	S917	6720	289	660	S867	5970	289	710	S817	5220	289
561	G477	7605	164	611	S916	6705	164	661	S866	5955	164	711	S816	5205	164
562	G479	7590	289	612	S915	6690	289	662	S865	5940	289	712	S815	5190	289
563	DUMMY	7575	164	613	S914	6675	164	663	S864	5925	164	713	S814	5175	164
564	DUMMY	7560	289	614	S913	6660	289	664	S863	5910	289	714	S813	5160	289
565	DUMMY	7395	164	615	S912	6645	164	665	S862	5895	164	715	S812	5145	164
566	DUMMY	7380	289	616	S911	6630	289	666	S861	5880	289	716	S811	5130	289
567	S960	7365	164	617	S910	6615	164	667	S860	5865	164	717	S810	5115	164
568	S959	7350	289	618	S909	6600	289	668	S859	5850	289	718	S809	5100	289
569	S958	7335	164	619	S908	6585	164	669	S858	5835	164	719	S808	5085	164
570	S957	7320	289	620	S907	6570	289	670	S857	5820	289	720	S807	5070	289
571	S956	7305	164	621	S906	6555	164	671	S856	5805	164	721	S806	5055	164
572	S955	7290	289	622	S905	6540	289	672	S855	5790	289	722	S805	5040	289
573	S954	7275	164	623	S904	6525	164	673	S854	5775	164	723	S804	5025	164
574	S953	7260	289	624	S903	6510	289	674	S853	5760	289	724	S803	5010	289
575	S952	7245	164	625	S902	6495	164	675	S852	5745	164	725	S802	4995	164
576	S951	7230	289	626	S901	6480	289	676	S851	5730	289	726	S801	4980	289
577	S950	7215	164	627	S900	6465	164	677	S850	5715	164	727	S800	4965	164
578	S949	7200	289	628	S899	6450	289	678	S849	5700	289	728	S799	4950	289
579	S948	7185	164	629	S898	6435	164	679	S848	5685	164	729	S798	4935	164
580	S947	7170	289	630	S897	6420	289	680	S847	5670	289	730	S797	4920	289
581	S946	7155	164	631	S896	6405	164	681	S846	5655	164	731	S796	4905	164
582	S945	7140	289	632	S895	6390	289	682	S845	5640	289	732	S795	4890	289
583	S944	7125	164	633	S894	6375	164	683	S844	5625	164	733	S794	4875	164
584	S943	7110	289	634	S893	6360	289	684	S843	5610	289	734	S793	4860	289
585	S942	7095	164	635	S892	6345	164	685	S842	5595	164	735	S792	4845	164
586	S941	7080	289	636	S891	6330	289	686	S841	5580	289	736	S791	4830	289
587	S940	7065	164	637	S890	6315	164	687	S840	5565	164	737	S790	4815	164
588	S939	7050	289	638	S889	6300	289	688	S839	5550	289	738	S789	4800	289
589	S938	7035	164	639	S888	6285	164	689	S838	5535	164	739	S788	4785	164
590	S937	7020	289	640	S887	6270	289	690	S837	5520	289	740	S787	4770	289
591	S936	7005	164	641	S886	6255	164	691	S836	5505	164	741	S786	4755	164
592	S935	6990	289	642	S885	6240	289	692	S835	5490	289	742	S785	4740	289
593	S934	6975	164	643	S884	6225	164	693	S834	5475	164	743	S784	4725	164
594	S933	6960	289	644	S883	6210	289	694	S833	5460	289	744	S783	4710	289

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
745	S782	4695	164	795	S732	3945	164	845	S682	3195	164	895	S632	2445	164
746	S781	4680	289	796	S731	3930	289	846	S681	3180	289	896	S631	2430	289
747	S780	4665	164	797	S730	3915	164	847	S680	3165	164	897	S630	2415	164
748	S779	4650	289	798	S729	3900	289	848	S679	3150	289	898	S629	2400	289
749	S778	4635	164	799	S728	3885	164	849	S678	3135	164	899	S628	2385	164
750	S777	4620	289	800	S727	3870	289	850	S677	3120	289	900	S627	2370	289
751	S776	4605	164	801	S726	3855	164	851	S676	3105	164	901	S626	2355	164
752	S775	4590	289	802	S725	3840	289	852	S675	3090	289	902	S625	2340	289
753	S774	4575	164	803	S724	3825	164	853	S674	3075	164	903	S624	2325	164
754	S773	4560	289	804	S723	3810	289	854	S673	3060	289	904	S623	2310	289
755	S772	4545	164	805	S722	3795	164	855	S672	3045	164	905	S622	2295	164
756	S771	4530	289	806	S721	3780	289	856	S671	3030	289	906	S621	2280	289
757	S770	4515	164	807	S720	3765	164	857	S670	3015	164	907	S620	2265	164
758	S769	4500	289	808	S719	3750	289	858	S669	3000	289	908	S619	2250	289
759	S768	4485	164	809	S718	3735	164	859	S668	2985	164	909	S618	2235	164
760	S767	4470	289	810	S717	3720	289	860	S667	2970	289	910	S617	2220	289
761	S766	4455	164	811	S716	3705	164	861	S666	2955	164	911	S616	2205	164
762	S765	4440	289	812	S715	3690	289	862	S665	2940	289	912	S615	2190	289
763	S764	4425	164	813	S714	3675	164	863	S664	2925	164	913	S614	2175	164
764	S763	4410	289	814	S713	3660	289	864	S663	2910	289	914	S613	2160	289
765	S762	4395	164	815	S712	3645	164	865	S662	2895	164	915	S612	2145	164
766	S761	4380	289	816	S711	3630	289	866	S661	2880	289	916	S611	2130	289
767	S760	4365	164	817	S710	3615	164	867	S660	2865	164	917	S610	2115	164
768	S759	4350	289	818	S709	3600	289	868	S659	2850	289	918	S609	2100	289
769	S758	4335	164	819	S708	3585	164	869	S658	2835	164	919	S608	2085	164
770	S757	4320	289	820	S707	3570	289	870	S657	2820	289	920	S607	2070	289
771	S756	4305	164	821	S706	3555	164	871	S656	2805	164	921	S606	2055	164
772	S755	4290	289	822	S705	3540	289	872	S655	2790	289	922	S605	2040	289
773	S754	4275	164	823	S704	3525	164	873	S654	2775	164	923	S604	2025	164
774	S753	4260	289	824	S703	3510	289	874	S653	2760	289	924	S603	2010	289
775	S752	4245	164	825	S702	3495	164	875	S652	2745	164	925	S602	1995	164
776	S751	4230	289	826	S701	3480	289	876	S651	2730	289	926	S601	1980	289
777	S750	4215	164	827	S700	3465	164	877	S650	2715	164	927	S600	1965	164
778	S749	4200	289	828	S699	3450	289	878	S649	2700	289	928	S599	1950	289
779	S748	4185	164	829	S698	3435	164	879	S648	2685	164	929	S598	1935	164
780	S747	4170	289	830	S697	3420	289	880	S647	2670	289	930	S597	1920	289
781	S746	4155	164	831	S696	3405	164	881	S646	2655	164	931	S596	1905	164
782	S745	4140	289	832	S695	3390	289	882	S645	2640	289	932	S595	1890	289
783	S744	4125	164	833	S694	3375	164	883	S644	2625	164	933	S594	1875	164
784	S743	4110	289	834	S693	3360	289	884	S643	2610	289	934	S593	1860	289
785	S742	4095	164	835	S692	3345	164	885	S642	2595	164	935	S592	1845	164
786	S741	4080	289	836	S691	3330	289	886	S641	2580	289	936	S591	1830	289
787	S740	4065	164	837	S690	3315	164	887	S640	2565	164	937	S590	1815	164
788	S739	4050	289	838	S689	3300	289	888	S639	2550	289	938	S589	1800	289
789	S738	4035	164	839	S688	3285	164	889	S638	2535	164	939	S588	1785	164
790	S737	4020	289	840	S687	3270	289	890	S637	2520	289	940	S587	1770	289
791	S736	4005	164	841	S686	3255	164	891	S636	2505	164	941	S586	1755	164
792	S735	3990	289	842	S685	3240	289	892	S635	2490	289	942	S585	1740	289
793	S734	3975	164	843	S684	3225	164	893	S634	2475	164	943	S584	1725	164
794	S733	3960	289	844	S683	3210	289	894	S633	2460	289	944	S583	1710	289

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
945	S582	1695	164	995	S532	945	164	1045	S482	195	164	1095	S436	-840	289
946	S581	1680	289	996	S531	930	289	1046	S481	180	289	1096	S435	-855	164
947	S580	1665	164	997	S530	915	164	1047	DUMMY	165	164	1097	S434	-870	289
948	S579	1650	289	998	S529	900	289	1048	DUMMY	150	289	1098	S433	-885	164
949	S578	1635	164	999	S528	885	164	1049	DUMMY	-150	289	1099	S432	-900	289
950	S577	1620	289	1000	S527	870	289	1050	DUMMY	-165	164	1100	S431	-915	164
951	S576	1605	164	1001	S526	855	164	1051	S480	-180	289	1101	S430	-930	289
952	S575	1590	289	1002	S525	840	289	1052	S479	-195	164	1102	S429	-945	164
953	S574	1575	164	1003	S524	825	164	1053	S478	-210	289	1103	S428	-960	289
954	S573	1560	289	1004	S523	810	289	1054	S477	-225	164	1104	S427	-975	164
955	S572	1545	164	1005	S522	795	164	1055	S476	-240	289	1105	S426	-990	289
956	S571	1530	289	1006	S521	780	289	1056	S475	-255	164	1106	S425	-1005	164
957	S570	1515	164	1007	S520	765	164	1057	S474	-270	289	1107	S424	-1020	289
958	S569	1500	289	1008	S519	750	289	1058	S473	-285	164	1108	S423	-1035	164
959	S568	1485	164	1009	S518	735	164	1059	S472	-300	289	1109	S422	-1050	289
960	S567	1470	289	1010	S517	720	289	1060	S471	-315	164	1110	S421	-1065	164
961	S566	1455	164	1011	S516	705	164	1061	S470	-330	289	1111	S420	-1080	289
962	S565	1440	289	1012	S515	690	289	1062	S469	-345	164	1112	S419	-1095	164
963	S564	1425	164	1013	S514	675	164	1063	S468	-360	289	1113	S418	-1110	289
964	S563	1410	289	1014	S513	660	289	1064	S467	-375	164	1114	S417	-1125	164
965	S562	1395	164	1015	S512	645	164	1065	S466	-390	289	1115	S416	-1140	289
966	S561	1380	289	1016	S511	630	289	1066	S465	-405	164	1116	S415	-1155	164
967	S560	1365	164	1017	S510	615	164	1067	S464	-420	289	1117	S414	-1170	289
968	S559	1350	289	1018	S509	600	289	1068	S463	-435	164	1118	S413	-1185	164
969	S558	1335	164	1019	S508	585	164	1069	S462	-450	289	1119	S412	-1200	289
970	S557	1320	289	1020	S507	570	289	1070	S461	-465	164	1120	S411	-1215	164
971	S556	1305	164	1021	S506	555	164	1071	S460	-480	289	1121	S410	-1230	289
972	S555	1290	289	1022	S505	540	289	1072	S459	-495	164	1122	S409	-1245	164
973	S554	1275	164	1023	S504	525	164	1073	S458	-510	289	1123	S408	-1260	289
974	S553	1260	289	1024	S503	510	289	1074	S457	-525	164	1124	S407	-1275	164
975	S552	1245	164	1025	S502	495	164	1075	S456	-540	289	1125	S406	-1290	289
976	S551	1230	289	1026	S501	480	289	1076	S455	-555	164	1126	S405	-1305	164
977	S550	1215	164	1027	S500	465	164	1077	S454	-570	289	1127	S404	-1320	289
978	S549	1200	289	1028	S499	450	289	1078	S453	-585	164	1128	S403	-1335	164
979	S548	1185	164	1029	S498	435	164	1079	S452	-600	289	1129	S402	-1350	289
980	S547	1170	289	1030	S497	420	289	1080	S451	-615	164	1130	S401	-1365	164
981	S546	1155	164	1031	S496	405	164	1081	S450	-630	289	1131	S400	-1380	289
982	S545	1140	289	1032	S495	390	289	1082	S449	-645	164	1132	S399	-1395	164
983	S544	1125	164	1033	S494	375	164	1083	S448	-660	289	1133	S398	-1410	289
984	S543	1110	289	1034	S493	360	289	1084	S447	-675	164	1134	S397	-1425	164
985	S542	1095	164	1035	S492	345	164	1085	S446	-690	289	1135	S396	-1440	289
986	S541	1080	289	1036	S491	330	289	1086	S445	-705	164	1136	S395	-1455	164
987	S540	1065	164	1037	S490	315	164	1087	S444	-720	289	1137	S394	-1470	289
988	S539	1050	289	1038	S489	300	289	1088	S443	-735	164	1138	S393	-1485	164
989	S538	1035	164	1039	S488	285	164	1089	S442	-750	289	1139	S392	-1500	289
990	S537	1020	289	1040	S487	270	289	1090	S441	-765	164	1140	S391	-1515	164
991	S536	1005	164	1041	S486	255	164	1091	S440	-780	289	1141	S390	-1530	289
992	S535	990	289	1042	S485	240	289	1092	S439	-795	164	1142	S389	-1545	164
993	S534	975	164	1043	S484	225	164	1093	S438	-810	289	1143	S388	-1560	289
994	S533	960	289	1044	S483	210	289	1094	S437	-825	164	1144	S387	-1575	164

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1145	S386	-1590	289	1195	S336	-2340	289	1245	S286	-3090	289	1295	S236	-3840	289
1146	S385	-1605	164	1196	S335	-2355	164	1246	S285	-3105	164	1296	S235	-3855	164
1147	S384	-1620	289	1197	S334	-2370	289	1247	S284	-3120	289	1297	S234	-3870	289
1148	S383	-1635	164	1198	S333	-2385	164	1248	S283	-3135	164	1298	S233	-3885	164
1149	S382	-1650	289	1199	S332	-2400	289	1249	S282	-3150	289	1299	S232	-3900	289
1150	S381	-1665	164	1200	S331	-2415	164	1250	S281	-3165	164	1300	S231	-3915	164
1151	S380	-1680	289	1201	S330	-2430	289	1251	S280	-3180	289	1301	S230	-3930	289
1152	S379	-1695	164	1202	S329	-2445	164	1252	S279	-3195	164	1302	S229	-3945	164
1153	S378	-1710	289	1203	S328	-2460	289	1253	S278	-3210	289	1303	S228	-3960	289
1154	S377	-1725	164	1204	S327	-2475	164	1254	S277	-3225	164	1304	S227	-3975	164
1155	S376	-1740	289	1205	S326	-2490	289	1255	S276	-3240	289	1305	S226	-3990	289
1156	S375	-1755	164	1206	S325	-2505	164	1256	S275	-3255	164	1306	S225	-4005	164
1157	S374	-1770	289	1207	S324	-2520	289	1257	S274	-3270	289	1307	S224	-4020	289
1158	S373	-1785	164	1208	S323	-2535	164	1258	S273	-3285	164	1308	S223	-4035	164
1159	S372	-1800	289	1209	S322	-2550	289	1259	S272	-3300	289	1309	S222	-4050	289
1160	S371	-1815	164	1210	S321	-2565	164	1260	S271	-3315	164	1310	S221	-4065	164
1161	S370	-1830	289	1211	S320	-2580	289	1261	S270	-3330	289	1311	S220	-4080	289
1162	S369	-1845	164	1212	S319	-2595	164	1262	S269	-3345	164	1312	S219	-4095	164
1163	S368	-1860	289	1213	S318	-2610	289	1263	S268	-3360	289	1313	S218	-4110	289
1164	S367	-1875	164	1214	S317	-2625	164	1264	S267	-3375	164	1314	S217	-4125	164
1165	S366	-1890	289	1215	S316	-2640	289	1265	S266	-3390	289	1315	S216	-4140	289
1166	S365	-1905	164	1216	S315	-2655	164	1266	S265	-3405	164	1316	S215	-4155	164
1167	S364	-1920	289	1217	S314	-2670	289	1267	S264	-3420	289	1317	S214	-4170	289
1168	S363	-1935	164	1218	S313	-2685	164	1268	S263	-3435	164	1318	S213	-4185	164
1169	S362	-1950	289	1219	S312	-2700	289	1269	S262	-3450	289	1319	S212	-4200	289
1170	S361	-1965	164	1220	S311	-2715	164	1270	S261	-3465	164	1320	S211	-4215	164
1171	S360	-1980	289	1221	S310	-2730	289	1271	S260	-3480	289	1321	S210	-4230	289
1172	S359	-1995	164	1222	S309	-2745	164	1272	S259	-3495	164	1322	S209	-4245	164
1173	S358	-2010	289	1223	S308	-2760	289	1273	S258	-3510	289	1323	S208	-4260	289
1174	S357	-2025	164	1224	S307	-2775	164	1274	S257	-3525	164	1324	S207	-4275	164
1175	S356	-2040	289	1225	S306	-2790	289	1275	S256	-3540	289	1325	S206	-4290	289
1176	S355	-2055	164	1226	S305	-2805	164	1276	S255	-3555	164	1326	S205	-4305	164
1177	S354	-2070	289	1227	S304	-2820	289	1277	S254	-3570	289	1327	S204	-4320	289
1178	S353	-2085	164	1228	S303	-2835	164	1278	S253	-3585	164	1328	S203	-4335	164
1179	S352	-2100	289	1229	S302	-2850	289	1279	S252	-3600	289	1329	S202	-4350	289
1180	S351	-2115	164	1230	S301	-2865	164	1280	S251	-3615	164	1330	S201	-4365	164
1181	S350	-2130	289	1231	S300	-2880	289	1281	S250	-3630	289	1331	S200	-4380	289
1182	S349	-2145	164	1232	S299	-2895	164	1282	S249	-3645	164	1332	S199	-4395	164
1183	S348	-2160	289	1233	S298	-2910	289	1283	S248	-3660	289	1333	S198	-4410	289
1184	S347	-2175	164	1234	S297	-2925	164	1284	S247	-3675	164	1334	S197	-4425	164
1185	S346	-2190	289	1235	S296	-2940	289	1285	S246	-3690	289	1335	S196	-4440	289
1186	S345	-2205	164	1236	S295	-2955	164	1286	S245	-3705	164	1336	S195	-4455	164
1187	S344	-2220	289	1237	S294	-2970	289	1287	S244	-3720	289	1337	S194	-4470	289
1188	S343	-2235	164	1238	S293	-2985	164	1288	S243	-3735	164	1338	S193	-4485	164
1189	S342	-2250	289	1239	S292	-3000	289	1289	S242	-3750	289	1339	S192	-4500	289
1190	S341	-2265	164	1240	S291	-3015	164	1290	S241	-3765	164	1340	S191	-4515	164
1191	S340	-2280	289	1241	S290	-3030	289	1291	S240	-3780	289	1341	S190	-4530	289
1192	S339	-2295	164	1242	S289	-3045	164	1292	S239	-3795	164	1342	S189	-4545	164
1193	S338	-2310	289	1243	S288	-3060	289	1293	S238	-3810	289	1343	S188	-4560	289
1194	S337	-2325	164	1244	S287	-3075	164	1294	S237	-3825	164	1344	S187	-4575	164

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1345	S186	-4590	289	1395	S136	-5340	289	1445	S86	-6090	289	1495	S36	-6840	289
1346	S185	-4605	164	1396	S135	-5355	164	1446	S85	-6105	164	1496	S35	-6855	164
1347	S184	-4620	289	1397	S134	-5370	289	1447	S84	-6120	289	1497	S34	-6870	289
1348	S183	-4635	164	1398	S133	-5385	164	1448	S83	-6135	164	1498	S33	-6885	164
1349	S182	-4650	289	1399	S132	-5400	289	1449	S82	-6150	289	1499	S32	-6900	289
1350	S181	-4665	164	1400	S131	-5415	164	1450	S81	-6165	164	1500	S31	-6915	164
1351	S180	-4680	289	1401	S130	-5430	289	1451	S80	-6180	289	1501	S30	-6930	289
1352	S179	-4695	164	1402	S129	-5445	164	1452	S79	-6195	164	1502	S29	-6945	164
1353	S178	-4710	289	1403	S128	-5460	289	1453	S78	-6210	289	1503	S28	-6960	289
1354	S177	-4725	164	1404	S127	-5475	164	1454	S77	-6225	164	1504	S27	-6975	164
1355	S176	-4740	289	1405	S126	-5490	289	1455	S76	-6240	289	1505	S26	-6990	289
1356	S175	-4755	164	1406	S125	-5505	164	1456	S75	-6255	164	1506	S25	-7005	164
1357	S174	-4770	289	1407	S124	-5520	289	1457	S74	-6270	289	1507	S24	-7020	289
1358	S173	-4785	164	1408	S123	-5535	164	1458	S73	-6285	164	1508	S23	-7035	164
1359	S172	-4800	289	1409	S122	-5550	289	1459	S72	-6300	289	1509	S22	-7050	289
1360	S171	-4815	164	1410	S121	-5565	164	1460	S71	-6315	164	1510	S21	-7065	164
1361	S170	-4830	289	1411	S120	-5580	289	1461	S70	-6330	289	1511	S20	-7080	289
1362	S169	-4845	164	1412	S119	-5595	164	1462	S69	-6345	164	1512	S19	-7095	164
1363	S168	-4860	289	1413	S118	-5610	289	1463	S68	-6360	289	1513	S18	-7110	289
1364	S167	-4875	164	1414	S117	-5625	164	1464	S67	-6375	164	1514	S17	-7125	164
1365	S166	-4890	289	1415	S116	-5640	289	1465	S66	-6390	289	1515	S16	-7140	289
1366	S165	-4905	164	1416	S115	-5655	164	1466	S65	-6405	164	1516	S15	-7155	164
1367	S164	-4920	289	1417	S114	-5670	289	1467	S64	-6420	289	1517	S14	-7170	289
1368	S163	-4935	164	1418	S113	-5685	164	1468	S63	-6435	164	1518	S13	-7185	164
1369	S162	-4950	289	1419	S112	-5700	289	1469	S62	-6450	289	1519	S12	-7200	289
1370	S161	-4965	164	1420	S111	-5715	164	1470	S61	-6465	164	1520	S11	-7215	164
1371	S160	-4980	289	1421	S110	-5730	289	1471	S60	-6480	289	1521	S10	-7230	289
1372	S159	-4995	164	1422	S109	-5745	164	1472	S59	-6495	164	1522	S9	-7245	164
1373	S158	-5010	289	1423	S108	-5760	289	1473	S58	-6510	289	1523	S8	-7260	289
1374	S157	-5025	164	1424	S107	-5775	164	1474	S57	-6525	164	1524	S7	-7275	164
1375	S156	-5040	289	1425	S106	-5790	289	1475	S56	-6540	289	1525	S6	-7290	289
1376	S155	-5055	164	1426	S105	-5805	164	1476	S55	-6555	164	1526	S5	-7305	164
1377	S154	-5070	289	1427	S104	-5820	289	1477	S54	-6570	289	1527	S4	-7320	289
1378	S153	-5085	164	1428	S103	-5835	164	1478	S53	-6585	164	1528	S3	-7335	164
1379	S152	-5100	289	1429	S102	-5850	289	1479	S52	-6600	289	1529	S2	-7350	289
1380	S151	-5115	164	1430	S101	-5865	164	1480	S51	-6615	164	1530	S1	-7365	164
1381	S150	-5130	289	1431	S100	-5880	289	1481	S50	-6630	289	1531	DUMMY	-7380	289
1382	S149	-5145	164	1432	S99	-5895	164	1482	S49	-6645	164	1532	DUMMY	-7395	164
1383	S148	-5160	289	1433	S98	-5910	289	1483	S48	-6660	289	1533	DUMMY	-7560	289
1384	S147	-5175	164	1434	S97	-5925	164	1484	S47	-6675	164	1534	DUMMY	-7575	164
1385	S146	-5190	289	1435	S96	-5940	289	1485	S46	-6690	289	1535	G480	-7590	289
1386	S145	-5205	164	1436	S95	-5955	164	1486	S45	-6705	164	1536	G478	-7605	164
1387	S144	-5220	289	1437	S94	-5970	289	1487	S44	-6720	289	1537	G476	-7620	289
1388	S143	-5235	164	1438	S93	-5985	164	1488	S43	-6735	164	1538	G474	-7635	164
1389	S142	-5250	289	1439	S92	-6000	289	1489	S42	-6750	289	1539	G472	-7650	289
1390	S141	-5265	164	1440	S91	-6015	164	1490	S41	-6765	164	1540	G470	-7665	164
1391	S140	-5280	289	1441	S90	-6030	289	1491	S40	-6780	289	1541	G468	-7680	289
1392	S139	-5295	164	1442	S89	-6045	164	1492	S39	-6795	164	1542	G466	-7695	164
1393	S138	-5310	289	1443	S88	-6060	289	1493	S38	-6810	289	1543	G464	-7710	289
1394	S137	-5325	164	1444	S87	-6075	164	1494	S37	-6825	164	1544	G462	-7725	164

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1545	G460	-7740	289	1595	G360	-8490	289	1645	G260	-9240	289	1695	G160	-9990	289
1546	G458	-7755	164	1596	G358	-8505	164	1646	G258	-9255	164	1696	G158	-10005	164
1547	G456	-7770	289	1597	G356	-8520	289	1647	G256	-9270	289	1697	G156	-10020	289
1548	G454	-7785	164	1598	G354	-8535	164	1648	G254	-9285	164	1698	G154	-10035	164
1549	G452	-7800	289	1599	G352	-8550	289	1649	G252	-9300	289	1699	G152	-10050	289
1550	G450	-7815	164	1600	G350	-8565	164	1650	G250	-9315	164	1700	G150	-10065	164
1551	G448	-7830	289	1601	G348	-8580	289	1651	G248	-9330	289	1701	G148	-10080	289
1552	G446	-7845	164	1602	G346	-8595	164	1652	G246	-9345	164	1702	G146	-10095	164
1553	G444	-7860	289	1603	G344	-8610	289	1653	G244	-9360	289	1703	G144	-10110	289
1554	G442	-7875	164	1604	G342	-8625	164	1654	G242	-9375	164	1704	G142	-10125	164
1555	G440	-7890	289	1605	G340	-8640	289	1655	G240	-9390	289	1705	G140	-10140	289
1556	G438	-7905	164	1606	G338	-8655	164	1656	G238	-9405	164	1706	G138	-10155	164
1557	G436	-7920	289	1607	G336	-8670	289	1657	G236	-9420	289	1707	G136	-10170	289
1558	G434	-7935	164	1608	G334	-8685	164	1658	G234	-9435	164	1708	G134	-10185	164
1559	G432	-7950	289	1609	G332	-8700	289	1659	G232	-9450	289	1709	G132	-10200	289
1560	G430	-7965	164	1610	G330	-8715	164	1660	G230	-9465	164	1710	G130	-10215	164
1561	G428	-7980	289	1611	G328	-8730	289	1661	G228	-9480	289	1711	G128	-10230	289
1562	G426	-7995	164	1612	G326	-8745	164	1662	G226	-9495	164	1712	G126	-10245	164
1563	G424	-8010	289	1613	G324	-8760	289	1663	G224	-9510	289	1713	G124	-10260	289
1564	G422	-8025	164	1614	G322	-8775	164	1664	G222	-9525	164	1714	G122	-10275	164
1565	G420	-8040	289	1615	G320	-8790	289	1665	G220	-9540	289	1715	G120	-10290	289
1566	G418	-8055	164	1616	G318	-8805	164	1666	G218	-9555	164	1716	G118	-10305	164
1567	G416	-8070	289	1617	G316	-8820	289	1667	G216	-9570	289	1717	G116	-10320	289
1568	G414	-8085	164	1618	G314	-8835	164	1668	G214	-9585	164	1718	G114	-10335	164
1569	G412	-8100	289	1619	G312	-8850	289	1669	G212	-9600	289	1719	G112	-10350	289
1570	G410	-8115	164	1620	G310	-8865	164	1670	G210	-9615	164	1720	G110	-10365	164
1571	G408	-8130	289	1621	G308	-8880	289	1671	G208	-9630	289	1721	G108	-10380	289
1572	G406	-8145	164	1622	G306	-8895	164	1672	G206	-9645	164	1722	G106	-10395	164
1573	G404	-8160	289	1623	G304	-8910	289	1673	G204	-9660	289	1723	G104	-10410	289
1574	G402	-8175	164	1624	G302	-8925	164	1674	G202	-9675	164	1724	G102	-10425	164
1575	G400	-8190	289	1625	G300	-8940	289	1675	G200	-9690	289	1725	G100	-10440	289
1576	G398	-8205	164	1626	G298	-8955	164	1676	G198	-9705	164	1726	G98	-10455	164
1577	G396	-8220	289	1627	G296	-8970	289	1677	G196	-9720	289	1727	G96	-10470	289
1578	G394	-8235	164	1628	G294	-8985	164	1678	G194	-9735	164	1728	G94	-10485	164
1579	G392	-8250	289	1629	G292	-9000	289	1679	G192	-9750	289	1729	G92	-10500	289
1580	G390	-8265	164	1630	G290	-9015	164	1680	G190	-9765	164	1730	G90	-10515	164
1581	G388	-8280	289	1631	G288	-9030	289	1681	G188	-9780	289	1731	G88	-10530	289
1582	G386	-8295	164	1632	G286	-9045	164	1682	G186	-9795	164	1732	G86	-10545	164
1583	G384	-8310	289	1633	G284	-9060	289	1683	G184	-9810	289	1733	G84	-10560	289
1584	G382	-8325	164	1634	G282	-9075	164	1684	G182	-9825	164	1734	G82	-10575	164
1585	G380	-8340	289	1635	G280	-9090	289	1685	G180	-9840	289	1735	G80	-10590	289
1586	G378	-8355	164	1636	G278	-9105	164	1686	G178	-9855	164	1736	G78	-10605	164
1587	G376	-8370	289	1637	G276	-9120	289	1687	G176	-9870	289	1737	G76	-10620	289
1588	G374	-8385	164	1638	G274	-9135	164	1688	G174	-9885	164	1738	G74	-10635	164
1589	G372	-8400	289	1639	G272	-9150	289	1689	G172	-9900	289	1739	G72	-10650	289
1590	G370	-8415	164	1640	G270	-9165	164	1690	G170	-9915	164	1740	G70	-10665	164
1591	G368	-8430	289	1641	G268	-9180	289	1691	G168	-9930	289	1741	G68	-10680	289
1592	G366	-8445	164	1642	G266	-9195	164	1692	G166	-9945	164	1742	G66	-10695	164
1593	G364	-8460	289	1643	G264	-9210	289	1693	G164	-9960	289	1743	G64	-10710	289
1594	G362	-8475	164	1644	G262	-9225	164	1694	G162	-9975	164	1744	G62	-10725	164

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No.	Name	X	Y
1745	G60	-10740	289
1746	G58	-10755	164
1747	G56	-10770	289
1748	G54	-10785	164
1749	G52	-10800	289
1750	G50	-10815	164
1751	G48	-10830	289
1752	G46	-10845	164
1753	G44	-10860	289
1754	G42	-10875	164
1755	G40	-10890	289
1756	G38	-10905	164
1757	G36	-10920	289
1758	G34	-10935	164
1759	G32	-10950	289
1760	G30	-10965	164
1761	G28	-10980	289
1762	G26	-10995	164
1763	G24	-11010	289
1764	G22	-11025	164
1765	G20	-11040	289
1766	G18	-11055	164
1767	G16	-11070	289
1768	G14	-11085	164
1769	G12	-11100	289
1770	G10	-11115	164
1771	G8	-11130	289
1772	G6	-11145	164
1773	G4	-11160	289
1774	G2	-11175	164
1775	DUMMY	-11190	289
1776	DUMMY	-11205	164
Alignment mark -Left		-11300	-270
Alignment mark -Right		11300	-270

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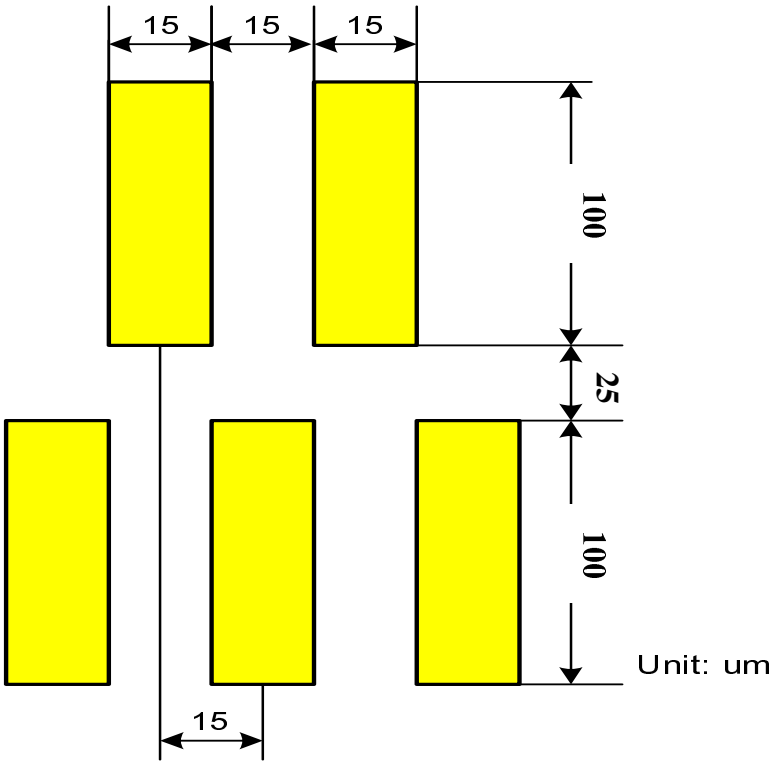
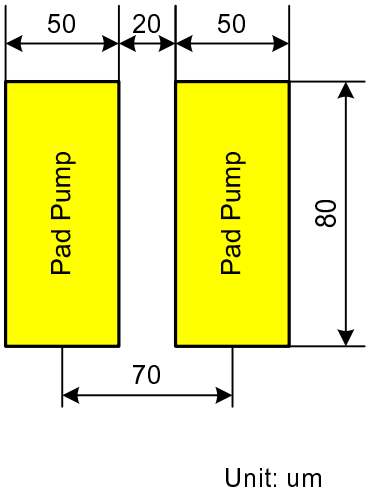
3.6. Bump Arrangement

S1 ~ S960 G1 ~ G480 (No. 321 ~ 1776)	
I/O pads (No.1 ~ 320)	

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4. System Interfaces

The ILI9488 supports MIPI DBI, DPI, and DSI. DBI supports (8-/9-/16-/18-/24-bit interface) Parallel Interface (Type B) and Serial Interface (Type C). The interface mode can be selected by IM [2:0] pins, as shown in Table 3 below.

Table 3: Interface Selection

IM2	IM1	IM0	Interface	Data Pins in Use	
				Command/Parameter	GRAM
0	0	0	DBI Type B 24-bit (DB_EN = 1)	DB [7:0]	DB [23:0]: 24-bits Data
0	0	0	DBI Type B 18-bit (DB_EN = 0)	DB [7:0]	DB [17:0]: 18-bits Data
0	0	1	DBI Type B 9-bit	DB [7:0]	DB [8:0]: 9-bits Data
0	1	0	DBI Type B 16-bit	DB [7:0]	DB [15:0]: 16-bits Data
0	1	1	DBI Type B 8-bit	DB [7:0]	DB [7:0]: 8-bits Data
1	0	1	DBI Type C Option 1 (3-line SPI)	SDA/SDO	
1	1	0	DSI	MIPI_DATA_P, MIPI_DATA_N, MIPI_CLOCK_P, MIPI_CLOCK_N	
1	1	1	DBI Type C Option 3 (4-line SPI)	SDA/SDO	

4.1. DBI Type B Parallel Interface

The ILI9488 includes an Index Register (IR), which stores the index data of internal Control Register (CR) and GRAM. The chip-select D/CX (active low) is used to enable or disable the ILI9488 chip. The RESX (active low) is an external reset signal, the WRX is a parallel data write strobe, the RDX is a parallel data read strobe, and DB [23:0] is a parallel data bus.

The ILI9488 latches the input data at the rising edge of the WRX signal. The D/CX is the signal for data/command selection. When D/CX = 1, DB [23:0] bits are RAM data or command parameters. When D/CX = 0, DB [23:0] bits are commands. The DBI Type B bi-directional interface is used for communication between the MCU controller and the LCD driver chip. The selection and operation of the parallel interface is shown in Table 4.

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Table 4: DBI Type B Parallel Interface

IM2	IM1	IM0	MPU-Interface Mode	WRX	RDX	D/CX	Function
0	0	0	DBI Type B 24-bit (DB_EN = 1)	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data
0	0	0	DBI Type B 18-bit (DB_EN = 0)	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data
0	0	1	DBI Type B 9-bit	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data
0	1	0	DBI Type B 16-bit	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data
0	1	1	DBI Type B 8-bit	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data

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4.1.1. Write Cycle Sequence

The WRX signal is driven from high to low then pulled back to high during the write cycle. The host processor provides information while the display module captures the information from the host processor on the rising edge of the WRX. Figure 1 below shows the write cycle of the DBI Type B interface.

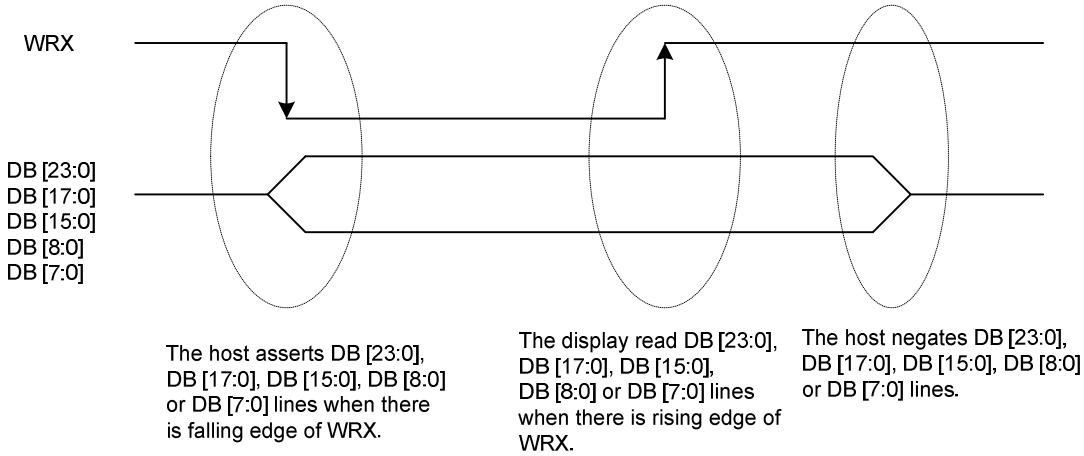

Figure 1: DBI Type B Write Cycle

Note: WRX is an unsynchronized signal that can be terminated when not being used.

When the D/CX signal is driven to low level, the input data on the interface is interpreted as command information. The D/CX signal can also be pulled to high level when the data is RAM data or command parameter.

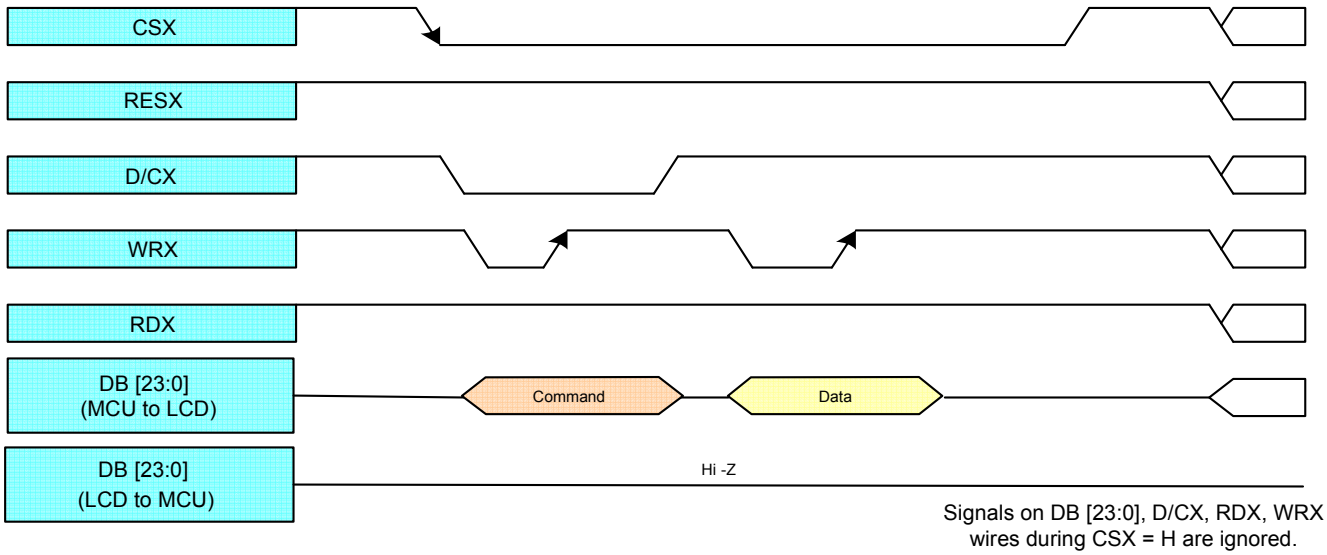

Figure 2: DBI Type B Write Cycle Sequence

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4.1.2. Read Cycle Sequence

The RDX signal is driven from high to low and then pulled back to high during the read cycle. The display module provides information to the host processor while the host processor reads the display module information on the rising edge of the RDX signal. Figure 3 below shows the read cycle of the DBI Type B interface.

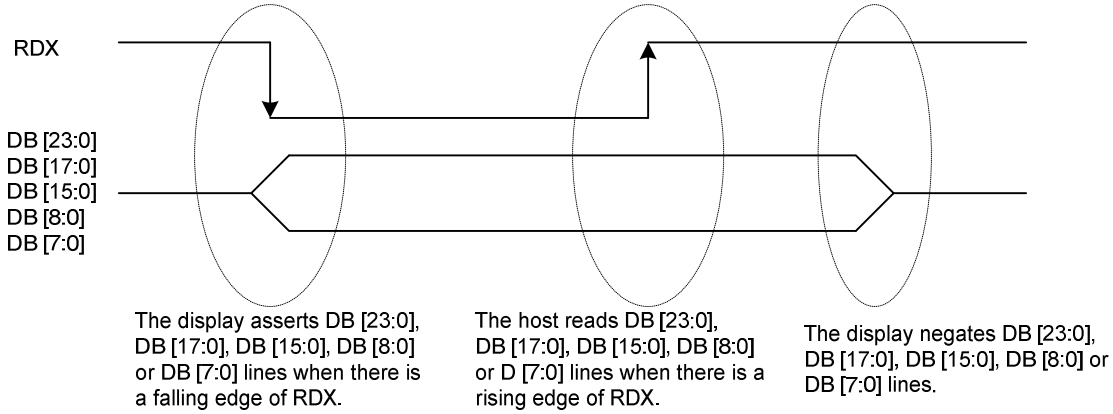

Figure 3: DBI Type B Read Cycle

Note: RDX is an unsynchronized signal that can be terminated when not being used.

When the D/CX signal is driven to the low level, the input data on the interface is interpreted as internal status or parameter data. The D/CX signal can also be pulled to a high level when the data on the interface is RAM data or a command parameter data.

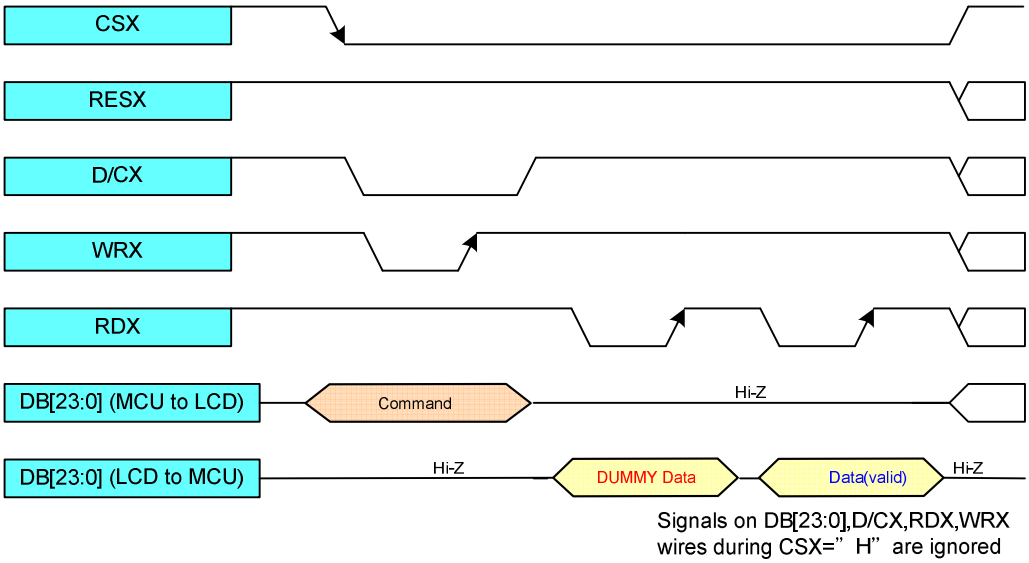

Figure 4: DBI Type B Read Cycle Sequence

Note: Read Data is only valid when the D/CX input is pulled high. If the D/CX signal is driven to low during the read cycle then the display information outputs will be High-Z.

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4.2. DBI Type C Serial Interface

The selection of this interface is done by the IM [2:0] pins, as shown in the table below.

Table 5: DBI Type C Serial Interface

IM2	IM1	IM0	DBI Type C	D/CX	CSX	SCL	Function
1	0	1	Option 1 (3-line SPI)	-	"L"	↑	Read/Write command, parameter or display data
1	1	1	Option 3 (4-line SPI)	"L"/"H"	"L"	↑	Read/Write command, parameter or display data

The ILI9488 uses 3-line 9-bit and 4-line 8-bit serial interfaces for communication between the host and the ILI9488. The 3-line serial interface consists of the chip enable input (CSX), the serial clock input (SCL), and serial data Input/Output (SDA). The 4-line serial interface consists of the Data/Command and selection input (D/CX), chip enable input (CSX), the serial clock input (SCL), and serial data Input/Output (SDA). If the data bus (DB [23:0]) is not used for the DPI interface data transfer, the unused pins will not be affected. The Serial clock (SCL) is used only for the interface with the MCU, so it can be stopped when no communication is necessary.

4.2.1. Write Cycle Sequence

In the write mode of the interface, the host writes commands and data to the ILI9488. The 3-line serial data packet contains a D/CX (data/command) select bit and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored in the GRAM as display data, or stored in the command register as parameter data.

Any instruction can be sent in any order to the ILI9488, and the MSB is transmitted first. The serial interface is initialized when the CSX is in high level. In this state, the SCL clock pulse and SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See detailed formats for 3-/4-line serial interface in the following two figures.

3-line Serial Interface Data Format

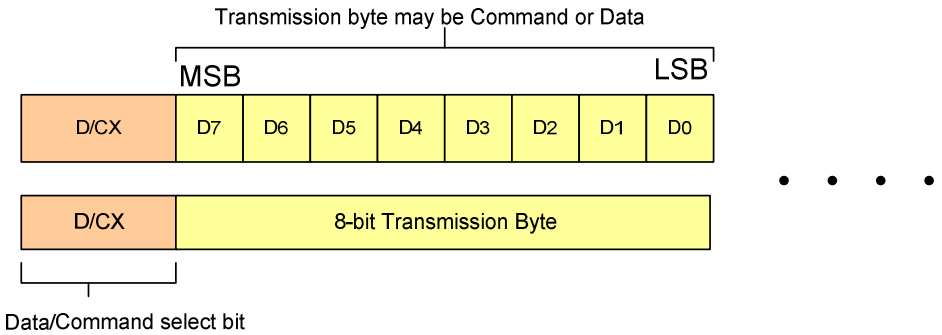

Figure 5: DBI Type C (Option 1) Data Format

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4-line Serial Interface Data Format

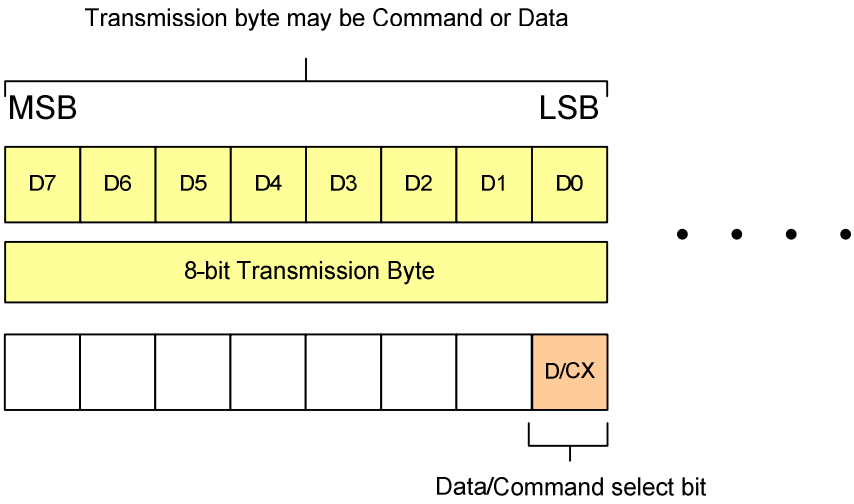

Figure 6: DBI Type C (Option 3) Data Format

The host drives the CSX pin to low and sets the D/CX bit on the SDA pin. The bit is read by the ILI9488 on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDA pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDA pin. If the optional D/CX signal is used, a byte is eight read cycles long. The 3-/4-line serial interface writing sequences are described in Figure 7 and Figure 8 below.

3-line Serial Interface Protocol

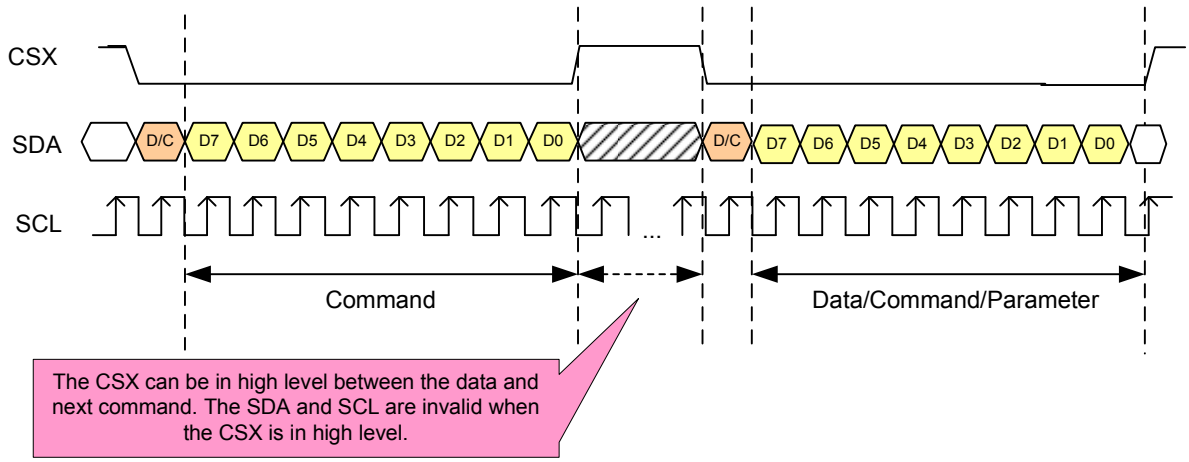

Figure 7: DBI Type C (Option 1) Protocol

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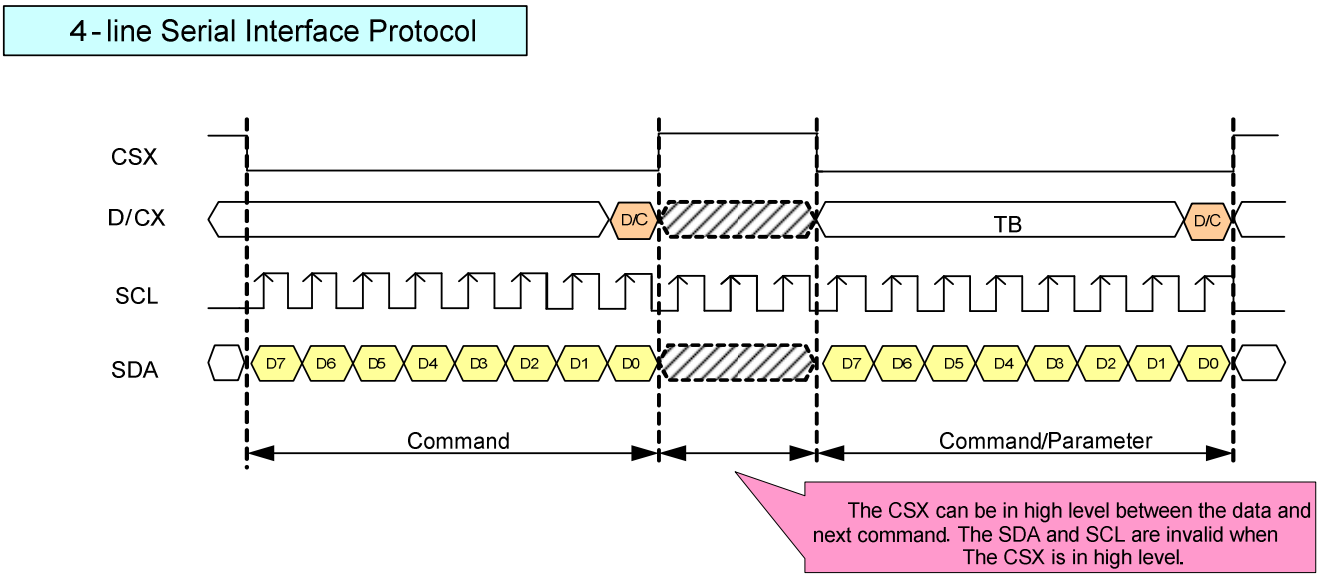

Figure 8: DBI Type C (Option 3) Protocol

4.2.2. Read Cycle Sequence

In the read mode of the interface, the host reads the register value from the ILI9488. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ILI9488 samples the SDA (input data) at the rising edges of the SCL (serial clock), and shifts to SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

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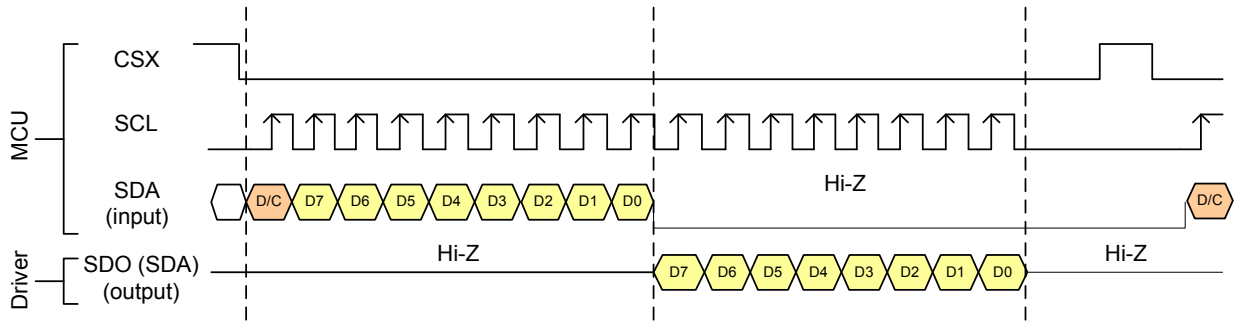
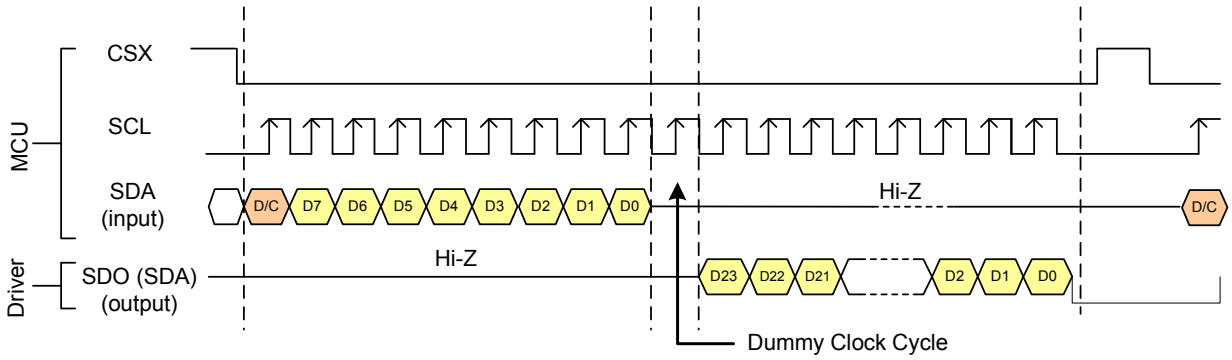
3-line Serial Protocol (for RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



3-line Serial Protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

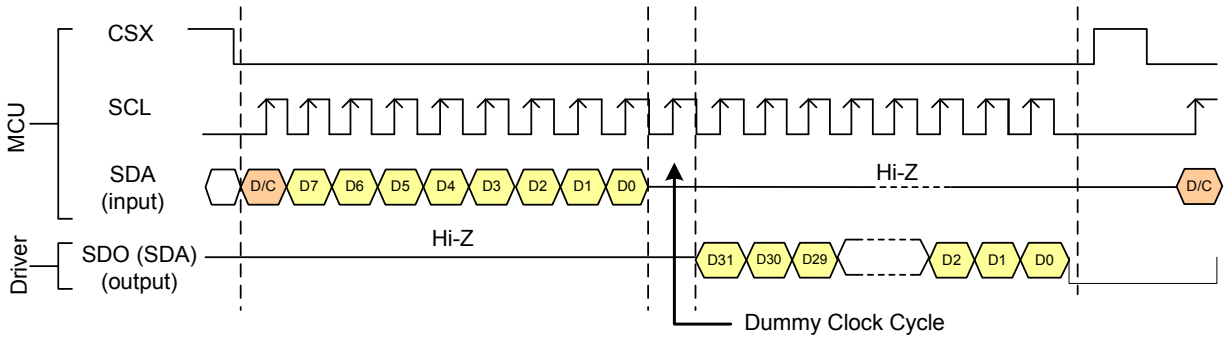


Figure 9: DBI Type C (Option 1) Read Cycle Sequence

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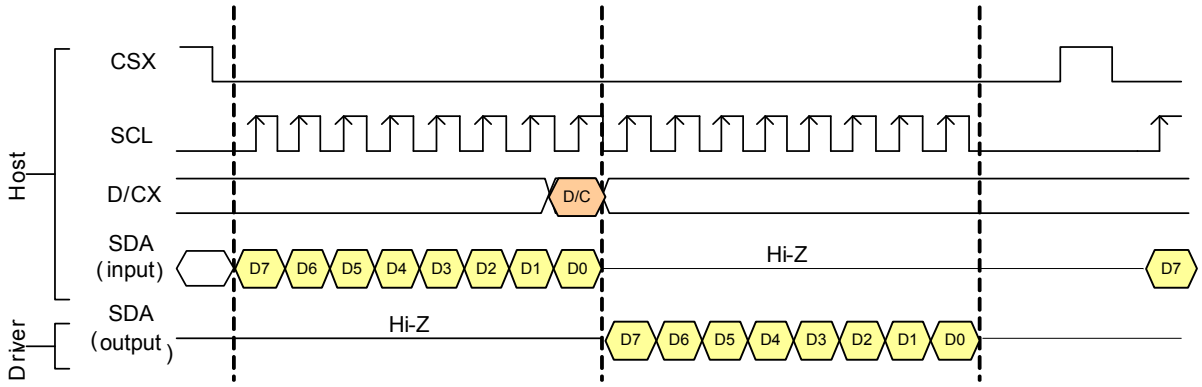
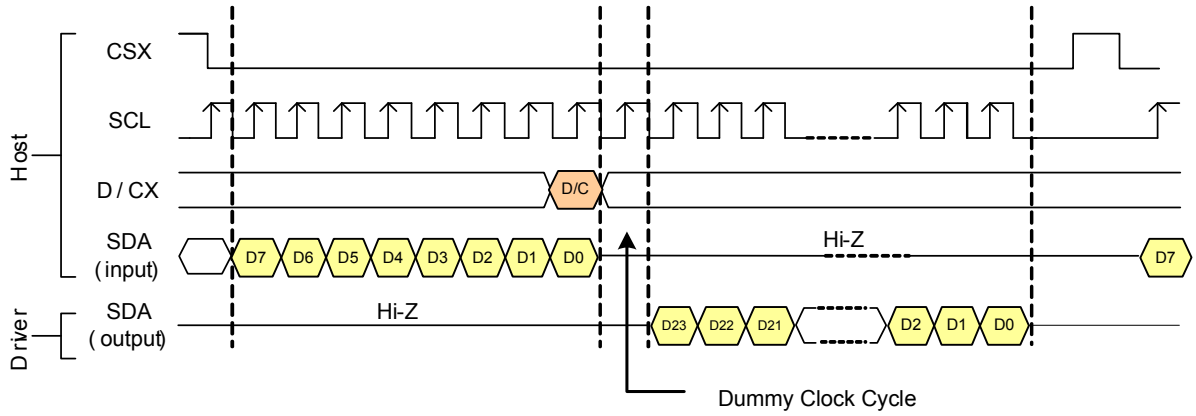
4-line Serial Protocol (for RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-line Serial Protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

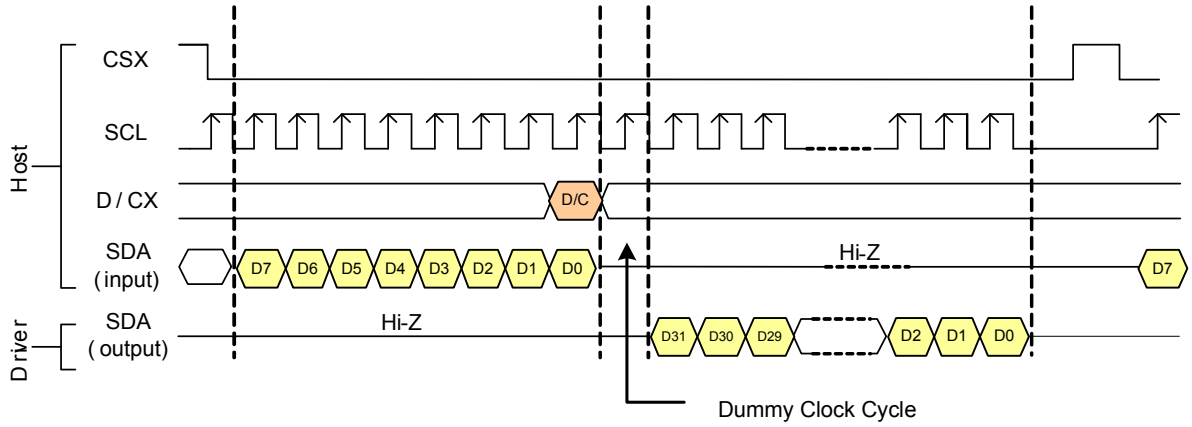


Figure 10: DBI Type C (Option 3) Read Cycle Sequence

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4.2.3. Data Transfer Break and Recovery

If data transmission is interrupted by the CSX pulse while transferring a Command, Frame Memory Data, or Multiple Parameter Command before Bit D0 of the byte is completed, then the driver will reject the previous bits and reset the interface so it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is activated again.

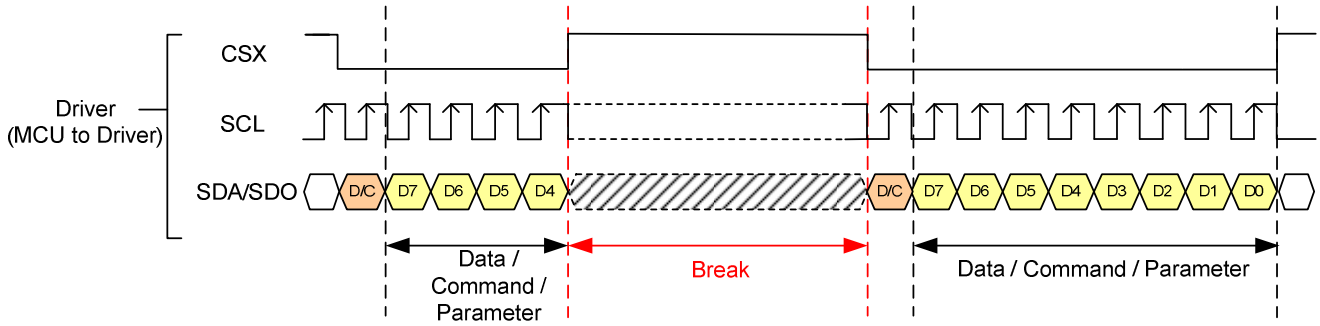

Figure 11: Data Transfer Break and Recovery

If there is a break when transmitting a command with multiple parameters, and the host initiates transfer of a new command, the parameters that were successfully transferred are stored and the incomplete parameter data where the break occurred is dropped. The interface is ready to receive the next byte as shown in the figure below.

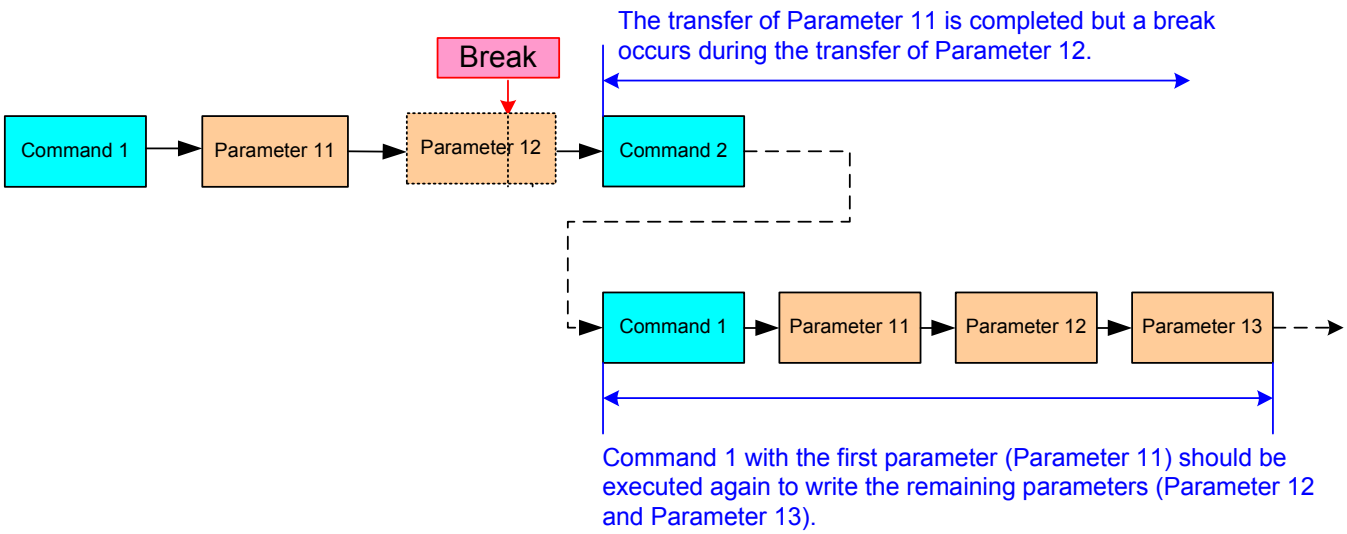

Figure 12: Data Transfer Break – Case 1

If a command with multiple parameters is sent and a break occurs by a new command before all the parameters are transferred, then the parameters that were successfully sent are stored and the remaining parameters of that command will remain at the previous value.

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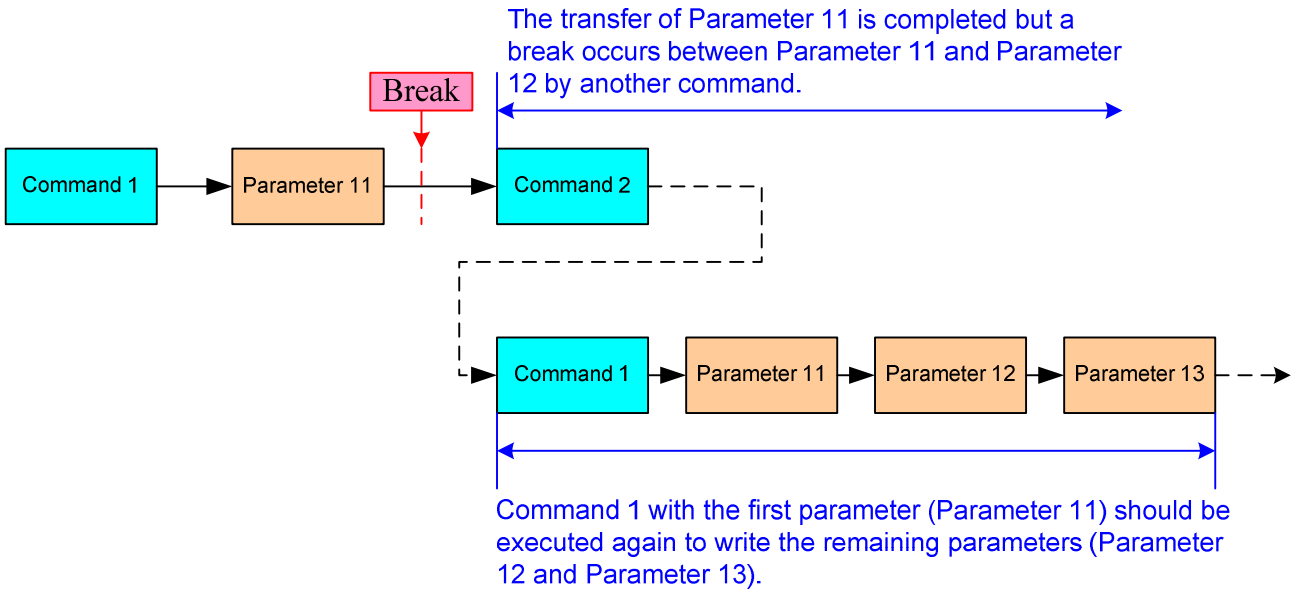

Figure 13: Data Transfer Break – Case 2

4.3. Data Transfer Pause

Transferring a Command, Frame Memory Data or Multiple Parameter Data might invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the ILI9488 will wait and continue the Frame Memory Data or Parameter Data transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completely transmitted, then the display module will receive either the command's parameters or a new command when the Chip Select Line is enabled again, as shown below.

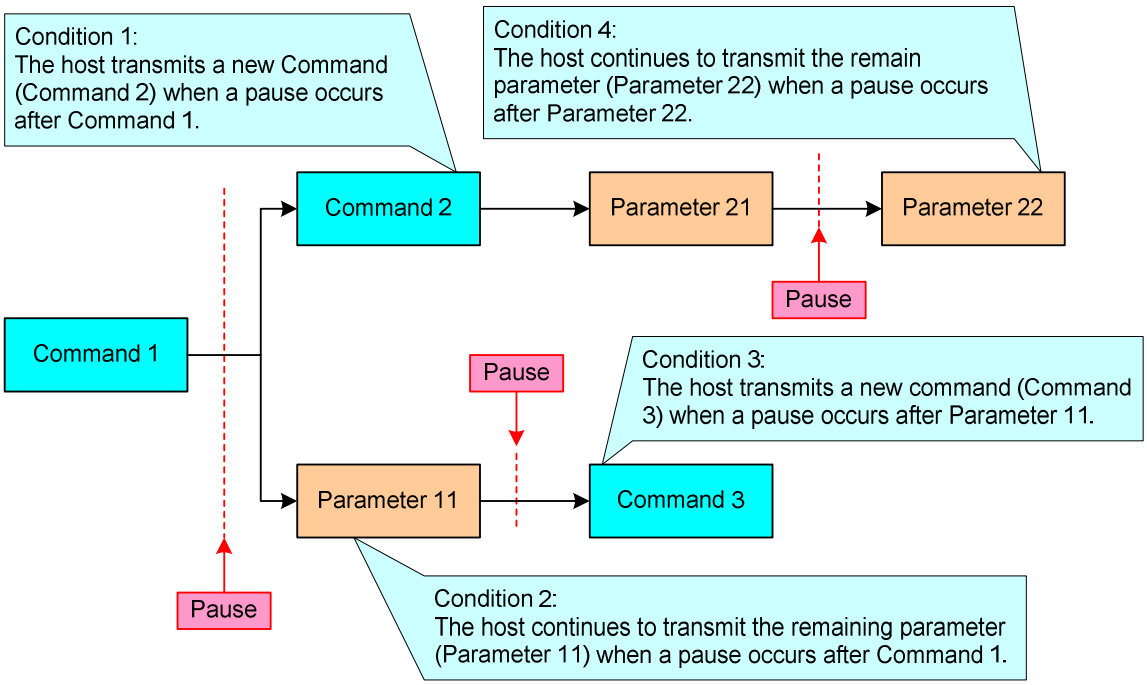

Figure 14: Data Transfer Pause

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4.3.1. Serial Interface Pause

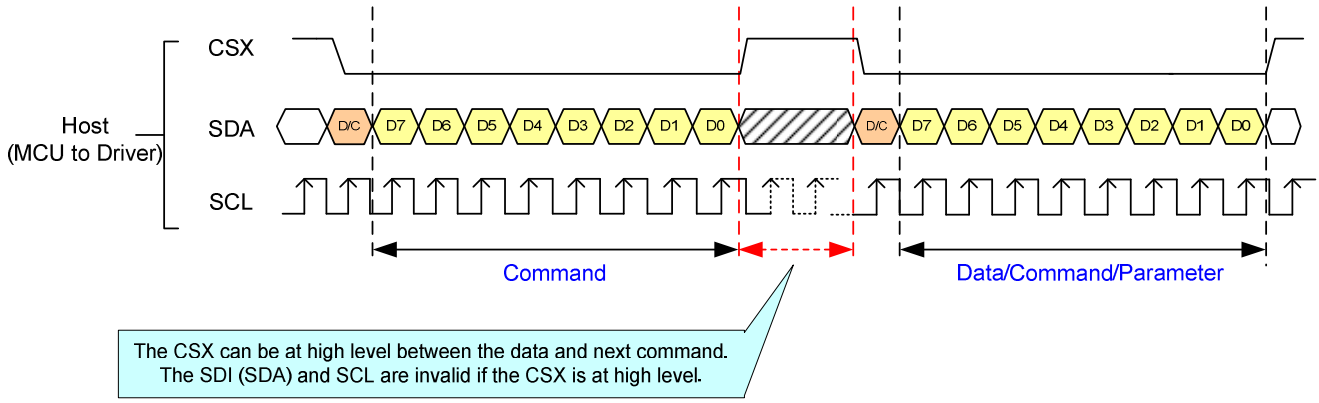

Figure 15: DBI Type C Data Transfer Pause

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

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4.3.2. Parallel Interface Pause

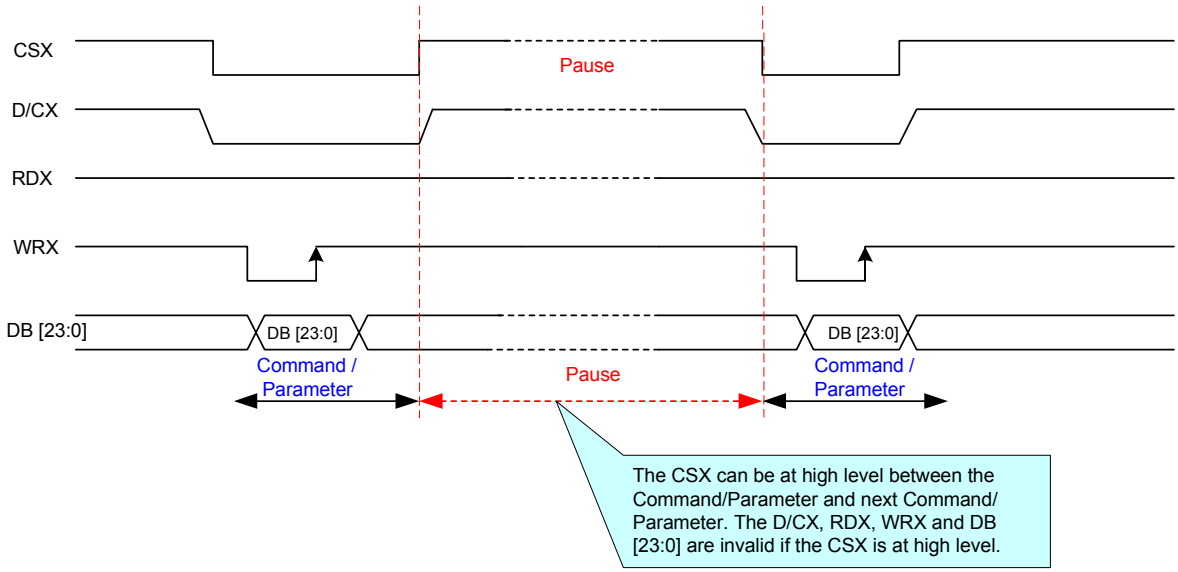

Figure 16: DBI Type B Data Transfer Pause

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

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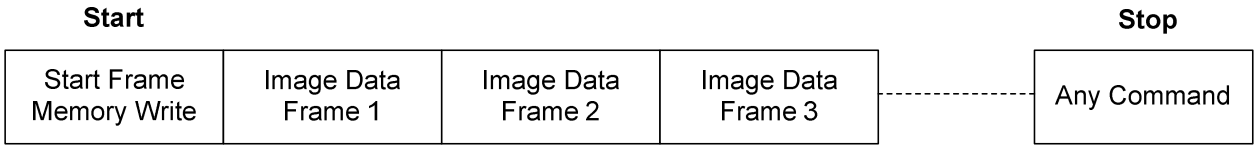
4.4. Data Transfer Mode

The ILI9488 can provide five different kinds of color depth (8-bit/pixel, 9-bit/pixel, 16-bit/pixel, 18-bit/pixel, and 24-bit/pixel) for display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

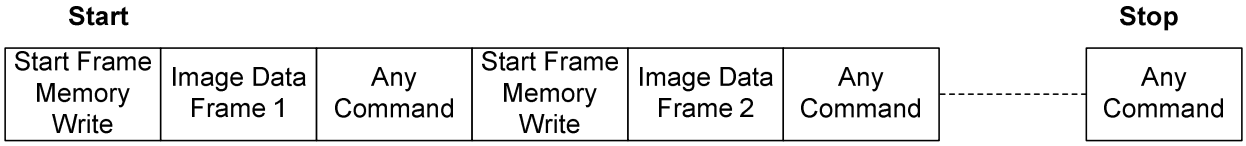
4.4.1. Method 1

The image data is sent to the Frame Memory in the successive Frame writing. Each time the Frame Memory is filled by image data, the Frame Memory pointer is reset to the start point and then the next Frame is written.



4.4.2. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is then sent to stop Frame Memory Writing. Then the Start Memory Write command is sent, and a new Frame is downloaded.



Notes:

1. These two methods can apply to all five kinds of color depth on both serial and parallel interfaces.
2. The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

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4.5. DPI Parallel Interface (RGB Interface)

The DPI can display moving pictures by two ways: rewrite into the GRAM and transmit directly to the shift register. The selection is set by the register BPGRAM (bypass GRAM) and RM bit. The RM bit selects an interface for the access operation of the Frame Memory. For the DPI, RM should be set as 1.

BPGRAM	Display Data Path
1	Direct to shift register
0	Write into Memory
RM	**Interface for RAM access**
0	System interface
1	RGB interface

The DM bit selects the clock operation mode. It allows switching between display operations in synchronization with the internal oscillation clock. If DM = 1, the external DOTCLK cannot be stopped unless it enters the Sleep-In mode.

DM	RGB Interface Operating Clock Selection
0	Internal system clock
1	RGB interface (DOTCLK)

4.5.1. RGB Interface Selection

The DPI can be selected by the RCM bit. When the RCM is set to 0, the DE mode is selected by VSYNC, HSYNC, DOTCLK, ENABLE, and DB [23:0] pins. When RCM is set to 1, the SYNC mode is selected by VSYNC, HSYNC, DOTCLK, and DB [23:0] pins. It supports several pixel formats that can be selected by DPI [2:0] bits in Pixel Format Set (R3Ah) command. The selection of a given interface is done by DPI [2:0], as shown in Table 6 and Figure 17.

Table 6: DPI Interface Selection

RCM	DPI [2:0]			RGB Interface Mode	RGB Mode	Used Pins
0	1	1	1	24-bit RGB interface (16.7M colors)	**DE Mode** Valid data is determined by the ENABLE signal.	VSYNC, HSYNC, ENABLE, DOTCLK, DB [23:0]
0	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, ENABLE, DOTCLK, DB [17:0]
0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, ENABLE, DOTCLK, DB [15:0]
1	1	1	1	24-bit RGB interface (16.7M colors)	**SYNC Mode** In the SYNC mode, ENABLE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, DB [23:0]
1	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, DB [17:0]
1	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB [15:0]

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24-bit DPI interface connection (DB [23:0] is used): set pixel format DPI [2:0] = 3'h7

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R[7]	R[6]	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit DPI interface connection (DB [15:0] is used): set pixel format DPI [2:0] = 3'h5

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 17: DPI Interface 24/18/16 Pixel Format Selection

The Pixel clock (DOTCLK) runs all the time without stop. It is used to enter VSYNC, HSYNC, ENABLE and DB [23:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as the internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Data Enable (ENABLE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DOTCLK signal. DB [23:0] is used to indicate what is the information of the image that is transferred on the display (when ENABLE = 0 (low) and there is a rising edge of DOTCLK). DB [23:0] can be 0 (low) or 1 (high). These lines are read by a rising edge of the DOTCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

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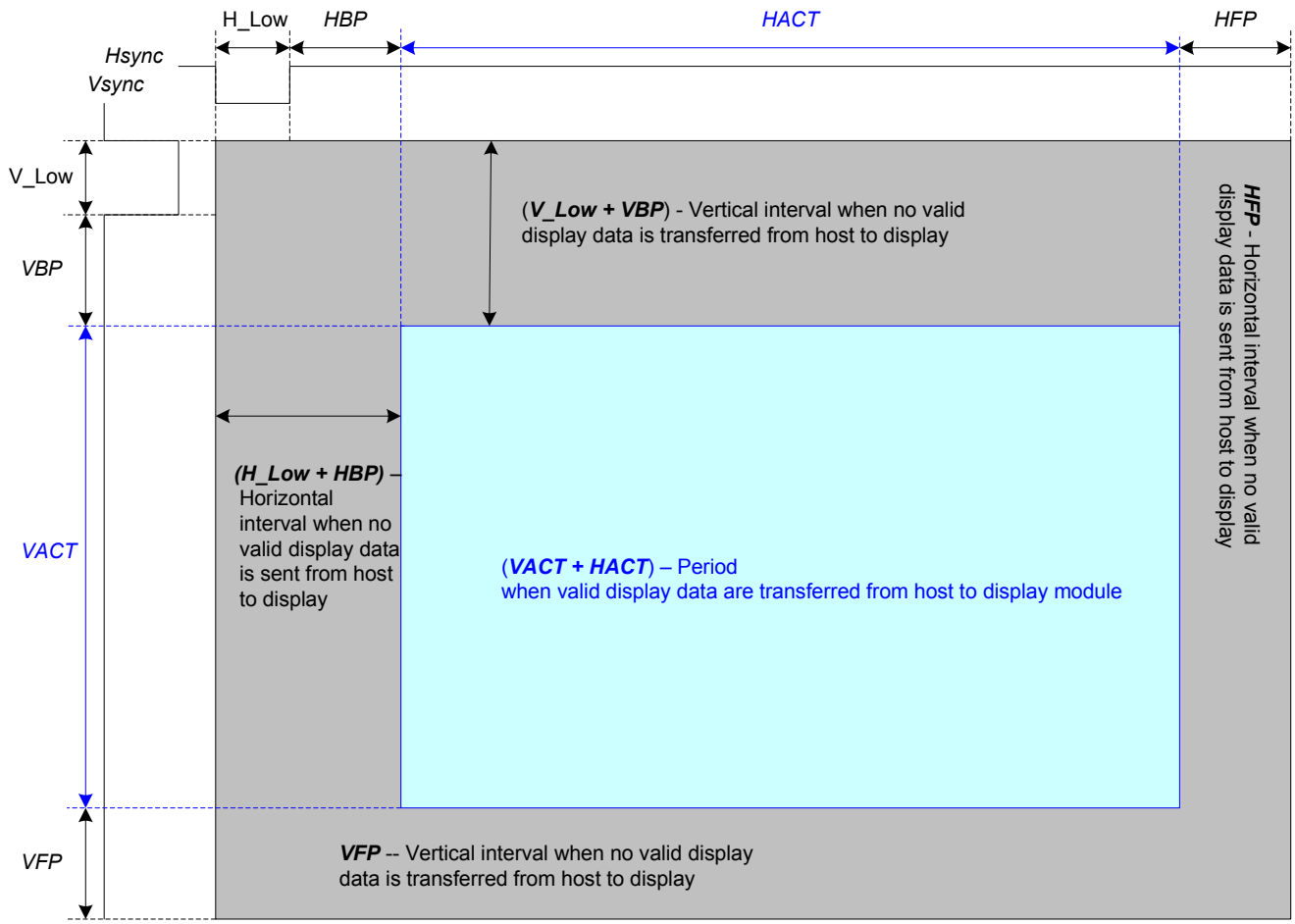
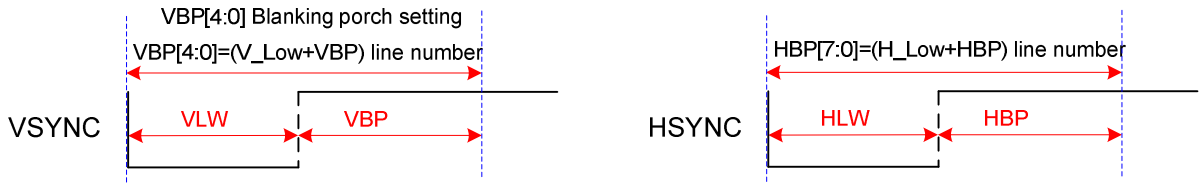


Figure 18: General DPI Timing Diagram

Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low+HBP <192	DOTCLK
Horizontal Back Porch	HBP	3	-		DOTCLK
Horizontal Front Porch	HFP	3	-	255	DOTCLK
Horizontal Address	HACT	-	320	-	DOTCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low+VBP+VFP < 32	Line
Vertical Back Porch	VBP	2	-		Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DOTCLK cycle		100	-	50	ns
DOTCLK Frequency		10	-	20	MHz

Example：DOTCLK = 20Mhz, TE=70Hz, V_Low+VBP=2, VFP=2, H_Low+HBP=100, HFP=170.

Note: VBP[4:0]/HBP[7:0] (Blanking Porch Control, RB5h) define as follows:



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4.5.2. RGB Interface Timing

The timing chart of 16-/18-/24-bit DPI interface mode is illustrated in Figure 19.

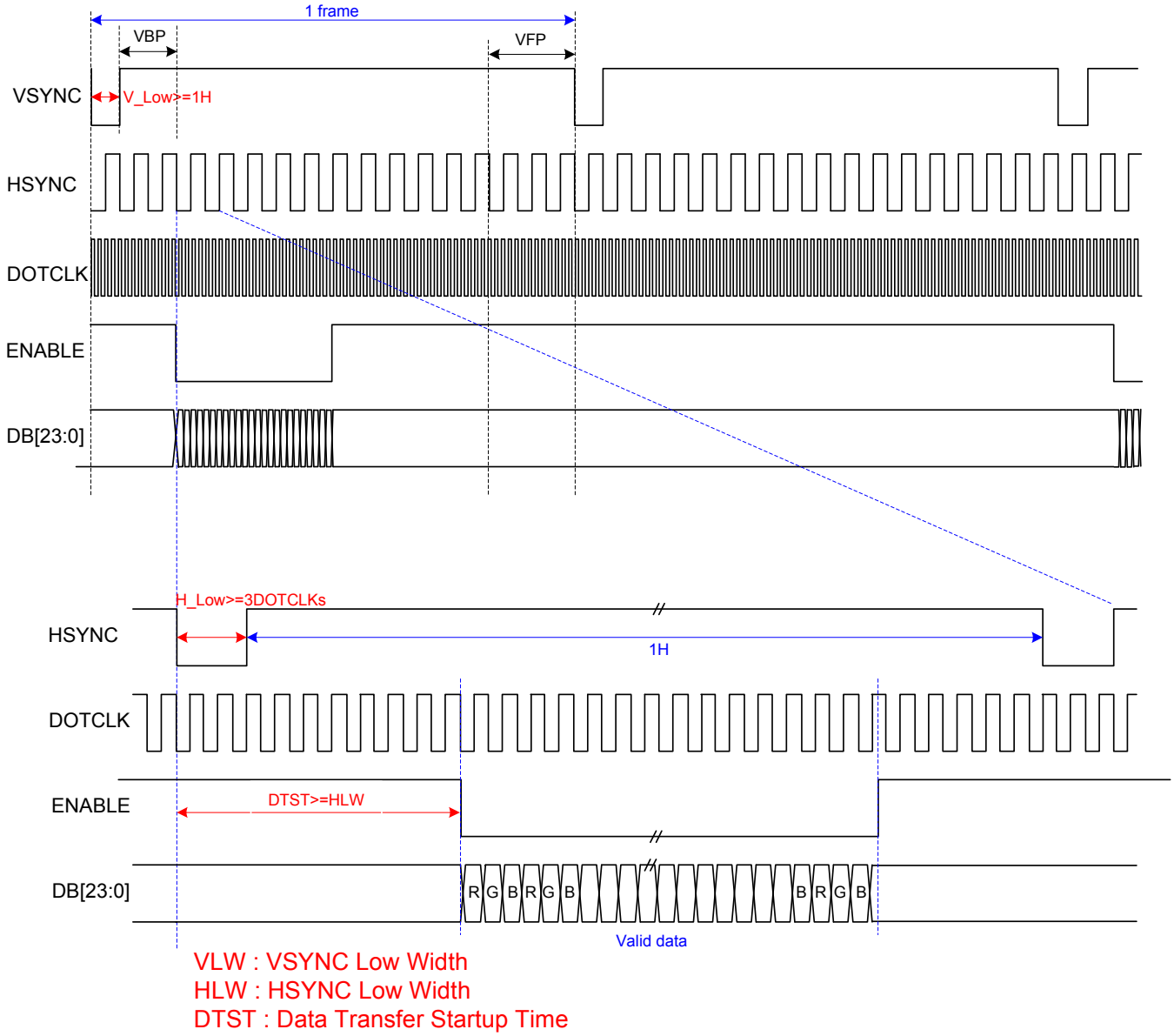

Figure 19: DPI Interface Timing Diagram

Note: VSPL = 0, HSPL = 0, DPL = 0 and EPL = 0 of Interface Mode Control B0h command.

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4.6. DSI System Interface

4.6.1. General Description

The MIPI-DSI is enabled or disabled by the external IM [2:0] pin.

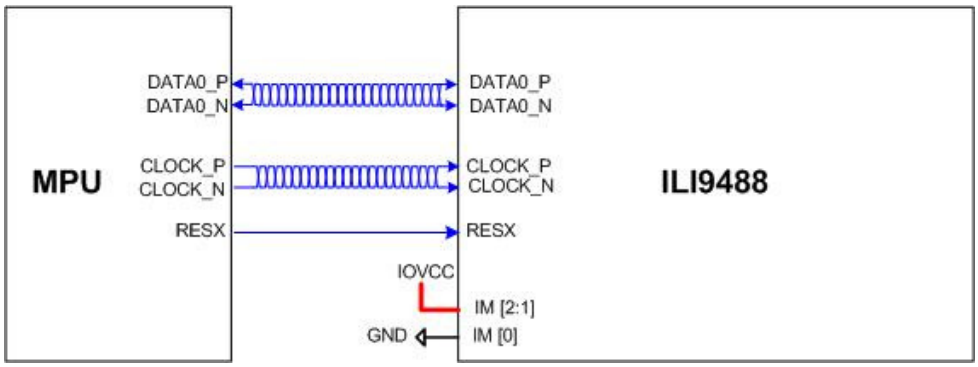

Figure 20: DSI System Interface Diagram

The communication is separated into two different levels between the MCU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

4.6.2. Interface Level Communication

4.6.2.1. General

The display module uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode. Low Power mode means that each line of the differential pair is used in the single ended mode, and a differential receiver is disable (the termination resistor of the receiver is disable), and it can be driven into a low power mode. High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode. Different modes and protocols are used in each mode when information is to be transferred from the MCU to the display module and vice versa. The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 7: High Speed and Low Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

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2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair will return to LP-11 of the Control Mode.

4.6.2.2. MIPI_CLOCK Lanes

MIPI_CLOCK_P/N lanes can be driven into three different power modes:

- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)
- High Speed Clock Mode (HSCM)

Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the High Speed Clock Mode (HSCM). These entering and leaving protocols use clock lanes in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different clock lanes power modes is illustrated below.

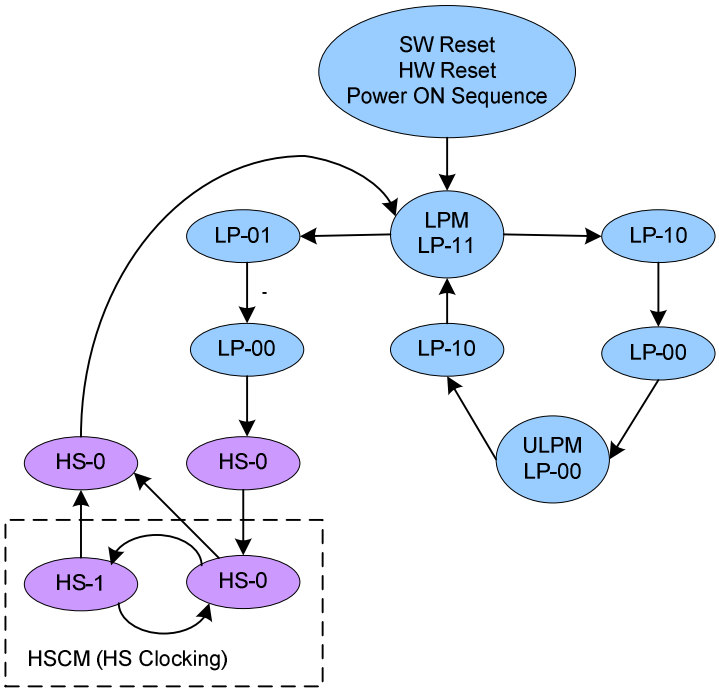

Figure 21: Clock Lanes Power Mode

4.6.2.2.1. Low Power Mode (LPM)

MIPI_CLOCK_P/N lanes can be driven to the Low Power Mode (LPM), when MIPI_CLOCK lanes enter the LP-11 State Code, in three different ways:

(1) After SW Reset, HW Reset or Power On Sequence => LP-11

(2) After MIPI_CLOCK_P/N lanes leave the Ultra Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11

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(LPM).

This sequence is illustrated below.

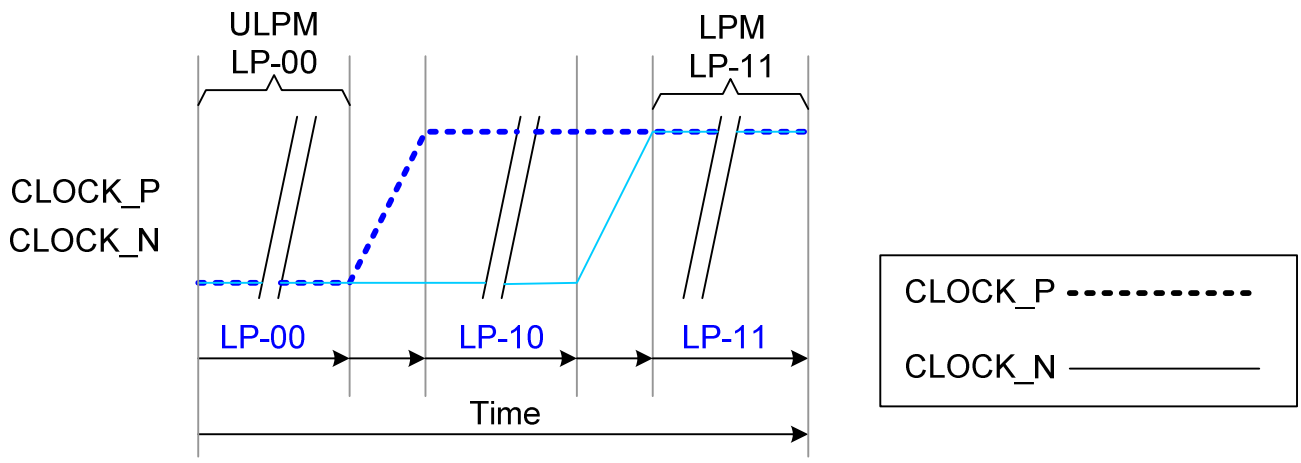

Figure 22: From ULPM to LPM

(3) After MIPI_CLOCK_P/N lanes leave the High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0 => LP-11 (LPM).

This sequence is illustrated below.

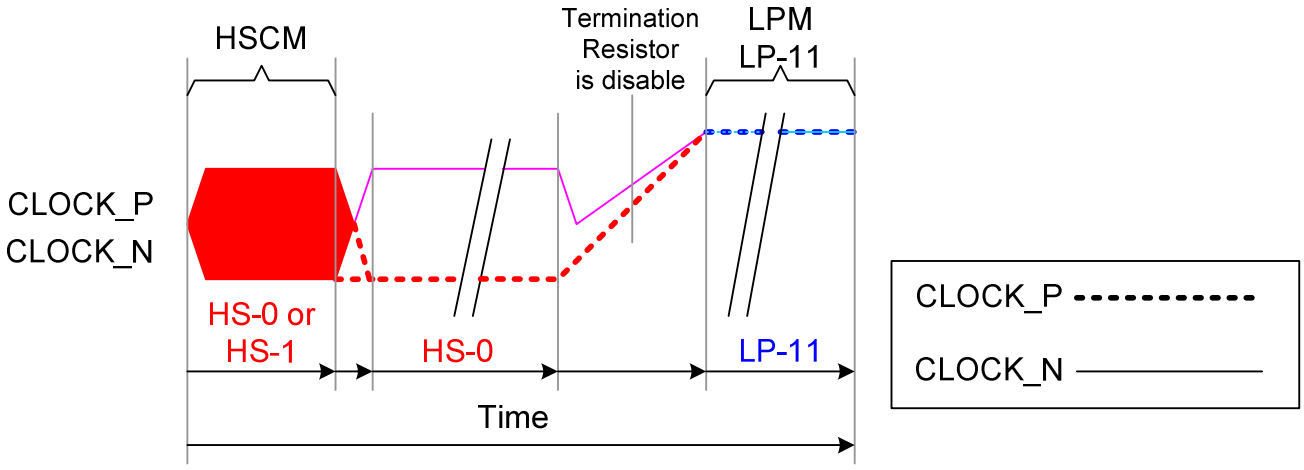

Figure 23: From High Speed Clock Mode (HSCM) to LPM

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All changes of the three modes are illustrated in the flow chart below.

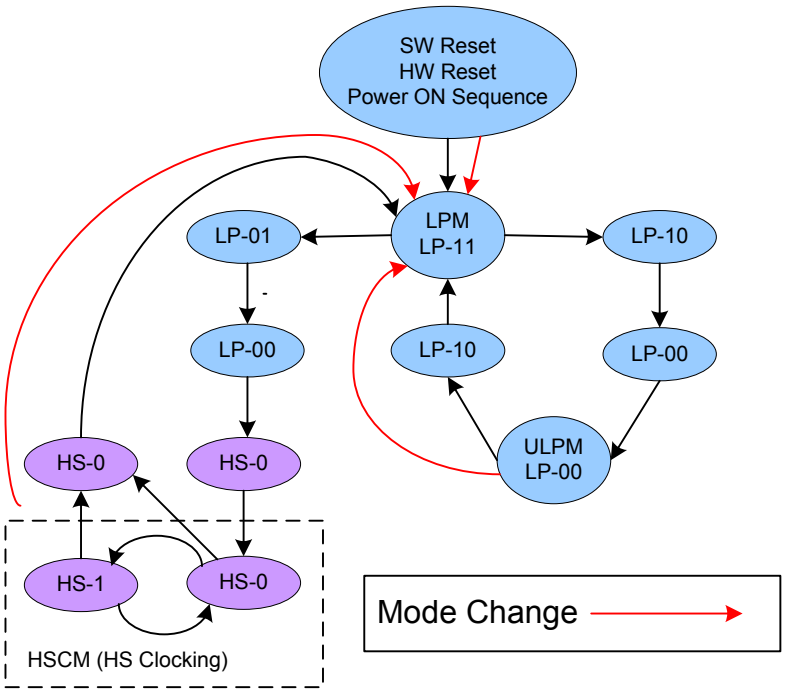

Figure 24: All Changes of the Three Modes to LPM

4.6.2.2.2. Ultra Low Power Mode (ULPM)

MIPI_CLOCK_P/N lanes can be driven to the Ultra Low Power Mode (ULPM) when MIPI_CLOCK lanes enter the LP-00 State Code. The only possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below.

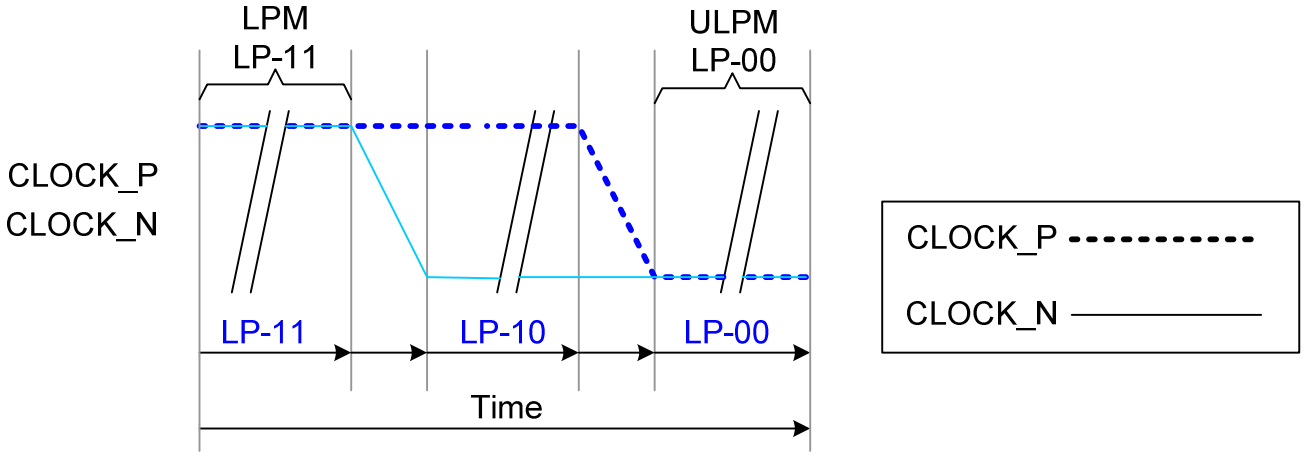

Figure 25: From LPM to ULPM

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The mode change is also illustrated below.

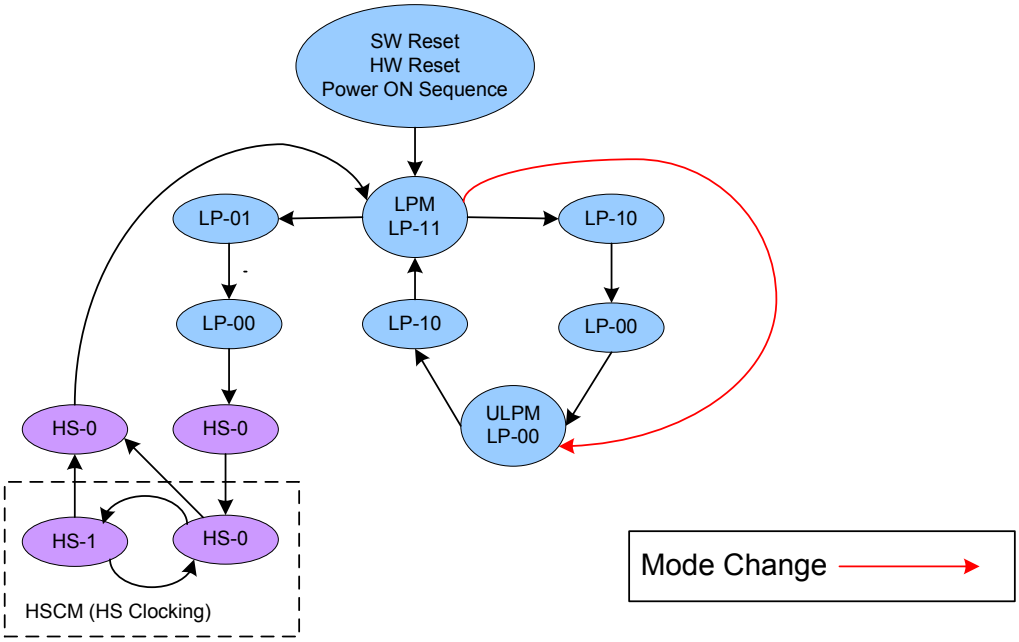

Figure 26: Mode Change from LPM to ULPM

4.6.2.2.3. High-Speed Clock Mode (HSCM)

MIPI_CLOCK_P/N lanes can be driven to the High Speed Clock Mode (HSCM), when MIPI_CLOCK lanes start to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

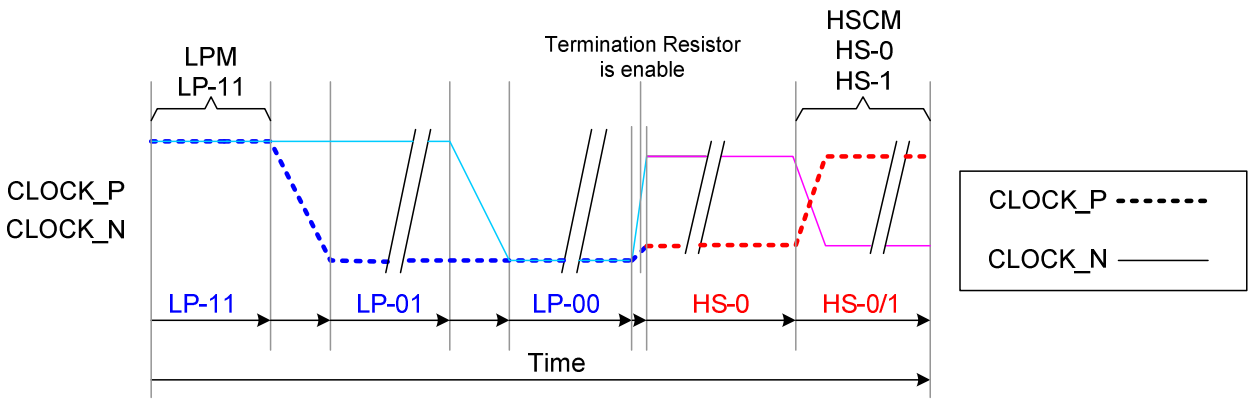

Figure 27: From LPM to HSCM

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The mode change is also illustrated below.

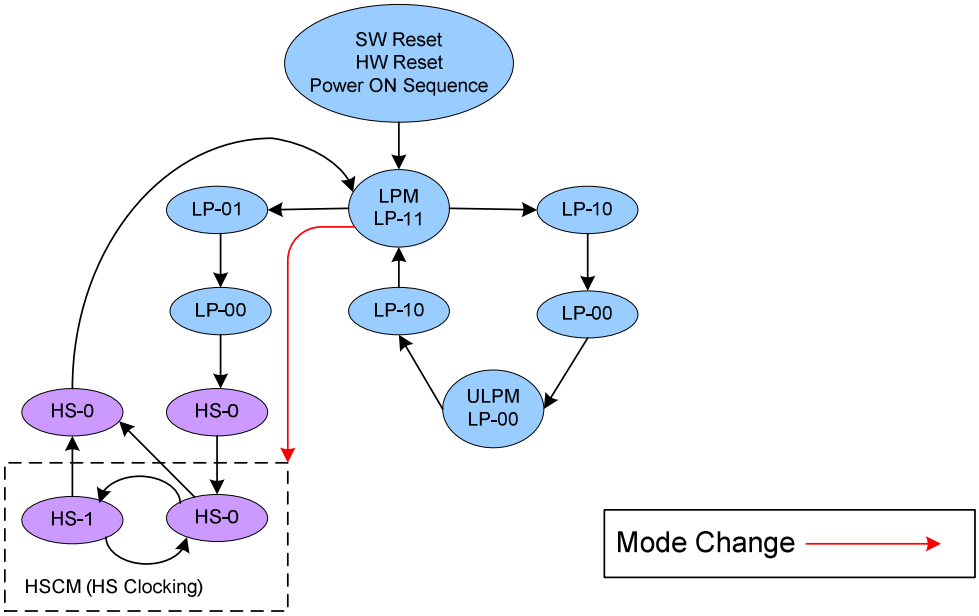

Figure 28: Mode Change from LPM to HSCM

The high speed clock (MIPI_CLOCK_P/N) starts before high speed data is sent via MIPI_DATA_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped. The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

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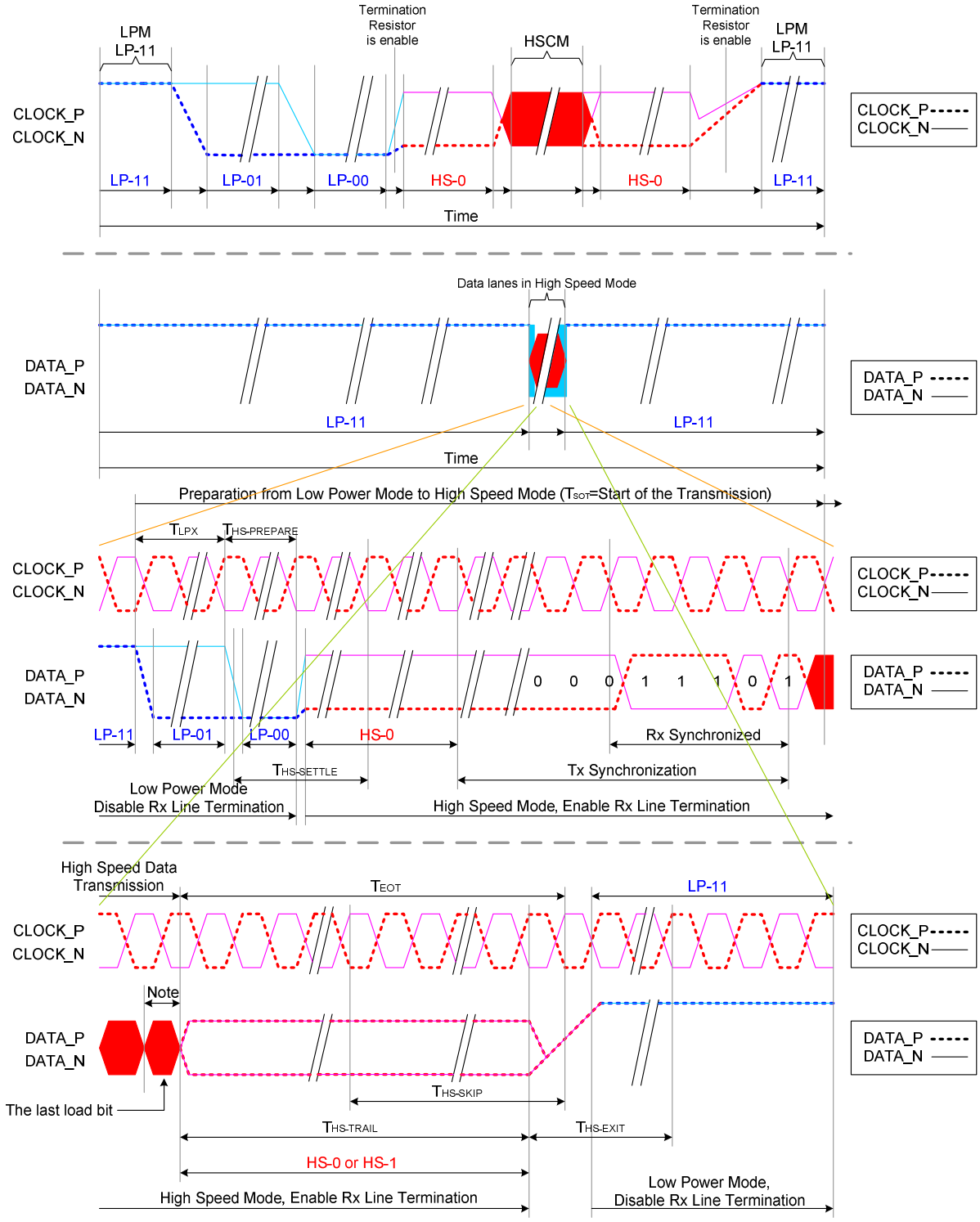

Figure 29: High Speed Clock Burst

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

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4.6.2.3. MIPI_DATA Lanes

4.6.2.3.1. General

MIPI_DATA_P/N Data Lanes can be driven in different modes:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined in the following table.

Table 8: Entering and Leaving Sequence

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 ➔ LP-10 ➔ LP-00 ➔ LP-01 ➔ LP-00	LP-00 ➔ LP-10 ➔ LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 ➔ LP-01 ➔ LP-00 ➔ HS-0	(HS-0 or HS-1) ➔ LP-11
Bus Turnaround Request	LP-11 ➔ LP-10 ➔ LP-00 ➔ LP-10 ➔ LP-00	Hi-Z

4.6.2.3.2. Escape Modes

Data lanes (MIPI_DATA_P/N) can be used in different Escape Modes when data lanes are in the Low Power (LP) mode.

These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which can reset the display module,
- Indicate “Tearing Effect” (TEE), which is used to transmit a TE line event from the display module to the MCU,
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded when one of the data lanes changes from low-to-high-to-low, then this changed data lane presents the value of the current data bit (MIPI_DATA_P = 1, MIPI_DATA_N = 0). For example, when MIPI_DATA_N changes from low-to-high-to-low, the receiver latches a data bit, which value is the logical 0. The receiver uses this low-to-high-to-low transition for its internal clock.
- A load if necessary
- Exit Escape (Mark-1): LP-00 => LP-10 => LP-11
- End: LP-11

This basic construction is illustrated below:

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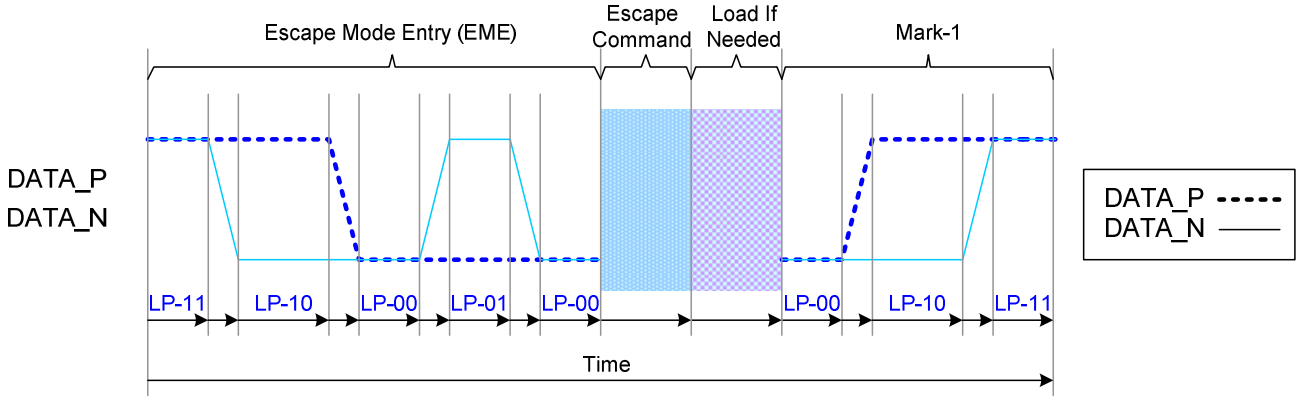

Figure 30: General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as described in Table 9.

An example of Mode Type Escape Commands is Ultra-Low Power Mode, by which the MCU instructs the display module how to enter its Ultra-Low Power Mode.

An example of Trigger type Escape Commands is Tearing Effect. In this case, the MCU has already instructed the display module to provide the TE trigger and is waiting for a response. The display module will then send a TE Trigger (TEE) on the next V-sync event.

Table 9: Escape Commands

Escape command	Command Type Mode/Trigger	Entry command Pattern (First ➔ Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001 b
Ultra-Low Power Mode	Mode	0001 1110 b
Undefined-1 Note	Mode	1001 1111 b
Undefined-2 Note	Mode	1101 1110 b
Remote Application Reset	Trigger	0110 0010 b
Tearing Effect	Trigger	0101 1101 b
Acknowledge	Trigger	0010 0001 b
Unknown-5 Note	Trigger	1010 0000 b

Note: This Escape Command is not implemented in the display module.

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4.6.2.3.2.1 Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and the Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module uses the same sequence as which it sends data to the MCU.

The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
  - One or more bytes (one byte = 8 bit)
  - Data lanes are in the pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

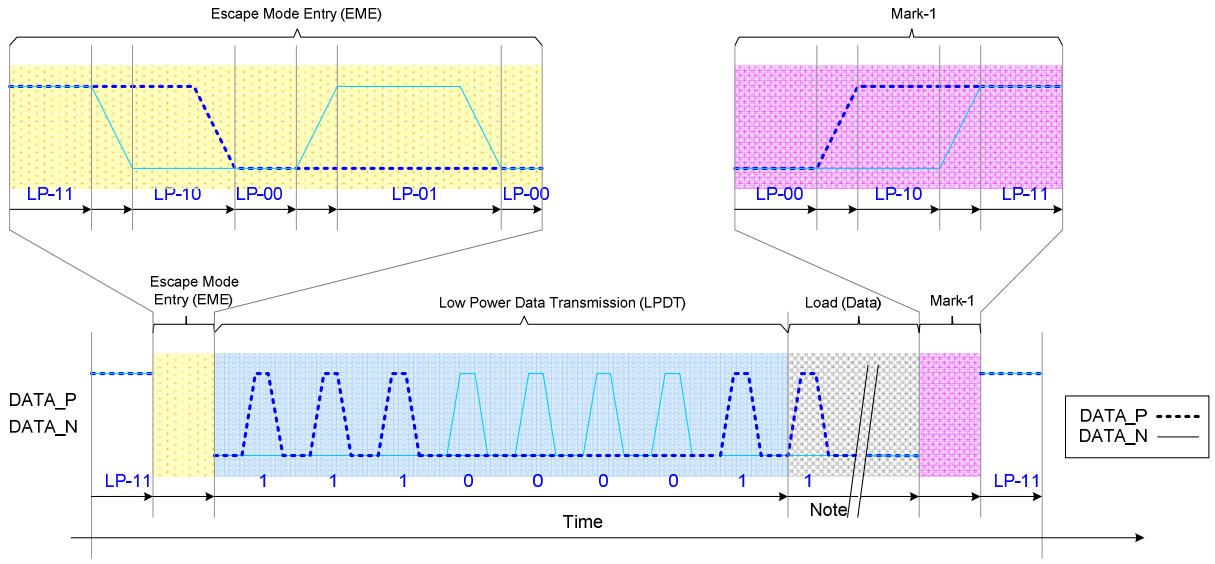

Figure 31: Low-Power Data Transmission (LPDT)

Note: Load (Data) presents that the first bit is the logical 1 in this example.

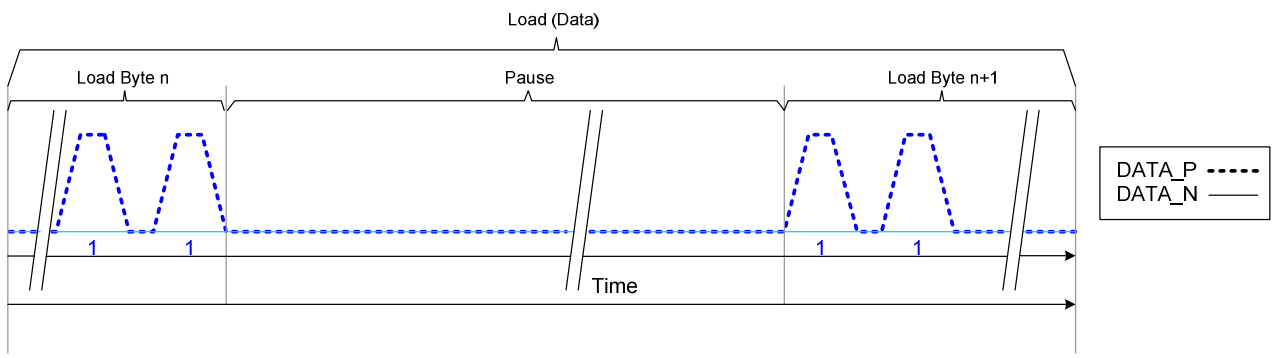

Figure 32: Pause (Example)

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4.6.2.3.2.2 Ultra-Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode.

The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

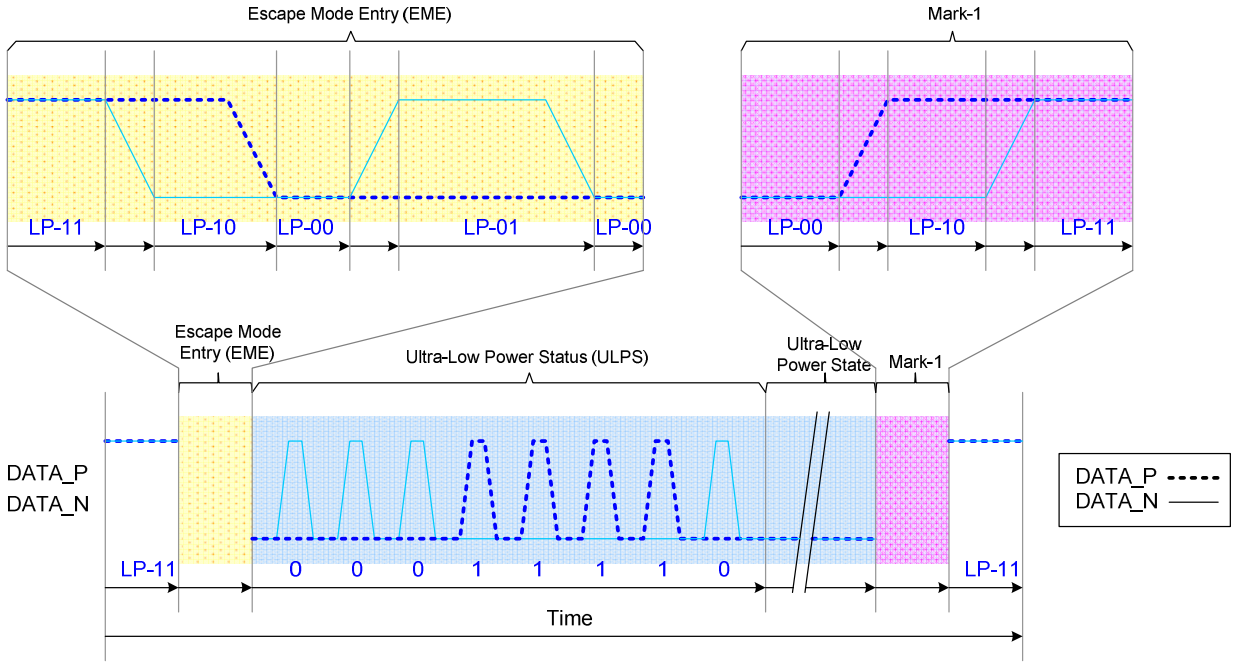

Figure 33: Ultra-Low Power State (ULPS)

4.6.2.3.2.3 Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode.

The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

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This sequence is illustrated below for reference purpose:

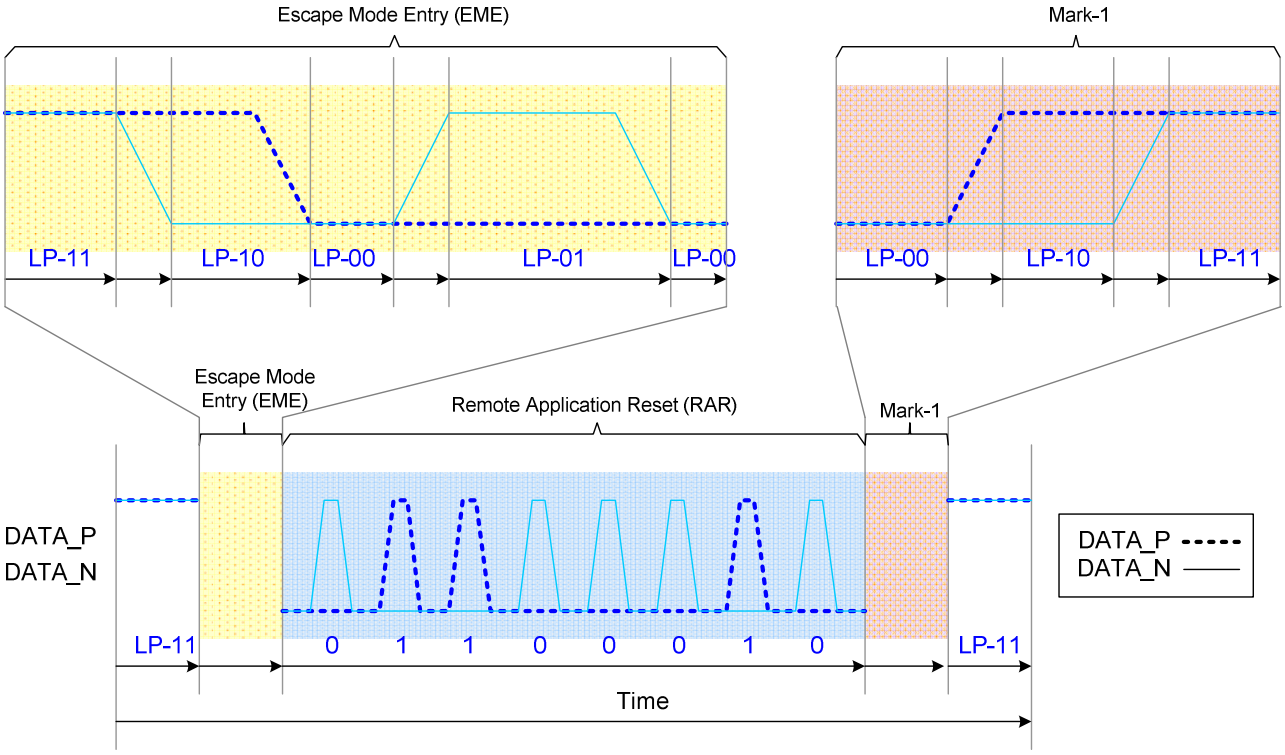

Figure 34: Remote Application Reset (RAR)

4.6.2.3.2.4 Tearing Effect (TEE)

The display module can inform the MCU by Tearing Effect (TEE) when a tearing affect event (New V-synch) has happened on the display module.

The display module sends the Tearing Effect (TEE) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Tearing Effect (TEE) trigger in the Escape Mode: 0101 1101 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

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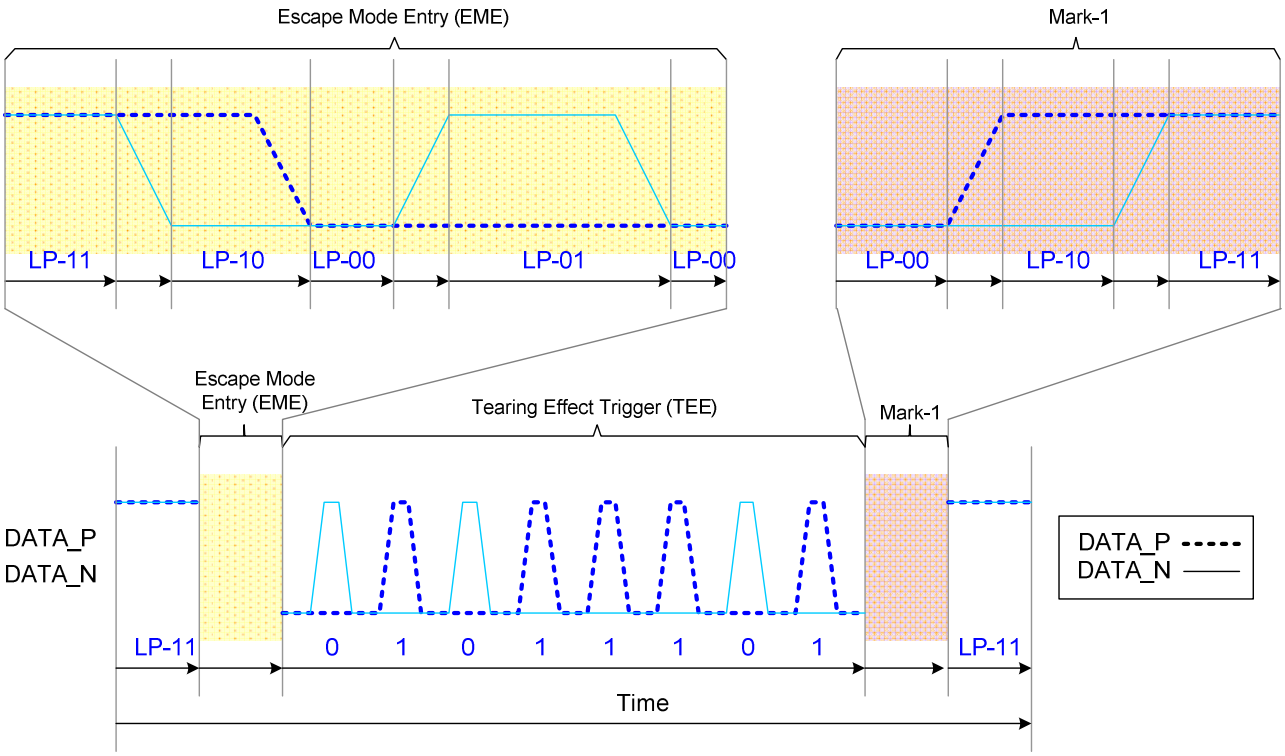

Figure 35: Tearing Effect (TEE)

4.6.2.3.2.5 Acknowledge (ACK)

The ILI9488 can inform the MCU that no errors are found by the Acknowledge (ACK).

The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

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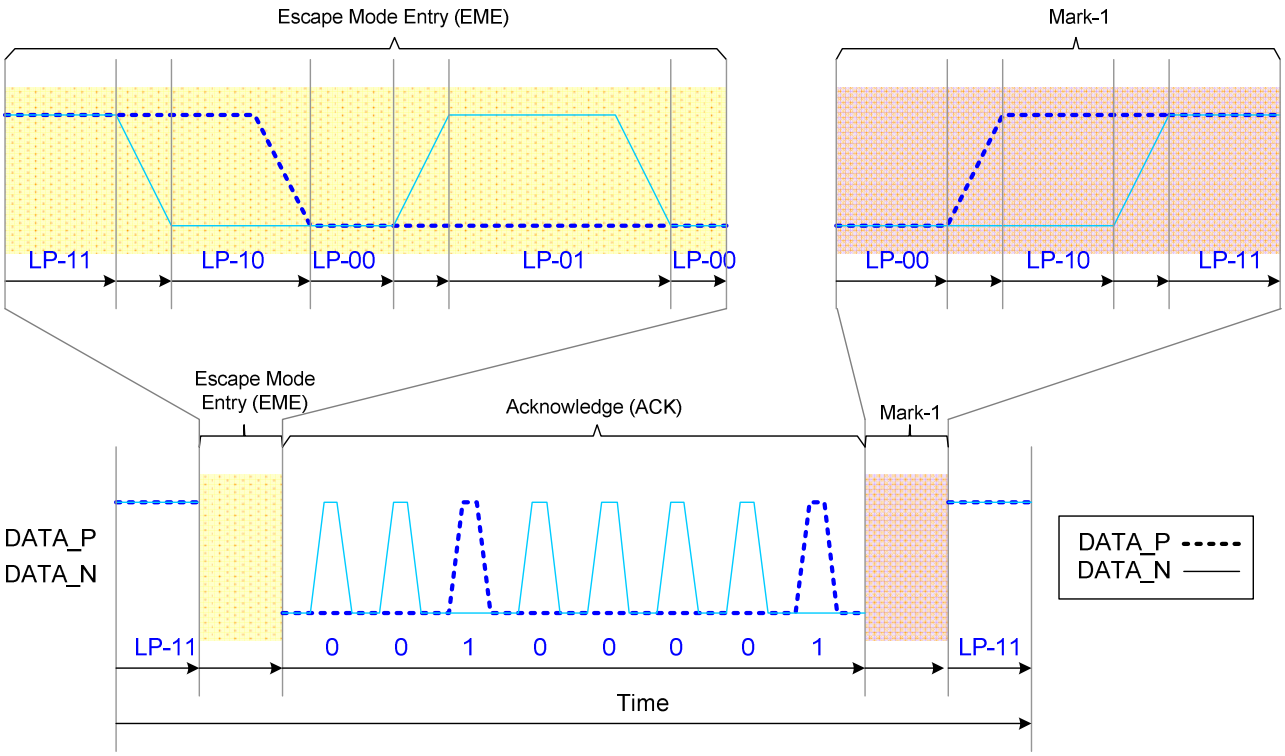

Figure 36: Acknowledge (ACK)

4.6.2.3.3. High-Speed Data Transmission (HSDT)

4.6.2.3.3.1 Enter High-Speed Data Transmission (T_{SOT} of HSDT)

The display module will enter High-Speed Data Transmission (HSDT) when Clock lanes MIPI_CLOCK_P/N have already entered the High-Speed Clock Mode (HSCM) through the MCU.

Data lanes MIPI_DATA_P/N of the display module enter (T_{SOT}) in the High-Speed Data Transmission (HSDT) with the following sequence:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The entering sequence of High-Speed Data Transmission (T_{SOT} of HSDT) is illustrated below:

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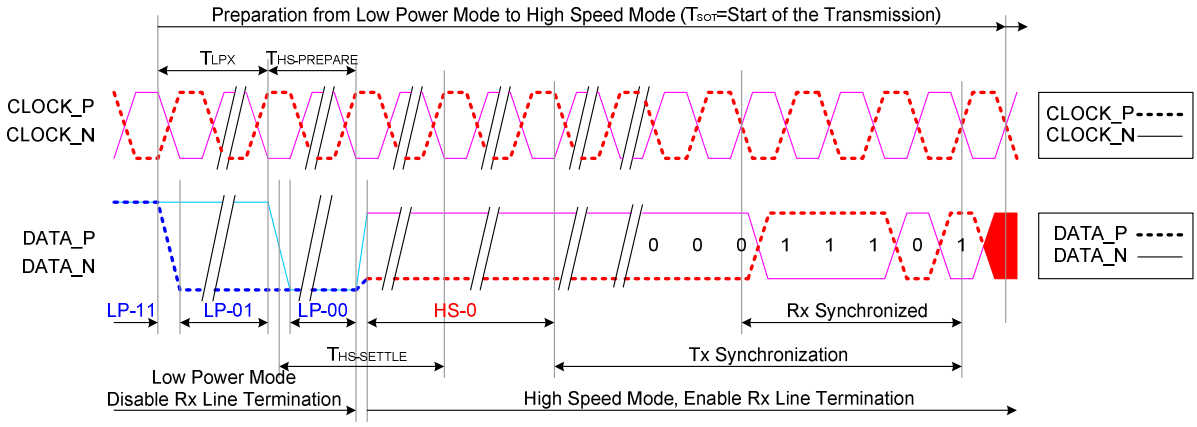

Figure 37: Entering High-Speed Data Transmission (T_{SOT} of HSDT)

4.6.2.3.3.2 Leave High-Speed Data Transmission (TEOT of HSDT)

The display module will leave the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes MIPI_CLOCK_P/N enter the High-Speed Clock Mode (HSCM) through the MCU. This HSCM is kept until data lanes MIPI_DATA_P/N are in the LP-11 mode. Data lanes MIPI_DATA_P/N of the display module leave the High-Speed Data Transmission (T_{EOT} of HSDT) with the following sequence:

- Start: High-Speed Data Transmission (HSDT)
- Stop High-Speed Data Transmission
  - MCU changes to HS-1 if the last load bit is HS-0
  - MCU changes to HS-0 if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The leaving sequence of High-Speed Data Transmission (T_{EOT} of HSDT) is illustrated below:

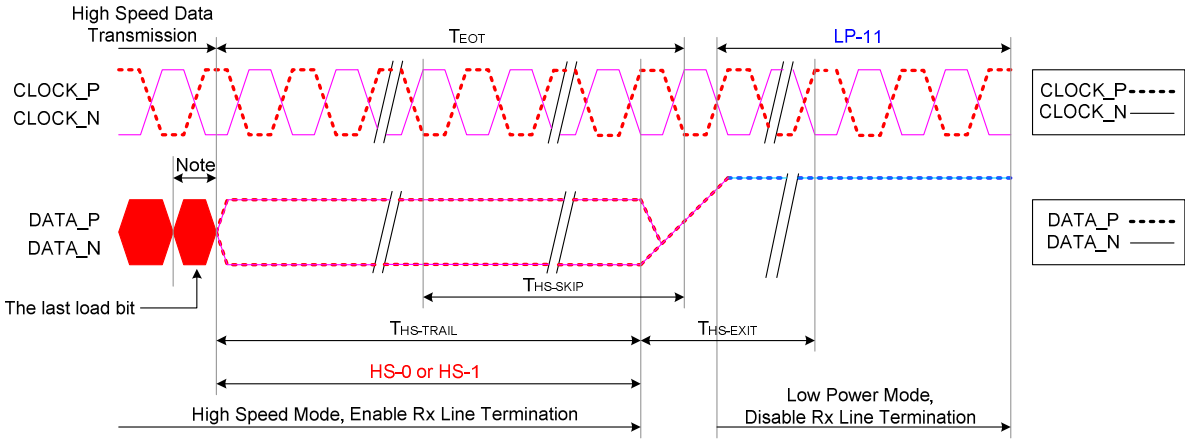

Figure 38: Leaving High-Speed Data Transmission

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

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4.6.2.3.3.3 Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the chapter "Short Packet (SPa) and Long Packet (LPa) Structures".

The single packet in High-Speed Data Transmission is illustrated below for reference purpose:

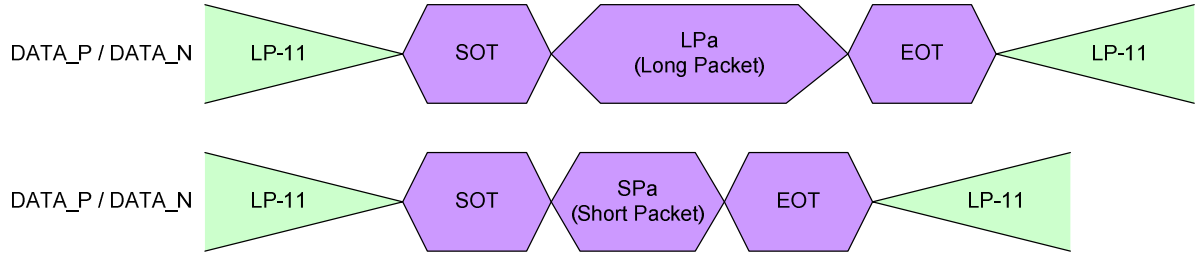

Figure 39: Single Packet in High-Speed Data Transmission

The multiple packets in High-Speed Data Transmission are illustrated below for reference purpose:

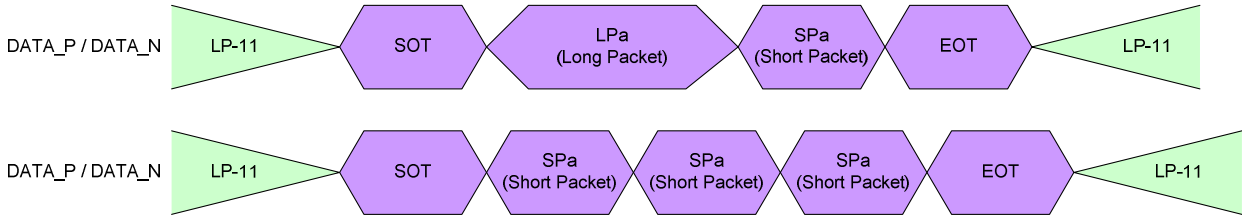

Figure 40: Multiple Packets in High-Speed Data Transmission (Examples)

Table 10: Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, both of Data lanes are 1 (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

4.6.2.3.3.4 Bus Turnaround (BTA)

The MCU or the display module, which controls MIPI_DATA_P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or the display module. The MCU and the display module use the same sequence when this bus turnaround procedure is applied. The sequence when the MCU wants to perform the bus turnaround procedure to the display module is described below for reference purpose:

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00=> LP-10=> LP-00
- The MCU waits until the display module starts to control MIPI_DATA_P/N data lanes and the MCU stops to

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control MIPI_DATA_P/N data lanes (= High-Z)

- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

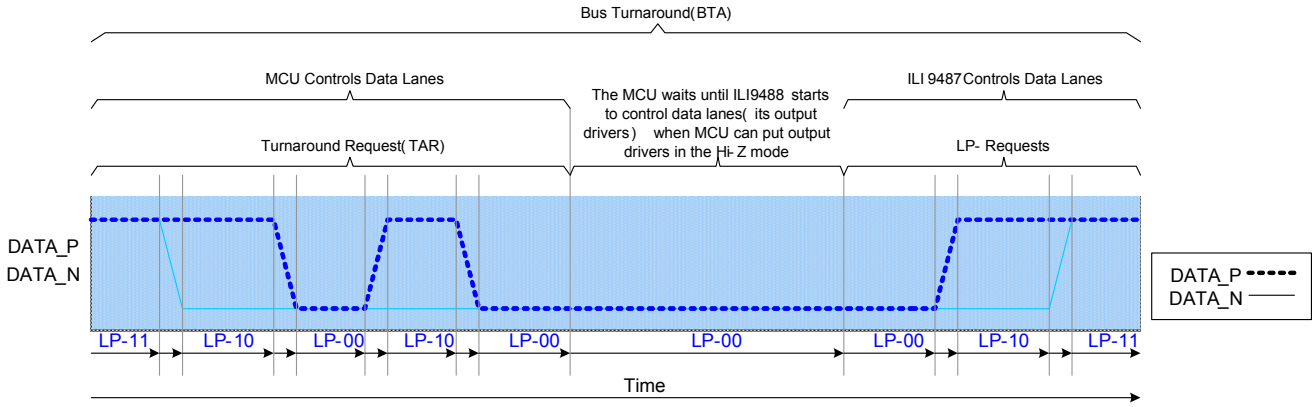

Figure 41: Bus Turnaround Procedure

MCU and display module can be switched in Figure 41 if the Bus Turnaround (BTA) is from the display module to the MCU.

4.6.3. Packet Level Communication

4.6.3.1. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type of the packet (SPa or LPa) can be recognized from their package headers (PH).

The Short Packet structure is illustrated as below:

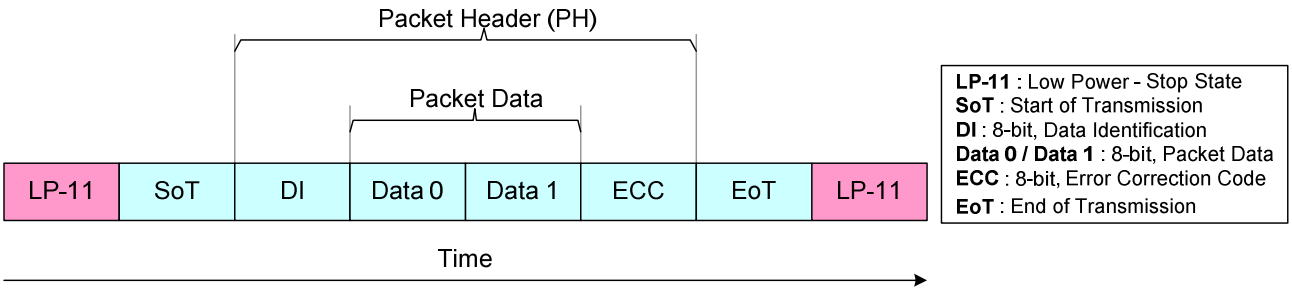

Figure 42: Short Packet (SPa) Structure

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The Long Packet structure is illustrated as below:

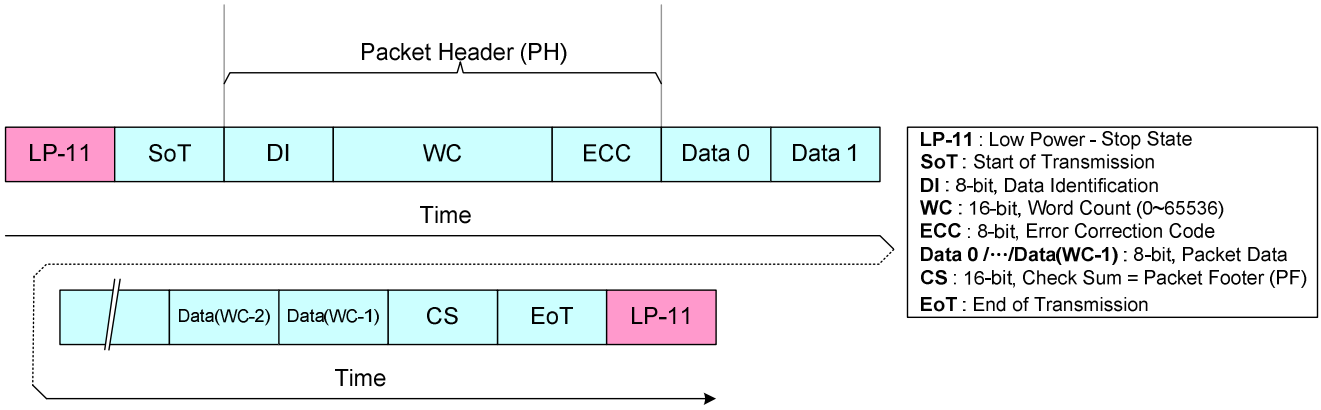

Figure 43: Long Packet (LPa) Structure

Note: Figure 42 and Figure 43 present a single packet sending (= includeing LP-11, SoT and EoT for each packet sending).

The other possibility is that SoT, EoT and LP-11 between packets are not necessary if packets are sent in multiple packet formats, for example:

- LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11
- LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11
- LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11

4.6.3.1.1. Bit Order of Bytes in Packets

The bit order of bytes, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first and the Most Significant Bit (MSB) of the byte is sent last.

This sending order is illustrated below for reference purpose.

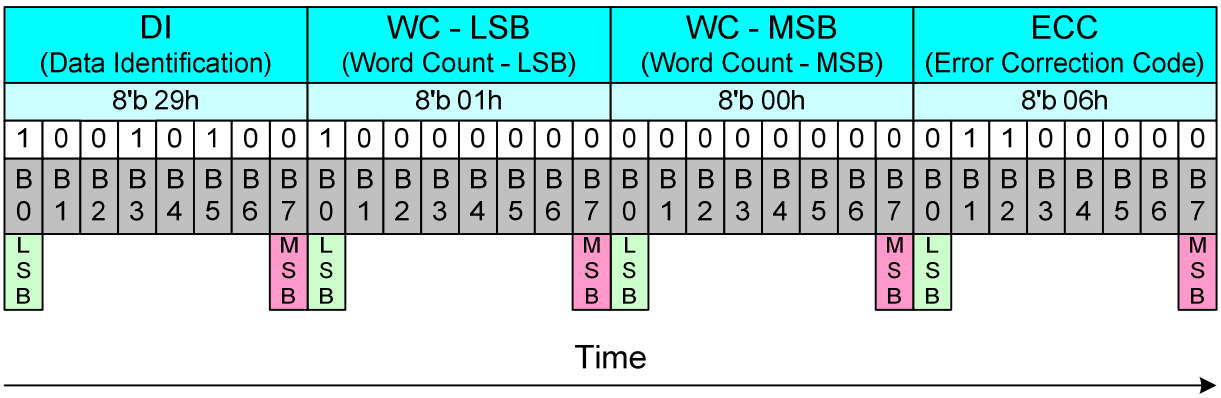

Figure 44: Bit Order of Bytes in Packets

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4.6.3.1.2. Byte Order of Multiple Byte Information in Packets

Byte order of multiple byte information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte of the information is sent last. For example, word Count (WC) consists of 2 bytes (= 16 bits), and the LS byte is sent first and the MS byte last.

This order is illustrated below for reference purpose.

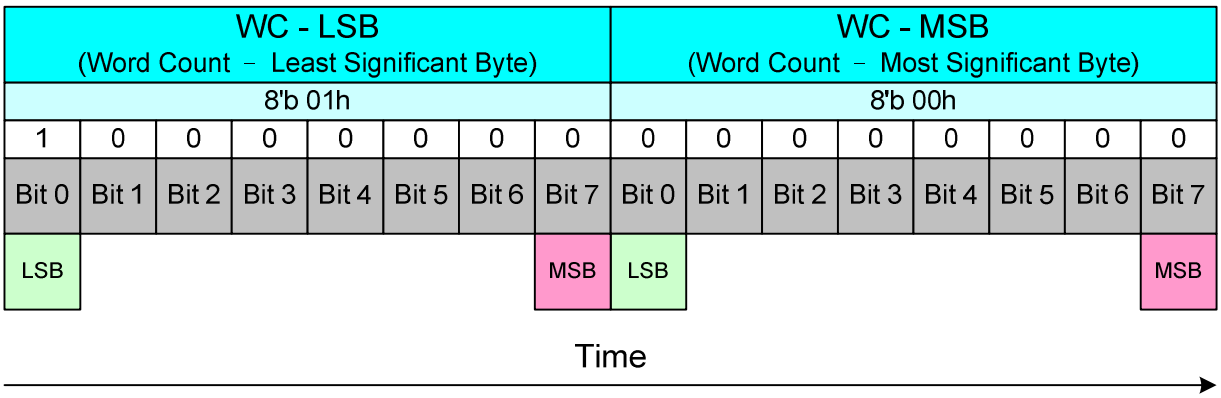

Figure 45: Byte Order of Multiple Byte Information in Packets

4.6.3.1.3. Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

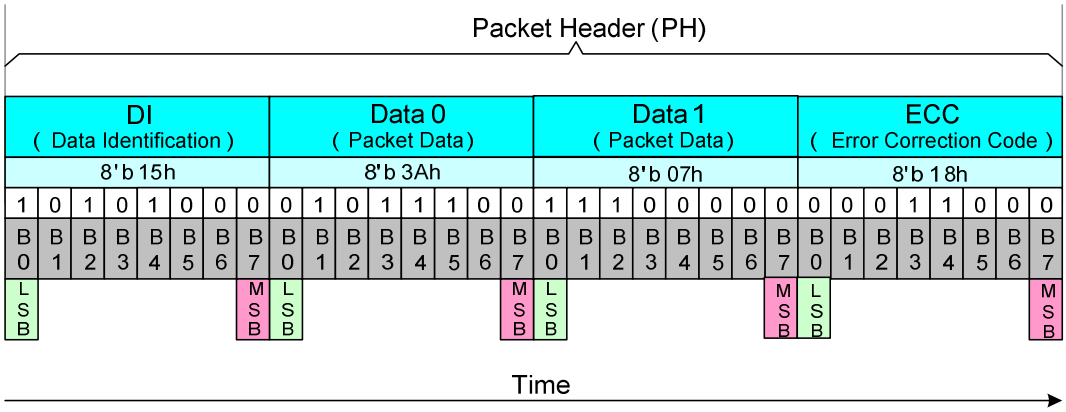

Figure 46: Packet Header (PH) of Short Packet

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Long Packet (LPa):

- 1st byte: Data Identification (DI) => identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

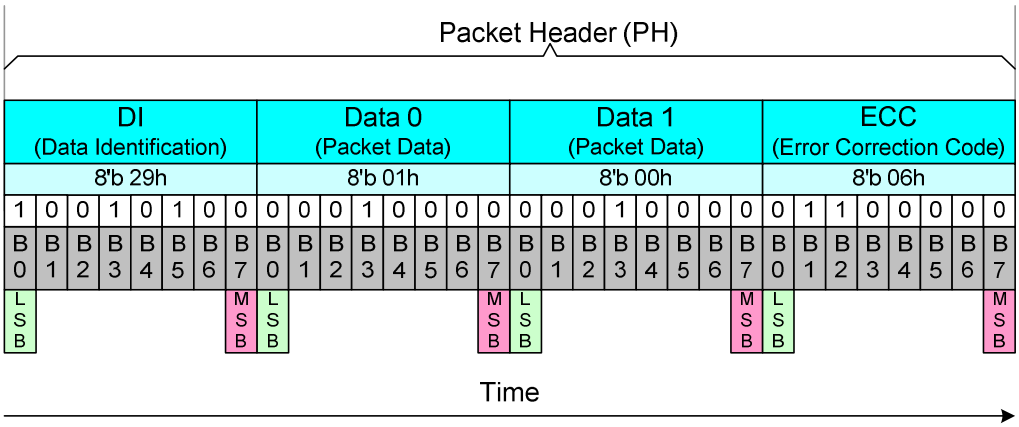

Figure 47: Packet Header (PH) of Long Packet

4.6.3.1.3.1 Data Identification (DI)

Data Identification (DI) is part of the Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated below.

DI (Data Identification)							
VC (Virtual Channel Identifier)		DT (Data Type)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure 48: Data Identification (DI) Structure

Data Identification (DI) of the Packet Header (PH) is illustrated below for reference purpose.

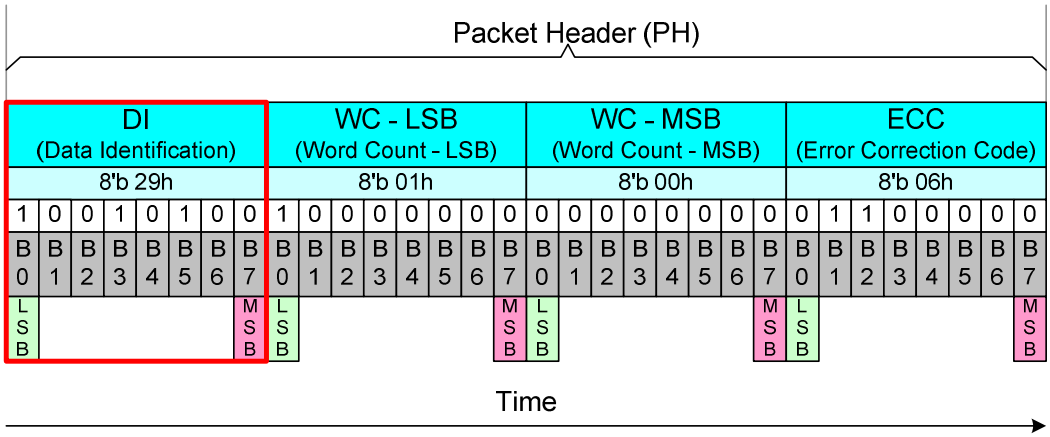

Figure 49: Data Identification (DI) of the Packet Header (PH)

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Virtual Channel (VC)

Virtual Channel (VC) is part of the Data Identification (DI [7…6]) structure, and it is used to indicate where a packet is to be sent from the MCU.

Bits of the Virtual Channel (VC) are illustrated below for reference purpose.

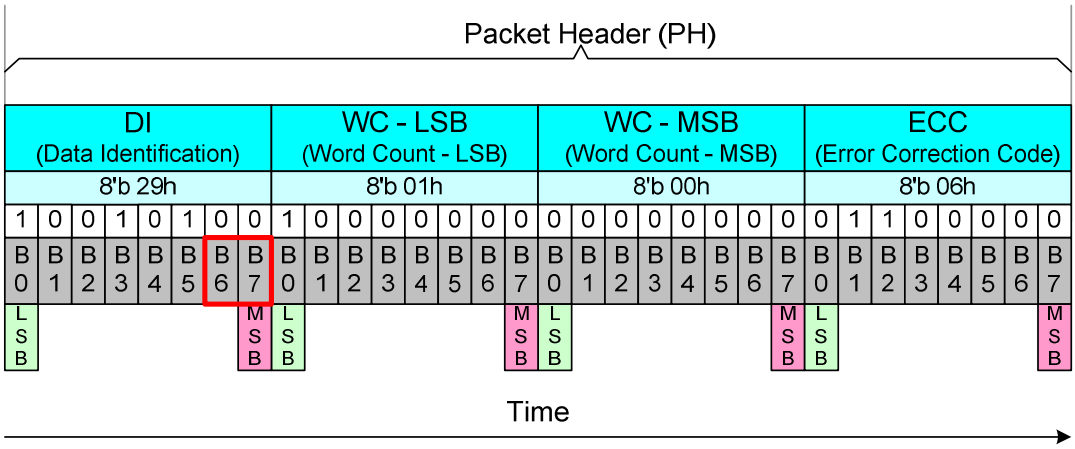
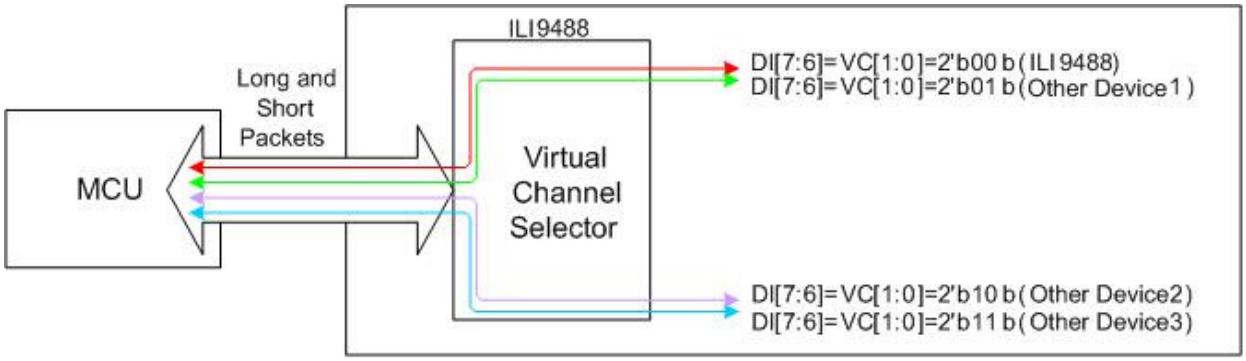


Figure 50: Virtual Channel (VC) of the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels to 4 different display modules. Devices use the same virtual channel as which the MCU uses to send packets to them, for example,

- The MCU uses the virtual channel 0 when it sends packets to the ILI9488.
- The ILI9488 also uses the virtual channel 0 when it sends packets to the MCU.

This functionality is illustrated below.



Virtual Channel (VC) is always 0 (DI [7..6] = VC [1..0] = 00b) when the MCU sends End of Transmission Packet to the display module.

The ILI9488 does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1…0]) is 00b for this display module.

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Data Type (DT)

Data Type (DT) is part of the Data Identification (DI [5…0]) structure, and it is used to define the type of the used data in a packet.

Bits of the Data Type (DT) are illustrated below for reference purpose.

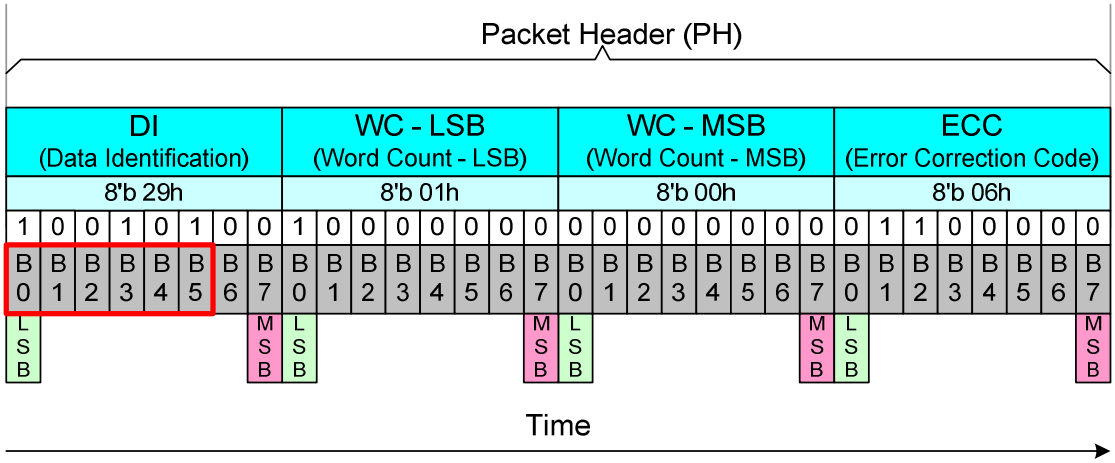

Figure 51: Data Type (DT) of the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. This Data Types (DT) is defined in the tables below.

Table 11: Data Type from the MCU to the Display Module (ILI9488)

From the MCU to the Display Module (ILI9488)									
Bit5	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Hex**	**Description**	**Short/Long Packet**	**Abbreviation**
0	0	1	0	0	0	08	End of Transmission Packet [Note1]	SPa (Short Packet)	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data [Note2]	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Notes:

1. This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.
2. This can be used when data lanes are to be kept in the High Speed Data Transferring (HSDT) Mode.

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Table 12: Data Type from the Display Module (ILI9488) to the MCU

From to the Display Module (ILI9488) to the MCU									
Bit5	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Hex**	**Description**	**Short/Long Packet**	**Abbreviation**
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

The receiver will ignore other Data Types (DT) if they are not defined in the two tables above.

4.6.3.1.3.2 Packet Data of a Short Packet

Packet Data (PD) of the Short Packet (SPa) is placed after the Data Type (DT) of the Data Identification (DI), which indicates that a Short Packet (SPa) is to be sent.

The Word Count (WC) indicates the number of Bytes of Packet Data (PD) sent after the Packet Header (PH).

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

The sending order of Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated below for reference purpose.

Packet Data (PD) information (2 bytes):

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)

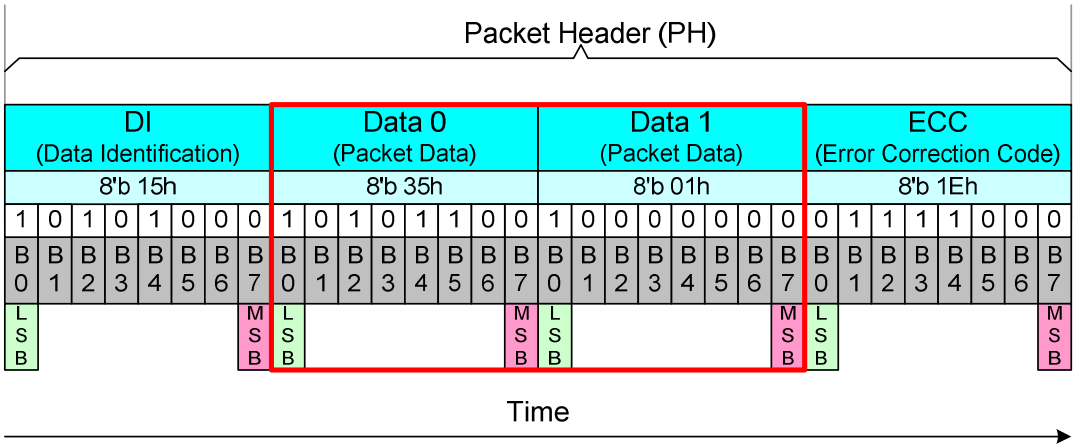

Figure 52: Packet Data (PD) of a Short Packet, 2 Bytes Information

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Packet Data (PD) information (1 byte):

- Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)

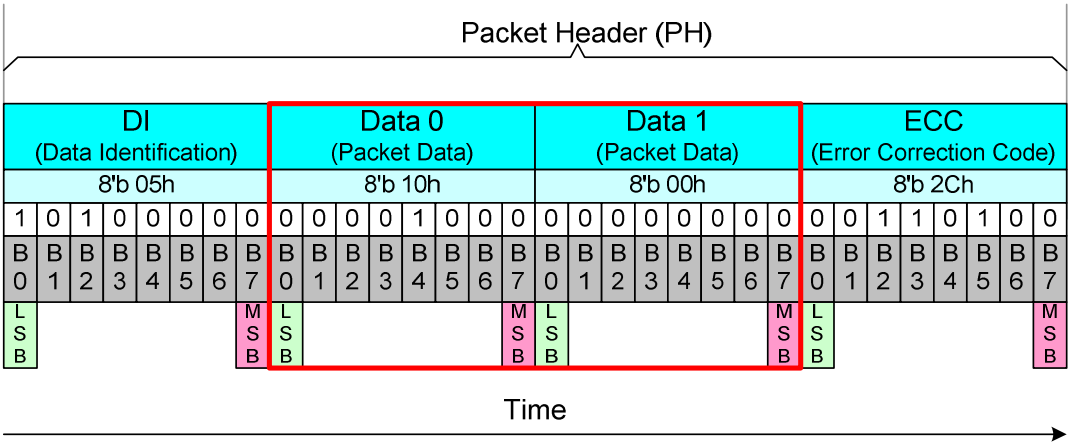

Figure 53: Packet Data (PD) of a Short Packet, 1 Byte Information

4.6.3.1.3.3 Word Count of a Long Packet

Word Count (WC) of a Long Packet (LPa) is placed after the Data Type (DT) of the Data Identification (DI), which indicates that a Long Packet (LPa) is to be sent.

Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) which are to be sent after the Packet Header (PH). The location of Word Count (WC) in a Long Packet is the same as which of Packet Data (PD) in a Short Packet, as illustrated in Figure 55 below.

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first and the Most Significant (MS) Byte is sent last.

Word Count (WC) of a Long Packet (LPa) is illustrated below for reference purpose.

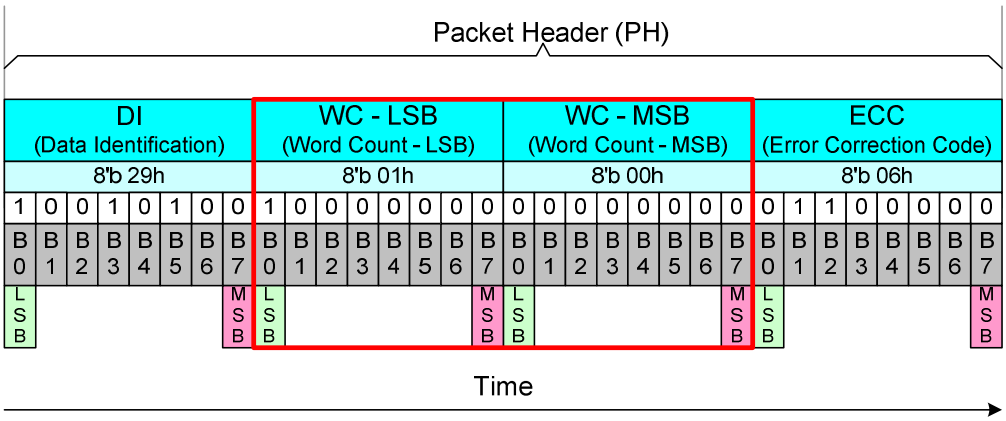

Figure 54: Word Count (WC) of a Long Packet

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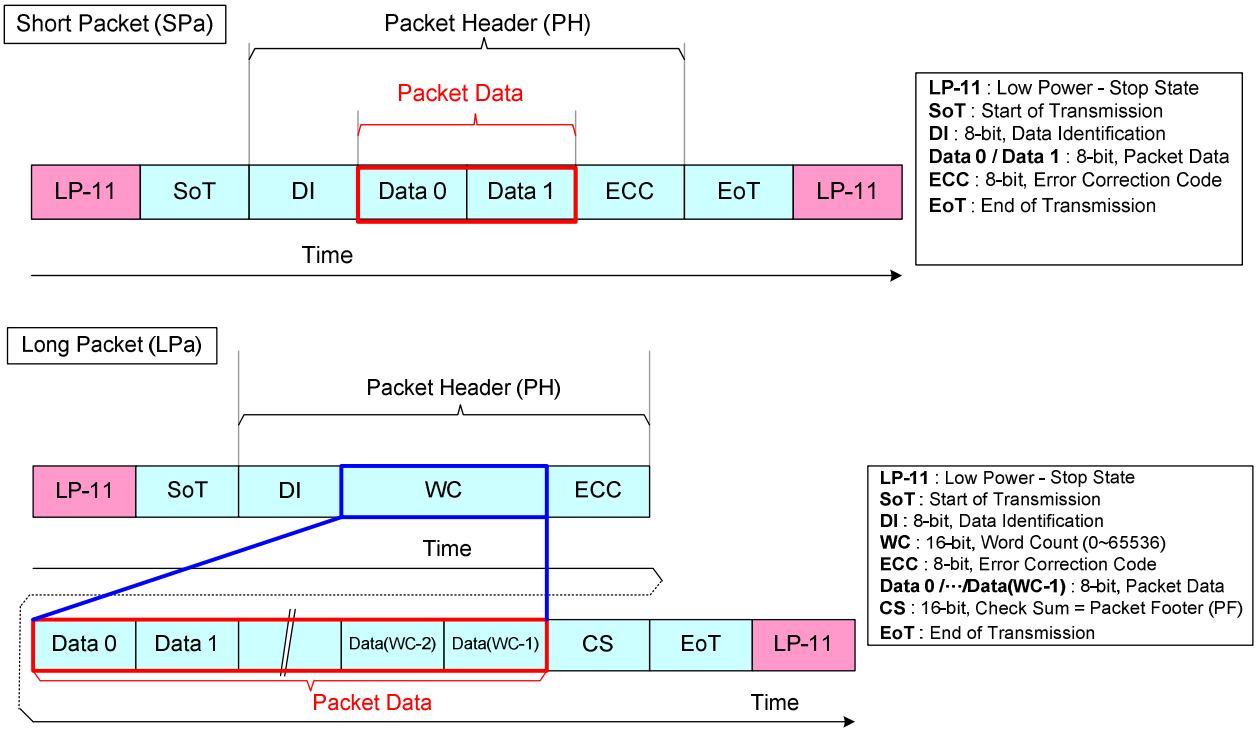

Figure 55: Packet Data in Short and Long Packets

4.6.3.1.3.4 Error Correction Code (ECC)

Error Correction Code (ECC) is part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D [23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D [23…0])

D [23…0] is illustrated for reference purposes below.

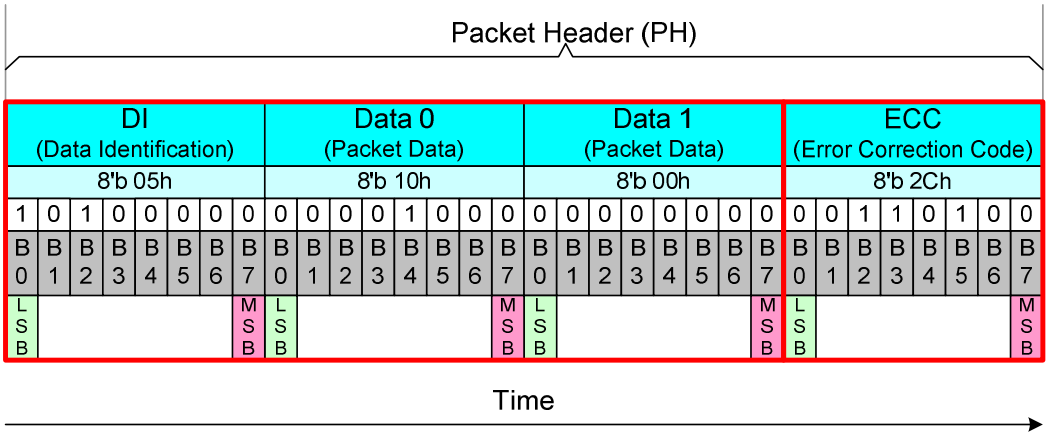

Figure 56: D [23…0] and P [7…0] in a Short Packet

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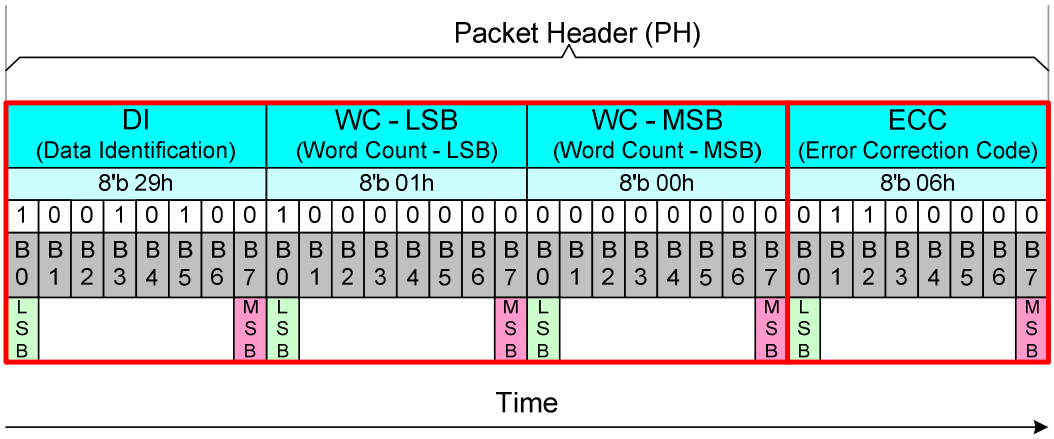

Figure 57: D [23…0] and P [7…0] in a Long Packet

Error Correction Code (ECC) can recognize one error or several errors, but only a one-bit error will be corrected. Bits (P [7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as below:

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D [63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, only 6 bits (P [5…0]) for Error Correction Code (ECC) are needed.

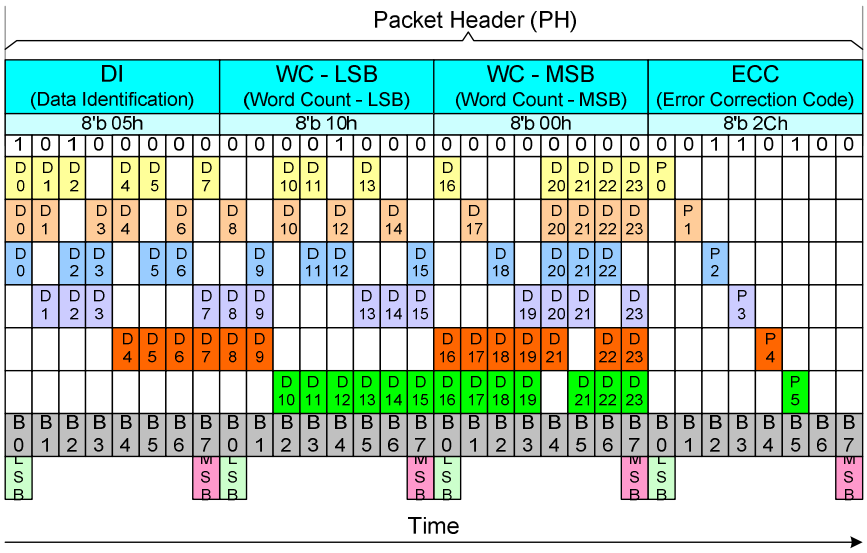

Figure 58: XOR Function on a Short Packet

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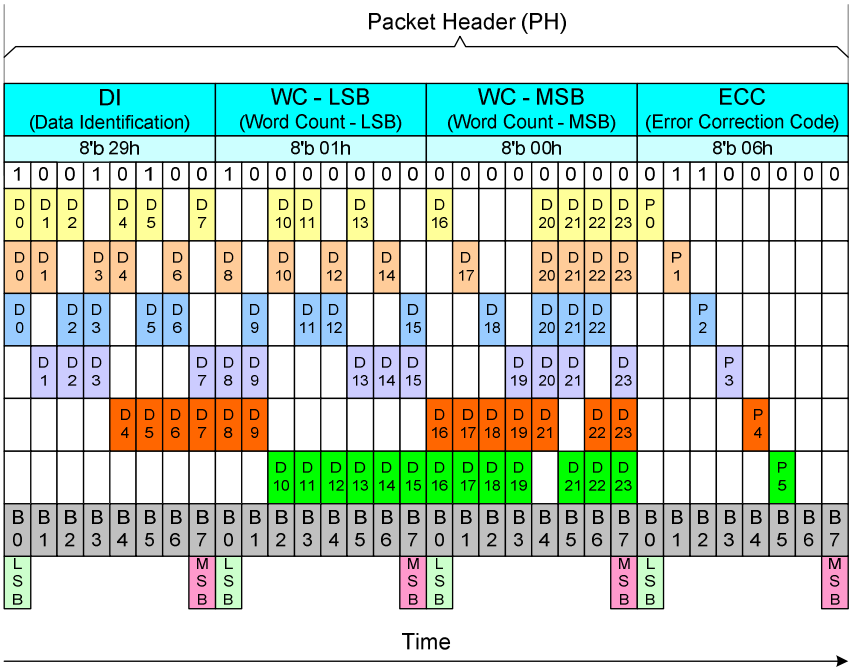
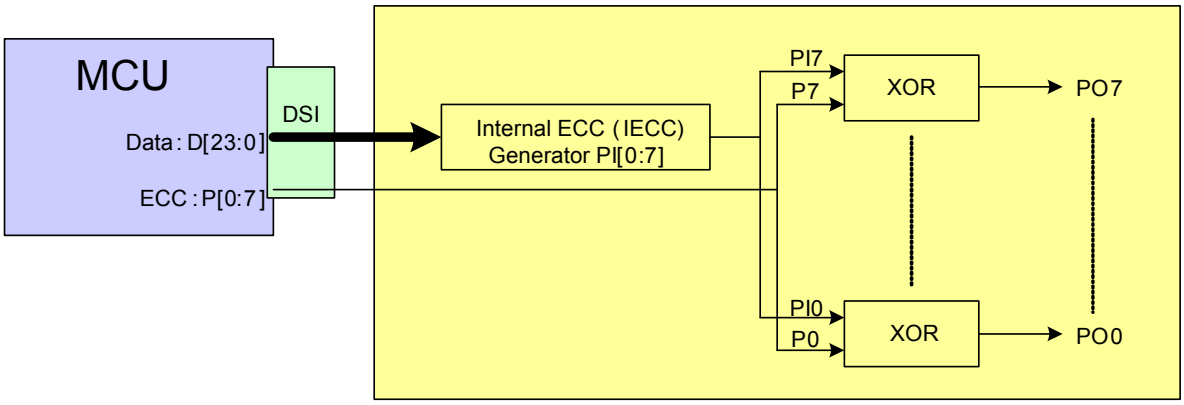


Figure 59: XOR Function on a Long Packet

The transmitter (the MCU or the Display Module) sends data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (the Display Module or the MCU) calculates an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated below for reference purpose.



The sent data bits (D [23…0]) and ECC (P [7…0]) are received correctly, if the value of the PO [7…0]) is 00h. The sent data bits (D [23…0]) and ECC (P [7…0]) are not received correctly, if the value of the PO [7…0]) is not 00h.

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ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 60: Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 61: Internal XOR Calculation between ECC and IECC Values – Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D [23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to values in the following table.

Table 13: One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

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One error is detected if the value of the PO [7…0] is in Table 13: One Bit Error Value of the Error Correction Code (ECC), and the receiver can correct this one bit error because this found value also defines the location of the corrupt bit, for example,

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), which is not correct, is D [3]

More than one error is detected if the value of the PO [7…0] is not in Table 13: One Bit Error Value of the Error Correction Code (ECC), for example, PO [7…0] = 0Ch.

4.6.3.1.4. Packet Data on a Long Packet

Packet Data (PD) of the Long Packet (LPa) is transmitted after the Packet Header (PH) of the Long Packet (LPa). The amount of the data bytes is defined in the chapter “Word Count (WC) of the Long Packet (LPa)”.

4.6.3.1.5. Packet Footer on a Long Packet

Packet Footer (PF) of the Long Packet (LPa) is placed after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is the checksum value which is calculated from the Packet Data of the Long Packet (LPa).

The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial $X_{16}+X_{12}+X_5+X_0$ as illustrated below.

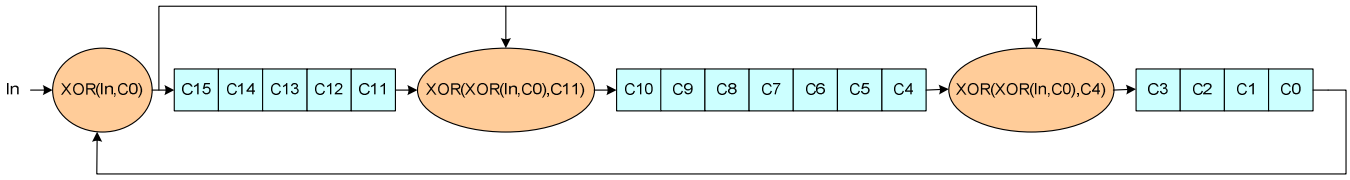

Figure 62: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

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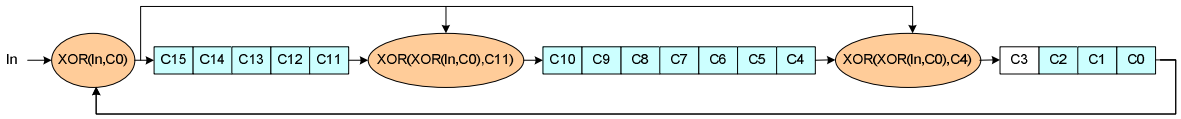

Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 63: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

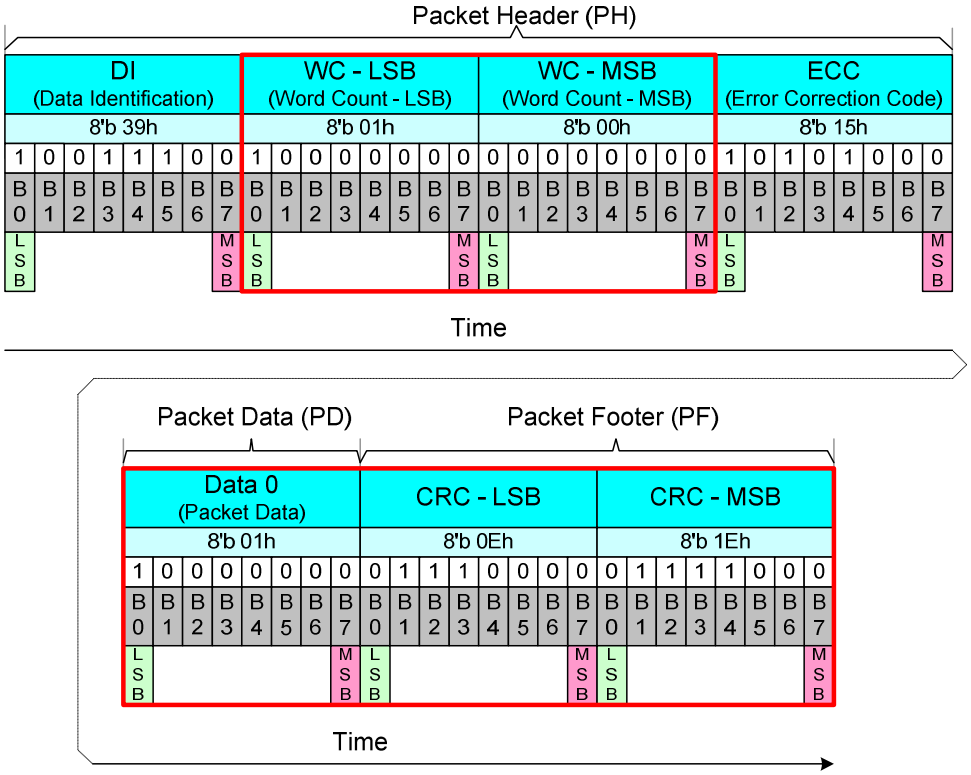

Figure 64: Packet Footer (PF) Example

The receiver calculates its own checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) which the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) is equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

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4.6.3.2. Packet Transmission

4.6.3.2.1. Packet from the MCU to the Display Module

4.6.3.2.1.1 Display Command Set (DCS)

Display Command Set (DCS) is transmitted from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), which is included in Short Packets (SPa) and Long packets (LPa), as illustrated below.

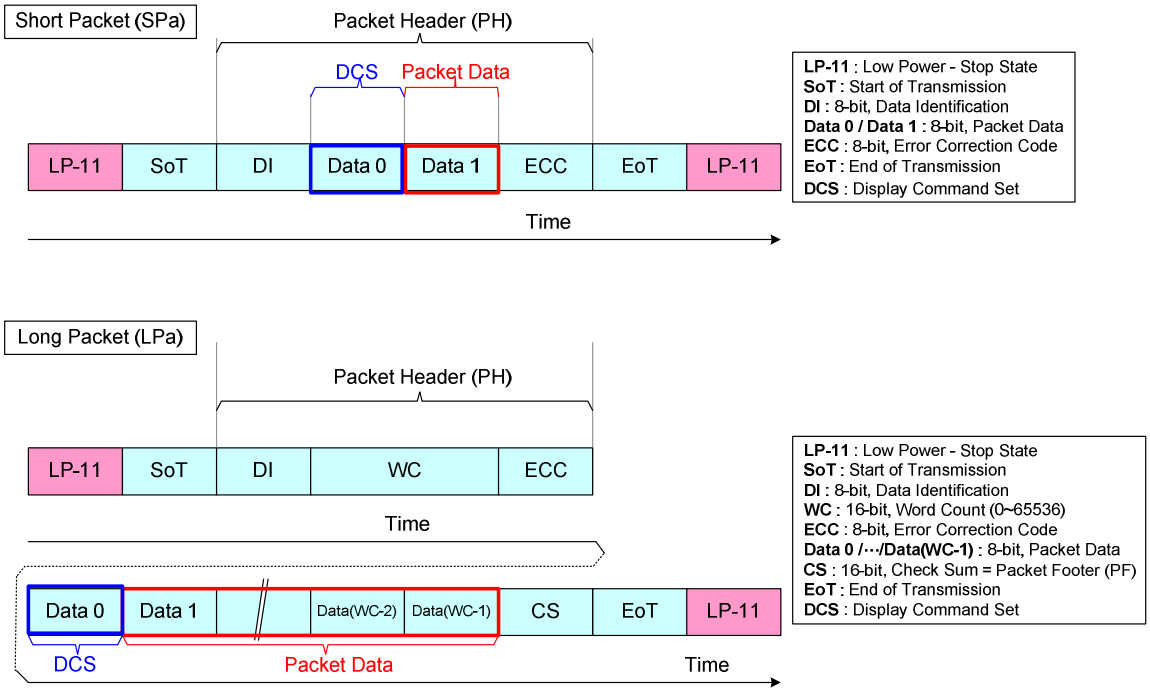

Figure 65: Display Command Set (DCS) in Short Packet and Long Packet

4.6.3.2.1.2 Display Command Set Write, no Parameter (DSCWN-S)

"Display Command Set (DCS) Write, No Parameter" is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined in the table below.

Table 14: Display Command Set Write, no Parameter (DSCWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep IN(10h)
Sleep Out (11h)
Partial Mode ON (12h)
Normal Display Mode ON (13h)
Display OFF (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode OFF (38h)

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Idle Mode ON (39h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 0101b
- Packet Data (PD)
  - Data 0: “Sleep In (10h)”, Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

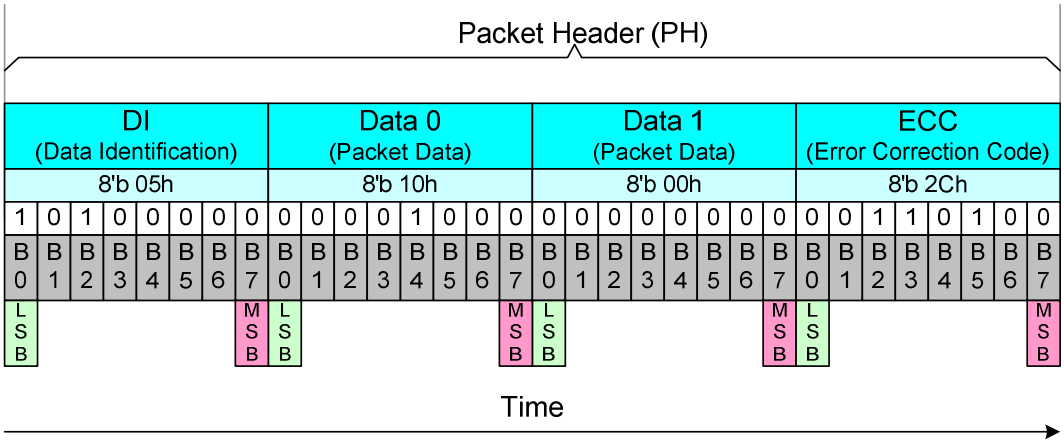

Figure 66: Display Command Set (DCS) Write, no Parameter (DCSWN-S) – Example

4.6.3.2.1.3 Display Command Set Write, 1 Parameter (DCSW1-S)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined in the table below.

Table 15: Display Command Set Write, 1 Parameter (DSCW1-S)

Command
Gamma Set
Memory Write (2Ch) [Note]
Tearing Effect Line ON (35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch) [Note]
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

Note: One Subpixel has been written.

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A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

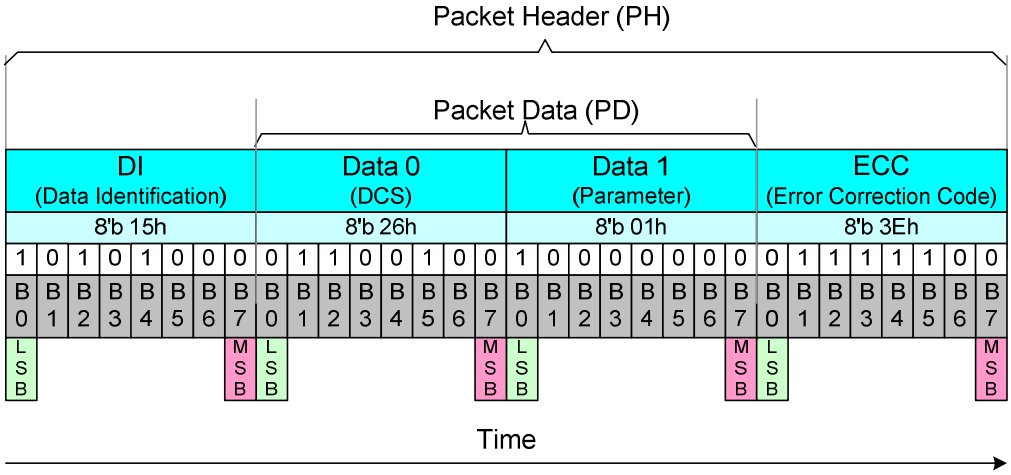

Figure 67: Display Command Set Write, 1 Parameter (DCSW1-S) – Example

4.6.3.2.1.4 Display Command Set Write Long (DCSW-L)

“Display Command Set (DCS) Write Long” (DCSW-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in the table below.

Table 16: Display Command Set Write Long (DSCW-L)

Command
NOP (00h) Note 1
Software Reset (01h) Note 1
Sleep IN(10h) Note 1
Sleep Out (11h) Note 1
Partial Mode ON (12h) Note 1
Normal Display Mode ON (13h) Note 1
Gamma Set (26h) Note 2
Display OFF (28h) Note 1
Display ON (29h) Note 1
Column Address Set (2Ah)
Page Address Set (2Bh)
Memory Write (2Ch) Note 2
Partial Area (30h)

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Tearing Effect Line OFF (34h) Note 1
Tearing Effect Line ON (35h) Note 2
Memory Access Control (36h) Note 2
Idle Mode OFF (38h) Note 1
Idle Mode ON (39h) Note 1
Interface Pixel Format(3Ah)
Memory Write Continue (3Ch) Note 2
Write Display Brightness (51h) Note 2
Write CTRL Display (53h) Note 2
Write Content Adaptive Brightness control (55h) Note 2
Write CABC Minimum Brightness (5Eh)

Notes:

1. It can also be used in a Short Packet (SPa); See chapter “Display Command Set (DCS) Write, No Parameter”.
2. It can also be used in a Short Packet (SPa); See chapter “Display Command Set (DCS) Write, 1 Parameter”.

The Long Packet (LPa), when a command (No Parameter) is sent, is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0 => “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

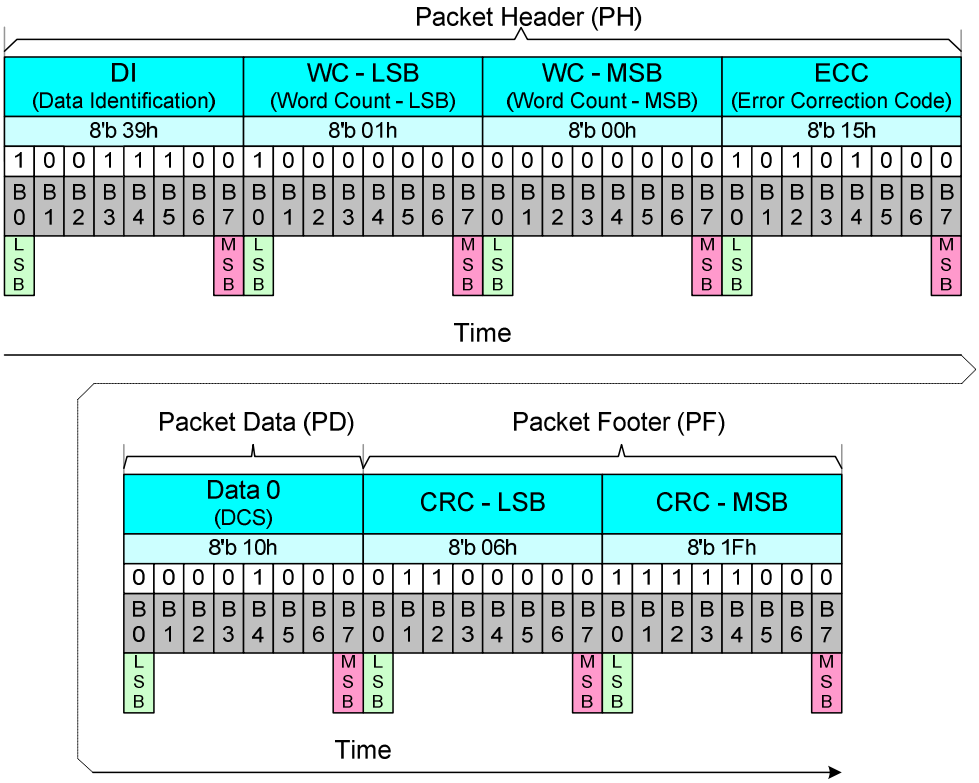

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Figure 68: Display Command Set Write Long (DCSW-L) with DCS Only – Example

The Long Packet (LPa), when a Write (1 parameter) is sent, is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

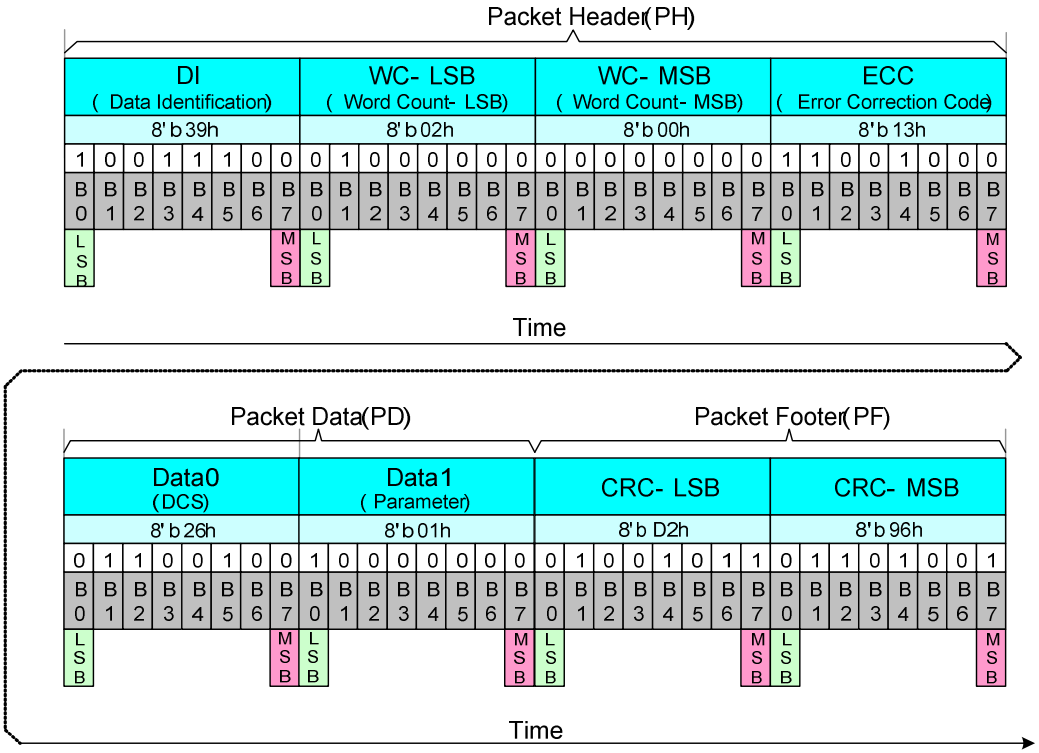

Figure 69: Display Command Set Write Long (DCSW-L) with DCS and 1 Parameter – Example

The Long Packet (LPa), when a Write (4 parameters) is sent, is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):

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- Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS)
- Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15…8]
- Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7…0]
- Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15…8]
- Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7…0]

- Packet Footer (PF)

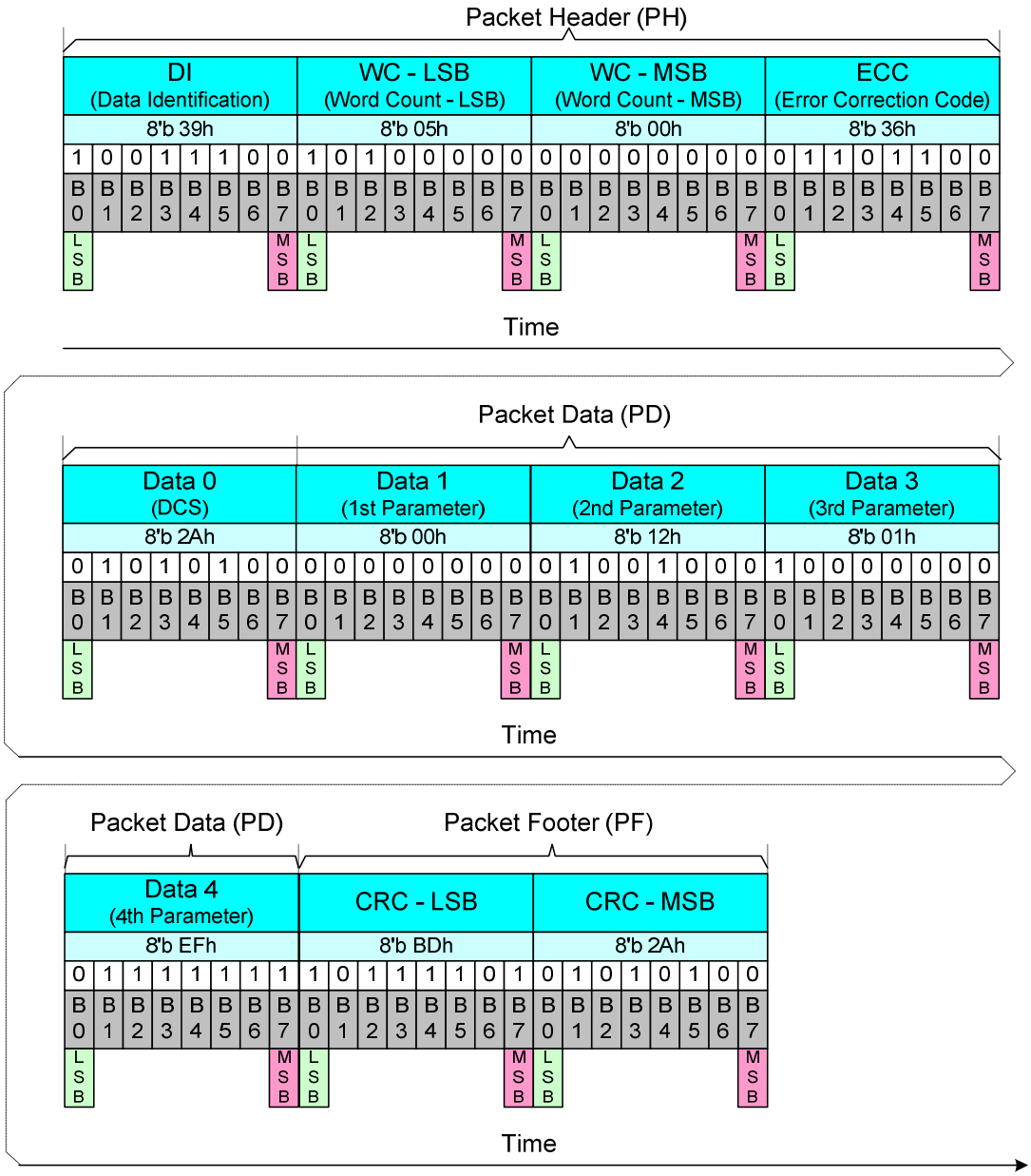

Figure 70: Display Command Set Write Long with DCS and 4 Parameters – Example

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4.6.3.2.1.5 Display Command Set Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined in the table below. The 1st parameter (Dummy Data) will not return to the DSI after it is done in the MCU parallel interface. The first returned parameter is the 2nd parameter in the DSI.

Table 17: Display Command Set Read, No Parameter (DCSRN-S)

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Memory Read (2Eh)
Memory Read Continue (3Eh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Content Adaptive Brightness Control (56h)
Read CABC Minimum Brightness (5Fh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command used for this purpose is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which uses Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This sequence is illustrated below for reference purpose.

Step 1:

- The MCU sends "Set Maximum Return Packet Size" (SMRPS-S) (Short Packet (SPa)) to the display module when the display module wants to return one byte to the display module.
- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - Data 0: 01hex
  - Data 1: 00hex
- Error Correction Code (ECC)

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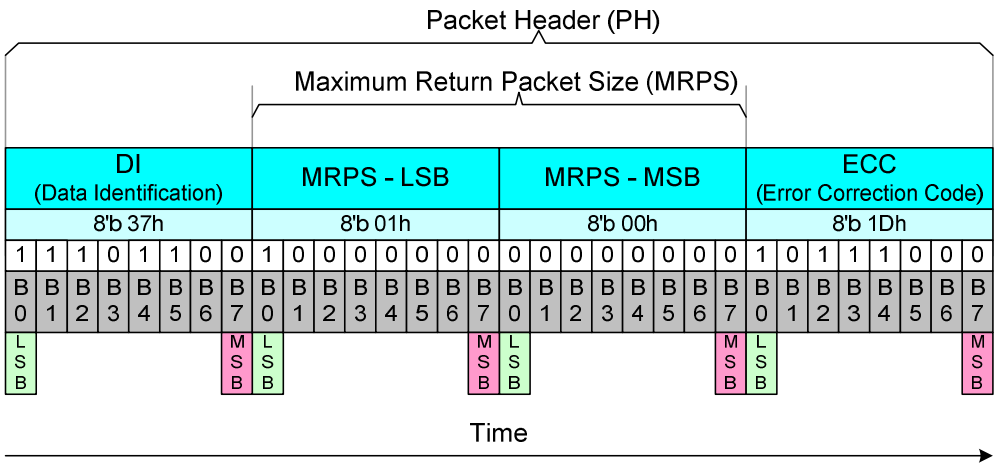

Figure 71: Set Maximum Return Packet Size (SMRPS-S) – Example

Step 2:

- The MCU wants to receive the value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to the display module.
- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 0110b
- Packet Data (PD)
  - Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

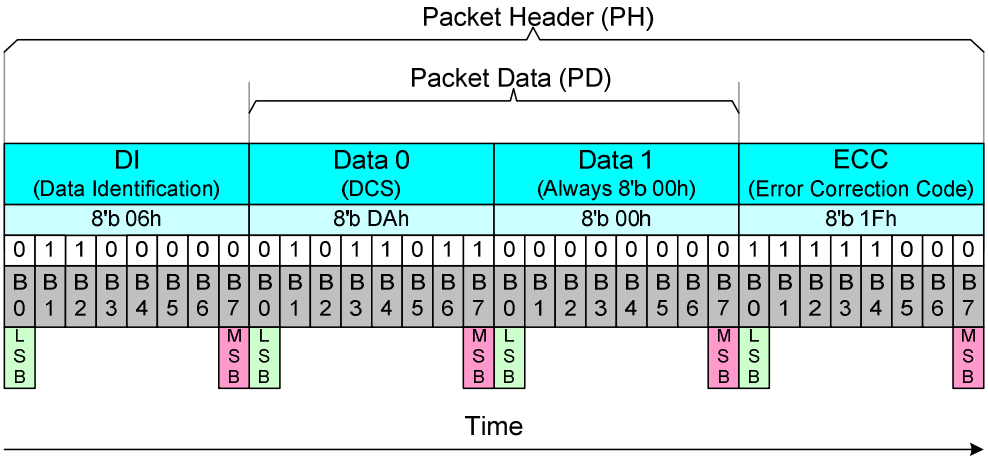

Figure 72: Display Command Set Read, No Parameter (DCSRN-S) – Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

- An Acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if an error is found while receiving a command.
- Information of the received command, which can be in a Short Packet (SPa) or Long Packet (LPa).

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4.6.3.2.1.6 Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 00 1001b), from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT), if necessary.

The display module can ignore the Packet Data (PD), which is sent by the MCU.

The Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) are sent, is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex (Random data)
  - Data 1: 23hex (Random data)
  - Data 2: 12hex (Random data)
  - Data 3: A2hex (Random data)
  - Data 4: E2hex (Random data)
- Packet Footer (PF)

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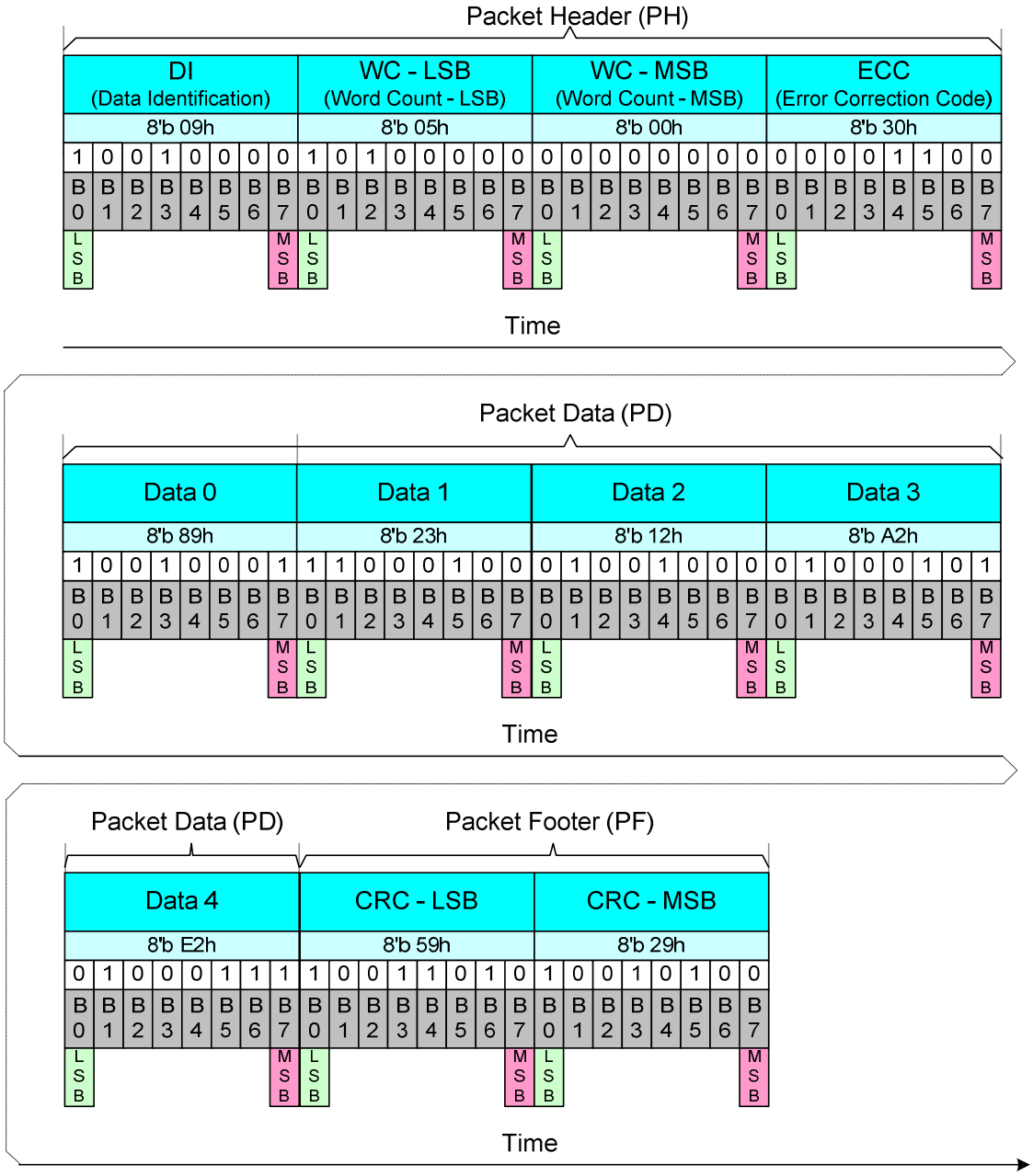

Figure 73: Null Packet, No Data (NP-L) – Example

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4.6.3.2.1.7 End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP), which is optional in the interface level and is defined in the Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the High Speed Data Transmission (HSDT) mode properly when the EoTP is added after the last payload packet before "End of Transmission" (EoT).

The MCU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module will/will not receive "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= leaving Escape mode), which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Table 18: Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) uses a fixed format as follows:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - Data 0: 0Fhex
  - Data 1: 0Fhex
- Error Correction Code (ECC)
  - ECC: 01hex

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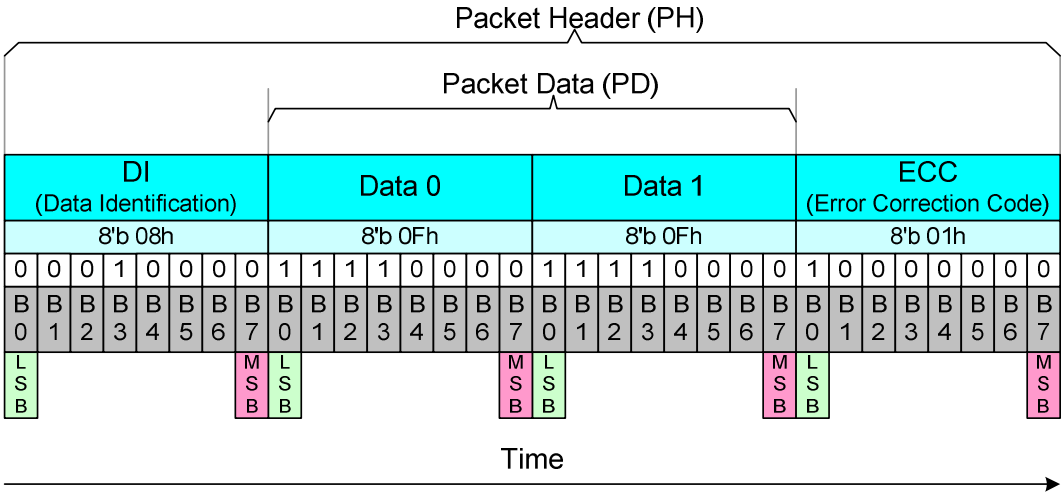

Figure 74: End of Transmission Packet (EoTP)

Some cases of the “End of Transmission Packet” (EoTP) are illustrated below for reference purpose only.

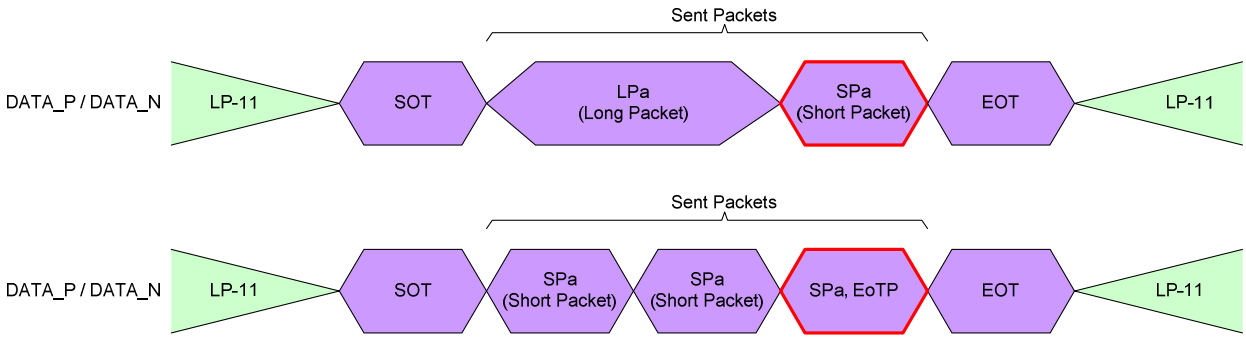

Figure 75: End of Transmission Packet (EoTP) – Examples

4.6.3.2.2. Packet from the Display Module to the MCU

4.6.3.2.2.1. Used Packet Type

The display module can use Short Packets (SPa) or Long Packets (LPa) when it returns information to the MCU after the MCU requests information from the Display Module. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report (AwER).

The used packet type is defined in the Data Type (DT). If the maximum size of the Packet Data (PD) could be sent in one packet, then the display module cannot separate returned bytes into several packets.

Both cases are illustrated below for reference purpose.

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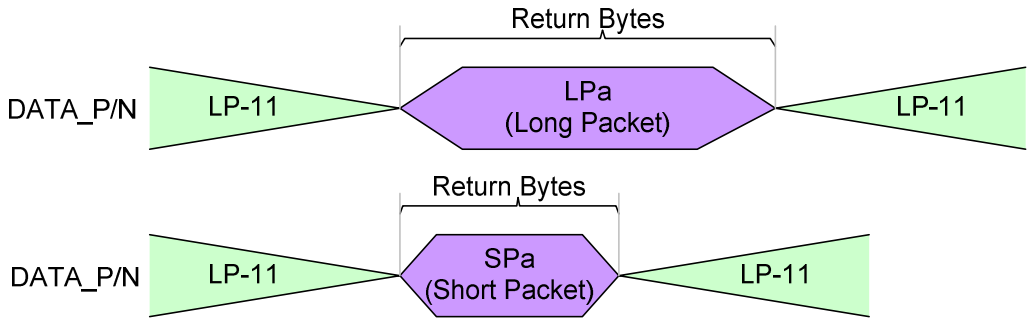

Figure 76: Return Bytes in Single Packet

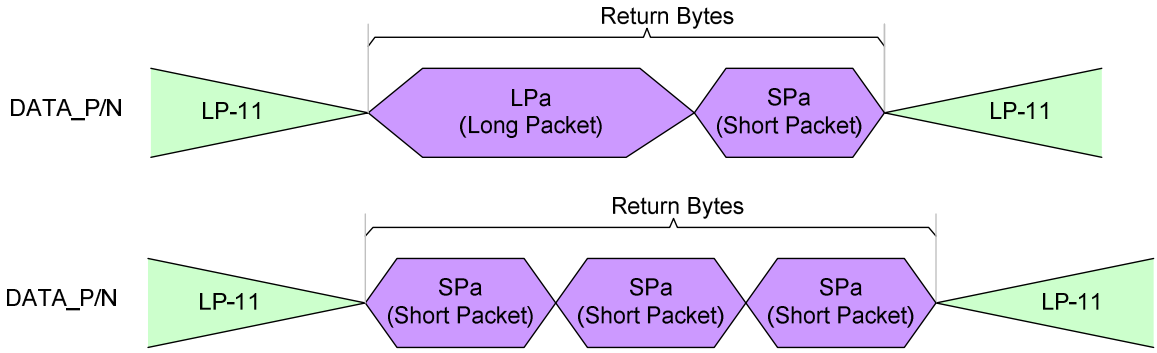

Figure 77: Return Bytes in Multiple Packets – Now Allowed

Exception:

The display module returns 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module receives a read command (see the chapter "Display Command Set (DCS) Read, No Parameter (DCSRN-S)"), in which a single bit error is detected and corrected by the EEC (see bit 8 in Table 19: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response). These returned packets are illustrated below for reference purpose.

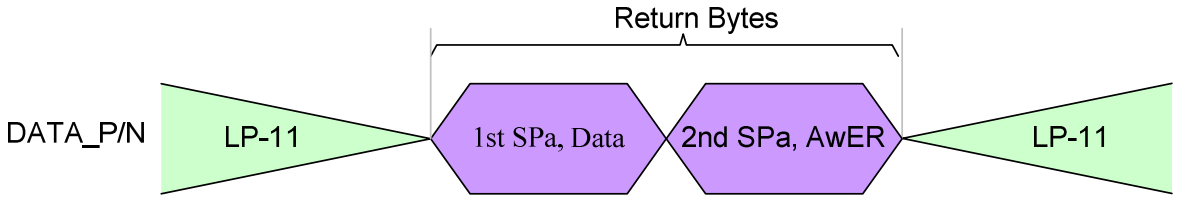

Figure 78: Exception when Return Bytes in Several Packets

AwER = Acknowledge with Error Report

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4.6.3.2.2.2 Acknowledge with Error Report

"Acknowledge with Error Report" (AwER) is always transmitted through a Short Packet (SPa), which is defined in the Data Type (DT, 00 0010b), from the display module to the MCU. The 16 bits in the Packet Data (PD) can indicate the current error(s) if one or more than one bit(s) is/are set to 1, as defined in the following table.

Table 19: Acknowledge with Error Report (AwER)

Bit	The Description of Acknowledge Error Report (AwER)	
	Short Packet	Long Packet
0	SoT Error	SoT Error
1	SoT Sync Error	SoT Sync Error
2	EoT Sync Error	EoT Sync Error
3	Escape Mode Entry Command Error	Escape Mode Entry Command Error
4	Low-Power Transmit Error	Low-Power Transmit Error
5	Any Protocol Timer-Out	Any Protocol Timer-Out
6	False Control Error	False Control Error
7	Contention is Detected on the Display Module	Contention is Detected on the Display Module
8	ECC Error, Single-Bit (Detected and Corrected)	ECC Error, Single-Bit (Detected and Corrected)
9	ECC Error, Multi-Bit (Detected, Not Corrected)	ECC Error, Multi-Bit (Detected, Not Corrected)
10	Reserved, Set to 0 internally	Checksum Error
11	DSI Data Type (DT), Not Recognized	DSI Data Type (DT), Not Recognized
12	DSI Virtual Channel (VC) ID Invalid	DSI Virtual Channel (VC) ID Invalid
13	DSI Protocol Violation	DSI Protocol Violation
14	Reserved, Set to 0 internally	Reserved, Set to 0 internally
15	Reserved, Set to 0 internally	Reserved, Set to 0 internally

These errors are included in all packages, which are received from the MCU to the display module before the Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) in a Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

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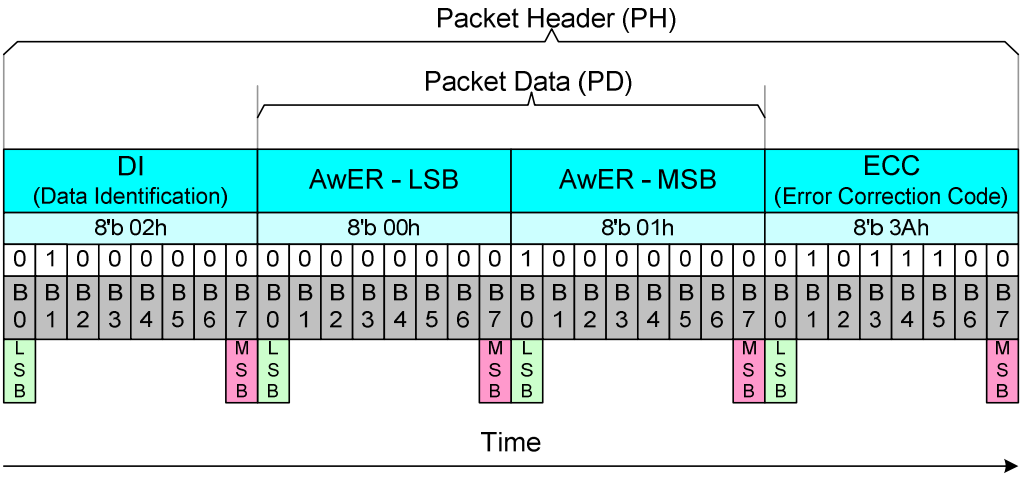
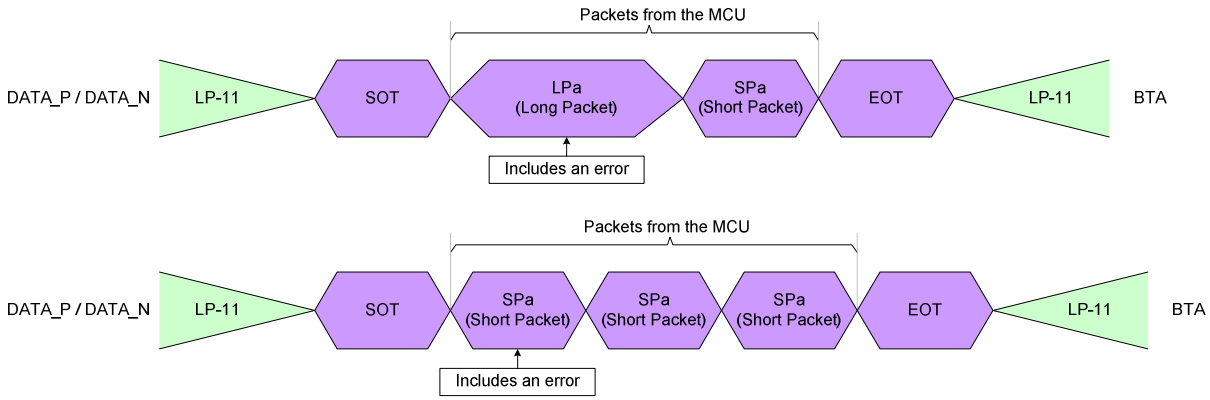


Figure 79: Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated below for reference purpose.



Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets are indicated by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. If a received packet includes an error, the bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1.

The numbers of the packets, including an ***ECC or CRC*** error, are calculated in the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated below for reference purpose.

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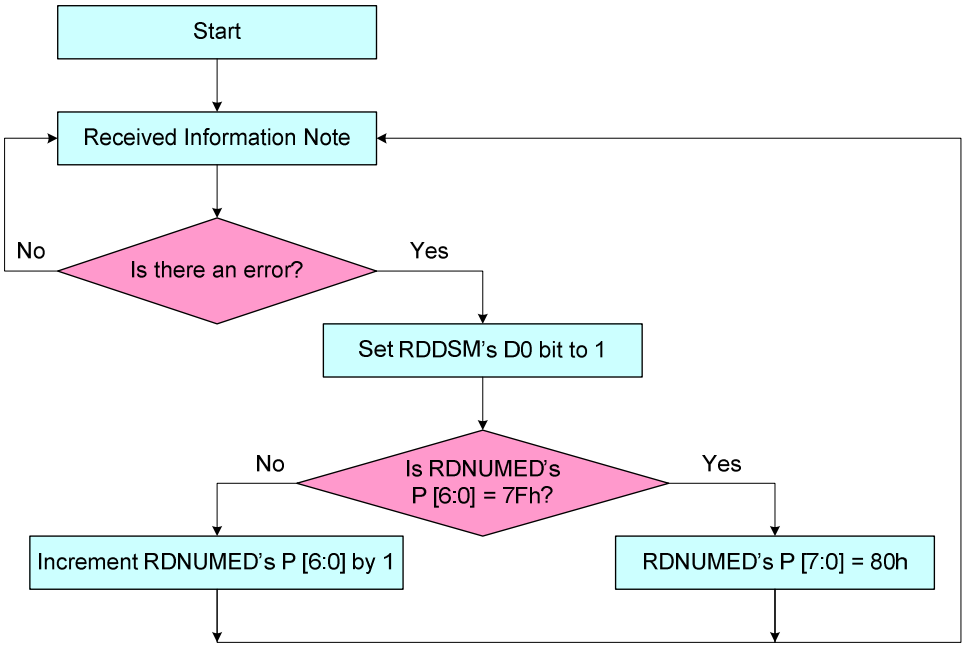

Figure 80: Flow Chart for Errors on DSI

4.6.3.2.2.3 DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 01 1100b), from the display module to the MCU.

"DCS Read Long Response" (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

The Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex
  - Data 1: 23hex
  - Data 2: 12hex
  - Data 3: A2hex
  - Data 4: E2hex
- Packet Footer (PF)

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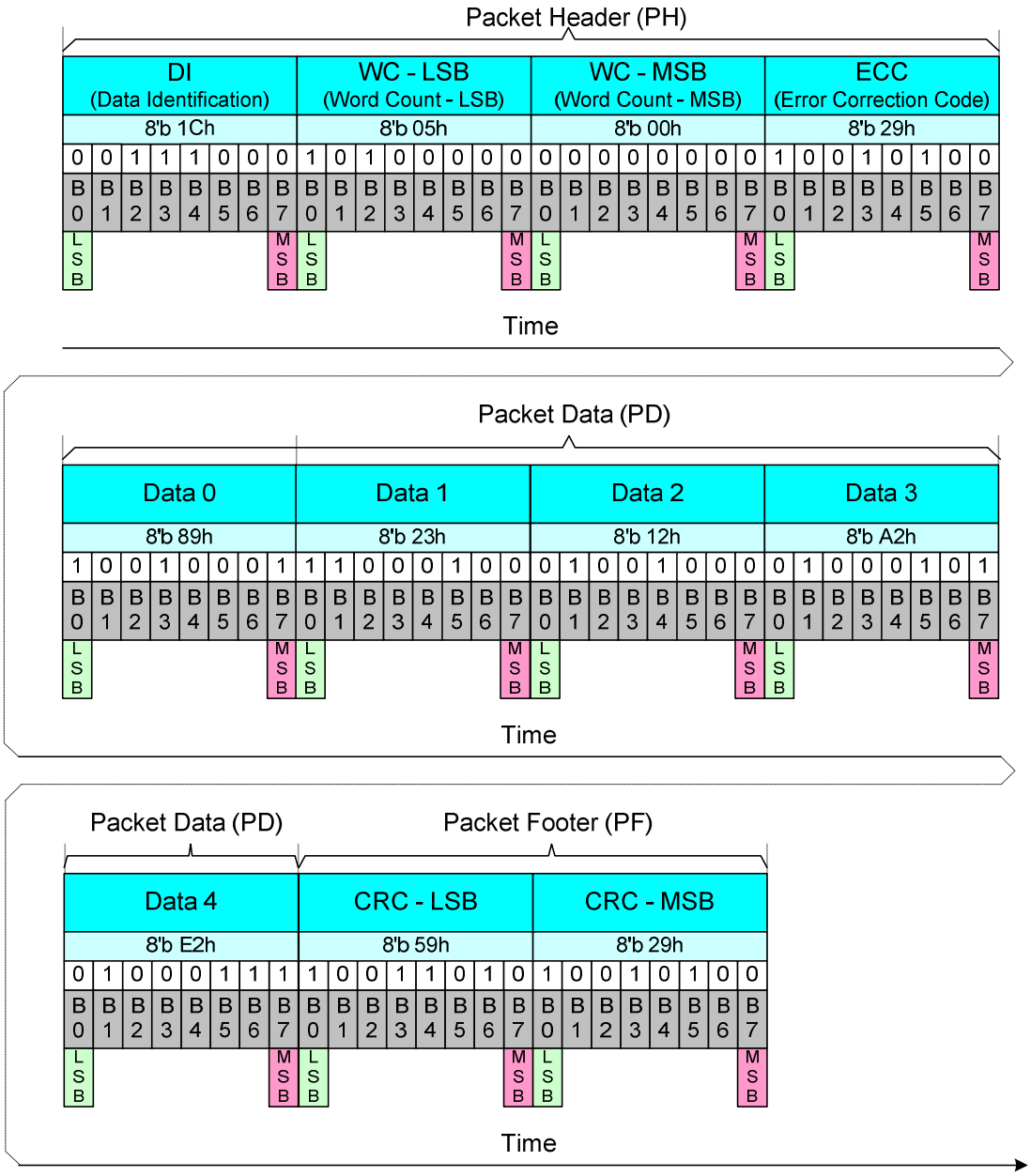

Figure 81: DCS Read Long Response (DCSRR-L) – Example

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4.6.3.2.2.4 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 10 0001b), from the display module to the MCU.

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 00hex (Always)
- Error Correction Code (ECC)

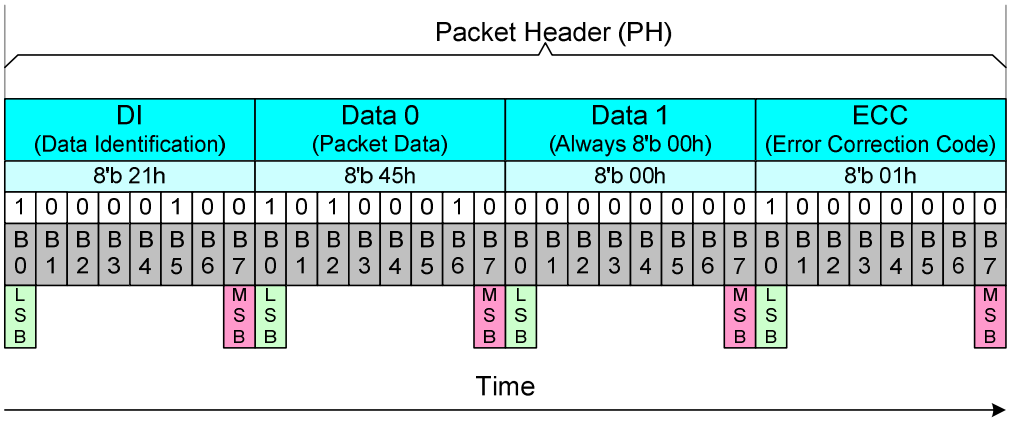

Figure 82: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) – Example

4.6.3.2.2.5 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 10 0010b), from the display module to the MCU.

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 32hex
- Error Correction Code (ECC)

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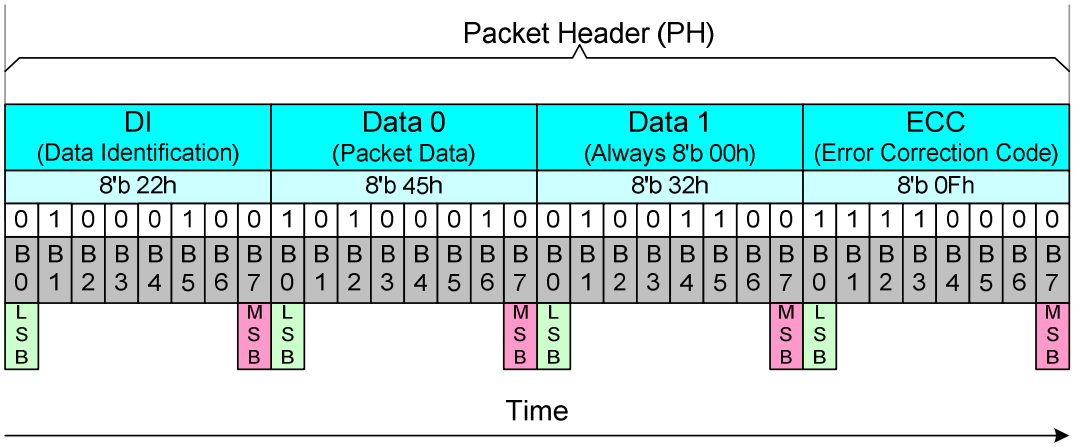

Figure 83: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) – Example

4.6.3.3. Communication Sequences

4.6.3.3.1. General

The communication sequences can be done on interface or packet levels between the MCU and the display module. This communication sequence description is for DSI data lanes (MIPI_DATA_P/N), and it is assumed that the needed low level communication is done on DSI clock lanes (MIPI_CLOCK_P/N) automatically. Functions of the interface level communication are described in the following table.

Table 20: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	TEE	Tearing Effect Event
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described in the following table.

Table 21: Packet Level Communication

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MCU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
Display Module (ILI9488)	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

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4.6.3.3.2. Sequence

4.6.3.3.2.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined in the chapter "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)", and examples of sequences on how this packet is used are described in the following tables.

Table 22: DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSW1-S	LPDT	➔	--	--	
3	--	LP-11	➔	--	--	End

Table 23: DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSW1-S	HSDT	➔	--	--	
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	End

Table 24: DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSW1-S	HSDT	➔	--	--	
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error ➔ Go to Line 8 If Error Occurs ➔ Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	➔	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	

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15	--	BTA	⇔	BTA	--	
16	--	LP-11	➔	--	--	End

4.6.3.3.2.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined in the chapter "Display Command Set Write, no Parameter (DCSWN-S)", and examples of sequences on how this packet is used are described in the following tables.

Table 25: DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSWN-S	LPDT	➔	--	--	
3	--	LP-11	➔	--	--	End

Table 26: DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSWN-S	HSDT	➔	--	--	
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	End

Table 27: DCS Write, No Parameter Sequence – Example 3

DCS Write, No Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSWN-S	HSDT	➔	--	--	
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	➔	LP-11	--	If No Error ➔ Go to Line 8 If Error Occurs ➔ Go to Line 13
7						
8	--	--	➔	ACK	--	No Error
9	--	--	➔	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	➔	--	--	End

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12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.6.3.3.2.3. DCS Write Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined in the chapter "Display Command Set Write Long (DCSW-L)", and examples of sequences on how this packet is used are described in the following tables.

Table 28: DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 29: DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 30: DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error

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9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

Table 31: DCS Write Long Sequence – Example 4

DCS Write Long Sequence – Example 4						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	Memory Write (2Ch)
3	DCSW-L	HSDT	→	--	--	Memory Write Continue (3Ch)
4	DCSW-L	HSDT	→	--	--	Memory Write Continue (3Ch)
5	DCSW1-S	HSDT	→	--	--	Memory Write Continue (3Ch) with 1 Parameter
6	EoTP	HSDT	→	--	--	End of Transmission Packet
7	--	LP-11	→	--	--	End

Note: This is an example that image data are sent in 4 packets.

4.6.3.3.2.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined in the chapter "Display Command Set Read, No Parameter (DCSRN-S)", and examples of sequences on how this packet is used are described in the following tables.

Table 32: DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						

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9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

Table 33: DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response "Memory Read" (2Eh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)

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21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

4.6.3.3.2.5. Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined in the chapter "Null Packet, No Data (NP-L)" and an example of the sequence on how this packet is used is described in the following table.

Table 34: Null Packet, No Data Sequence -- Example

Null Packet, No Data Sequence – Example						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.6.3.3.2.6. End of Transmission Packet

A Short Packet (SPa) of "End of Transmission (EoTP)" is defined in the chapter "End of Transmission Packet (EoTP)" and an example of the sequence on how this packet is used is described in the following table.

Table 35: End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MCU		Information Direction	Display Module (ILI9488)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

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4.6.3.4. 16 Bit/Pixel Writing

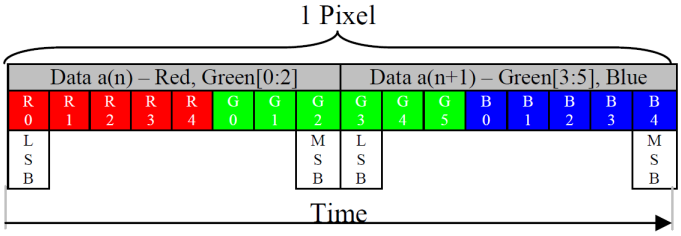

Figure 84: One Pixel Bit and Write Color Orders

The MCU can send the following packet to the display module.

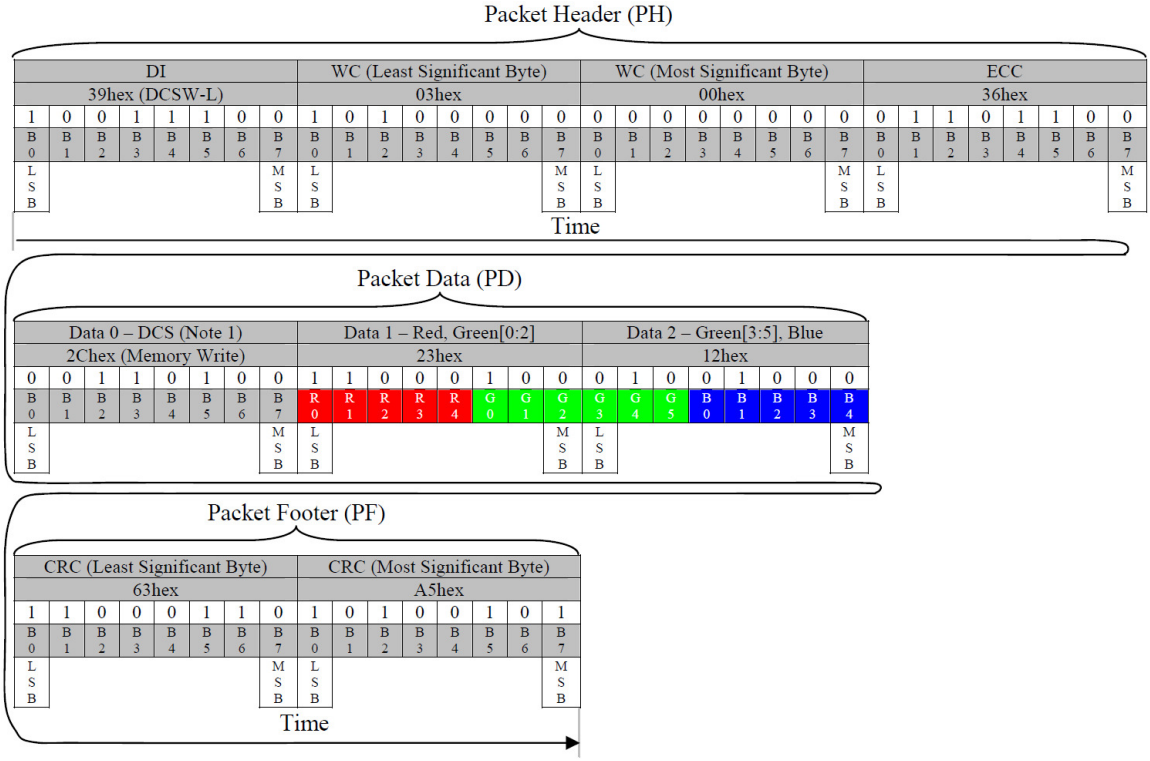

Figure 85: One Pixel Write (DCSW-L) – Example 1

Notes:

1. DCS (Data 0) can be Memory Write (2Ch) or Memory Write Continue (3Ch) command.
2. It is possible that one pixel information is split into different packets, which ends and starts as follows: RG – GB (2 packets).
3. A packet can include several pixels (not just one pixel as in this example).

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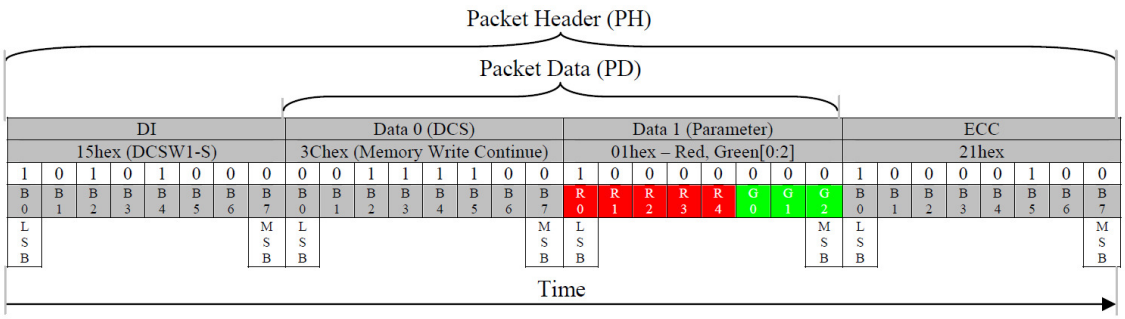

Figure 86: Red/Green [0:2] Sub-pixel Write (DCSW1-S) – Example 2

Note: DCS (Data 0) can also be “Memory Write” (2Ch) command.

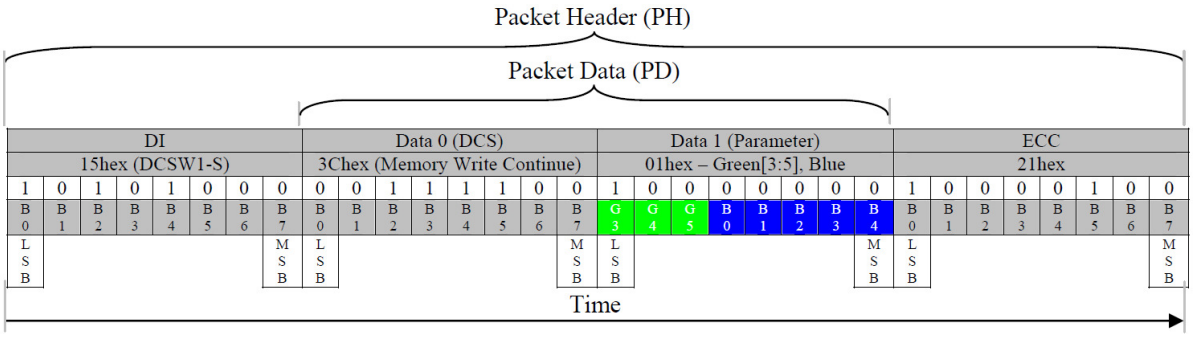

Figure 87: Green [3:5]/Blue Sub-pixel Write (DCSW1-S) – Example 3

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch).
2. Previous data byte is R [0:4] G [0:2].

4.6.3.5. 24 Bit/Pixel Writing

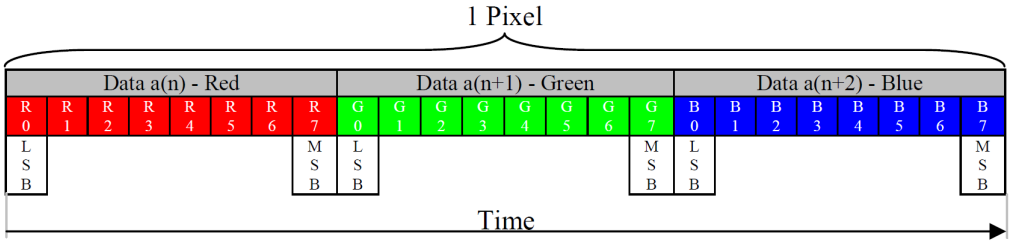

Figure 88: One Pixel Bit and Color Write Orders

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The MCU can send the following packet to the display module.

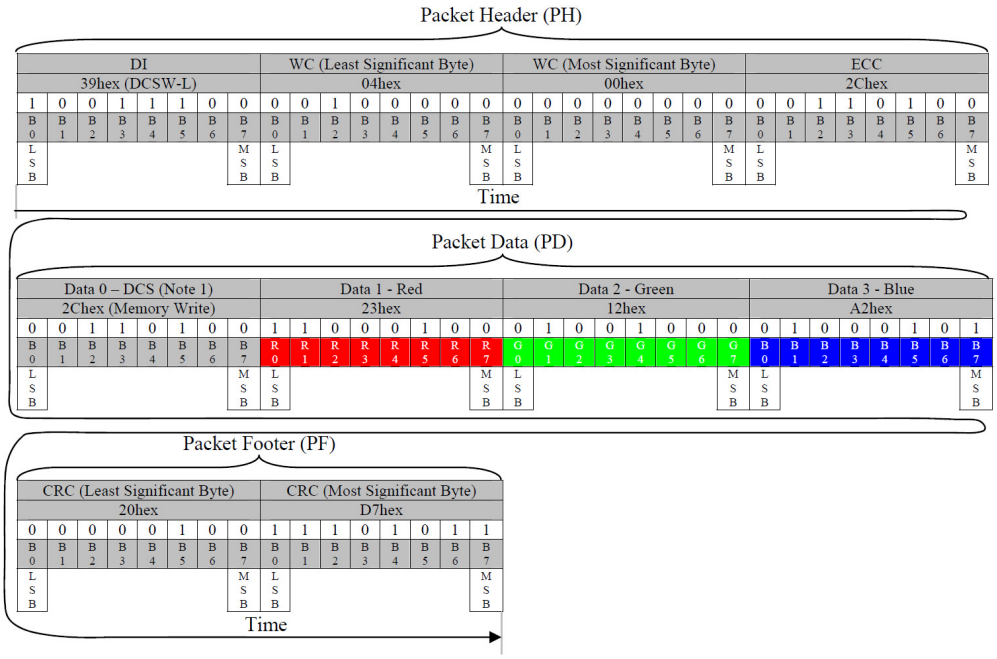

Figure 89: One Pixel Write (DCSW-L) – Example 1

Notes:

1. DCS (Data 0) can be Memory Write (2Ch) or Memory Write Continue (3Ch) command.
2. It is possible that one pixel information is split into two or three different packets which end and start as follows:
   - R – GB (2 packets)
   - RG – B (2 packets)
   - R – G – B (3 packets)
3. A packet can include several pixels (not just one pixel as in this example).

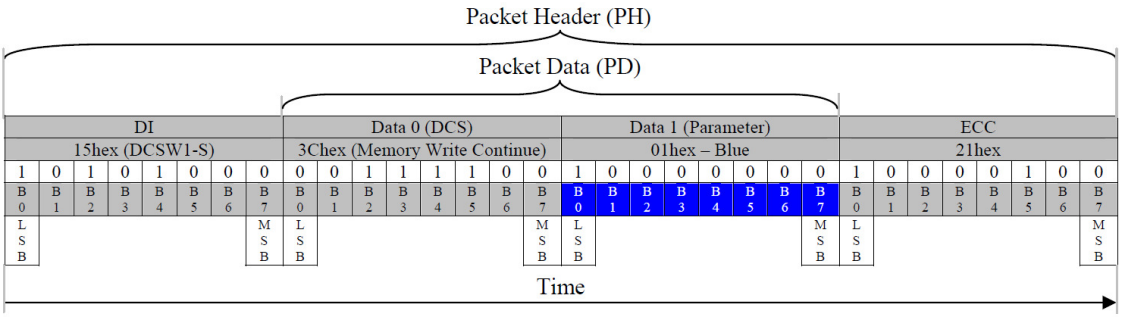

Figure 90: Blue Sub-pixel Write (DCSW1-S) – Example 2

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch).
2. Previous data byte is G [0:7].

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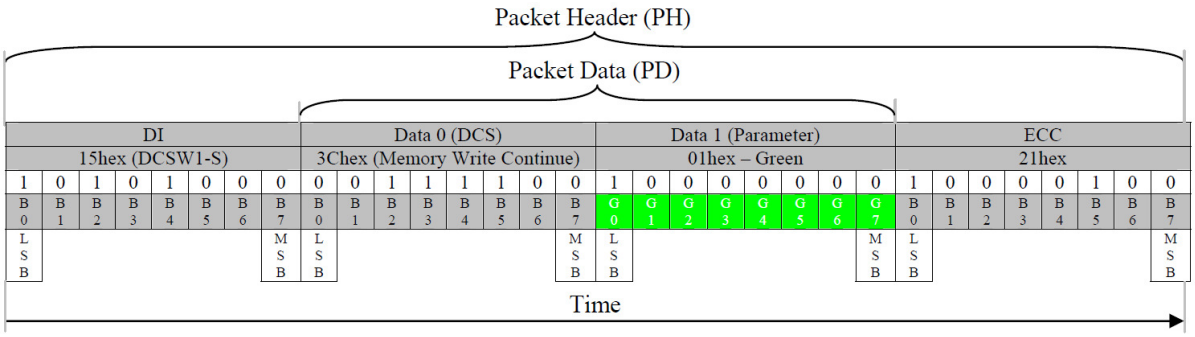

Figure 91: Green Sub-pixel Write (DCSW1-S) – Example 3

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch).
2. Previous data byte is R [0:7].

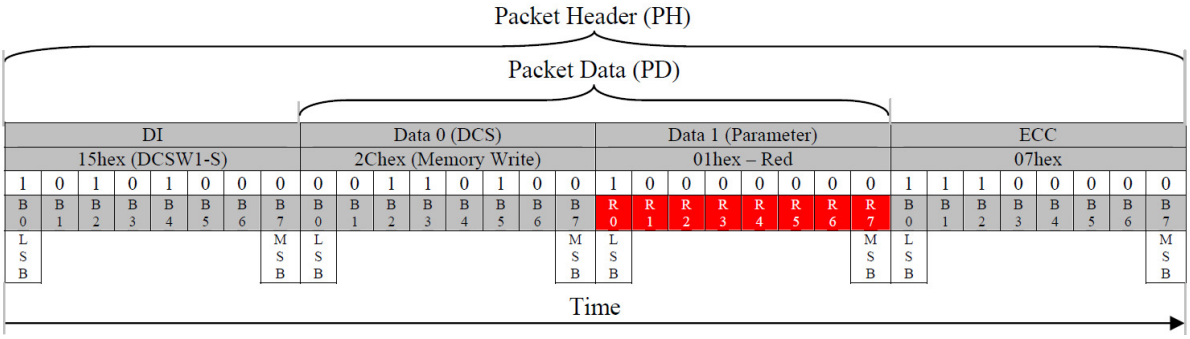

Figure 92: Red Sub-pixel Write (DCSW1-S) – Example 4

Notes:

1. DCS (Data 0) can also be “Memory Write Continue” (3Ch) command.
2. Previous data byte is B [0:7].

4.6.3.5.1. 24 Bit/Pixel Reading

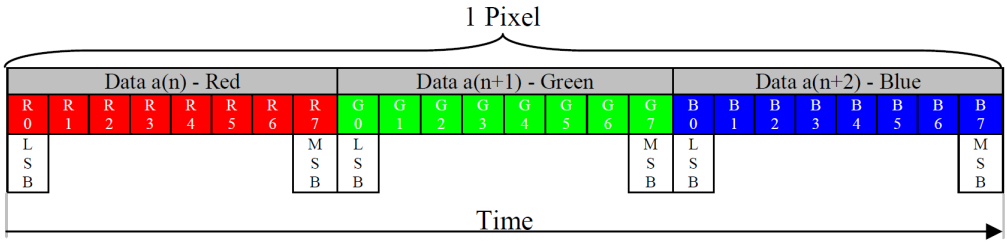

Figure 93: One Pixel Bit and Color Read Order

The display module can send following packets to the MCU after the MCU has sent a read command “Memory Read (2Eh)” or “Memory Read Continue (3Eh)”.

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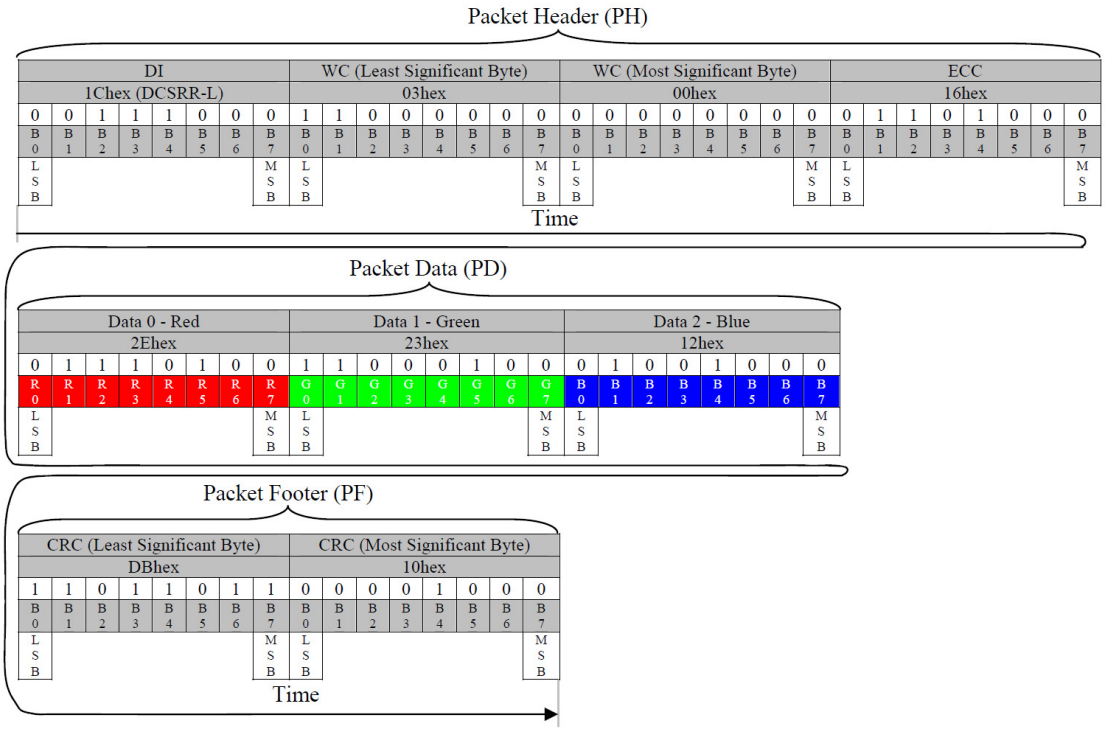

Figure 94: One Pixel Read Response (DCSRR-L) – Example 1

Note: It is possible that one pixel information is split into two or three different packets:

- R – GB (2 packets)
- RG – B (2 packets)
- R – G – B (3 packets)

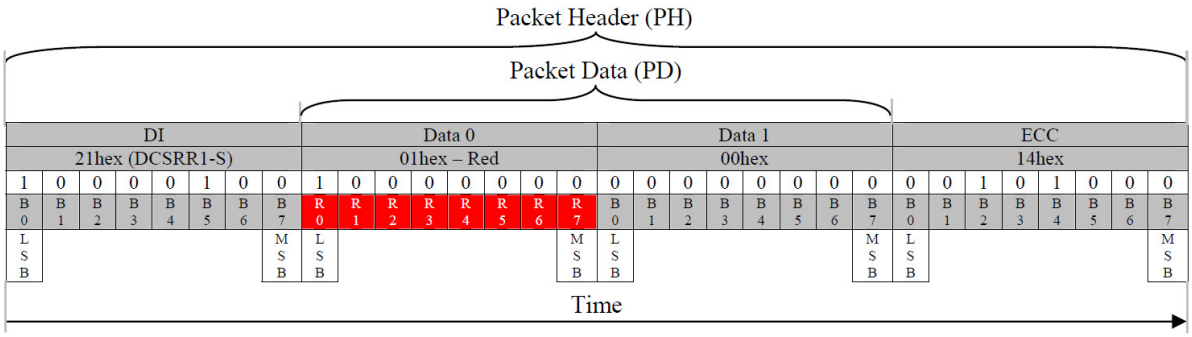

Figure 95: Red Sub-pixel Response (DCSRR1-S) – Example 2

Notes:

1. Data 1 is always 00h.
2. Previous data byte is B [0:7].

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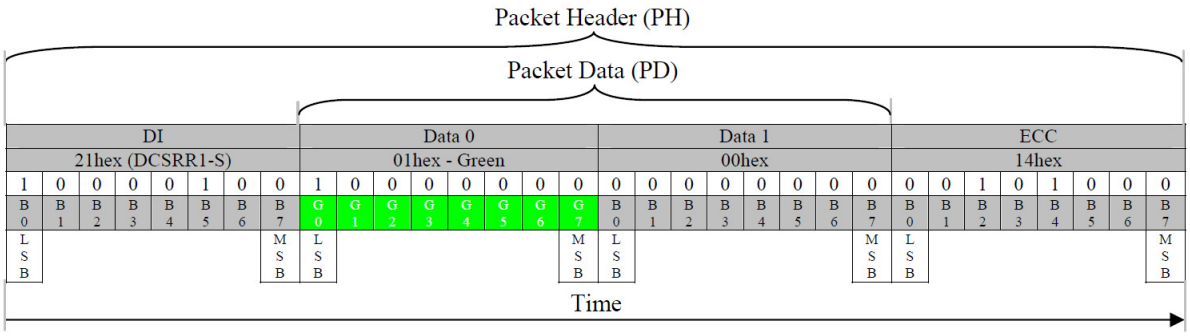

Figure 96: Green Sub-pixel Response (DCSRR1-S) – Example 3

Notes:

1. Data 1 is always 00h.
2. Previous data byte is R [0:7].

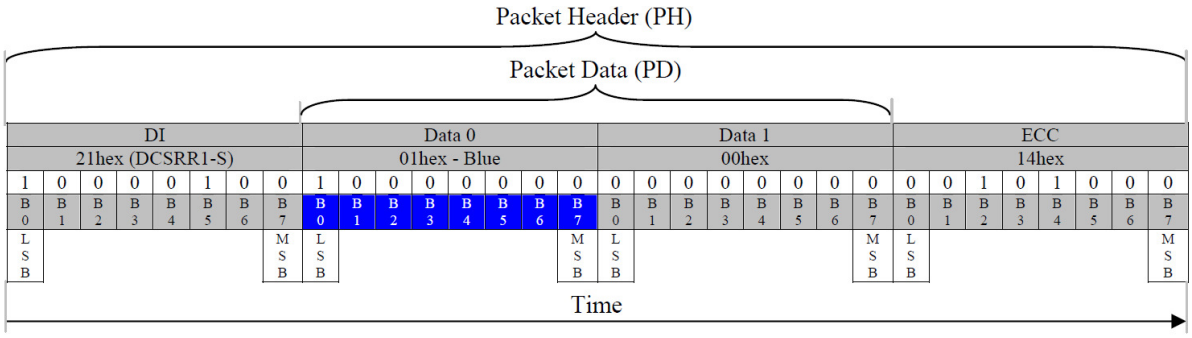

Figure 97: Blue Sub-pixel Response (DCSRR1-S) – Example 4

Notes:

1. Data 1 is always 00h.
2. Previous data byte is G [0:7].

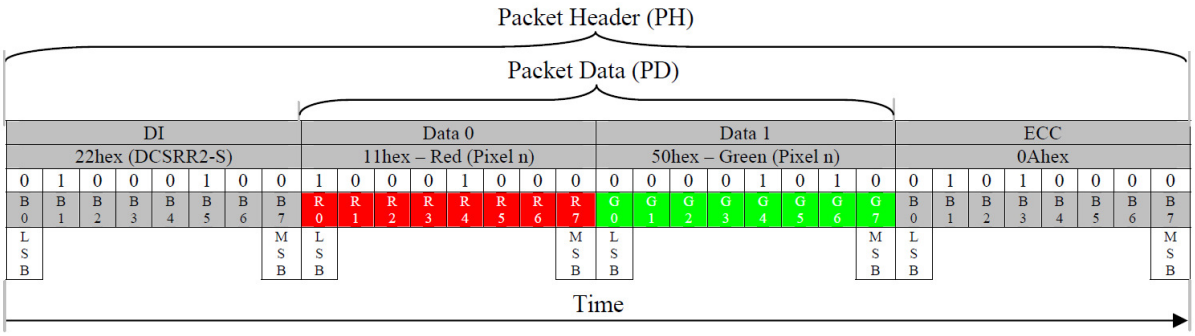

Figure 98: Red and Green Sub-pixels Response (DCSRR2-S) – Example 5

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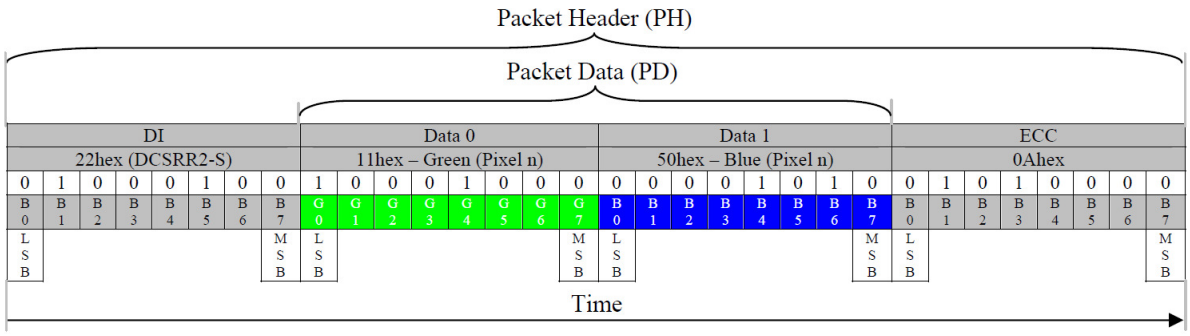

Figure 99: Green and Blue Sub-pixels Response (DCSRR2-S) – Example 6

Note: Previous data byte is R [0:7].

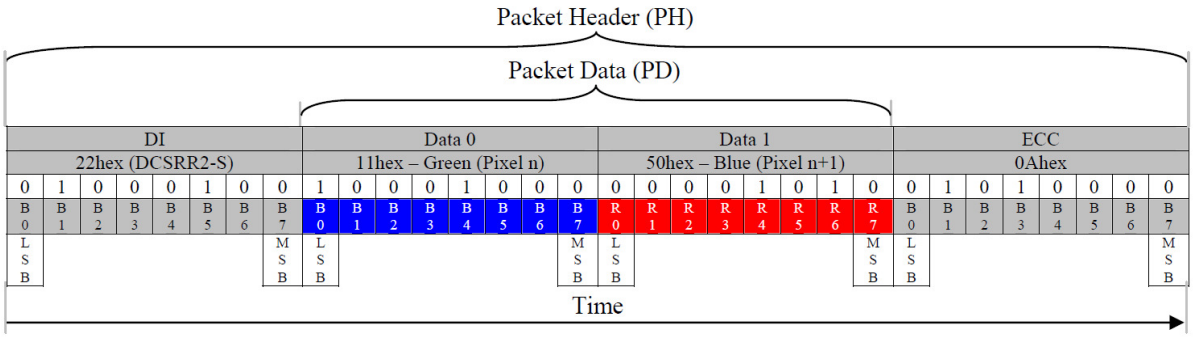

Figure 100: Blue and Red Sub-pixels Response (DCSRR2-S) – Example 7

Note: Previous data byte is G [0:7].

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4.7. Display Data Format

4.7.1. DBI Type C Option 1 (3-Line Serial Interface)

The 3-line/9-bit serial bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 101. Figure 101 describes an interface with 8080 MCU system interface.

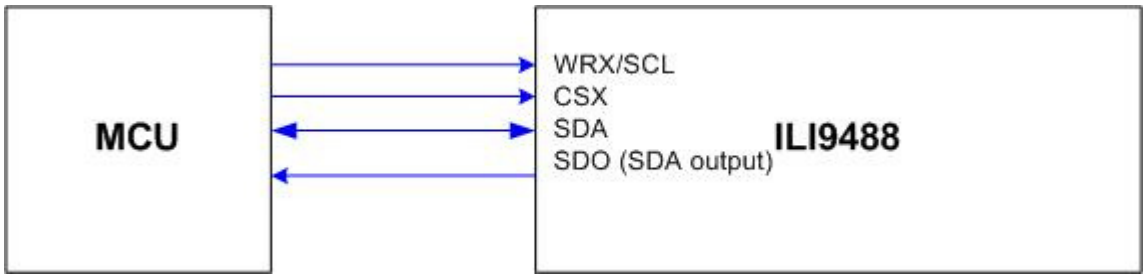

Figure 101: 3-Line Serial Interface

The available display data formats are:

- 8 colors, RGB 1, 1, 1 bits input (set Standard Command 3Ah, DBI [2:0] as 001)
- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.1.1. SPI Data for 3-bit/pixel (RGB 1-1-1 Bits Input), 8-color

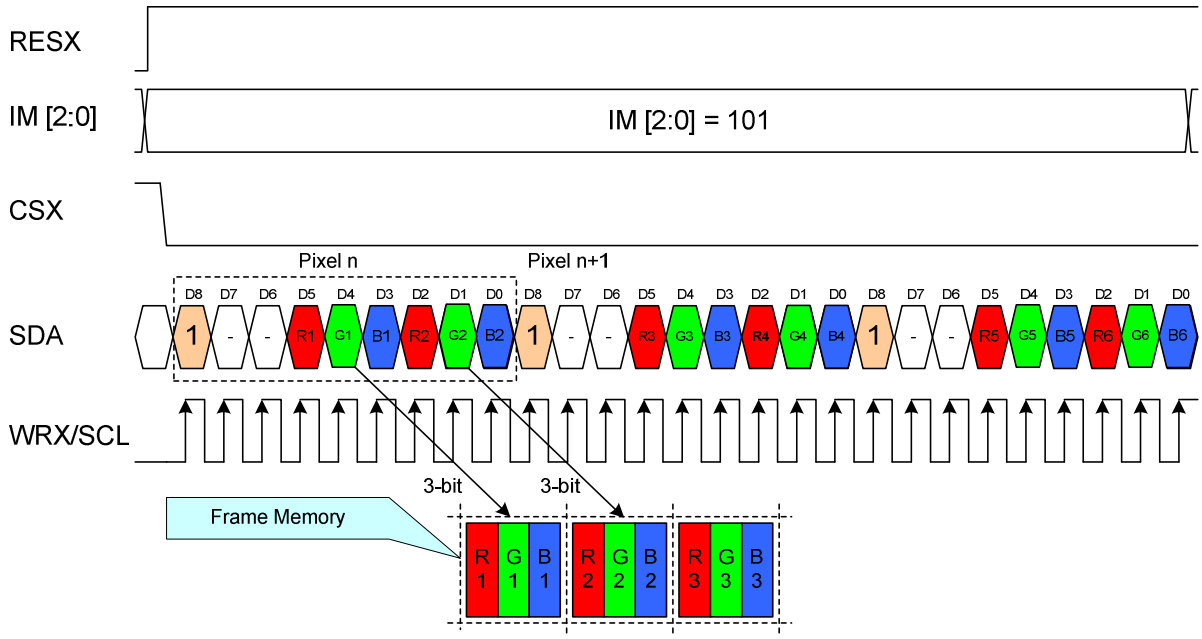

Figure 102: SPI Data for 3 bit/pixel (RGB 1-1-1 Bits Input), 8-color

Notes:

1. One pixel data contains 3-bit color depth information.
2. '-' = void

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4.7.1.2. SPI Data for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

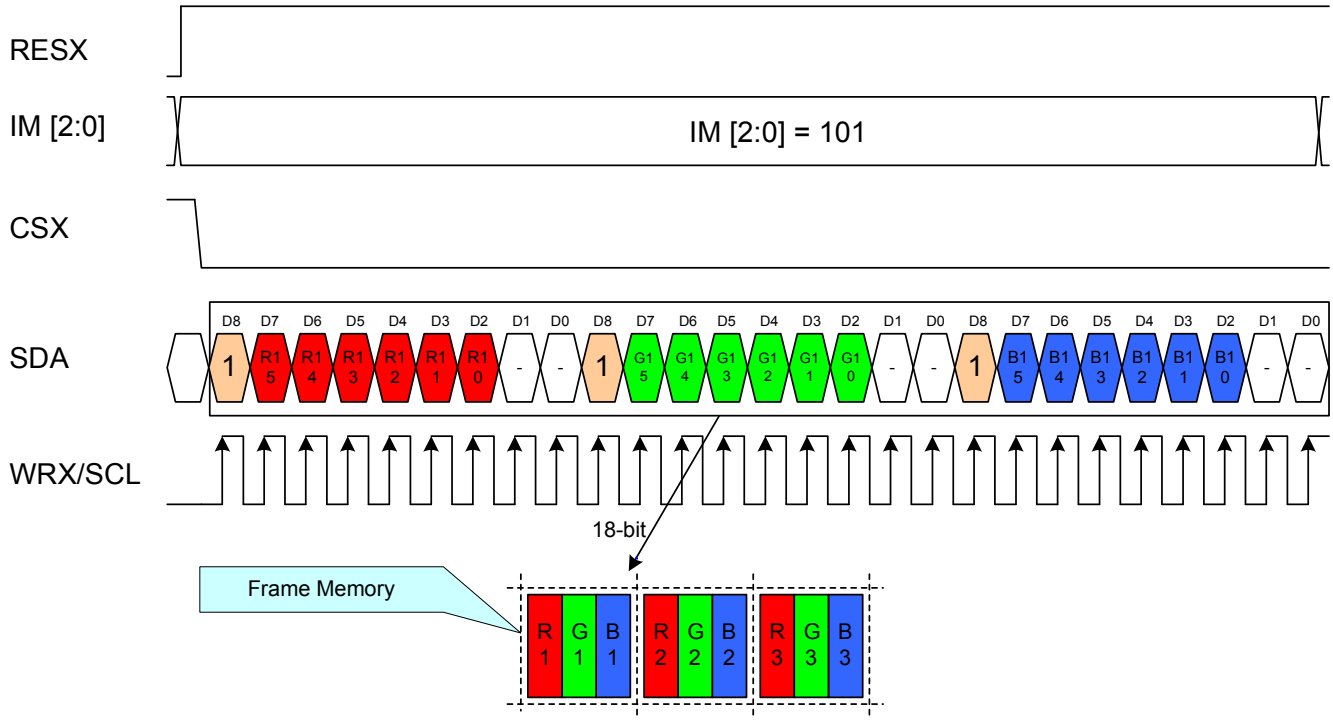

Figure 103: SPI Data for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. One pixel data contains 18-bit color depth information.
2. The most significant bits are: R x 5, G x 5, and B x 5.
3. The least significant bits are: R x 0, G x 0, and B x 0.
4. '-' = void

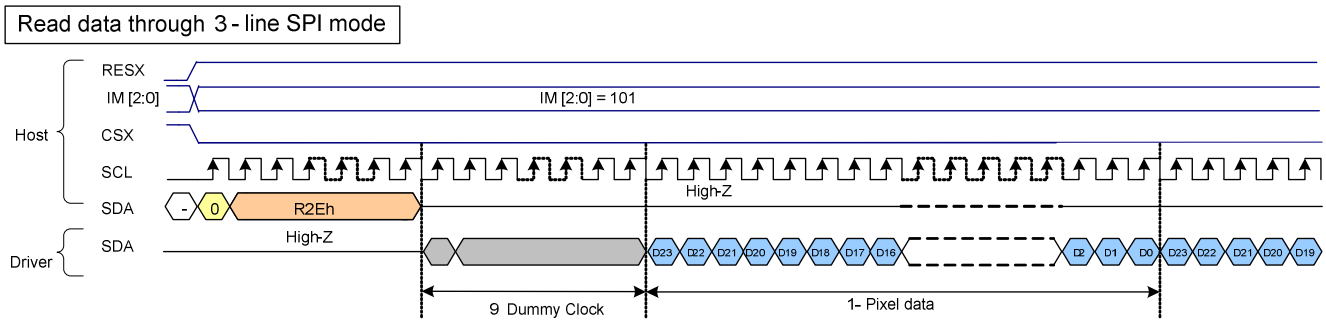

Figure 104: 3-Line SPI Mode Read Data

Note: '-' = void

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4.7.2. DBI Type-C Option 3 (4-Line Serial Interface)

The 4-line/8-bit serial bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 111. Figure 105 describes an interface with 8080 MCU system interface.

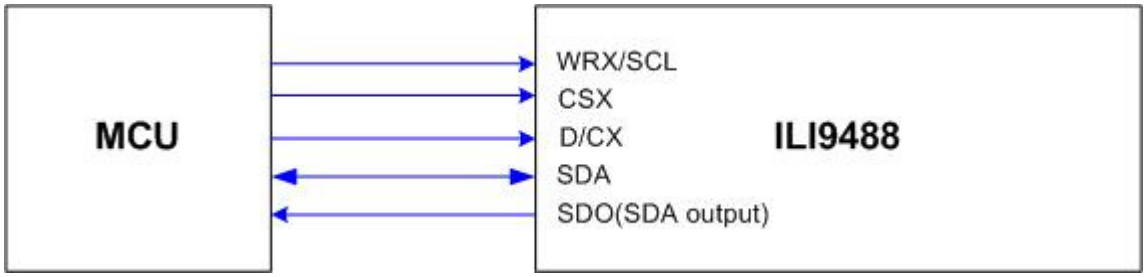

Figure 105: 4-Line Serial Interface

The available display data formats are:

- 8 colors, RGB 1, 1, 1 bits input (set Standard Command 3Ah, DBI [2:0] as 001)
- 65K-Colors, RGB 5, 6, 5 bits input data (set Standard Command 3Ah, DBI [2:0] as 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.2.1. SPI Data for 3-bit/pixel (RGB 1-1-1 Bits Input), 8-color

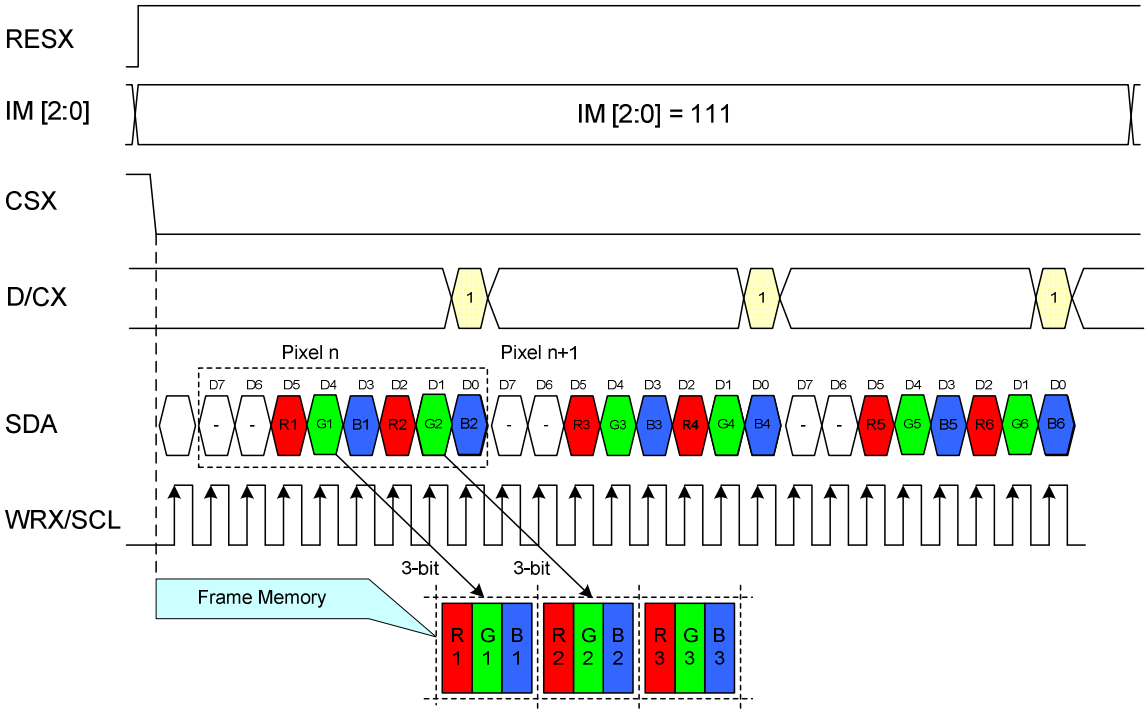

Figure 106: SPI Data for 3-bit/pixel (RGB 1-1-1 Bits Input), 8-color

Notes:

1. One pixel data contains 3-bit color depth information.
2. '-' = void

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4.7.2.2. SPI Data for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

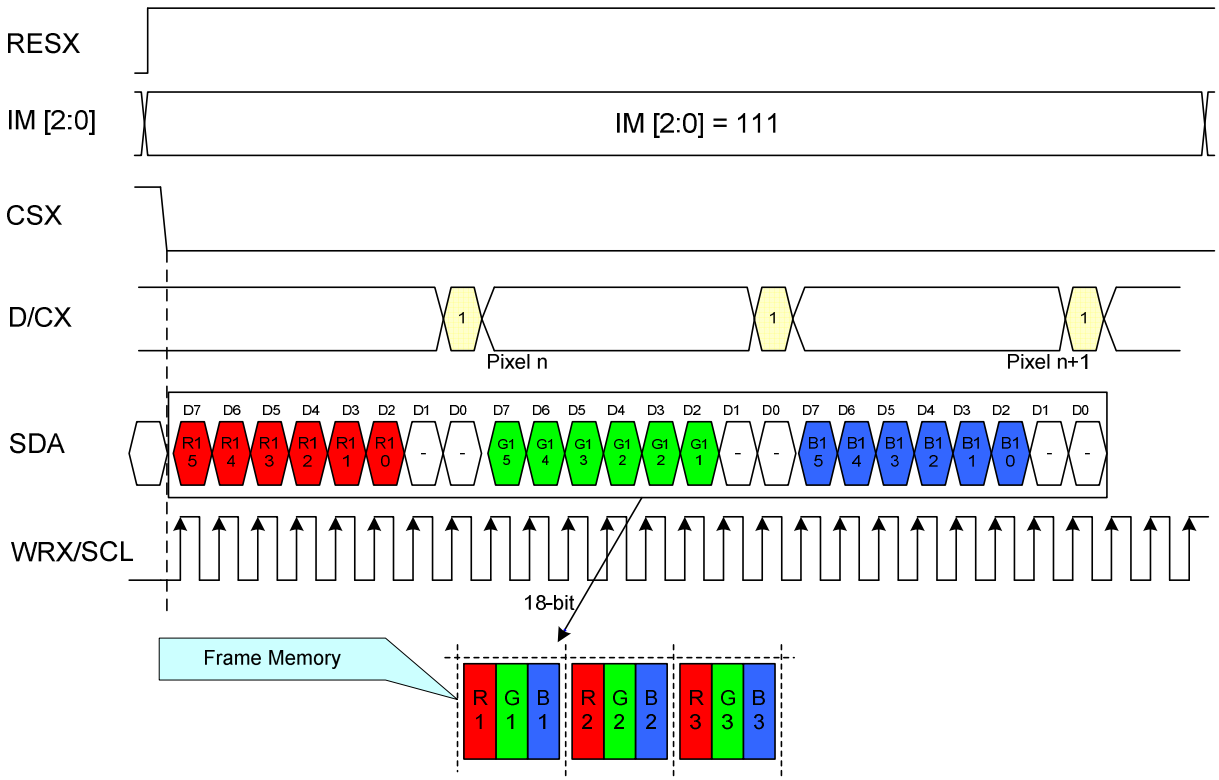

Figure 107: SPI Data for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. One pixel data contains 18-bit color depth information.
2. The most significant bits are: R x 5, G x 5, and B x 5.
3. The least significant bits are: R x 0, G x 0, and B x 0.
4. '-' = void

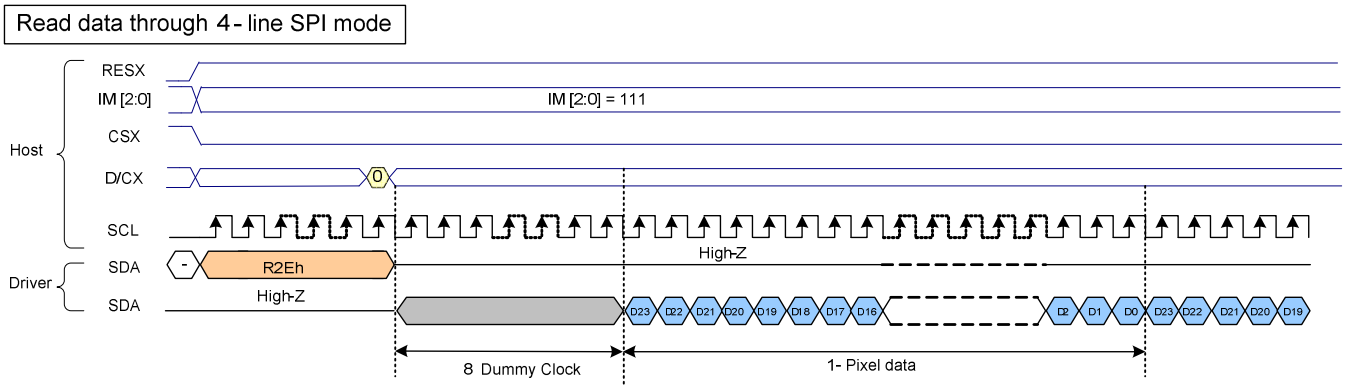

Figure 108: 4-Line SPI Mode Read Data

Note: '-' = Leave these pins open.

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4.7.3. 8-bit Parallel MCU Interface

The DBI TYPE B 8-bit parallel bus interface of the ILI9488 is used by setting the external pin IM [2:0] as 011. Figure 109 shows this system interface.

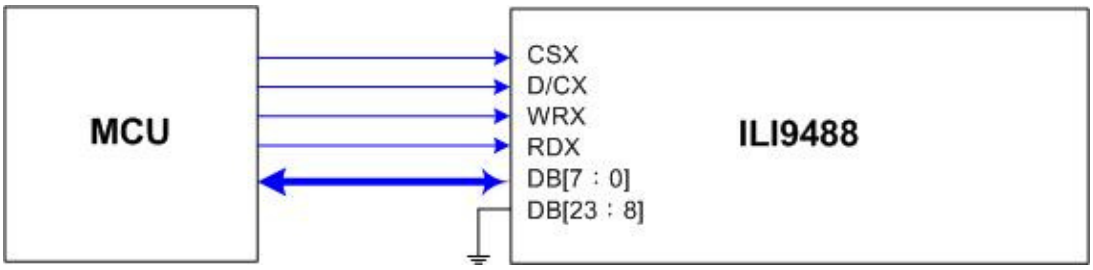

Figure 109: 8-bit Parallel MCU Interface

The available display data formats are:

- 65K-Colors, RGB 5, 6, 5 bits input data (set Standard Command 3Ah, DBI [2:0] as 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.3.1. 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

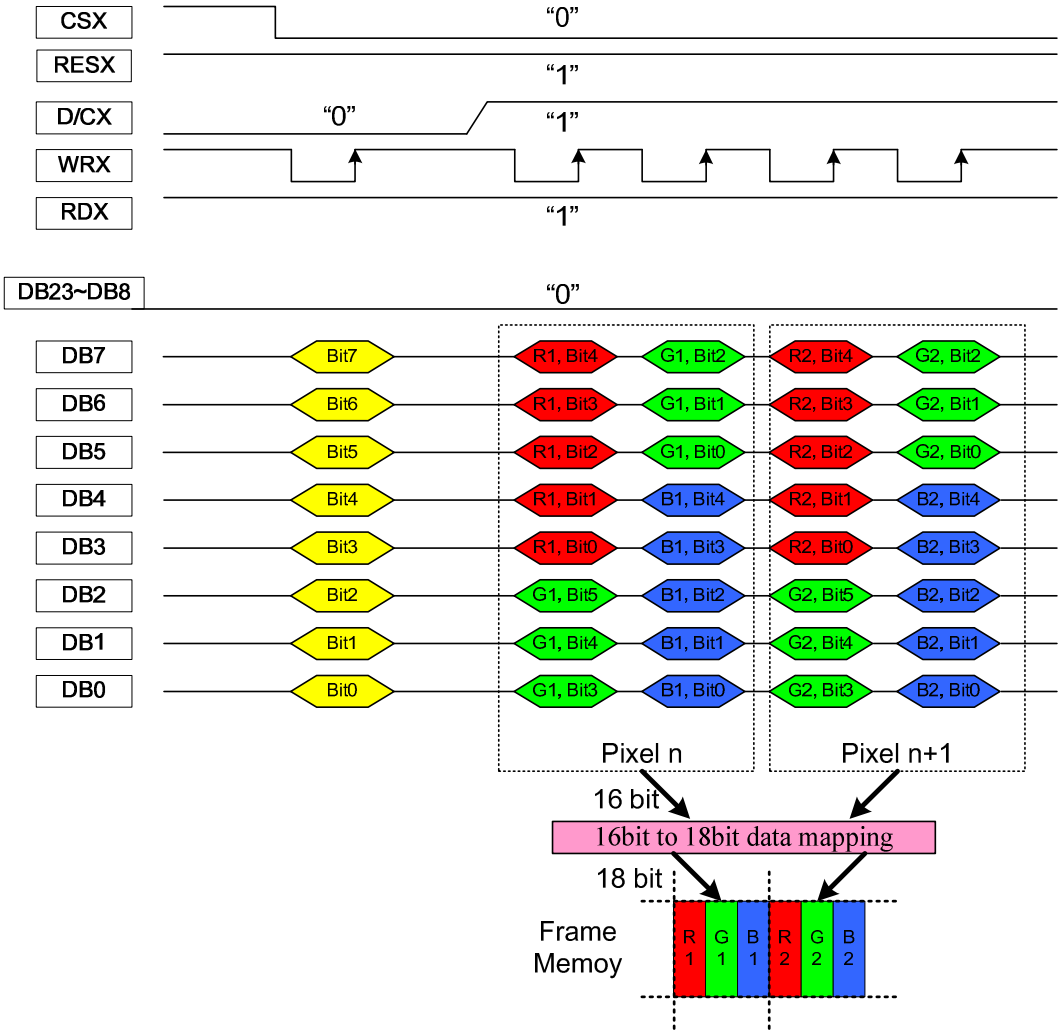

Figure 110: 8-bit Data Bus for 16-bit/pixel (RGB 6-5-6 Bits Input), 65K-color

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Notes:

1. The data order is as follows: MSB = DB7, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green data, and MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 2-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

4.7.3.2. 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

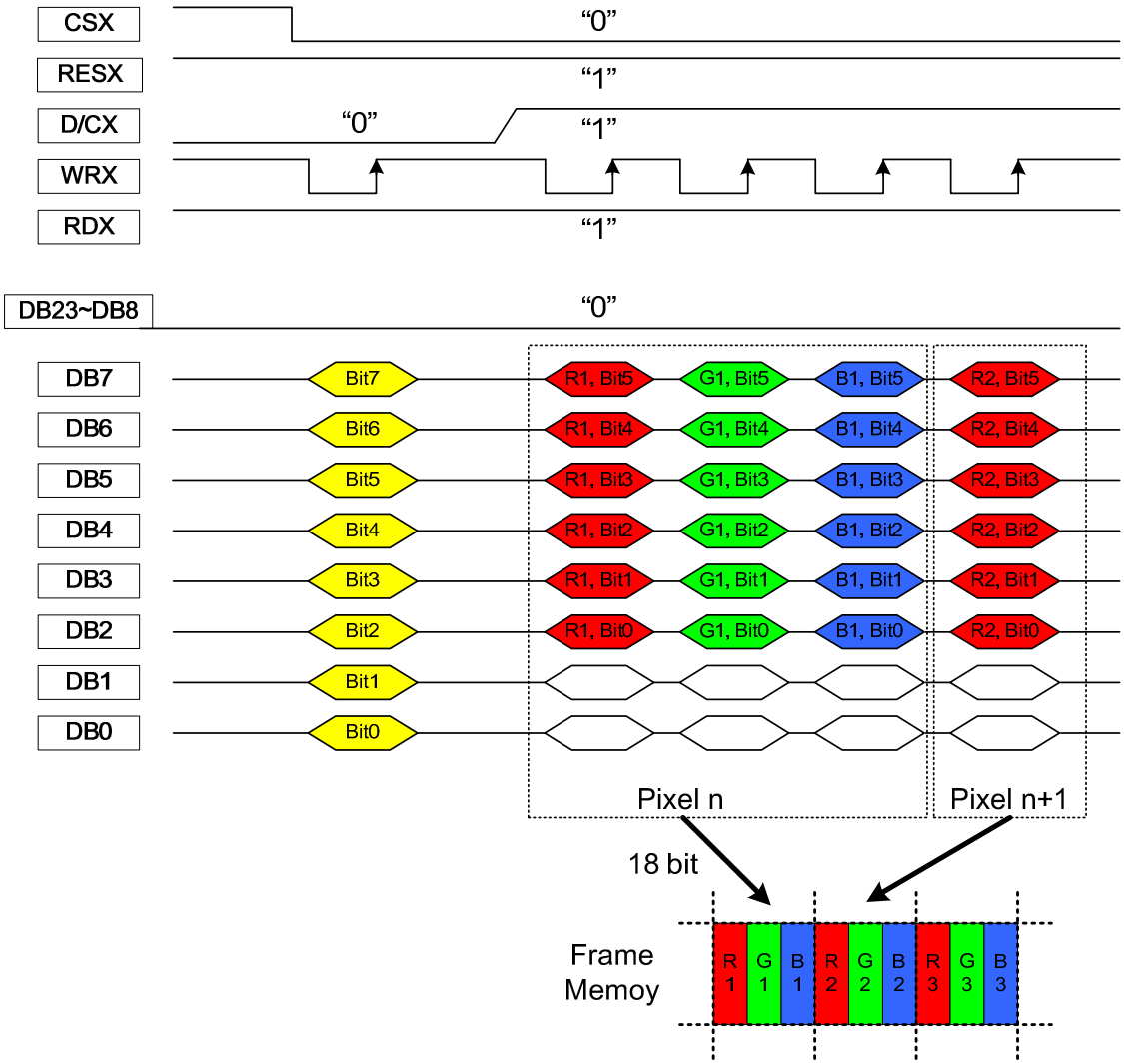

Figure 111: 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB = DB7, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. '-' = void

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4.7.4. 9-bit Parallel MCU Interface

The DBI TYPE B 9-bit parallel bus interface of the ILI9488 is used by setting the external pin IM [2:0] as 001. Figure 112 shows this system interface.

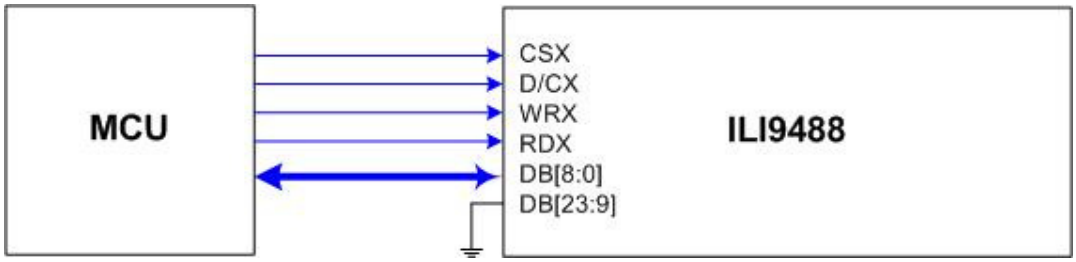

Figure 112: 9-bit Parallel MCU Interface

The available display data format is:

- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

4.7.4.1. 9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

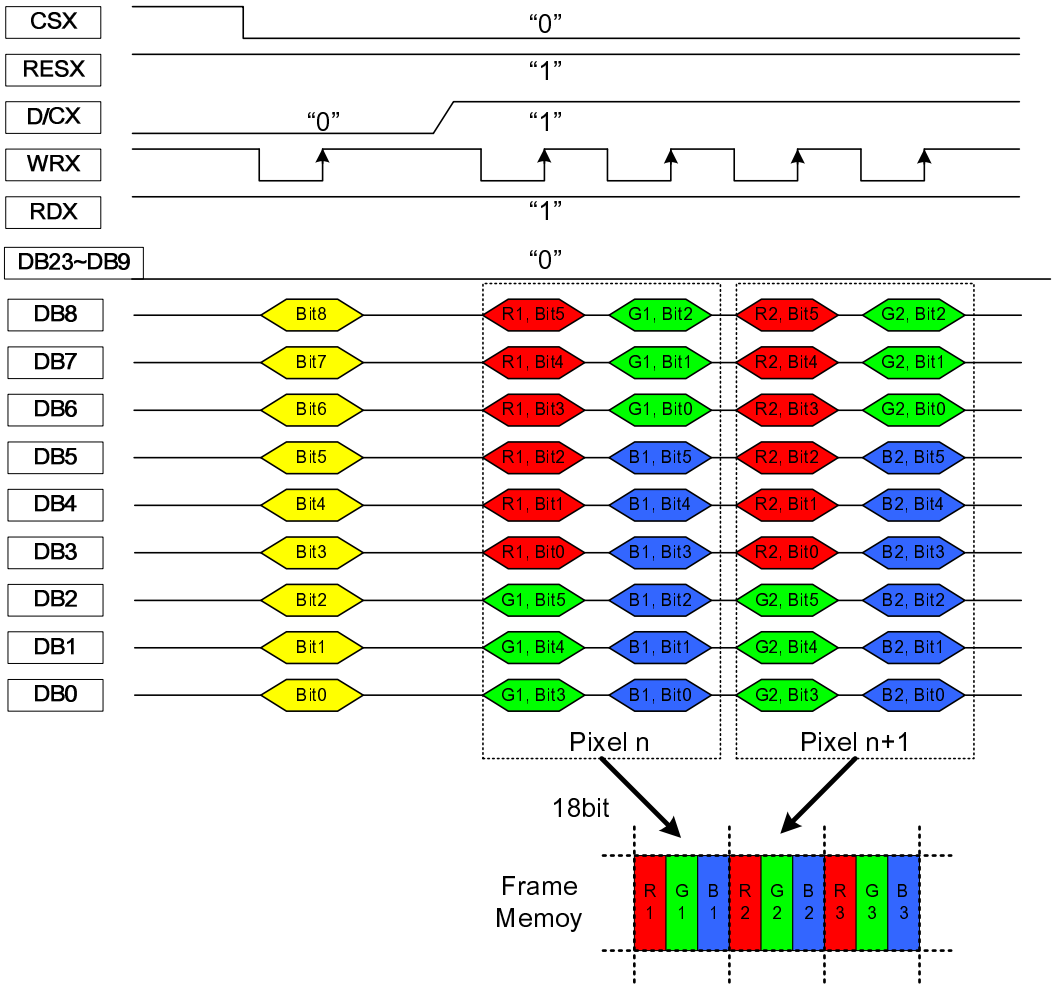

Figure 113: 9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB= DB8, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red

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and Blue data.

2. 2-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. '-' = void

4.7.5. 16-bit Parallel MCU Interface

The 8080-system 16-bit parallel bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 010. Figure 114 shows this system interface.

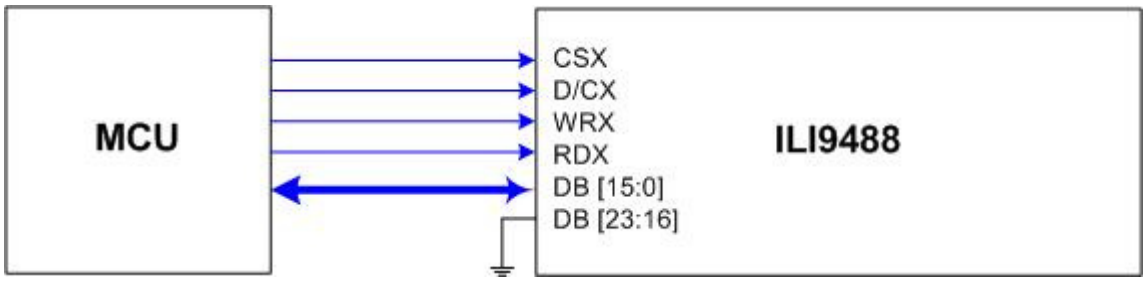

Figure 114: 16-bit Parallel MCU Interface

The available display data formats are:

- 65K-Colors, RGB 5, 6, 5 bits input data (set Standard Command 3Ah, DBI [2:0] as 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (set Standard Command 3Ah, DBI [2:0] as 110)

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4.7.5.1. 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

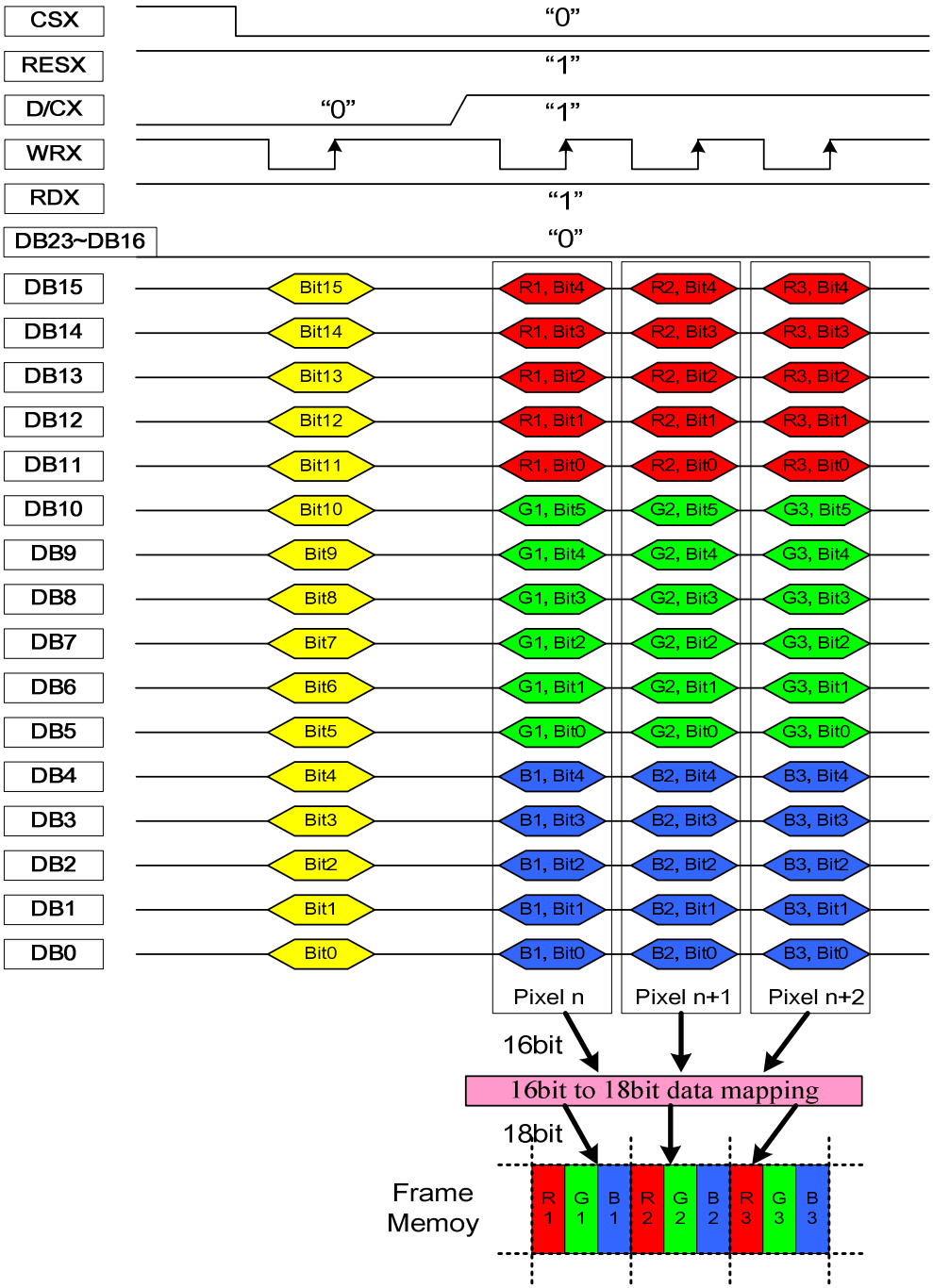

Figure 115: 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green data, and MSB = Bit 4, LSB = Bit0 for Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

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4.7.5.2. 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

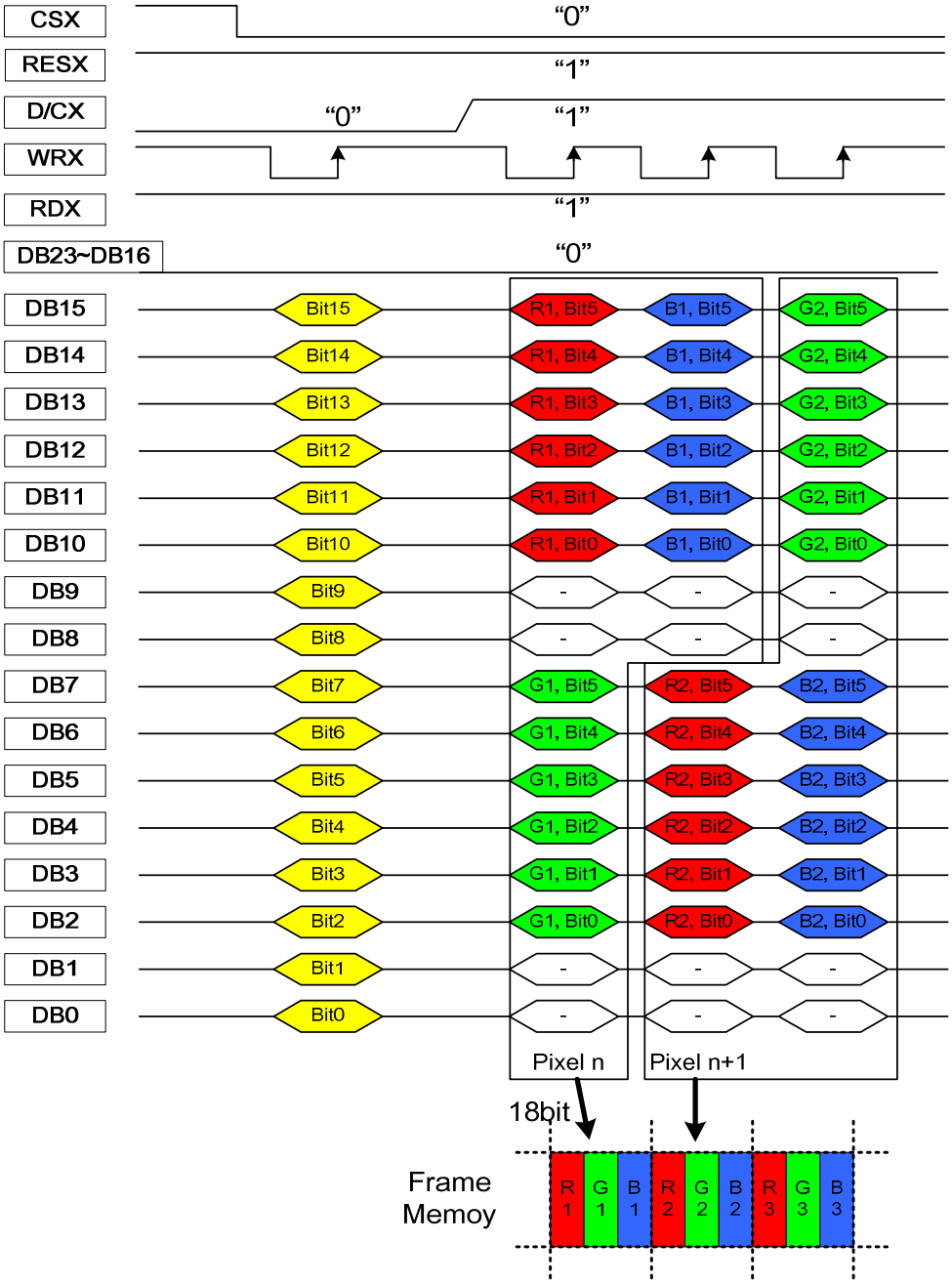

Figure 116: 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 2 pixel data to the 18-bit color depth information.
3. '-' = void

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4.7.6. 18-bit Parallel MCU Interface

The 8080-system 18-bit parallel bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 000. Figure 117 shows this system interface.

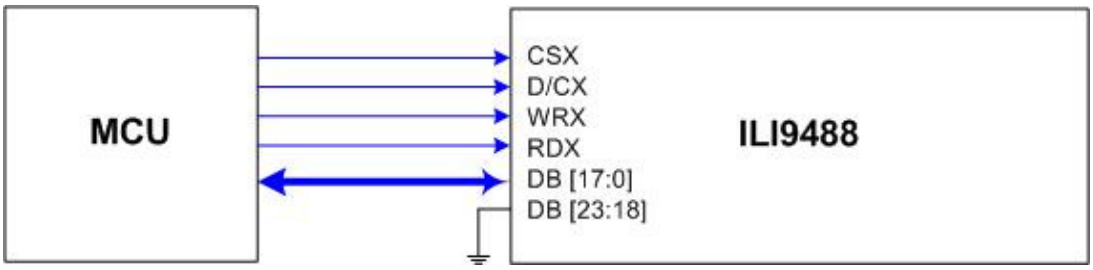

Figure 117: 18-bit Parallel MCU Interface

The available display data format is:

- 262K-Colors, RGB 6, 6, 6 -bits input data (set Standard Command 3Ah, DBI [2:0] = 110)

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4.7.6.1. 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

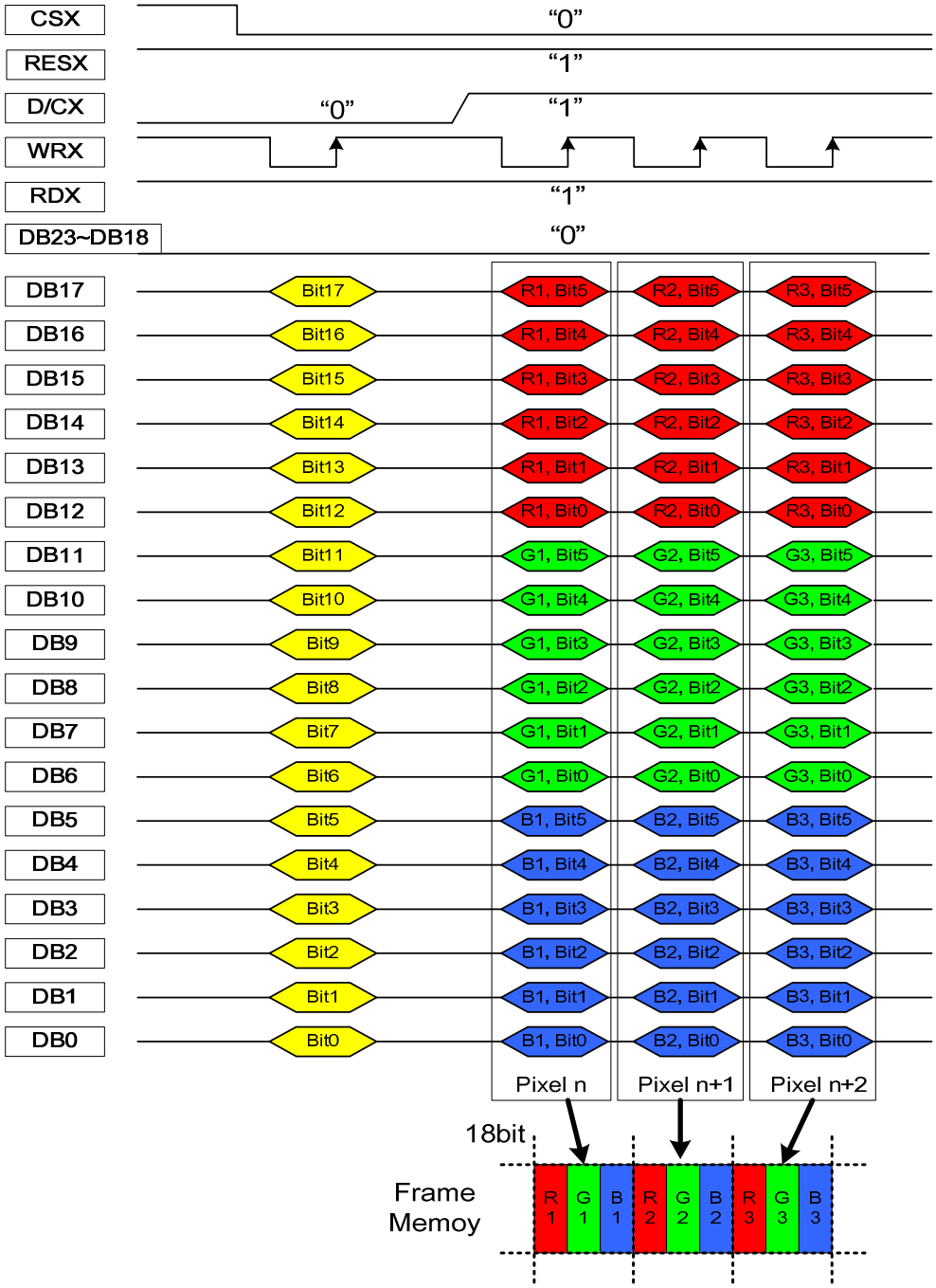

Figure 118: 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB = DB17, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 18-bit color depth information.

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4.7.7. 24-bit Parallel MCU Interface

The 8080-system 24-bit parallel bus interface of the ILI9488 can be used by setting external pin IM [2:0] as 000 and register setting DB_EN as 1. Figure 119 shows this system interface.

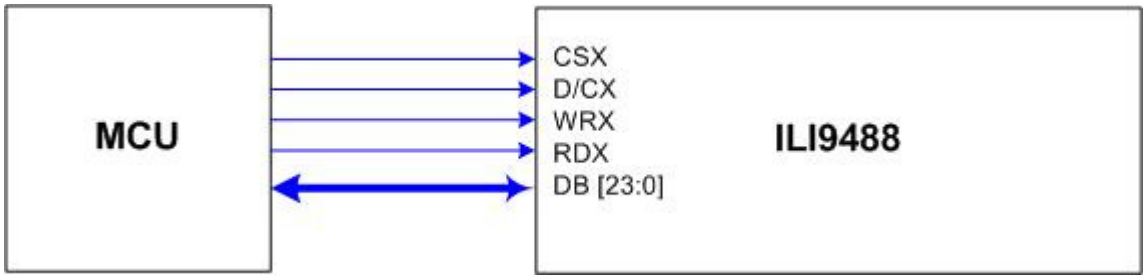

Figure 119: 24-bit Parallel MCU Interface

The available display data format is:

- 262K-Colors, RGB 8, 8, 8 -bits input data (set Standard Command 3Ah, DBI [2:0] = 111)

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4.7.7.1. 24-bit Data Bus for 24-bit/pixel (RGB 8-8-8 Bits Input), 262K-color

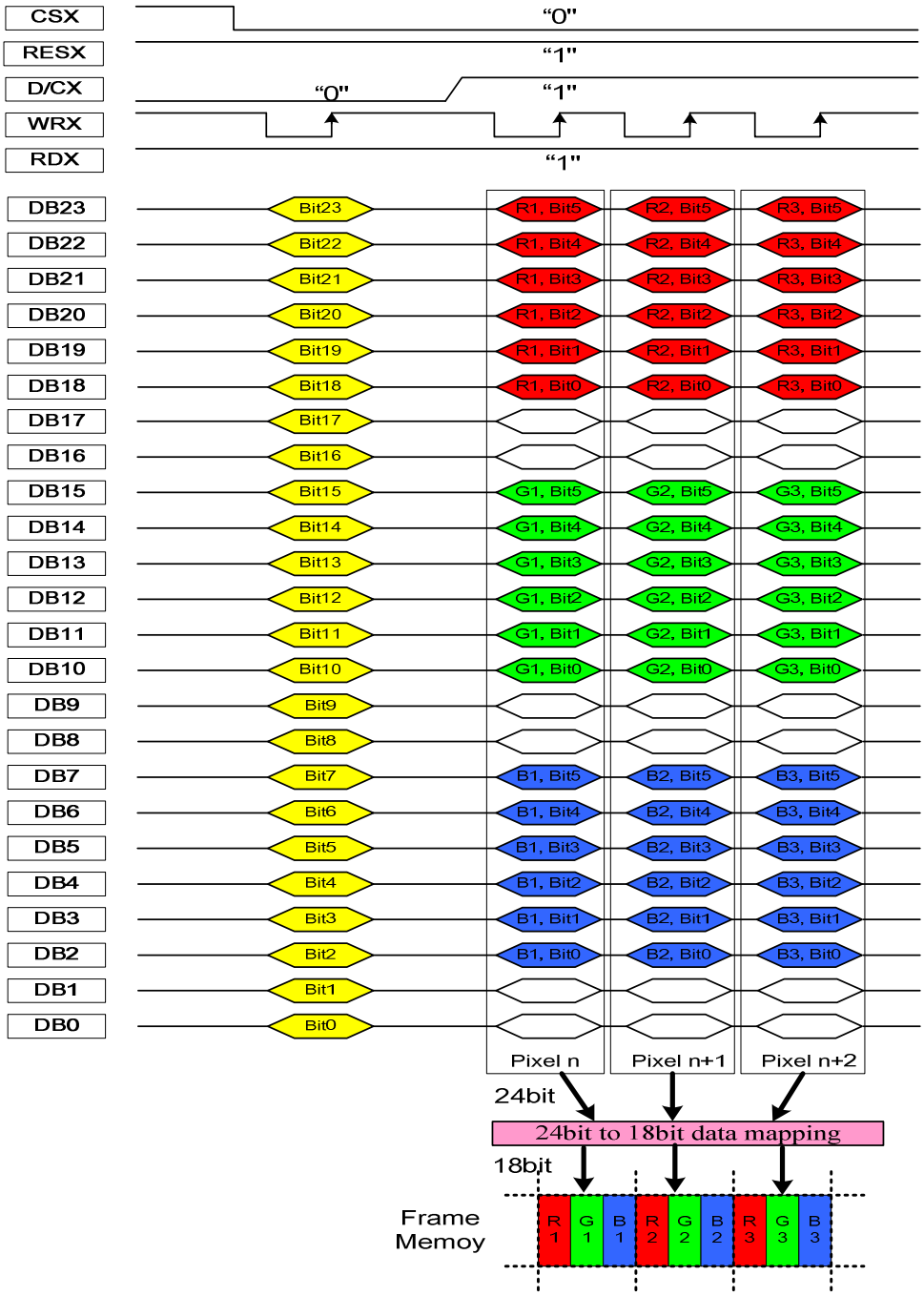

Figure 120: 24-bit Data Bus for 18-bit/pixel (RGB 8-8-8 Bits Input), 262K-color

Notes:

1. The data order is as follows: MSB = DB23, LSB = DB0, and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 1-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.

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4.8. DPI Parallel Interface（RGB Interface）

4.8.1. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits as 101. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM through the 16-bit RGB data bus in synchronization with the display operation.

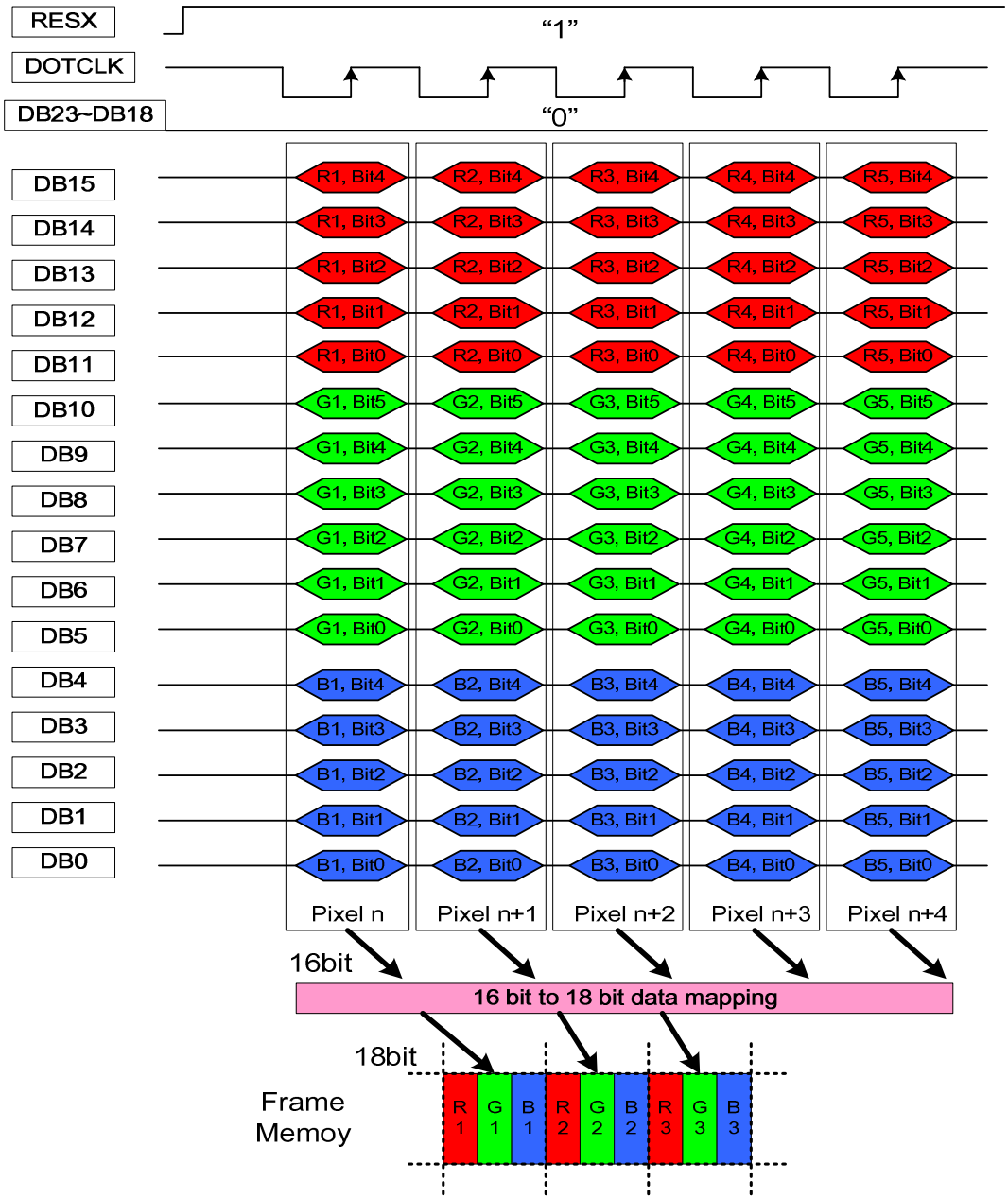

Figure 121: 16-bit/pixel 65K Colors Order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 16-bit color depth information.

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4.8.2. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits as 110. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM through the 18-bit RGB data bus in synchronization with the display operation.

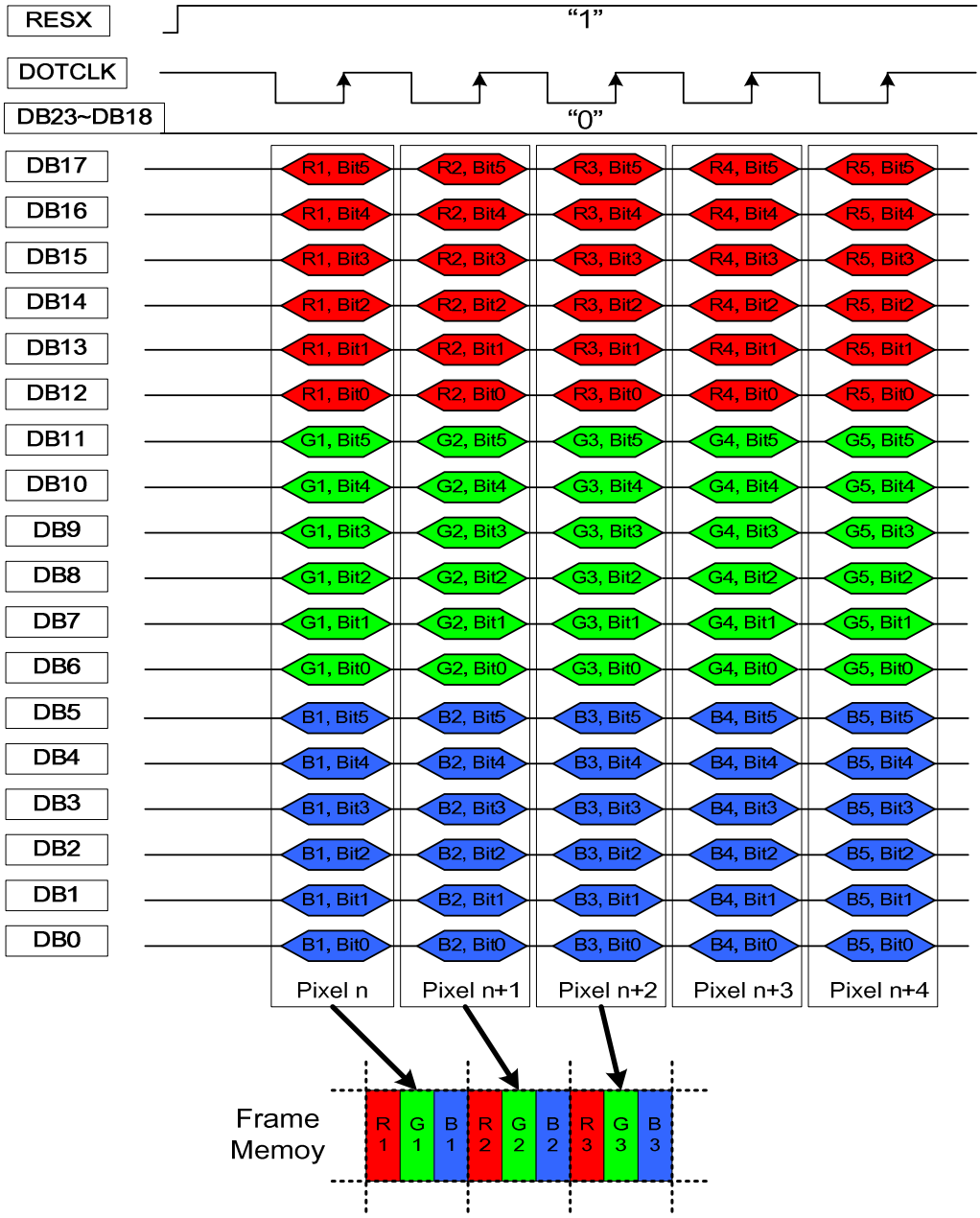

Figure 122: 18-bit/pixel 262K Colors Order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB17, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 18-bit color depth information.

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4.8.3. 24-bit Parallel RGB Interface

4.8.3.1. 18-bit/pixel

The 24-bit RGB interface is selected by setting the DPI [2:0] bits to 111 and DB_EN to 1. The display operation is synchronized with VSYNC, HSYNC, ENABLE, and DOTCLK signals. Display data is transferred to the internal GRAM through the 18-bit RGB data bus in synchronization with the display operation.

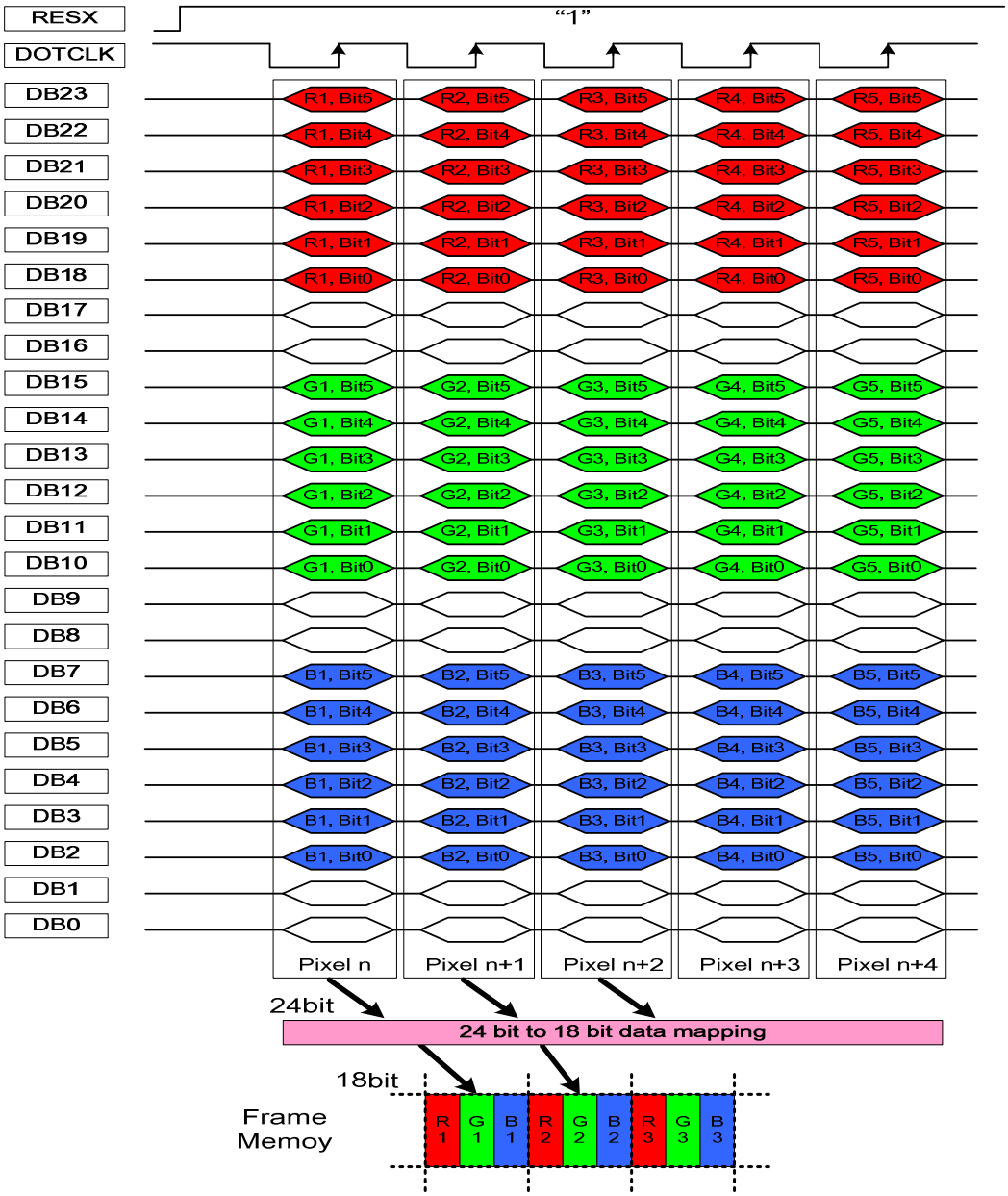

Figure 123: 24-bit/pixel 262K Colors Order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB23, LSB = DB0, and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 18-bit color depth information.

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4.8.3.2. 24-bit/pixel Constrained by Dither and Bypass

The 24-bit RGB interface is selected by setting the DPI [2:0] bits as 111, DB_EN as 1, Dither_Enable as 1, and Bypass as 1. The display operation is synchronized with VSYNC, HSYNC, ENABLE and DOTCLK signals.

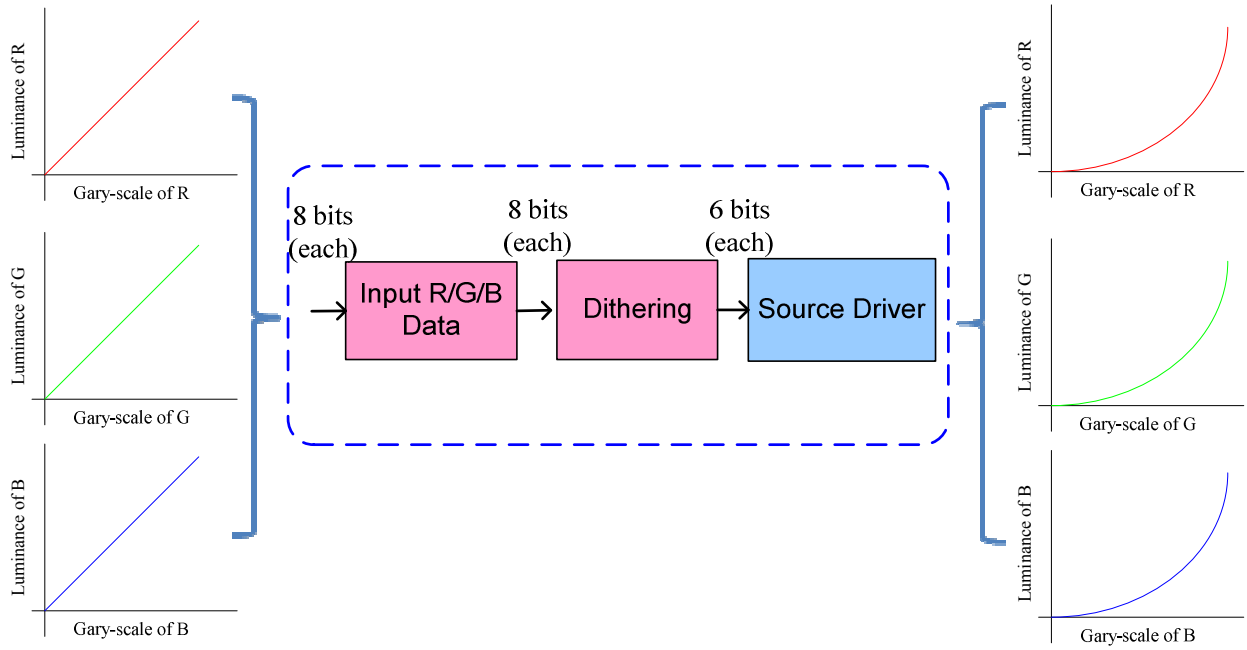

Figure 124: 24-bit/pixel 16.7M Colors Order on the DPI Interface

Notes:

1. To configure the Bypass, please refer to the Section 5.3.7 Display Function Control (B6h).
2. 1-time transfer is used to transmit 1 pixel data to the 24-bit color depth information.

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4.9. DSI Transmission Data Format

4.9.1. 16-bit per Pixel, Long Packet, Data Type = 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long packet, used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of a DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the ILI9488 has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

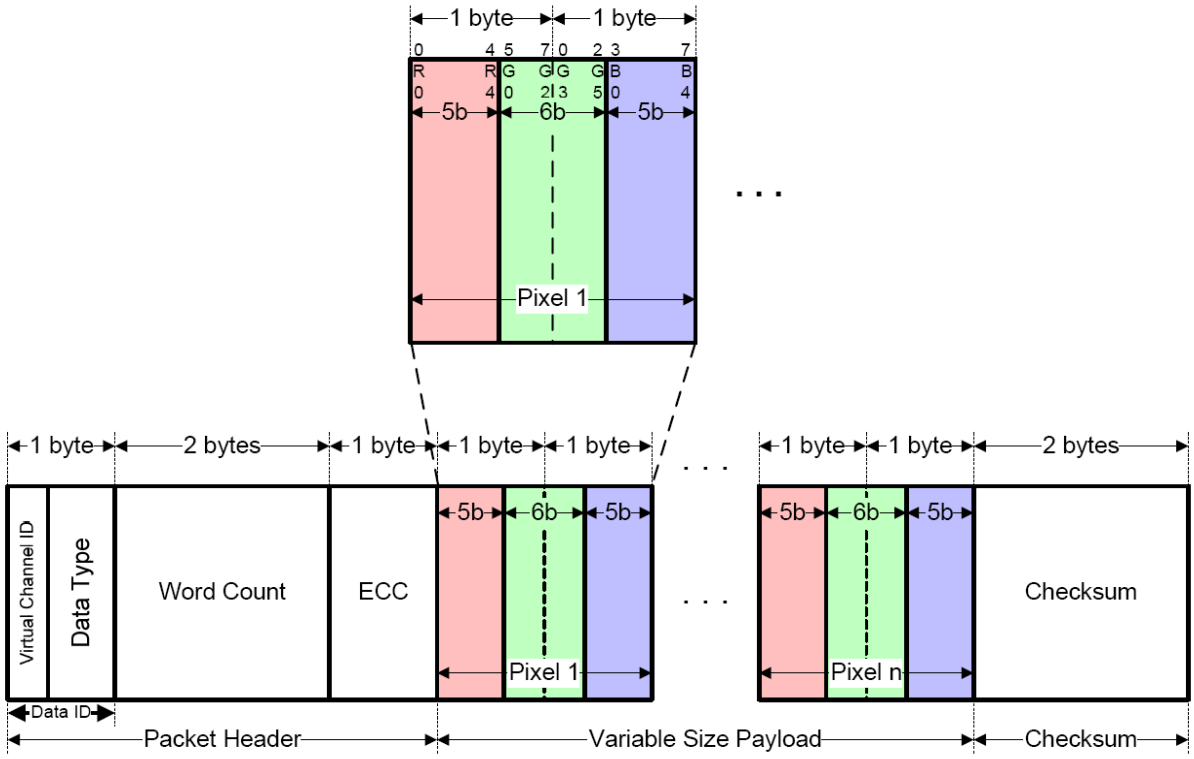

Figure 125: 16-bit per Pixel, Data Type = 00 1110 (0Eh)

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4.9.2. MIPI – 18-bit per Pixel, Long Packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of a DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first and the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission. With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

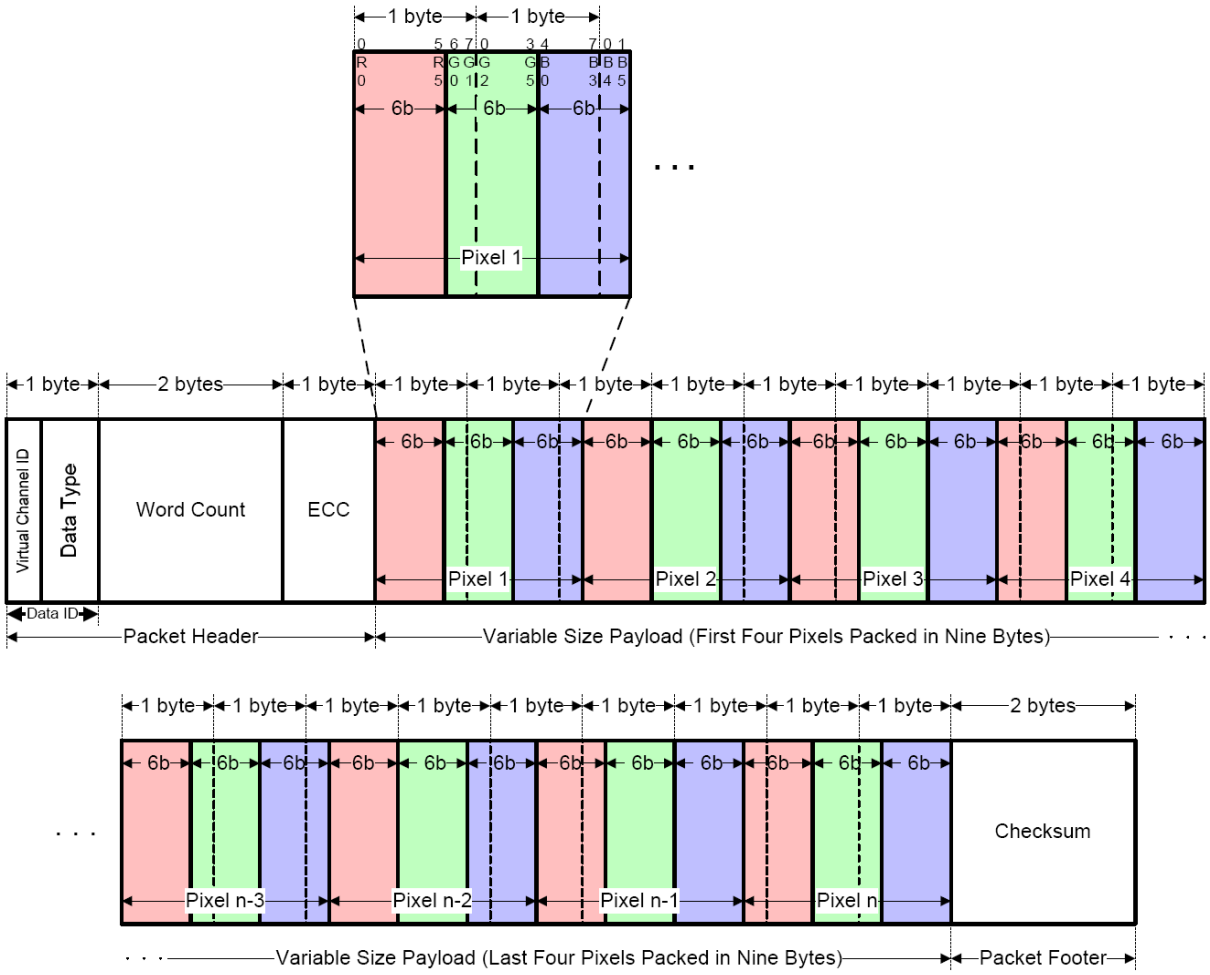

Figure 126: 18-bit per Pixel, Data Type = 01 1110 (1Eh)

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4.9.3. MIPI – 18-bit per Pixel, Long Packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte, representing active pixels, are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the "packed" format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of a DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first and the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

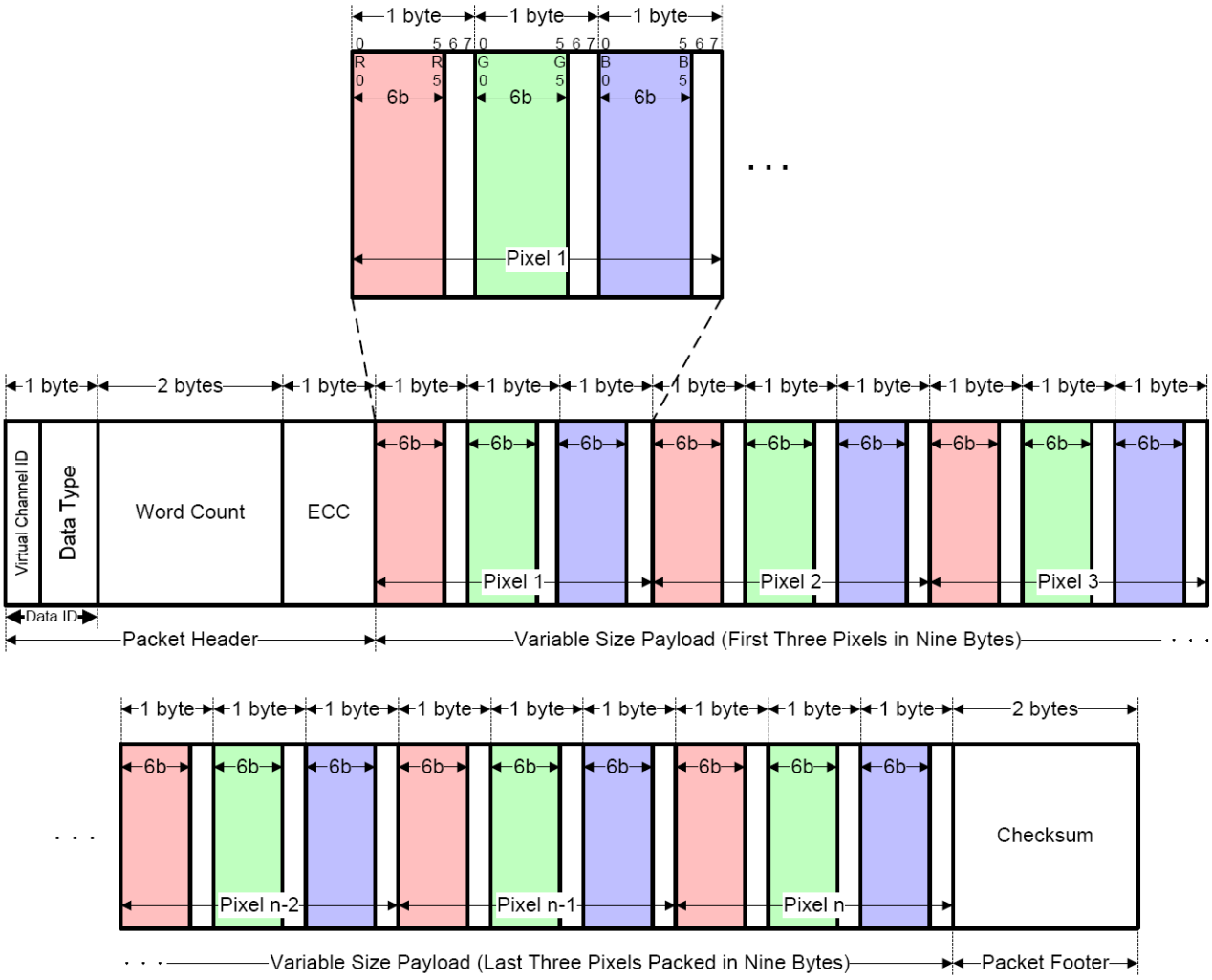

Figure 127: 18-bit per Pixel, Data Type = 10 1110 (2Eh)

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5. Command

5.1.Command List

5.1.1. Standard Command List

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	0	1	↑	XX	0	0	0	0	0	0	0	0	00h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Soft Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read display identification information	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								XX
	1	↑	1	XX	ID2 [7:0]								XX
	1	↑	1	XX	ID3 [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Number of the Errors on DSI	0	1	↑	XX	0	0	0	0	0	1	0	1	05h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	P [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [31:24]								XX
	1	↑	1	XX	D [23:16]								XX
	1	↑	1	XX	D [15:8]								XX
	1	↑	1	XX	D [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	DPI [2:0]			0	DBI [2:0]			XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Image Mode	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	0	0	0	0	0	D0	XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Sleep IN	0	1	↑	XX	0	0	0	1	0	0	0	0	10h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h

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Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
All Pixel OFF	0	1	↑	XX	0	0	1	0	0	0	1	0	22h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
All Pixel ON	0	1	↑	XX	0	0	1	0	0	0	1	1	23h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC [15:8]								XX
	1	1	↑	XX	SC [7:0]								XX
	1	1	↑	XX	EC [15:8]								XX
	1	1	↑	XX	EC [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP [15:8]								XX
	1	1	↑	XX	SP [7:0]								XX
	1	1	↑	XX	EP [15:8]								XX
	1	1	↑	XX	EP [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D1 [23:0]									XX
	1	1	↑	Dx [23:0]									XX
	1	1	↑	Dn [23:0]									XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Read	0	↑	↑	XX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D1 [23:0]									XX
	1	↑	1	Dx [23:0]									XX
	1	↑	1	Dn [23:0]									XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR [15:8]								XX
	1	1	↑	XX	SR [7:0]								XX
	1	1	↑	XX	ER [15:8]								XX
	1	1	↑	XX	ER [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA [15:8]								XX
	1	1	↑	XX	TFA [7:0]								XX
	1	1	↑	XX	VSA [15:8]								XX
	1	1	↑	XX	VSA [7:0]								XX
	1	1	↑	XX	BFA [15:8]								XX
	1	1	↑	XX	BFA [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	0	0	0	0	0	0	0	M	XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex

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Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP [15:8]								XX
	1	1	↑	XX	VSP [7:0]								XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Interface Pixel Format	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	0	DPI [6:4]			0	DBI [2:0]			XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Write Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D1 [23:0]									XX
	1	1	↑	Dx [23:0]									XX
	1	1	↑	Dn [23:0]									XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Read Continue	0	↑	↑	XX	0	0	1	1	1	1	1	0	3Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D1 [23:0]									XX
	1	↑	1	Dx [23:0]									XX
	1	↑	1	Dn [23:0]									XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Tear Scan line	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	N [15:8]								XX
	1	1	↑	XX	N [7:0]								XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Tear Scan Line	0	↑	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	N [15:8]								XX
	1	↑	1	XX	N [7:0]								XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Display Brightness value	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV [7:0]								XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Brightness Value	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	DBV [7:0]								XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write CTRL Display value	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read CTRL Display value	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Content Adaptive Brightness Control value	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XX	0	0	0	0	0	0	C [1:0]		XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Content Adaptive Brightness Control value	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	0	0	0	0	C [1:0]		XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	XX	CMB [7:0]								XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	CMB [7:0]								XX
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read automatic brightness	0	1	↑	XX	0	1	1	0	1	0	0	0	68h

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control self-diagnostic result	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:6]		0	0	0	0	0	0	XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID2 [7:0]								XX

Command Function	D/CX	RDX	WRX	D [23:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID3 [7:0]								XX

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5.1.2. Extended Command List

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Interface Mode Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	SDA_EN	0	0	0	VSPL	HSPL	DPL	EPL	00h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Frame Rate Control (In Normal Mode/Full Colors)	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XX	FRS [3:0]				0	0	DIVA [1:0]		A0h
	1	1	↑	XX	0	0	0	RTNA [4:0]					11h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Frame Rate Control (In Idle Mode/8 colors)	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XX	0	0	0	0	0	0	DIVB[1:0]		00h
	1	1	↑	XX	0	0	0	RTNB [4:0]					11h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Frame Rate Control (In Partial Mode/Full colors)	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XX	0	0	0	0	0	0	DIVC[1:0]		00h
	1	1	↑	XX	0	0	0	RTNC [4:0]					11h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XX	0	0	0	0	0	DINV[2:0]			02h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	0	0	VFP [4:0]					02h
	1	1	↑	XX	0	0	0	VBP [4:0]					02h
	1	1	↑	XX	HFP [7:0]								0Ah
	1	1	↑	XX	HBP [7:0]								04h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	BYPASS	RCM	RM	DM	PTG [1:0]		PT [1:0]		02h
	1	1	↑	XX	0	GS	SS	SM	ISC [3:0]				02h
	1	1	↑	XX	0	0	NL [5:0]						3Bh

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Entry Mode Set	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XX	EPF [1:0]		0	0	DSTB	GON	DTE	GAS	06h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Color Enhancement Control 1	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
	1	1	↑	XX	0	0	0	First_Axis 1 [4:0]					04h
	1	1	↑	XX	0	0	0	First_Axis 2 [4:0]					04h
	1	1	↑	XX	0	0	0	First_Axis 3 [4:0]					04h
	1	1	↑	XX	0	0	0	First_Axis 4 [4:0]					04h
	1	1	↑	XX	0	0	0	Second_Axis 1 [4:0]					04h
	1	1	↑	XX	0	0	0	Second _Axis 2 [4:0]					04h
	1	1	↑	XX	0	0	0	Second _Axis 3 [4:0]					04h
	1	1	↑	XX	0	0	0	Second _Axis 4 [4:0]					04h
	1	1	↑	XX	0	0	0	Third_Axis 1 [4:0]					04h
	1	1	↑	XX	0	0	0	Third _Axis 2 [4:0]					04h
	1	1	↑	XX	0	0	0	Third _Axis 3 [4:0]					04h
	1	1	↑	XX	0	0	0	Third _Axis 4 [4:0]					04h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Color Enhancement Control 1	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
	1	1	↑	XX	0	0	0	Fourth_Axis 1 [4:0]					04h
	1	1	↑	XX	0	0	0	Fourth _Axis 2 [4:0]					04h
	1	1	↑	XX	0	0	0	Fourth _Axis 3 [4:0]					04h
	1	1	↑	XX	0	0	0	Fourth _Axis 4 [4:0]					04h
	1	1	↑	XX	0	0	0	Fifth _Axis 1 [4:0]					04h
	1	1	↑	XX	0	0	0	Fifth _Axis 2 [4:0]					04h
	1	1	↑	XX	0	0	0	Fifth _Axis 3 [4:0]					04h
	1	1	↑	XX	0	0	0	Fifth _Axis 4 [4:0]					04h

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	1	1	↑	XX	0	0	0	Sixth _Axis 1 [4:0]					04h
	1	1	↑	XX	0	0	0	Sixth _Axis 2 [4:0]					04h
	1	1	↑	XX	0	0	0	Sixth _Axis 3 [4:0]					04h
	1	1	↑	XX	0	0	0	Sixth_Axis 4 [4:0]					04h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
HS Lanes Control	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh
	1	1	↑	XX	0	D/C_ Swap	PN_Inv	0	0	BT_ OTP	0	0	00h
	1	1	↑	XX	0	0	0	0	0	ENHIBI T	0	0	00h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Power Control 1	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XX	0	0	0	VRH1 [4:0]					0Eh
	1	1	↑	XX	0	0	0	VRH2 [4:0]					0Eh
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Power Control 2	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	0	1	0	0	0	BT [2:0]			44h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Power Control 3	0	1	↑	XX	1	1	0	0	0	0	1	0	C2h
	1	1	↑	XX	0	DCA1 [2:0]			0	DCA0 [2:0]			33h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Power Control 4	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XX	0	DCB1 [2:0]			0	DCB0 [2:0]			33h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Power Control 5	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XX	0	DCC2 [2:0]			0	DCC0 [2:0]			33h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VCOM Control 1	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XX	0	0	0	0	0	0	0	nVM	00h
	1	1	↑	XX	VCM_REG [7:0]								40h
	1	1	↑	XX	VCM_REG_ EN	0	0	0	0	0	0	0	00h
	1	1	↑	XX	VCM_OUT [7:0]								40h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 1	0	1	↑	XX	1	1	0	0	0	1	1	0	C6h
	1	1	↑	XX	SCD_VLINE [7:0]								E0h
	1	1	↑	XX	0	0	0	0	0	SCD_VLINE [10:8]			01h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 2	0	1	↑	XX	1	1	0	0	1	0	0	0	C8h
	1	1	↑	XX	0	0	0	0	0	0	0	PWMPOL	B0h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 3	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
	1	1	↑	XX	THRES_MOV [3:0]				THRES_STILL [3:0]				BBh
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 4	0	1	↑	XX	1	1	0	0	1	0	1	0	CAh
	1	1	↑	XX	0	0	0	0	THRES_UI [3:0]				0Bh
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 5	0	1	↑	XX	1	1	0	0	1	0	1	1	CBh
	1	1	↑	XX	DTH_MOV [3:0]				DTH_STILL [3:0]				A8h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 6	0	1	↑	XX	1	1	0	0	1	1	0	0	CCh
	1	1	↑	XX	0	0	0	0	DTH_UI [3:0]				03h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 7	0	1	↑	XX	1	1	0	0	1	1	0	1	CDh
	1	1	↑	XX	0	DIM_MOV [2:0]			0	DIM_STILL [2:0]			43h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 8	0	1	↑	XX	1	1	0	0	1	1	1	0	CEh
	1	1	↑	XX	DIM_MIN [3:0]				0	DIM_UI [2:0]			02h

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Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CABC Control 9	0	1	↑	XX	1	1	0	0	1	1	1	1	CFh
	1	1	↑	XX	PWM_DIV [7:0]								F8h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NV Memory Write	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
	1	1	↑	XX	PGM_ADR [7:0]								00h
	1	1	↑	XX	PGM_DATA [7:0]								00h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NV Memory Protection Key	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h
	1	1	↑	XX	KEY [23:16]								55h
	1	1	↑	XX	KEY [15:8]								AAh
	1	1	↑	XX	KEY [7:0]								66h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NV Memory Status Read	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID2_CNT [3:0]				ID1_CNT [3:0]				00h
	1	↑	1	XX	VCM_CNT [3:0]				ID3_CNT [3:0]				00h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read ID4	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								00h
	1	↑	1	XX	ID2 [7:0]								94h
	1	↑	1	XX	ID3 [7:0]								88h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Adjust Control 1	0	1	↑	XX	1	1	0	1	0	1	1	1	D7h
	1	1	↑	XX	0	0	Chopper_op_clk_opt	Chopper_op_clk_sel[1:0]		0	1	1	03h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read ID4 Check	0	1	↑	XX	1	1	0	1	1	0	0	0	D8h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID [7:0]								00h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PGAMCTRL(Positive Gamma Control)	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
	1	1	↑	XX	0	0	0	0	VP0 [3:0]				00h
	1	1	↑	XX	0	0	VP1 [5:0]						07h
	1	1	↑	XX	0	0	VP2 [5:0]						0Ch
	1	1	↑	XX	0	0	0	0	VP4 [3:0]				05h
	1	1	↑	XX	0	0	0	VP6 [4:0]					13h
	1	1	↑	XX	0	0	0	0	VP13 [3:0]				09h
	1	1	↑	XX	0	VP20 [6:0]							36h
	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]				AAh
	1	1	↑	XX	0	VP43 [6:0]							46h
	1	1	↑	XX	0	0	0	0	VP50 [3:0]				09h
	1	1	↑	XX	0	0	0	VP57 [4:0]					10h
	1	1	↑	XX	0	0	0	0	VP59 [3:0]				0Dh
	1	1	↑	XX	0	0	VP61 [5:0]						1Ah
	1	1	↑	XX	0	0	VP62 [5:0]						1Eh
	1	1	↑	XX	0	0	0	0	VP63 [3:0]				1Fh

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NGAMCTRL(Negative Gamma Control)	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h
	1	1	↑	XX	0	0	0	0	VN0 [3:0]				00h
	1	1	↑	XX	0	0	VN1 [5:0]						20h
	1	1	↑	XX	0	0	VN2 [5:0]						23h
	1	1	↑	XX	0	0	0	0	VN4 [3:0]				04h
	1	1	↑	XX	0	0	0	VN6 [4:0]					10h

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	1	1	↑	XX	0	0	0		VN13 [3:0]				06h
	1	1	↑	XX	0	VN20 [6:0]							37h
	1	1	↑	XX	VN27 [3:0]				VN36 [3:0]				56h
	1	1	↑	XX	0	VN43 [6:0]							49h
	1	1	↑	XX	0	0	0	0	VN50 [3:0]				04h
	1	1	↑	XX	0	0	0	VN57 [4:0]					0Ch
	1	1	↑	XX	0	0	0	0	VN59 [3:0]				0Ah
	1	1	↑	XX	0	0	VN61 [5:0]						33h
	1	1	↑	XX	0	0	VN62 [5:0]						37h
	1	1	↑	XX	0	0	0	0	VN63 [3:0]				0Fh
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				00h
	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				00h
	1	1	↑	XX	RCA63 [3:0]				BCA63 [3:0]				00h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				00h
	1	1	↑	XX	RFAx [3:0]				BFAx [3:0]				00h
	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]				00h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Set Image Function	0	1	↑	XX	1	1	1	0	1	0	0	1	E9h
	1	1	↑	XX	0	0	0	0	0	0	0	DB_EN	00h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Adjust Control 2	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	0	1	0	1	1	0	0	Chopper_delay_opt	58h
	1	1	↑	XX	0	GSW_TG1[5:0]						0	04h
	1	1	↑	XX	0	0	0	1	0	0	1	0	12h
	1	1	↑	XX	0	0	0	0	0	0	1	0	02h
	1	1	↑	XX	0	EQRTI[2:0]			0	0	1	0	22h
	1	1	↑	XX	0	1	0	1	0	0	1	0	42h
	1	1	↑	XX	1	1	1	1	1	1	1	1	FFh
	1	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	1	↑	XX	1	0	0	1	0	0	0	0	90h
	1	1	↑	XX	0	0	0	0	GSW_MODE [1:0]		0	0	14h
	1	1	↑	XX	Chopper_sel [1:0]		0	0	1	0	0	0	88h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Adjust Control 3	0	1	↑	XX	1	1	1	1	0	1	1	1	F7h
	1	1	↑	XX	1	0	1	0	1	0	0	1	A9h
	1	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	XX	DSI_18_option	0	0	0	0	0	1	0	82h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Adjust Control 4	0	1	↑	XX	1	1	1	1	1	0	0	0	F8h
	1	1	↑	XX	0	0	1	0	0	0	0	1	21h
	1	1	↑	XX	0	0	0	0	0	1	3Gamma_Enable	Dither_Enable	04h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Adjust Control 5	0	1	↑	XX	1	1	1	1	1	0	0	1	F9h
	1	1	↑	XX	0	0	0	0	Chopper_opt	0	0	0	00h
Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex

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SPI Read Command Setting	0	1	↑	XX	1	1	1	1	1	0	1	1	FBh
	1	1	↑	XX	SPI_READ_EN	0	0	0	SPI_CNT [3:0]				00h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Adjust Control 6	0	1	↑	XX	1	1	1	1	1	1	0	0	FCh
	1	1	↑	XX	0	0	0	0	0	0	0	0	00h
	1	1	↑	XX	0	0	0	NOWI [4:0]					05h

Command Function	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Adjust Control 7	0	1	↑	XX	1	1	1	1	1	1	0	0	FFh
	1	1	↑	XX	0	0	0	0	0	0	0	0	00h
	1	1	↑	XX	SAT_AXIS_EN	1	0	0	0	0	1	0	42h

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5.2.Command Description

5.2.1. NOP (00h)

00h	NOP (No Operation)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
1st Parameter	No parameter												
Description	This command is an empty command. It does not have any effect on the ILI9488. However, it can be used to terminate Frame Memory Write or Read, as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = void												
Restriction	None												
Register Availability													
Default													
Flow Chart	None												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

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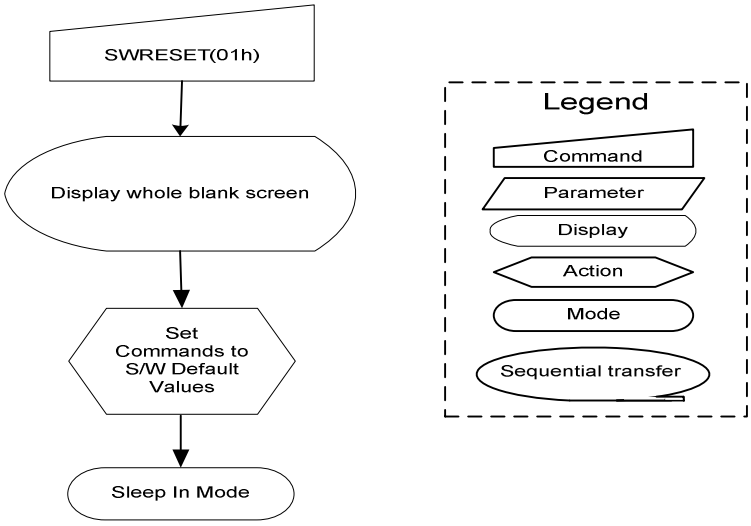
5.2.2. Software Reset (01h)

01h	SWRESET (Software Reset)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
1st Parameter	No parameter												
Description	When the Software Reset command is written, it causes software reset. It resets commands and parameters to their S/W Reset default values. (See default tables in each command description.) After the Software Reset is applied, the display becomes blank immediately. X = void ***Note:*** The Frame Memory contents are not affected by this command.												
Restriction	It is necessary to wait 5msec before sending a new command after software reset. The display module loads all factory default values of the display supplier to the registers during this 5msec. If Software Reset is applied during the Sleep Out mode, it will be necessary to wait 120msec before sending the Sleep Out command. The Software Reset Command cannot be sent during the Sleep Out sequence.												
Register Availability													
Default													
Flow Chart													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A



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5.2.3. Read Display Identification Information (04h)

04h	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D [17:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	ID1 [7:0]								XX
3rd Parameter	1	↑	1	XX	ID2 [7:0]								XX
4th Parameter	1	↑	1	XX	ID3 [7:0]								XX

Description

This read byte can read 24 bits of display identification information.

The 1st parameter is a dummy data.

The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID

The 3rd parameter (ID2 [7:0]): LCD module/driver version ID

The 4th parameter (ID3 [7:0]): LCD module/driver ID

X = void

Restriction

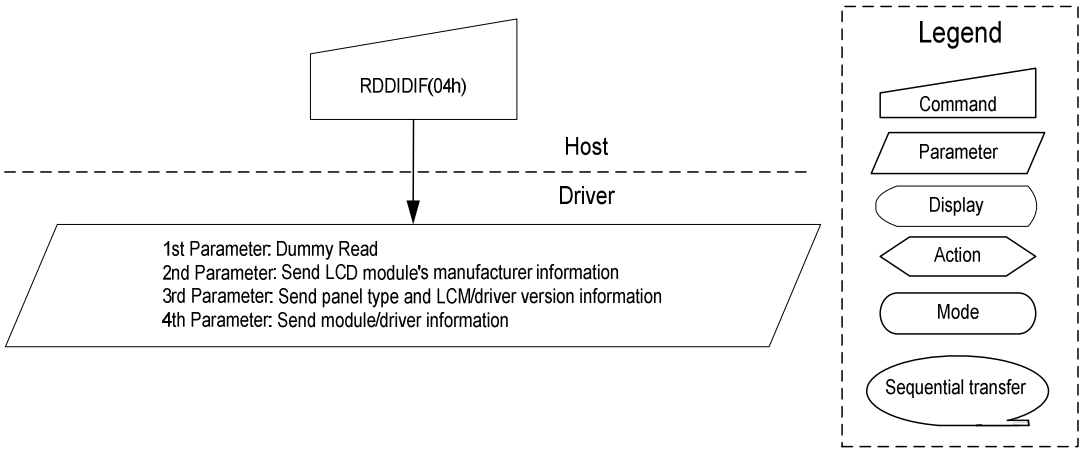
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description

Flow Chart



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5.2.4. Read Number of the Errors on DSI (05h)

05h	RDNUMED (Read Number of the Errors on DSI)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	1	05h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	P [7:0]								XX

Description

The 1st parameter is a dummy data.

The 2nd parameter indicates the number of errors on the DSI. More detailed description of the bits is below.

P [6...0] bits indicate the number of the errors.

P [7] is set to 1 if there is overflow with P [6..0] bits.

P [7...0] bits are set to 0 (RDDSM(0Eh)'s D0 is set to 0 at the same time) after the second parameter information is sent (= The read function is completed). This function always returns P [7...0] = 00h if the parallel MCU interface is selected.

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on DSI; the 1st parameter is not sent.

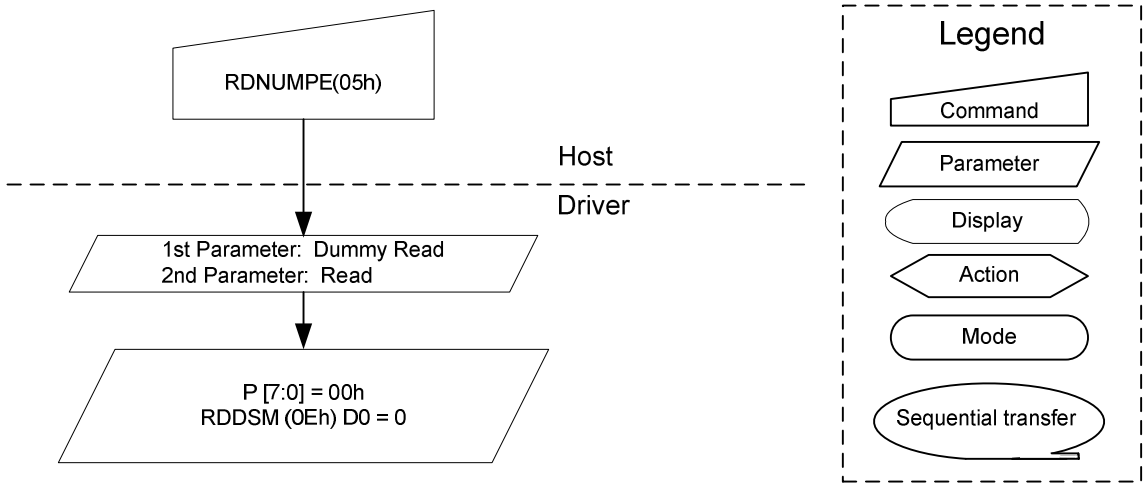
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



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5.2.5. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	D [31:24]								XX
3rd Parameter	1	↑	1	XX	D [23:16]								XX
4th Parameter	1	↑	1	XX	D [15:8]								XX
5th Parameter	1	↑	1	XX	D [7:0]								XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster OFF
		1	Booster ON
D30	Row address order	0	Top to Bottom (When MADCTL D7 = 0)
		1	Bottom to Top (When MADCTL D7 = 1)
D29	Column address order	0	Left to Right (When MADCTL D6 = 0)
		1	Right to Left (When MADCTL D6 = 1)
D28	Row/column exchange	0	Normal Mode (When MADCTL D5 = 0)
		1	Reverse Mode (When MADCTL D5 = 1)
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL D4 = 0)
		1	LCD Refresh Bottom to Top (When MADCTL D4 = 1)
D26	RGB/BGR order	0	RGB (When MADCTL D3 = 0)
		1	BGR (When MADCTL D3 = 1)
D25	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL D2 = 0)
		1	LCD Refresh Right to Left (When MADCTL D2 = 1)
D22	Interface color pixel format definition	101	16-bit/pixel
D21		110	18-bit/pixel
D20		111	24-bit/pixel
D19	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON
D17	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode
D16	Display normal mode ON/OFF	0	Display Normal Mode OFF
		1	Display Normal Mode ON
D15	Vertical scrolling status	0	Vertical Scroll OFF
		1	Vertical Scroll ON
D13	Inversion status	0	Inversion OFF
		1	Inversion ON
D10	Display ON/OFF	0	Display is OFF
		1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON

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D [8:6]	Gamma curve selection	000	GC0
D5	Tearing effect line mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking

Note: This bit indicates the current status of the line when this command is sent.

X = void

Restriction

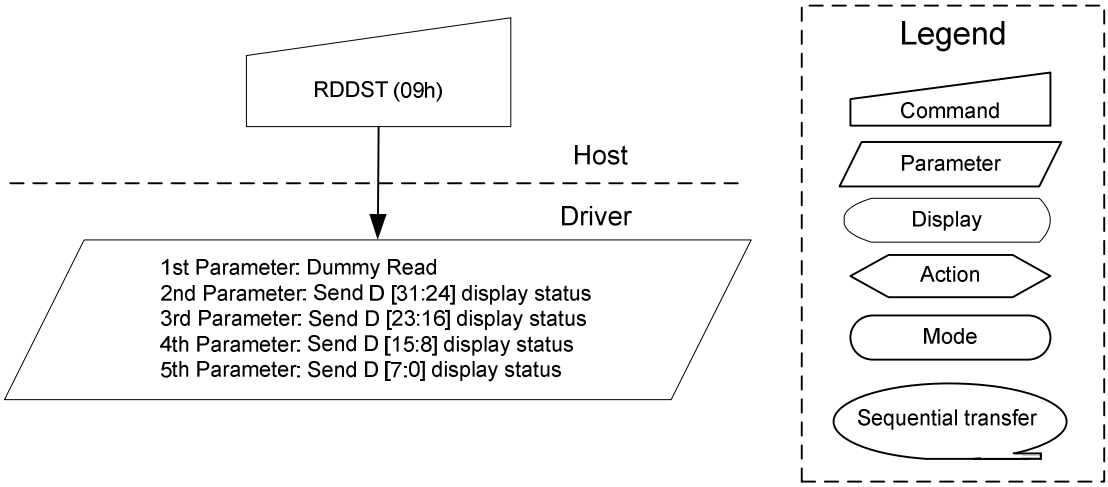
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	32'h00610000h
SW Reset	32'h00610000h
HW Reset	32'h00610000h

Flow Chart



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5.2.6. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XX	D [7:2]						0	0	XX

Description

This command indicates the current status of the display, as described in the table below:

Bit	Description	Comment
D7	Booster Voltage Status	
D6	Idle Mode On/Off	
D5	Partial Mode On/Off	
D4	Sleep In/Out	
D3	Display Normal Mode On/Off	
D2	Display On/Off	
D1	Not Defined	Set to 0
D0	Not Defined	Set to 0

- Bit D7 – Booster Voltage Status

  0 = Booster Off or has a fault.

  1 = Booster On and works OK.

- Bit D6 - Idle Mode On/Off

  0 = Idle Mode Off

  1 = Idle Mode On

- Bit D5 – Partial Mode On/Off

  0 = Partial Mode Off

  1 = Partial Mode On

- Bit D4 – Sleep In/Out

  0 = Sleep In Mode

  1 = Sleep Out Mode

- Bit D3 – Display Normal Mode On/Off

  0 = Display Normal Mode Off

  1 = Display Normal Mode On

- Bit D2 – Display On/Off

  0 = Display is Off

  1 = Display is On

- Bit D1 – Not Defined

  This bit is not applicable for this project, so it is set to 0.

- Bit D0 – Not Defined

  This bit is not applicable for this project, so it is set to 0.

X = void

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Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

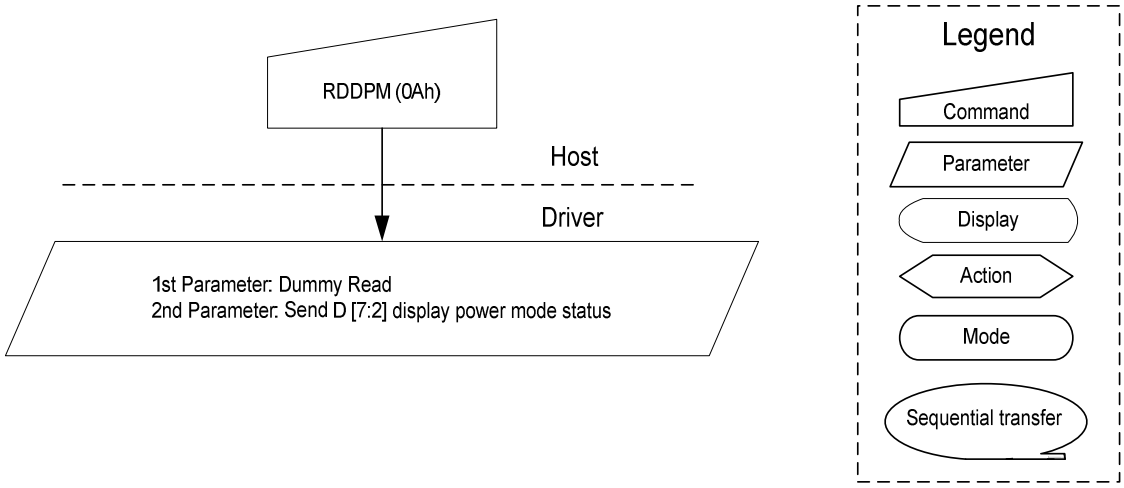
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08_{HEX}
SW Reset	08_{HEX}
HW Reset	08_{HEX}

Flow Chart



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5.2.7. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XX	D [7:2]						0	0	XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	
D6	Column Address Order	
D5	Page/Column Order	
D4	Line Address Order	
D3	RGB/BGR Order	
D2	Display Data Latch Data Order	
D1	Reserved	Set to 0
D0	Reserved	Set to 0

- Bit D7 – Page Address Order
  - 0 = Top to Bottom
  - 1 = Bottom to Top
- Bit D6 – Column Address Order
  - 0 = Left to Right
  - 1 = Right to Left
- Bit D5 - Page/Column Order
  - 0 = Normal Mode
  - 1 = Reverse Mode
  - Note: For Bits D7 to D5, also refer to Section 6.3 MCU to Memory Write/Read Direction.
- Bit D4 – Line Address Order
  - 0 = LCD Refresh Top to Bottom
  - 1 = LCD Refresh Bottom to Top
- Bit D3 – RGB/BGR Order
  - 0 = RGB
  - 1 = BGR
- Bit D2 – Display Data Latch Data Order
  - 0 = LCD Refresh Left to Right
  - 1 = LCD Refresh Right to Left

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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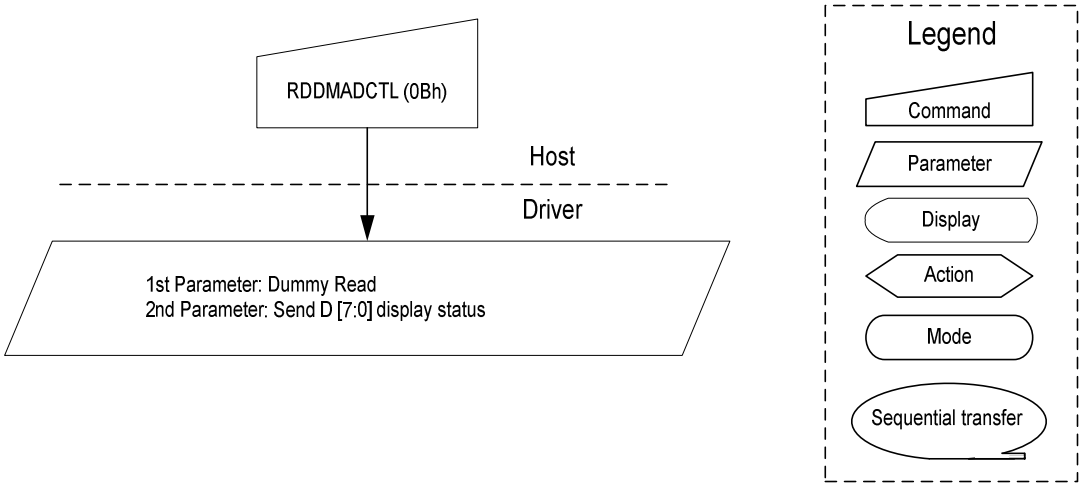
Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



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5.2.8. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display COLMOD)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	DPI [2:0]			0	DBI [2:0]			XX

Description

This command indicates the current status of the display, as described in the tables below:

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits/pixel
1	1	0	18 bits/pixel
1	1	1	24 bits/pixel

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	3 bits/pixel(8 color)
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits/pixel
1	1	0	18 bits/pixel
1	1	1	24 bits/pixel

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

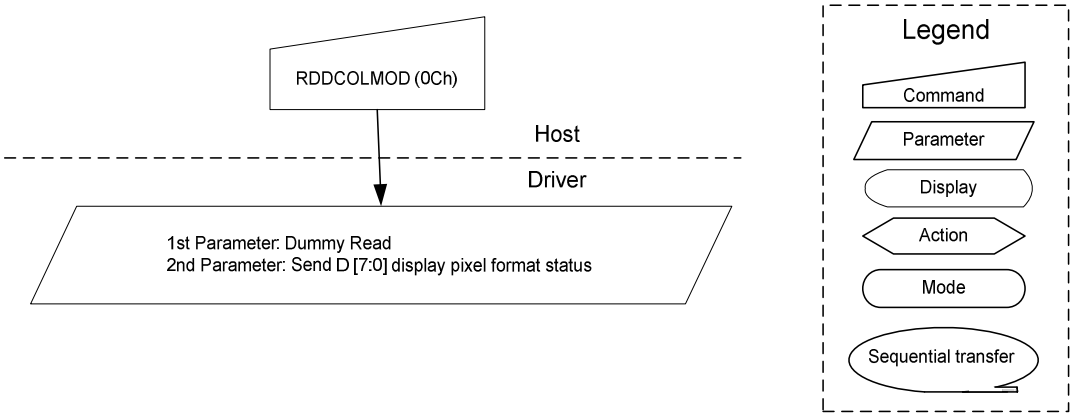
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	06_{HEX}
SW Reset	No Change
HW Reset	06_{HEX}

Flow Chart



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5.2.9. Read Display Image Mode (0Dh)

0Dh	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	D [7:0]								XX

Description

The ILI9488 can read the Display Image Mode status. This command indicates the current status of the display, as described in the table below:

Bit	Description
D7	Vertical Scrolling Status
D6	Reserved
D5	Inversion On/Off
D4	Reserved
D3	Reserved
D2	Reserved
D1	Reserved
D0	Reserved

- Bit D7 – Vertical Scrolling On/Off
  - 0 = Vertical Scrolling is Off.
  - 1 = Vertical Scrolling is On.
- Bit D6 – Reserved
- Bit D5 – Inversion On/Off
  - 0 = Inversion is Off.
  - 1 = Inversion is On.
- Bit D4 – Reserved
- Bit D3 – Reserved
- Bit D2 – Reserved
- Bit D1 – Reserved
- Bit D0 – Reserved

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

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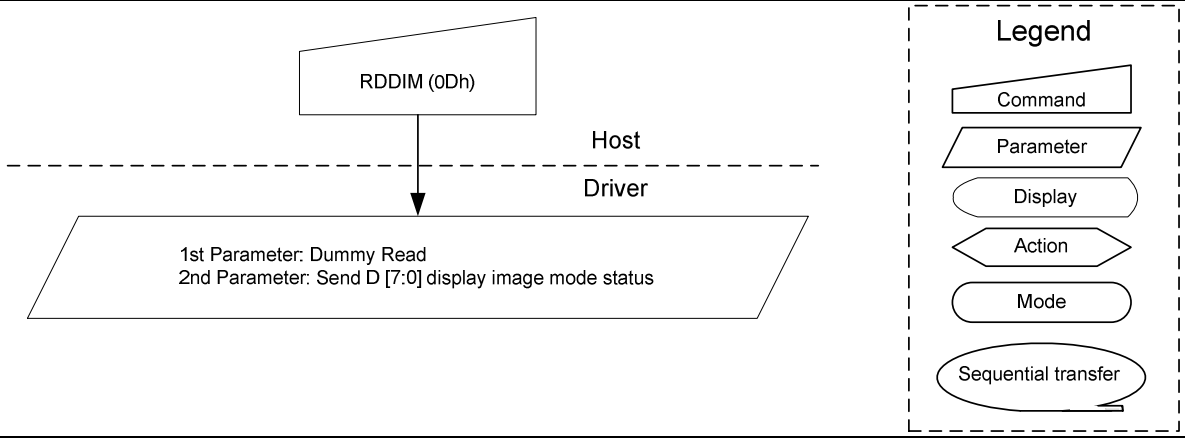
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



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5.2.10. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	XX

Description

This command indicates the current status of the display, as described in the table below:

Bit	Value	Function
D7	0	Tearing Effect Line OFF
	1	Tearing Effect Line ON
D6	0	Tearing Effect Line Mode 1
	1	Tearing Effect Line Mode 2
D5	0	Horizontal Sync (RGB interface) OFF
	1	Horizontal Sync (RGB interface) ON
D4	0	Vertical Sync (RGB interface) OFF
	1	Vertical Sync (RGB interface) ON
D3	0	Pixel Clock (DOTCLK, RGB interface) OFF
	1	Pixel Clock (DOTCLK, RGB interface) ON
D2	0	Data Enable (ENABLE, RGB interface) OFF
	1	Data Enable (ENABLE, RGB interface) ON
D1	0	Reserved
	1	Reserved
D0	0	No Error on DSI
	1	Error on DSI

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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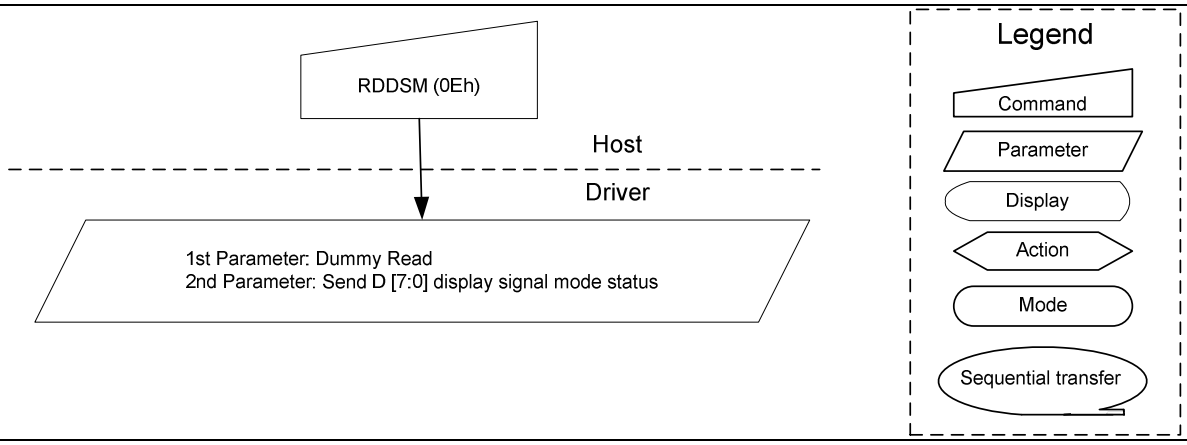
Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



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5.2.11. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	D0	XX

Description

This command indicates the status of the display self-diagnostic results after Sleep Out command, as described in the table below:

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly
D6	Functionality Detection	Invert the D6 bit if the display is working
D5	Not Used	0
D4	Not Used	0
D3	Not Used	0
D2	Not Used	0
D1	Not Used	0
D0	Checksums Comparison	0 = Checksums are same 1 = Checksums are not same

X = void

Restriction

It is necessary to wait 300ms after the last write access to registers on the User area before the Bit D0 value can be read.

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

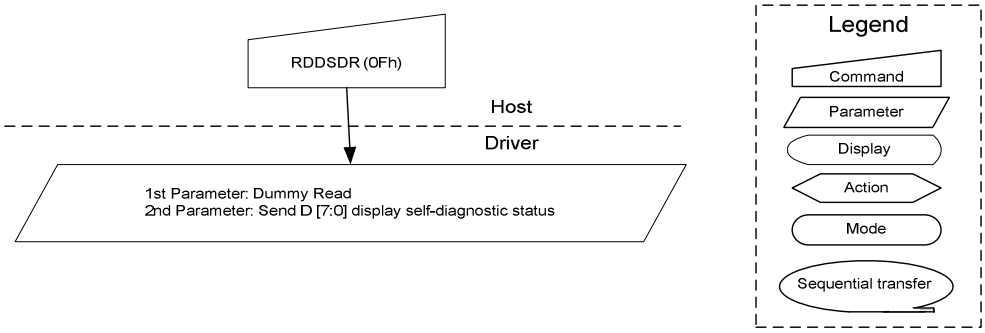
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart



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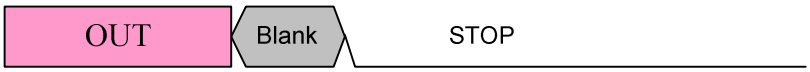
5.2.12. Sleep IN (10h)

10h	SLPIN (Sleep IN)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
1st Parameter	No parameter												

Description

This command will cause the ILI9488 enter the minimum power consumption mode.

In this mode, the DC/DC converter, Internal oscillator, and panel scanning are all stopped.



The MCU interface and memory are still working, and the memory keeps its contents.

Dimming function does not work when the mode changes from Sleep OUT to Sleep IN.

X = void

Restriction

This command has no effect when the module is already in the Sleep In mode. To exit the Sleep In mode, only the Sleep Out Command (11h) is workable. It is necessary to wait 5msec before sending the next command; this is to allow time for supply voltages and clock circuits to stabilize. It is necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

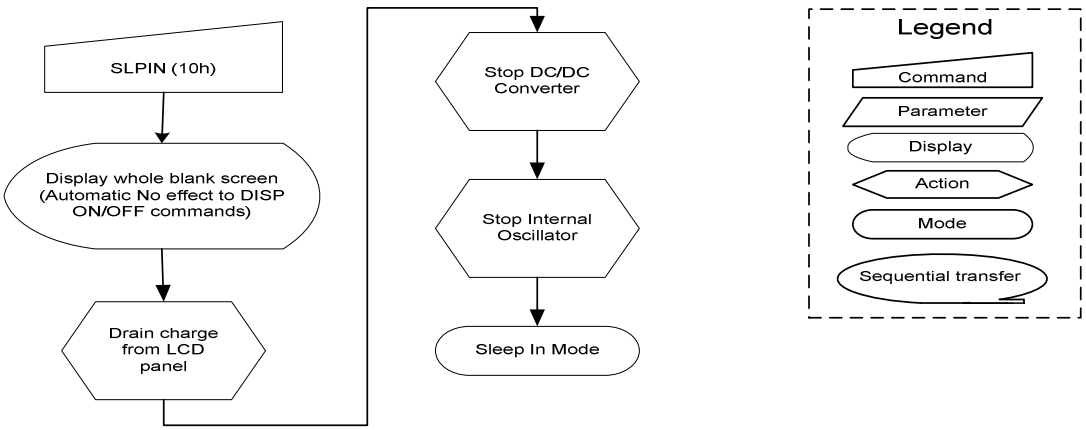
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart



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5.2.13. Sleep OUT (11h)

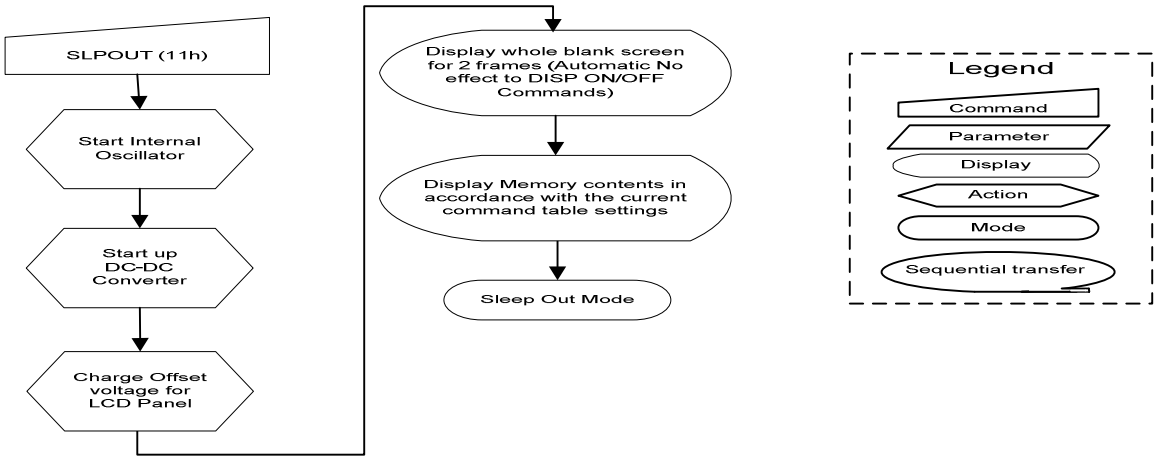
11h	SLPOUT (Sleep OUT)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
1st Parameter	No parameter												
Description	This command turns off the sleep mode. In this mode, the DC/DC converter is enabled, and Internal oscillator and panel scanning are activated. X = void												
Restriction	To exit the Sleep Out Mode, only the Sleep In Command (10h) is workable. It is necessary to wait 5msec before sending the next command; this is to allow time for supply voltages and clock circuits to stabilize. The ILI9488 loads all factory default values of the display supplier to the registers during this 5msec. There cannot be any abnormal visual effects on the display image if factory defaults and register values are the same when this load is done and when the ILI9488 is already in the Sleep Out mode. The ILI9488 performs self-diagnostic functions during this 5msec. It is necessary to wait 120msec after sending the Sleep In command (when in the Sleep Out mode) before the Sleep Out command can be sent.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep Out Mode
SW Reset	Sleep Out Mode
HW Reset	Sleep Out Mode

Flow Chart



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5.2.14. Partial Mode ON (12h)

12h	PTLON (Partial Mode ON)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
1st Parameter	No parameter												
Description	This command will turn on the Partial mode. The Partial mode window is described in the Partial Area command (30H). To leave the Partial mode, the Normal Display Mode On command (13H) should be written. X = void												
Restriction	This command has no effect when the Partial Display Mode is already active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Partial Mode On
SW Reset	Partial Mode On
HW Reset	Partial Mode On

Flow Chart: See Partial Area (30h)

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5.2.15. Normal Display Mode ON (13h)

13h	NORON (Normal Display Mode ON)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
1st Parameter	No parameter												
Description	This command will make the display return to the normal mode. Normal Display Mode On means Partial mode off and Scroll mode off. X = void												
Restriction	This command has no effect when the Normal Display mode is active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

Flow Chart: See Partial Area Descriptions for details when using this command.

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5.2.16. Display Inversion OFF (20h)

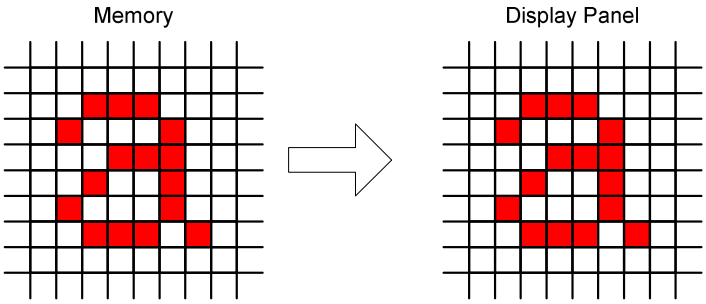
20h	INVOFF (Display Inversion OFF)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
1st Parameter	No parameter												

Description

This command is used to recover from the Display Inversion mode. Output from the Frame Memory is enabled.

This command makes no change to the content of the frame memory.

This command does not change any other status.



X = void

Restriction

This command has no effect when the ILI9488 is already in the Inversion Off mode.

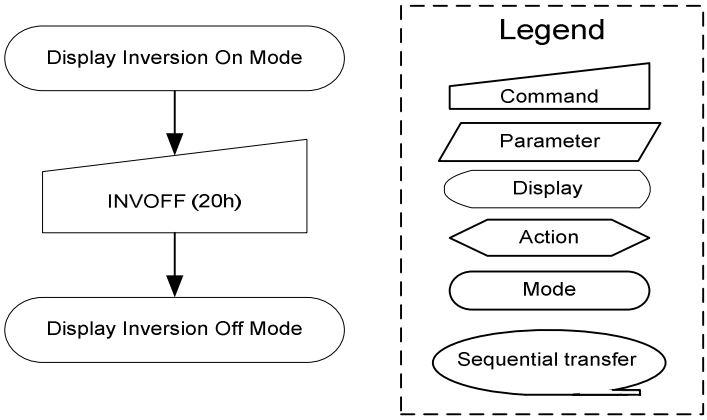
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



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5.2.17. Display Inversion ON (21h)

21h	INVON (Display Inversion ON)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
1st Parameter	No parameter												

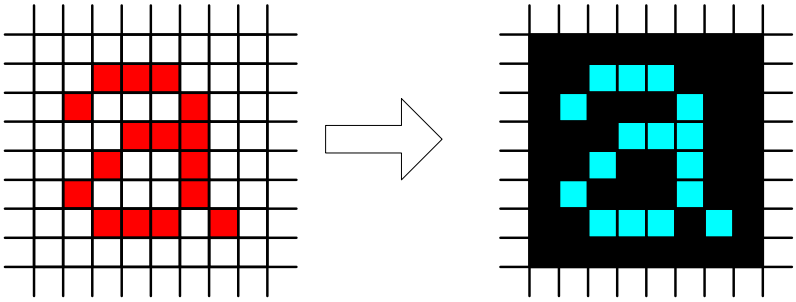
Description

This command is used to enter the Display Inversion mode.

This command makes no change of the content of the frame memory. Every bit is inverted from the frame memory to the display.

This command does not change any other status.

To exit Display Inversion mode, the Display inversion OFF command (20h) should be written.



X = void

Restriction

This command has no effect when the ILI9488 is already in the Inversion On mode.

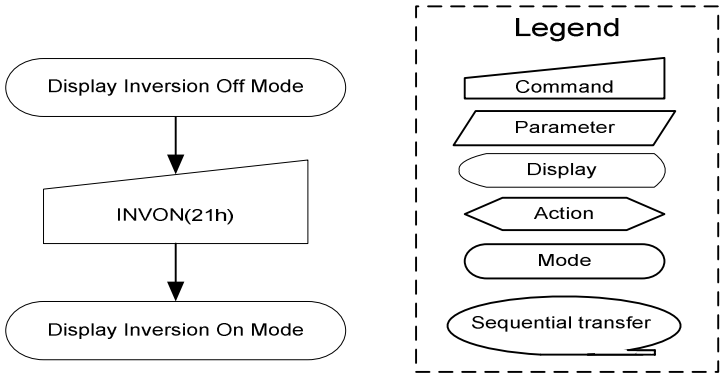
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



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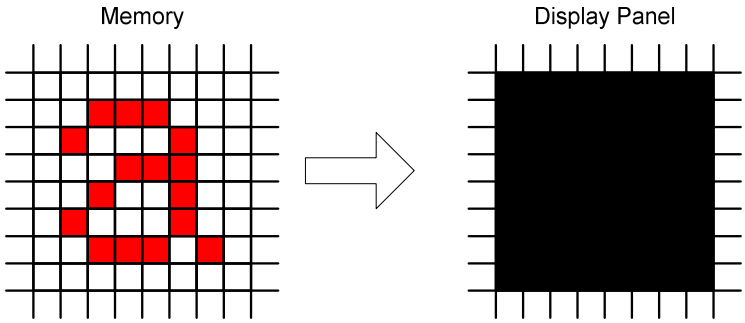
5.2.18. All Pixels OFF (22h)

22h	ALLPOFF (All pixels off)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	1	0	22h
1st Parameter	No parameter												

Description

This command turns the display panel black in the Sleep Out mode, and the status of the Display On/Off register can be On or Off. This command makes no change to the contents of the Frame Memory. This command does not change any other status.



To exit this mode, All Pixels On, Normal Display Mode On or Partial Mode On commands can be used. The display panel shows the content of the Frame Memory after applying Normal Display Mode On and Partial Mode On commands.

X = void

Restriction

This command has no effect when the ILI9488 is already in the Display Inversion On mode.

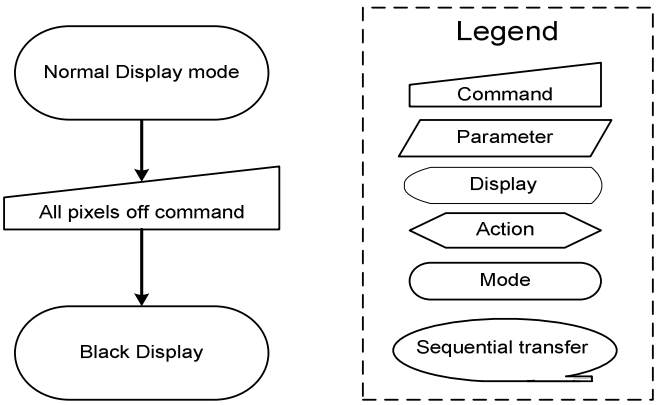
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



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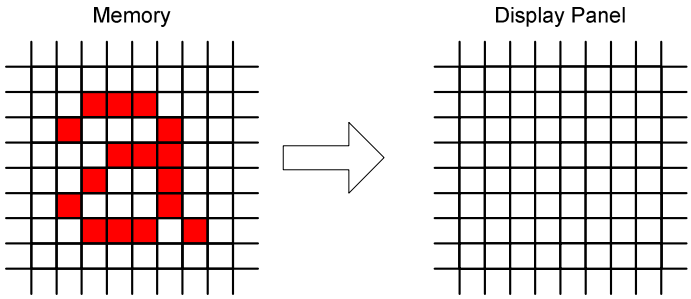
5.2.19. All Pixels ON (23h)

23h	ALLPON (All pixels on)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	1	1	23h
1st Parameter	No parameter												

Description

This command turns the display panel white in the Sleep Out mode, and the status of the Display On/Off register can be On or Off. This command makes no change to the contents of the Frame Memory. This command does not change any other status.



To exit this mode, All Pixels Off, Normal Display Mode On or Partial Mode On commands can be used. The display shows the content of the Frame Memory after applying Normal Display Mode On and Partial Mode On commands.

X = void

Restriction

This command has no effect when the ILI9488 is already in the Inversion On mode.

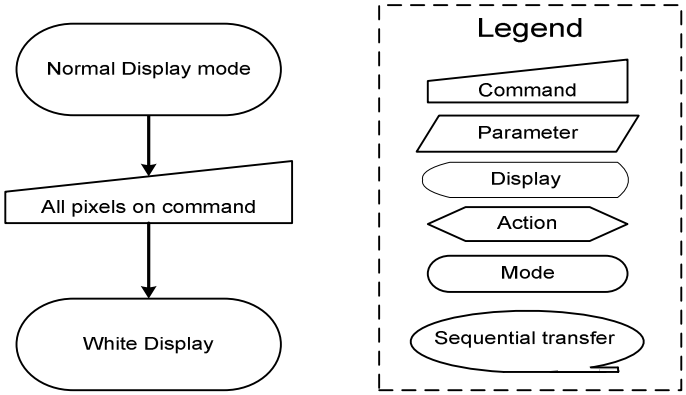
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



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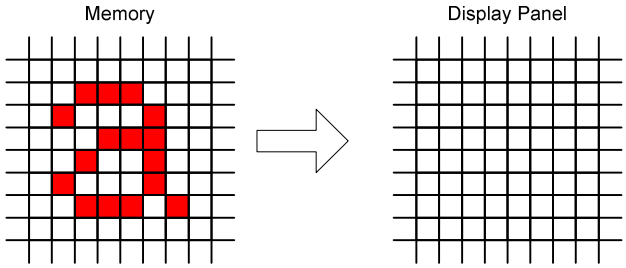
5.2.20. Display OFF (28h)

28h	DISOFF (Display OFF)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
1st Parameter	No parameter												
Description	This command causes the ILI9488 to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.  X = void												
Restriction	This command has no effect when the ILI9488 is already in the Display Off mode.												

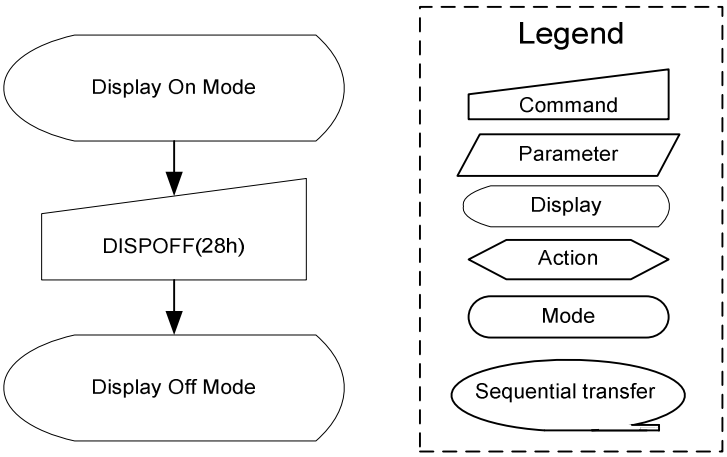
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



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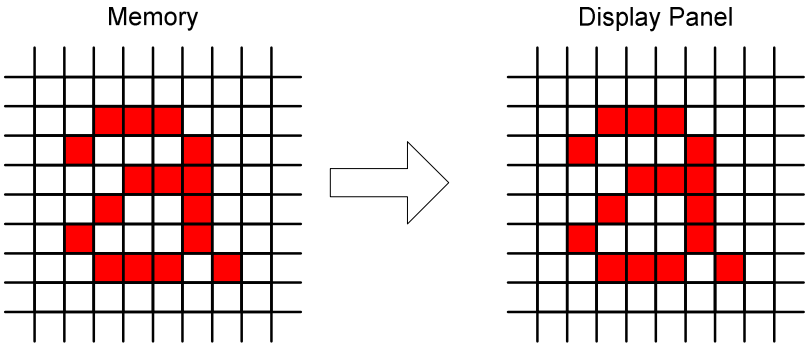
5.2.21. Display ON (29h)

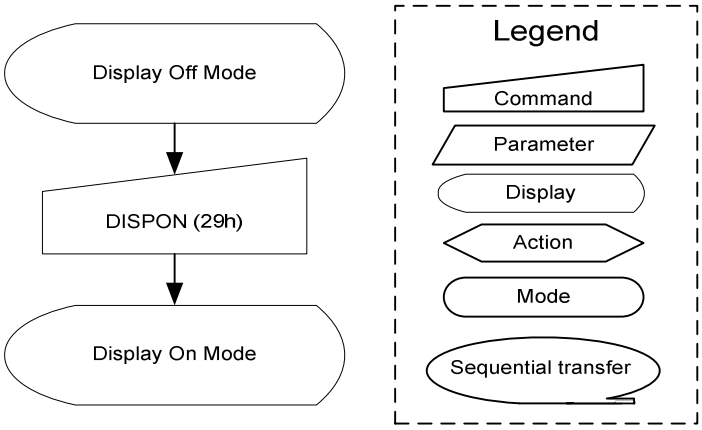
29h	DISON (Display ON)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
1st Parameter	No parameter												
Description	This command causes the ILI9488 to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.  X = void												
Restriction	This command has no effect when the ILI9488 is already in the Display On mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



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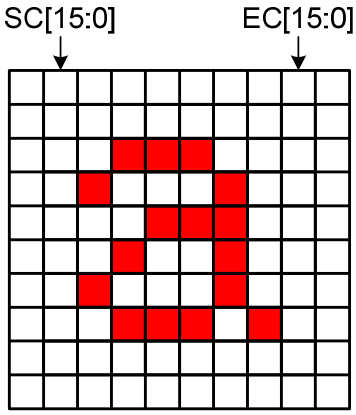
5.2.22. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC [15:8]								XX
2nd Parameter	1	1	↑	XX	SC [7:0]								XX
3rd Parameter	1	1	↑	XX	EC [15:8]								XX
4th Parameter	1	1	↑	XX	EC [7:0]								XX

Description

This command is used to define the area of the frame memory that the MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command is applied. Each value represents one column line in the Frame Memory.



X = void

Restriction

SC [15:0] must always be equal to or less than EC [15:0].

Note: When SC [15:0] or EC [15:0] is greater than 013Fh (when MADCTL's D5 = 0) or 01DFh (when MADCTL's D5 = 1), data out of range will be ignored.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC [15:0] = 0000h	EC [15:0] = 00EFh
SW Reset	SC [15:0] = 0000h	If MADCTL's D5 = 0: EC [15:0] = 013Fh If MADCTL's D5 = 1: EC [15:0] = 01DFh
HW Reset	SC [15:0] = 0000h	EC [15:0] = 013Fh

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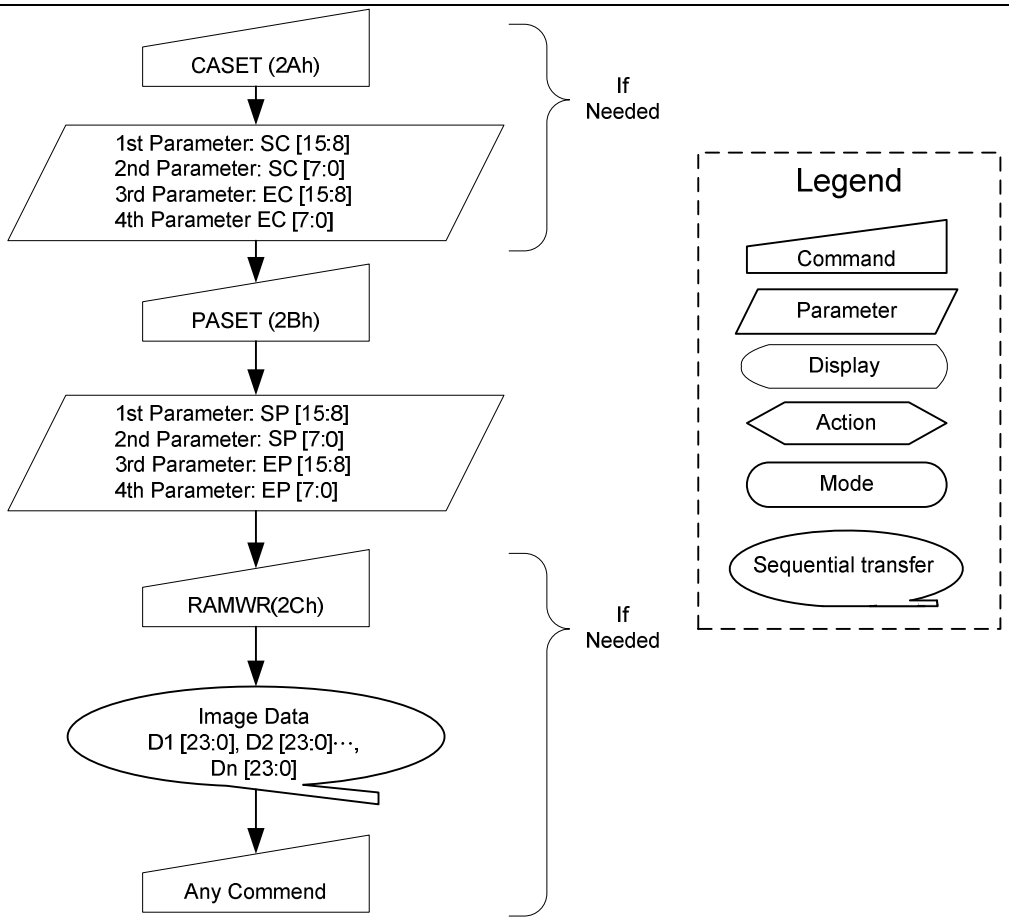
Flow Chart	

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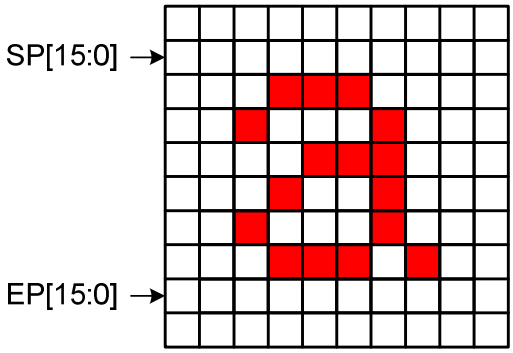
5.2.23. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XX	SP [15:8]								XX
2nd Parameter	1	1	↑	XX	SP [7:0]								XX
3rd Parameter	1	1	↑	XX	EP [15:8]								XX
4th Parameter	1	1	↑	XX	EP [7:0]								XX

Description

This command is used to define the area of the frame memory that the MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command is applied. Each value represents one Page line in the Frame Memory.



X = void

Restriction

SP [15:0] must always be equal to or less than EP [15:0]

When SP [15:0] or EP [15:0] is greater than 01DFh (when MADCTL's D5 = 0) or 013Fh (when MADCTL's D5 = 1), data out of range will be ignored.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP [15:0] = 0000h	EP [15:0] = 013Fh
SW Reset	SP [15:0] = 0000h	If MADCTL's D5 = 0: EP [15:0] = 01DFh If MADCTL's D5 = 1: EP [15:0] = 013Fh
HW Reset	SP [15:0] = 0000h	EP [15:0] = 01EFh

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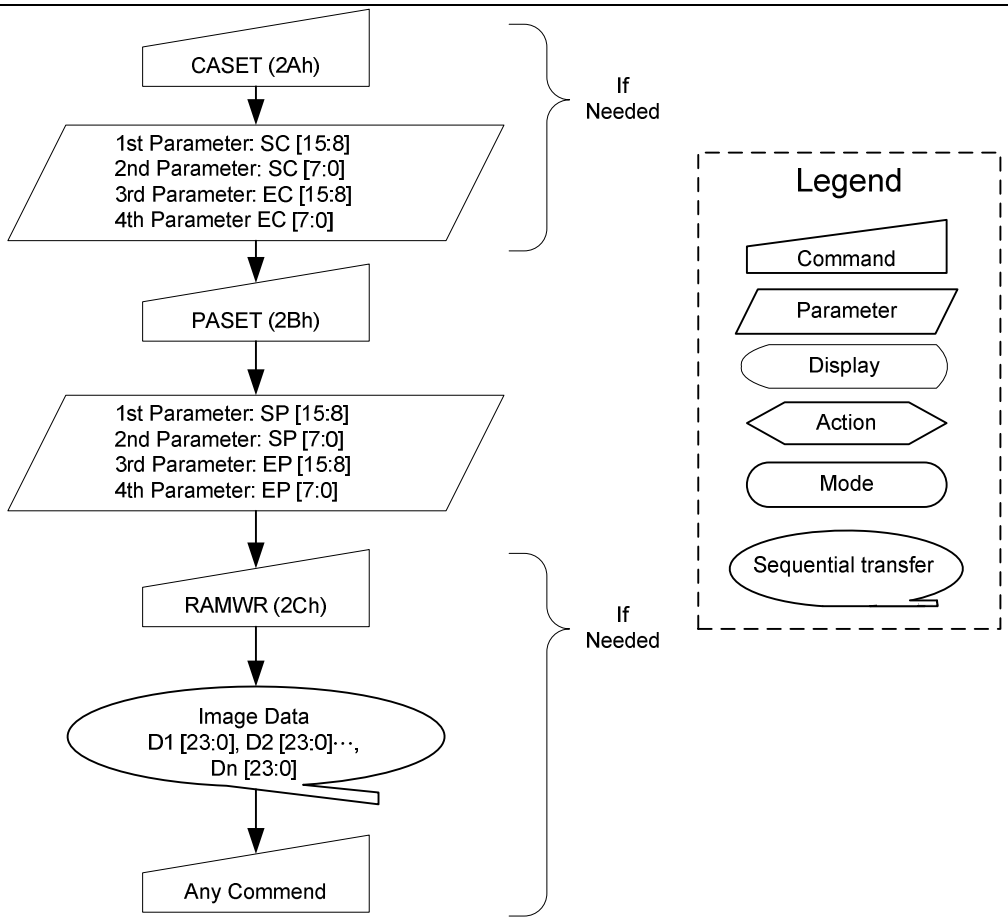
Flow Chart	

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5.2.24. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [23:0]									XX
:	1	1	↑	Dx [23:0]									XX
Nth Parameter	1	1	↑	Dn [23:0]									XX

Description

This command transfers image data from the host processor to the ILI9488's frame memory starting at the pixel location specified by Column Address Set (2Ah) and Page Address Set (2Bh) commands.

If Memory Access Control (36h) D5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in the frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1), the extra pixels are ignored.

If Memory Access control (36h) D5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in the frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1), the extra pixels are ignored.

X = void

Restriction

There is no restriction on the length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

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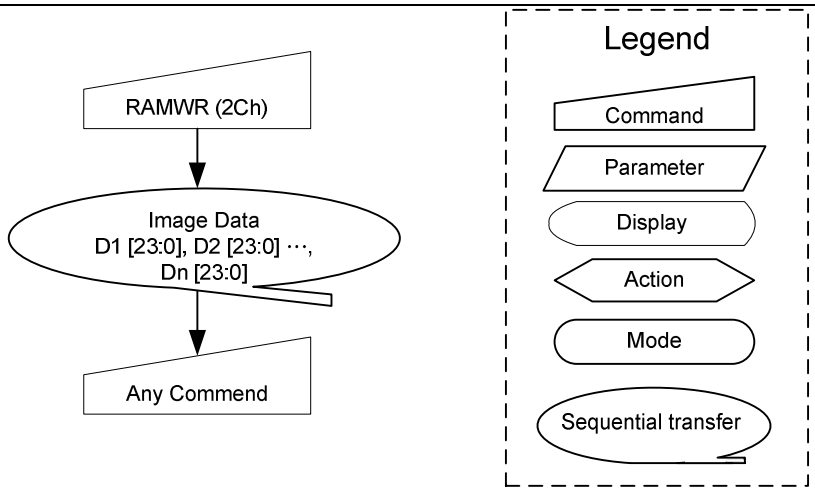
Flow Chart	

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5.2.25. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	D1 [23:0]									XX
:	1	↑	1	Dx [23:0]									XX
(N+1)th Parameter	1	↑	1	Dn [23:0]									XX

Description

This command transfers image data from the ILI9488's frame memory to the host processor starting at the pixel location specified by set_column_address and set_page_address commands.

If Memory Access control (36h) D5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from the frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control (36h) D5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from the frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

X = void

Restriction

There is no restriction on the length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

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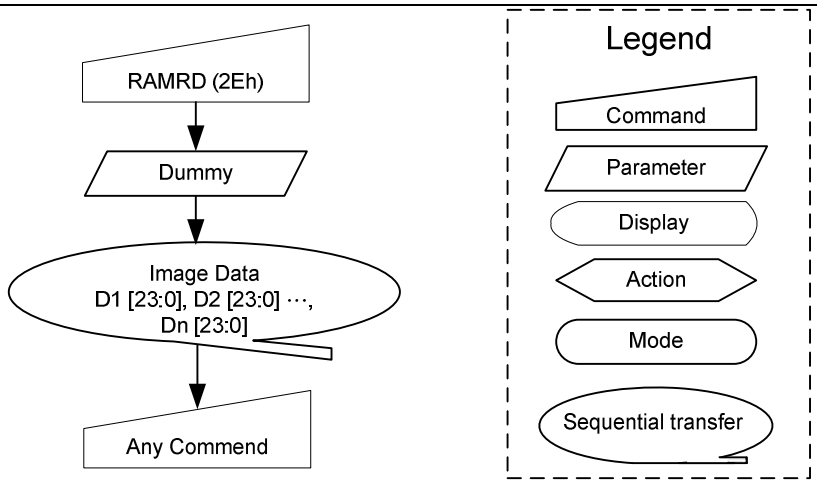
Flow Chart	

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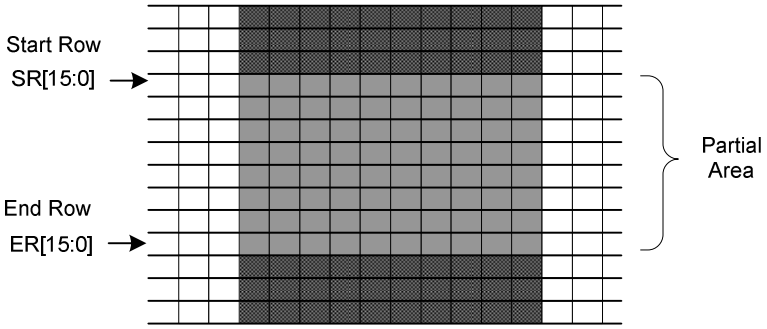
5.2.26. Partial Area (30h)

30h	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR [15:8]								XX
2nd Parameter	1	1	↑	XX	SR [7:0]								XX
3rd Parameter	1	1	↑	XX	ER [15:8]								XX
4th Parameter	1	1	↑	XX	ER [7:0]								XX

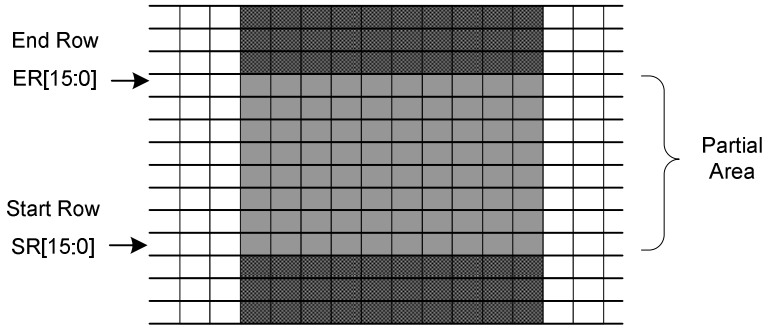
Description

This command defines the Partial Display mode's display area. There are two parameters associated with this command: the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory

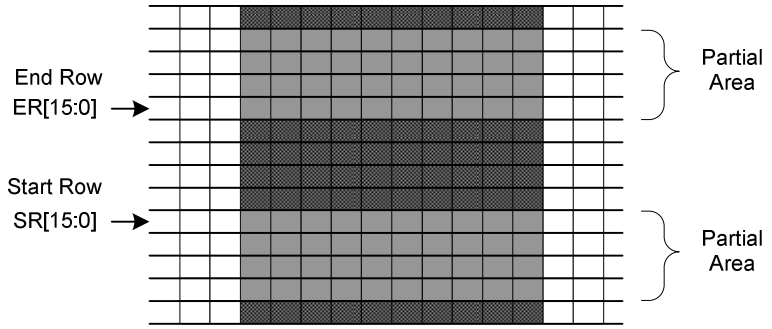
If End Row > Start Row when MADCTL (36h) D4 = 0:



If End Row > Start Row when MADCTL (36h) D4 = 1:



If End Row < Start Row when MADCTL (36h) D4 = 0:



If End Row = Start Row, then the Partial Area will be one row deep.

X = void

Restriction

SR [15:0] and ER [15:0] cannot be 0000h or exceed the last vertical line number (01EFh).

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Register Availability

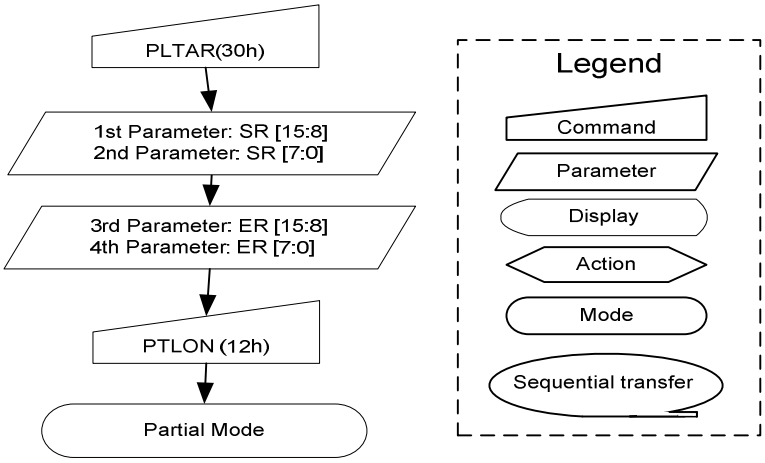
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

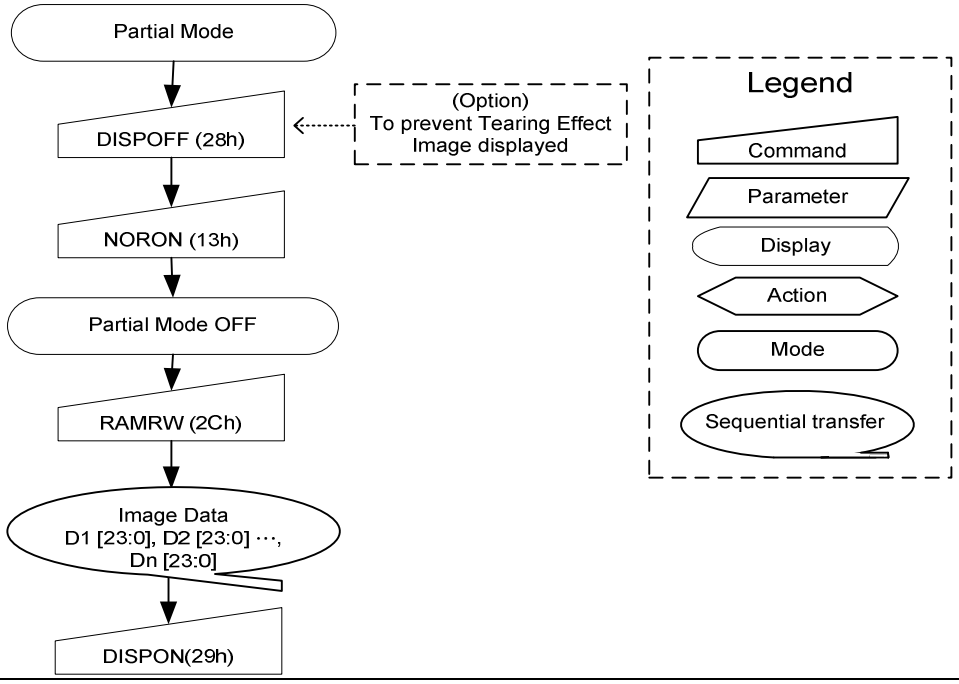
Status	Default Value	
Power On Sequence	SR [15:0] = 0000_{HEX}	ER [15:0] = $01DF_{HEX}$
SW Reset	SR [15:0] = 0000_{HEX}	ER [15:0] = $01DF_{HEX}$
HW Reset	SR [15:0] = 0000_{HEX}	ER [15:0] = $01DF_{HEX}$

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



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5.2.27. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								XX
2nd Parameter	1	1	↑	XX	TFA [7:0]								XX
3rd Parameter	1	1	↑	XX	VSA [15:8]								XX
4th Parameter	1	1	↑	XX	VSA [7:0]								XX
5th Parameter	1	1	↑	XX	BFA [15:8]								XX
6th Parameter	1	1	↑	XX	BFA [7:0]								XX

Description

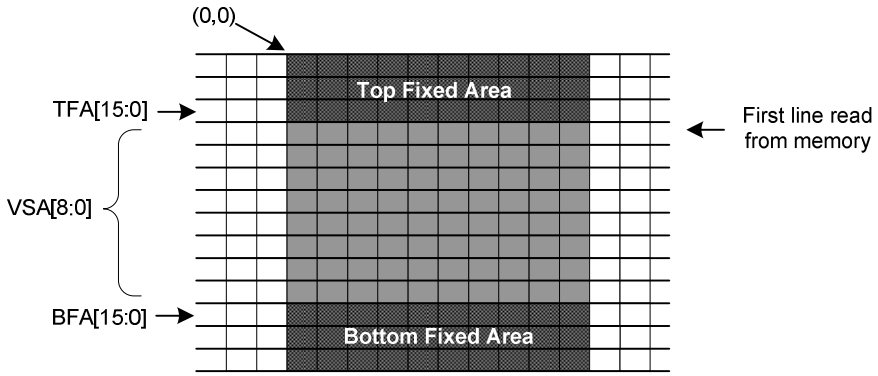
This command defines the display vertical scrolling area.

Memory Access Control (36h) D4 = 0:

The 1st and 2nd parameter, TFA [8:0], describe the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd and 4th parameter, VSA [8:0], describe the height of the Vertical Scrolling Area in number of lines of the frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th and 6th parameter, BFA [8:0], describe the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

TFA, VSA, and BFA refer to the Frame Memory Line Pointer.



Memory Access Control (36h) D4 = 1:

The 1st and 2nd parameter, TFA [8:0], describe the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

The 3rd and 4th parameter, VSA [8:0], describe the height of the Vertical Scrolling Area in number of lines of the frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th and 6th parameter, BFA [8:0], describe the Bottom Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned.

TFA, VSA, and BFA refer to the Frame Memory Line Pointer.

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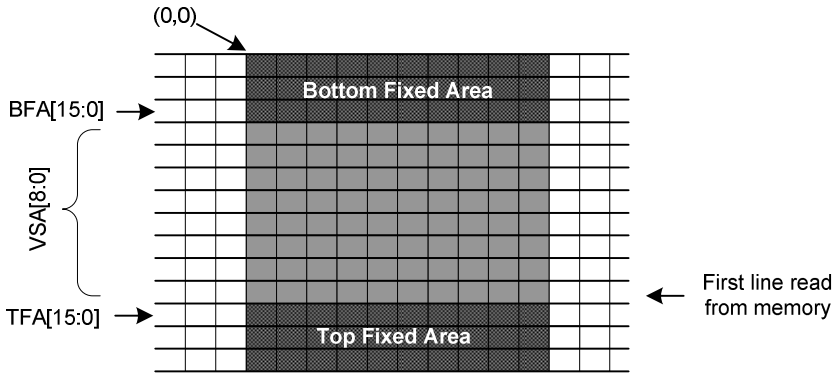
<table>
<tr><td></td><td>


X = void
</td></tr>
<tr><td>Restriction</td><td>The sum of TFA, VSA, and BFA must equal the number of the display device's horizontal lines (pages); otherwise, the Scrolling mode is undefined. In the Vertical Scroll Mode, set_address_mode B5 should be set to 0 – this only affects the Frame Memory Write.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="3">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>TFA [15:0] = 0000_{HEX}</td><td>VSA [15:0] = $01E0_{HEX}$</td><td>BFA [15:0] = 0000_{HEX}</td></tr>
<tr><td>SW Reset</td><td>TFA [15:0] = 0000_{HEX}</td><td>VSA [15:0] = $01E0_{HEX}$</td><td>BFA [15:0] = 0000_{HEX}</td></tr>
<tr><td>HW Reset</td><td>TFA [15:0] = 0000_{HEX}</td><td>VSA [15:0] = $01E0_{HEX}$</td><td>BFA [15:0] = 0000_{HEX}</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>1. To enter the Vertical Scroll Mode:</td></tr>
</table>

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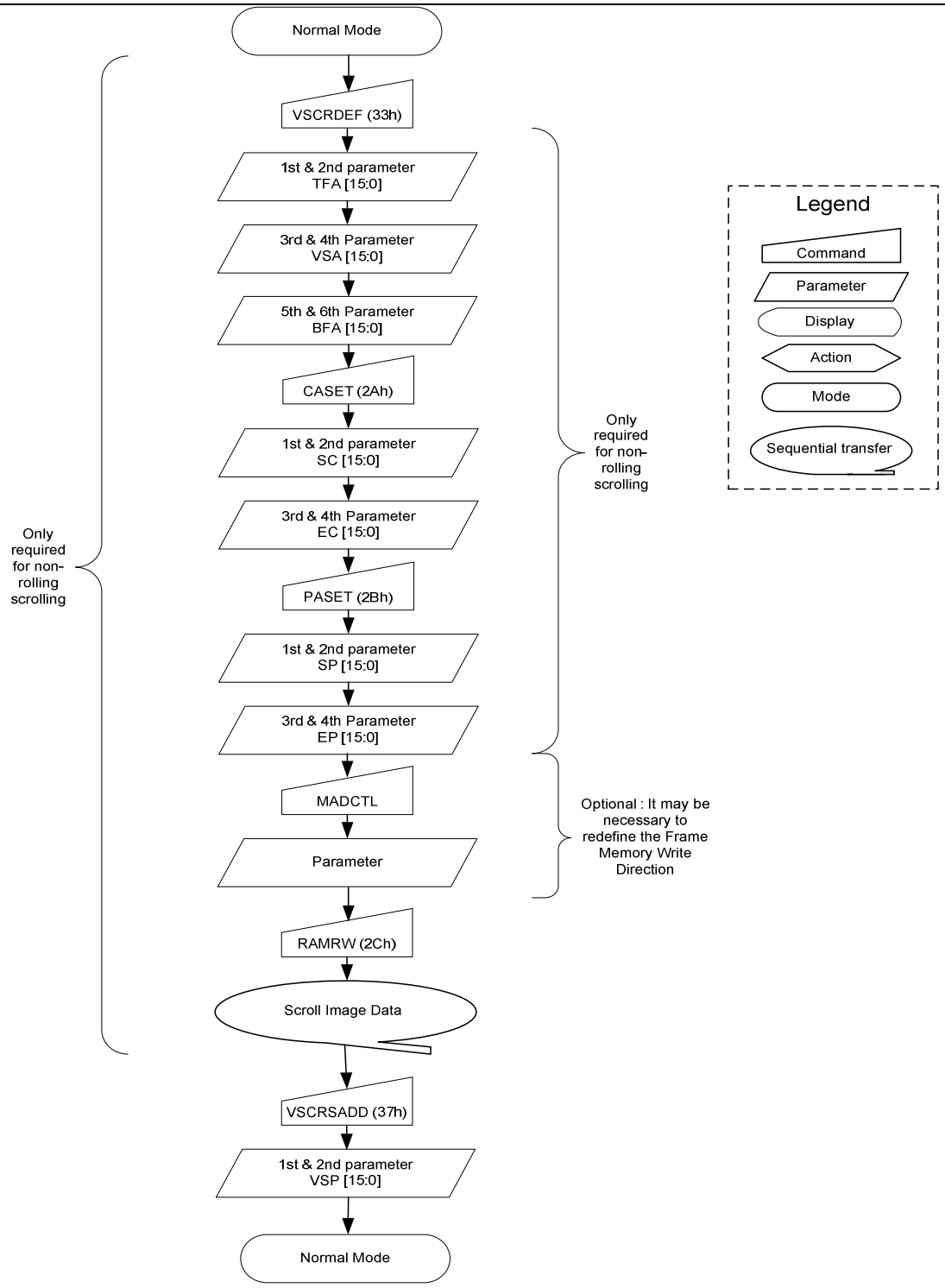

Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise, an undesirable image may appear on the Display Panel.

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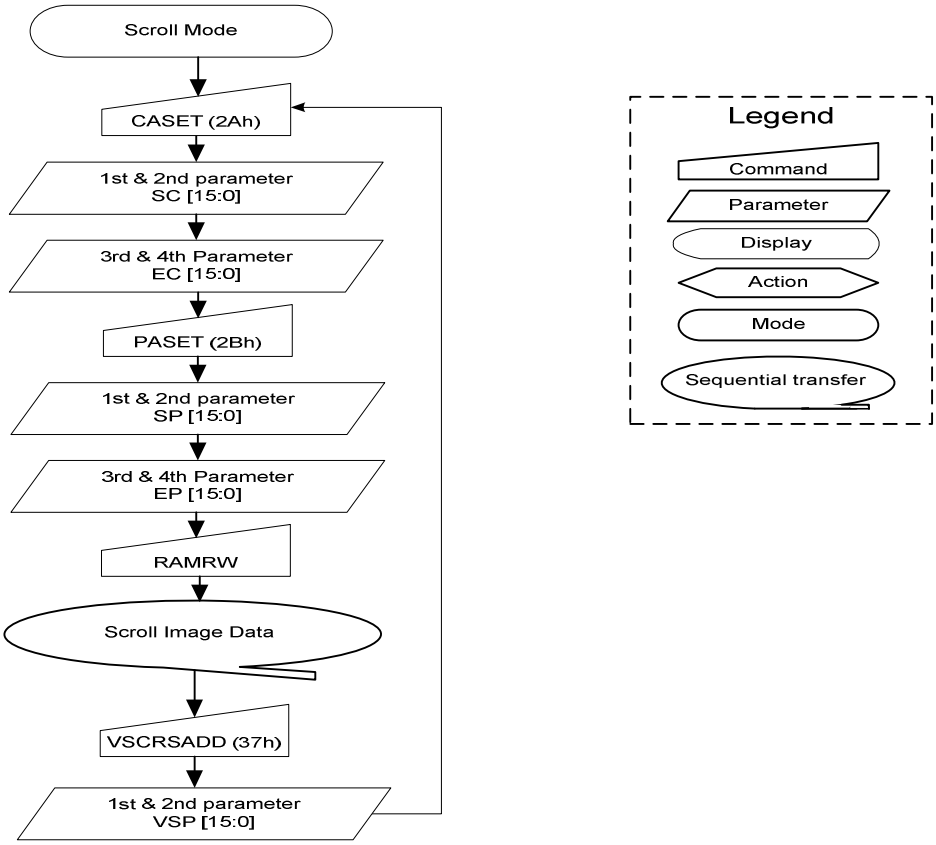
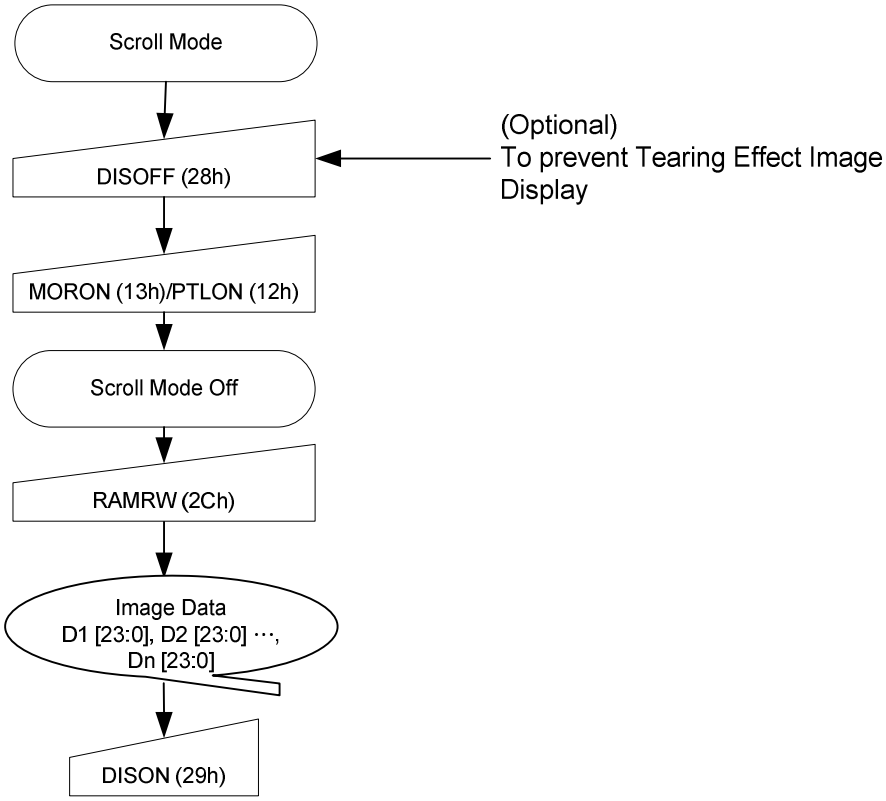
2. Continuous Scroll:



3. To Leave the Vertical Scroll Mode:



Note: To exit the Scroll Mode, both Normal Display Mode On (13h) and Partial Mode On (12h) commands can be used.

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5.2.28. Tearing Effect Line OFF (34h)

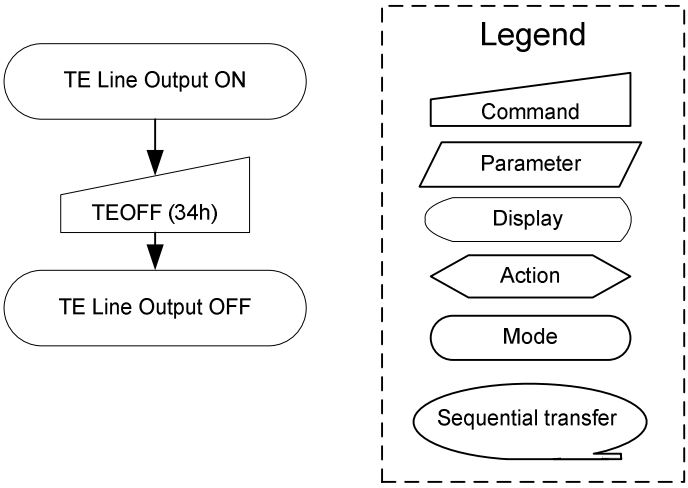
34h	TEOFF (Tearing Effect Line OFF)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
1st Parameter	No parameter												
Description	This command turns off the ILI9488's Tearing Effect output signal on the TE signal line. X = void												
Restriction	This command has no effect when the Tearing Effect output is already Off.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



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5.2.29. Tearing Effect Line ON (35h)

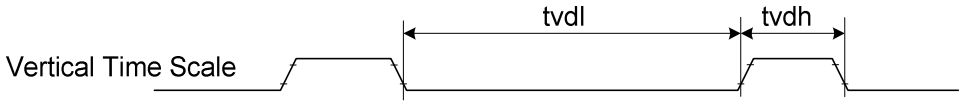
35h	TEOFF (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	M	XX

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. Changing the MADCTL bit D4 will not affect this output. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.

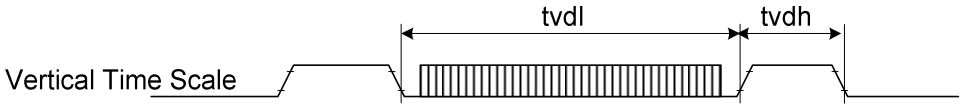
When **M = 0**:

The Tearing Effect Output line consists of V-Blanking information only:



When **M = 1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information：



Note: During the Sleep In Mode with the Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = void

Restriction

This command has no effect when the Tearing Effect output is already off.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

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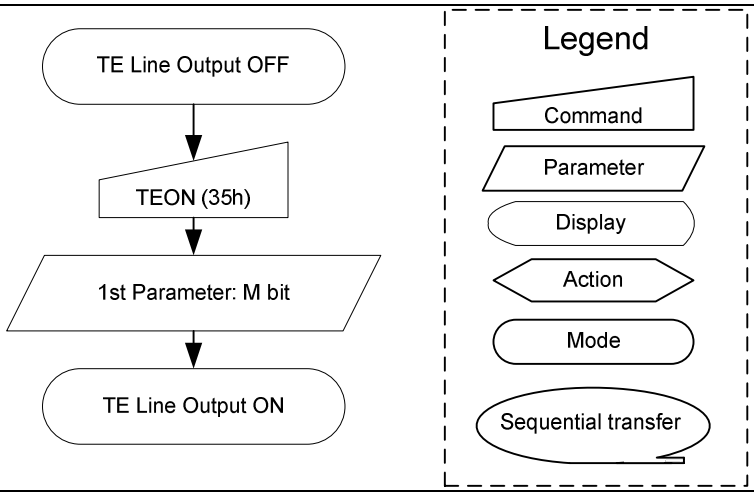
Flow Chart	

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5.2.30. Memory Access Control (36h)

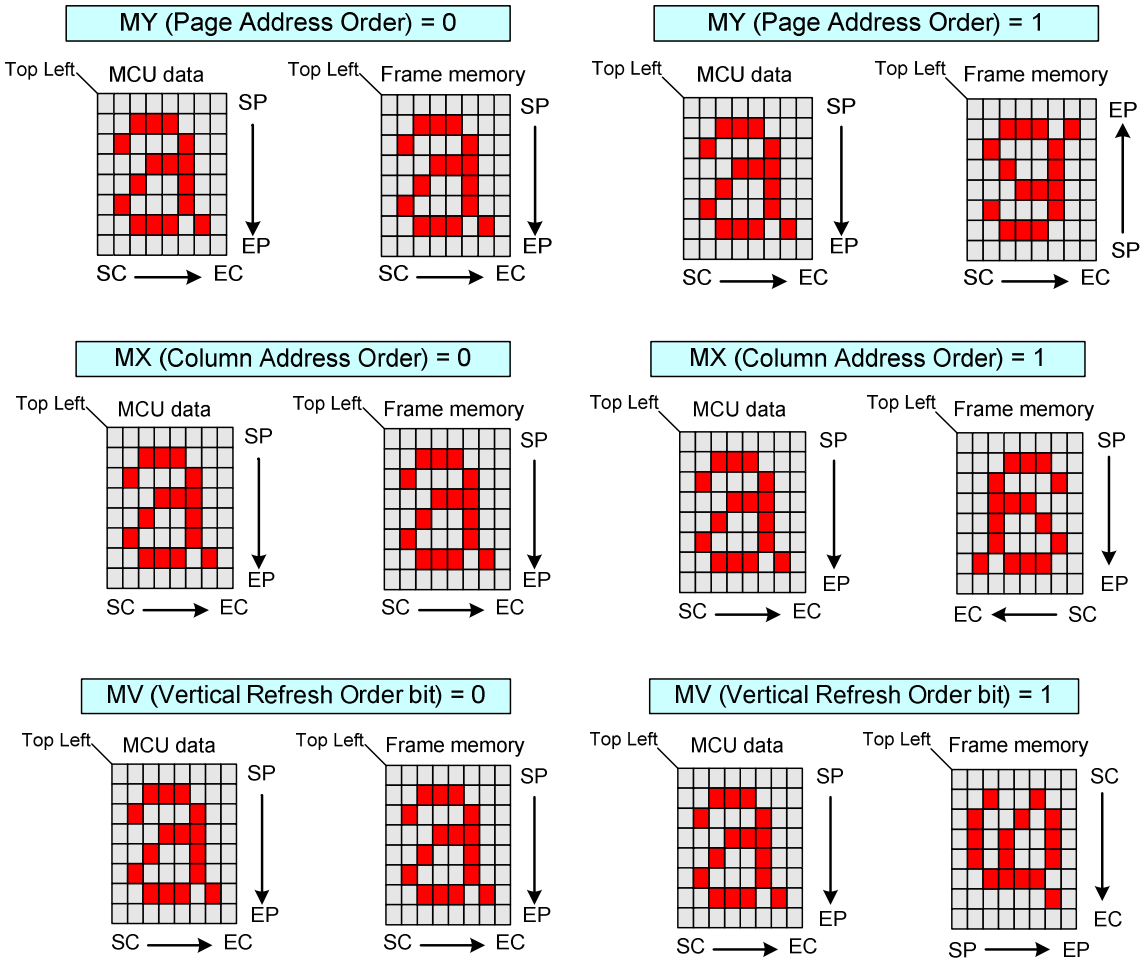
36h	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
1st Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	XX

Description

This command defines read/write scanning direction of the frame memory.

This command makes no change on other driver status.

Bit	Symbol	Name	Description
D7	MY	Row Address Order	These 3 bits control the direction from the MPU to memory write/read.
D6	MX	Column Address Order	
D5	MV	Row/Column Exchange	
D4	ML	Vertical Refresh Order	LCD vertical refresh direction control.
D3	BGR	RGB-BGR Order	Color selector switch control (0 = RGB color filter panel, 1 = BGR color filter panel)
D2	MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.
D1	X	Reserved	Reserved
D0	X	Reserved	Reserved



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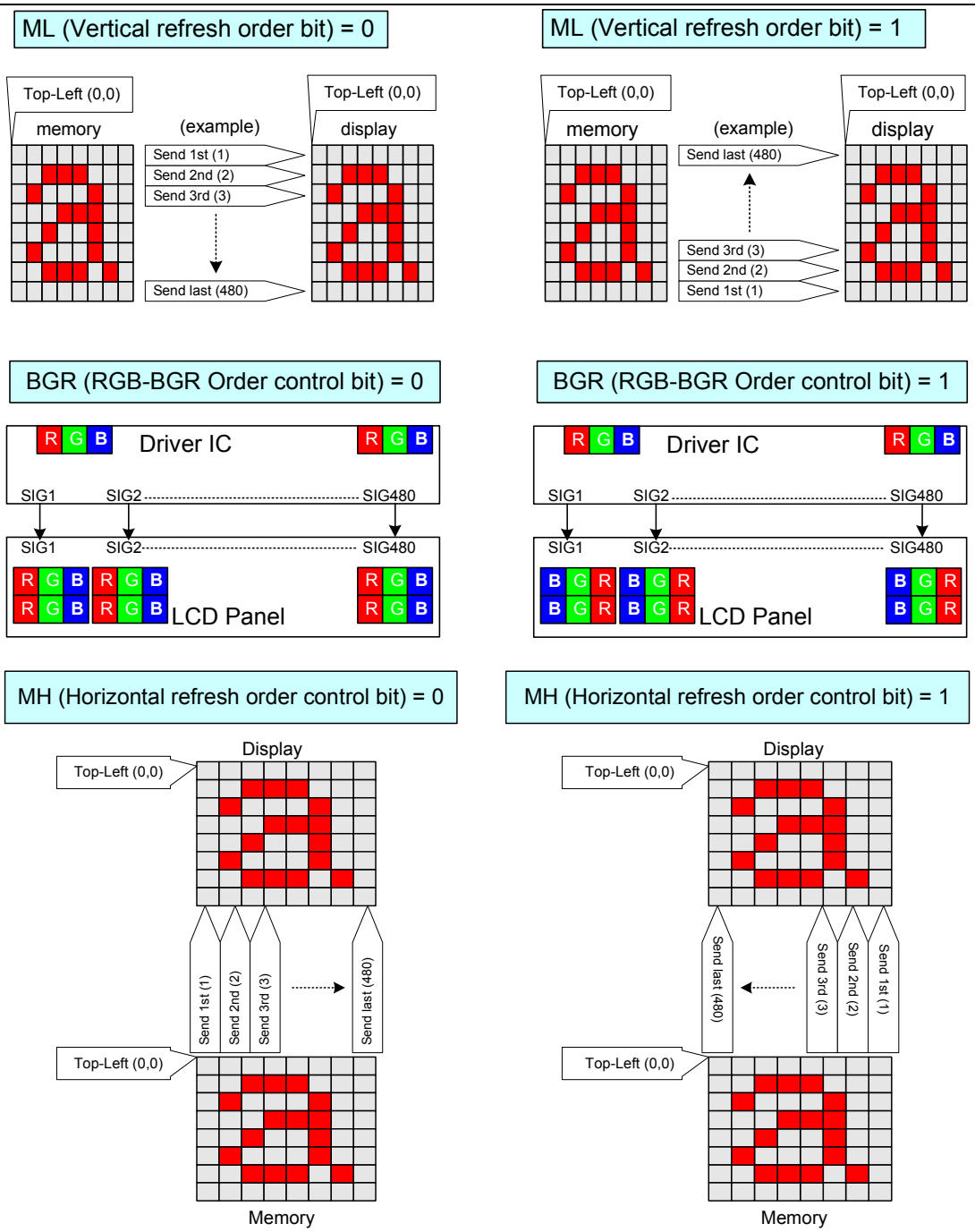

Note: Top-Left (0,0) represents the physical memory location.

X = void

Restriction	

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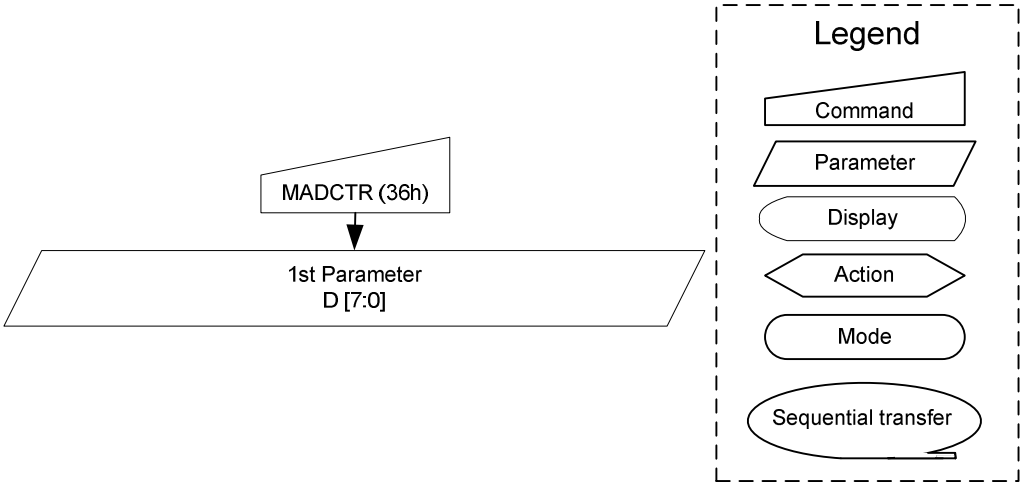
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



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5.2.31. Vertical Scrolling Start Address (37h)

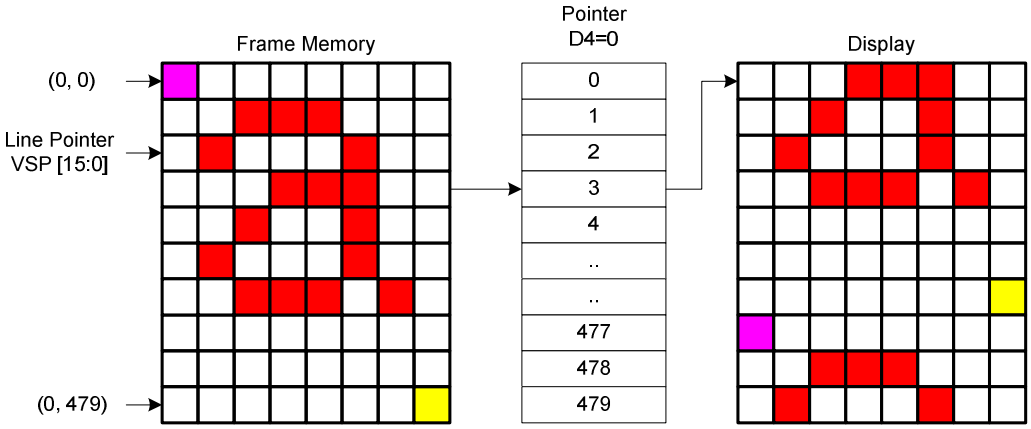
37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	XX	VSP [15:8]								XX
2nd Parameter	1	1	↑	XX	VSP [7:0]								XX

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display, as illustrated below:

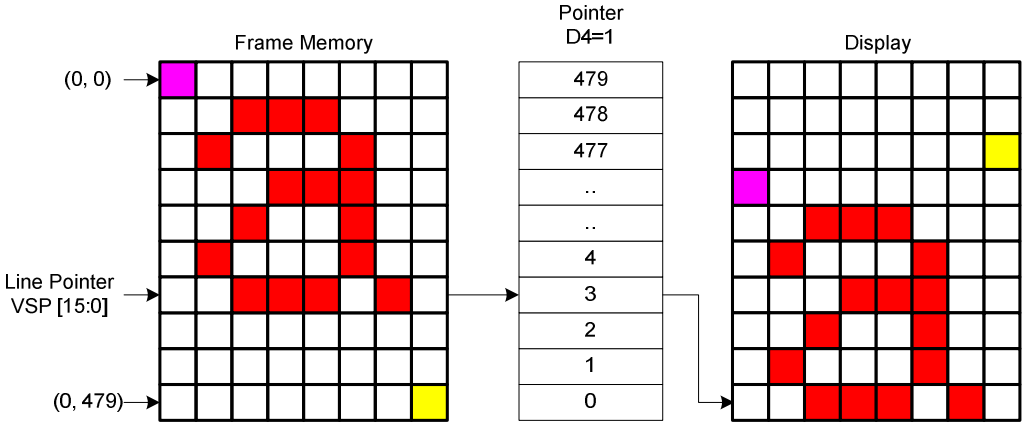
When MADCTL(36h) D4 = 0

Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480, and VSP = 3



When MADCTL(36h) D4 = 1

Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480, and VSP = 3



Note: When the new Pointer position and Picture Data are sent, the result on the display will appear at the next Panel Scan to avoid tearing effect.

VSP refers to the Frame Memory line Pointer.

X = void

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) . Otherwise, undesirable image will occur on the Panel.

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<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

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5.2.32. Idle Mode OFF (38h)

38h	IDMOFF (Idle Mode OFF)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
1st Parameter	No parameter												
Description	This command causes the ILI9488 to exit the Idle mode. In the Idle Mode OFF, the display panel can display a maximum of 262,144 colors. X = void												
Restriction	This command has no effect when the ILI9488 is not in the Idle mode.												

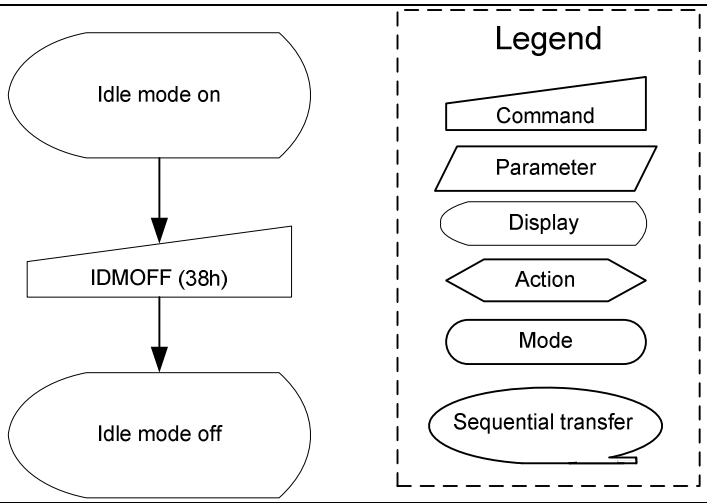
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



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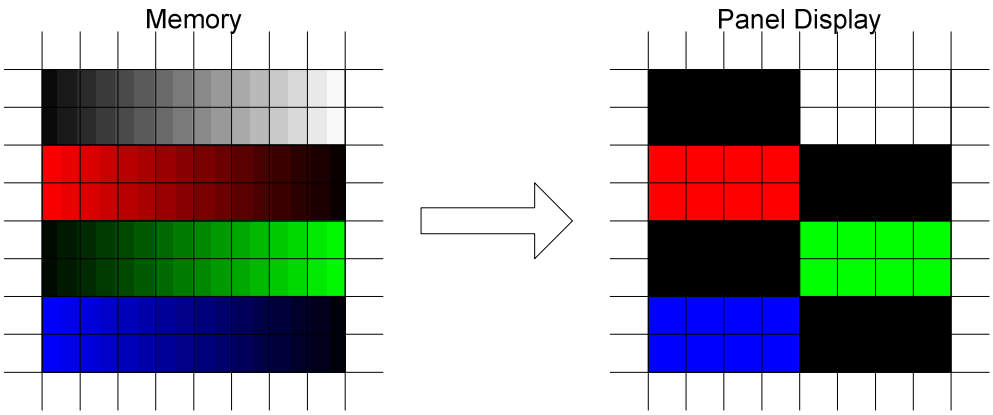
5.2.33. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
1st Parameter	No parameter												

Description

This command is used to enter the Idle Mode On.

In the Idle Mode On, color expression is reduced. The first bits of R, G, and B in the Frame Memory will determine the display color, as shown in the table below.



Memory Contents vs. Display Color			
	R_5 R_4 R_3 R_2 R_1 R_0	G_5 G_4 G_3 G_2 G_1 G_0	B_5 B_4 B_3 B_2 B_1 B_0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = void

Restriction

This command has no effect when the module is already in the Idle Off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

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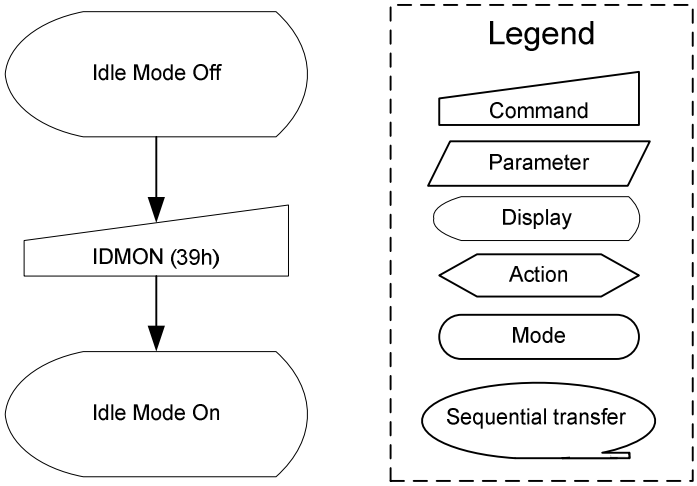
Flow Chart	

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5.2.34. Interface Pixel Format (3Ah)

3Ah	COLMOD (Interface Pixel Format)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
1st Parameter	1	1	↑	XX	X	DPI [2:0]			X	DBI [2:0]			XX

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format selector of the RGB interface, and DBI [2:0] is the pixel format of the MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [2:0]			RGB Interface Format	DBI [2:0]			MCU Interface Format
0	0	0	Reserved	0	0	0	Reserved
0	0	1	Reserved	0	0	1	3 bits/pixel (8 color)
0	1	0	Reserved	0	1	0	Reserved
0	1	1	Reserved	0	1	1	Reserved
1	0	0	Reserved	1	0	0	Reserved
1	0	1	16 bits/pixel	1	0	1	16 bits / pixel
1	1	0	18 bits/pixel	1	1	0	18 bits / pixel
1	1	1	24 bits/pixel	1	1	1	24 bits / pixel

X = void

Restriction

Register Availability

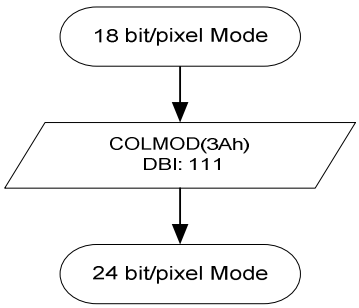
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

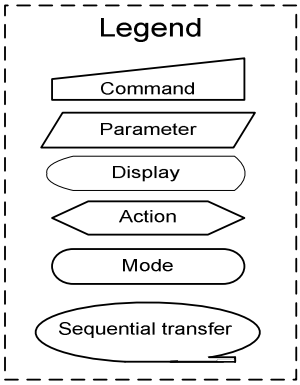
Default

Status	Default Value
Power On Sequence	06h
SW Reset	06h
HW Reset	06h

Flow Chart

Example :





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5.2.35. Memory Write Continue (3Ch)

3Ch	RAMWRC (Memory Write Continue)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	D1 [23:0]									XX
:	1	1	↑	Dx [23:0]									XX
Nth Parameter	1	1	↑	Dn [23:0]									XX

Description

This command is used to transfer data from the MCU to the frame memory if the frame memory wants to continue memory write after the "Memory Write (2Ch)" command.

This command makes no change to the other driver status.

When this command is accepted, the column register and the page register will not reset to the Start Column/Start Page positions as it has been done by the "Memory Write (2Ch)" command.

Then D [23:0] is stored in the frame memory and the column register and the page register incremented as the table below:

Column and Page Counter Control.

Condition	Column counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to Start Column	Return to Start Page
Complete Pixel Read/Write action	Incremented by 1	No change
The Column counter value is large than the End Column	Return to Start Column	Incremented by 1
The Page counter value is large than the End Page	Return to Start Column	Return to Start Page

Sending any other command can stop the Frame Write.

X = void

Restriction

There is no restriction on the length of parameters.

No access to the frame memory in the Sleep In mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

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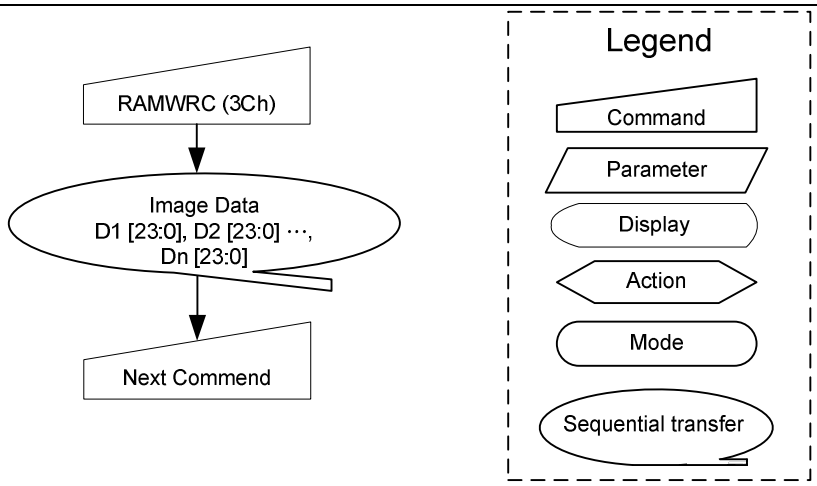
Flow Chart	

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5.2.36. Memory Read Continue (3Eh)

3Eh	RAMRDRC (Memory Read Continue)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	D1 [23:0]									XX
:	1	↑	1	Dx [23:0]									XX
Nth Parameter	1	↑	1	Dn [23:0]									XX

Description

This command is used to transfer data from the frame memory to the MCU, if the MCU wants to continue memory read after "Memory Read (2Eh)" command.

This command makes no change to the other driver status.

When this command is accepted, the column register and the page register will not reset to the Start Column/Start Page positions as it has been done by the "Memory Read (2Eh)" command.

Then D [23:0] is read back from the frame memory, and the column register and the page register are incremented as shown in the table below: Column and Page Counter Control.

Condition	Column counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column"	Return to "Start Page"
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is large than "End Column"	Return to "Start Column"	Increment by 1
The Page counter value is large than "End Page"	Return to "Start Column"	Return to "Start Page"

Frame Read can be stopped by sending any other command.

X = void

Restriction

There is no restriction on the length of parameters.

No access to the frame memory in the Sleep In mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

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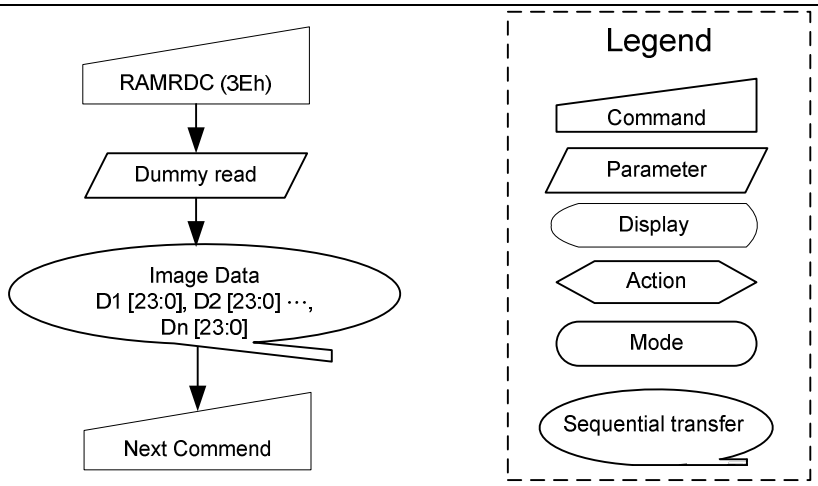
Flow Chart	

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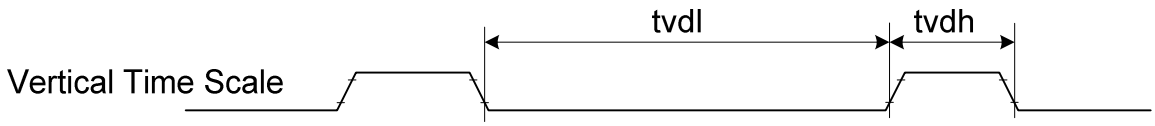
5.2.37. Write Tear Scan Line (44h)

44h	TESLWR (Write Tear Scan Line)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	XX	N [15:8]								XX
2nd Parameter	1	1	↑	XX	N [7:0]								XX

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. Changing Memory Access Control (36h) D4 will not affect the TE signal. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.



Note that set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.

The Tearing Effect Output line shall be active low when the ILI9488 is in the Sleep mode.

X = void

Restriction

This command has no effect when the Tearing Effect output is already ON.

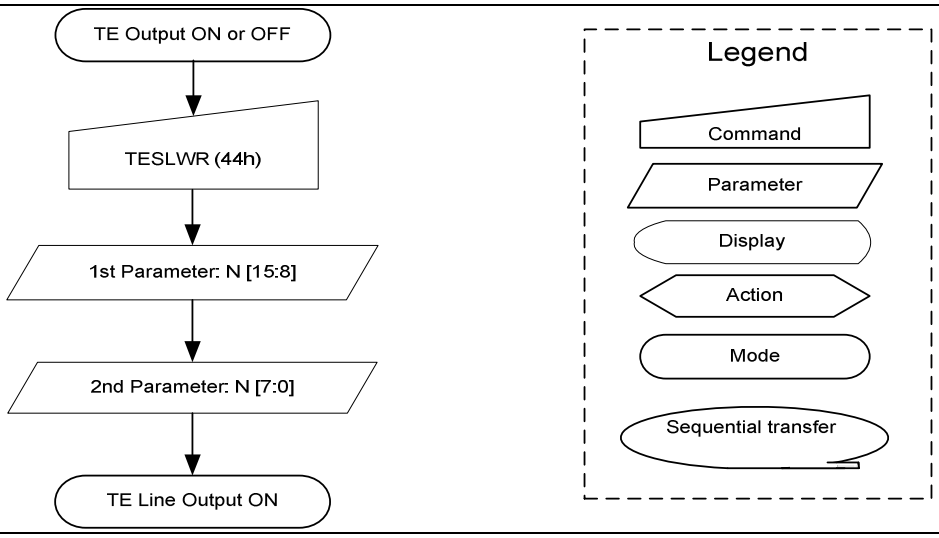
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No change
HW Reset	00h

Flow Chart



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5.2.38. Read Scan Line (45h)

45h	TESLRD (Read Tear Scan Line)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	N [15:8]								XX
3rd Parameter	1	↑	1	XX	N [7:0]								XX

Description

The display reads the current scan line N, used to update the display device. The total number of scan lines on a display device is defined as: V_Low + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.

When in the Sleep Mode, the value returned by Read Scan Line command is undefined.

X = void

Restriction

None

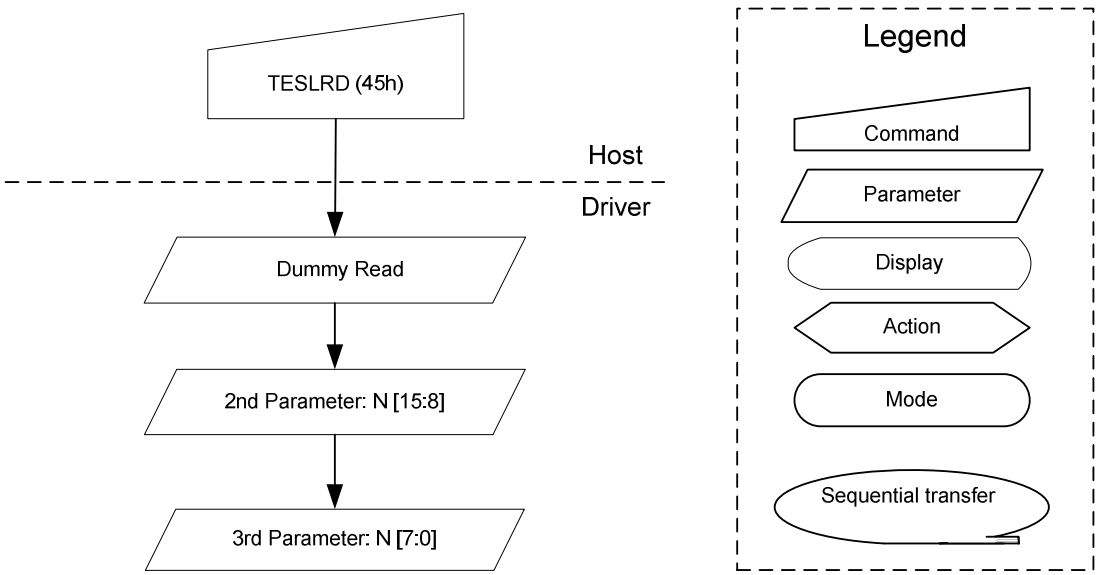
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No change
HW Reset	00h

Flow Chart



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5.2.39. Write Display Brightness Value (51h)

51h	WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
1st Parameter	1	1	↑	XX	DBV [7:0]								XX

Description

This command is used to adjust the brightness value of the display.

DBV [7:0]: 8 bit, for display brightness of the manual brightness setting and the CABC in the ILI9488. PWM output signal and PWM_OUT pin control the LED driver IC in order to control the display brightness.

In principle, 00h value means the lowest brightness and FFh value means the highest brightness.

X = void

Restriction

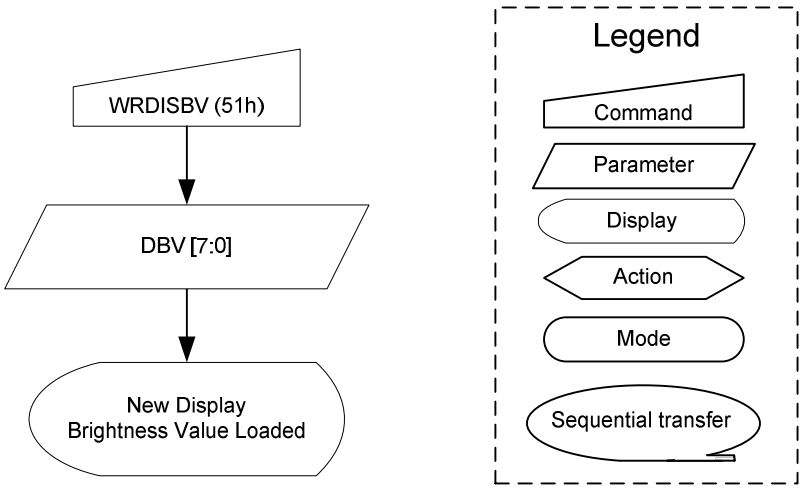
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
SW Reset	No Change
H/W Reset	00h

Flow Chart



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5.2.40. Read Display Brightness Value (52h)

52h	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	DBV [7:0]								XX

Description

This command is used to return the brightness value of the display.

DBV [7:0] is reset when the display is in the Sleep In mode.

DBV [7:0] is 0 when the bit BCTRL of Write CTRL Display (53h) command is 0.

DBV [7:0] is the manual set brightness specified by the Write CTRL Display (53h) command when the BCTRL bit is 1.

When the bit BCTRL of Write CTRL Display (53h) command is 1 and C1/C0 bit of Write Content Adaptive Brightness Control (55h) command are 0, DBV [7:0] output is the brightness value specified by the Write Display Brightness (51h) command.

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

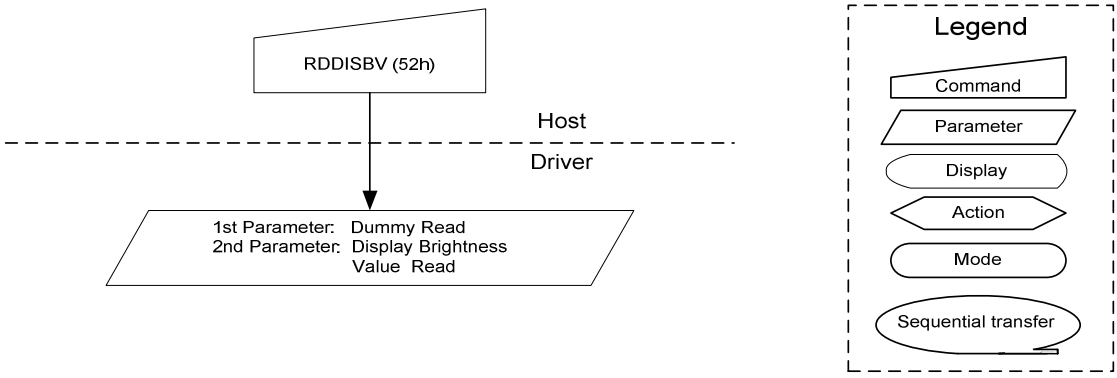
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
SW Reset	No Change
H/W Reset	00h

Flow Chart



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5.2.41. Write CTRL Display Value (53h)

53h	WRCTRLD (Write Control Display)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
1st Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	XX

Description

This command is used to control the display brightness.

BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV [7:0] = 00h)
1	Brightness Control Block ON (DBV [7:0] is active)

DD: Display Dimming Control. This function is only for the manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD = 1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When the BL bit changes from On to Off, backlight is turned off without gradual dimming, even if dimming-on (DD = 1) are selected.

X = void

Restriction

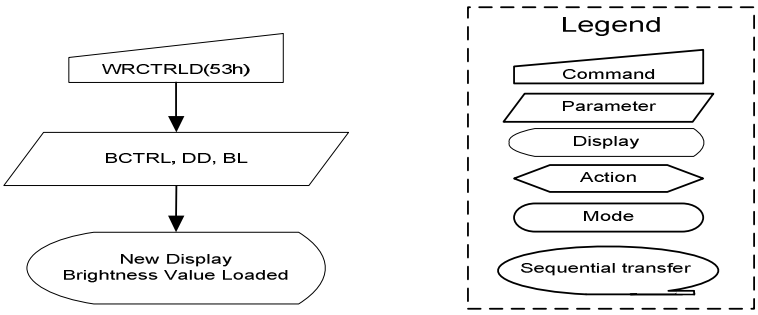
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
SW Reset	No Change
H/W Reset	00h

Flow Chart



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5.2.42. Read CTRL Display Value (54h)

54h	RDCTRLD (Read Control Display Value)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	XX

Description

This command is used to control the display brightness.

BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV [7:0] = 00h)
1	Brightness Control Block ON (DBV [7:0] is active)

DD: Display Dimming Control. This function is only for the manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

X = void

Restriction

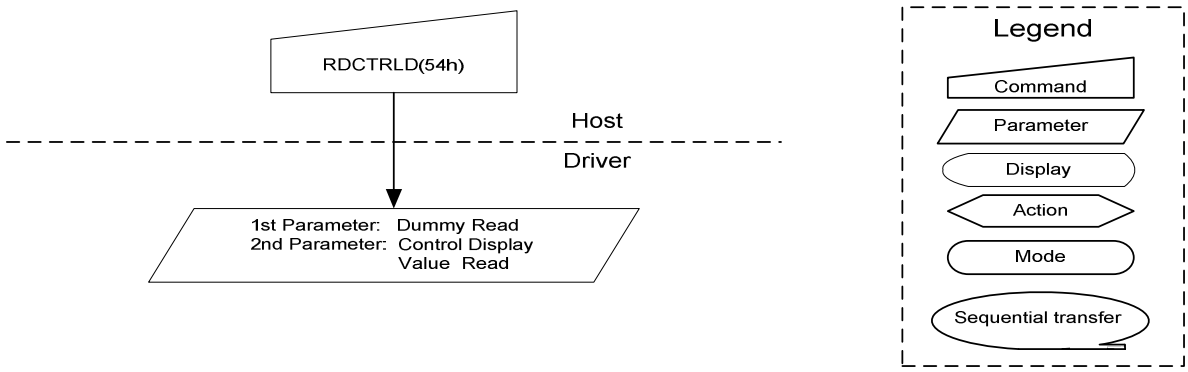
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
SW Reset	No Change
H/W Reset	00h

Flow Chart



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5.2.43. Write Content Adaptive Brightness Control Value (55h)

55h	WRCABC (Write Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
1st Parameter	1	1	↑	XX	C [7:0]								XX

Description

This command is used to set parameters of image content based on the adaptive brightness control functionality.

The first 4 different modes are for content adaptive image functionality, which are defined in the table below.

C [7:0]								Description	CE Ratio Range
0	0	0	0	0	0	0	0	OFF	-
0	0	0	0	0	0	0	1	User Interface Image	-
0	0	0	0	0	0	1	0	Still Picture	-
0	0	0	0	0	0	1	1	Moving Image	-
1	0	0	0	0	0	0	0	Low enhancement	1.250
1	0	0	1	0	0	0	0	Medium enhancement	1.750
1	0	1	1	0	0	0	0	High enhancement	2.250

X = void

Restriction

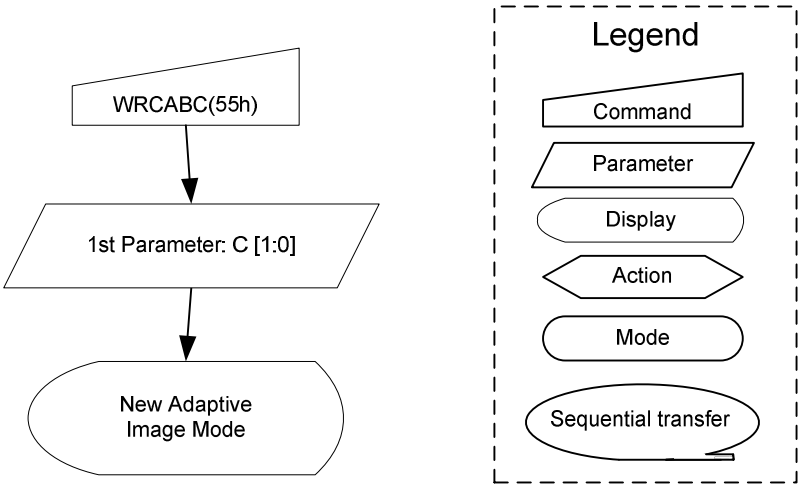
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
SW Reset	No Change
H/W Reset	00h

Flow Chart



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5.2.44. Read Content Adaptive Brightness Control Value (56h)

56h	RDCABC (Read Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	C [7:0]								XX

Description

This command is used to read the settings of image content based on the adaptive brightness control functionality. The first 4 different modes are for the content adaptive image functionality, which are defined in the table below.

C [7:0]								Description	CE Ratio Range
0	0	0	0	0	0	0	0	OFF	-
0	0	0	0	0	0	0	1	User Interface Image	-
0	0	0	0	0	0	1	0	Still Picture	-
0	0	0	0	0	0	1	1	Moving Image	-
1	0	0	0	0	0	0	0	Low enhancment	1.250
1	0	0	1	0	0	0	0	Medium enhancement	1.750
1	0	1	1	0	0	0	0	High enhancement	2.250

X = void

Restriction

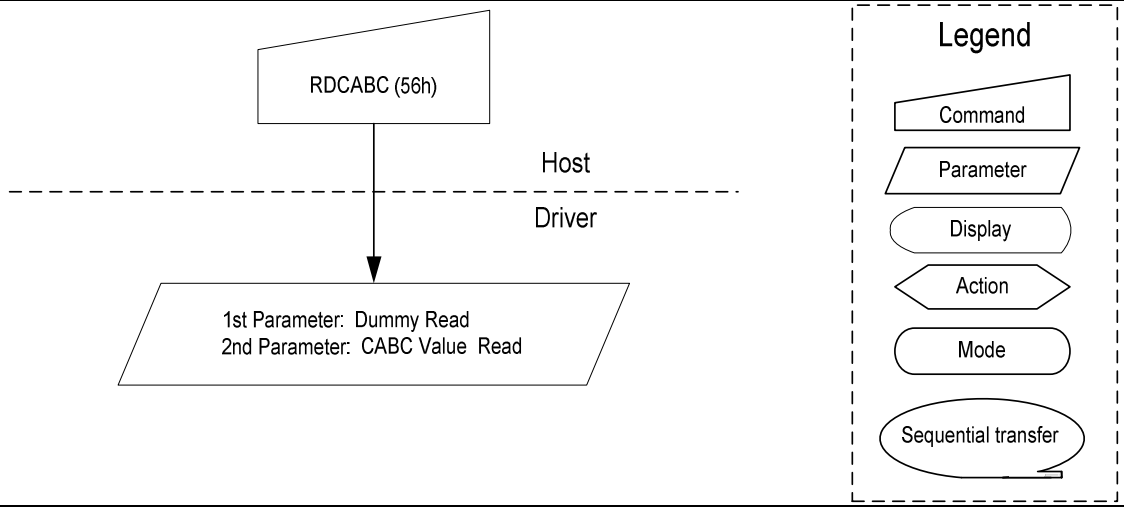
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
SW Reset	No Change
H/W Reset	00h

Flow Chart



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5.2.45. Write CABC Minimum Brightness (5Eh)

5Eh	WRCABCMB (Write CABC Minimum Brightness)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
1st Parameter	1	1	↑	XX	CMB [7:0]								XX

Description

This command is used to set the minimum brightness value of the display for the CABC function.

CMB [7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When the CABC is active, it cannot reduce the display brightness to less than the CABC minimum brightness setting. Image processing function works normally, even if the brightness cannot be changed.

This manual brightness setting does not affect other functions. Manual brightness can set the display brightness to less than the CABC minimum brightness. Smooth transition and dimming function can work normally.

When display brightness is turned off (BCTRL = 0 of Write CTRL Display (53h)), the CABC minimum brightness setting is ignored.

In principle, 00h value means the lowest brightness for CABC, and FFh value means the highest brightness for CABC.

X = void

Restriction

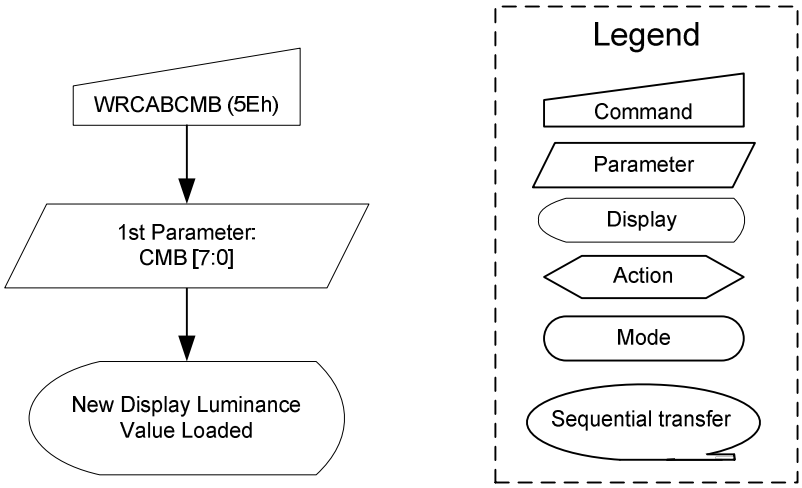
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
SW Reset	No Change
H/W Reset	00h

Flow Chart



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5.2.46. Read CABC Minimum Brightness (5Fh)

5Fh	RDCABCMB (Read CABC Minimum Brightness)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	CMB [7:0]								XX

Description

This command reads the minimum brightness value of the CABC function.

In principle, 00h value means the lowest brightness and FFh value means the highest brightness.

CMB [7:0] is the CABC minimum brightness specified by the Write CABC minimum brightness (5Eh) command.

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

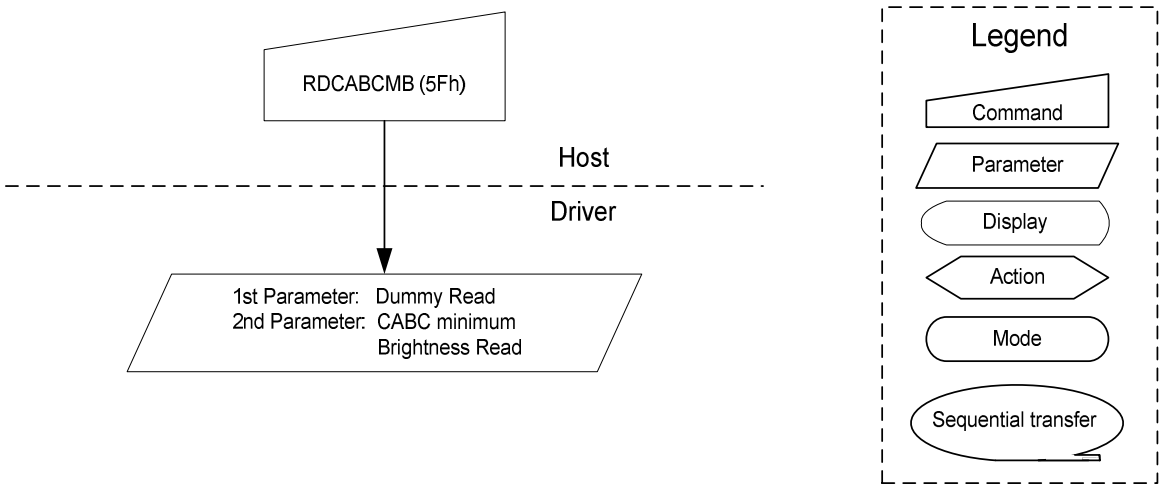
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
SW Reset	No Change
H/W Reset	00h

Flow Chart



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5.2.47. Read Automatic Brightness Control Self-diagnostic Result (68h)

68h	RDABCSDR (Read automatic brightness control self-diagnostic result)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	1	0	0	0	68h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	D [7:6]		0	0	0	0	0	0	XX

Description

This command indicates the status of the display self-diagnostic results for automatic brightness control after the Sleep Out command, as described in the table below.

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly
D6	Functionality Detection	Invert the D6 bit if the display is working

Bit D7 – Register Loading Detection, see the section “Register loading Detection ”.

Bit D6 – Functionality Detection, see the section “Functionality Detection “.

Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to 0.

X = void

Restriction

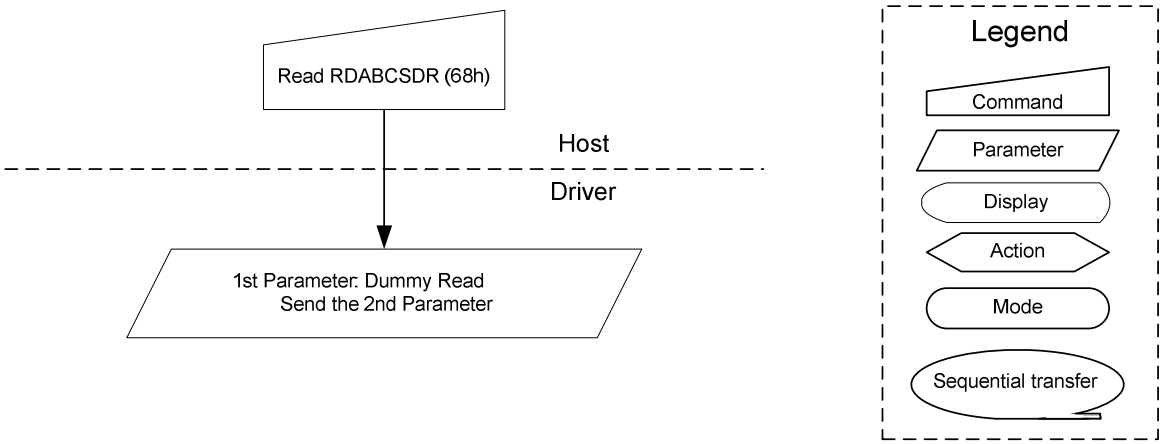
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.2.48. Read ID1 (DAh)

DAh	RDID1 (Read ID1)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	ID1 [7:0]								XX

Description

This read byte identifies the LCD module's manufacturer ID and it is specified by users.

The 1st parameter is a dummy data.

The 2nd parameter is the LCD module's manufacturer ID.

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

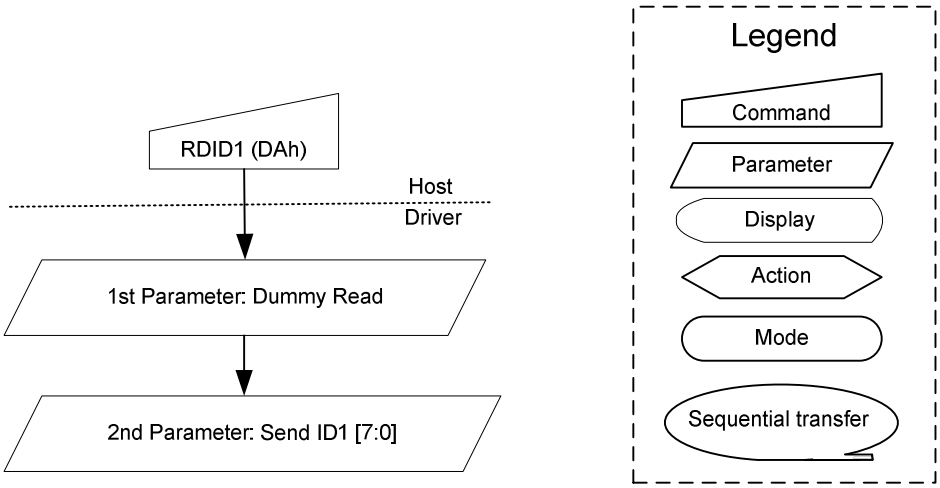
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	54h	OTP value
SW Reset	54h	OTP value
HW Reset	54h	OTP value

Flow Chart



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5.2.49. Read ID2 (DBh)

DBh	RDID2 (Read ID2)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	ID2 [7:0]								XX

Description

This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.

The 1st parameter is a dummy data.

The 2nd parameter is the LCD module/driver version ID, and the ID parameter range is from 80h to FFh.

The ID2 can be programmed by the OTP function.

X = void

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

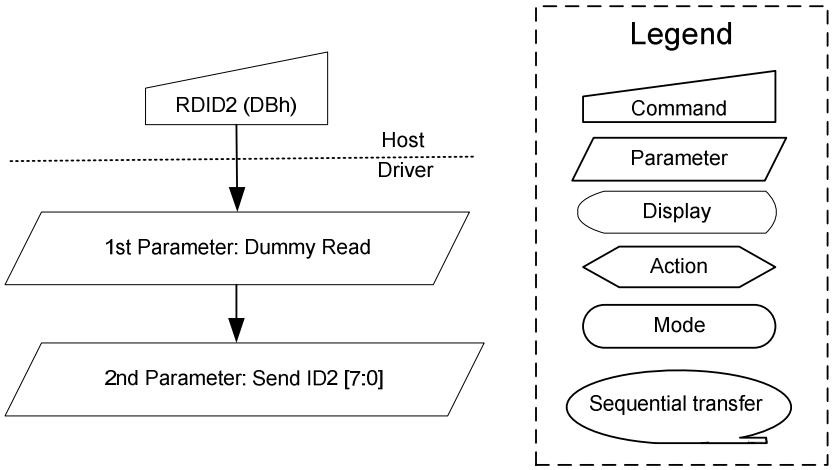
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	80h	OTP value
SW Reset	80h	OTP value
HW Reset	80h	OTP value

Flow Chart



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5.2.50. Read ID3 (DCh)

DCh	RDID3 (Read ID3)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	ID3 [7:0]								XX

Description

This read byte identifies the LCD module/driver, and It is specified by users.

The 1st parameter is a dummy data.

The 2nd parameter is the LCD module/driver ID.

The ID3 can be programmed by the OTP function.

X = Void.

Restriction

The ILI9488 sends the 2nd parameter value to the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MCU interface.

Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.

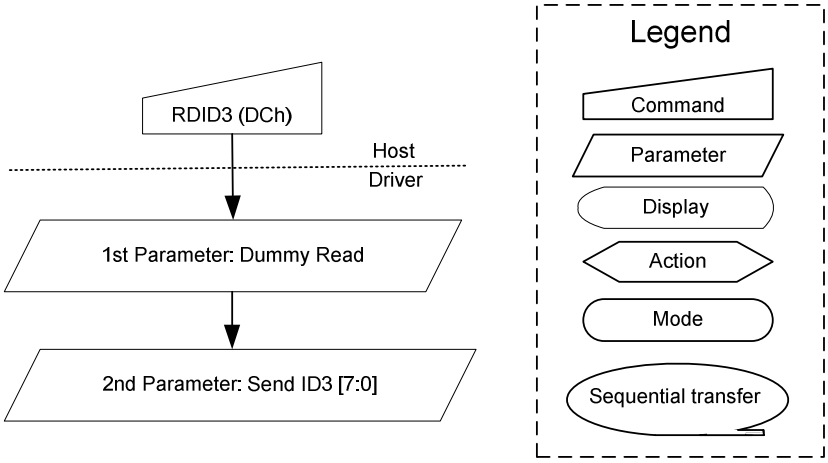
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	66h	OTP value
SW Reset	66h	OTP value
HW Reset	66h	OTP value

Flow Chart



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5.3. Extend Command (EXTC) Description

5.3.1. Interface Mode Control (B0h)

B0h	IFMODE (Interface Mode Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
1st Parameter	1	1	↑	XX	SDA_EN	0	0	0	VSPL	HSPL	DPL	EPL	00h
Description	Set the operation status of the display interface. The setting becomes effective as soon as the command is received. **EPL**: ENABLE polarity (0 = High enable for RGB interface, 1 = Low enable for RGB interface) **DPL**: DOTCLK polarity set (0 = data fetched at the rising time, 1 = data fetched at the falling time) **HSPL**: HSYNC polarity (0 = Low level sync clock, 1 = High level sync clock) **VSPL**: VSYNC polarity (0 = Low level sync clock, 1 = High level sync clock) **SDA_EN:** 3/4 wire serial interface selection SDA_EN = 0, DIN and SDO pins are used for 3/4 wire serial interface. SDA_EN = 1, DIN/SDA pin is used for 3/4 wire serial interface and SDO pin is not used. X = void												

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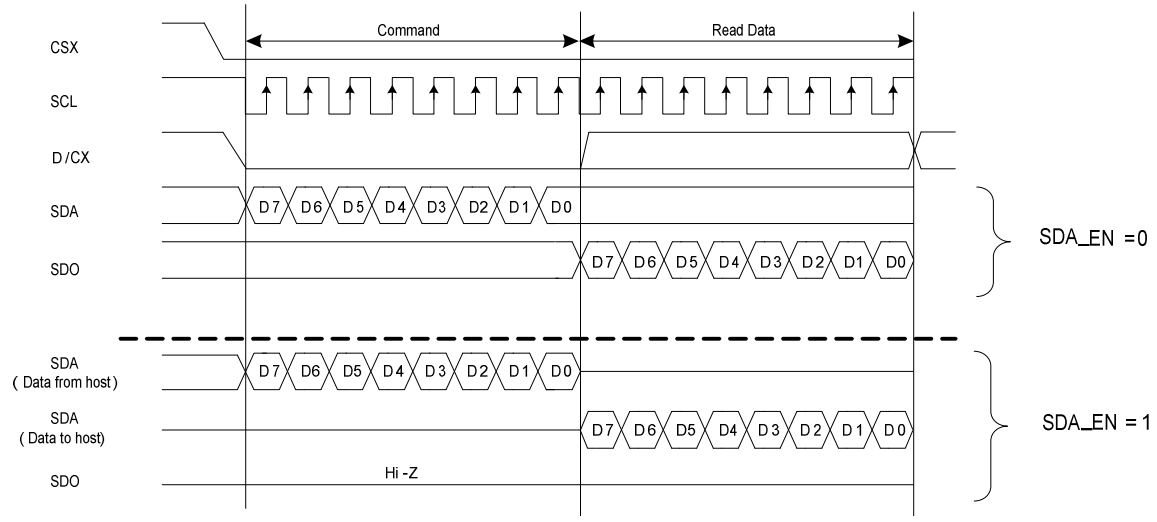

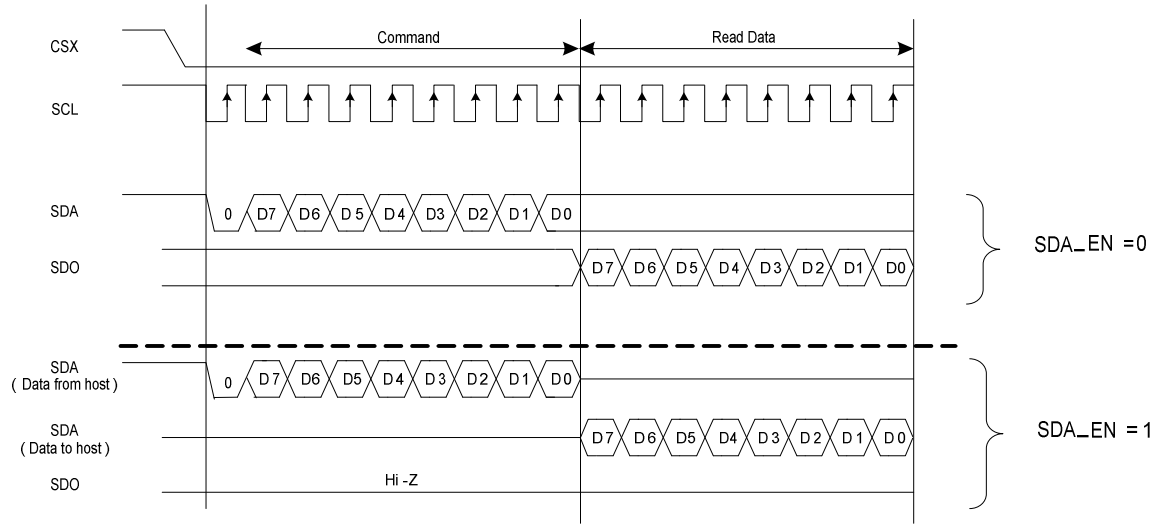

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode/Full colors))												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XX	FRS [3:0]				0	0	DIVA [1:0]		A0h
2nd Parameter	1	1	↑	XX	0	0	0	RTNA [4:0]					11h

Description

DIVA [1:0]: division ratio for internal clocks when Normal mode.

DIVA [1:0]		Division Ratio
0	0	Fosc
0	1	Fosc/2
1	0	Fosc/4
1	1	Ffosc/8

FRS [3:0]: Set the frame frequency of full color normal mode.

Set the division ratio for internal clocks of the Normal Display Mode On

$$\text{Frame Rate}=\frac{\text{Fosc}}{\text{DIVA x ((CNT+1) x 2) x RTNA x (Display Line+VBP+VFP)}}$$

Fosc: Internal oscillator frequence

CNT: Frame rate setting

DIVA: Division Ratio

RTNA: Clocks per line

Display Line: Total driving line number

VBP: Back porch line number

VFP: Front porch line number

FRS [3:0]				CNT	Frame rate(Hz) Tearing Effect Line OFF(R34h)	Frame rate(Hz) Tearing Effect Line ON(R35h) VBP+VFP <24
0	0	0	0	37	28.78	27.64
0	0	0	1	35	30.38	29.17
0	0	1	0	33	32.17	30.89
0	0	1	1	31	34.18	32.82
0	1	0	0	29	36.46	35.01
0	1	0	1	27	39.06	37.51
0	1	1	0	25	42.07	40.40
0	1	1	1	23	45.57	43.76
1	0	0	0	21	49.71	47.74
1	0	0	1	19	54.69	52.52
1	0	1	0	17	60.76	58.35
1	0	1	1	15	68.36	65.65
1	1	0	0	13	78.13	75.03
1	1	0	1	11	91.15	87.53

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Case 1 Tearing Effect Line OFF(R34h)

Example1: Fose=18Mhz, DIVA=1, CNT=17, RTNC=17 clock, Display Line=480 lines, VBP=VFP=2 lines.

Following the formula, the frame rate = 60.76Hz.

Case 2 Tearing Effect Line ON(R35h)

(1) Example1: Fose=18Mhz, DIVA=1, CNT=17, RTNC=17 clock, Display Line=480 lines, VBP=VFP=2 lines.

If VBP+VFP less than 24, the VBP+VFP will be set to 24. The frame rate = 58.35Hz

(2) Example2: Fose=18Mhz, DIVA=1, CNT=17, RTNC=17 clock, Display Line=480 lines, VBP=VFP=14 lines.

VBP+VFP greater than 24, the original setting is kept. The frame rate = 57.89Hz.

RTNA [4:0]: RTNA [4:0] is used to set 1H (line) period of the Normal mode at the MCU interface.

RTNA [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNA [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNA [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.3. Frame Rate Control (In Idle Mode/8 Colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control (In Idle Mode/8 colors))												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVB [1:0]		00h
2nd Parameter	1	1	↑	XX	0	0	0	RTNB [4:0]					11h

Description

Set the division ratio for internal clocks of the Idle Mode ON.

DIVB [1:0]: division ratio for internal clocks when in the Idle mode.

DIVB [1:0]		Division Ratio
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

RTNB [4:0]: RTNB [4:0] is used to set 1H (line) period of the Idle Mode ON.

RTNB [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNB [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNB [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.4. Frame Rate Control (In Partial Mode/Full Colors) (B3h)

B3h	FRMCTR3 (Frame Rate Control (In Partial Mode/Full colors))												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC [1:0]		00h
2nd Parameter	1	1	↑	XX	0	0	0	RTNC [4:0]					11h

Description

Set the division ratio for internal clocks of the Partial mode ON (Idle mode off).

DIVC [1:0]: division ratio for internal clocks when in the Partial mode.

DIVC [1:0]		Division Ratio
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of the Partial mode ON.

RTNC [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNC [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNC [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.5. Display Inversion Control (B4h)

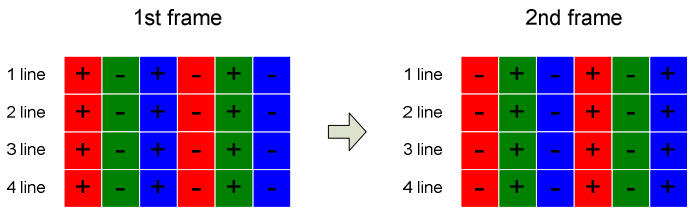
B4h	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XX	0	0	0	0	0	DINV [2:0]			02h

Description

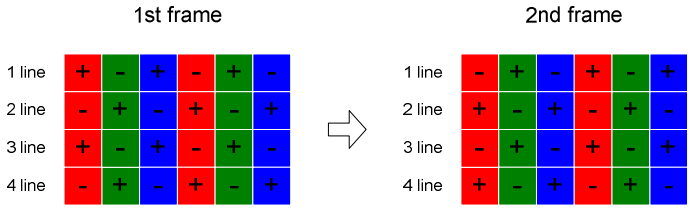
DINV: set the Display Inversion mode

DINV [2:0]			Inversion
0	0	0	Column inversion
0	0	1	1 dot inversion
0	1	0	2 dot inversion
other			Setting prohibited

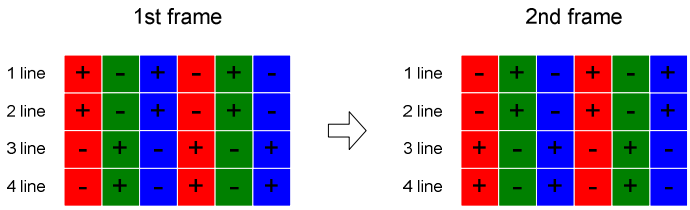
Column Inversion



1-Dot Inversion



2-Dot Inversion



X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.6. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	0	0	0	VFP [4:0]					02h
2nd Parameter	1	1	↑	XX	0	0	0	VBP [4:0]					02h
3rd Parameter	1	1	↑	XX	HFP [7:0]								0Ah
4th Parameter	1	1	↑	XX	HBP [7:0]								04h

Description

VFP [4:0]/VBP [4:0]: The VFP [4:0] and VBP [4:0] bits specify the line number of vertical front and back porch period respectively.

VFP [4:0]	Number of lines of front porch
00000	Setting prohibited
00001	Setting prohibited
00010	2
00011	3
: :	: :
11100	28
11101	29
11110	30
11111	31

VBP [4:0]	Number of lines of back porch
00000	Setting prohibited
00001	Setting prohibited
00010	2
00011	3
: :	: :
11100	28
11101	29
11110	30
11111	31

Notes:

1. VBP + VFP ≤ 32

2. Recommendation: The porch number of VBP + VFP must be even.

HFP [7:0]: The HFP [7:0] bits specify the dotclk number of horizontal front porch period.

HFP [7:0]	Number of dotclk of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
: :	: :
11111100	252
11111101	253
11111110	254
11111111	255

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HBP [7:0]: The HBP [7:0] bits specify the dotclk number of horizontal back porch period.

HBP [7:0]	Number of dotclk of back porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
: :	: :
10111101	189
10111110	190
10111111	191
11000000	192
Other	Setting prohibited

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	BYPASS	RCM	RM	DM	PTG [1:0]		PT [1:0]		02h
2ndParameter	1	1	↑	XX	0	GS	SS	SM	ISC [3:0]				02h
3rdParameter	1	1	↑	XX	0	0	NL [5:0]						3Bh

Description

DM: Select the display operation mode.

DM	Interface Mode
0	Internal system clock
1	RGB interface(DOTCLK)

RM: Select the interface to access the GRAM. When RM = 0, the driver will write display data to the GRAM via the system interface, and the driver will write display data to the GRAM via the RGB interface when RM = 1.

RM	Interface for RAM access
0	System interface
1	RGB interface

RCM: RGB interface selection (refer to the RGB interface section).

RCM	RGB transfer mode
0	DE Mode
1	SYNC Mode

BYPASS: Select the display data path (memory or direct to shift register) when the RGB interface is used.

BYPASS	Display data path
0	Memory
1	Direct to shift register

Note: The RGB input signal, when set to the BYPASS mode, the Hsync low ≧ 3, HBP ≧ 3, HFP ≧ 10.

PTG [1:0]: Set the scan mode in a non-display area.

PTG1	PTG0	Gate outputs in a non-display area	Source outputs in a non-display area
0	0	Normal scan	Set with the PT [2:0] bits
0	1	Setting prohibited	---
1	0	Interval scan	Set with the PT [2:0] bits
1	1	Setting prohibited	---

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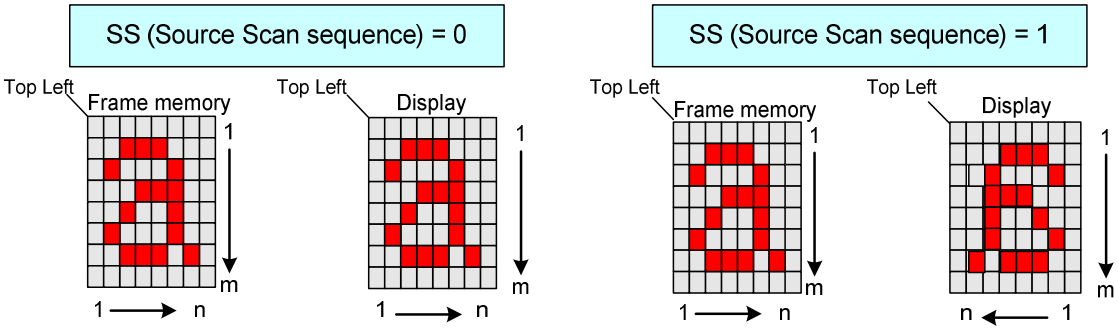
PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT [1:0]		Source output in a non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS: Select the shift direction of outputs from the source driver.



SS	Source Output Scan Direction
0	S1 → S960
1	S960 → S1

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S960, set SS = 0.

To assign R, G, B dots to the source driver pins from S960 to S1, set SS = 1.

ISC [3:0]: Set the scan cycle when the PTG selects interval scan in a non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

ISC [3:0]	Scan cycle	(f_{FRAME})=60Hz
4'h0	Setting inhibited	–
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

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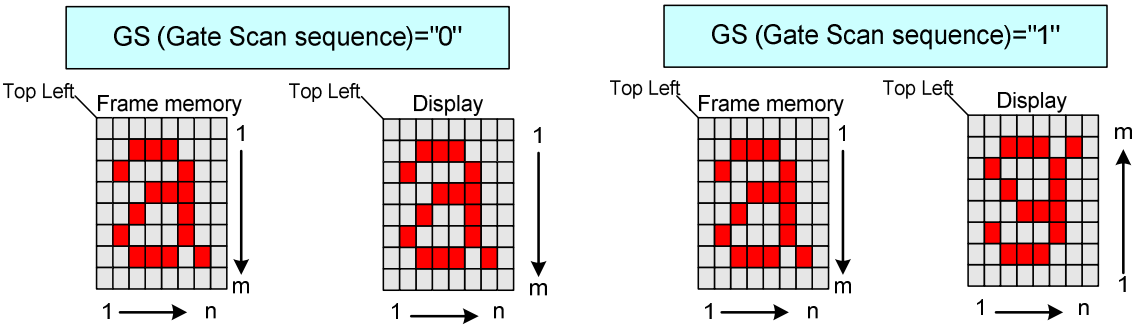
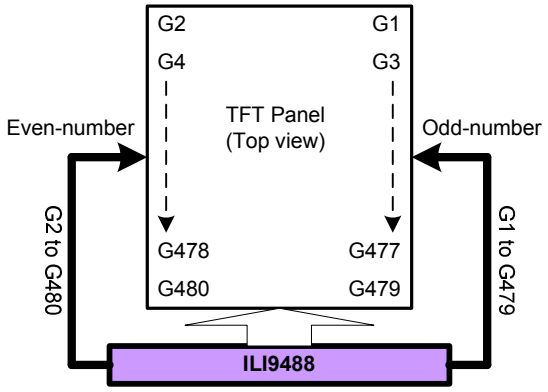
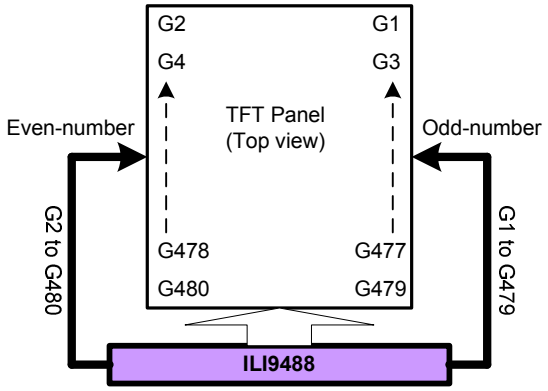
GS: Set the direction of scan by the gate driver.



GS	Gate Output Scan Direction
0	G1 → G480
1	G480 → G1

SM: Set the gate driver pin arrangement in combination with the GS bit (RB6h) to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→ G4 …… …… →G477→G478→G479→G480
0	1		G480→G479→G478→G477→…….. …….. …….. …→G4→G3→G2→G1

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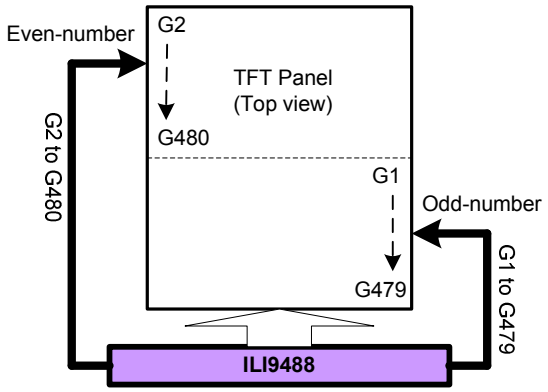
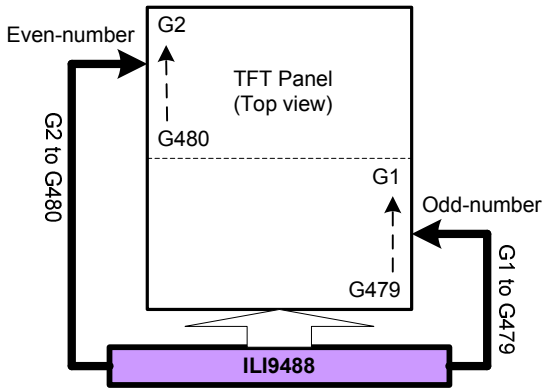
	1	0		G1→G3→…….→G477→G479→ G2→G4→……..→G478→G480
	1	1		G480→G478→……→G4→G2→ G479→G477→……→G3→G1

NL [5:0]: Set the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same as or more than the number of lines necessary for the size of the liquid crystal panel.

NL [5:0]	LCD Drive Line
6'h01 ~ 6'h3B	8 * (NL [5:0]+1) lines
Others	Setting inhibited

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.8. Entry Mode Set (B7h)

B7h	ETMOD (Entry Mode Set)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
1st Parameter	1	1	↑	XX	EPF [1:0]		0	0	DSTB	GON	DTE	GAS	06h

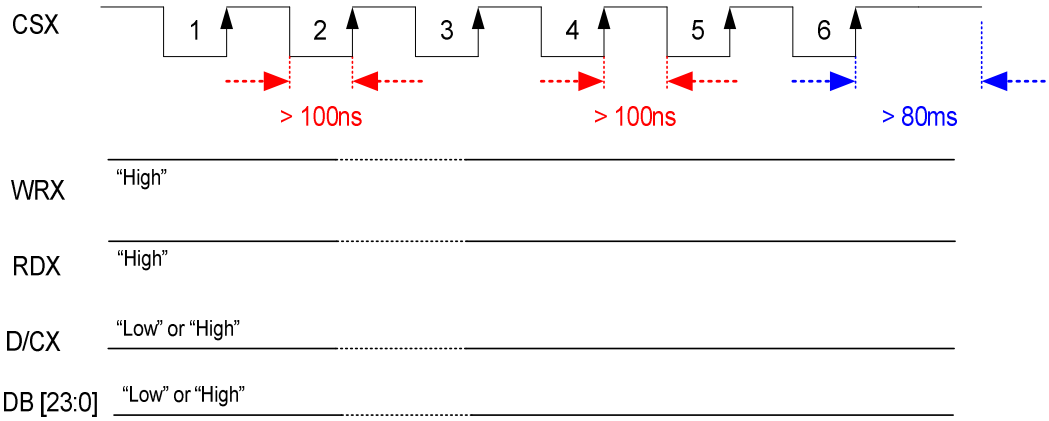
Description

DSTB: The ILI9488 driver enters the Deep Standby Mode when the DSTB is set to high (= 1). In the Deep Standby mode, both internal logic power and SRAM power are turned off, the display data are stored in the Frame Memory, and the instructions are not saved. Rewrite Frame Memory content and instructions after exiting the Deep Standby Mode.

Note: The ILI9488 provides two ways to exit the Deep Standby Mode:

(1) Exit Deep Standby Mode by pull down CSX to low (= 0) 6 times.

(2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state.



GAS: Low voltage detection control

GAS	Low voltage detection
0	Enable
1	Disable

GON/DTE: Set the output level of the gate driver G1 ~ G480 as follows:

GON	DTE	G1~G480 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

EPF [1:0]: Set the data format when 16bbp (R, G, B) to 18 bbp (R, G, B) is stored in the internal GRAM

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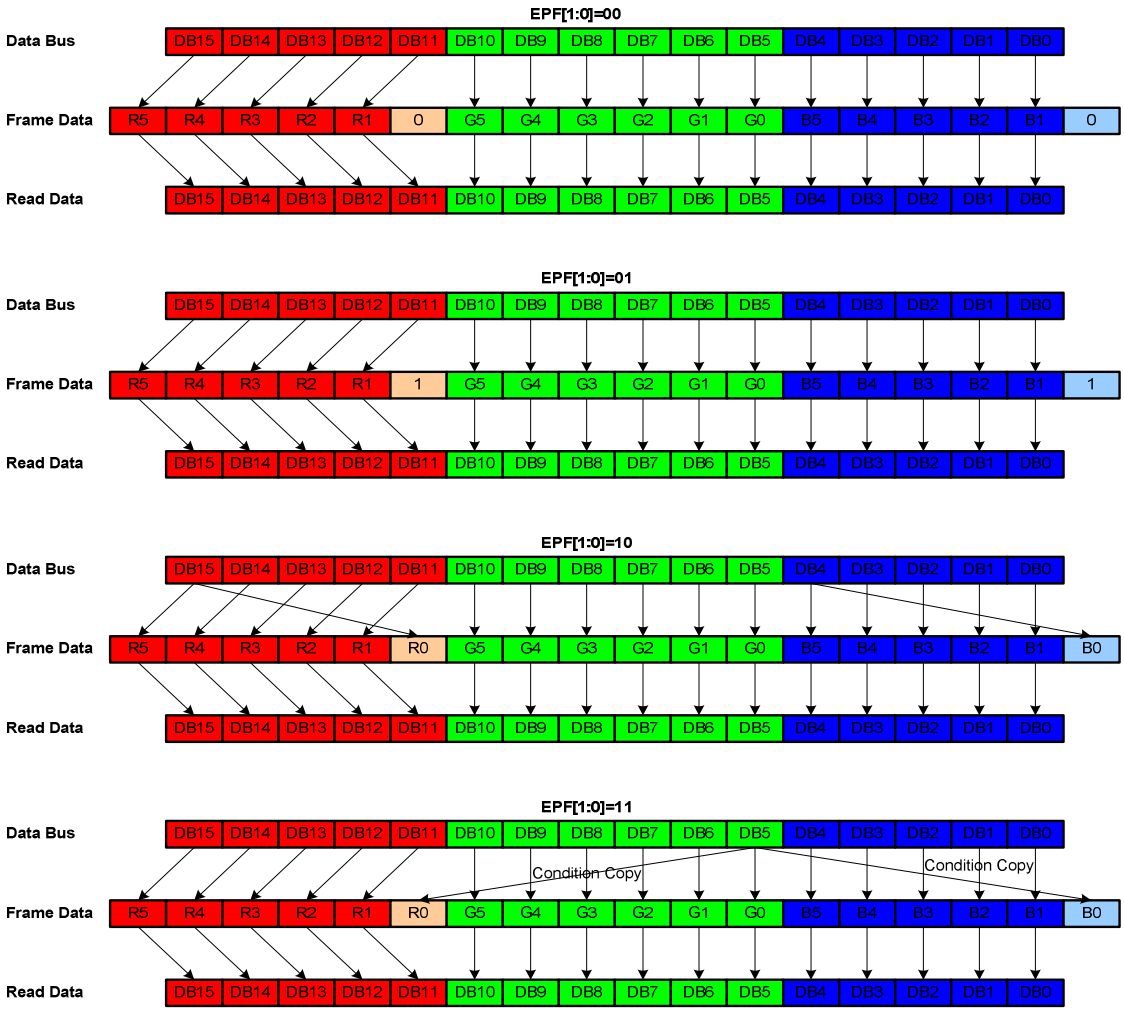

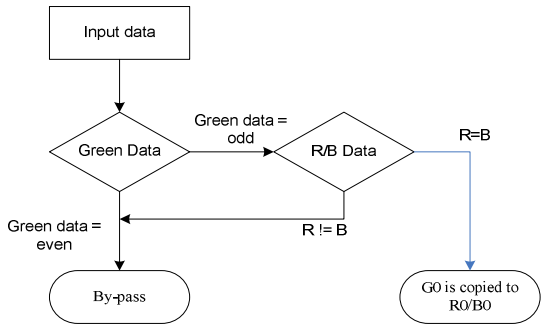

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.9. Color Enhancement Control 1 (B9h)

B9h	CECTRL1 (Color Enhancement Control 1)												
	D/CX	RDX	WRX	D[23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
1st parameter	1	1	↑	XX	0	0	0	First_Axis 1 [4:0]					04h
2nd parameter	1	1	↑	XX	0	0	0	First_Axis 2 [4:0]					04h
3rd parameter	1	1	↑	XX	0	0	0	First_Axis 3 [4:0]					04h
4th parameter	1	1	↑	XX	0	0	0	First_Axis 4 [4:0]					04h
5th parameter	1	1	↑	XX	0	0	0	Second_Axis 1 [4:0]					04h
6th parameter	1	1	↑	XX	0	0	0	Second _Axis 2 [4:0]					04h
7th parameter	1	1	↑	XX	0	0	0	Second _Axis 3 [4:0]					04h
8th parameter	1	1	↑	XX	0	0	0	Second _Axis 4 [4:0]					04h
9th parameter	1	1	↑	XX	0	0	0	Third_Axis 1 [4:0]					04h
10th parameter	1	1	↑	XX	0	0	0	Third _Axis 2 [4:0]					04h
11th parameter	1	1	↑	XX	0	0	0	Third _Axis 3 [4:0]					04h
12th parameter	1	1	↑	XX	0	0	0	Third _Axis 4 [4:0]					04h

Description

Each parameter is a base value 40h, the localization saturation ratio is calculated:

$$\text{Saturation Ratio} = \frac{\text{Axis setting value}}{64}$$

Axis setting value= 0~31 (00h~1Fh, default = 40h)

Saturation Ratio = 0~3.98 (default = 1)

See chapter " 9 Color Enhancement Function" for these parameters operation.

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.10. Color Enhancement Control 2 (BAh)

BAh	CECTRL2 (Color Enhancement Control 2)												
	D/CX	RDX	WRX	D[23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
1st parameter	1	1	↑	XX	0	0	0	Fourth_Axis 1 [4:0]					04h
2nd parameter	1	1	↑	XX	0	0	0	Fourth _Axis 2 [4:0]					04h
3rd parameter	1	1	↑	XX	0	0	0	Fourth _Axis 3 [4:0]					04h
4th parameter	1	1	↑	XX	0	0	0	Fourth _Axis 4 [4:0]					04h
5th parameter	1	1	↑	XX	0	0	0	Fifth _Axis 1 [4:0]					04h
6th parameter	1	1	↑	XX	0	0	0	Fifth _Axis 2 [4:0]					04h
7th parameter	1	1	↑	XX	0	0	0	Fifth _Axis 3 [4:0]					04h
8th parameter	1	1	↑	XX	0	0	0	Fifth _Axis 4 [4:0]					04h
9th parameter	1	1	↑	XX	0	0	0	Sixth _Axis 1 [4:0]					04h
10th parameter	1	1	↑	XX	0	0	0	Sixth _Axis 2 [4:0]					04h
11th parameter	1	1	↑	XX	0	0	0	Sixth _Axis 3 [4:0]					04h
12th parameter	1	1	↑	XX	0	0	0	Sixth_Axis 4 [4:0]					04h

Description

Each parameter is a base value 40h, the localization saturation ratio is calculated:

$$\text{Saturation Ratio} = \frac{\text{Axis setting value}}{64}$$

Axis setting value= 0~31 (00h~1Fh, default = 40h)

Saturation Ratio = 0~3.98 (default = 1)

See chapter " 9 Color Enhancement Function" for these parameters operation.

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.11. HS Lanes Control (BEh)

BEh	HSLCTRL (HS Lanes Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh
1st Parameter	1	1	↑	XX	0	D/C_Swap	PN_Inv	0	BT_FROM_OTP	BT_OTP[2:0]			00h
2nd parameter	1	1	↑	XX	0	0	0	0	0	ENHIBIT	0	0	00h

Description

BT_OTP: When the BT_FROM_OTP of 1Ah in the NV Memory Write (D0h) command is set to 1, then this BT_OTP will become 1 as well.

D/C_Swap: Swap the DATA/CLOCK of DSI Lanes.

PN_Inv: Swap the positive/negitive of the polarity of HS Lanes.

Type	D/C_Swap	PN_Inv	Pin define			
Type1	0	0	CLOCK_P	CLOCK_N	DATA_P	DATA_N
Type2	1	0	DATA_P	DATA_N	CLOCK_P	CLOCK_N
Type3	0	1	CLOCK_N	CLOCK_P	DATA_N	DATA_P
Type4	1	1	DATA_N	DATA_P	CLOCK_N	CLOCK_P

ENHIBIT: ESD protection.

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.12. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
1st Parameter	1	1	↑	XX	0	0	0	VRH1 [4:0]					0Eh
2nd Parameter	1	1	↑	XX	0	0	0	VRH2 [4:0]					0Eh

Description

VRH1 [4:0]: Set the VREG1OUT voltage for positive gamma

VRH1 [4:0]	VREG1OUT	VRH1 [4:0]	VREG1OUT
5'h00	Halt (Vreg1out = Hiz)	5'h10	1.25 x 3.65 = 4.5625
5'h01	1.25 x 2.90 = 3.6250	5'h11	1.25 x 3.70 = 4.6250
5'h02	1.25 x 2.95 = 3.6875	5'h12	1.25 x 3.75 = 4.6875
5'h03	1.25 x 3.00 = 3.7500	5'h13	1.25 x 3.80 = 4.7500
5'h04	1.25 x 3.05 = 3.8125	5'h14	1.25 x 3.85 = 4.8125
5'h05	1.25 x 3.10 = 3.8750	5'h15	1.25 x 3.90 = 4.8750
5'h06	1.25 x 3.15 = 3.9375	5'h16	1.25 x 3.95 = 4.9375
5'h07	1.25 x 3.20 = 4.0000	5'h17	1.25 x 4.00 = 5.0000
5'h08	1.25 x 3.25 = 4.0625	5'h18	1.25 x 4.05 = 5.0625
5'h09	1.25 x 3.30 = 4.1250	5'h19	1.25 x 4.10 = 5.1250
5'h0A	1.25 x 3.35 = 4.1875	5'h1A	1.25 x 4.15 = 5.1875
5'h0B	1.25 x 3.40 = 4.2500	5'h1B	1.25 x 4.20 = 5.2500
5'h0C	1.25 x 3.45 = 4.3125	5'h1C	1.25 x 4.25 = 5.3125
5'h0D	1.25 x 3.50 = 4.3750	5'h1D	1.25 x 4.30 = 5.3750
5'h0E	1.25 x 3.55 = 4.4375	5'h1E	1.25 x 4.35 = 5.4375
5'h0F	1.25 x 3.60 = 4.5000	5'h1F	1.25 x 4.40 = 5.5000

VRH2 [4:0]: Set the VREG2OUT voltage for negative gammas

VRH2 [4:0]	VREG2OUT	VRH2 [4:0]	VREG2OUT
5'h00	Halt (Vreg2out = Hiz)	5'h10	-1.25 x 3.65 = -4.5625
5'h01	-1.25 x 2.90 = -3.6250	5'h11	-1.25 x 3.70 = -4.6250
5'h02	-1.25 x 2.95 = -3.6875	5'h12	-1.25 x 3.75 = -4.6875
5'h03	-1.25 x 3.00 = -3.7500	5'h13	-1.25 x 3.80 = -4.7500
5'h04	-1.25 x 3.05 = -3.8125	5'h14	-1.25 x 3.85 = -4.8125
5'h05	-1.25 x 3.10 = -3.8750	5'h15	-1.25 x 3.90 = -4.8750
5'h06	-1.25 x 3.15 = -3.9375	5'h16	-1.25 x 3.95 = -4.9375
5'h07	-1.25 x 3.20 = -4.0000	5'h17	-1.25 x 4.00 = -5.0000
5'h08	-1.25 x 3.25 = -4.0625	5'h18	-1.25 x 4.05 = -5.0625
5'h09	-1.25 x 3.30 = -4.1250	5'h19	-1.25 x 4.10 = -5.1250
5'h0A	-1.25 x 3.35 = -4.1875	5'h1A	-1.25 x 4.15 = -5.1875
5'h0B	-1.25 x 3.40 = -4.2500	5'h1B	-1.25 x 4.20 = -5.2500
5'h0C	-1.25 x 3.45 = -4.3125	5'h1C	-1.25 x 4.25 = -5.3125
5'h0D	-1.25 x 3.50 = -4.3750	5'h1D	-1.25 x 4.30 = -5.3750
5'h0E	-1.25 x 3.55 = -4.4375	5'h1E	-1.25 x 4.35 = -5.4375
5'h0F	-1.25 x 3.60 = -4.5000	5'h1F	-1.25 x 4.40 = -5.5000

Note 1: The setting of DDVDH and VRH1 should be: VREG1OUT ≦ (DDVDH – 0.5) V.

Note 2: The setting of DDVDL and VRH2 should be VREG2OUT ≧ (DDVDL + 0.5) V.

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<table>
<tr><td></td><td>X = void</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

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5.3.13. Power Control 2 (C1h)

C1h	PWCTRL 2 (Power Control 2)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
1st Parameter	1	1	↑	XX	0	1	0	0	0	BT [2:0]			44h

Description

BT [2:0]: Set the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT [2:0]	DDVDH	DDVDL	VCL	VGH	VGL
3'h0	VCI x 2	-(VCI x 2)	- VCI	VCI x 6	- VCI x 5
3'h1					- VCI x 4
3'h2				Inhibited	
3'h3				VCI x 5	- VCI x 5
3'h4					- VCI x 4
3'h5					- VCI x 3
3'h6				VCI x 4	- VCI x4
3'h7					- VCI x3

Notes:

1. DDVDH setting restriction: DDVDH ≤ 6.0 V.

2. To prevent the device damage, please keep VGH – VGL ≤ 32V.

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.14. Power Control 3 (For Normal Mode) (C2h)

C2h	PWCTRL 3 (Power Control 3)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	0	C2h
1st Parameter	1	1	↑	XX	0	DCA1 [2:0]			0	DCA0 [2:0]			33h

Description

DCA0 [2:0]: Select the operating frequency of the step-up circuit 1/4/5 for the Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption.

DCA1 [2:0]: Select the operating frequency of the step-up circuit 2/3 for the Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption..

DCA0 [2:0]			Step-up cycle for step-up circuit 1/4/5
0	0	0	1/8 H
0	0	1	1/4 H
0	1	0	1/2 H
0	1	1	1 H
1	0	0	2 H

DCA1 [2:0]			Step-up cycle for step-up circuit 2/3
0	0	0	1/2 H
0	0	1	1 H
0	1	0	2 H
0	1	1	4 H
1	0	0	8 H

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.15. Power Control 4 (For Idle Mode) (C3h)

C3h	PWCTRL 4 (Power Control 4)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
1st Parameter	1	1	↑	XX	0	DCB1 [2:0]			0	DCB0 [2:0]			33h

Description

DCB0 [2:0]: Select the operating frequency of the step-up circuit 1/4/5 for the Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption.

DCB1 [2:0]: Select the operating frequency of the step-up circuit 2/3 for the Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption.

DCB0 [2:0]			Step-up cycle for step-up circuit 1/4/5
0	0	0	1/8 H
0	0	1	1/4 H
0	1	0	1/2 H
0	1	1	1 H
1	0	0	2 H

DCB1 [2:0]			Step-up cycle for step-up circuit 2/3
0	0	0	1/2 H
0	0	1	1 H
0	1	0	2 H
0	1	1	4 H
1	0	0	8 H

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.16. Power Control 5 (For Partial Mode) (C4h)

C4h	PWCTRL 5 (Power Control 5)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
1st Parameter	1	1	↑	XX	0	DCC1 [2:0]			0	DCC0 [2:0]			33h

Description

DCC0 [2:0]: Select the operating frequency of the step-up circuit 1/4/5 for the Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption.

DCC1 [2:0]: Select the operating frequency of the step-up circuit 2/3 for the Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display, but increases the current consumption. Adjust the frequency will affect the display quality and the current consumption.

DCC0 [2:0]			Step-up cycle for step-up circuit 1/4/5
0	0	0	1/8 H
0	0	1	1/4 H
0	1	0	1/2 H
0	1	1	1 H
1	0	0	2 H

DCC1 [2:0]			Step-up cycle for step-up circuit 2/3
0	0	0	1/2 H
0	0	1	1 H
0	1	0	2 H
0	1	1	4 H
1	0	0	8 H

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.17. VCOM Control (C5h)

C5h	VMCTRL (VCOM Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
1st Parameter	1	↑	1	XX	0	0	0	0	0	0	0	nVM	00h
2nd Parameter	1	1	↑	XX	VCM_REG [7:0]								40h
3rd Parameter	1	1	↑	XX	VCM_REG_EN	0	0	0	0	0	0	0	00h
4rd Parameter	1	↑	1	XX	VCM_OUT [7:0]								40h

Description

nVM: When the NV memory is programmed, the nVM will be set to 1 automatically.
0: NV memory is not programmed
1: NV memory is programmed

VCM_REG [7:0] is used to set the factor to generate VCOM voltage from the reference voltage VREG2OUT.

VCM_REG [7:0]								VCOM
0	0	0	0	0	0	0	0	-2
0	0	0	0	0	0	0	1	-1.98438
0	0	0	0	0	0	1	0	-1.96875
0	0	0	0	0	0	1	1	-1.95313
0	0	0	0	0	1	0	0	-1.9375
0	0	0	0	0	1	0	1	-1.92188
0	0	0	0	0	1	1	0	-1.90625
0	0	0	0	0	1	1	1	-1.89063
0	0	0	0	1	0	0	0	-1.875
0	0	0	0	1	0	0	1	-1.85938
0	0	0	0	1	0	1	0	-1.84375
0	0	0	0	1	0	1	1	-1.82813
0	0	0	0	1	1	0	0	-1.8125
0	0	0	0	1	1	0	1	-1.79688
0	0	0	0	1	1	1	0	-1.78125
0	0	0	0	1	1	1	1	-1.76563
0	0	0	1	0	0	0	0	-1.75
0	0	0	1	0	0	0	1	-1.73438
0	0	0	1	0	0	1	0	-1.71875
0	0	0	1	0	0	1	1	-1.70313
0	0	0	1	0	1	0	0	-1.6875
0	0	0	1	0	1	0	1	-1.67188
0	0	0	1	0	1	1	0	-1.65625
0	0	0	1	0	1	1	1	-1.64063
0	0	0	1	1	0	0	0	-1.625
0	0	0	1	1	0	0	1	-1.60938
0	0	0	1	1	0	1	0	-1.59375
0	0	0	1	1	0	1	1	-1.57813
0	0	0	1	1	1	0	0	-1.5625
0	0	0	1	1	1	0	1	-1.54688
0	0	0	1	1	1	1	0	-1.53125
0	0	0	1	1	1	1	1	-1.51563

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		0	0	1	0	0	0	0	0	-1.5	
		0	0	1	0	0	0	0	1	-1.48438	
		0	0	1	0	0	0	1	0	-1.46875	
		0	0	1	0	0	0	1	1	-1.45313	
		0	0	1	0	0	1	0	0	-1.4375	
		0	0	1	0	0	1	0	1	-1.42188	
		0	0	1	0	0	1	1	0	-1.40625	
		0	0	1	0	0	1	1	1	-1.39063	
		0	0	1	0	1	0	0	0	-1.375	
		0	0	1	0	1	0	0	1	-1.35938	
		0	0	1	0	1	0	1	0	-1.34375	
		0	0	1	0	1	0	1	1	-1.32813	
		0	0	1	0	1	1	0	0	-1.3125	
		0	0	1	0	1	1	0	1	-1.29688	
		0	0	1	0	1	1	1	0	-1.28125	
		0	0	1	0	1	1	1	1	-1.26563	
		0	0	1	1	0	0	0	0	-1.25	
		0	0	1	1	0	0	0	1	-1.23438	
		0	0	1	1	0	0	1	0	-1.21875	
		0	0	1	1	0	0	1	1	-1.20313	
		0	0	1	1	0	1	0	0	-1.1875	
		0	0	1	1	0	1	0	1	-1.17188	
		0	0	1	1	0	1	1	0	-1.15625	
		0	0	1	1	0	1	1	1	-1.14063	
		0	0	1	1	1	0	0	0	-1.125	
		0	0	1	1	1	0	0	1	-1.10938	
		0	0	1	1	1	0	1	0	-1.09375	
		0	0	1	1	1	0	1	1	-1.07813	
		0	0	1	1	1	1	0	0	-1.0625	
		0	0	1	1	1	1	0	1	-1.04688	
		0	0	1	1	1	1	1	0	-1.03125	
		0	0	1	1	1	1	1	1	-1.01563	
		0	1	0	0	0	0	0	0	-1	
		0	1	0	0	0	0	0	1	-0.98438	
		0	1	0	0	0	0	1	0	-0.96875	
		0	1	0	0	0	0	1	1	-0.95313	
		0	1	0	0	0	1	0	0	-0.9375	
		0	1	0	0	0	1	0	1	-0.92188	
		0	1	0	0	0	1	1	0	-0.90625	
		0	1	0	0	0	1	1	1	-0.89063	
		0	1	0	0	1	0	0	0	-0.875	
		0	1	0	0	1	0	0	1	-0.85938	
		0	1	0	0	1	0	1	0	-0.84375	
		0	1	0	0	1	0	1	1	-0.82813	
		0	1	0	0	1	1	0	0	-0.8125	
		0	1	0	0	1	1	0	1	-0.79688	
		0	1	0	0	1	1	1	0	-0.78125	
		0	1	0	0	1	1	1	1	-0.76563	

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		0	1	0	1	0	0	0	0	-0.75	
		0	1	0	1	0	0	0	1	-0.73438	
		0	1	0	1	0	0	1	0	-0.71875	
		0	1	0	1	0	0	1	1	-0.70313	
		0	1	0	1	0	1	0	0	-0.6875	
		0	1	0	1	0	1	0	1	-0.67188	
		0	1	0	1	0	1	1	0	-0.65625	
		0	1	0	1	0	1	1	1	-0.64063	
		0	1	0	1	1	0	0	0	-0.625	
		0	1	0	1	1	0	0	1	-0.60938	
		0	1	0	1	1	0	1	0	-0.59375	
		0	1	0	1	1	0	1	1	-0.57813	
		0	1	0	1	1	1	0	0	-0.5625	
		0	1	0	1	1	1	0	1	-0.54688	
		0	1	0	1	1	1	1	0	-0.53125	
		0	1	0	1	1	1	1	1	-0.51563	
		0	1	1	0	0	0	0	0	-0.5	
		0	1	1	0	0	0	0	1	-0.48438	
		0	1	1	0	0	0	1	0	-0.46875	
		0	1	1	0	0	0	1	1	-0.45313	
		0	1	1	0	0	1	0	0	-0.4375	
		0	1	1	0	0	1	0	1	-0.42188	
		0	1	1	0	0	1	1	0	-0.40625	
		0	1	1	0	0	1	1	1	-0.39063	
		0	1	1	0	1	0	0	0	-0.375	
		0	1	1	0	1	0	0	1	-0.35938	
		0	1	1	0	1	0	1	0	-0.34375	
		0	1	1	0	1	0	1	1	-0.32813	
		0	1	1	0	1	1	0	0	-0.3125	
		0	1	1	0	1	1	0	1	-0.29688	
		0	1	1	0	1	1	1	0	-0.28125	
		0	1	1	0	1	1	1	1	-0.26563	
		0	1	1	1	0	0	0	0	-0.25	
		0	1	1	1	0	0	0	1	-0.23438	
		0	1	1	1	0	0	1	0	-0.21875	
		0	1	1	1	0	0	1	1	-0.20313	
		0	1	1	1	0	1	0	0	-0.1875	
		0	1	1	1	0	1	0	1	-0.17188	
		0	1	1	1	0	1	1	0	-0.15625	
		0	1	1	1	0	1	1	1	-0.14063	
		0	1	1	1	1	0	0	0	-0.125	
		0	1	1	1	1	0	0	1	-0.10938	
		0	1	1	1	1	0	1	0	-0.09375	
		0	1	1	1	1	0	1	1	-0.07813	
		0	1	1	1	1	1	0	0	-0.0625	
		0	1	1	1	1	1	0	1	-0.04688	
		0	1	1	1	1	1	1	0	-0.03125	
		0	1	1	1	1	1	1	1	-0.01563	

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1	0	0	0	0	0	0	0	0
10000001~11111110								Inbibit
11111111								Halt

VCM_REG_EN: Select the Vcom value from **VCM_REG [7:0]** or **NV memory**.

0: VCOM value from NV memory.
1: VCOM value from VCM_REG [7:0].

VCM_OUT [7:0]: NV memory programmed value.

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.18. CABC Control 1 (C6h)

C6h	CABCCTRL1 (CABC Control 1)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	0	C6h
1st Parameter	1	1	↑	XX	SCD_VLINE [7:0]								E0h
2nd Parameter	1	1	↑	XX	0	0	0	0	0	SCD_VLINE [10:8]			01h

Description

SCD_VLINE [10:0]: This parameter is used to set the display line per frame while the partial mode is ON.

SCD_VLINE [8:0]											Display line
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	0	0	0	1	1	3 lines
0	0	0	0	0	0	0	0	1	0	0	4 lines
:											:
:											:
0	0	1	1	1	0	1	1	1	0	1	477 lines
0	0	1	1	1	0	1	1	1	1	0	478 lines
0	0	1	1	1	0	1	1	1	1	1	479 lines
0	0	1	1	1	1	0	0	0	0	0	480 lines
Others											Setting prohibited

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.19. CABC Control 2 (C8h)

C8h	CABCCTRL2 (CABC Control 2)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	0	0	0	C8h
1st Parameter	1	1	↑	XX	1	0	1	1	0	0	0	PWMPOL	B0h

Description

PWMPOL: The bit is used to define the polarity of the CABC_PWM signal.

BL	LEDPWMPOL	CABC_PWM pin
0	0	Always low
0	1	Always high
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.20. CABC Control 3 (C9h)

C9h	CABCCTRL3 (CABC Control 3)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
1st Parameter	1	1	↑	XX	THRES_MOV [3:0]				THRES_STILL [3:0]				BBh

Description

THRES_MOV [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the MOVING image mode. After this parameter sets the number of pixels that makes display image white, the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed.

THRES_MOV [3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_MOV [3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %

THRES_STILL [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the STILL mode. After this parameter sets the number of pixels that makes display image white, the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed.

THRES_STILL [3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_STILL [3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %

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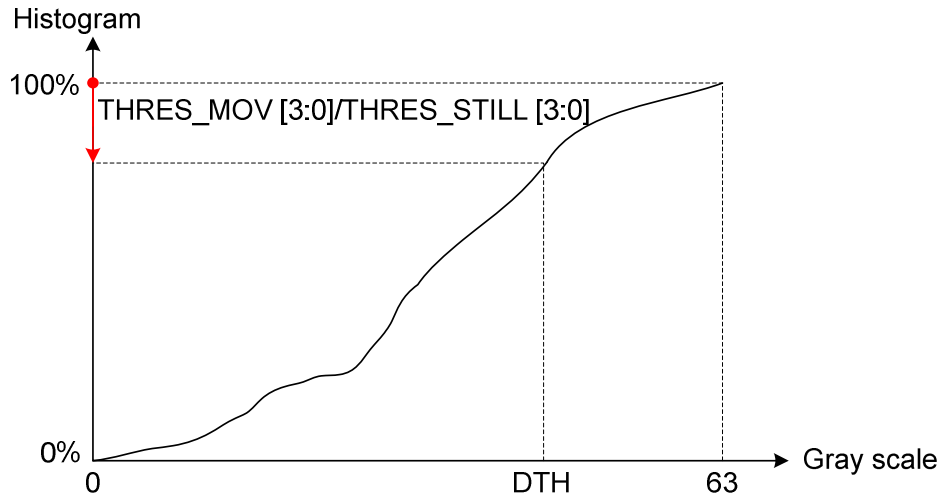
<table>
<tr><td></td><td> 

X = Void</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

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5.3.21. CABC Control 4 (CAh)

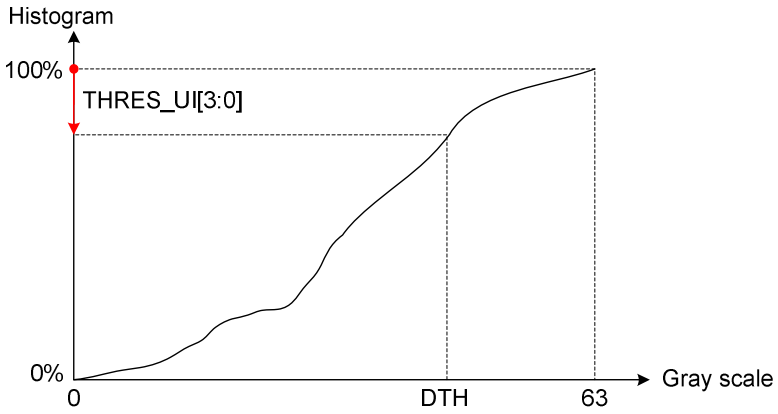
CAh	CABCCTRL4 (CABC Control 4)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	0	1	0	CAh
1st Parameter	1	1	↑	XX	0	0	0	0	THRES_UI [3:0]				0Bh

Description

THRES_UI [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the USER INTERFACE mode. After this parameter sets the number of pixels that makes display image white, the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed.

THRES_UI [3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_UI [3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



X = Void.

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.22. CABC Control 5 (CBh)

CBh	CABCCTRL5 (CABC Control 5)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	0	1	1	CBh
1st Parameter	1	1	↑	XX	DTH_MOV [3:0]				DTH_STILL [3:0]				A8h

Description

DTH_MOV [3:0]: This parameter is used to set the minimum limitation of the grayscale threshold value in the MOVING image mode.

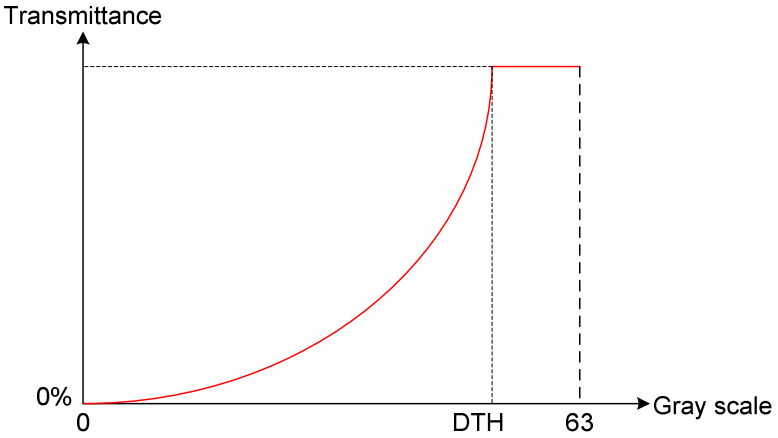
DTH_MOV [3:0]				Description
D3	D2	D1	D0	
0	0	0	0	224
0	0	0	1	220
0	0	1	0	216
0	0	1	1	212
0	1	0	0	208
0	1	0	1	204
0	1	1	0	200
0	1	1	1	196

DTH_MOV [3:0]				Description
D3	D2	D1	D0	
1	0	0	0	192
1	0	0	1	188
1	0	1	0	184
1	0	1	1	180
1	1	0	0	176
1	1	0	1	172
1	1	1	0	168
1	1	1	1	164

DTH_STILL [3:0]: This parameter is used to set the minimum limitation of the grayscale threshold value in the STILL image mode.

DTH_STILL [3:0]				Description
D3	D2	D1	D0	
0	0	0	0	224
0	0	0	1	220
0	0	1	0	216
0	0	1	1	212
0	1	0	0	208
0	1	0	1	204
0	1	1	0	200
0	1	1	1	196

DTH_STILL [3:0]				Description
D3	D2	D1	D0	
1	0	0	0	192
1	0	0	1	188
1	0	1	0	184
1	0	1	1	180
1	1	0	0	176
1	1	0	1	172
1	1	1	0	168
1	1	1	1	164



X = void

Restriction

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Register Availability		**Status**	**Availability**
		Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
		Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
		Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
		Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
		Sleep IN	Yes

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5.3.23. CABC Control 6 (CCh)

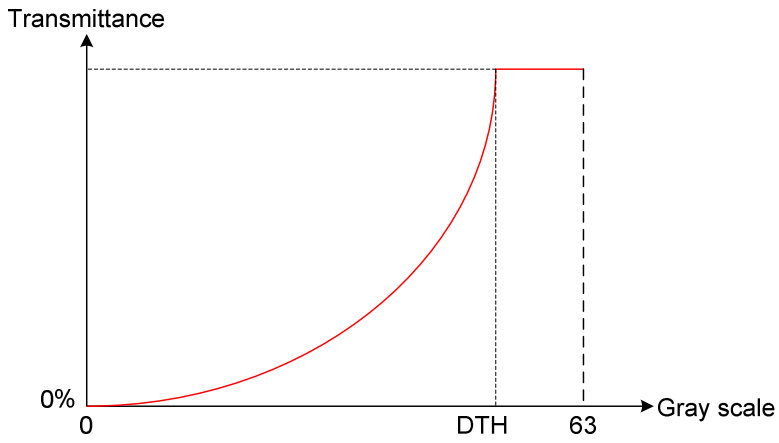
CCh	CABCCTRL6 (CABC Control 6)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	1	0	0	CCh
1st Parameter	1	1	↑	XX	0	0	0	0	DTH_UI [3:0]				03h

Description

DTH_UI [3:0]: This parameter is used to set the minimum limitation of the grayscale threshold value in the USER INTERFACE mode.

DTH_UI [3:0]				Description
D3	D2	D1	D0	
0	0	0	0	252
0	0	0	1	248
0	0	1	0	244
0	0	1	1	240
0	1	0	0	236
0	1	0	1	232
0	1	1	0	228
0	1	1	1	224

DTH_UI [3:0]				Description
D3	D2	D1	D0	
1	0	0	0	220
1	0	0	1	216
1	0	1	0	212
1	0	1	1	208
1	1	0	0	204
1	1	0	1	200
1	1	1	0	196
1	1	1	1	192



X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.24. CABC Control 7 (CDh)

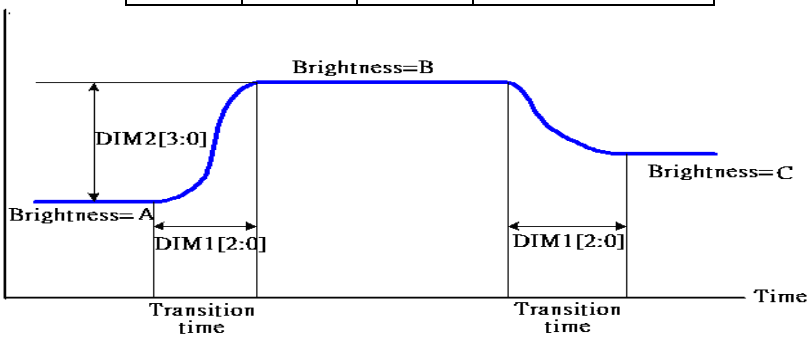
CDh	CABCCTRL7 (CABC Control 7)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	1	0	1	CDh
1st Parameter	1	1	↑	XX	0	DIM_MOV [2:0]			0	DIM_STILL [2:0]			43h

Description

DIM_STILL [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the Still mode.

DIM_MOV [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the Still mode.

DIM_MOV [2:0]/DIM_STILL [2:0]			Description
D2	D1	D0	
0	0	0	2 frame
0	0	1	3 frame
0	1	0	4~6 frames
0	1	1	8~12 frames
1	0	0	16~24 frames
1	0	1	32~48 frames
1	1	0	64~96 frames
1	1	1	128~192 frames



X = void

Note: In the above picture, **DIM1 [2:0]** means **DIM_MOV [2:0]**, **DIM_STILL [2:0],** and **DIM_UI [2:0]** are in different modes.

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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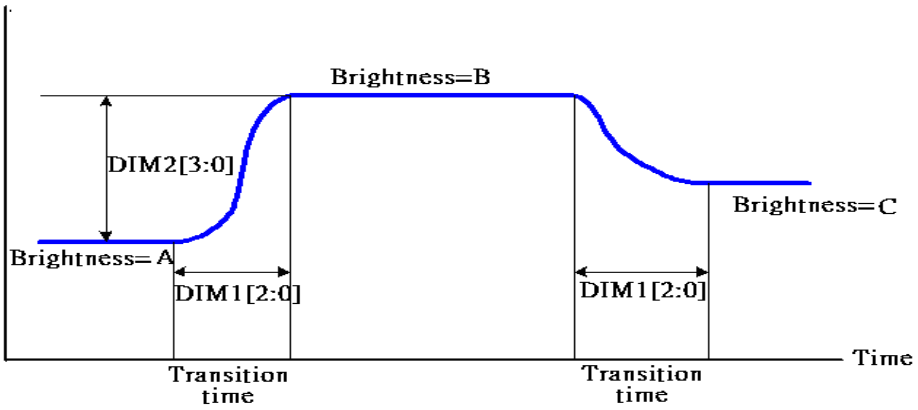
5.3.25. CABC Control 8 (CEh)

CEh	CABCCTRL8 (CABC Control 8)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	1	1	0	CEh
1st Parameter	1	1	↑	XX	DIM_MIN [3:0]				0	DIM_UI [2:0]			02h

Description

DIM_UI [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the UI mode.

DIM_UI [2:0]			Description
D2	D1	D0	
0	0	0	2 frame
0	0	1	3 frame
0	1	0	4~6 frames
0	1	1	8~12 frames
1	0	0	16~24 frames
1	0	1	32~48 frames
1	1	0	64~96 frames
1	1	1	128~192 frames



DIM_MIN [3:0]: The parameter is used to set the limitation of the minimum brightness change. If the parameter is larger than the difference between the target brightness and the current brightness, then the brightness will not be changed.

Notes:

1. In the above picture, **DIM1 [2:0]** means **DIM_MOV [2:0]**, **DIM_STILL [2:0]**, and **DIM_UI [2:0]** are in different modes.
2. In the above picture, **DIM2 [3:0]** means **DIM_MIN [3:0]**.

X = void

Restriction

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Register Availability	

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.26. CABC Control 9 (CFh)

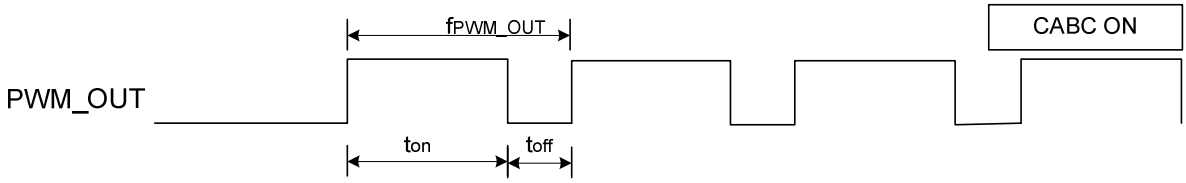
CFh	CABCCTRL9 (CABC Control 9)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	1	1	1	CFh
1st Parameter	1	1	↑	XX	PWM_DIV [7:0]								F8h

Description

PWM_DIV [7:0]: CABC_PWM output period control. This command is used to adjust the PWM waveform period of CABC_PWM. The PWM period can be calculated using the equation below:

$$f_{PWM_OUT} = \frac{18MHz}{(PWM_DIV[7:0]+1)\times 255}$$

PWM_DIV [7:0]								f_{PWM_OUT}
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	70.58 KHz
0	0	0	0	0	0	0	1	35.29 KHz
0	0	0	0	0	0	1	0	23.53 KHz
0	0	0	0	0	0	1	1	17.64 KHz
0	0	0	0	0	1	0	0	14.11KHz
:								:
1	1	1	1	1	0	1	1	280.0Hz
1	1	1	1	1	1	0	0	279.0 Hz
1	1	1	1	1	1	0	1	277.9 Hz
1	1	1	1	1	1	1	0	276.8 Hz
1	1	1	1	1	1	1	1	275.8 Hz



X = void

Note: The output frequency tolerance of the internal frequency divider in the CABC is ±10%.

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.27. NV Memory Write (D0h)

D0h	NVMWR (NV Memory Write)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
1st Parameter	1	1	↑	XX	PGM_ADR [7:0]								00h
2nd Parameter	1	1	↑	XX	PGM_DATA [7:0]								00h

Description

This command is used to program the NV memory data. After a successful OTP operation, the information of PGM_DATA [7:0] will be programmed to the NV memory.

PGM_ADR [7:0]: The select bits of ID1, ID2, ID3, ID4, VCM [7:0], VRH1, VRH2, BT and MADCTL programming.

PGM_DATA [7:0]: The programmed data.

PGM_ADR [7:0]	PGM_DATA [7:0]								Programmed NV Memory Selection
00h	ID4								ID4 programming
03h	ID1								ID1 programming
07h	ID2								ID2 programming
0Bh	ID3								ID3 programming
0Fh	VCM[7:0]								VCM[7:0] programming
16h	0	0	0	VRH1 [4:0]					VRH1 programming
17h	0	0	0	VRH2 [4:0]					VRH2 programming
19h	BGR	REV	MX	MY	0	0	0	0	MADCTL programming
1Ah	0	0	0	0	BT_FROM_OTP	BT [2:0]			BT programming

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.28. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h
1st Parameter	1	1	↑	XX	KEY [23:16]								55h
2nd Parameter	1	1	↑	XX	KEY [15:8]								AAh
3rd Parameter	1	1	↑	XX	KEY [7:0]								66h
Description	**KEY [23:0]:** NV memory programming protection key. When writing OTP data to D0h, this register must be set to 0x55AA66h to enable the OTP programming. If the D1h register is not written with 0x55AA66h, then the NV memory programming will be aborted. X = void												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.29. NV Memory Status Read (D2h)

D2h	DISON (Display ON)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	ID2_CNT [3:0]				ID1_CNT [3:0]				00h
3rd Parameter	1	↑	1	XX	VCM_CNT [3:0]				ID3_CNT [3:0]				00h

Description

ID2_CNT [3:0], ID1_CNT [3:0], VCM_CNT [3:0], ID3_CNT [3:0]: NV memory program record. The bits will increase "+1" automatically after writing to the NV memory.

ID1_CNT [3:0]/ID2_CNT [3:0]/ID3_CNT [3:0]/ VCM_CNT [3:0]				Description
0	0	0	0	No Programmed
0	0	0	1	Programmed 1 time
0	0	1	1	Programmed 2 times
0	1	1	1	Programmed 3 times
1	1	1	1	Programmed 4 times

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.30. Read ID4 (D3h)

D3h	RDID4 (Read ID4)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00h
3rd Parameter	1	↑	1	XX	1	0	0	1	0	1	0	0	94h
4th Parameter	1	↑	1	XX	1	0	0	0	1	0	0	0	88h

Description

This command is used to read the IC device code.

The 1st parameter shows the dummy read period.

The 2rd and 3th parameter mean the IC model name.

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.31. Adjust Control 1 (D7h)

D7h	Adjust Control 1												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	1	1	1	D7h
1st Parameter	1	1	↑	XX	0	0	Chopper_op _clk_opt	Chopper_op _clk_sel [1:0]		0	1	1	03h

Description

Chopper_op_clk_opt: Source Op-amp chopper function option (0 or 1)

0 (default) = refer to the table of Chopper_sel [1:0] in F2h

1 = refer to the table of Chopper_op_clk_sel below

Chopper_op_clk_sel[1:0]: Source Op-amp chopper function option

Chopper_op_clk_sel [1:0]		Description
0	0	op_clk
1	0	op_clk/2
0	1	op_clk/4
1	1	op_clk/8

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.32. Read ID Version(D8h)

D8h	Read ID Version (Read IDV)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	0	0	D8h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	ID [7:0]								00h
Description	This command is used to read the IC version. The 1st parameter shows the dummy read period. The 2rd parameter means the IC version. The ID[7:0] can be programmed by the OTP function one time. X = void												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.33. PGAMCTRL (Positive Gamma Control) (E0h)

E0h	PGAMCTRL (Positive Gamma Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
1st Parameter	1	1	↑	XX	0	0	0	0	VP0 [3:0]				00h
2nd Parameter	1	1	↑	XX	0	0	VP1 [5:0]						07h
3rd Parameter	1	1	↑	XX	0	0	VP2 [5:0]						0Ch
4th Parameter	1	1	↑	XX	0	0	0	0	VP4 [3:0]				05h
5th Parameter	1	1	↑	XX	0	0	0	VP6 [4:0]					13h
6th Parameter	1	1	↑	XX	0	0	0	0	VP13 [3:0]				09h
7th Parameter	1	1	↑	XX	0	VP20 [6:0]							36h
8th Parameter	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]				AAh
9th Parameter	1	1	↑	XX	0	VP43 [6:0]							46h
10thParameter	1	1	↑	XX	0	0	0	0	VP50 [3:0]				09h
11thParameter	1	1	↑	XX	0	0	0	VP57 [4:0]					10h
12thParameter	1	1	↑	XX	0	0	0	0	VP59 [3:0]				0Dh
13thParameter	1	1	↑	XX	0	0	VP61 [5:0]						1Ah
14thParameter	1	1	↑	XX	0	0	VP62 [5:0]						1Eh
15thParameter	1	1	↑	XX	0	0	0	0	VP63 [3:0]				0Fh
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. X = void												
Restriction													
Register Availability													

Status	Availa ility
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.34. NGAMCTRL (Negative Gamma Control) (E1h)

E1h	NGAMCTRL (Negative Gamma Control)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h
1st Parameter	1	1	↑	XX	0	0	0	0	VN0 [3:0]				00h
2nd Parameter	1	1	↑	XX	0	0	VN1 [5:0]						20h
3rd Parameter	1	1	↑	XX	0	0	VN2 [5:0]						23h
4th Parameter	1	1	↑	XX	0	0	0	0	VN4 [3:0]				04h
5th Parameter	1	1	↑	XX	0	0	0	RVN6 [4:0]					10h
6th Parameter	1	1	↑	XX	0	0	0	0	VN13 [3:0]				06h
7th Parameter	1	1	↑	XX	0	VN20 [6:0]							37h
8th Parameter	1	1	↑	XX	VN27 [3:0]				VN36 [3:0]				56h
9th Parameter	1	1	↑	XX	0	VN43 [6:0]							49h
10thParameter	1	1	↑	XX	0	0	0	0	VN50 [3:0]				04h
11thParameter	1	1	↑	XX	0	0	0	VN57 [4:0]					0Ch
12thParameter	1	1	↑	XX	0	0	0	0	VN59 [3:0]				0Ah
13thParameter	1	1	↑	XX	0	0	VN61 [5:0]						33h
14thParameter	1	1	↑	XX	0	0	VN62 [5:0]						37h
15thParameter	1	1	↑	XX	0	0	0	0	VN63 [3:0]				0Fh
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. X = void												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.35. Ditigal Gamma Control 1 (E2h)

E2h	DGAMCTRL (Digital Gamma Control 1)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				00h
2nd Parameter	1	1	↑	XX	RCA1 [3:0]				BCA1 [3:0]				00h
3rd Parameter	1	1	↑	XX	RCA2 [3:0]				BCA2 [3:0]				00h
4th Parameter	1	1	↑	XX	RCA3 [3:0]				BCA3 [3:0]				00h
5th Parameter	1	1	↑	XX	RCA4 [3:0]				BCA4 [3:0]				00h
6th Parameter	1	1	↑	XX	RCA5 [3:0]				BCA5 [3:0]				00h
7th Parameter	1	1	↑	XX	RCA6 [3:0]				BCA6 [3:0]				00h
8th Parameter	1	1	↑	XX	RCA7 [3:0]				BCA7 [3:0]				00h
9th Parameter	1	1	↑	XX	RCA8 [3:0]				BCA8 [3:0]				00h
10thParameter	1	1	↑	XX	RCA9 [3:0]				BCA9 [3:0]				00h
11thParameter	1	1	↑	XX	RCA10 [3:0]				BCA10 [3:0]				00h
12thParameter	1	1	↑	XX	RCA11 [3:0]				BCA11 [3:0]				00h
13thParameter	1	1	↑	XX	RCA12 [3:0]				BCA12 [3:0]				00h
14thParameter	1	1	↑	XX	RCA13 [3:0]				BCA13 [3:0]				00h
15thParameter	1	1	↑	XX	RCA14 [3:0]				BCA14 [3:0]				00h
16thParameter	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]				00h
Description	**RCA0 [3:0]** ~ **RCA15 [3:0]:** Gamma Macro-adjustment registers for red gamma curve. **BCA0 [3:0]** ~ **BCA15 [3:0]:** Gamma Macro-adjustment registers for blue gamma curve. X = void												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.36. Digital Gamma Control 2 (E3h)

E3h	DGAMCTRL (Digital Gamma Control 2)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1st Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				00h
2nd Parameter	1	1	↑	XX	RFA1 [3:0]				BFA1 [3:0]				00h
3rd Parameter	1	1	↑	XX	RFA2 [3:0]				BFA2 [3:0]				00h
4th Parameter	1	1	↑	XX	RFA3 [3:0]				BFA3 [3:0]				00h
5th Parameter	1	1	↑	XX	RFA4 [3:0]				BFA4 [3:0]				00h
6th Parameter	1	1	↑	XX	RFA5 [3:0]				BFA5 [3:0]				00h
7th Parameter	1	1	↑	XX	RFA6 [3:0]				BFA6 [3:0]				00h
8th Parameter	1	1	↑	XX	RFA7 [3:0]				BFA7 [3:0]				00h
9th Parameter	1	1	↑	XX	RFA8 [3:0]				BFA8 [3:0]				00h
10thParameter	1	1	↑	XX	RFA9 [3:0]				BFA9 [3:0]				00h
11thParameter	1	1	↑	XX	RFA10 [3:0]				BFA10 [3:0]				00h
12thParameter	1	1	↑	XX	RFA11 [3:0]				BFA11 [3:0]				00h
13thParameter	1	1	↑	XX	RFA12 [3:0]				BFA12 [3:0]				00h
14thParameter	1	1	↑	XX	RFA13 [3:0]				BFA13 [3:0]				00h
15thParameter	1	1	↑	XX	RFA14 [3:0]				BFA14 [3:0]				00h
16thParameter	1	1	↑	XX	RFA15 [3:0]				BFA15 [3:0]				00h
17thParameter	1	1	↑	XX	RFA16 [3:0]				BFA16 [3:0]				00h
18thParameter	1	1	↑	XX	RFA17 [3:0]				BFA17 [3:0]				00h
19thParameter	1	1	↑	XX	RFA18 [3:0]				BFA18 [3:0]				00h
20thParameter	1	1	↑	XX	RFA19 [3:0]				BFA19 [3:0]				00h
21thParameter	1	1	↑	XX	RFA20 [3:0]				BFA20 [3:0]				00h
22thParameter	1	1	↑	XX	RFA21 [3:0]				BFA21 [3:0]				00h
23thParameter	1	1	↑	XX	RFA22 [3:0]				BFA22 [3:0]				00h
24thParameter	1	1	↑	XX	RFA23 [3:0]				BFA23 [3:0]				00h
25thParameter	1	1	↑	XX	RFA24 [3:0]				BFA24 [3:0]				00h
26thParameter	1	1	↑	XX	RFA25 [3:0]				BFA25 [3:0]				00h
27thParameter	1	1	↑	XX	RFA26 [3:0]				BFA26 [3:0]				00h
28thParameter	1	1	↑	XX	RFA27 [3:0]				BFA27 [3:0]				00h
29thParameter	1	1	↑	XX	RFA28 [3:0]				BFA28 [3:0]				00h
30thParameter	1	1	↑	XX	RFA29 [3:0]				BFA29 [3:0]				00h
31thParameter	1	1	↑	XX	RFA30 [3:0]				BFA30 [3:0]				00h
32thParameter	1	1	↑	XX	RFA31 [3:0]				BFA31 [3:0]				00h

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33thParameter	1	1	↑	XX	RFA32 [3:0]	BFA32 [3;0]	00h
34thParameter	1	1	↑	XX	RFA33 [3:0]	BFA33 [3:0]	00h
35thParameter	1	1	↑	XX	RFA34 [3:0]	BFA34 [3:0]	00h
36thParameter	1	1	↑	XX	RFA35 [3:0]	BFA35 [3:0]	00h
37thParameter	1	1	↑	XX	RFA36 [3:0]	BFA36 [3:0]	00h
38thParameter	1	1	↑	XX	RFA37 [3:0]	BFA37 [3:0]	00h
39thParameter	1	1	↑	XX	RFA38 [3:0]	BFA38 [3:0]	00h
40thParameter	1	1	↑	XX	RFA39 [3:0]	BFA39 [3:0]	00h
41thParameter	1	1	↑	XX	RFA40 [3:0]	BFA40 [3:0]	00h
42thParameter	1	1	↑	XX	RFA41 [3:0]	BFA41 [3:0]	00h
43thParameter	1	1	↑	XX	RFA42 [3:0]	BFA42 [3:0]	00h
44thParameter	1	1	↑	XX	RFA43 [3:0]	BFA43 [3:0]	00h
45thParameter	1	1	↑	XX	RFA44 [3:0]	BFA44 [3:0]	00h
46thParameter	1	1	↑	XX	RFA45 [3:0]	BFA45 [3:0]	00h
47thParameter	1	1	↑	XX	RFA46 [3:0]	BFA46 [3:0]	00h
48thParameter	1	1	↑	XX	RFA47 [3:0]	BFA47 [3:0]	00h
49thParameter	1	1	↑	XX	RFA48 [3:0]	BFA48 [3:0]	00h
50thParameter	1	1	↑	XX	RFA49 [3:0]	BFA49 [3:0]	00h
51thParameter	1	1	↑	XX	RFA50 [3:0]	BFA50 [3:0]	00h
52thParameter	1	1	↑	XX	RFA51 [3:0]	BFA51 [3:0]	00h
53thParameter	1	1	↑	XX	RFA52 [3:0]	BFA52 [3:0]	00h
54thParameter	1	1	↑	XX	RFA53 [3:0]	BFA53 [3:0]	00h
55thParameter	1	1	↑	XX	RFA54 [3:0]	BFA54 [3:0]	00h
56thParameter	1	1	↑	XX	RFA55 [3:0]	BFA55 [3:0]	00h
57thParameter	1	1	↑	XX	RFA56 [3:0]	BFA56 [3:0]	00h
58thParameter	1	1	↑	XX	RFA57 [3:0]	BFA57 [3:0]	00h
59thParameter	1	1	↑	XX	RFA58 [3:0]	BFA58 [3:0]	00h
60thParameter	1	1	↑	XX	RFA59 [3:0]	BFA59 [3:0]	00h
61thParameter	1	1	↑	XX	RFA60 [3:0]	BFA60 [3:0]	00h
62thParameter	1	1	↑	XX	RFA61 [3:0]	BFA61 [3:0]	00h
63thParameter	1	1	↑	XX	RFA62 [3:0]	BFA62 [3:0]	00h
64thParamete	1	1	↑	XX	RFA63 [3:0]	BFA63 [3:0]	00h
Description	**RFA0 [3:0]** ~ **RFA63 [3:0]**: Gamma Micro-adjustment register for red gamma curve. **BFA0 [3:0]** ~ **BFA63 [3:0]**: Gamma Micro-adjustment register for blue gamma curve. X = void						
Restriction							

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Register Availability	

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.37. Set Image Function (E9h)

E9h	SETIMAGE (Set Image Function)												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	0	0	1	E9h
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	DB_EN	00h
Description	**DB_EN:** Enable 24-bits Data Bus; users can use DB23~DB0 as 24-bits data input. X = void												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.38. Adjust Control 2 (F2h)

F2h	Adjust Control 2												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
1st Parameter	1	1	↑	XX	0	1	0	1	1	0	0	Chopper_ delay_opt	58h
2nd Parameter	1	1	↑	XX	0	GSW_TG1[5:0]						0	04h
3rd Parameter	1	1	↑	XX	0	0	0	1	0	0	1	0	12h
4th Parameter	1	1	↑	XX	0	0	0	0	0	0	1	0	02h
5th Parameter	1	1	↑	XX	0	EQTI[2:0]			0	0	1	0	22h
6th Parameter	1	1	↑	XX	0	1	0	0	0	0	1	0	42h
7th Parameter	1	1	↑	XX	1	1	1	1	1	1	1	1	FFh
8th Parameter	1	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
9th Parameter	1	1	↑	XX	1	0	0	1	0	0	0	0	90h
10thParameter	1	1	↑	XX	0	0	0	1	GSW_Mode [1:0]		0	0	14h
11thParameter	1	1	↑	XX	Chopper_sel [1:0]		0	0	1	0	0	0	88h

Description

Chopper_delay_opt: Source Op-amp chopper function option.

Chopper_delay_opt	Description
0	Original Chopper
1	Chopper delay one line

Chopper_sel [1:0]: Source Op-amp chopper function option.

Chopper_opt	Chopper_sel[1:0]		Descripition
1	0	0	Close chopper
1	0	1	1 frame chopper
1	1	0	2 frame chopper
1	1	1	3 frame chopper
0	0	0	1-line(1 frame chopper polarity change)
0	0	1	2-line(1 frame chopper polarity change)
0	1	0	1-line(2 frame chopper polarity change)
0	1	1	2-line(2 frame chopper polarity change)

*Chopper_opt on F9h command.

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Eqrti [2:0]: Source EQ internal timing adjustment. The timing can be adjusted from 0 to 7 time scales.（time scal: op_clk）

Eqrti [2:0]			Descripition
0	0	0	1 unit op_clk
0	0	1	2 unit op_clk
0	1	0	3 unit op_clk
0	1	1	4 unit op_clk
1	0	0	5 unit op_clk
1	0	1	6 unit op_clk
1	1	0	7 unit op_clk
1	1	1	8 unit op_clk

GSW_Mode[1:0]: Slope function setting.

GSW_Mode[1:0]		Description
0	0	Sharp slope
0	1	Normal slope
1	0	Gently slope
1	1	GSW off

GSW_TG1[5:0]: Gate modulation timing control. The timing can be adjusted:

Gsw_tg1[5:0]						Description
0	0	0	0	0	0	40 unit Osc_clk
0	0	0	0	0	1	44 unit Osc_clk
0	0	0	0	1	0	48 unit Osc_clk
0	0	0	0	1	1	52 unit Osc_clk
0	0	0	1	0	0	56 unit Osc_clk
0	0	0	1	0	1	60 unit Osc_clk
0	0	0	1	1	0	64 unit Osc_clk
0	0	0	1	1	1	68 unit Osc_clk
0	0	1	0	0	0	72 unit Osc_clk
0	0	1	0	0	1	76 unit Osc_clk
0	0	1	0	1	0	80 unit Osc_clk
0	0	1	0	1	1	84 unit Osc_clk
0	0	1	1	0	0	88 unit Osc_clk
0	0	1	1	0	1	92 unit Osc_clk
0	0	1	1	1	0	96 unit Osc_clk
0	0	1	1	1	1	100 unit Osc_clk
0	1	0	0	0	0	104 unit Osc_clk
0	1	0	0	0	1	108 unit Osc_clk
0	1	0	0	1	0	112 unit Osc_clk

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0	1	0	0	1	1	116 unit Osc_clk
0	1	0	1	0	0	120 unit Osc_clk
0	1	0	1	0	1	124 unit Osc_clk
0	1	0	1	1	0	128 unit Osc_clk
0	1	0	1	1	1	132 unit Osc_clk
0	1	1	0	0	0	136 unit Osc_clk
0	1	1	0	0	1	140 unit Osc_clk
0	1	1	0	1	0	144 unit Osc_clk
0	1	1	0	1	1	148 unit Osc_clk
0	1	1	1	0	0	152 unit Osc_clk
0	1	1	1	0	1	156 unit Osc_clk
0	1	1	1	1	0	160 unit Osc_clk
0	1	1	1	1	1	164 unit Osc_clk
1	0	0	0	0	0	168 unit Osc_clk
1	0	0	0	0	1	172 unit Osc_clk
1	0	0	0	1	0	176 unit Osc_clk
1	0	0	0	1	1	180 unit Osc_clk
1	0	0	1	0	0	184 unit Osc_clk
1	0	0	1	0	1	188 unit Osc_clk
1	0	0	1	1	0	192 unit Osc_clk
1	0	0	1	1	1	196 unit Osc_clk
1	0	1	0	0	0	200 unit Osc_clk
1	0	1	0	0	1	204 unit Osc_clk
1	0	1	0	1	0	208 unit Osc_clk
1	0	1	0	1	1	212 unit Osc_clk
1	0	1	1	0	0	216 unit Osc_clk
1	0	1	1	0	1	220 unit Osc_clk
1	0	1	1	1	0	224 unit Osc_clk
1	0	1	1	1	1	228 unit Osc_clk
1	1	0	0	0	0	232 unit Osc_clk
1	1	0	0	0	1	236 unit Osc_clk
1	1	0	0	1	0	240 unit Osc_clk
1	1	0	0	1	1	244 unit Osc_clk
1	1	0	1	0	0	248 unit Osc_clk
1	1	0	1	0	1	252 unit Osc_clk
1	1	0	1	1	0	256 unit Osc_clk
1	1	0	1	1	1	260 unit Osc_clk
1	1	1	0	0	0	264 unit Osc_clk
1	1	1	0	0	1	268 unit Osc_clk
1	1	1	0	1	0	272 unit Osc_clk
1	1	1	0	1	1	276 unit Osc_clk
1	1	1	1	0	0	280 unit Osc_clk
1	1	1	1	0	1	284 unit Osc_clk
1	1	1	1	1	0	288 unit Osc_clk
1	1	1	1	1	1	292 unit Osc_clk

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<table>
<tr><td></td><td>X = void</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

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5.3.39. Adjust Control 3 (F7h)

F7h	Adjust Control 3												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	1	F7h
1st Parameter	1	1	↑	XX	1	0	1	0	1	0	0	1	A9h
2nd Parameter	1	1	↑	XX	0	1	0	1	0	0	0	1	51h
3rd Parameter	1	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
4th Parameter	1	1	↑	XX	DSI_18_option	0	0	0	0	0	1	0	82h

Description

DSI_18_option: DSI 18bit option

DSI_18_option	Description
0	DSI write DCS command, use stream packet RGB 666
1	DSI write DCS command, use loose packet RGB 666

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.40. Adjust Control 4 (F8h)

F8h	Adjust Control 4												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	0	0	0	F8h
1st Parameter	1	1	↑	XX	0	0	1	0	0	0	0	1	21h
2nd Parameter	1	1	↑	XX	0	0	0	0	0	1	3-Gamma _Enable	Dither _Enable	04h
Description	**3-Gamma_Enable:** 3-Gamma function enable. **Dither_Enable:** Dither function enable. X = void												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.41. Adjust Control 5(F9h)

F9h	Adjust Control 5												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	0	0	1	F9h
1st Parameter	1	1	↑	XX	0	0	0	0	Chopper_opt	0	0	0	00h
Description	**Chopper_opt**: Source Op-amp chopper function option.Please refer to F2h (Section 5.3.38) for more information. X = void												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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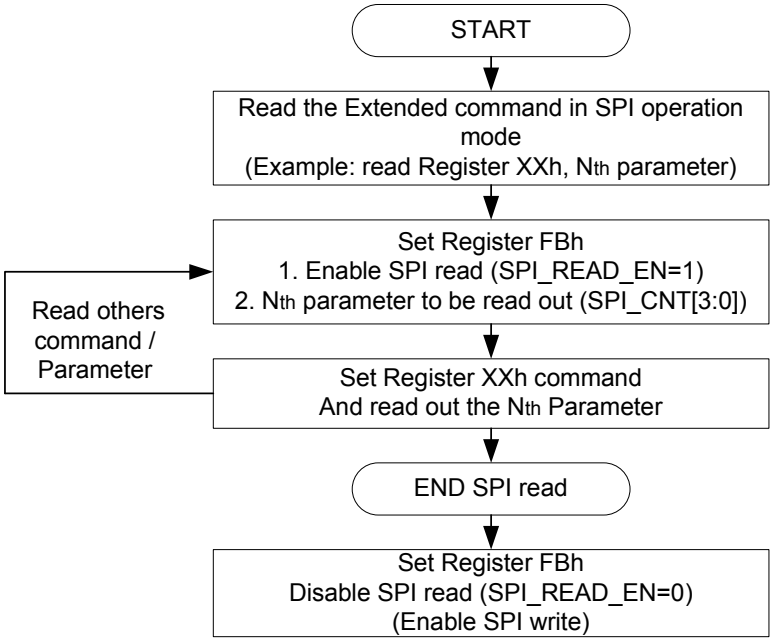
5.3.42. SPI Read Command Setting (FBh)

FBh	Read EXTC command is SPI mode												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	0	1	1	FBh
1st Parameter	1	1	↑	XX	SPI_READ_EN	0	0	0	SPI_CNT [3:0]				00h

Description

SPI_READ_EN: SPI read enable (see Note)

SPI_CNT [3:0]: SPI read parameter number (see Note)



Note: Setting "RFBh" once is only useful to read one parameter of the register one time; it is necessary to set "RFBh" again for the next read.

X = void

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.43. Adjust Control 6 (FCh)

FCh	Adjust Control 6												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	0	0	FCh
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00h
2nd Parameter	1	1	↑	XX	0	0	0	NOWI [4:0]					05h

Description

NOWI [4:0]:Gate driver non-overlap timing control.

NOWI [4:0]					Descripition
0	0	0	0	1	1 unit op_clk
0	0	0	1	0	2 unit op_clk
0	0	0	1	1	3 unit op_clk
0	0	1	0	0	4 unit op_clk
0	0	1	0	1	5 unit op_clk
0	0	1	1	0	6 unit op_clk
0	0	1	1	1	7 unit op_clk
0	1	0	0	0	8 unit op_clk
0	1	0	0	1	9 unit op_clk
0	1	0	1	0	10 unit op_clk
0	1	0	1	1	11 unit op_clk
0	1	1	0	0	12 unit op_clk
0	1	1	0	1	13 unit op_clk
0	1	1	1	0	14 unit op_clk
0	1	1	1	1	15 unit op_clk
1	0	0	0	0	16 unit op_clk

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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5.3.44. Adjust Control 7 (FFh)

FFh	Adjust Control 7												
	D/CX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	0	0	FFh
1st Parameter	1	1	↑	XX	SAT_AXIS_EN	1	0	0	0	0	1	0	42h
Description	**SAT_AXIS_EN:** 24-axis adjustment enable singal for color enchance (RB9h, RBAh).												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

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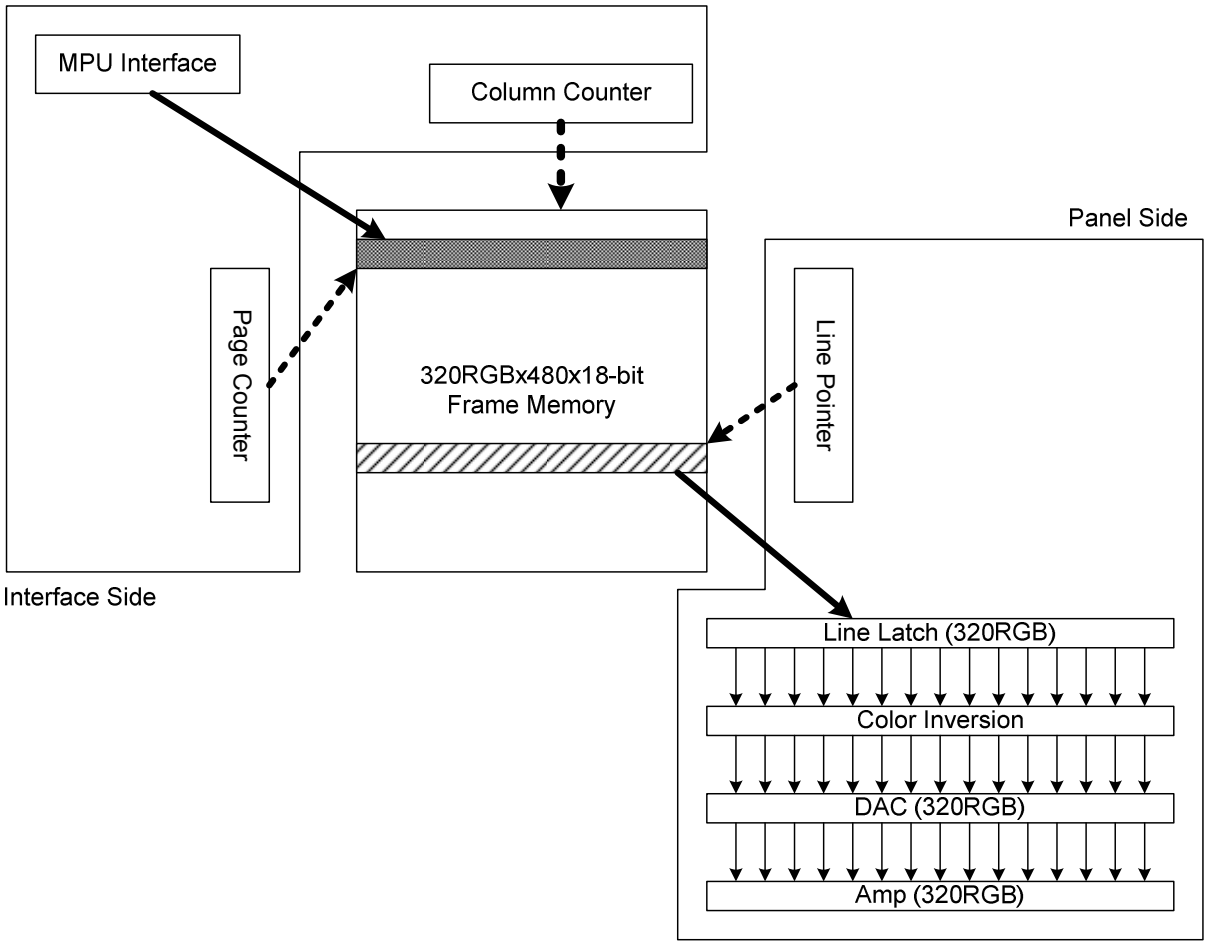
6. Display Data RAM

6.1. Configuration

The 320 x 480 x 18-bit graphic type static RAM has a 345,600-byte memory allowing the storage of a 320 (RGB) x 480 image with the 18-bit resolution.

Panel Read and Interface Read (or Interface Write) can occur simultaneously with the Frame Memory. This process will not cause any visible effects on the display.



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6.2. Memory to Display Address Mapping

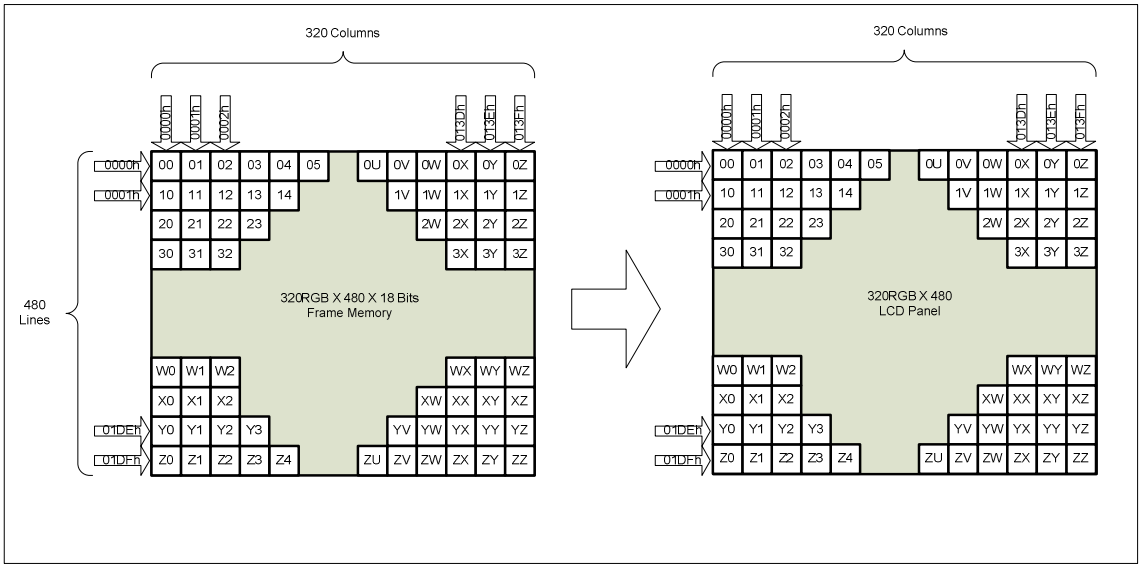
6.2.1. Fully Display

Example: 320 (RGB) x 480 dot display mode

(1) In this mode, the content of the Frame Memory within an area where the column pointer is 0000h to 013Fh and page pointer is 0000h to 01DFh is displayed.

(2) NORON (Normal Display Mode On) instruction (R13h).

(3) SC = 0 x 0000h, EC = 0 x 013Fh (R2Ah) and SP = 0 x 0000h, EP = 0 x 01DFh (R2Bh), ML = 0.



6.2.2. Vertical Scrolling Display

The Vertical Scrolling Mode is determined by Vertical Scrolling Definition (33h) and Vertical Scrolling Start Address (37h) commands. The Vertical Scroll Mode function is explained by the examples of (TFA + VSA + BFA) = 480 in Figure 128.

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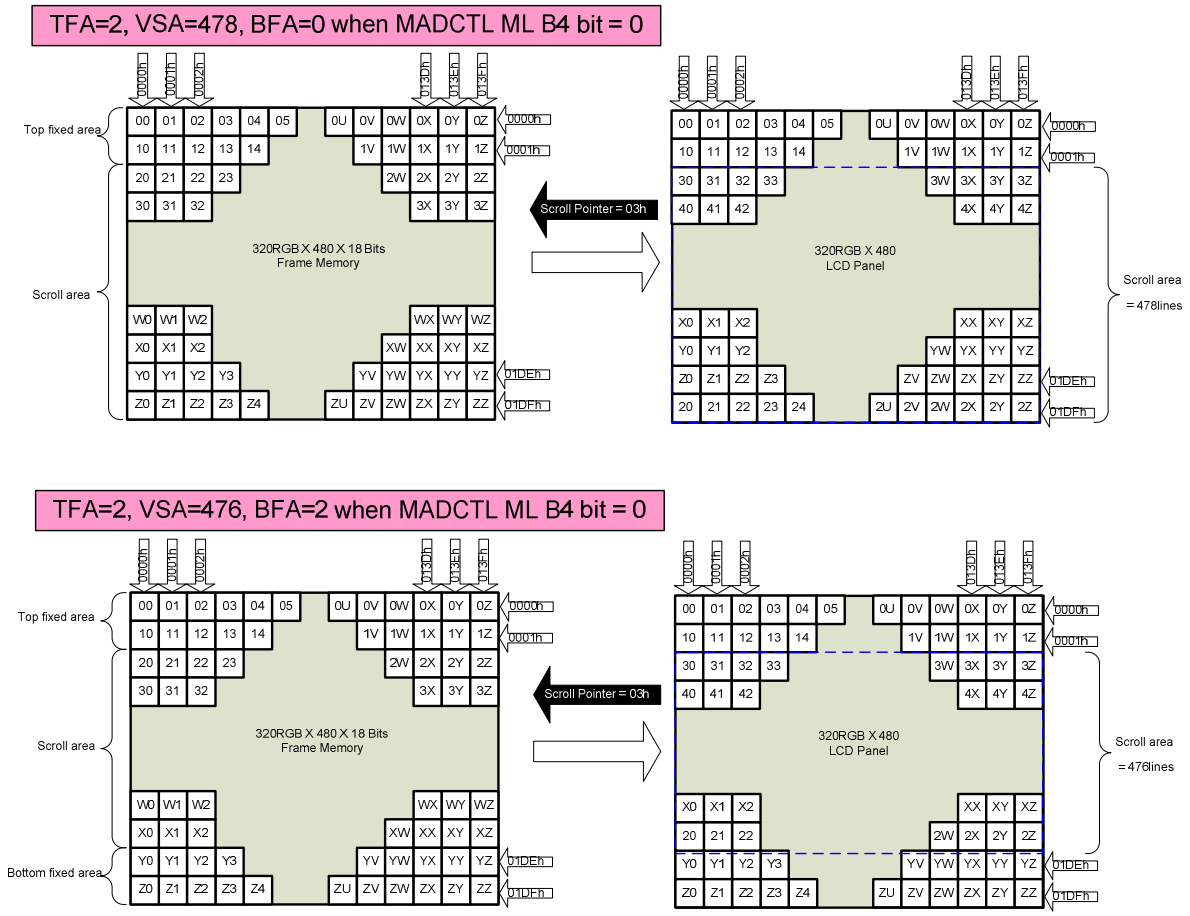


Figure 128: Vertical Scrolling Mode Function

Note: When Vertical Scrolling Definition Parameters (TFA + VSA + BFA) ≠ 480, the Scrolling Mode is undefined.

6.2.3. Vertical Scrolling 320 (RGB) (H) x 480 (V) Example

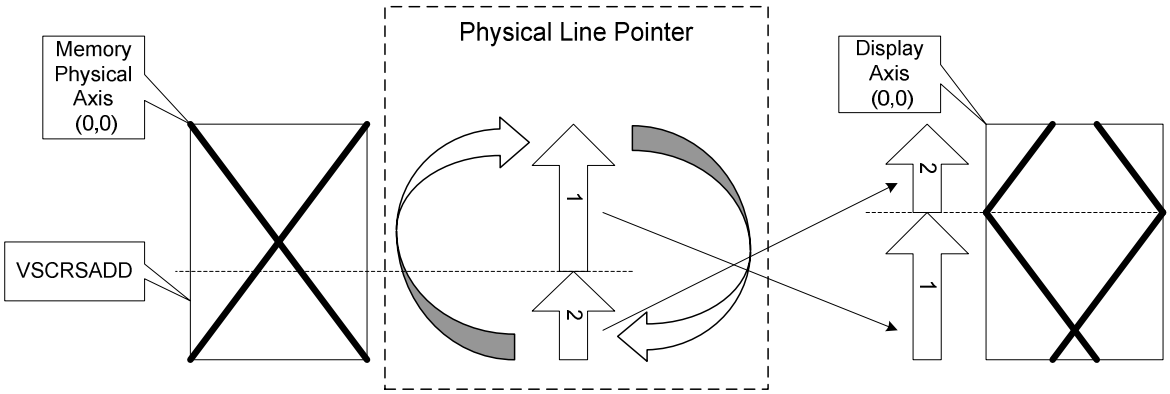
6.2.3.1. Case 1: TFA + VSA + BFA ≠ 480

This setting is prohibited because it will cause a display output error.

6.2.3.2. Case 2: TFA + VSA + BFA = 480

The operations of the Rolling Scrolling are explained by those examples below.

When TFA=0, VSA=480, BFA=0, VSCRSADD=40 and MADCTL ML B4 bit = 1



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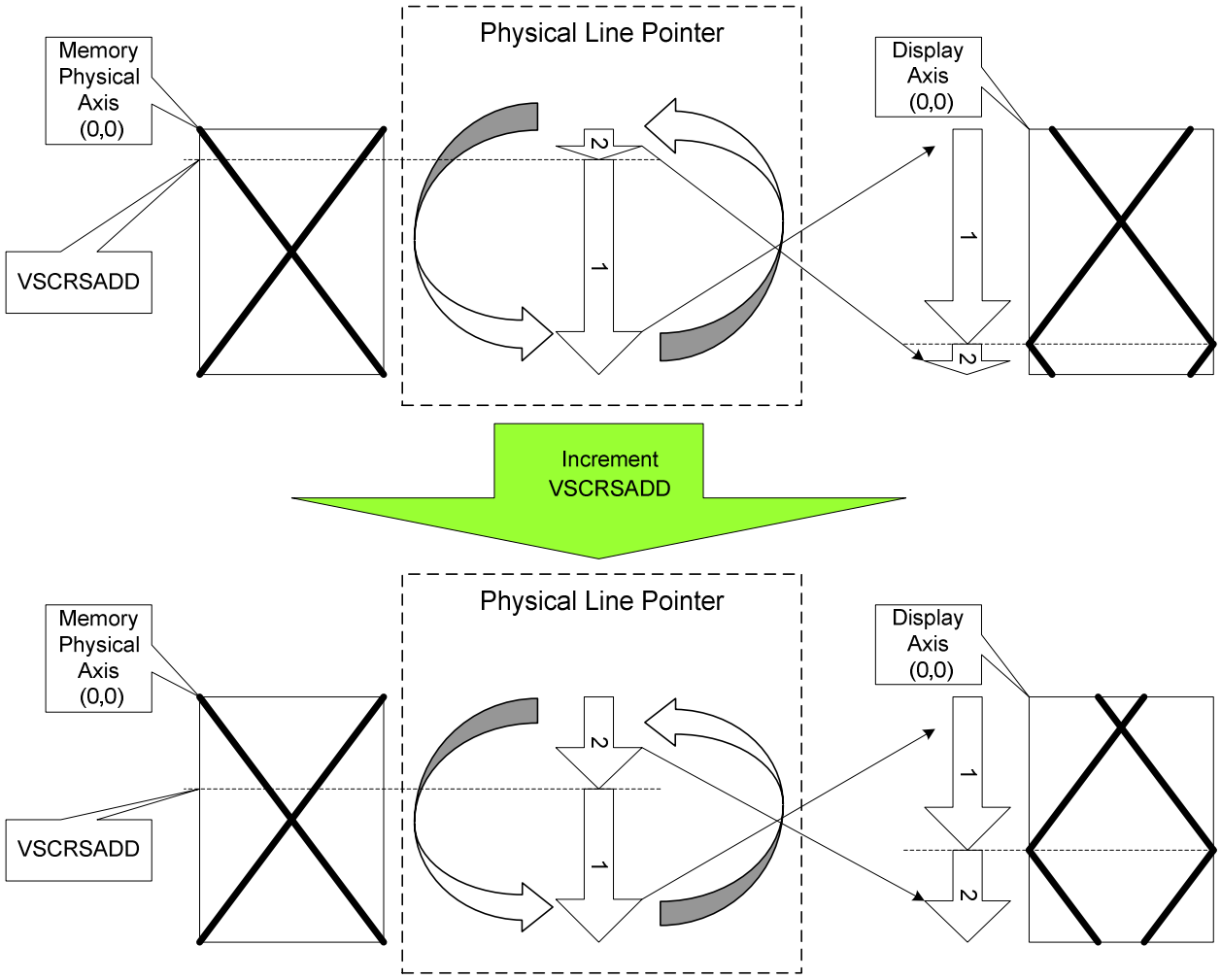
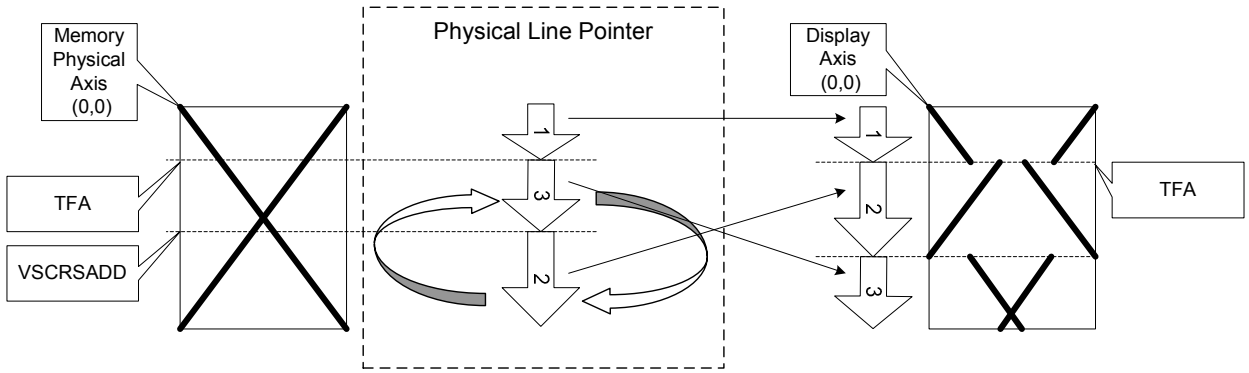
When TFA=0, VSA=480, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



When TFA=30, VSA=450, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



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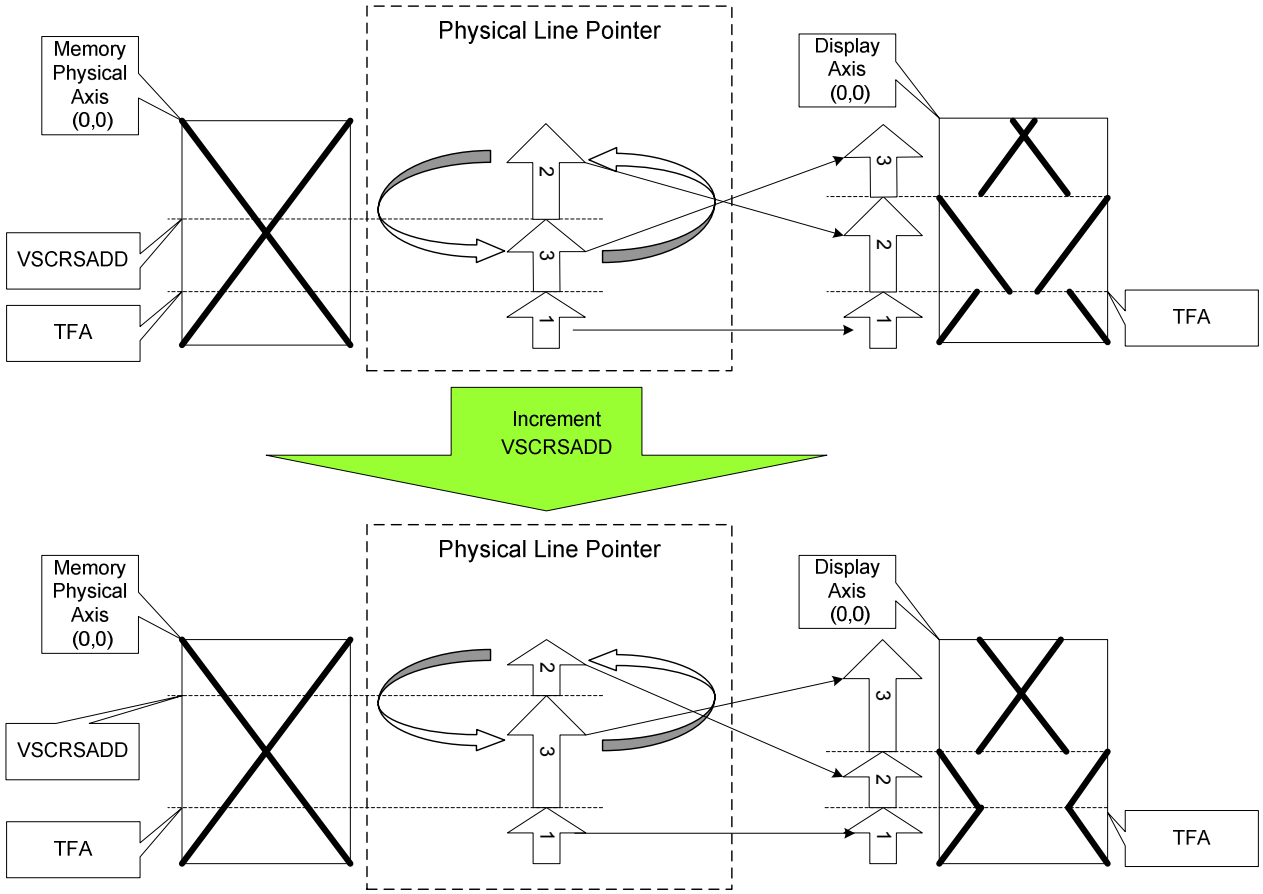
When TFA=30, VSA=450, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



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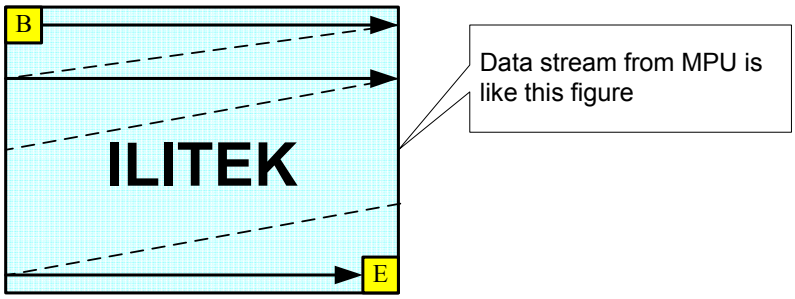
6.3. MCU to Memory Write/Read Direction



The data is written in the order illustrated above. The Counter, indicating where in the physical memory the data is to be written, is controlled by the Memory Data Access Control Command, Bits D7, D6, and D5, as described below.

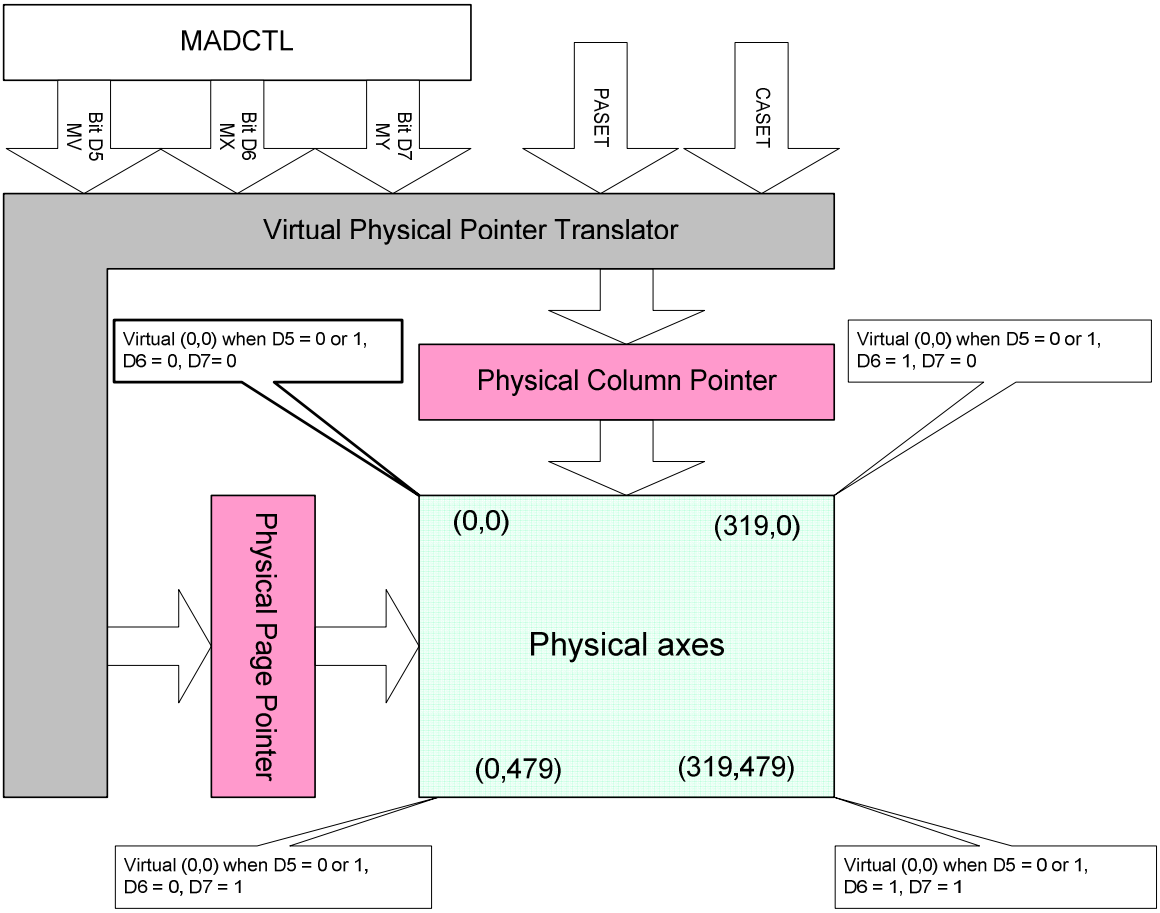


Figure 129: MV, MX, MY Setting (320 (RGB) x 480)

D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Page Pointer)	Direct to Physical Column Pointer

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1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to Start column	Return to Start Page
Complete Pixel Read/Write action	Incremented by 1	No change
The Column values are large than End Column	Return to Start column	Incremented by 1
The Page counter are large than End Page	Return to Start column	Return to Start Page

Note: One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

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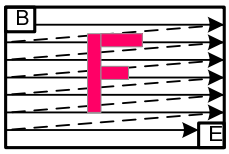
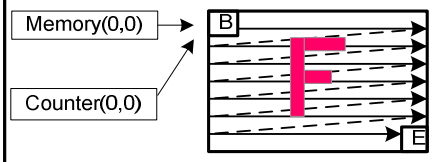
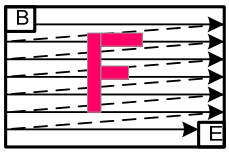
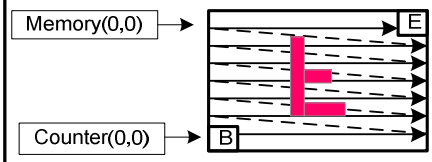
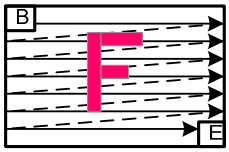
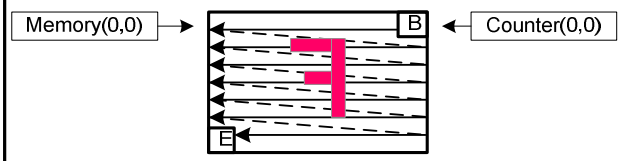
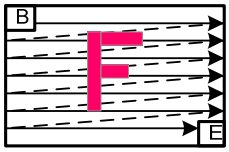
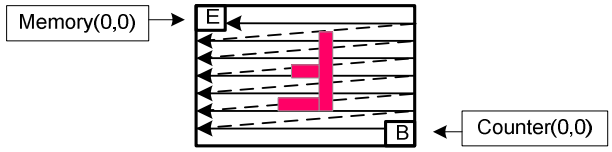
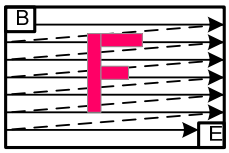
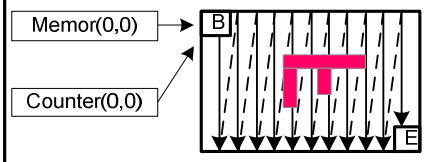
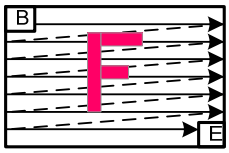
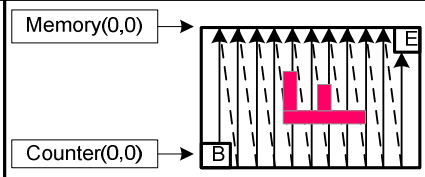
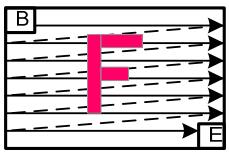
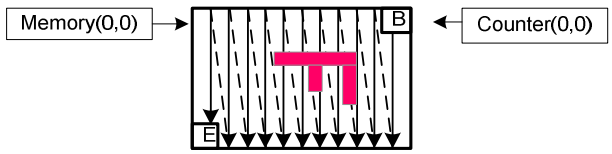
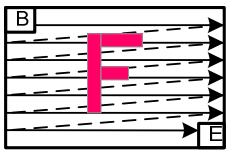
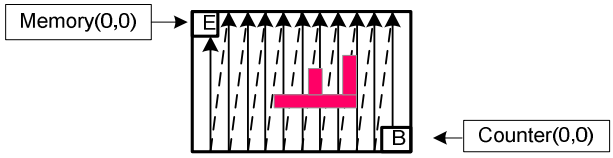
Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

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7. Tearing Effect Information

The Tearing Effect Line (TE) signal supplies panel synchronization information to the MCU. The TE signal determines the position for refreshing GRAM data for the display panel; the MCU can reference the TE to decide when to send image data in order to avoid abnormal visual effect on the display panel. The TE signal is enabled or disabled by the Tearing Effect Line ON or OFF commands. The TE Line output mode is defined by the parameter of the “Tearing Effect Line ON” command.

Tearing Effect information is sent in two different ways:

- Separated Line, which is the Tearing Effect Line (TE)
- Tearing Effect Bus Trigger (TEE): the ILI9488 sends a trigger to inform the MCU.

The TE is used in the MCU parallel interface, and can also be used in the DSI if the Tearing Effect Bus Trigger (TEE) is not possible to be used. However, the Tearing Effect (TEE) Bus Trigger can only be used in the DSI.

7.1. Tearing Effect Line

7.1.1. Tearing Effect Line Modes

Mode 1, illustrated in Figure 130, the Tearing Effect output signal consists of V-Sync information only:

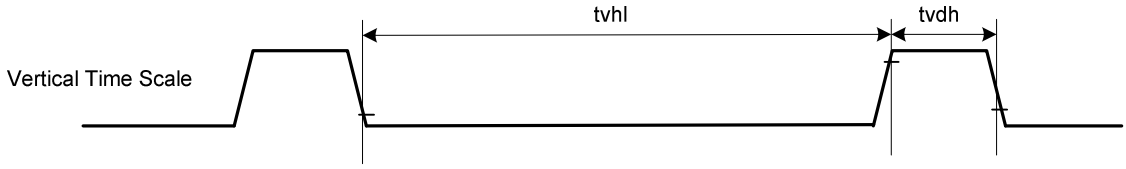

Figure 130: Tearing Effect Line Mode 1

tvdh = The LCD display is not updated from the Frame Memory.

tvdl = The LCD display is updated from the Frame Memory (except the Invisible Line – see the figure above).

Mode 2, illustrated in Figure 131, the Tearing Effect output signal consists of V-Sync and H-Sync information; there is one V-sync and “N” H-sync pulses per field. The resolution is 320 (RGB) x 480, and N = 480.

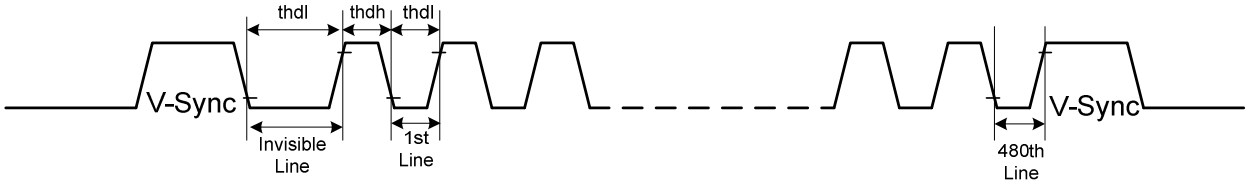

Figure 131: Tearing Effect Line Mode 2

thdh = The LCD display is not updated from the Frame Memory.

thdl = The LCD display is updated from the Frame Memory (except the Invisible Line – see the figure above).

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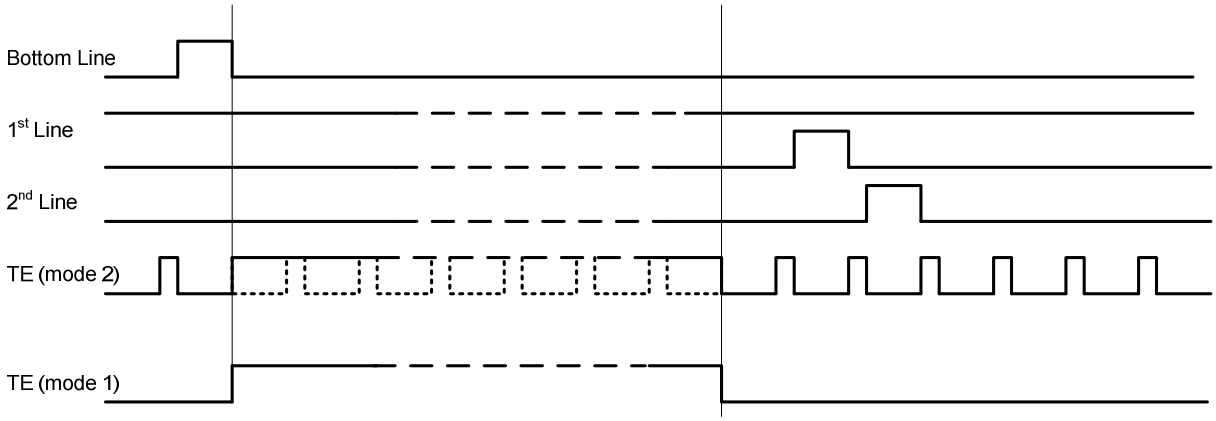
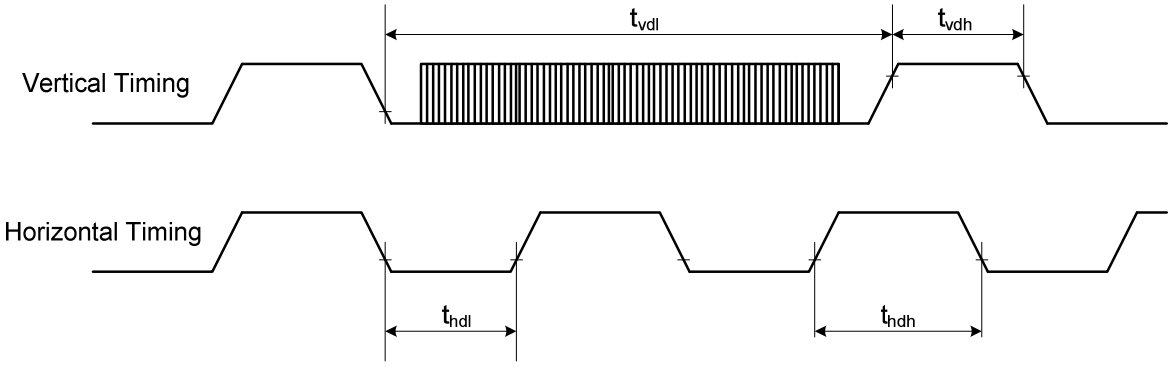


Note: During the Sleep In Mode, the Tearing Effect Output Pin is active Low.

7.1.2. Tearing Effect Line Timing

The tearing effect signal is described below:



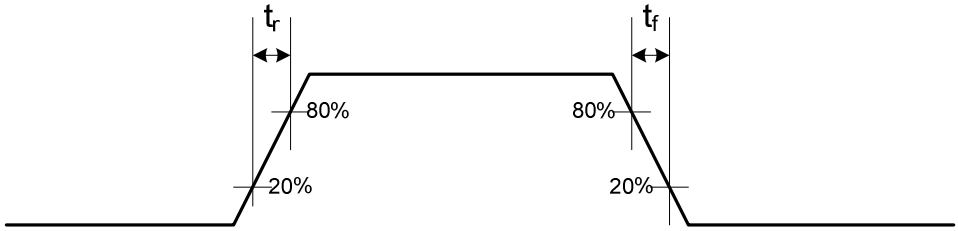
The AC characteristic of the Tearing Effect Signal is: 320 (RGB) x 480 Resolution.

Table 36: Tearing Effect Line Timing

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	10	40	ms	
t_{vdh}	Vertical timing high duration	500	2000	us	
t_{hdl}	Horizontal timing low duration	15	75	us	
t_{hdh}	Horizontal timing high duration	1	5	us	

Notes:

1. The timings in Table 36 are applied when MADCTL D4 = 0 and D4 = 1.
2. The signal's rising and falling times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid the Tearing Effect.

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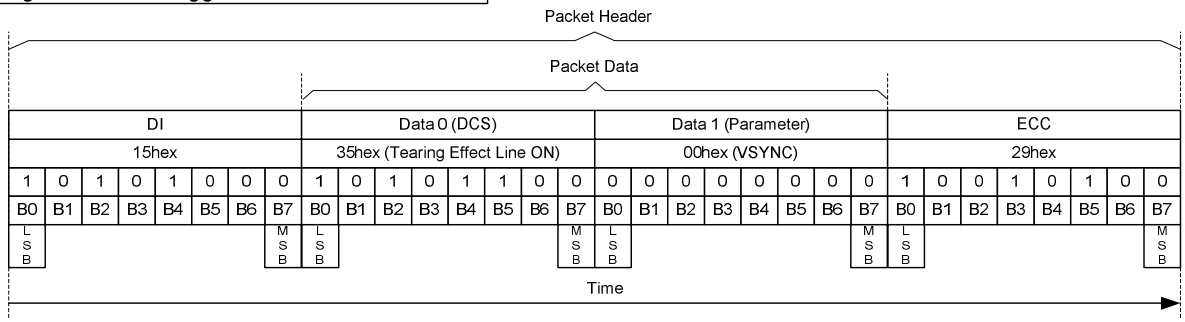
7.2. Tearing Effect Bus Trigger

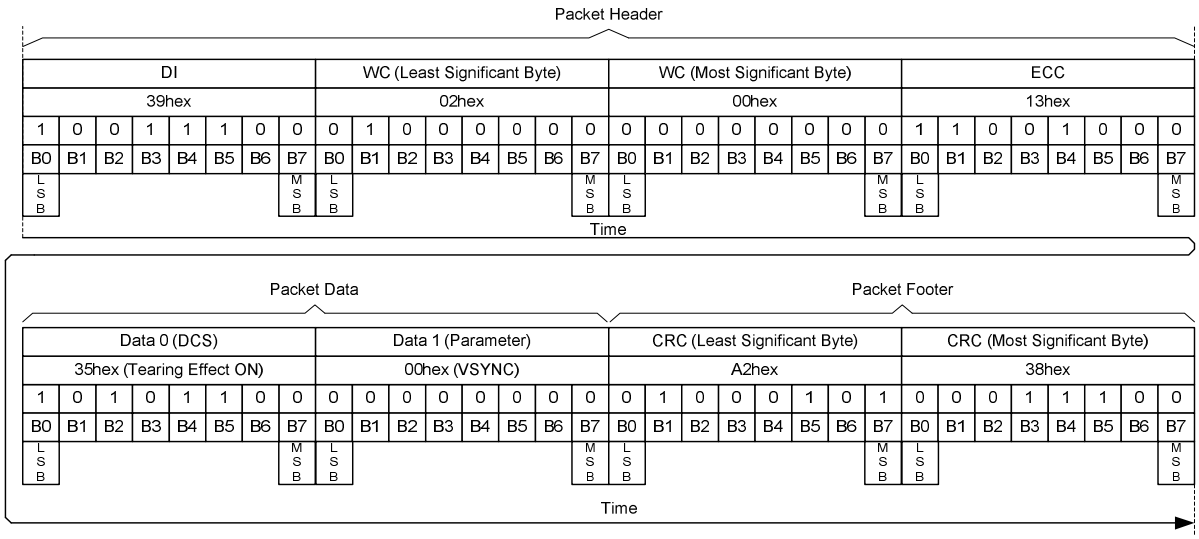
Tearing Effect Bus Trigger information supplies a Panel synchronization trigger to the MCU and this Tearing Effect Bus Trigger information can be enabled or disabled by Tearing Effect Line Off (34h) and Tearing Effect Line On (35h) commands when the only mode of the Tearing Effect Signal is VSYNC information. The ILI9488 sends this trigger information in the Escape Mode after the Bus Turnaround (BTA) and the Tearing Effect Bus Trigger can only be used in the DSI without the TE line.

7.2.1. Tearing Effect Bus Trigger Enable

Tearing Effect Bus Trigger Enable - Short Packet



Tearing Effect Bus Trigger Enable - Long Packet



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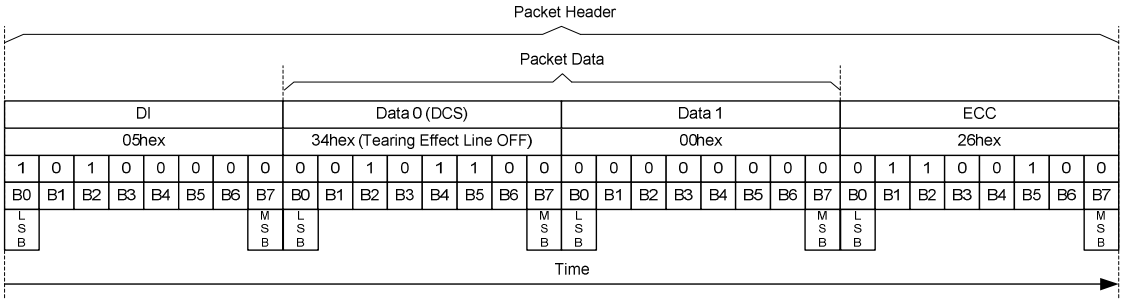
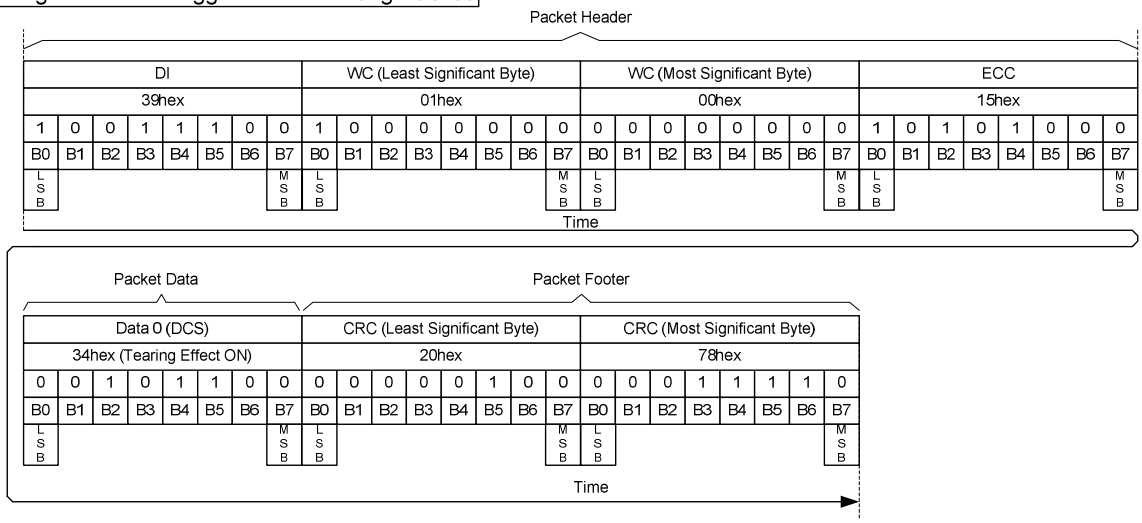
7.2.2. Tearing Effect Bus Trigger Disable

The MCU can disable the Tearing Effect Bus Trigger on the ILI9488 in 2 different ways: when a Short Packet (SPa) or Long Packet (LPa) is used. These both possibilities are illustrated below.

Tearing Effect Bus Trigger Disable - Short Packet



Tearing Effect Bus Trigger Disable - Long Packet



7.2.3. Tearing Effect Bus Trigger Sequences

Tearing Effect Bus Trigger Enable Sequence – DCS Write (Long Packet) and HSDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	➔	-	-	Start
2	DCS Write (LPa)	HSDT	➔	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	➔	-	-	
4	-	BTA	⇔	BTA	-	Interface Control Change from the MCU to the display module (ILI9488)
5	-	-	←	LP-11	-	If No Error, then go to Line 7 If Error occurs, then go to Line 12
6						
7	-	-	←	TEE	-	TE (Escape Trigger) on the next VSYNC
8	-	-	←	LP-11	-	
9	-	BTA	⇔	BTA	-	Interface Control Change from the display module (ILI9488) to MCU
10	-	LP-11	➔	-	-	End

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11						
12	-	-	←	LPDT	Acknowledge Error Report	Error Report
13	-	-	←	LP-1	-	
14	-	BTA	⇔	BTA	-	
15	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Enable Sequence – DCS Write (Long Packet) and LPDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (LPa)	LPDT	→	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	→	-	-	
4	-	BTA	⇔	BTA	-	Interface Control Change from the MCU to the display module (ILI9488)
5	-	-	←	LP-11	-	If No Error, then go to Line 7 If Error occurs, then go to Line 12
6						
7	-	-	←	TEE	-	TE (Escape Trigger) on the next VSYNC
8	-	-	←	LP-11	-	
9	-	BTA	⇔	BTA	-	Interface Control Change from the display module (ILI9488) to MCU
10	-	LP-11	→	-	-	End
11						
12	-	-	←	LPDT	Acknowledge Error Report	Error Report
13	-	-	←	LP-1	-	
14	-	BTA	⇔	BTA	-	
15	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Enable Sequence – DCS Write, 1 Parameter (Short Packet) and HSDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	HSDT	→	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	→	-	-	
4	-	BTA	⇔	BTA	-	Interface Control Change from the MCU to the display module (ILI9488)
5	-	-	←	LP-11	-	If No Error, then go to Line 7 If Error occurs, then go to Line 12
6						
7	-	-	←	TEE	-	TE (Escape Trigger) on the next VSYNC
8	-	-	←	LP-11	-	
9	-	BTA	⇔	BTA	-	Interface Control Change from the display module (ILI9488) to MCU
10	-	LP-11	→	-	-	End

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11						
12	-	-	←	LPDT	Acknowledge Error Report	Error Report
13	-	-	←	LP-1	-	
14	-	BTA	⇔	BTA	-	
15	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Enable Sequence – DCS Write, 1 Parameter (Short Packet) and LPDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	LPDT	→	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	→	-	-	
4	-	BTA	⇔	BTA	-	Interface Control Change from the MCU to the display module (ILI9488)
5	-	-	←	LP-11	-	If No Error, then go to Line 7 If Error occurs, then go to Line 12
6						
7	-	-	←	TEE	-	TE (Escape Trigger) on the next VSYNC
8	-	-	←	LP-11	-	
9	-	BTA	⇔	BTA	-	Interface Control Change from the display module (ILI9488) to MCU
10	-	LP-11	→	-	-	End
11						
12	-	-	←	LPDT	Acknowledge Error Report	Error Report
13	-	-	←	LP-1	-	
14	-	BTA	⇔	BTA	-	
15	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Disable Sequence – DCS Write, No Parameter (Short Packet) and LPDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	LPDT	→	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Disable Sequence – DCS Write, No Parameter (Short Packet) and HSDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	HSDT	→	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	→	-	-	End

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8. CABC (Content Adaptive Brightness Control)

The CABC, a dynamic backlight control function, drastically reduces power consumption of the luminance source. The ILI9488 refers the gray scale content of display image to output in PWM waveform then to the LED driver for backlight brightness control. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

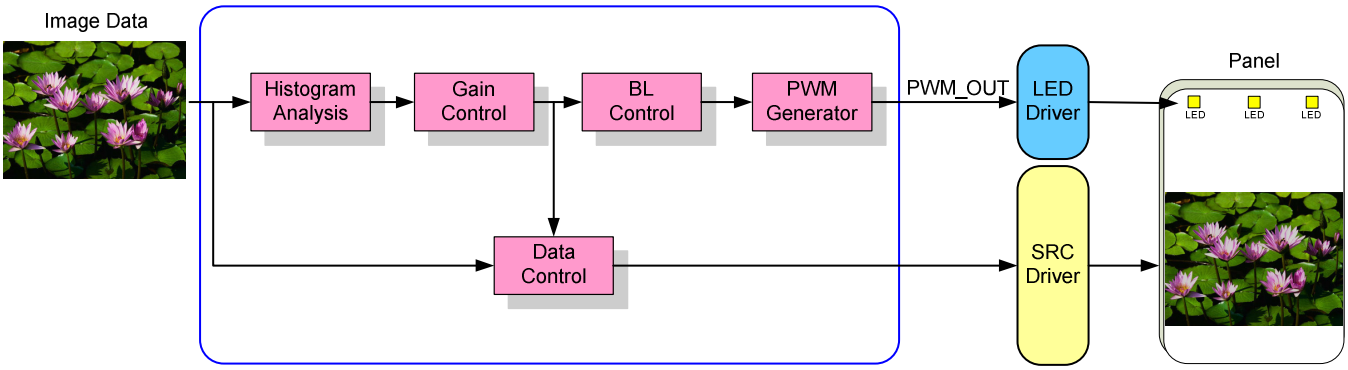

Figure 132: CABC Block Diagram

The ILI9488 can calculate the backlight brightness level and send a PWM_OUT pulse to the LED driver via PWM_OUT pin for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below:

$$fpwm_out = \frac{18\,MHz}{(PWM_DIV[7:0]+1)\ x\ 255}$$

Figure 133 is the basic timing diagram which is applied from the ILI9488 line order to control a LED driver.

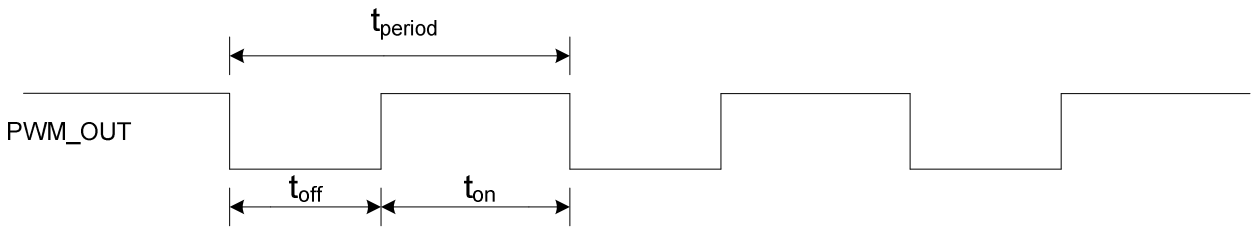

Figure 133: PWM OUT On/Off Period

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9. Color Enhancement Function

The Color Enhancement Function enhances saturation by calculating image data of the display on the liquid crystal panel. The saturation enhancement coefficients of red, yellow, green, cyan, blue, magenta, are set independently. The function enhances color and makes pixel colors more vivid.

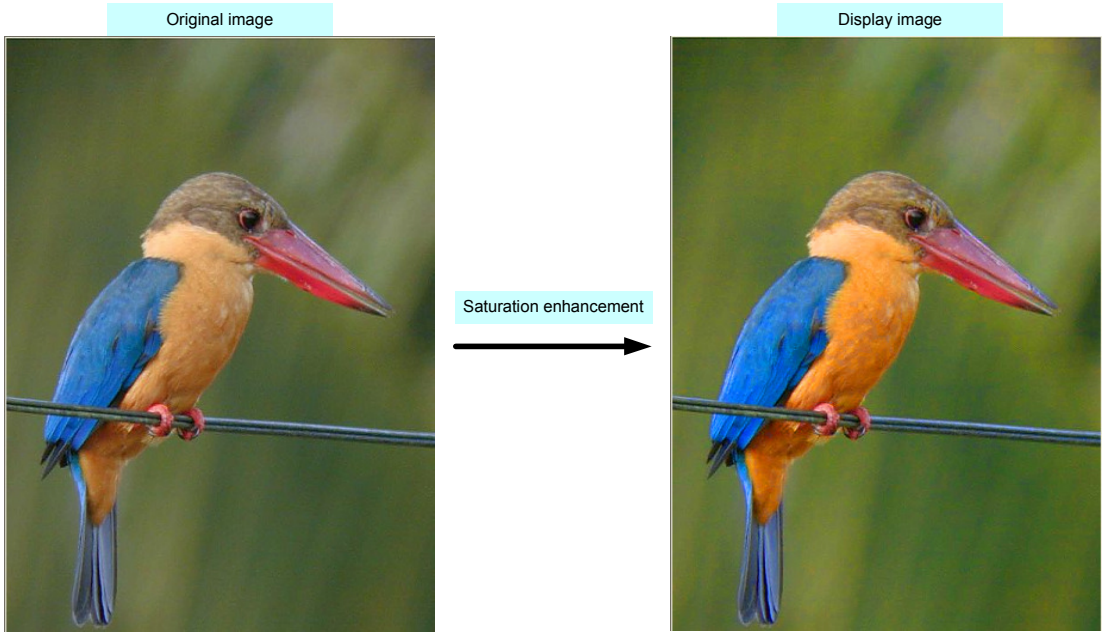

Figure 134: Saturation Enhancement Image

The displayed image with color enhanced is generated when the saturation enhancement coefficients of the input image are 1.0 or more. See the saturation diagram Figure 135. The colors of the input image are enhanced. Both green and magenta colors keep the original gray value without enhanced.

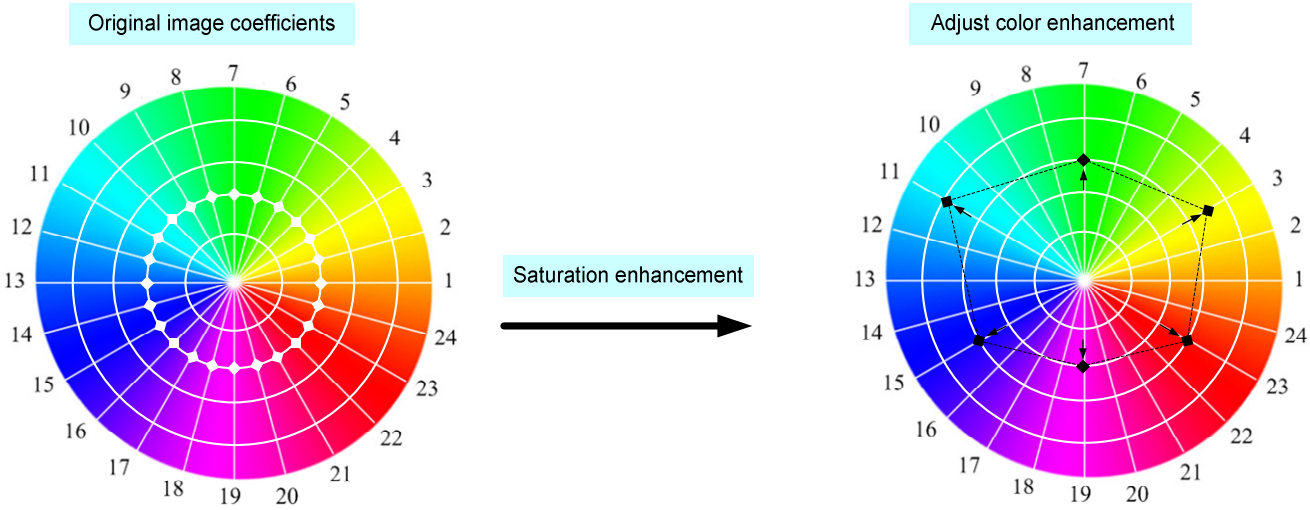

Figure 135: 6-axis Color Enhancement

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10. Sleep Out Command and Self-Diagnostic Functions

10.1. Register Loading Detection

The Sleep Out command (Sleep Out (11h)) is a trigger for an internal function of the ILI9488, which indicates if the ILI9488 loading function of factory default values from EEPROM (or similar devices) to registers of the display controller works properly. Factory values of the EEPROM and register values of the display controller are compared by the display controller (1st step: compare register and EEPROM values, 2nd step: load the EEPROM value to register). If those two values (EEPROM and register values) are the same, the bit D7 is inverted (= increased by 1), which is defined in the command "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D7). If those two values are not the same, this bit (D7) is not inverted (= not increased by 1), and the used TE-line is set to low (registers will keep their current values) and can only be reactivated by the "Tearing Effect Line On (35h)" command.

The flow chart for this internal function is:

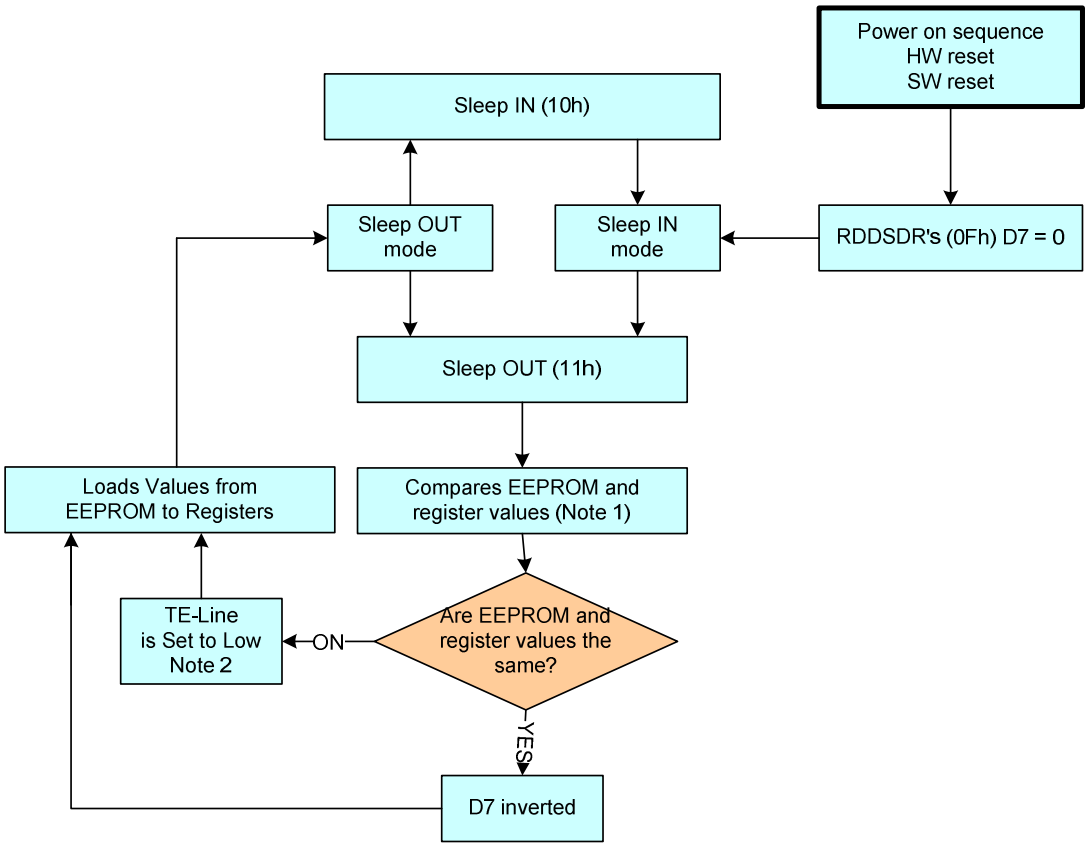

Figure 136: Register Loading Detection

Notes:

1. If the EEPROM and register values are not compared and loaded, they can be changed by commands 00h to AFh and DAh to DDh.
2. This information is only used when the TE line is used.

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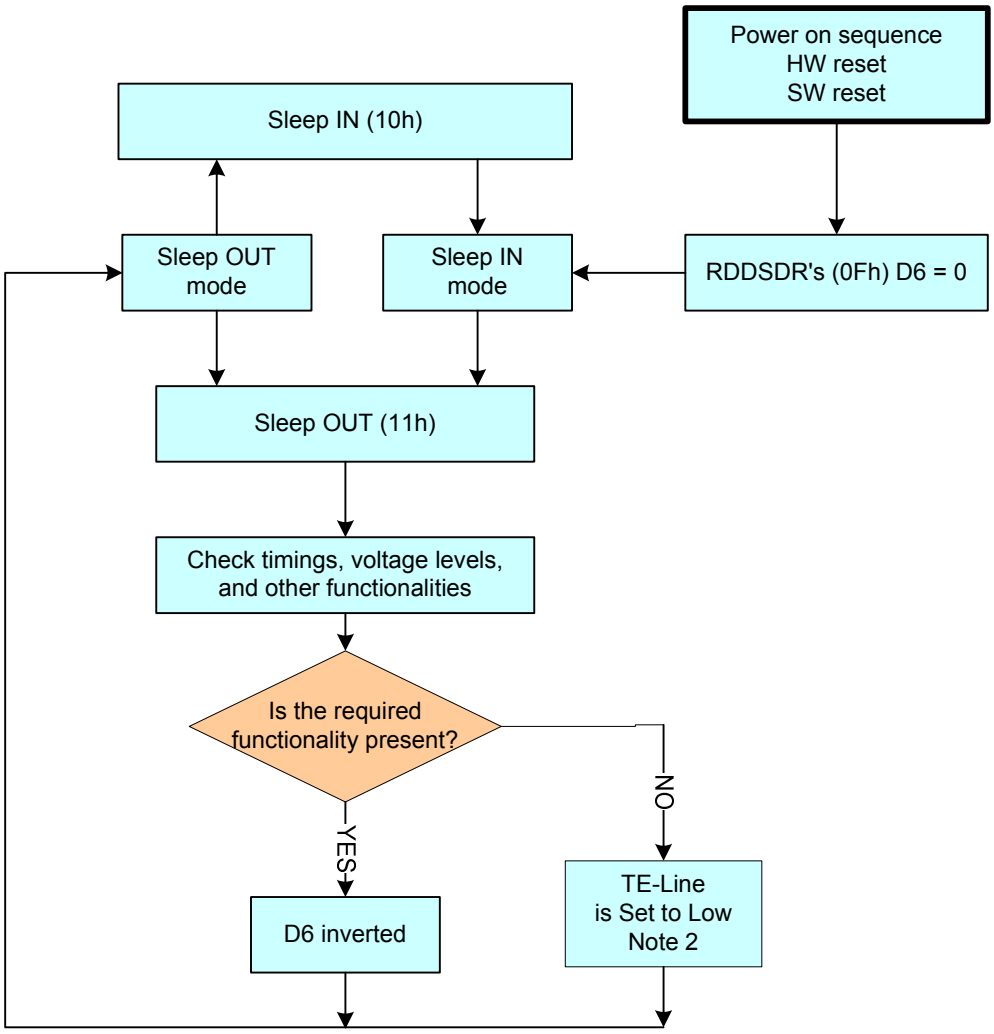
10.2. Functionality Detection

The Sleep Out command (Command "Sleep Out (11h)") is a trigger for an internal function of the ILI9488, which indicates if the ILI9488 is still running and meets functionality requirements. The internal function (the display controller) is compared if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (increased by 1), defined in the command "Read Display Self-Diagnostic Result (0Fh)" (RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (not increased by 1) and the used TE-line is set to low (registers will keep their current values) and can only be reactivated by the Tearing Effect Line On (35h) command.

The flow chart for this internal function is:



Notes:

1. When changing from the Sleep In mode to the Sleep Out mode, 120msec are needed after the Sleep Out command before it is able to check if functionality requirements are met and the value of RDDSDR's D6 is valid. Otherwise, there will be 5msec delay for the D6's value to be valid when the Sleep Out command is sent in the Sleep Out mode.
2. This function is only used when the TE-line is used.

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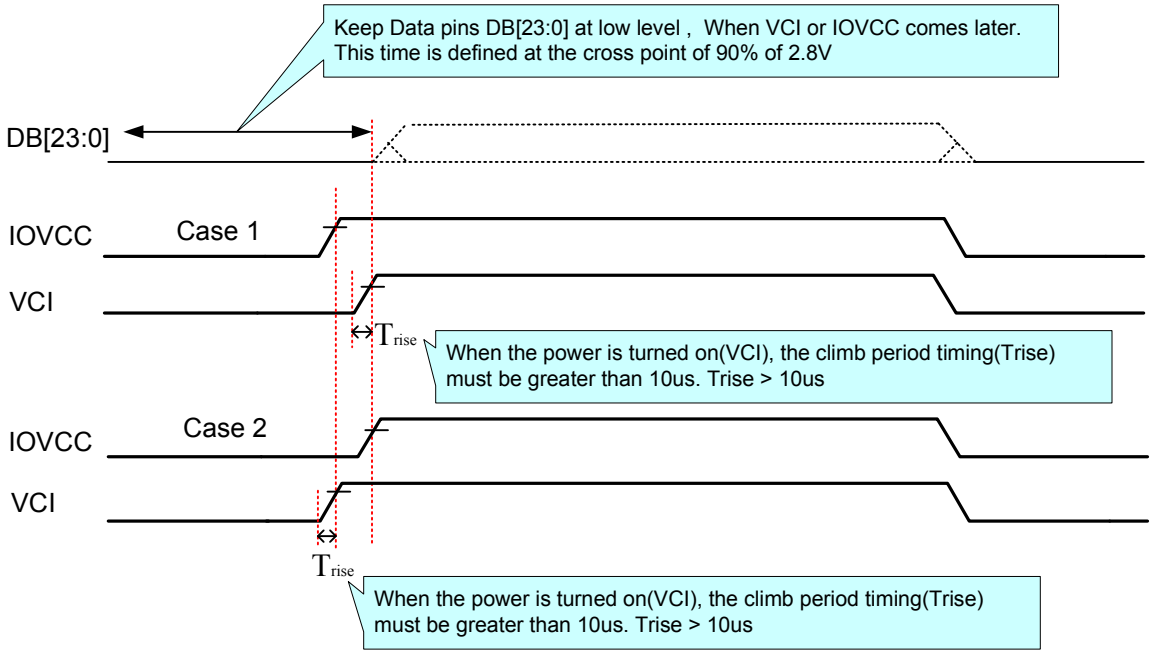
11. Power ON/OFF Sequence

IOVCC and VCI can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with a minimum of 120msec. If the LCD is in the Sleep In mode, VCI and IOVCC can be powered down with a minimum of 0msec after the RESX has been released.
CSX can be applied at any time or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ILI9488 if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. When the power is turned on, the climb period timing(T_{rise}) must be greater than 10us.
6. Keep data pins DB[23:0] at low level, when VCI or IOVCC comes later



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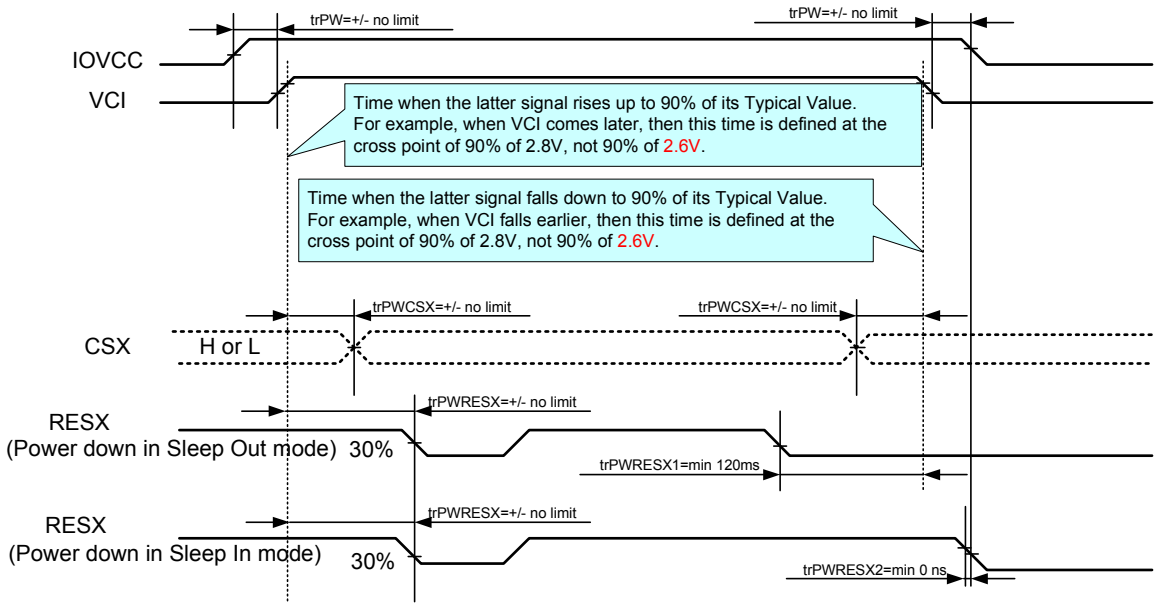
11.1. Case 1 – RESX Line is Held High or Unstable by Host at Power ON

If the RESX line is held High or unstable by the host during Power On, then Hardware Reset must be applied after both VCI and IOVCC have been applied. Otherwise, the correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



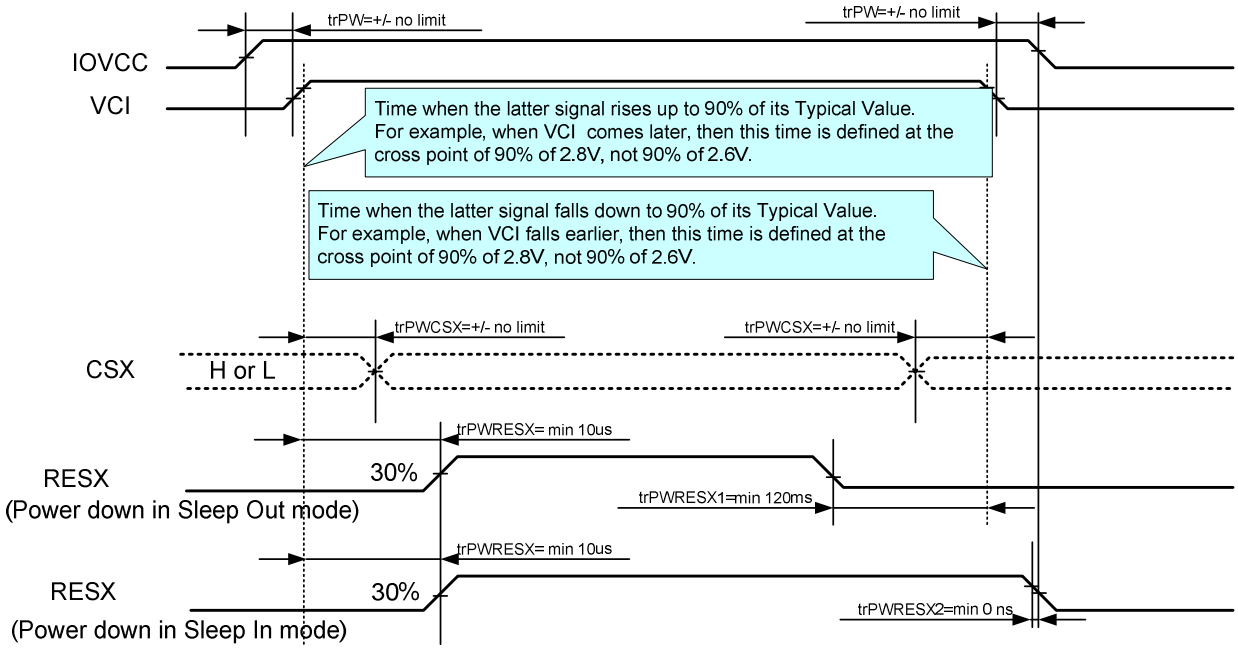
trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

11.2. Case 2 – RESX Line is Held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for a minimum of 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

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Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

11.3. Uncontrolled Power Off

The Uncontrolled Power Off means the situation when a battery is removed without the controlled power off sequence. There will not be any damages on the display module, or the display module will not cause any damages on the host or lines of the interface. At an uncontrolled power off event, the ILI9488 will force the display to become blank and will not cause any abnormal visible effects within 1 second on the display and remains blank until “Power On Sequence” powers it up.

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12. Power Level Definition

12.1. Power Levels

6 level modes are defined in order from Maximum to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
   In this mode, the display is able to show a maximum of 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with a maximum of 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used with 8 colors.
5. Sleep In Mode
   In this mode, the DC/DC converter, internal oscillator, and panel driver circuit are stopped. Only the MCU interface and memory can work with the VCI power supply. Contents of the memory are safe and cannot be changed.
6. Power Off Mode
   In this mode, both VCI and IOVCC are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Only when both Power supplies are removed can Mode 6 be entered.

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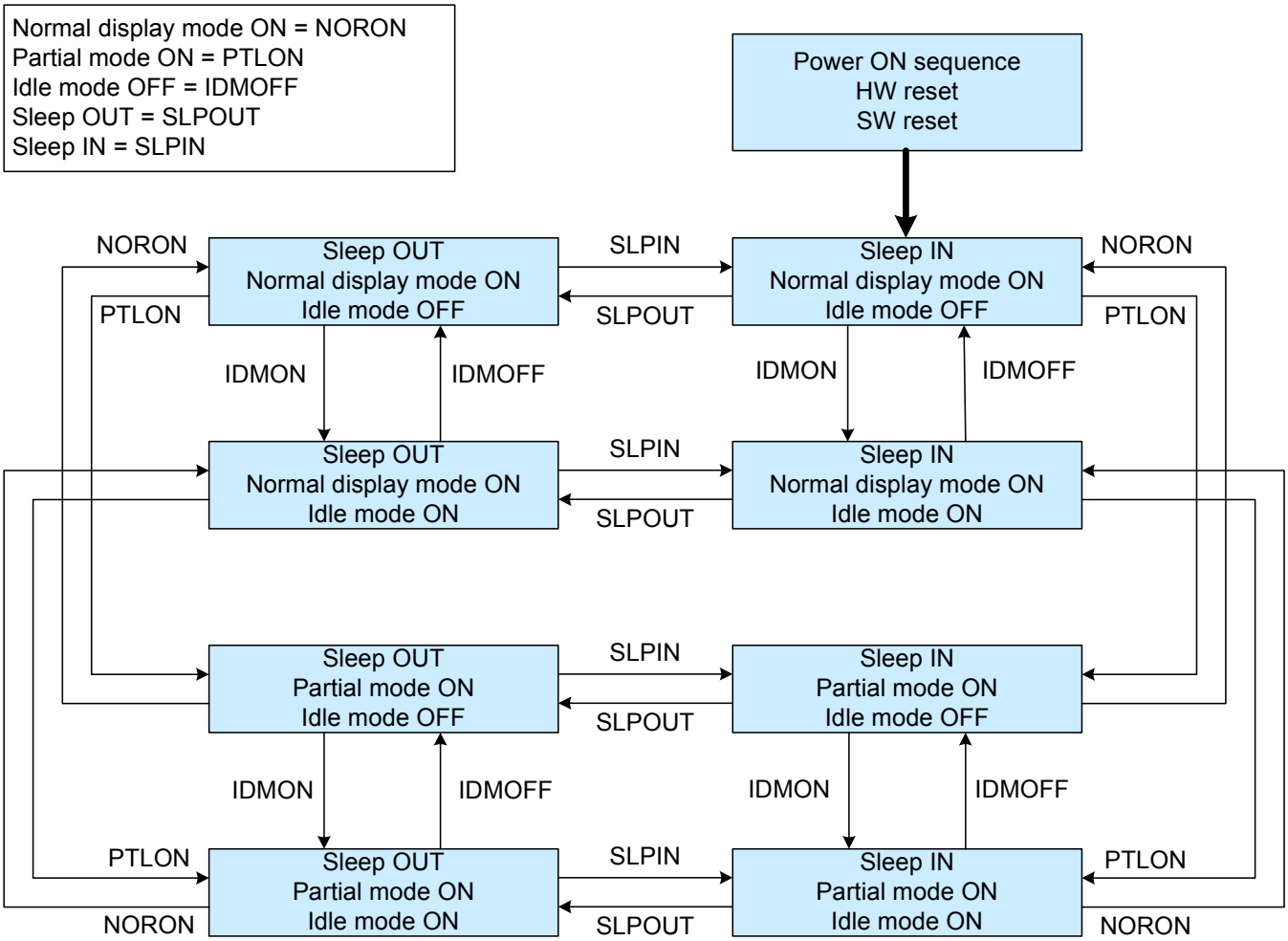
12.2. Power Flow Chart



Notes:

1. There are not any abnormal visual effects when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by users, when one power mode changes to another power mode.

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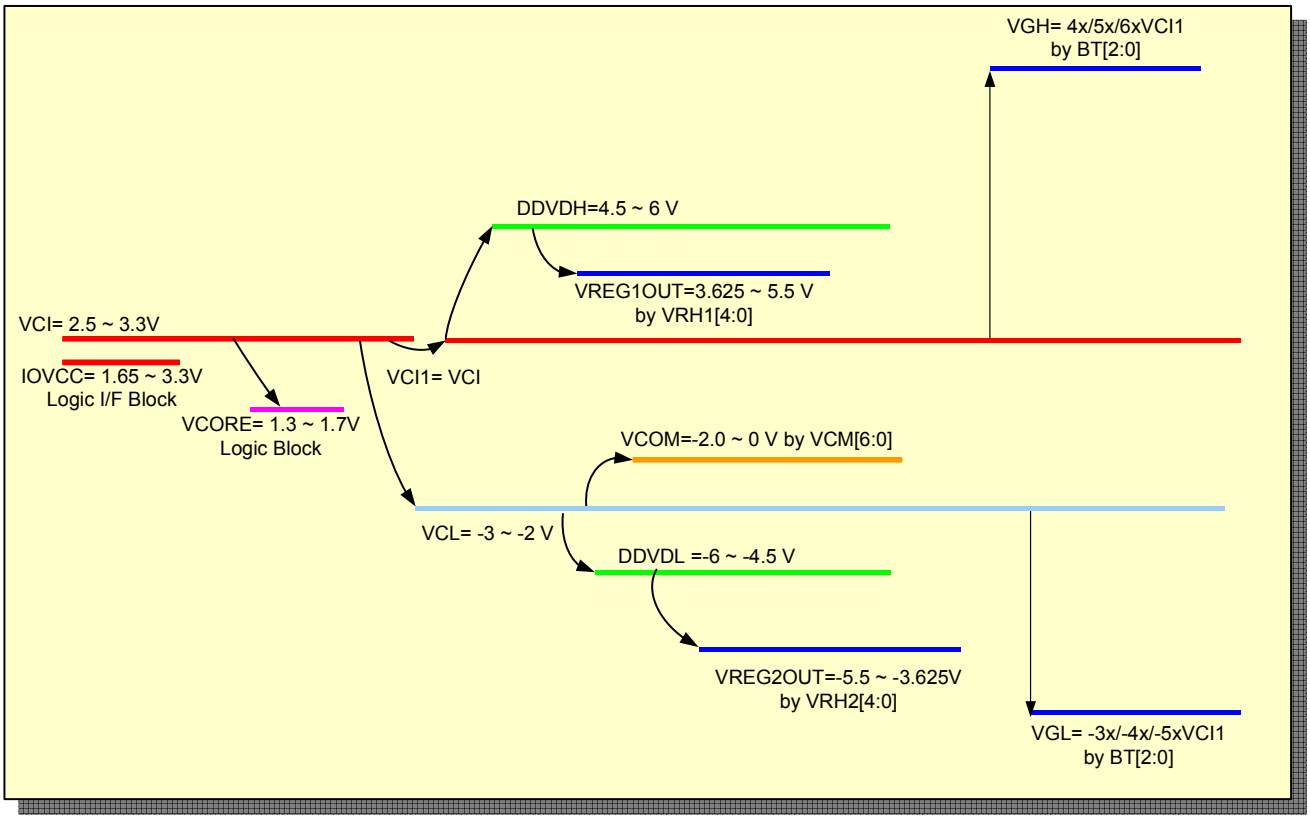
12.3. LCM Voltage Generation



Note: The DDVDH, DDVDL, VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to the current consumption at respective outputs.

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13. Reset

13.1. Registers

The initialized values of registers are listed in Table 37.

Table 37: Initial Values of Registers

Register	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Random	Random
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display Status	Display Off	Display Off	Display Off
Idle Mode	Off	Off	Off
All Pixels Off	Off	Off	Off
All Pixels On	Off	Off	Off
Column Start Address (2Ah)	0000 h	0000 h	0000 h
Column End Address (2Ah)	013F h	013F h	013F h
Page Start Address (2Bh)	0000 h	0000 h	0000 h
Page End Address (2Bh)	01DF h	01DF h	01DF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start (30h)	0000 h	0000 h	0000 h
Partial Area End (30h)	01DF h	01DF h	01DF h
MADCTL (36h)	00 h	00 h	00h
RDNUMED (05h)	00 h	00 h	00h
RDDPM (0Ah)	08 h	08 h	08 h
RDDMADCTL (0Bh)	00 h	00 h	00 h
RDDCOLMOD (0Ch)	06 h	06 h	06 h
RDDIM (0Dh)	00 h	00 h	00 h
RDDSM (0Eh)	00 h	00 h	00 h
RDDSDR (0Fh)	00 h	00 h	00 h
Color Pixel Format (3Ah)	18 Bit/Pixel	18 Bit/Pixel	18 Bit/Pixel
TE Output Line (35h)	Off	Off	Off
TE Line Mode (35h)	Mode 1[Note 2]	Mode 1[Note 2]	Mode 1[Note 2]
RDDISBV (52h)	00 h	00 h	No charge
RDCTRLD (54h)	00 h	00 h	No charge
RDCABC (56h)	00 h	00 h	No charge
RDCABCMB (5Fh)	00 h	00 h	No charge

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.
2. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

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13.2. Output Pins, I/O Pins

Table 38: Output and I/O Pins

Pin/Line	After Power ON	After Hardware Reset	After Software Reset
DB [23:0]	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
SDA (Output direction), SDO	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
MIPI_DATA_P	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
MIPI_DATA_N	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
CABC_PWM	Low	Low	Low
TE	Low	Low	Low

Note: There will be no output from DB [23:0], SDA, SDO, CABC_PWM, TE, MIPI_DATA_P, and MIPI_DATA_N, during the Power ON/OFF sequence, hardware reset, and software reset.

13.3. Input Pins

Pin/Line	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	*See Chapter 11*	Input valid	Input valid	Input valid	*See Chapter 11*
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX/SCL	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input valid	Input invalid
ENABLE	Input invalid	Input valid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB [23:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
MIPI_CLOCK_P	Input invalid	Input valid	Input valid	Input valid	Input invalid
MIPI_CLOCK_N	Input invalid	Input valid	Input valid	Input valid	Input invalid
MIPI_DATA_P	Input invalid	Input valid	Input valid	Input valid	Input invalid
MIPI_DATA_N	Input invalid	Input valid	Input valid	Input valid	Input invalid

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13.4. Reset Timing

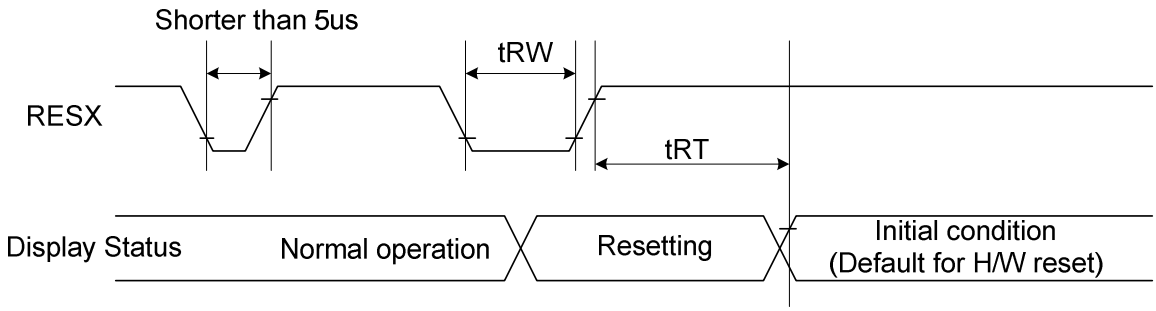

Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

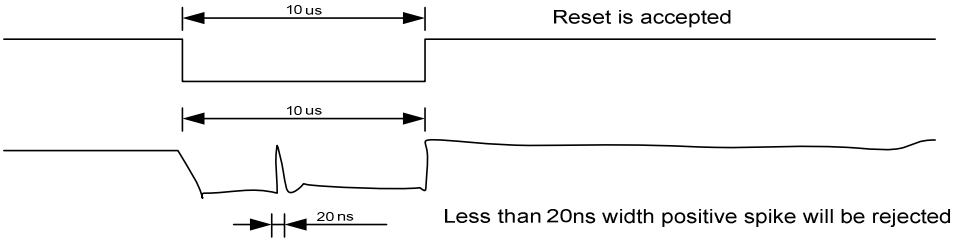

Figure 137: Positive Noise Pulse during Reset Low

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5. When Reset is applied during the Sleep In Mode.
6. When Reset is applied during the Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. The Sleep Out command also cannot be sent in 120msec.

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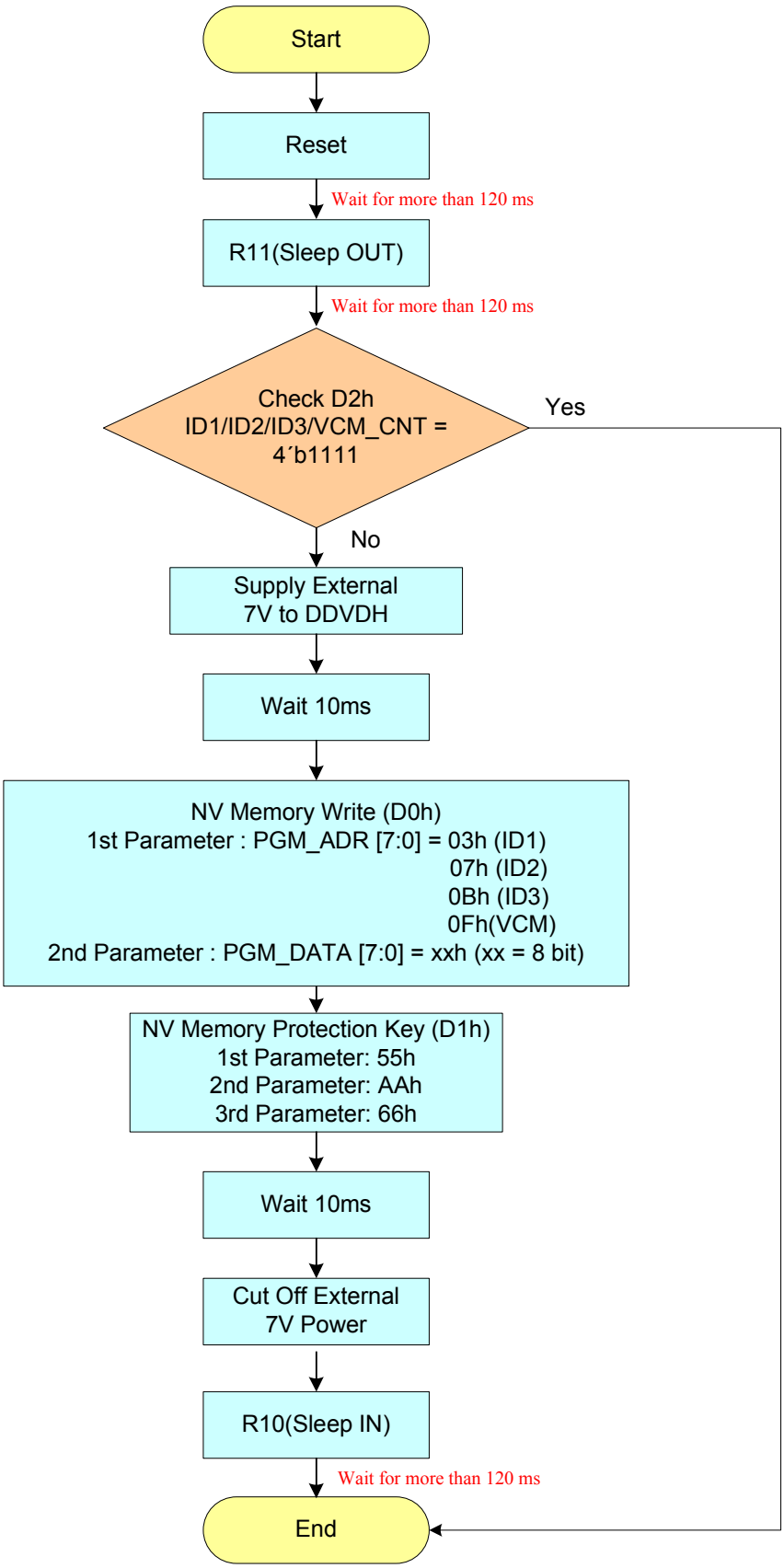
14. NV Memory Programming Flow

14.1. ID1/ID2/ID3 and VCOM Programming Flow



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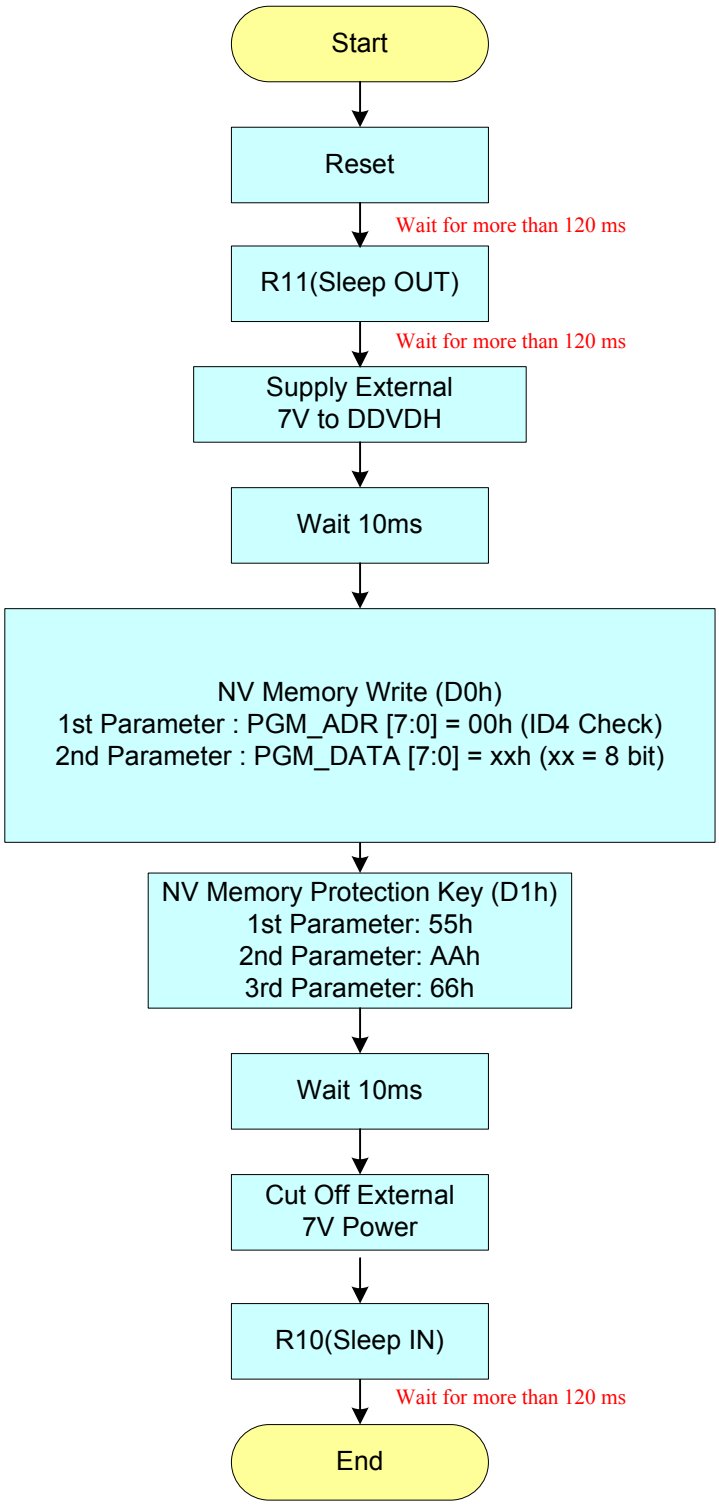
14.2. ID4 Programming Flow



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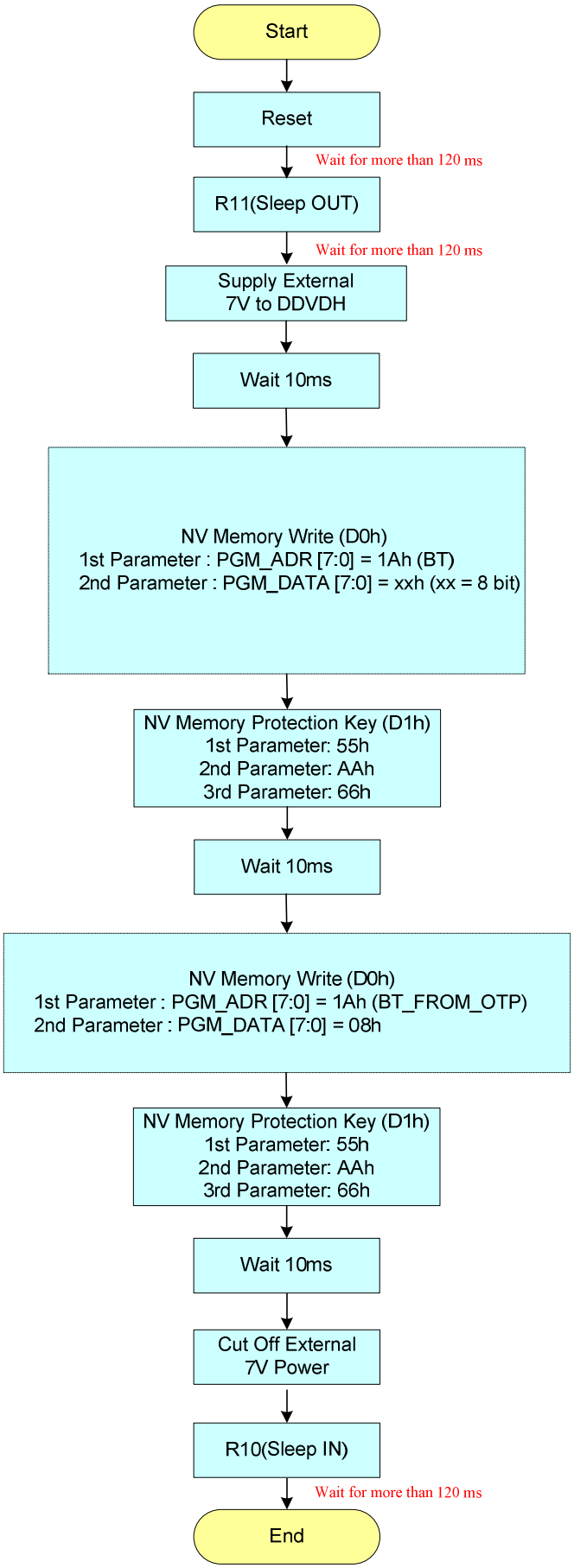
14.3. BT Programming Flow



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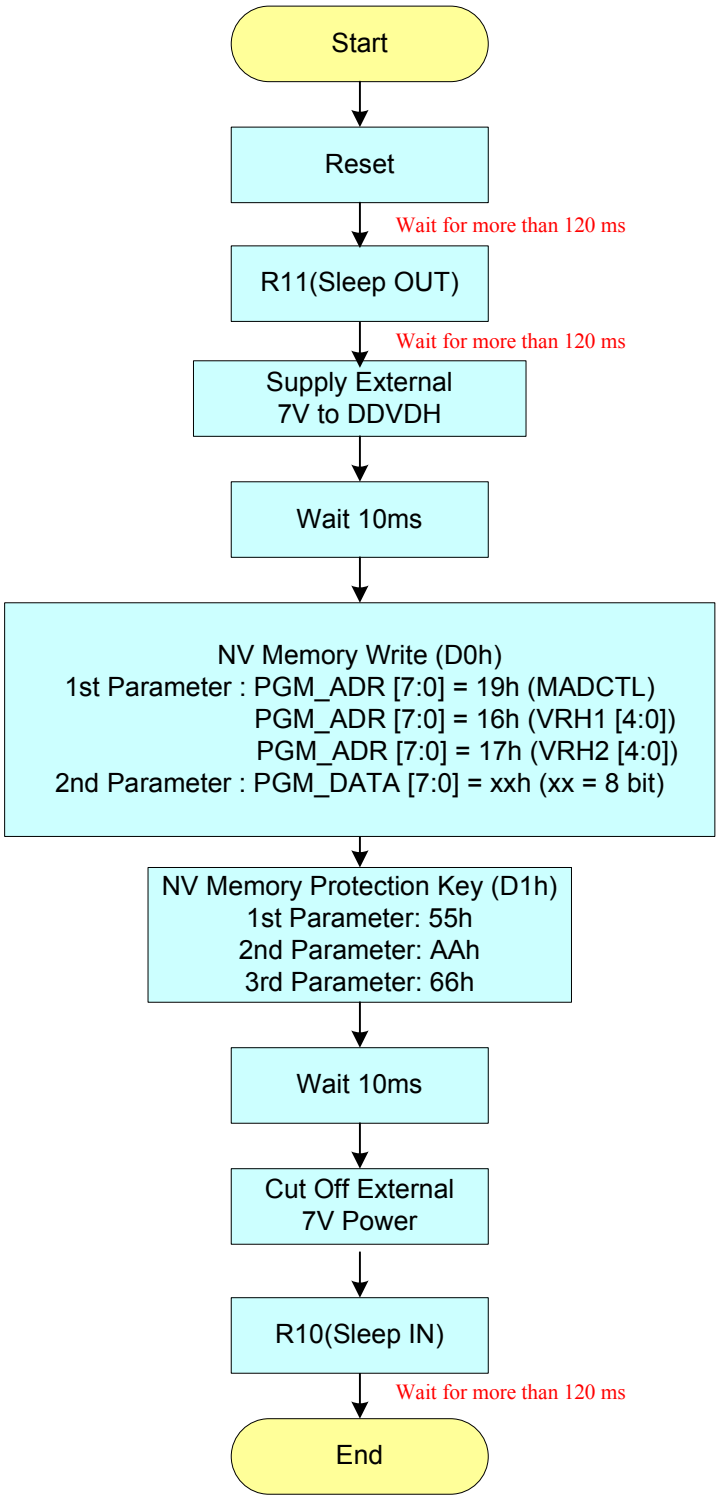
14.4. VRH1, VRH2 and MADCTL Programming Flow



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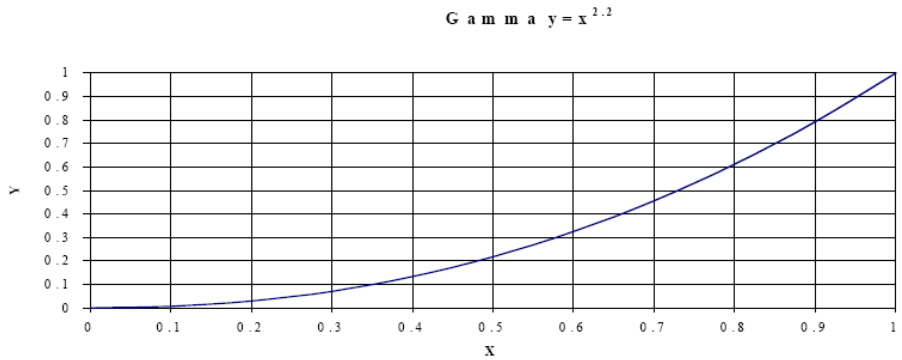
15. GAMMA Correction

The ILI9488 provides one gamma curve (Gamma2.2).

15.1. Gamma Curve

15.1.1. Gamma Curve (GC0), applies the function $y = x^{2.2}$



15.2. Gamma Default Values

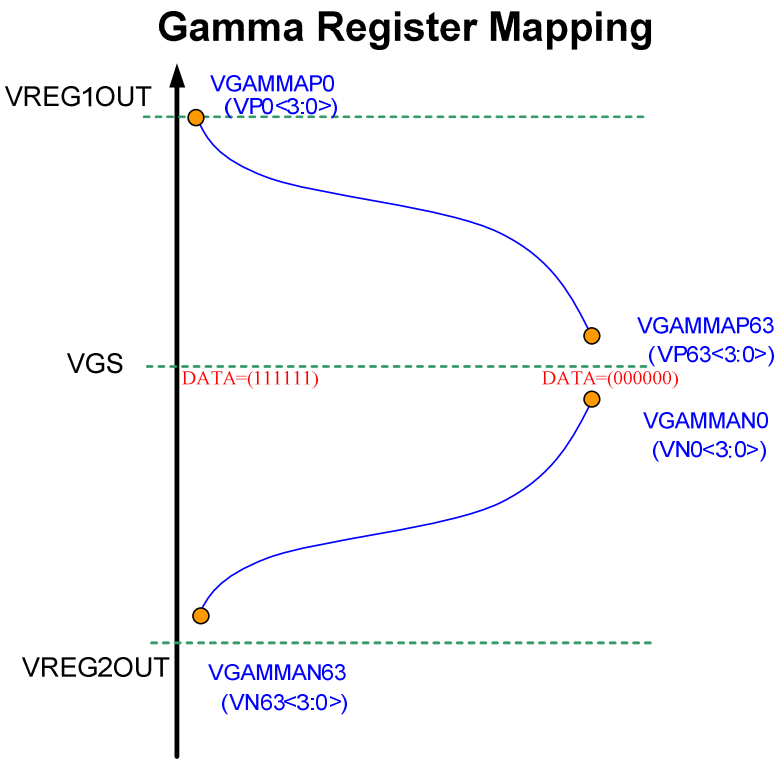


Figure 138:Gamma Register Mapping

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15.2.1. Positive Gamma Control (E0h)

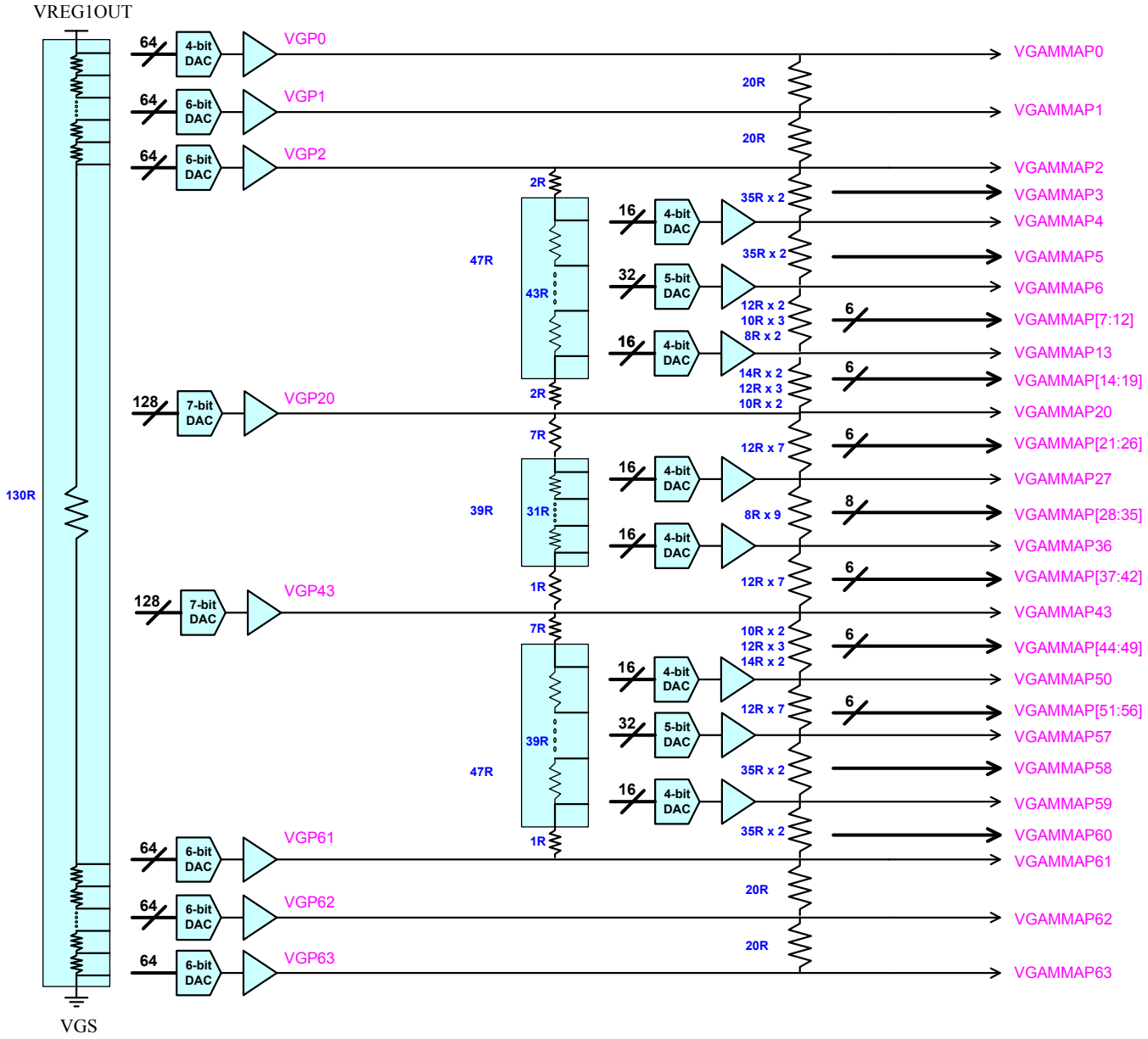

Figure 139: Positive Gamma Control (E0h)

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15.2.2. Negative Gamma Control (E1h)

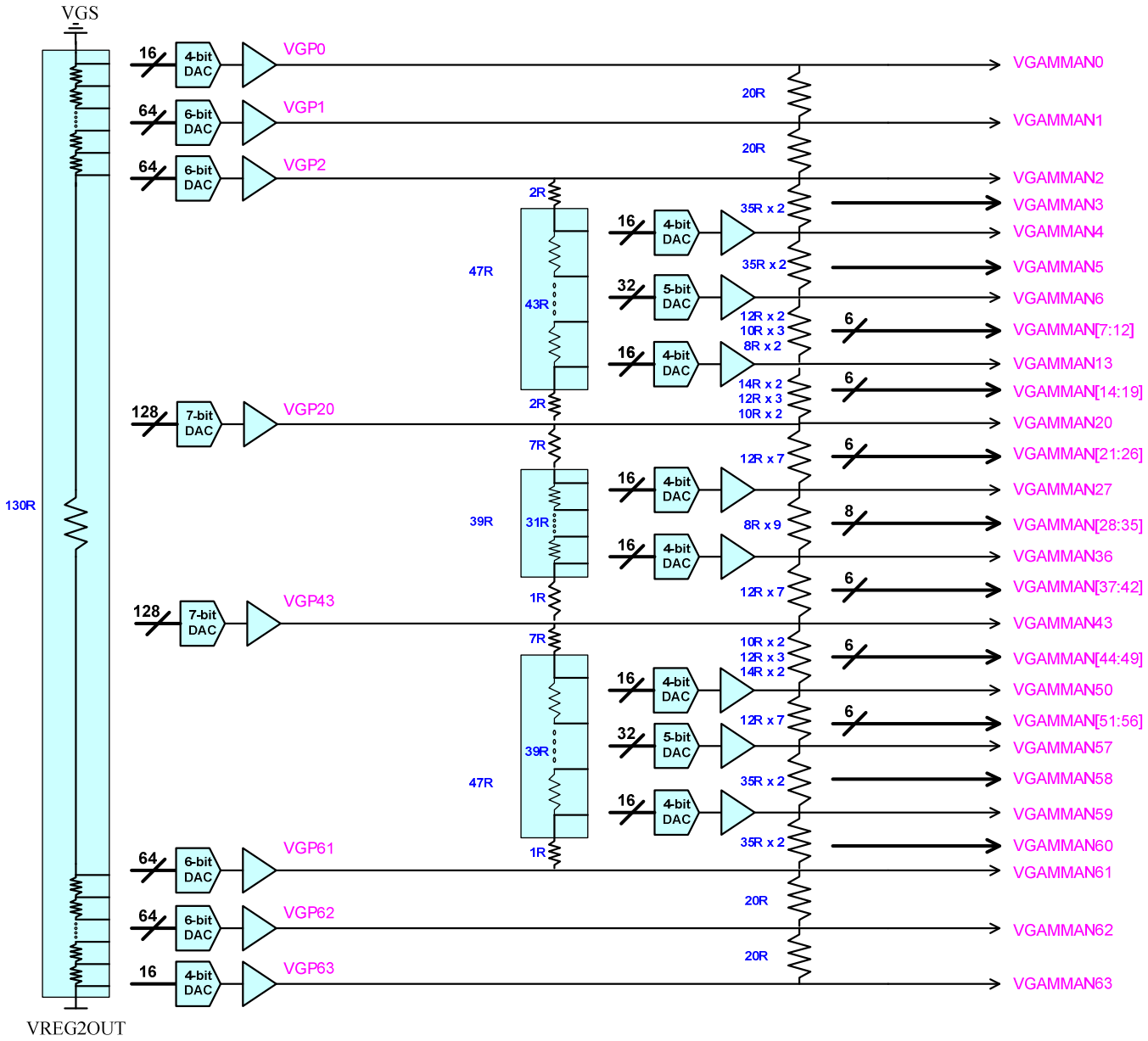

Figure 140: Negative Gamma Control (E1h)

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Positive polarity	Resister stream	Gamma 64 grayscale voltage calculation formula
VGAMMAP0		VGSP+ΔVDHP(130R-1R*VP0 [3:0])/130R
VGAMMAP1		VGSP+ΔVDHP(130R-1R*VP0 [5:0])/130R
VGAMMAP2	3.5R	VGSP+ΔVDHP(130R-1R*VP0 [5:0])/130R
VGAMMAP3	3.5R	VGAMMAP4+(VGAMMAP2-VGAMMAP4)*(3.5R)/(7R)
VGAMMAP4	3.5R	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((40R-1R*VP4 [3:0])/47R)
VGAMMAP5	3.5R	VGAMMAP6+(VGAMMAP4-VGAMMAP6)*(3.5R)/(7R)
VGAMMAP6	1.2R	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((45R-1R*VP6 [4:0])/47R)
VGAMMAP7	1.2R	VGAMMAP13+(VGAMMAP6-VGAMMAP13)*(5.8R)/(7R)
VGAMMAP8	1R	VGAMMAP13+(VGAMMAP6-VGAMMAP13)*(4.6R)/(7R)
VGAMMAP9	1R	VGAMMAP13+(VGAMMAP6-VGAMMAP13)*(3.6R)/(7R)
VGAMMAP10	1R	VGAMMAP13+(VGAMMAP6-VGAMMAP13)*(2.6R)/(7R)
VGAMMAP11	0.8R	VGAMMAP13+(VGAMMAP6-VGAMMAP13)*(1.6R)/(7R)
VGAMMAP12	0.8R	VGAMMAP13+(VGAMMAP6-VGAMMAP13)*(0.8R)/(7R)
VGAMMAP13	1.4R	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((17R-1R*VP13 [3:0])/47R)
VGAMMAP14	1.4R	VGAMMAP20+(VGAMMAP13-VGAMMAP20)*(7R)/(8.4R)
VGAMMAP15	1.2R	VGAMMAP20+(VGAMMAP13-VGAMMAP20)*(5.6R)/(8.4R)
VGAMMAP16	1.2R	VGAMMAP20+(VGAMMAP13-VGAMMAP20)*(4.4R)/(8.4R)
VGAMMAP17	1.2R	VGAMMAP20+(VGAMMAP13-VGAMMAP20)*(3.2R)/(8.4R)
VGAMMAP18	1R	VGAMMAP20+(VGAMMAP13-VGAMMAP20)*(2R)/(8.4R)
VGAMMAP19	1R	VGAMMAP20+(VGAMMAP13-VGAMMAP20)*(1R)/(8.4R)
VGMMAP20	1.2R	VGSP+ΔVDHP(130R-1R*VP20 [6:0])/130R : VP20 [6:0] = 0~63 VGSP+ΔVDHP(129R-1R*VP20 [6:0])/130R : VP20 [6:0] = 64~127
VGAMMAP21	1.2R	VGAMMAP27+(VGAMMAP20-VGAMMAP27)*(7.2R)/(8.4R)
VGAMMAP22	1.2R	VGAMMAP27+(VGAMMAP20-VGAMMAP27)*(6R)/(8.4R)
VGAMMAP23	1.2R	VGAMMAP27+(VGAMMAP20-VGAMMAP27)*(4.8R)/(8.4R)
VGAMMAP24	1.2R	VGAMMAP27+(VGAMMAP20-VGAMMAP27)*(3.6R)/(8.4R)
VGAMMAP25	1.2R	VGAMMAP27+(VGAMMAP20-VGAMMAP27)*(2.4R)/(8.4R)
VGAMMAP26	1.2R	VGAMMAP27+(VGAMMAP20-VGAMMAP27)*(1.2R)/(8.4R)
VGAMMAP27	1.2R	VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((32R-1R*VP27 [3:0])/39R)
VGAMMAP28	1.2R	VGAMMAP36+(VGAMMAP27-VGAMMAP36)*(9.6R)/(10.8R)
VGAMMAP29	1.2R	VGAMMAP36+(VGAMMAP27-VGAMMAP36)*(8.4R)/(10.8R)
VGAMMAP30	1.2R	VGAMMAP36+(VGAMMAP27-VGAMMAP36)*(7.2R)/(10.8R)
VGAMMAP31	1.2R	VGAMMAP36+(VGAMMAP27-VGAMMAP36)*(6R)/(10.8R)
VGAMMAP32	1.2R	VGAMMAP36+(VGAMMAP27-VGAMMAP36)*(4.8R)/(10.8R)
VGAMMAP33	1.2R	VGAMMAP36+(VGAMMAP27-VGAMMAP36)*(3.6R)/(10.8R)
VGAMMAP34	1.2R	VGAMMAP36+(VGAMMAP27-VGAMMAP36)*(2.4R)/(10.8R)

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VGAMMAP35	1.2R	VGAMMAP36+(VGAMMAP27-VGAMMAP36)*(1.2R)/(10.8R)
VGAMMAP36	1.2R	VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((16R-1R*VP36 [3:0])/39R)
VGAMMAP37	1.2R	VGAMMAP43+(VGAMMAP36-VGAMMAP43)*(7.2R)/(8.4R)
VGAMMAP38	1.2R	VGAMMAP43+(VGAMMAP36-VGAMMAP43)*(6R)/(8.4R)
VGAMMAP39	1.2R	VGAMMAP43+(VGAMMAP36-VGAMMAP43)*(4.8R)/(8.4R)
VGAMMAP40	1.2R	VGAMMAP43+(VGAMMAP36-VGAMMAP43)*(3.6R)/(8.4R)
VGAMMAP41	1.2R	VGAMMAP43+(VGAMMAP36-VGAMMAP43)*(2.4R)/(8.4R)
VGAMMAP42	1.2R	VGAMMAP43+(VGAMMAP36-VGAMMAP43)*(1.2R)/(8.4R)
VGAMMAP43	1R	VGSP+ΔVDHP(130R-1R*VP43 [6:0])/130R : VP43 [6:0] = 0~63 VGSP+ΔVDHP(129R-1R*VP43 [6:0])/130R : VP43 [6:0] = 64~127
VGAMMAP44	1R	VGAMMAP50+(VGAMMAP43-VGAMMAP50)*(7.4R)/(8.4R)
VGAMMAP45	1.2R	VGAMMAP50+(VGAMMAP43-VGAMMAP50)*(6.4R)/(8.4R)
VGAMMAP46	1.2R	VGAMMAP50+(VGAMMAP43-VGAMMAP50)*(5.2R)/(8.4R)
VGAMMAP47	1.2R	VGAMMAP50+(VGAMMAP43-VGAMMAP50)*(4R)/(8.4R)
VGAMMAP48	1.4R	VGAMMAP50+(VGAMMAP43-VGAMMAP50)*(2.8R)/(8.4R)
VGAMMAP49	1.4R	VGAMMAP50+(VGAMMAP43-VGAMMAP50)*(1.4R)/(8.4R)
VGAMMAP50	0.8R	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((40R-1R*VP50 [3:0])/47R)
VGAMMAP51	0.8R	VGAMMAP57+(VGAMMAP50-VGAMMAP57)*(6.2R)/(7R)
VGAMMAP52	1R	VGAMMAP57+(VGAMMAP50-VGAMMAP57)*(5.4R)/(7R)
VGAMMAP53	1R	VGAMMAP57+(VGAMMAP50-VGAMMAP57)*(4.4R)/(7R)
VGAMMAP54	1R	VGAMMAP57+(VGAMMAP50-VGAMMAP57)*(3.4R)/(7R)
VGAMMAP55	1.2R	VGAMMAP57+(VGAMMAP50-VGAMMAP57)*(2.4R)/(7R)
VGAMMAP56	1.2R	VGAMMAP57+(VGAMMAP50-VGAMMAP57)*(1.2R)/(7R)
VGAMMAP57	3.5R	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((31R-1R*VP57 [3:0])/47R)
VGAMMAP58	3.5R	VGAMMAP59+(VGAMMP57-VGAMMAP59)*(3.5R)/(7R)
VGAMMAP59	3.5R	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((21R-1R*VP59 [3:0])/47R)
VGAMMAP60	3.5R	VGAMMAP61+(VGAMMAP59-VGAMMAP61)*(3.5R)/(7R)
VGAMMAP61		VGSP+ΔVDHP(65R-1R*VP61 [5:0])/130R
VGAMMAP62		VGSP+ΔVDHP(65R-1R*VP62 [5:0])/130R
VGAMMAP63		VGSP+ΔVDHP(23R-1R*VP63 [3:0])/130R

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Negative polarity	Resister stream	Gamma 64 grayscale voltage calculation formula
VGAMMAN63		VREG2OUT+ΔVDHN(23R-1R*VN63 [3:0])/130R
VGAMMAN62		VREG2OUT+ΔVDHN(65R-1R*VN62 [5:0])/130R
VGAMMAN61		VREG2OUT+ΔVDHN(65R-1R*VN61 [5:0])/130R
VGAMMAN60	3.5R	VGAMMAN61+(VGAMMAN59-VGAMMAN61)*(3.5R)/(7R)
VGAMMAN59	3.5R	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((21R-1R*VN59 [3:0])/47R)
VGAMMAN58	3.5R	VGAMMAN59+(VGAMMAN57-VGAMMAN59)*(3.5R)/(7R)
VGAMMAN57	3.5R	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((31R-1R*VN57 [3:0])/47R)
VGAMMAN56	1.2R	VGAMMAN57+(VGAMMAN50-VGAMMAN57)*(1.2R)/(7R)
VGAMMAN55	1.2R	VGAMMAN57+(VGAMMAN50-VGAMMAN57)*(2.4R)/(7R)
VGAMMAN54	1R	VGAMMAN57+(VGAMMAN50-VGAMMAN57)*(3.4R)/(7R)
VGAMMAN53	1R	VGAMMAN57+(VGAMMAN50-VGAMMAN57)*(4.4R)/(7R)
VGAMMAN52	1R	VGAMMAN57+(VGAMMAN50-VGAMMAN57)*(5.4R)/(7R)
VGAMMAN51	0.8R	VGAMMAN57+(VGAMMAN50-VGAMMAN57)*(6.2R)/(7R)
VGAMMAN50	0.8R	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((40R-1R*VN50 [3:0])/47R)
VGAMMAN49	1.4R	VGAMMAN50+(VGAMMAN43-VGAMMAN50)*(1.4R)/(8.4R)
VGAMMAN48	1.4R	VGAMMAN50+(VGAMMAN43-VGAMMAN50)*(2.8R)/(8.4R)
VGAMMAN47	1.2R	VGAMMAN50+(VGAMMAN43-VGAMMAN50)*(4R)/(8.4R)
VGAMMAN46	1.2R	VGAMMAN50+(VGAMMAN43-VGAMMAN50)*(5.2R)/(8.4R)
VGAMMAN45	1.2R	VGAMMAN50+(VGAMMAN43-VGAMMAN50)*(6.4R)/(8.4R)
VGAMMAN44	1R	VGAMMAN50+(VGAMMAN43-VGAMMAN50)*(7.4R)/(8.4R)
VGAMMAN43	1R	VREG2OUT+ΔVDHN(130R-1R*VN43 [5:0])/130R : VN43 [5:0] = 0~63 VREG2OUT+ΔVDHN(129R-1R*VN43 [5:0])/130R : VN43 [5:0] = 64~127
VGAMMAN42	1.2R	VGAMMAN43+(VGAMMAN36-VGAMMAN43)*(1.2R)/(8.4R)
VGAMMAN41	1.2R	VGAMMAN43+(VGAMMAN36-VGAMMAN43)*(2.4R)/(8.4R)
VGAMMAN40	1.2R	VGAMMAN43+(VGAMMAN36-VGAMMAN43)*(3.6R)/(8.4R)
VGAMMAN39	1.2R	VGAMMAN43+(VGAMMAN36-VGAMMAN43)*(4.8R)/(8.4R)
VGAMMAN38	1.2R	VGAMMAN43+(VGAMMAN36-VGAMMAN43)*(6R)/(8.4R)
VGAMMAN37	1.2R	VGAMMAN43+(VGAMMAN36-VGAMMAN43)*(7.2R)/(8.4R)
VGAMMAN36	1.2R	VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((16R-1R*VN36 [3:0])/39R)
VGAMMAN35	1.2R	VGAMMAN36+(VGAMMAN27-VGAMMAN36)*(1.2R)/(10.8R)
VGAMMAN34	1.2R	VGAMMAN36+(VGAMMAN27-VGAMMAN36)*(2.4R)/(10.8R)
VGAMMAN33	1.2R	VGAMMAN36+(VGAMMAN27-VGAMMAN36)*(3.6R)/(10.8R)
VGAMMAN32	1.2R	VGAMMAN36+(VGAMMAN27-VGAMMAN36)*(4.8R)/(10.8R)
VGAMMAN31	1.2R	VGAMMAN36+(VGAMMAN27-VGAMMAN36)*(6R)/(10.8R)
VGAMMAN30	1.2R	VGAMMAN36+(VGAMMAN27-VGAMMAN36)*(7.2R)/(10.8R)
VGAMMAN29	1.2R	VGAMMAN36+(VGAMMAN27-VGAMMAN36)*(8.4R)/(10.8R)
VGAMMAN28	1.2R	VGAMMAN36+(VGAMMAN27-VGAMMAN36)*(9.6R)/(10.8R)

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VGAMMAN27	1.2R	VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((32R-1R*VN27 [3:0])/39R)
VGAMMAN26	1.2R	VGAMMAN27+(VGAMMAN20-VGAMMAN27)*(1.2R)/(8.4R)
VGAMMAN25	1.2R	VGAMMAN27+(VGAMMAN20-VGAMMAN27)*(2.4R)/(8.4R)
VGAMMAN24	1.2R	VGAMMAN27+(VGAMMAN20-VGAMMAN27)*(3.6R)/(8.4R)
VGAMMAN23	1.2R	VGAMMAN27+(VGAMMAN20-VGAMMAN27)*(4.8R)/(8.4R)
VGAMMAN22	1.2R	VGAMMAN27+(VGAMMAN20-VGAMMAN27)*(6R)/(8.4R)
VGAMMAN21	1.2R	VGAMMAN27+(VGAMMAN20-VGAMMAN27)*(7.2R)/(8.4R)
VGAMMAN20	1.2R	VREG2OUT+△VDHN(130R-1R*VN20 [5:0])/130R : VN20 [5:0] = 0~63 VREG2OUT+△VDHN(129R-1R*VN20 [5:0])/130R : VN20 [5:0] = 64~127
VGAMMAN19	1R	VGAMMAN20+(VGAMMAN13-VGAMMAN20)*(1R)/(8.4R)
VGAMMAN18	1R	VGAMMAN20+(VGAMMAN13-VGAMMAN20)*(2R)/(8.4R)
VGAMMAN17	1.2R	VGAMMAN20+(VGAMMAN13-VGAMMAN20)*(3.2R)/(8.4R)
VGAMMAN16	1.2R	VGAMMAN20+(VGAMMAN13-VGAMMAN20)*(4.4R)/(8.4R)
VGAMMAN15	1.2R	VGAMMAN20+(VGAMMAN13-VGAMMAN20)*(5.6R)/(8.4R)
VGAMMAN14	1.4R	VGAMMAN20+(VGAMMAN13-VGAMMAN20)*(7R)/(8.4R)
VGAMMAN13	1.4R	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((17R-1R*VN13 [3:0])/47R)
VGAMMAN12	0.8R	VGAMMAN13+(VGAMMAN6-VGAMMAN13)*(0.8R)/(7R)
VGAMMAN11	0.8R	VGAMMAN13+(VGAMMAN6-VGAMMAN13)*(1.6R)/(7R)
VGAMMAN10	1R	VGAMMAN13+(VGAMMAN6-VGAMMAN13)*(2.6R)/(7R)
VGAMMAN9	1R	VGAMMAN13+(VGAMMAN6-VGAMMAN13)*(3.6R)/(7R)
VGAMMAN8	1R	VGAMMAN13+(VGAMMAN6-VGAMMAN13)*(4.6R)/(7R)
VGAMMAN7	1.2R	VGAMMAN13+(VGAMMAN6-VGAMMAN13)*(5.8R)/(7R)
VGAMMAN6	1.2R	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((45R-1R*VN6 [4:0])/47R)
VGAMMAN5	3.5R	VGAMMAN6+(VGAMMP4-VGAMMAN6)*(3.5R)/(7R)
VGAMMAN4	3.5R	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((40R-1R*VN4 [3:0])/47R)
VGAMMAN3	3.5R	VGAMMAN4+(VGAMMAN2-VGAMMAN4)*(3.5R)/(7R)
VGAMMAN2	3.5R	VREG2OUT+ΔVDHN(130R-1R*VN2 [5:0])/130R
VGAMMAN1		VREG2OUT+ΔVDHN(130R-1R*VN1 [5:0])/130R
VGAMMAN0		VREG2OUT+ΔVDHN(130R-1R*VN0 [3:0])/130R

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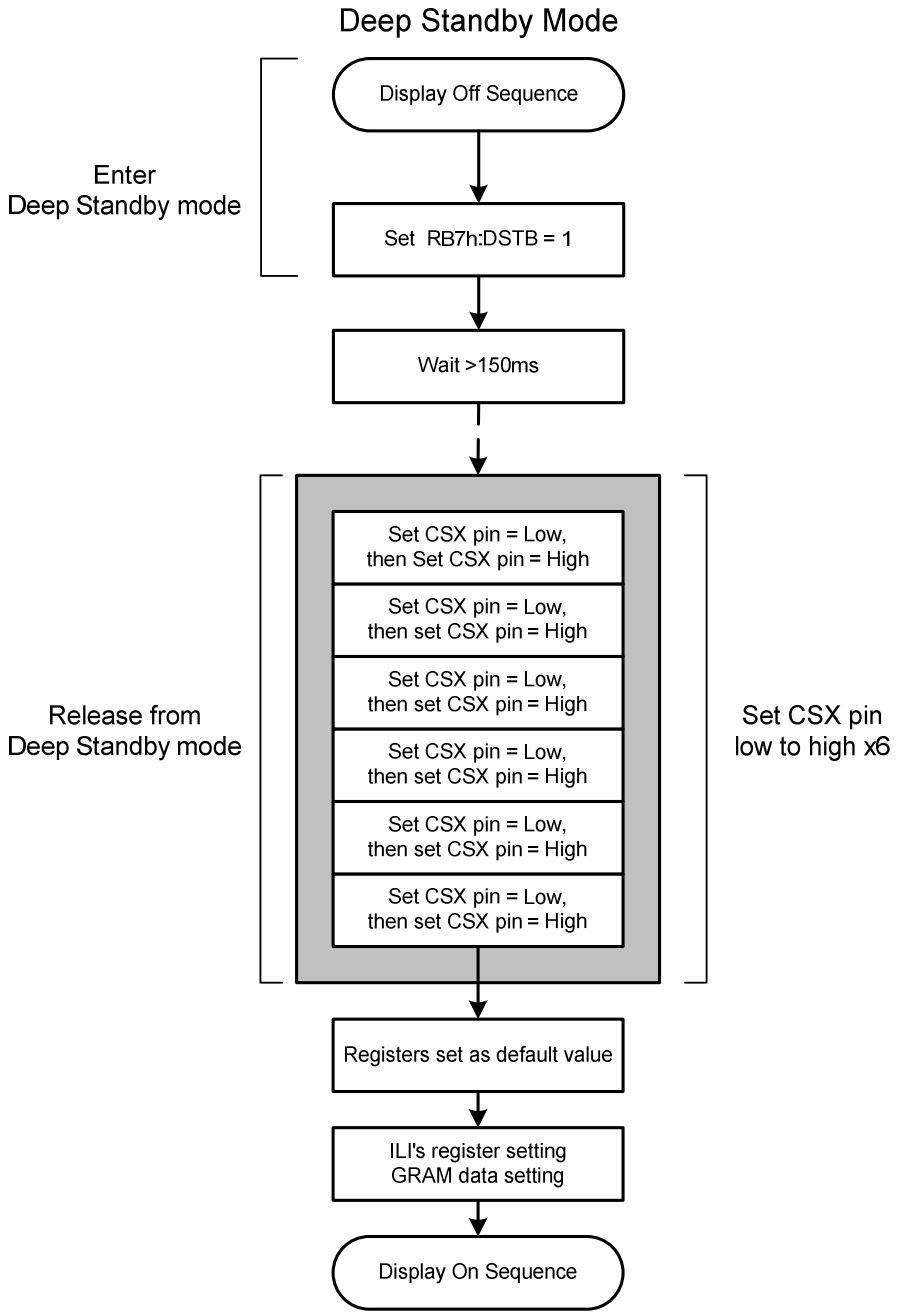
16. Deep Standby Mode Setting



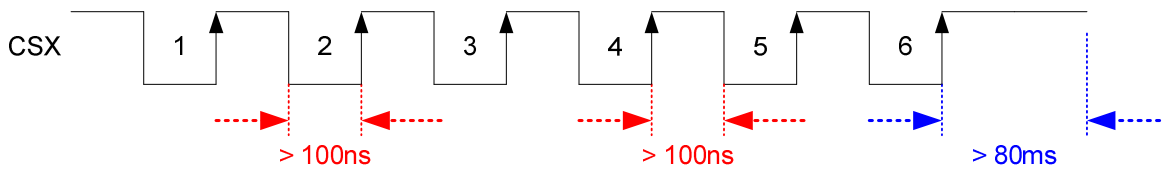


Figure 141: Deep Standby Mode Entry/Exit

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17. Electrical Characteristics

17.1. Absolute Maximum Ratings

The absolute maximum ratings are listed in Table 41. When the ILI9488 is used beyond the absolute maximum ratings, it may be permanently damaged. Using the ILI9488 within the following limits of electrical characteristics is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9488 will malfunction and cause poor reliability.

Table 41: Absolute maximum Ratings

Item	Symbol	Unit	Value
Supply voltage(Analog)	VCI ~ DGND	V	-0.3 ~ +3.3
Supply voltage (I/O)	IOVCC ~ DGND	V	-0.3 ~ +3.3
OTP Supply voltage	DDVDH ~ DGND	V	-0.3 ~ +7.0
Supply voltage	DDVDH ~ DGND	V	-0.3 ~ +6.0
Supply voltage	DDVDL ~ DGND	V	0.3 ~ -6.0
Supply voltage	VGH ~ DGND	V	-0.3 ~ +25
Supply voltage	VGL ~ DGND	V	0.3 ~ -16
Driver supply voltage	VCI - VCL	V	≦ 6.0V
Driver supply voltage	VGH-VGL	V	≦ 32.0V
Input voltage	VIN	V	-0.3 ~ IOVCC + 0.3
HS Input voltage	VHSIN	V	-0.3 ~ + 1.65
Operating temperature	Topr	℃	-30 ~ +70
Storage temperature	Tstg	℃	-55 ~ +110

Note: Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.

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17.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	3.3	V	
Logic operating voltage	IOVCC	-	1.65	1.8	3.3	V	Note 1, 2
OTP Supply voltage	DDVDH	-	-	7	-	V	Note 1
Logic High level input voltage	V_{IH}	-	0.7*IOVCC		IOVCC	V	Note 1
Logic Low level input voltage	V_{IL}	-	-0.3		0.3*IOVCC	V	Note 1
Logic High level output voltage TE, SDO (SDA) , CABC_PWM	V_{OH}	IOH = -1.0mA	0.8*IOVCC		IOVCC	V	Note 1
Logic Low level output voltage TE, SDO (SDA) , CABC_PWM	V_{OL}	IOL = +1.0mA	0		0.2*IOVCC	V	Note 1
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	
Driver Supply Voltage	-	|VGH-VGL|	16	-	32	V	
Input and Output							
Logic High Level Input Voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	
Logic Low Level Input Voltage	VIL	-	DGND	-	0.3*IOVCC	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-2.0	-	-0.06	V	Note 3
Source Driver							
Source Output Range	V_{SOUT}	-	0.1	-	VREG1OUT-0.1	V	Note 4
Positive Gamma Reference Voltage	VREG1OUT	-	3.625	-	5.5	V	
Negative Gamma Reference Voltage	VREG2OUT	-	-5.5	-	-3.625	V	
Source Output Setting Time	Tr	Below with 99% precision	-	10	-	uS	Note 3. 4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	20	mV	Note 3
		4.2V>Sout>0.8V	-	-	15	mV	-
Output Offset Voltage	V_{OFFSET}	-	-	-	35	mV	Note 3
Booster Operation							
Booster (VCIx2) Voltage	DDVDH	-			6	V	
Booster (VCIx2) Voltage	DDVDL	-	-6			V	
Booster (VCIx2 Drop Voltage)	VCI1x2 drop	loading=1mA	-	-	5	%	
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	
Standby mode current consumption (Ta = 25℃, Interface: DBI and DPI)							
Sleep in mode	VCI	VCI=2.8V IOVCC=1.8V	-	100	-	uA	
Deep Standby mode	VCI		-	1	-	uA	

Notes:

1. Ta = -30 to 70 ℃ (no damage up to 85℃ (at maximum)), IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, DGND=0V.
2. Supply the digital IOVCC voltage equal to or less than the analog VCI voltage.
3. Source channel loading = 10KΩ,30pF/channel
4. The maximum value is between 10KΩ,30pF/channel and Gamma setting value.

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17.3. DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

Note: Ta = -30℃ to 70℃ (no damage up to 85℃ (at maximum))

17.3.1. DC Characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	V_{CI}	Operating voltage	2.5	2.8	3.3	V
Digital power supply voltage	V_{IOVCC}	I/O supply voltage	1.65	1.8	3.3	V
Analog power supply voltage noise	V_{VCI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
I/O power supply voltage noise	V_{IOVCC_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Notes:

1. Ta = -30℃ to 70℃ (no damage up to 85℃ (at maximum))
2. These values are not symmetric amplitude, which center points are IOVCC or VCI. See examples, when VVCI_NOISE and VIOVCC_NOISE are maximums, below for reference purpose.

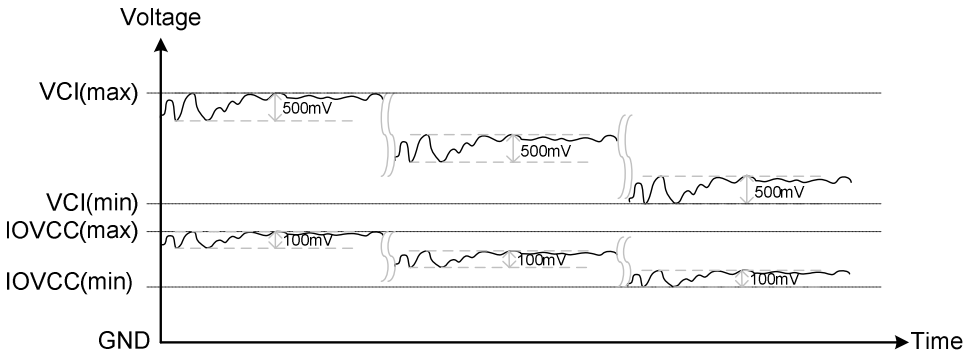

Figure 142: Noise on Power Supply Lines

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17.3.2. DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10, and LP-11 are defined in the table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD, or LP-TX is mentioned in the condition column. Other logical levels in the table are for the MCU interface.

Parameter	Symbol	Condition	Specification			Unit
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA[Note 2]	0.8 V_{IOVCC}	-	V_{IOVCC}	V
Logic Low level output voltage	V_{OL}	I_{OUT}=-1mA[Note 2]	0.0	-	0.2V_{IOVCC}	V
Logic High level input voltage	V_{IHLPCD}	LP-CD[Note 3]	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD[Note 3]	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLOCK, DATA)[Note 3]	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLOCK, DATA)[Note 3]	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLOCK ULP mode)[Note 3]	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (DATA)[Note 3]	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (DATA)[Note 3]	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX[Note 3]	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX[Note 3]	-10	-	-	uA

Notes:

1. Ta = -30℃ to 70℃ (no damage up to 85℃ (at maximum))
2. PWM_OUT, TE signals
3. DSI High Speed mode is Off.

17.3.3. Spike/Glitch Rejection

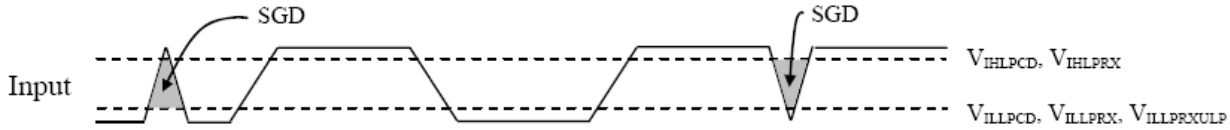

Figure 143: Spike/Glitch Rejection

Note: A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and the Interference Frequency is 450 MHz (at the very least).

Table 42: Spike/Glitch Rejection

Spike/Glitch Rejection – DSI					
Signal	**Symbol**	**Parameter**	**Min**	**Max**	**Unit**
MIPI_DATA_P/N, MIPI_CLOCK_P/N	SGD	Input pulse rejection for DSI	-	300	Vps

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17.3.4. DC Characteristics for DSI HS Mode

DC levels of the HS-0 and HS-0 are defined in the table below:

Table 43: DC Characteristics for DSI HS Mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	MIPI_CLOCK_P/N[Note 2,3]	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	MIPI_DATA_P/N[Note 2,3]	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	MIPI_CLOCK_P/N[Note 4]	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	MIPI_DATA_P/N[Note 4]	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	MIPI_CLOCK_P/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	MIPI_DATA_P/N	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	MIPI_CLOCK_P/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	MIPI_DATA_P/N	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	MIPI_CLOCK_P/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	MIPI_DATA_P/N	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	MIPI_CLOCK_P/N, MIPI_DATA_P/N[Note 3]	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	MIPI_CLOCK_P/N, MIPI_DATA_P/N[Note 3]	-	-	460	mV
Differential Termination Resistor	R_{TERM}	MIPI_CLOCK_P/N, MIPI_DATA_P/N	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	MIPI_CLOCK_P/N, MIPI_DATA_P/N	-	-	450	mV
Termination Capacitor	C_{TERM}	MIPI_CLOCK_P/N, MIPI_DATA_P/N	-	-	14	pF

Notes:

1. Ta = -30 to 70 ℃ (no damage up to 85℃ (at maximum)), IOVCC = 1.65 to 3.3V, GND = 0V
2. Includes 50mV (-50mV to 50mV) ground difference
3. Without VCMRCLKM450/VCMRDATAM450
4. Without 50mV (-50mV to 50mV) ground difference

The DSI receiver (HS mode) realizes that there is logical 1 (HS-1) when a differential voltage is more than VTHH (CLOCK_P/DATA_P). The DSI receiver (HS mode) realizes that there is logical 0 (HS-0) when a differential voltage is more than VTHL (CLOCK_N/DATA_N). There is an undefined state if the differential voltage is less than VTHH (CLOCK_P/DATA_P) and less than VTHL (CLOCK_N/DATA_N). A reference figure is below.

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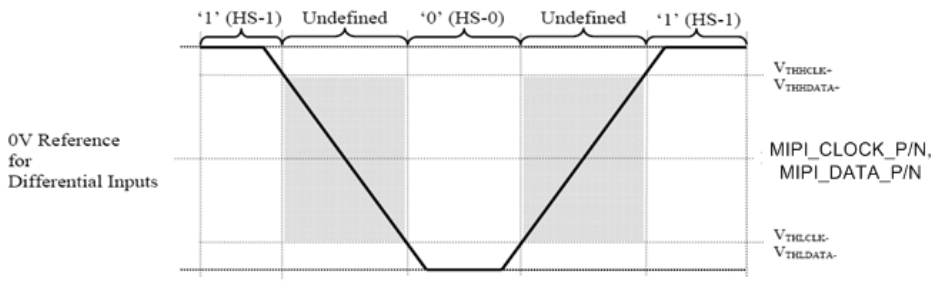

Figure 144: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range

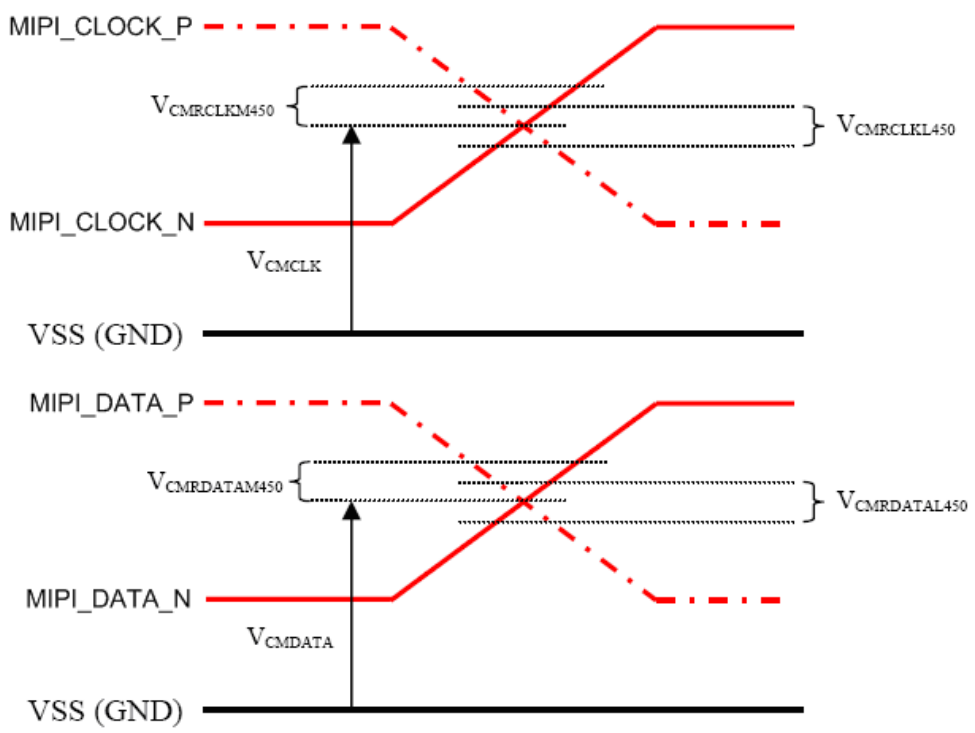

Figure 145: Common Mode Voltage on Clock and Data Channels

The termination resistor (RTERM) of the differential DSI receiver can be driven to two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (MIPI_CLOCK_P <=> MIPI_CLOCK_N or MIPI_DATA_P <=> MIPI_DATA_N)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (MIPI_CLOCK_P <=> MIPI_CLOCK_N or MIPI_DATA_P <=> MIPI_DATA_N)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

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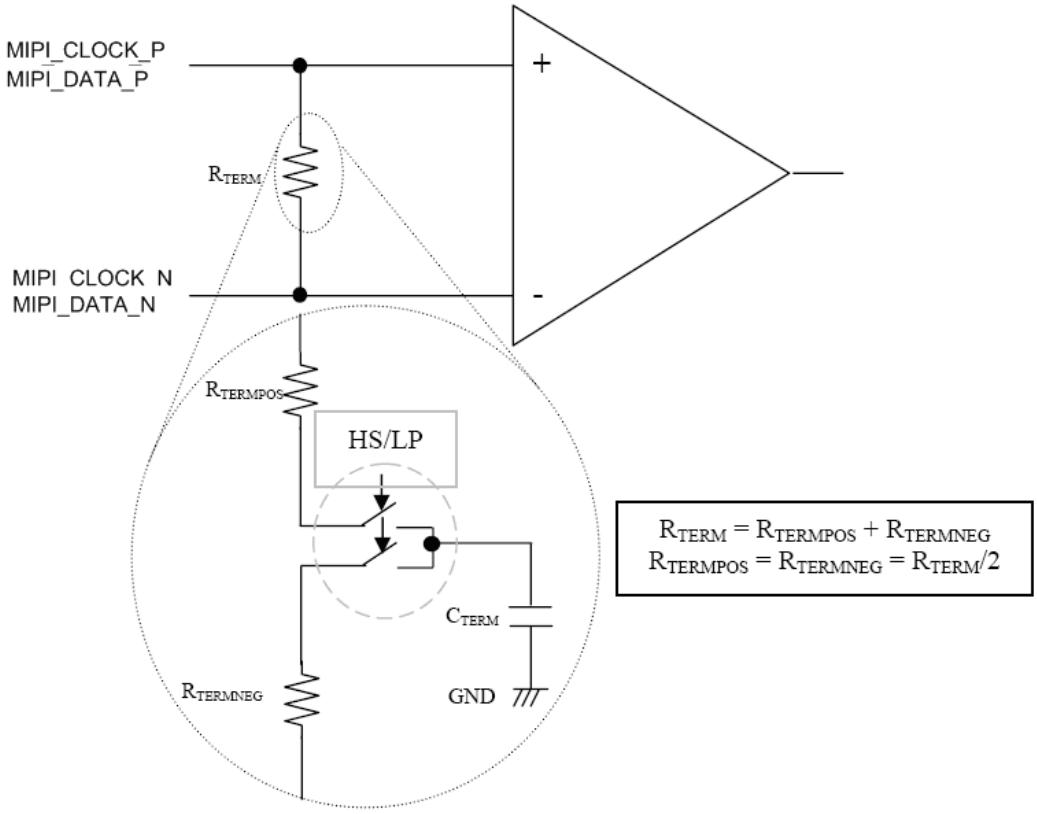

Figure 146: Differential Pair Termination Resister on the Receiver Side

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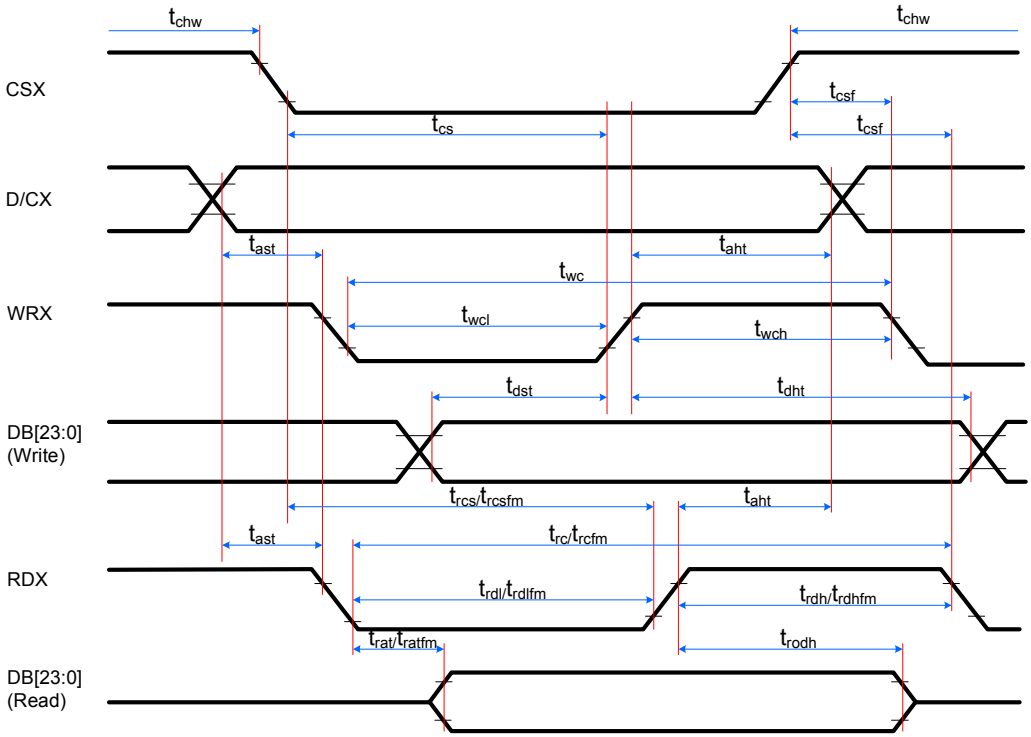
17.4. AC Characteristics

17.4.1. DBI Type B Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	that	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

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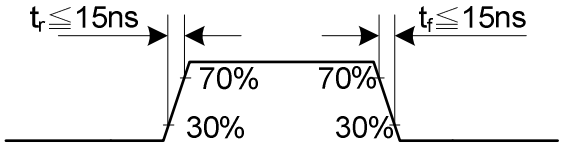
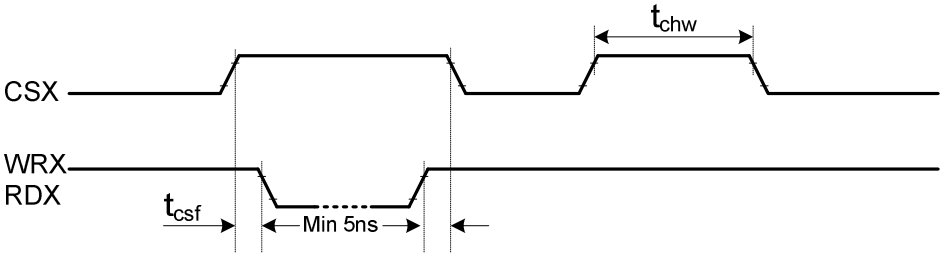
Notes:

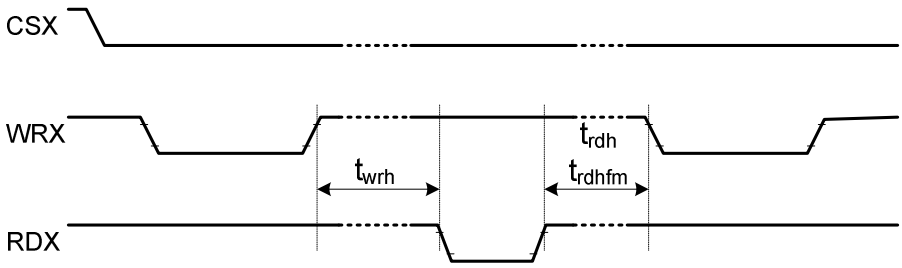
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
3. Input signal rising time and falling time:



4. The CSX timing:



5. The Write to Read or the Read to Write timing:



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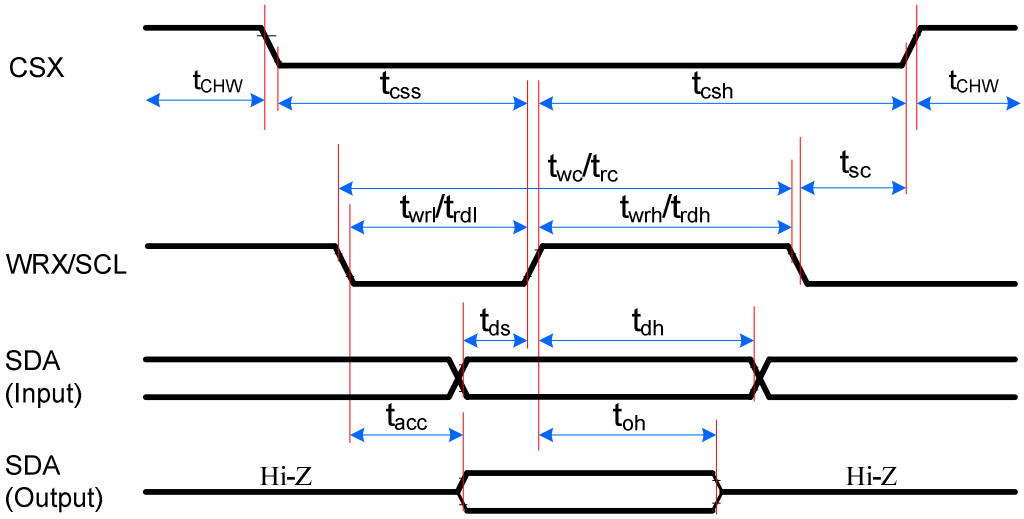
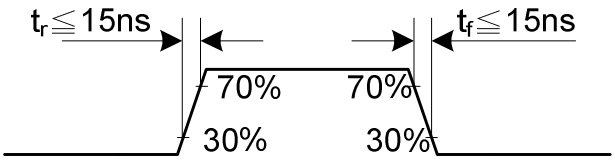
17.4.2. DBI Type C Option 1 (3-Line SPI System) Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



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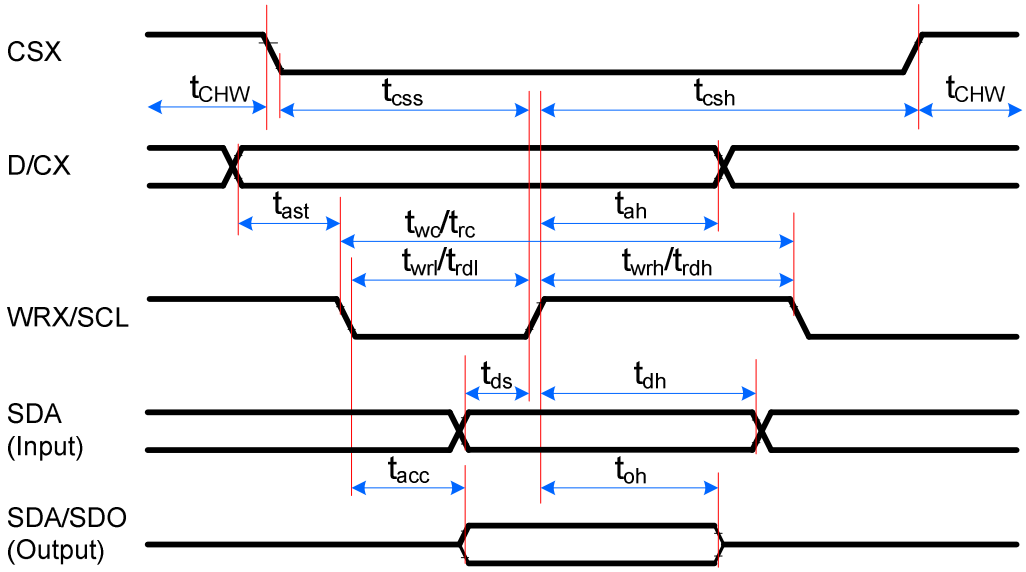
17.4.3. DBI Type C Option 3 (4-Line SPI System) Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Notes:

1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.
2. Does not include signal rising and falling times.

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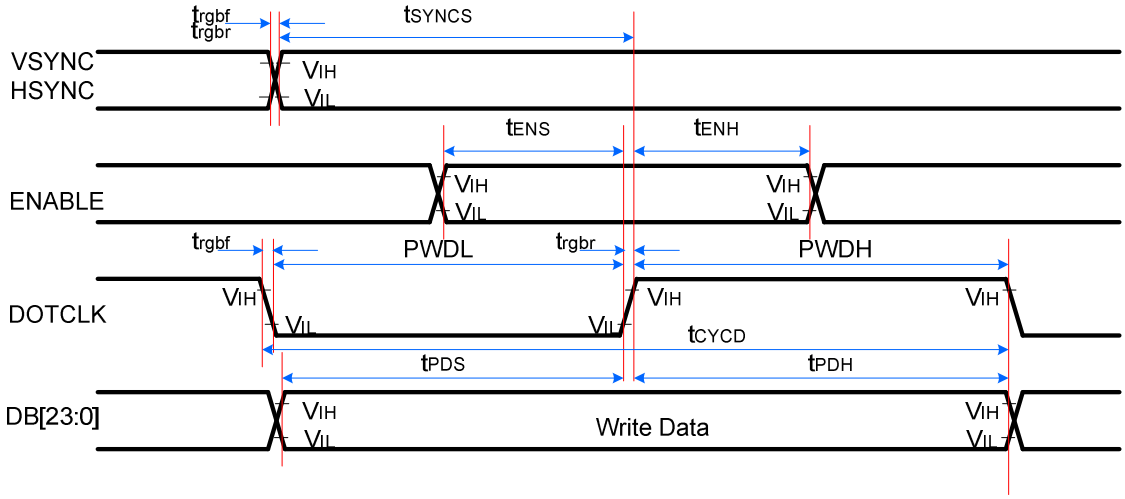
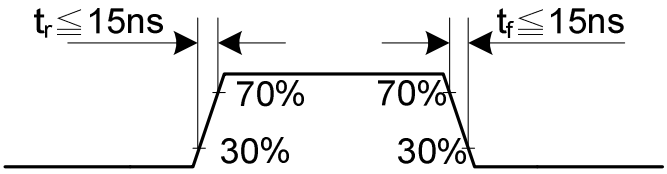
17.4.4. DPI (Display Parallel 16-/18-/24-bit interface) Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V



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17.5. Timing Characteristics of the DSI

17.5.1. High Speed Mode – Clock Channel Timing

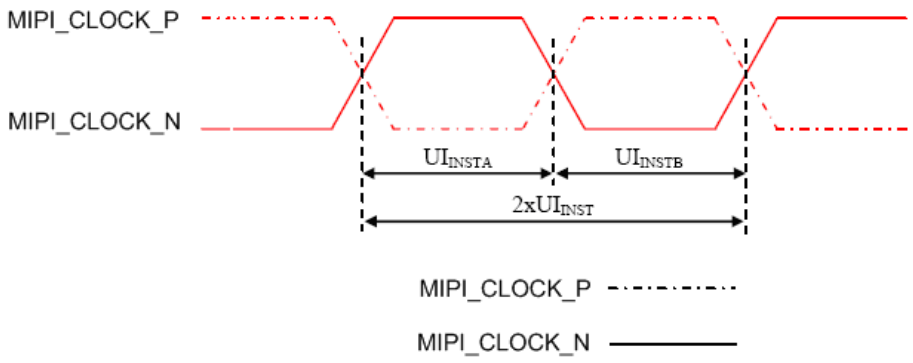


Figure 147: DSI Clock Channel Timing

Table 44: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
MIPI_CLOCK_P/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
MIPI_CLOCK_P/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

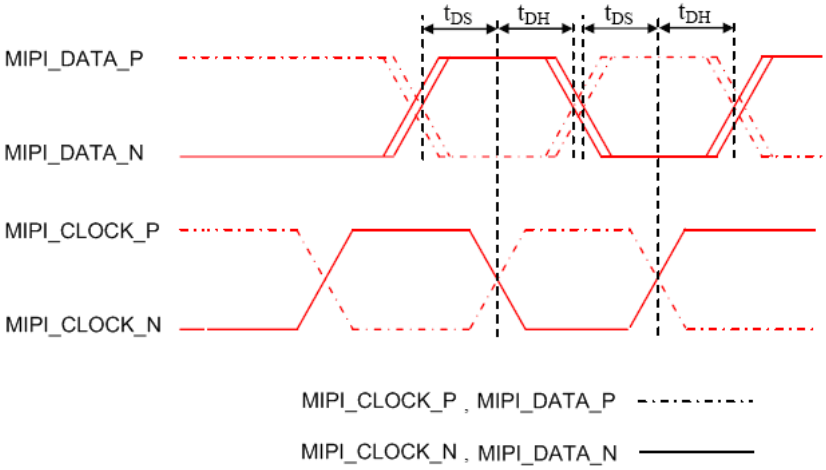
Notes:

1. UI = UIINSTA = UIINSTB
2. See Table 45 for the minimum value of 24 UI per Pixel.

Table 45: Clock Channel Speed Limited

Data type	One Lanes speed	Unit
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	500M	bps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	500M	bps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	500M	bps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	500M	bps

17.5.2. High Speed Mode – Data Clock Channel Timing



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Signal	Symbol	Parameter	Min	Max	Unit
MIPI_DATA_P/N	t_{DS}	Data to Clock Setup time	0.15xUI	-	ps
MIPI_DATA_P/N	t_{DH}	Clock to Data Hold Time	0.15xUI	-	ps

17.5.3. High Speed Mode – Rising and Falling Timings

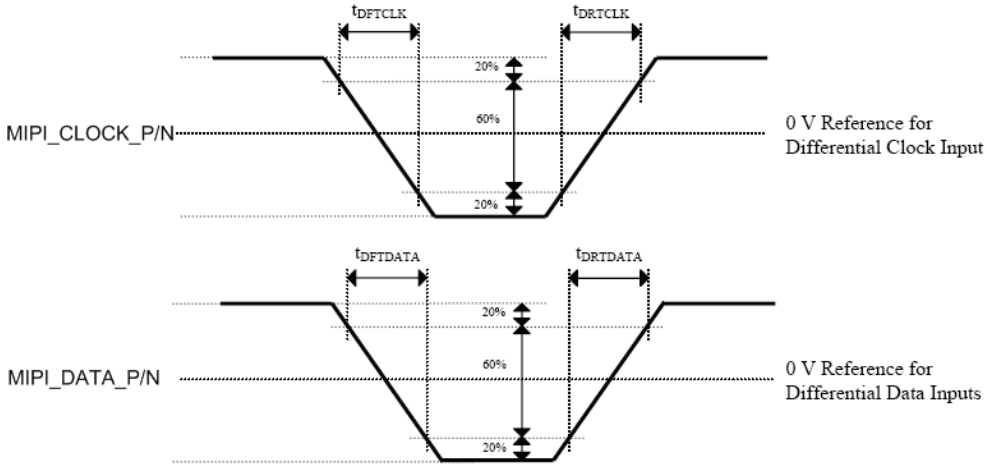

Figure 148: Rising and Falling Timings on Clock and Data Channels

Table 46: Rising and Falling Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	MIPI_CLOCK_P/N	-	-	900	ps
Differential Rise Time for Data	$t_{DRTDATA}$	MIPI_DATA_P/N	-	-	900	ps
Differential Fall Time for Clock	t_{DFTCLK}	MIPI_CLOCK_P/N	-	-	900	ps
Differential Fall Time for Data	$t_{DFTDATA}$	MIPI_DATA_P/N	-	-	900	ps

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

17.5.4. Low Power Mode – Bus Turnaround

Low Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the display module (ILI9488) sequence are illustrated below for reference purpose.

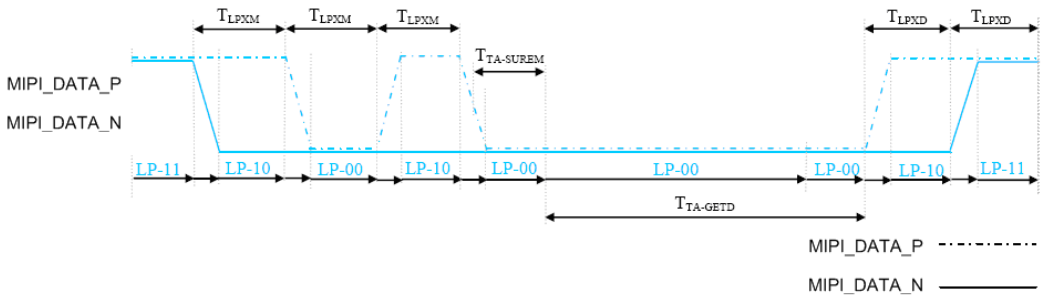

Figure 149: BTA from the MCU to the Display Module

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Low Power Mode and its State Periods on the Bus Turnaround (BTA) from the display module (ILI9488) to the MCU sequence are illustrated below for reference purpose.

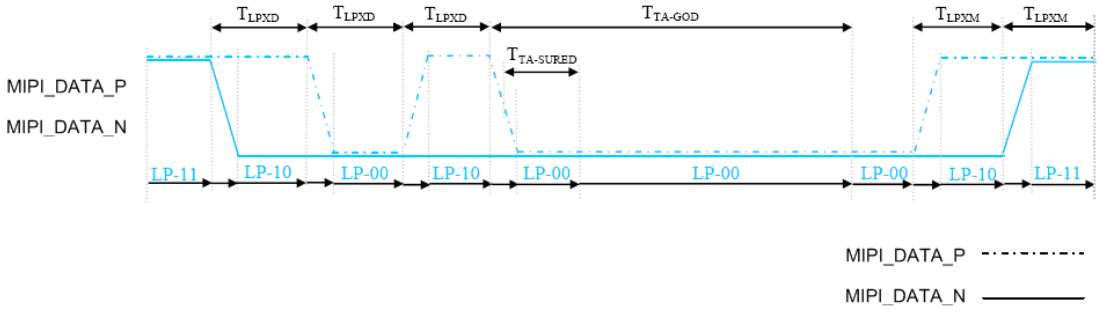

Figure 150: BTA from the Display Module to the MCU

Table 47: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
Input (MIPI_DATA_P/N)	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9488)	50	75	ns
Output (MIPI_DATA_P/N)	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9488_ ➔ MCU)	50	75	ns
Input (MIPI_DATA_P/N)	$T_{TA\text{-}SUREM}$	Time-out before the ILI9488 starts driving	T_{LPXM}	$2xT_{LPXM}$	ns
Output (MIPI_DATA_P/N)	$T_{TA\text{-}SURED}$	Time-out before the MCU starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 48: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
Input (MIPI_DATA_P/N)	$T_{TA\text{-}GETD}$	Time to drive LP-00 by the ILI9488	$5xT_{LPXD}$	ns
Output (MIPI_DATA_P/N)	$T_{TA\text{-}GOD}$	Time to drive LP-00 after turnaround request – MCU	$4xT_{LPXD}$	ns

17.5.5. Data Lanes from Low Power Mode to High Speed Mode

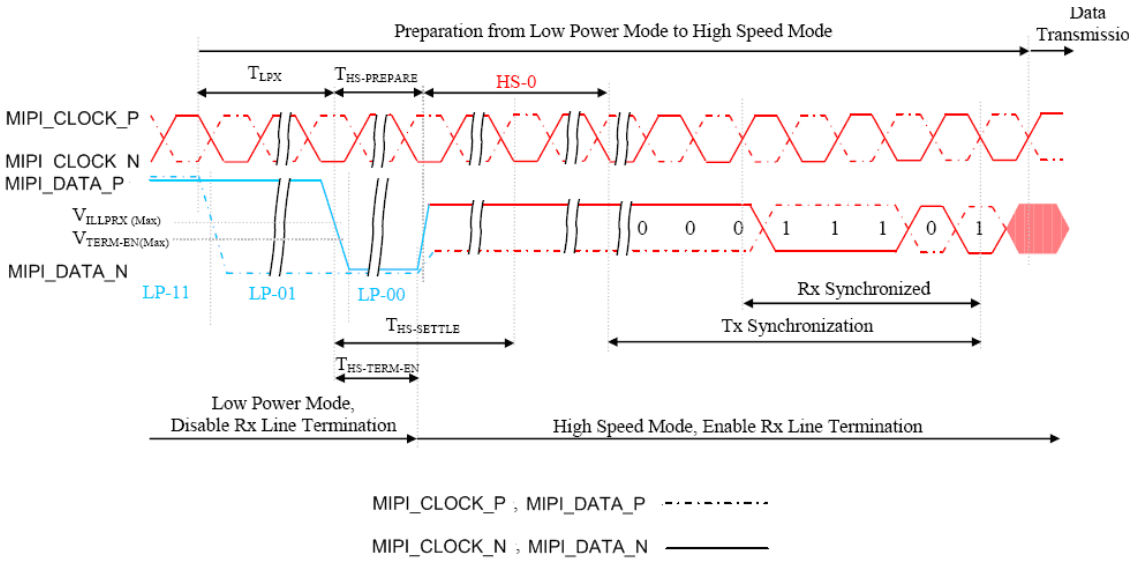

Figure 151: Data Lanes – Low Power Mode to High Speed Mode Timings

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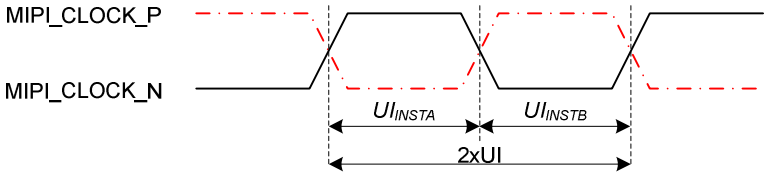
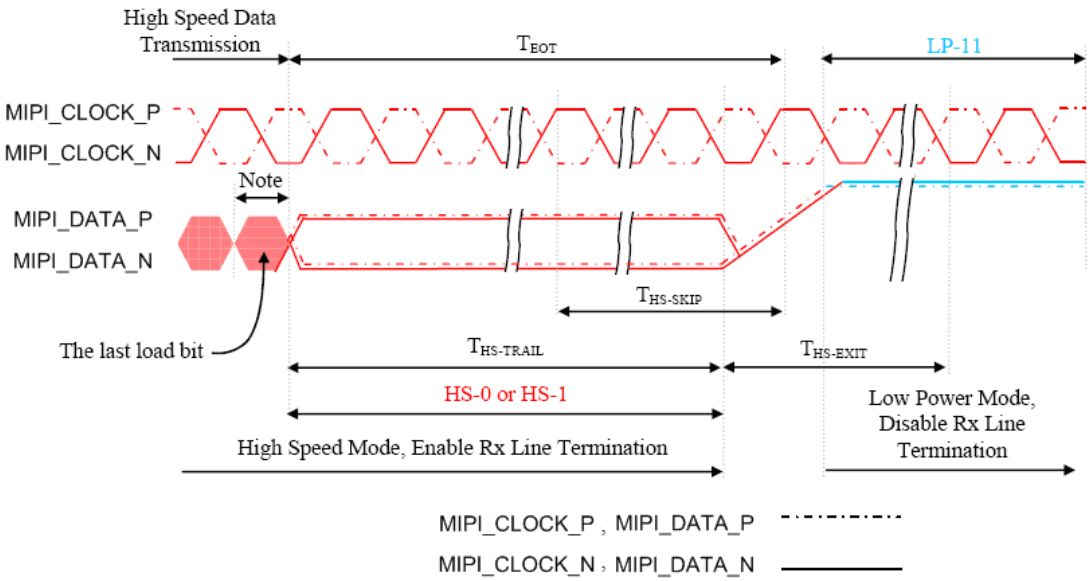
Table 49: Data Lanes – Low Power Mode High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
Input (MIPI_DATA_P/N)	T_{LPX}	Length of any Low Power State Period	50	-	ns
Input (MIPI_DATA_P/N)	$T_{HS\text{-}PREPARE}$	Time to Drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
Input (MIPI_DATA_P/N)	$T_{HS\text{-}TERM\text{-}EN}$	Time to enable Data Lane Receiver line termination measured from when D_n crosses V_{ILMAX}	-	35+4xUI	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$



17.5.6. Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 152: Data Lanes – High Speed Mode to Low Power Mode Timings

Table 50: Data Lanes – High Speed Mode to Low Power Timings

Signal	Symbol	Description	Min	Max	Unit
Input (MIPI_DATA_P/N)	$T_{HS\text{-}SKIP}$	Time-out at the ILI9488 to Ignore Transition Period of EoT	40	50+4xUI	ns
Input (MIPI_DATA_P/N)	$T_{HS\text{-}EXIT}$	Time to Driver LP-11 after HS burst	100	-	ns

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17.5.7. DSI Clock Burst – High Speed Mode to/from Low Power Mode

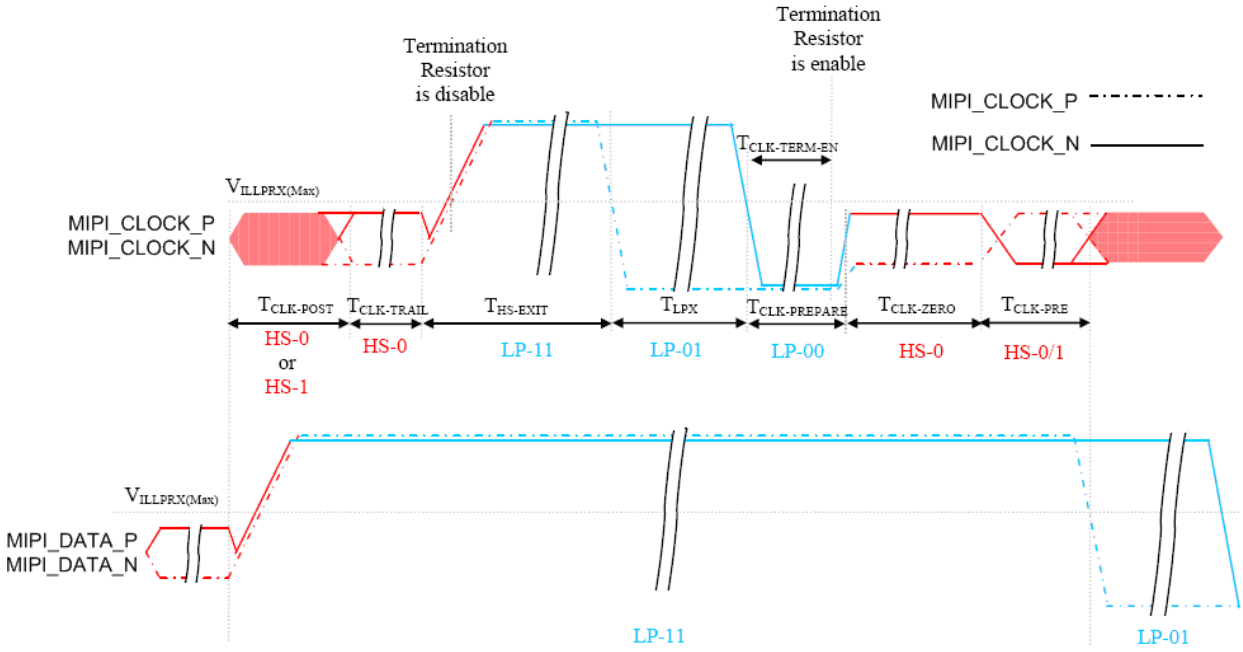
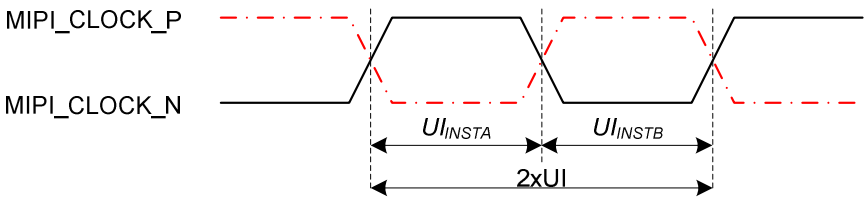


Figure 153: Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 51: Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
Input (MIPI_CLOCK_P/N)	$T_{CLK\text{-}POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK\text{-}TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
Input (MIPI_CLOCK_P/N)	$T_{HS\text{-}EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK\text{-}PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK\text{-}TERM\text{-}EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK\text{-}PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK\text{-}PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$



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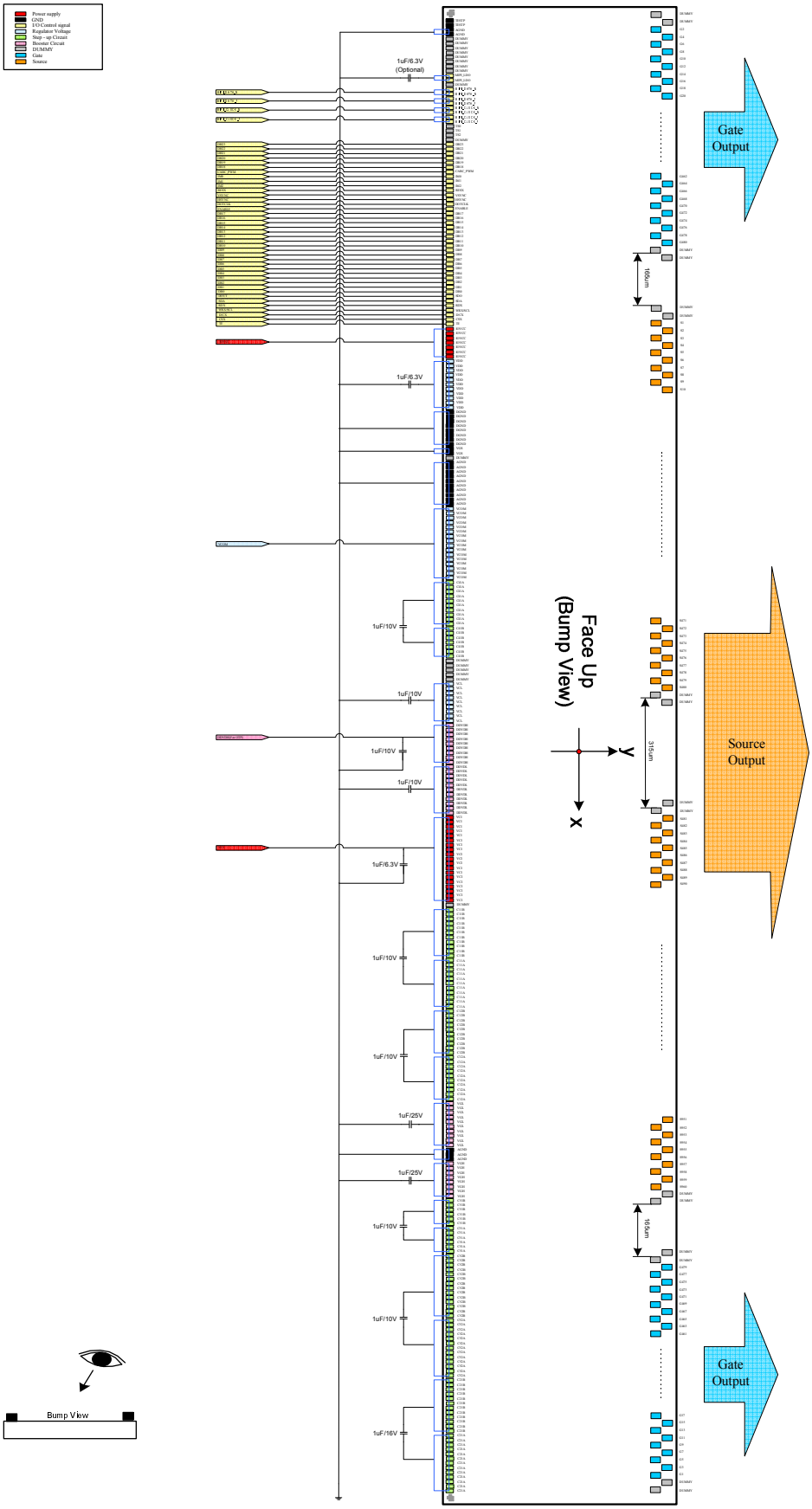
18. Application Circuit



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18.1. Maximum layout resistance

Pin Name	Type	Maximum series resistance	Unit
TESTP	DUMMY	10	Ω
DUMMY	DUMMY	100	Ω
MIPI_LDO	Power Supply	10	Ω
MIPI_DATA_N / P	I / O	10	Ω
MIPI_CLOCK_N / P	Input	10	Ω
TS0	DUMMY	100	Ω
TS1	DUMMY	100	Ω
TS2	DUMMY	100	Ω
DB[23:0]	I / O	100	Ω
CABC_PWM	Output	100	Ω
IM[2:0]	Input	100	Ω
RESX	Input	100	Ω
YSYNC	Input	100	Ω
HSYNC	Input	100	Ω
DOTCLK	Input	100	Ω
ENABLE	Input	100	Ω
SDO	Output	100	Ω
SDA	I / O	100	Ω
RDX	Input	100	Ω
WRX/SCL	Input	100	Ω
D/CX	Input	100	Ω
CSX	Input	100	Ω
TE	Output	100	Ω
IOVCC	Power Supply	5	Ω
VDD	Capacitor connection	5	Ω
DGND	GND	5	Ω
AGND	GND	5	Ω
VGS	GND	10	Ω
C15A/B	Capacitor connection	5	Ω
DDVDL	Capacitor connection	5	Ω
DDVDH	Capacitor connection	5	Ω
VCL	Capacitor connection	5	Ω
VCI	Power Supply	5	Ω
C41A/B	Capacitor connection	5	Ω
VGL	Capacitor connection	5	Ω
VGH	Capacitor connection	5	Ω
C11A/B	Capacitor connection	5	Ω
C12A/B	Capacitor connection	5	Ω
C51A/B	Capacitor connection	5	Ω
C52A/B	Capacitor connection	5	Ω
C21A/B	Capacitor connection	5	Ω
VCOM	Output	5	Ω

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18.2. External Component

The Table 52 shows specifications of external elements connected to the power supply circuit of the ILI9488.

Table 52: External Component Table

Items	Recommended Specification	Pin connection
Capacity 1 µF	6.3V	VDD, VCI, MIPI_LDO(optional, for MIPI-DSI only)
	10V	DDVDH, DDVDL, VCL, C41A/B, C11A/B, C51A/B, C52A/B, C12A/B
	16V	C21A/C21B
	25V	VGH, VGL

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19. Liquid Crystal Power Supply Specifications

Table 53: Liquid Crystal Power Supply Specifications

Item		Description
TFT Source Driver		960 pins, 320 (RGB)
TFT Gate Driver		480 pins
TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
Liquid Crystal Drive Output	S1 ~ S960	V0 ~ V63 grayscales
	G1 ~ G480	VGH – VGL
	VCOM	-2.0 ~ 0V
Input Voltage	IOVCC	1.65 ~ 3.30V
	VCI	2.50 ~ 3.30V
Liquid Crystal Drive Voltages	DDVDH	4.5 ~ 6.0V
	DDVDL	-6.0 ~ -4.5V
	VGH	10.0V ~ 20.0V
	VGL	-15.0V ~ -6.0V
	VCL	-3.0V ~ -2.0 V
	VGH – VGL	Max. 32.0V
Internal Step-up Circuits	VGH	VCI x4, x5, x6,
	VGL	VCI x-3, x-4, x-5

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20. Revision History

Version No.	Date	Page	Description
V100	2012/11/28	All	New created

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