MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI160160H-G

Revision	1.0
Engineering	
Date	
Our Reference	

MODE OF DISPLAY

Display mode	**Display condition**	**Viewing direction**
STN : ☐ Yellow green	☐ Reflective type	☐ 6 O' clock
☐ Grey	☐ Transflective type	☐ 12 O' clock
☐ Blue (negative)	☐ Transmissive type	☐ 3 O' clock
☐ FSTN positive	☐ Others	☐ 9 O' clock
☐ FSTN negative		

GENERAL DESCRIPTION

Display mode : 160 x160 dots COG LCD module

Interface : 8/16 bit parallel or serial

Driving method : 1/160 duty, 1/14 bias

Controller IC : Sitronix **ST7529** or equivalent

For the detailed information, please refer to the IC specifications.

MECHANICAL DIMENSIONS

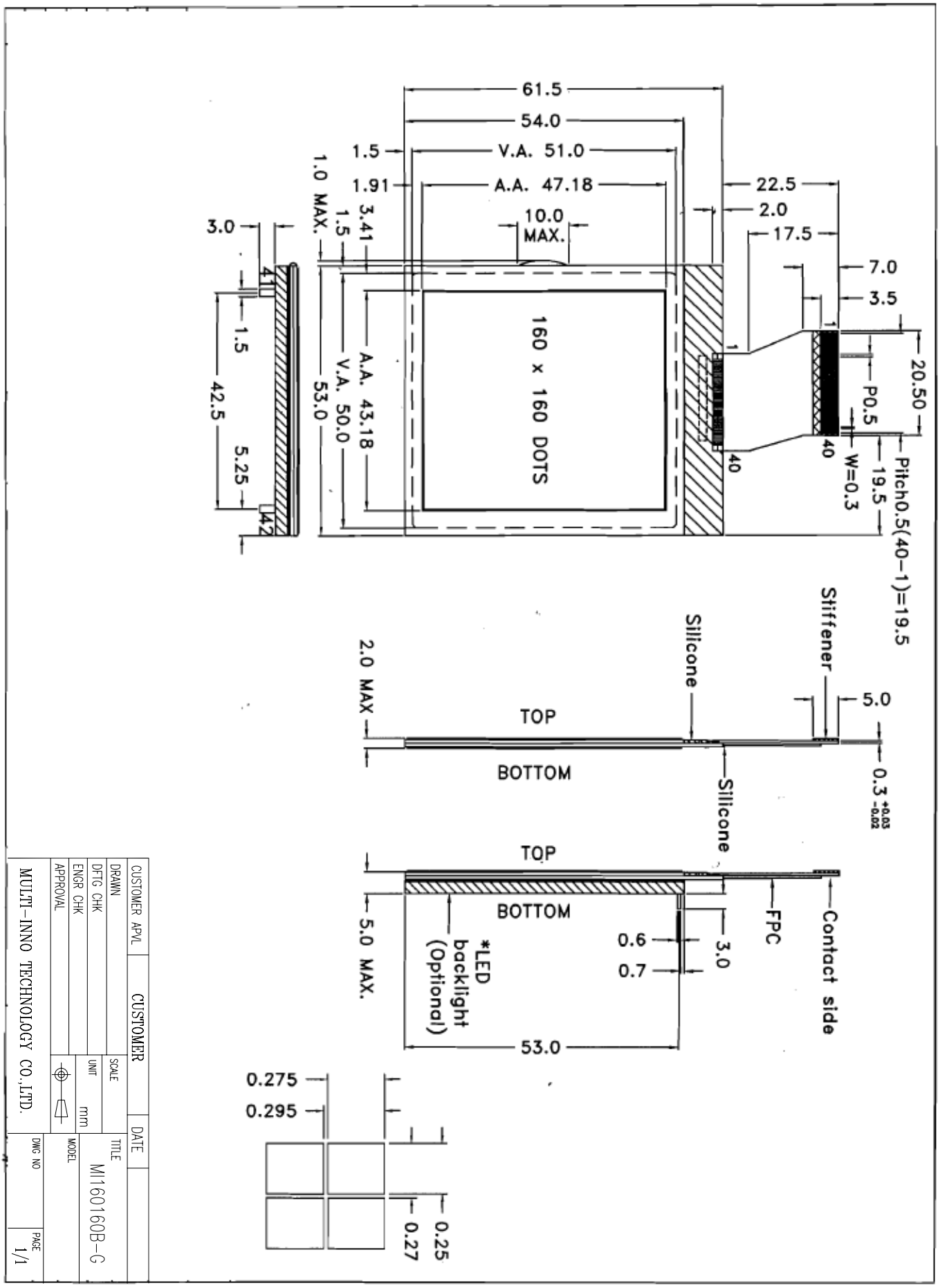
Item	Dimension	Unit	Item	Dimension	Unit
Outline Dimension (LED backlight)	53.0(L)x61.5(W)x5.0MAX.(H)	mm	Dot Pitch	0.27(L)x0.295(W)	mm
Outline Dimension (No backlight)	53.0(L)x61.5(W)x2.0MAX.(H)	mm	Dot Size	0.25(L)x0.275(W)	mm
Viewing Area	50.0(L)x51.0(W)	mm	-	-	-

CONNECTOR PIN ASSIGNMENT

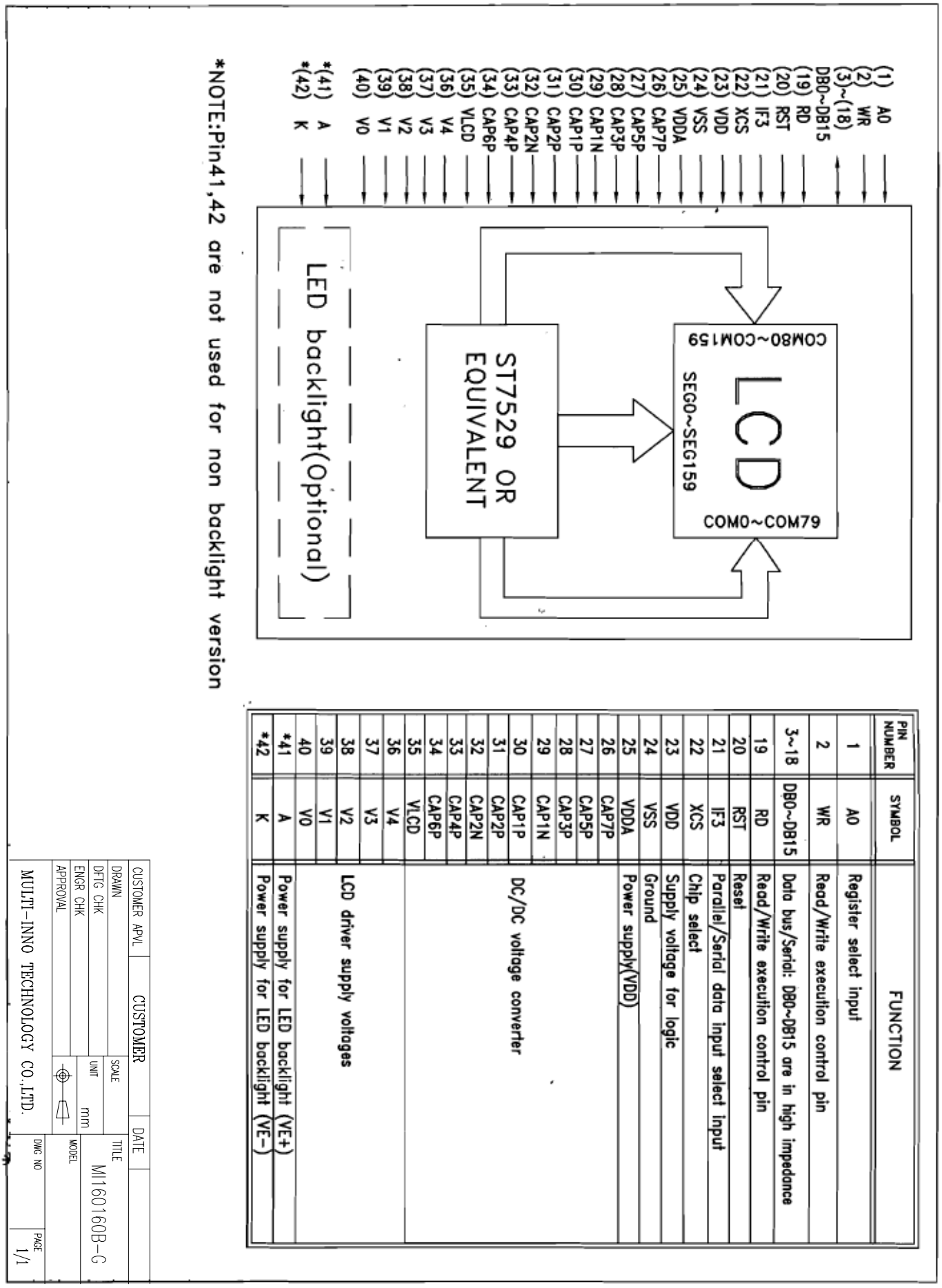
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	A0	Register select input	30	CAP1P	DC/DC voltage converter
2	WR	Read/Write execution control pin	31	CAP2P	
3~18	DB0~DB15	Data bus/Serial: DB0~DB15 are in high impedance	32	CAP2N	
19	RD	Read/Write execution control pin	33	CAP4P	
20	RST	Reset	34	CAP6P	
21	IF3	Parallel/Serial data input select input	35	VLCD	
22	XCS	Chip select	36	V4	LCD driver supply voltages
23	VDD	Supply voltage for logic	37	V3	
24	VSS	Ground	38	V2	
25	VDDA	Power supply(VDD)	39	V1	
26	CAP7P	DC/DC voltage converter	40	V0	
27	CAP5P		*41	A	Power supply for LED backlight (VE+)
28	CAP3P		*42	K	Power supply for LED backlight (VE-)
29	CAP1N				

Note (*): Pin 41, 42 are used for backlight versions only.

COUNTER DRAWING OF MODULE DIMENSION



COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



PIN NUMBER	SYMBOL	FUNCTION
1	A0	Register select input
2	WR	Read/Write execution control pin
3~18	DB0~DB15	Data bus/Serial: DB0~DB15 are in high impedance
19	RD	Read/Write execution control pin
20	RST	Reset
21	IF3	Parallel/Serial data input select input
22	XCS	Chip select
23	VDD	Supply voltage for logic
24	VSS	Ground
25	VDDA	Power supply(VDD)
26	CAP7P	DC/DC voltage converter
27	CAP5P	
28	CAP3P	
29	CAP1N	
30	CAP1P	
31	CAP2P	
32	CAP2N	
33	CAP4P	
34	CAP6P	
35	VLCD	
36	V4	LCD driver supply voltages
37	V3	
38	V2	
39	V1	
40	V0	
*41	A	Power supply for LED backlight (VE+)
*42	K	Power supply for LED backlight (VE-)

CUSTOMER APVL	CUSTOMER		DATE
DRAWN		SCALE	TITLE
DFTG CHK		UNIT mm	MI160160B-G
ENGR CHK			MODEL
APPROVAL			DWG NO
MULTI-INNO TECHNOLOGY CO.,LTD.			PAGE 1/1

COUNTER DRAWING OF SPECIFICATION

1.General specification

Display mode	: 160X160 dots COG LCD module
Interface	: 8/16 bit parallel or serial
Driving method	: 1/160 duty, 1/14 bias

2.Electrical specification

Supply voltage for logic(VDD)	: 3.3V
Supply voltage for LCD drive(Vlcd)	: 15.0V(Generated by internal booster)

3.Electrical specification

Backlight type	: Side-lited LED backlight
Backlight voltage	: 3.3V@60mA
Backlight color	: White

4.Mechanical specification

Dot size[mm]	: 0.25(L)x0.275(W)
Dot pitch[mm]	: 0.27(L)x0.295(W)
Module dimension[mm]	: 53.0(L)x61.5(W)x2.0/5.0MAX.(H)
Viewing area[mm]	: 50.0(L)x51.0(W)

CUSTOMER APVL	CUSTOMER		DATE
DRAWN		SCALE	TITLE MI160160B-G
DFTG CHK		UNIT mm	
ENGR CHK			
APPROVAL			MODEL
MULTI-INNO TECHNOLOGY CO.,LTD.			DWG NO / PAGE 1/1

ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, @Ta=25℃

Item	Symbol	MIN.	TYP.	MAX.	Unit	Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage for logic	VDD	3.2	3.3	3.4	V	"H"Level Input Voltage	VIH	0.7VDD	—	VDD	V
Supply Current for logic	IDD	—	166	190	μA	"L"Level Input Voltage	VIL	VSS	—	0.3VDD	V
Operating Voltage for LCD	VLCD	11.8	12.0(*)	12.2	V	—	—	—	—	—	—
EL Backlight Voltage (VEL)						**Backlight Current**					
EL (@ Frequency 400Hz)	—	—	—	—	—	—	—	—	—	—	—
Side-lited LED Backlight Forward Voltage (VF)						**Side-lited LED Backlight Forward Current (IF)**					
White	VBL	3.1	3.3	3.5	V	White	IBL	—	60	100	mA
Blue	VBL				V	Blue	IBL	—			mA
Yellow Green	VBL				V	Yellow Green	IBL	—			mA

Note : (*) Please refer to **REFERENCE CIRCUIT EXAMPLE** (5X Boosting Circuit).

ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions.

Item	Symbol	Rating (for normal temperature)	Rating (for wide temperature)	Unit
Supply Voltage for Logic	VDD	-0.5 to 4.0	-0.5 to 4.0	V
Input Voltage for Logic	VIN	-0.5 to VDD +0.5	-0.5 to VDD +0.5	V
Operating Temperature	Topr	0 to 50	-20 to 70	℃
Storage Temperature	Tstg	-10 to 60	-30 to 80	℃

DC CHARACTERISTICS

T_a = -30℃ to +85℃

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)		VDD VDD1	-	2.4	-	3.3	V	VDD*1 VDD1
Operating Voltage (2)		VDD2 VDD3 VDD4 VDD5	(Relative to VSS)	2.4	-	3.3	V	VDD2 VDD3 VDD4 VDD5
High-level Input Voltage		VIH	-	0.7 VDD	-	VDD	V	*2
Low-level Input Voltage		VIL	-	VSS	-	0.3 VDD	V	*2
High-level Output Current		IOH	VDD=2.7V VOH =2.2V	0.5	-	-	mA	*3
Low-level Output Current		IOL	VDD=2.7V VOL = 0.5V	-	-	-0.5	mA	*3
Input leakage current		ILI	VIN = VDD or VSS	-1.0	-	1.0	μA	*4
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VSS) V0 = 14.0V VDD = 2.7V	-	1.4	2.0	KΩ	SEGn COMn *5
Oscillator Frequency	Internal Oscillator	fOSC	1/160 duty Ta = 25°C VDD = 2.7V CLD = 0	-	12.4	26	kHz	CL*6
	External Input	fCL		-	12.4	26	kHz	CL
	Frame frequency	fFRAME		-	78	160	Hz	SEGn

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	2.4	-	3.3	V	VDD
	Supply Step-up output voltage Circuit	VLCDOUT	(Relative To VSS)	-	-	18	V	VLCDOUT
	Voltage regulator Circuit Operating Voltage	VLCDIN	(Relative To VSS)	-	-	18	V	VLCDIN

RESET CIRCUIT

When Power is Turned On

Input power (VDD1~VDD5)

↓

Be sure to apply POWER-ON RESET (RST = LOW)

↓

<Display Setting>	**<<State after resetting>>**
Display control (DISCTRL)	
Setting clock dividing ratio:	2 dividing
Duty setting:	1/4
Setting reverse rotation number of line:	11H reverse rotations
Common scan direction (COMSCN)	
Setting scan direction:	COM0 -> COM79, COM80-> COM159
Temperature Gradient Setting (TMPGRD)	

↓

Oscillation ON (OSCON)	Oscillation OFF

↓

Sleep-out (SLIPOUT)	Sleep-in

↓

<Power Supply Setting>	**<<State after resetting>>**
Electronic volume control (VOLCTRL)	
Setting volume value:	0
Setting built-in resistance value:	0 (3.95)
Power control (PWRCTR)	
Setting operation of power supply circuit:	All OFF

↓

<Display Setting 2>	**<<State after resetting>>**
Normal rotation of display (DISNOR)/Inversion of display (DISINV):	Normal rotation of display
Partial-in (PTLIN)/Partial-out (PTLOUT)	Partial-out
Setting fix area:	0
Area scroll set (ASSET)	
Setting area scroll region:	0
Setting area scroll type:	Full-screen scroll
Scroll start set (SCSTART)	
Setting scroll start address:	0

↓

<Display Setting 3>	**<<State after resetting>>**
Data control (DATCTRL)	
Setting normal rotation/inversion of line address:	Normal rotation

Setting normal rotation/inversion of column address: Normal rotation

Setting direction of address scanner: Column direction

Setting gradation: 2B3P mode

↓

<RAM Setting> **<<State after resetting>>**

Line address set (LASET)

Setting start line address: 0

Setting end line address: 0

Column address set (CASET)

Setting start column address: 0

Setting end column address: 0

↓

<RAM Write> **<<State after resetting>>**

Memory write command (RAMWR)

Writing displayed data: Repeat as many as the number needed and exit by entering other command.

↓

<Waiting (approximately 100ms)>

Wait until the power supply voltage has stabilized.

Enter the command of power supply control first, and then wait at least 100ms before entering the display ON command when the built-in power supply circuit operates.

If you do not wait, an unexpected display may appear on the liquid crystal panel.

↓

DISPLAY ON (DISON): DISPLAY OFF

*1: When the IC is in SLEEP IN state, the liquid crystal drive power supply, the boosting power output, and GND pin are connected together, therefore, the SLEEP OUT command must be entered to cancel the SLEEP state prior to turning on the built-in circuit.

(Note) If changes are unnecessary after resetting, command input is unnecessary.

Command table

Ext=0 or Ext=1

Index	Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	Ext In	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None
2	Ext Out	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None

Ext=0

Index	Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None
2	DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None
3	DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None
4	DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse Display	A7	None
5	COMSCN	0	1	0	1	0	1	1	1	0	1	1	COM Scan Direction	BB	1 byte
6	DISCTRL	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3 bytes
7	SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None
8	SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None
9	LASET	0	1	0	0	1	1	1	0	1	0	1	Line Address Set	75	2 bytes
10	CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set	15	2 bytes
11	DATSDR	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	3 bytes
12	RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data
13	RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from Memory	5D	Data
14	PTLIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 bytes
15	PTLOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None
16	RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read and Modify Write	E0	None
17	RMWOUT	0	1	0	1	1	1	0	1	1	1	0	RMW end	EE	None
18	ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 bytes
19	SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte
20	OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None
21	OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None
22	PWRCTRL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte
23	VOLCTRL	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 bytes
24	VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None
25	VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None
26	RESERVED	0	1	0	1	0	0	0	0	0	1	0	Not Use	82	0
27	EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None

28	EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None
29	NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None
30	STREAD	0	0	1	Read Data								Status Read		
31	EPINT	0	1	0	0	0	0	0	0	1	1	1	Initial code(1)	07	1 byte

Ext=1

Index	*Command*	*A0*	*RD*	*WR*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*	*Function*	*Hex*	*Parameter*
1	Gray 1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Gray PWM Set	20	16 bytes
2	Gray 2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Gray PWM Set	21	16 bytes
3	Wt. Set	0	1	0	0	0	1	0	0	0	1	0	Weight Set	22	3 bytes
4	ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog Circuit Set	32	3 bytes
5	DITHOFF	0	1	0	0	0	1	1	0	1	0	0	Dithering Circuit Off	34	None
6	DITHON	0	1	0	0	0	1	1	0	1	0	1	Dithering Circuit On	35	None
7	EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1 byte
8	EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM	CC	None
9	EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write to EEPROM	FC	None
10	EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None

Note: The table above is for 8-bit interface. For the application of 16-bit interface, fill D15~8 with 0, and other bits are just the same with the table above.

Initializing with the Built-in Power Supply Circuits

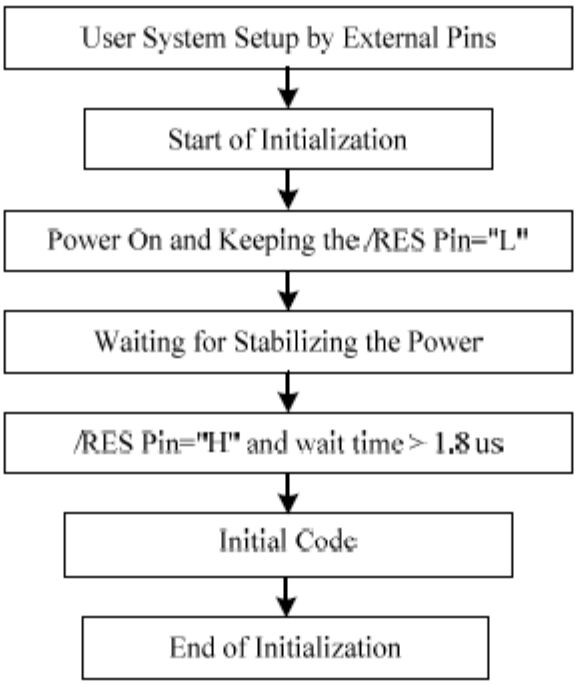


Figure 8.2.2.1 Initializing with the Built-in Power Supply Circuits

AC CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

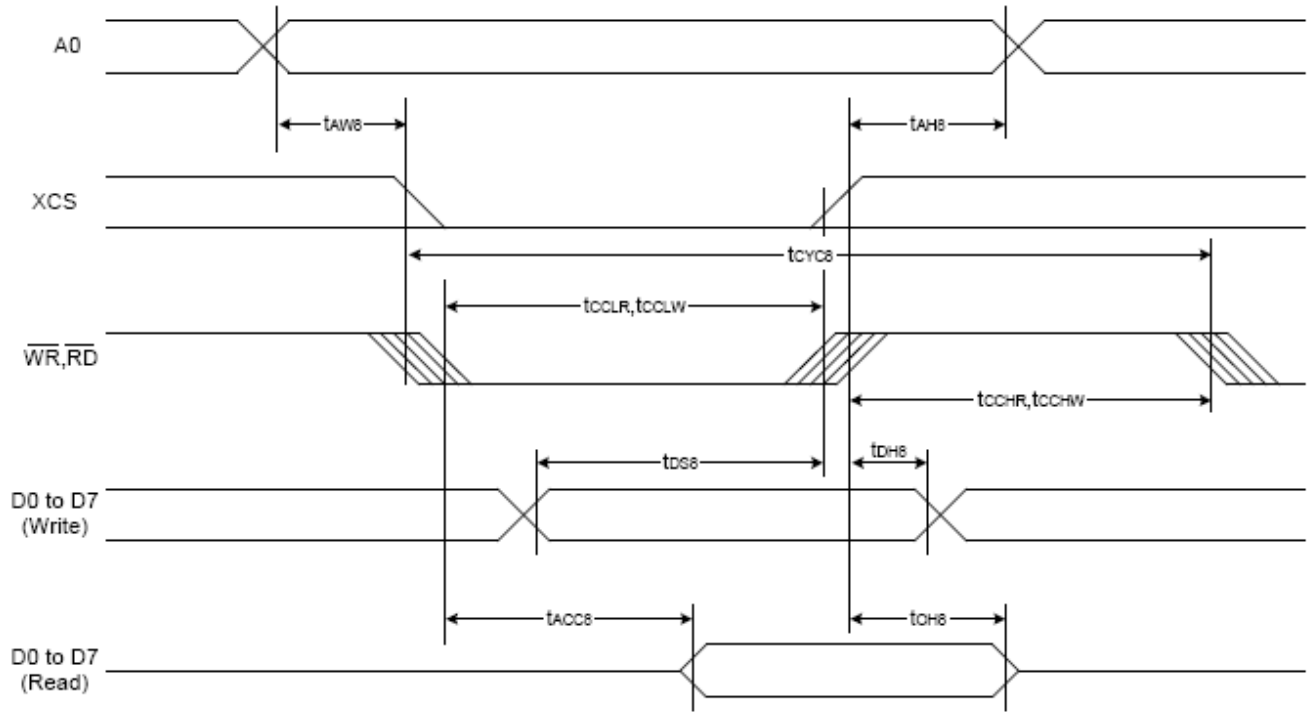


Figure 39.

(VDD = 3.3V , Ta = –30 to 85°C, Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8	-	20	-	ns
Address setup time		tAW8	-	20	-	
System cycle time		tCYC8	-	200	-	
Enable L pulse width (WRITE)	WR	tCCLW	-	100	-	
Enable H pulse width (WRITE)		tCCHW	-	100	-	
Enable L pulse width (READ)	RD	tCCLR	-	100	-	
Enable H pulse width (READ)		tCCHR	-	100	-	
WRITE Data setup time	D0 to D7	tDS8	-	150	-	
WRITE Data hold time		tDH8	-	20	-	
READ access time		tACC8	CL = 100 pF	-	40	
READ Output disable time		tOH8	CL = 100 pF	-	30	

(VDD = 2.7 V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8	-	20	-	ns
Address setup time		tAW8	-	30	-	
System cycle time		tCYC8	-	250	-	
Enable L pulse width (WRITE)	WR	tCCLW	-	150	-	
Enable H pulse width (WRITE)		tCCHW	-	100	-	
Enable L pulse width (READ)	RD	tCCLR	-	150	-	
Enable H pulse width (READ)		tCCHR	-	100	-	
WRITE Data setup time	D0 to D7	tDS8	-	200	-	
WRITE Data hold time		tDH8	-	20	-	
READ access time		tACC8	CL = 100 pF	-	40	
READ Output disable time		tOH8	CL = 100 pF	-	30	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between XCS being "L" and WR and RD being at the "L" level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

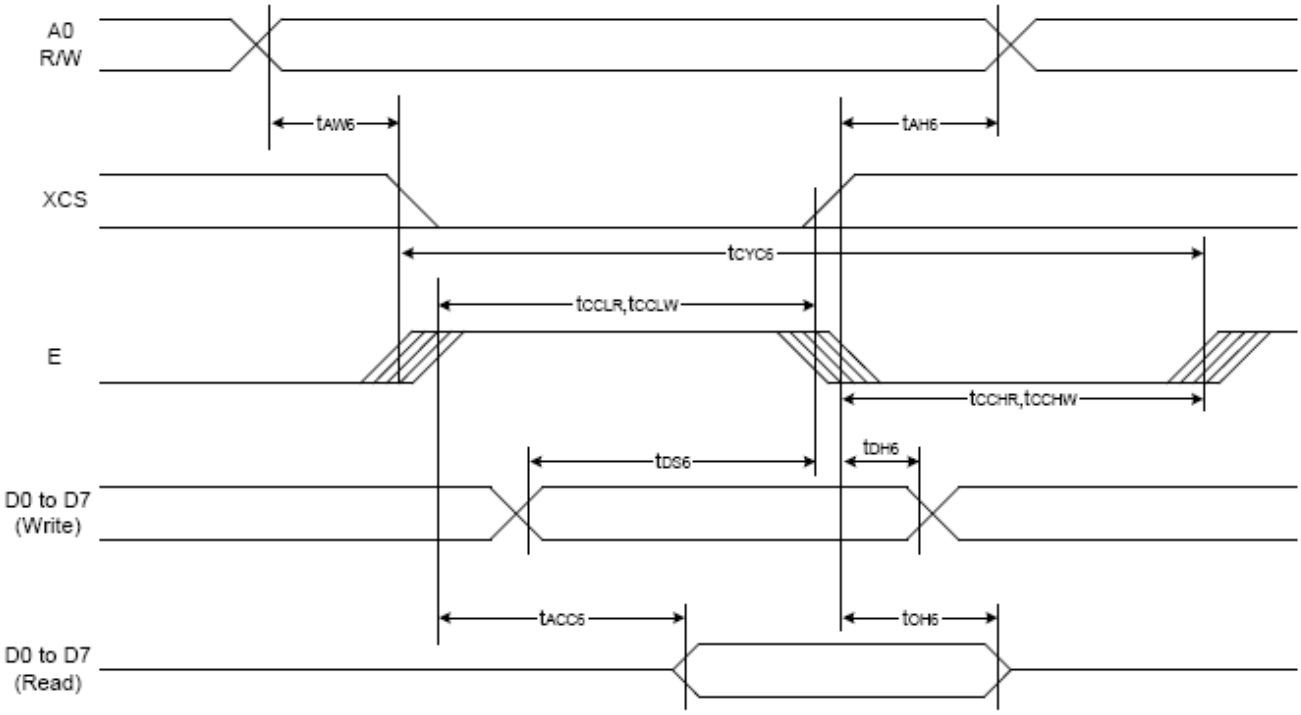


Figure 40.

(VDD = 3.3 V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6	-	20	-	ns
Address setup time		tAW6	-	20	-	
System cycle time		tCYC6	-	200	-	
Enable L pulse width (WRITE)	WR	tEWLW	-	100	-	
Enable H pulse width (WRITE)		tEWHW	-	100	-	
Enable L pulse width (READ)	RD	tEWLR	-	100	-	
Enable H pulse width (READ)		tEWHR	-	100	-	
WRITE Data setup time	D0 to D7	tDS6	-	150	-	
WRITE Data hold time		tDH6	-	20	-	
READ access time		tACC6	CL = 100 pF	-	40	
READ Output disable time		tOH6	CL = 100 pF	-	30	

(VDD = 2.7V , Ta =–30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6	-	20	-	ns
Address setup time		tAW6	-	30	-	
System cycle time		tCYC6	-	250	-	
Enable L pulse width (WRITE)	WR	tEWLW	-	150	-	
Enable H pulse width (WRITE)		tEWHW	-	100	-	
Enable L pulse width (READ)	RD	tEWLR	-	150	-	
Enable H pulse width (READ)		tEWHR	-	100	-	
WRITE Data setup time	D0 to D7	tDS6	-	200	-	
WRITE Data hold time		tDH6	-	20	-	
READ access time		tACC6	CL = 100 pF	-	40	
READ Output disable time		tOH6	CL = 100 pF	-	30	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between XCS being “L” and E.

SERIAL INTERFACE (4-Line Interface)

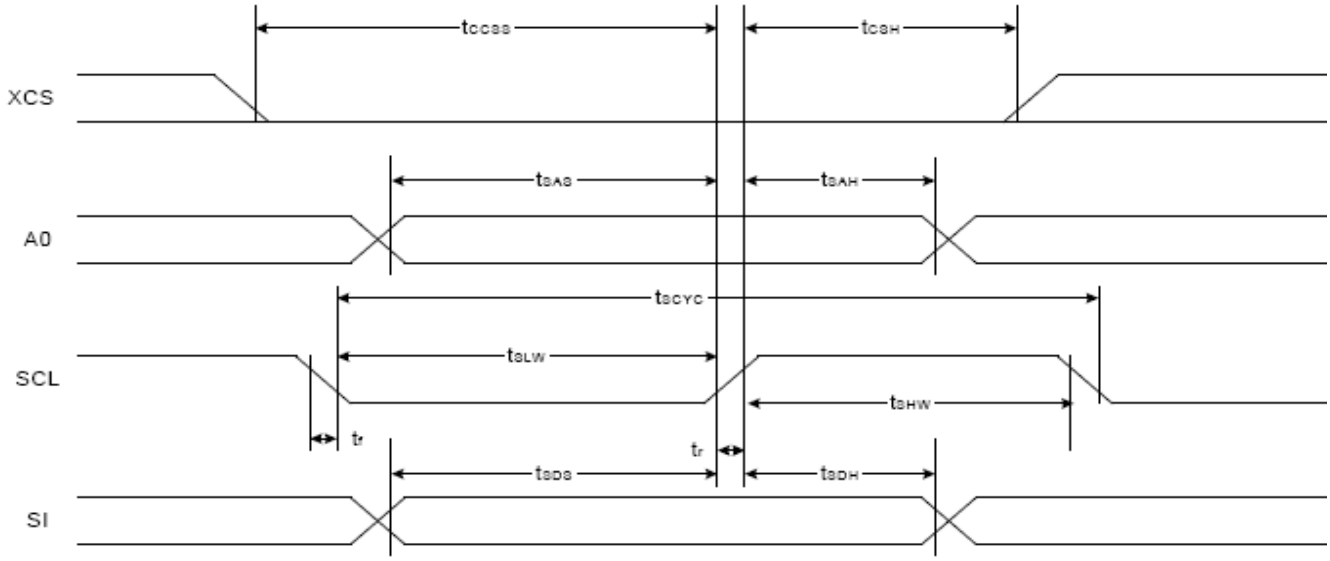


Fig 41.

(V_{DD}=3.3V,Ta= –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	100	-	ns
SCL “H” pulse width		tSHW	-	50	-	
SCL “L” pulse width		tSLW	-	50	-	
Address setup time	A0	tSAS	-	40	-	
Address hold time		tSAH	-	30	-	
Data setup time	SI	tSDS	-	30	-	
Data hold time		tSDH	-	30	-	
CS-SCL time	XCS	tCSS	-	20	-	
CS-SCL time		tCSH	-	50	-	

(V_{DD}=2.7V,Ta= –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	110	-	ns
SCL “H” pulse width		tSHW	-	60	-	
SCL “L” pulse width		tSLW	-	50	-	
Address setup time	A0	tSAS	-	50	-	
Address hold time		tSAH	-	40	-	
Data setup time	SI	tSDS	-	40	-	
Data hold time		tSDH	-	40	-	
CS-SCL time	XCS	tCSS	-	30	-	
CS-SCL time		tCSH	-	60	-	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE (3-Line Interface)

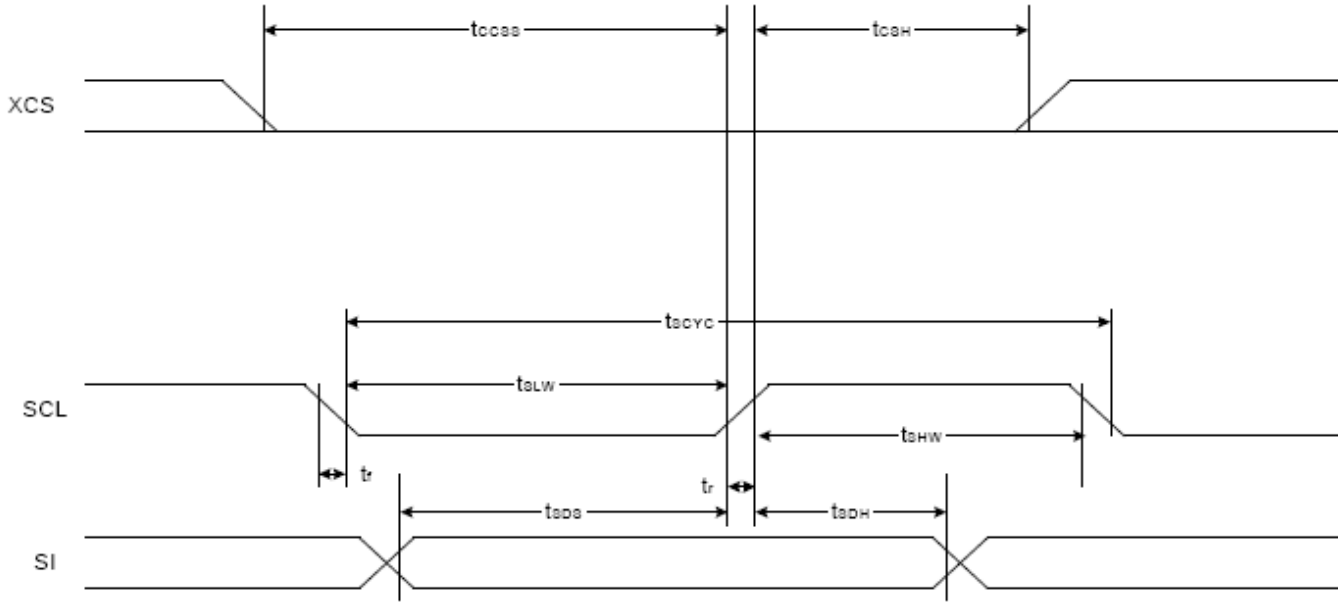


Fig 42.

(V_{DD}=3.3V,Ta= –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	100	-	ns
SCL "H" pulse width		tSHW	-	50	-	
SCL "L" pulse width		tSLW	-	50	-	
Data setup time	SI	tSDS	-	30	-	
Data hold time		tSDH	-	30	-	
CS-SCL time	XCS	tCSS	-	20	-	
CS-SCL time		tCSH	-	50	-	

(V_{DD}=2.7V,Ta= –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	110	-	ns
SCL "H" pulse width		tSHW	-	60	-	
SCL "L" pulse width		tSLW	-	50	-	
Data setup time	SI	tSDS	-	40	-	
Data hold time		tSDH	-	40	-	
CS-SCL time	XCS	tCSS	-	30	-	
CS-SCL time		tCSH	-	60	-	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

RESET TIMING

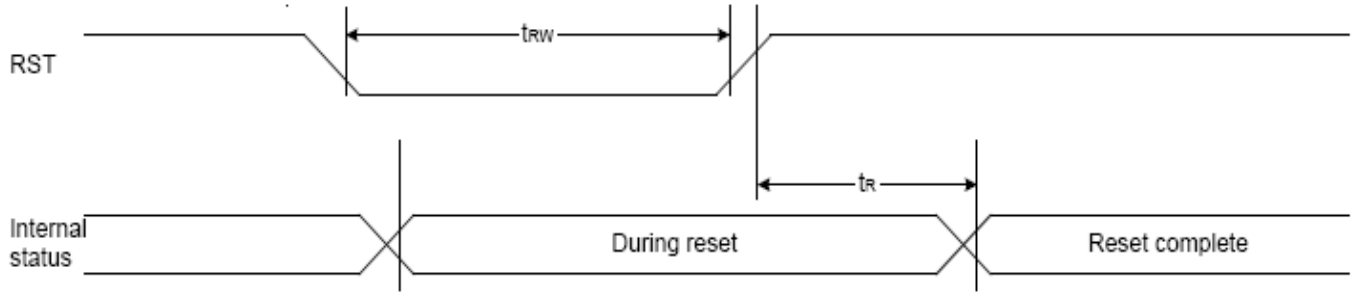


Fig 43.

(VDD =3.3V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR	-	-	-	1	us
Reset "L" pulse width	RST	tRW	-	1	-	-	us

(VDD = 2.7V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR	-	-	-	1.5	us
Reset "L" pulse width	RST	tRW	-	1.5	-	-	us

ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = VOP / 64 Hz
TEMPERATURE = 23 ± 5 °C
RELATIVE HUMIDITY = 60 ± 20 %

ITEM	SYMBOL	UNIT	TYP. STN
RESPONSE TIME	Ton	ms	320
	Toff	ms	430
CONTRAST RATIO	Cr	-	8
VIEWING ANGLE (Cr ≥ 2)	V3:00	°	40
	V6:00	°	55
	V9:00	°	40
	V12:00	°	35

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

RELIABILITY OF LCD MODULE

ITEM	TEST CONDITION FOR NORMAL TEMPERATURE	TEST CONDITION FOR WIDE TEMPERATURE	TIME
High temperature operating	50°C	70°C	240 hours
Low temperature operating	0°C	-20°C	240 hours
High temperature storage	60°C	80°C	240 hours
Low temperature storage	-10°C	-30°C	240 hours
Temperature-humidity storage	40°C 90% R.H.	60°C 90% R.H.	96 hours
Temperature cycling	-10°C to 60°C 30 Min Dwell	-30°C to 80°C 30 Min Dwell	5 cycle
Vibration Test at LCM Level	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	—

SAMPLING METHOD

SAMPLING PLAN: MIL-STD 105E

CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65% MINOR – 1.5%

QUALITY STANDARD

DEFECT	CRITERIA	TYPE	FIGURE
SHORT CIRCUIT	-	MAJOR	-
MISSING SEGMENT	-	MAJOR	-
UNEVEN / POOR CONTRAST	-	MAJOR	-
CROSS TALK	-	MAJOR	-
PIN HOLE	MAX(a,b) ≤ 1 / 4 W	MINOR	1
EXCESS SEGMENT	MAX(c,d) ≤ 1 / 4 T	MINOR	1
BUBBLES	d* ≤ 0.2 QTY=2	MINOR	2
BLACKS SPOTS	d ≤ 0.2 N.A.** 0.2<d≤0.3 QTY≤1 d>0.3 QTY=0	MINOR	2
LINE SCRATCHES	x≤0.5 y≤0.05 QTY=1	MINOR	3
BLACK LINE	x≤0.5 y≤0.05 QTY=1	MINOR	3

*d = MAX (d_1,d_2) ** N. A . = NOT APPLICABLE DEFECT TABLE : B

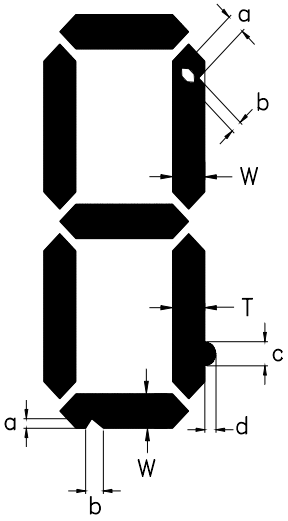
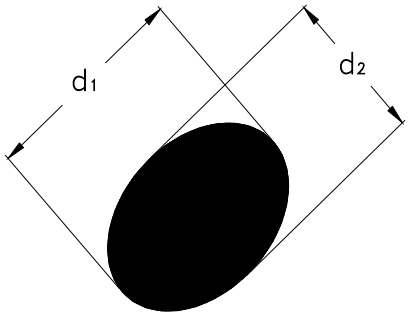
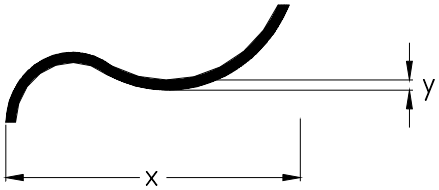


fig . 1



POLARIZER BUBBLES / SPOTS
fig . 2



LINE SCRATCHES / BLACK LINE
fig . 3

QUALITY STANDARD (CONT .)

DEFECT		CRITERIA	TYPE	FIGURE
CHIPS	CONTACT EDGE	e≤1/2T f<1/4W g<2.0	MINOR	4
	BOTTOM GLASS	P<0.5 q<2.0 r<1/2T		4
	CORNER	a≤1.5 b≤1/2W		4
	TOP GLASS	a<2.5 b<1/2T c<1/3W		5
GLASS PROTRUSION		a < 1/5 W	MINOR	6
RAINBOW		-	MINOR	-

UNLESS STATE OTHERWISE , ALL UNIT ARE IN MILLIMETER . DEFECT TABLE : B

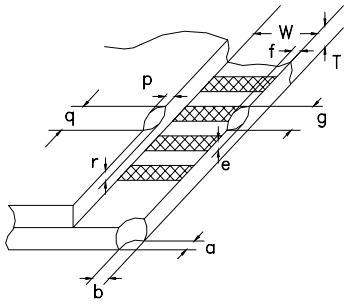


fig . 4

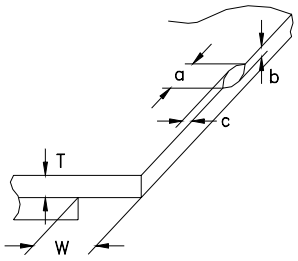


fig . 5

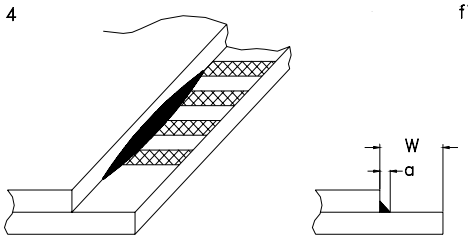


fig . 6

HANDLING PRECAUTIONS

(1) CAUTION OF LCD HANDLING & CLEANING

Use soft cloth with solvent (recommended below) to clean the display surface and wipe lightly.
- Isopropyl alcohol, ethyl alcohol, trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent;
-water, ketone, aromatics

(2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommend that any unused input terminal would be connected to V_{DD} or V_{SS}, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

Remove the protective film slowly and, if possible, under ESD control device like ion blower and humidity of working room should be kept over 50%RH to reduce risk of static charge.

(3) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed direct to sunshine or high temperature/humidity.

(4) CAUTION FOR OPERATION

It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. The use of direct current drive should be avoided because an electrochemical reaction due to direct current causes LCD's undesirable deterioration.

Response time will be extremely delayed at low temperature, and LCD's show dark color at high temperature. However those phenomena do not mean malfunction or out of order with LCD's.

Some font will be abnormally displayed when the display area is pushed hard during operation. But it resumes normal condition after turning off once.

(5) SOLDERING (for Pin type)

It is recommended to complete dip soldering at 270 ^{o}C or hand soldering at 280 ^{o}C within 3 seconds. The soldering position is at least 3mm apart from the pin head. Wave or reflow soldering are not recommended. Metal pins should not be soldered for more than 3 times and each soldering should be done after cool down of metal pins**.**

(6) SAFETY

For crash damaged or unnecessary LCD's, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.

When any liquid leaked out of a damaged glass cell comes in contact with your hands, wash it off with soap and water.

WARRANTY

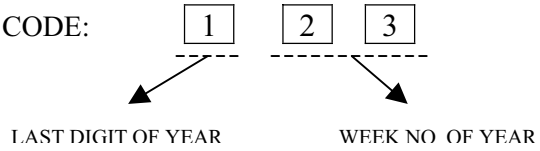
Multi-Inno will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of Multi-Inno is limited to repair and/or replacement. Multi-Inno will not be responsible for any subsequent or consequential event.

APPENDIX

LOT INDICATION OF LCD MODULE

CODING SYSTEM:

3-DIGIT COLOR CODE:



COLOR CODE:

	COLOR
0	BLACK
1	BROWN
2	RED
3	ORANGE
4	YELLOW
5	GREEN
6	BLUE
7	PURPLE
8	GREY
9	WHITE

LOCATION AS SHOWN BELOW: