MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI128128J-G

Revision	1.0
Engineering	
Date	
Our Reference	

REVISION RECORD

Date	Rev.No.	Page	Revision Items	Prepared
2008.4.15	**V1.0**		**The first release**	常伟

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1. General Specifications

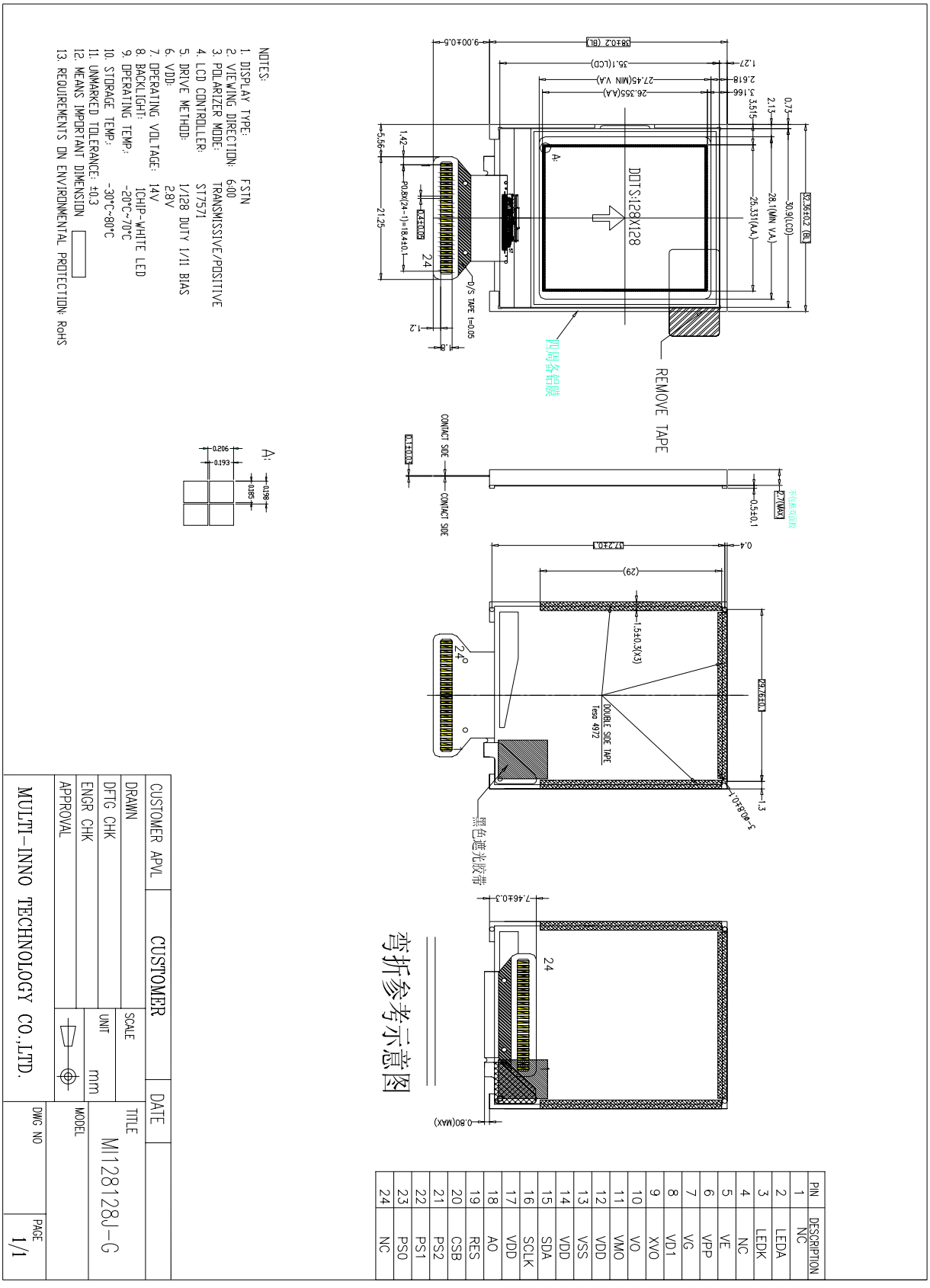
MI128128J-G is a STN active matrix LCD module i. It is composed of a mono STN-LCD panel, driver IC, FPC, a back light unit . The display area contains 128 x 128 pixels. This product accords with RoHS environmental criterion.

Item	Contents	Unit	Note
LCD Type	STN	-	
Display Color	B/W		
LCD Duty	1/128	-	
LCD Bias	1/9	-	
Viewing Direction	6:00	O'Clock	1
Active Area(W×H)	25.331×26.355	mm	
Number of Dots	128×128	mm	
Dot Pitch(W×H)	0.206X0.198	mm	
Controller	ST7571	-	
V_{DD}	2.8V	V	
Outline Dimensions	Refer to outline drawing on next page		
Backlight	1-LEDs (white)	-	
Weight	-	g	
Interface	3/4-line-SPI	-	
Polarizer Mode	Transmissive/Positive	-	

Notes:

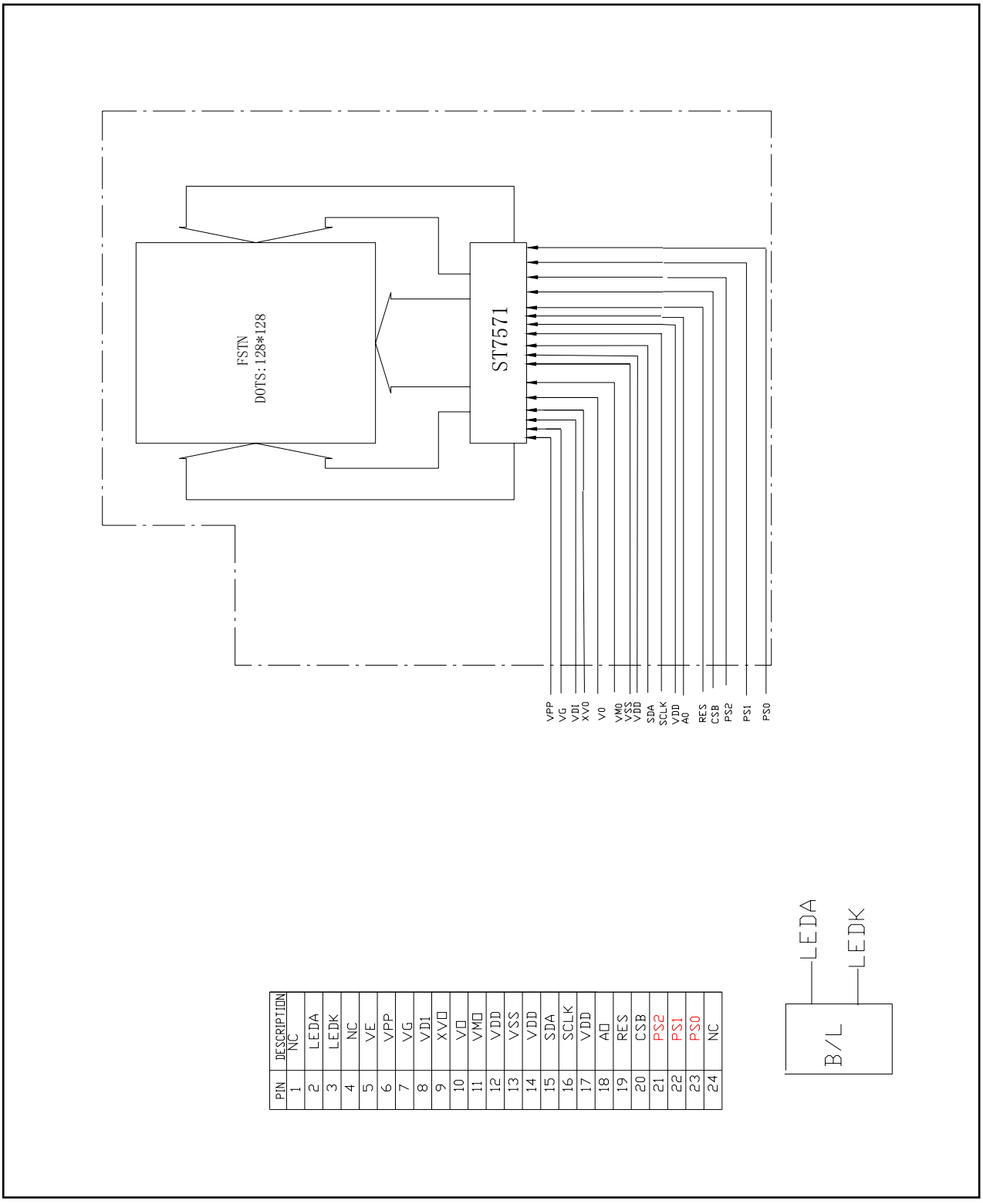
Generally the contrast is the best when viewing the display from the viewing direction.

2. Outline Drawing



PIN	DESCRIPTION
1	NC
2	LEDA
3	LEDK
4	NC
5	VE
6	VPP
7	VG
8	VD1
9	XVO
10	VO
11	VMO
12	VDD
13	VSS
14	VDD
15	SDA
16	SCLK
17	VDD
18	A0
19	RES
20	CSB
21	PS2
22	PS1
23	PS0
24	NC

3. Circuit Block Diagram



PIN	DESCRIPTION
1	NC
2	LEDA
3	LEDK
4	NC
5	VE
6	VPP
7	VG
8	VD1
9	XV□
10	V□
11	VM□
12	VDD
13	VSS
14	VDD
15	SDA
16	SCLK
17	VDD
18	A□
19	RES
20	CSB
21	PS2
22	PS1
23	PS0
24	NC

4. Absolute Maximum Ratings(Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	-0.3	2.8	V	1，2
Logic Signal Input /Output Voltage	V_{IOVCC}	-0.3	V_{DD}+0.3	V	
Power Supply Voltage for LCD	Vop	11.8	12.2	V	
Operating Temperature	Top	-20	+70	℃	
Storage Temperature	Tst	-30	+80	℃	

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.

2. V_{DD} >V_{SS} must be maintained.

5. Electrical Specifications and Instruction Code

5.1 Electrical characteristics(Vss=0V ,Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Operation voltage		V_{OP}	Ta=25℃	11.8	12	12.2	V	1
Input voltage	'H'	V_{IH}		$0.8V_{DD}$	-	V_{DD}	V	
	'L'	V_{IL}		Vss	-	$0.2V_{DD}$	V	
Output Voltage	'H'	V_{OH}	-	$0.8V_{DD}$	-	V_{DD}	V	
	'L'	V_{OL}	-	Vss	-	$0.2V_{DD}$	V	
Current Consumption		I_{CC1}	Normal mode	-	—	—	mA	1.2
		I_{CC2}	Standby mode	-	—	—	mA	3

Note:

1: IC default setting, Duty:1/128,Bias:1/9

2:Display full white. Backlight on state, the default voltage is 2.8V.

3: IC on standby mode.

5.2 LED backlight specification(Vss=0V ,Ta=25℃)

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Supply voltage		-	-	2.4	-	2.8	V	
Supply current		I_f	V_f=3.3V	-	15	-	mA	
Reverse voltage		V_r	-	-	-	-	V	
Forward current	Normal	I_{pn}	1-chip Serial		15	20	mA	
	Dimming	I_{pd}			2			
Reverse Current		I_r	-	-	-	-	μA	
Uniformity		△Bp	I_f=15mA	70%				
Color coordinate		X		-	-	-	-	
		Y		-	-	-	-	

5.3 Interface Signals

Pin No.	Symbol	I/O	Function
1	NC		NC
2	LEDA	I	Anode for LED backlighting
3	LEDK	I	Cathode for LED backlighting
4	NC		NC
5	VE	I	NC
6	VPP	I	NC
7	VG	O	Connect a capacitor to vss
8	VD1	O	Connect a capacitor to vss
9	XVO	O	Connect a capacitor to vo
10	V0	O	Connect a capacitor to xvo
11	VMO	O	Connect a capacitor to vss
12	VDD	P	Power Supply
13	VSS	P	Ground
14	VDD	P	Power Supply
15	SDA	I/O	Serial data
16	SCLK	I/O	Serial clock
17	VDD	P	Power Supply
18	A0	I	Register select signal
19	RES	I	Reset pin
20	CSB	I	Chip select signal
21	PS2	I	Parallel/Serial data input select
22	PS1	I	
23	PS0	I	
24	NC	I	NC

5.4 Interface Timing Chart

Note: Please refer to Sitronix's ST7571data sheet for more details.

Sitronix's ST7571 INTERFACE PROTOCOL

Inter 4-SPI system CPU interface

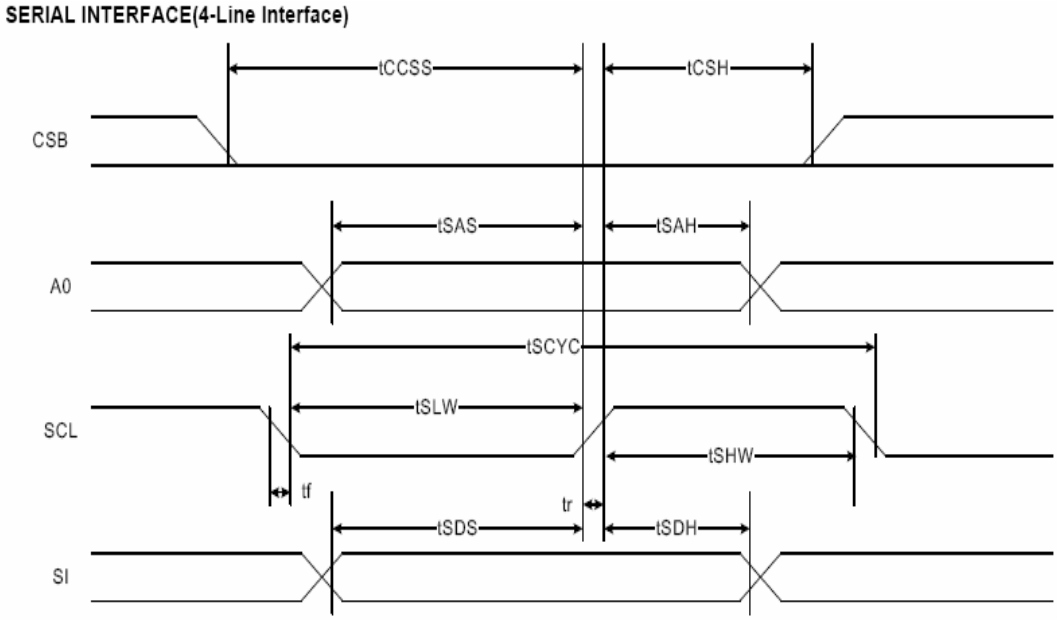


Fig. 33

(VDD1=1.8V~3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

Inter 3-SPI system CPU interface

SERIAL INTERFACE(3-Line Interface)

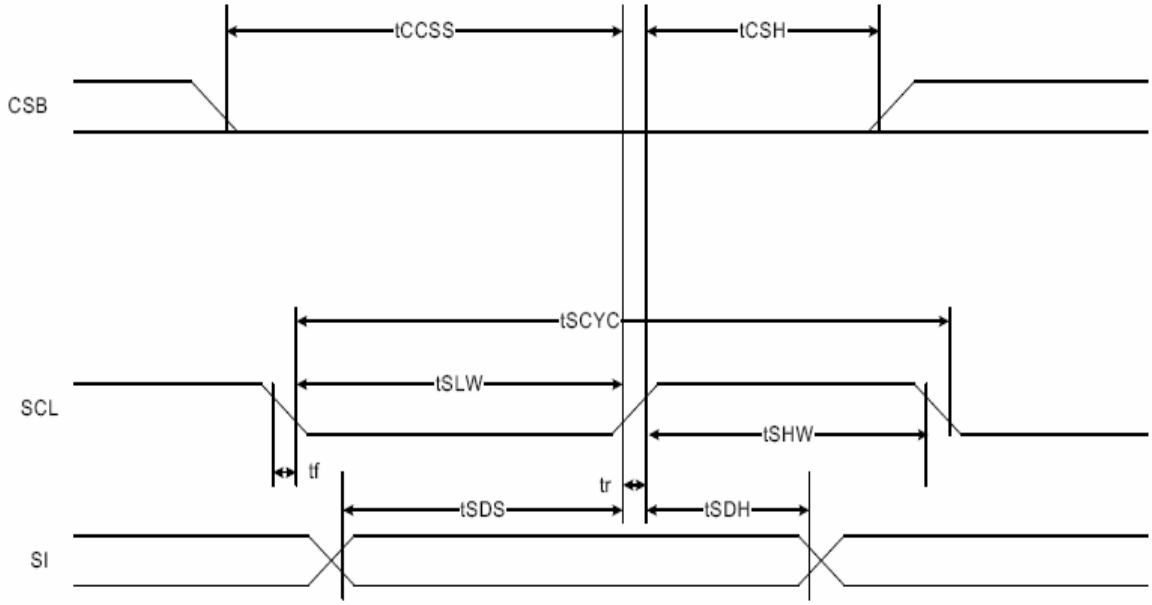


Fig. 34

(VDD1=1.8V~3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

INSTRUCTION DESCRIPTION(Sitronix's ST7571)

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	
Mode Set	0	0	0	0	1	1	1	0	0	0	2-byte instruction to set Mode and FR(Frame frequency control) BE(Booster efficiency control)	9.1.1
	0	0	FR3	FR2	FR1	FR0	BE1	BE0	x'	0		
Write display data	1	0	Write data								Write data into DDRAM	9.1.2
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable(default) ICON=1: ICON enable & set the page address to 16	9.1.3
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address	9.1.4
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB	9.1.5
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB	9.1.6
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON	9.1.7
Set initial display line register	0	0	0	1	0	0	0	0	x'	x'	2-byte instruction to specify the initial display line to realize vertical scrolling	9.1.8
	0	0	x'	S6	S5	S4	S3	S2	S1	S0		
Set initial COM0 register	0	0	0	1	0	0	0	1	x'	x'	2-byte instruction to specify the initial COM0 to realize window scrolling	9.1.9
	0	0	x'	C6	C5	C4	C3	C2	C1	C0		
Set partial display duty ration	0	0	0	1	0	0	1	0	x'	x'	2-byte instruction to set partial display duty ratio	9.1.10
	0	0	D7	D6	D5	D4	D3	D2	D1	D0		
Set N-line inversion	0	0	0	1	0	0	1	1	x'	x'	2-byte instruction to set N-line inversion register	9.1.11
	0	0	x'	x'	x'	N4	N3	N2	N1	N0		
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode	9.1.12
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1: reverse display	9.1.13
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display EON=1: entire display ON	9.1.14

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation	9.1.15
Select regulator register	0	0	0	0	1	0	0	R2	R1	R0	Select the internal resistance ratio of the regulator resistor	9.1.16
Select electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the reference voltage	9.1.17
	0	0	x'	x'	EV5	EV4	EV3	EV2	EV1	EV0		
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias	9.1.18
SHL select	0	0	1	1	0	0	SHL	x'	x'	x'	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction	9.1.19
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0: normal direction ADC=1: reverse direction	9.1.20
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator	9.1.21
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode	9.1.22
Release power save mode	0	0	1	1	1	0	0	0	0	1	release power save mode	9.1.23
Reset	0	0	1	1	1	0	0	0	1	0	initial the internal function	9.1.24
Display data length	x'	x'	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI mode)	9.1.25
	x'	x'	D7	D6	D5	D4	D3	D2	D1	D0		
NOP	0	0	1	1	1	0	0	0	1	1	No operation	9.1.26
Test Command set 1	0	0	1	1	1	1	x'	x'	x'	x'	Enter test command set 1 Use for Burning EE	9.1.27
Test Command set 2	0	0	1	1	0	1	0	0	0	1	Enter test command set 2 Use for Burning EE	9.1.28
Test Command set 3	0	0	0	1	1	1	1	0	1	1	Don't use this instruction	9.1.29

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
COMMAND SET 1											
Disable autoread	0	0	1	0	1	0	1	0	1	0	Disable autoread
Enter EEPROM mode	0	0	0	0	0	1	0	0	1	1	Enter EEPROM mode
Enable read mode	0	0	0	0	1	0	0	0	0	0	Enable read mode
Set read pulse	0	0	0	1	1	1	0	0	0	1	Set read pulse width (Do not modify this value)
Exit EEPROM mode	0	0	1	0	0	0	0	0	1	1	Exit EEPROM mode
Enable erase mode	0	0	0	1	0	0	1	0	1	0	Enable erase mode
Set erase pulse	0	0	0	1	0	1	0	1	0	1	Set erase pulse width (Do not modify this value)
Enable write mode	0	0	0	0	1	1	0	1	0	1	Enable write mode
Set write pulse	0	0	0	1	1	0	1	0	1	0	Set write pulse width (Do not modify this value)
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
COMMAND SET 2											
Increase vop offset	0	0	0	1	0	1	0	0	0	1	Increase vop offset 1 level
Decrease vop offset	0	0	0	1	0	1	0	0	1	0	Decrease vop offset 1 level
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode

6. Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp	θ=0° Φ=0°	-	-	-	Cd/m^2	1
Uniformity	△Bp		70%	-	-		1,2
Viewing Angle	θ1 (Φ=90° or270°)	Cr≥10	-30～+20			Deg	3
	θ2 (Φ=0° or 180°)		-30～+20				
Contrast Ratio	Cr	θ=0° Φ=0°		3.0		-	4
Response Time	t_{on}		-	-	300	ms	5
	t_{off}		-	-	300	ms	

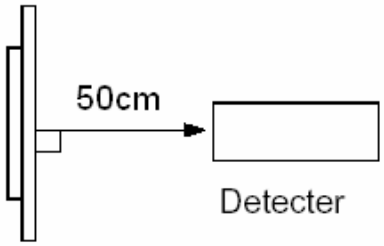
Note：The parameter is slightly changed by temperature, driving voltage and materiel.

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

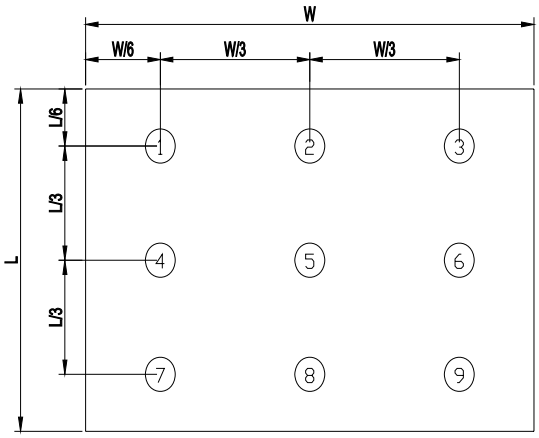


Note 2: The luminance uniformity is calculated by using following formula.

△Bp = Bp (Min.) / Bp (Max.)×100 (%)

Bp (Max.) = Maximum brightness in 9 measured spots

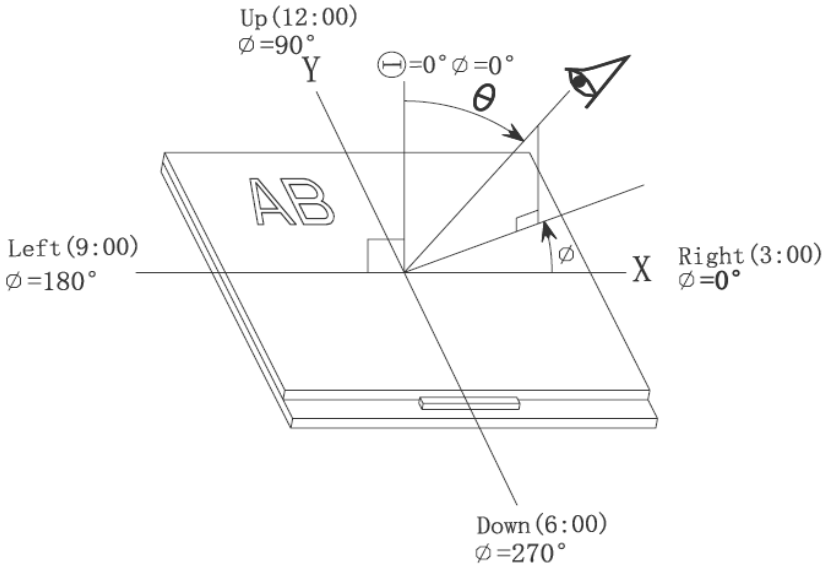
Bp (Min.) = Minimum brightness in 9 measured spots.



Measurement equipment PR-705 (Φ8mm)

Note 3: The definition of viewing angle:

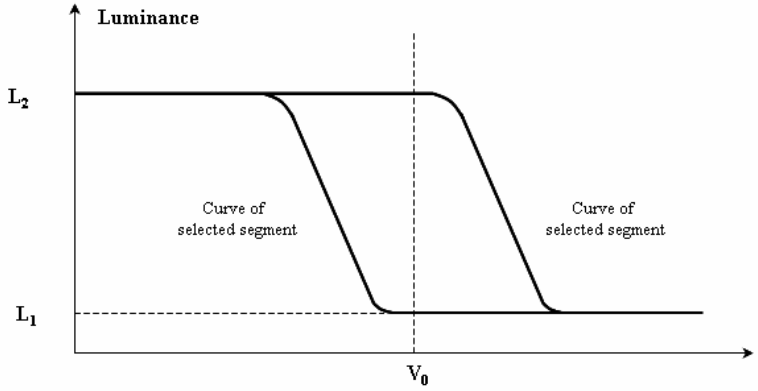
Refer to the graph below marked by *θ* and *Φ*



Note 4: The definition of contrast ratio (Test LCM using PR-705):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at “White” state}}{\text{Luminance When LCD is at “Black” state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

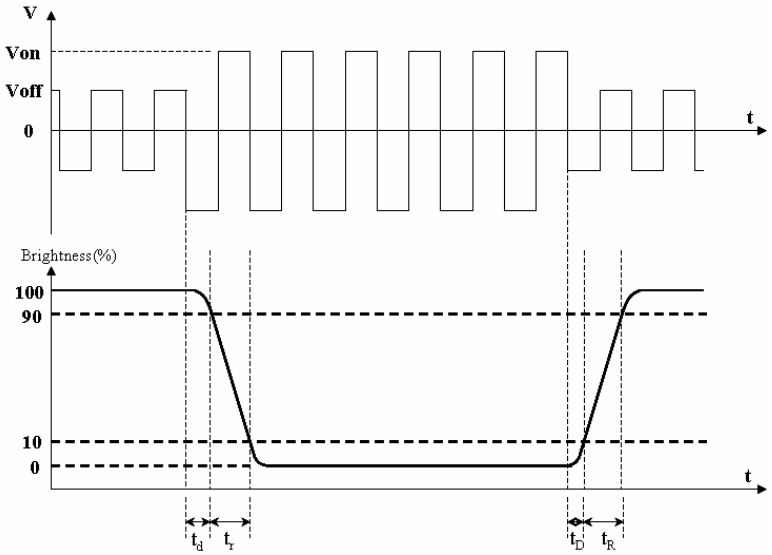


Electro-optical characteristic (EOC) graph (positive type)

Note 5: Definition of Response time. (Test LCD using DMS501):

Turn on time (rise time): $t_{on} = t_d + t_r$ (from non-selected state to selected state)
Turn off time (fall time): $t_{off} = t_D + t_R$ (from selected state to non-selected state)

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



The definition of response time

7. Reliability Test Items and Criteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	80℃±2℃ 96H Restore 2H at 25℃ Power off	After testing, cosmetic and electrical defects should not happen.
2	Low Temperature Storage	-30℃±2℃ 96H Restore 2H at 25℃ Power off	
3	High Temperature Operation	70℃±2℃ 96H Restore 2H at 25℃ Power on	
4	Low Temperature Operation	-20℃±2℃ 96H Restore 4H at 25℃ Power on	
5	High Temperature & Humidity Operation	60℃±2℃ 90%RH 96H Power on	
6	Temperature Cycle	−30℃←→25℃←→80℃ 30min 5min 30min after 10cycle, Restore 2H at 25℃ Power off	
7	Vibration Test	10Hz~150Hz, 100m/s^2, 120min	
8	Shock Test	Half-sine wave,300m/s^2,11ms	
9	Drop Test(package state)	800mm, concrete floor,1corner, 3edges, 6 sides each time	1.After testing, cosmetic and electrical defects should not happen. 2.the product should remain at initial place 3.Product uncovered or package broken is not permitted.

Note:Additional test Item proposed by customer shall be determined by mutual agreement between customer and Tianma

8 Quality level

8.1 Classification of defects

Major defects (MA): A major defect refers to a defect that may substantially degrade usability for product applications, including all functional defects(such as no display, abnormal display, open or missing segment, short circuit, missing component), outline dimension beyond the drawing, progressive defects and those affecting reliability.

Minor defects (MI): A minor defect refers to a defect which is not considered to be able to substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation, such as black spot, white spot, bright spot, pinhole, black line, white line, contrast variation, glass defect, polarizer defect, etc.

8.2 Definition of inspection range

For dot defect of STN LCD which is not smaller than 3 inches, dividing three areas to make a judgment (according to figure 1).

A area : center of viewing area

B area : periphery of viewing area

C area : Outside viewing area

For other defects, dividing two areas to make a judgment (according figure 2).

A zone : Inside Viewing area

B zone : Outside Viewing area

X1(A.A~V.A):1.4mm X2(A.A~V.A): 1.4mm

Y1(A.A~V.A): 0.5mm Y2(A.A~V.A): 0.5mm

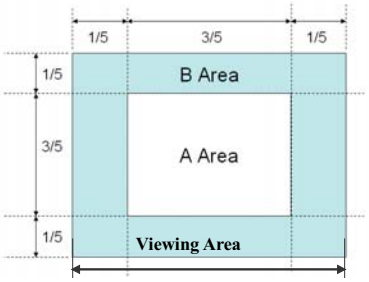


Figure 1

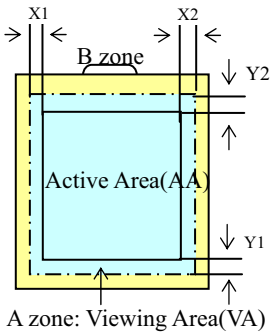


Figure 2

8.3 Inspection items and general notes

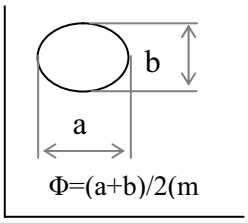
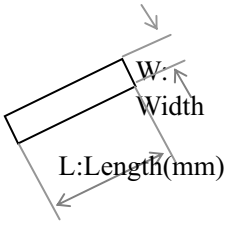
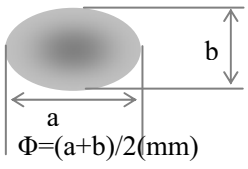
General notes	①Should any defects which are not specified in this standard happen, additional standard shall be determined by mutual agreement between customer and TIANMA. ②Viewing area should be the area which TIANMA guarantees. ③Limit sample should be prior to this Inspection standard. ④Viewing judgment should be under static pattern. ⑤Inspection conditions Inspection distance: 250 mm (from the sample) Temperature : 25±5 ºC Inspection angle : 45 degrees in 6 o′clock direction (all defects in viewing area should be inspected from this direction)	
Inspection items	Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble	The color of a small area is different from the remainder. The phenomenon doesn't change with voltage
	Contrast variation	The color of a small area is different from the remainder. The phenomenon changes with voltage
	Polarizer defect	Scratch, Dirt, Particle, Bubble on polarizer or between polarizer and glass
	Dot defect (STN LCD)	The pixel appears bright or dark abnormally when display

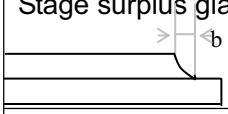
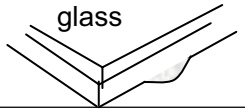
	Functional defect	No display, Abnormal display, Open or missing segment, Short circuit, False viewing direction
	Glass defect	Glass crack, Shaved corner of glass, Surplus glass
	PCB defect	Components assembly defect

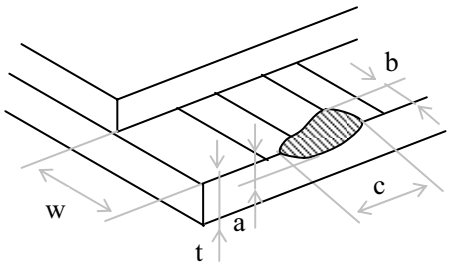
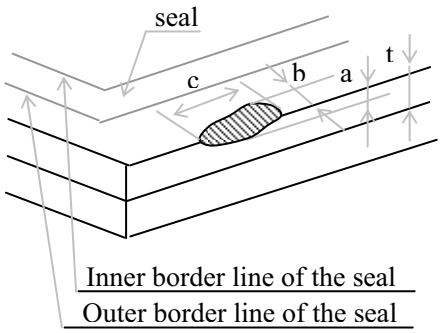
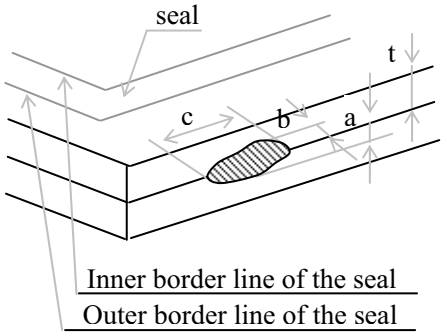
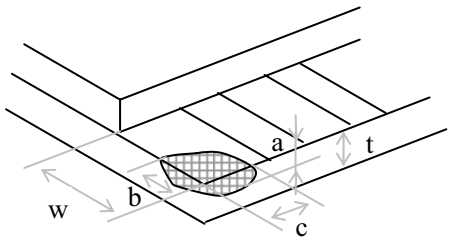
8.4 Outgoing Inspection level

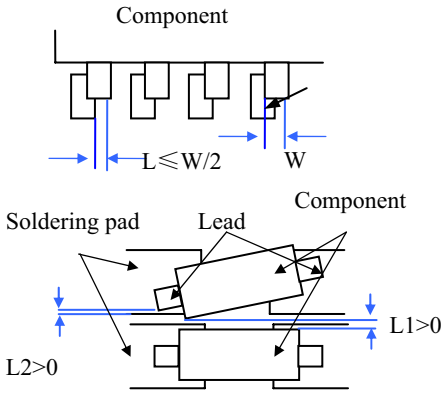
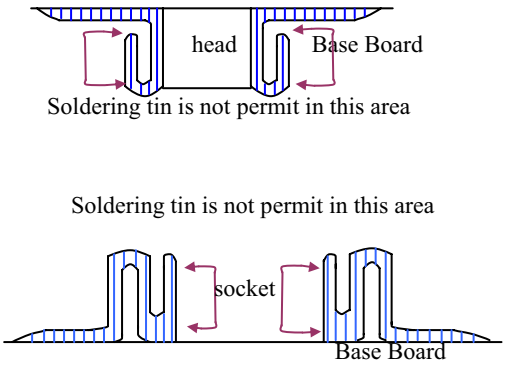
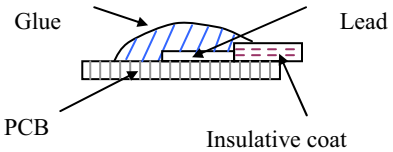
Outgoing Inspection standard	Inspection conditions	Inspection				
		Min.	Max.	Unit	IL	AQL
Major Defects	See 8.3 general notes	See 8.5			II	0.65
Minor Defects	See 8.3 general notes	See 8.5			II	1.5
Note：Sampling standard conforms to GB2828						

8.5 Inspection Items and Criteria

Inspection items			Judgment standard			
			Category		Acceptable number	
					A zone	B zone
1	Black spot, White spot, Bright Spot, Pinhole, Foreign Particle, Particle in or on glass, Scratch on glass		A	Φ≦0.10	Neglected	Neglected
			B	0.10<Φ≦0.15	2	
			C	0.15<Φ≦0.20	1	
			D	0.20<Φ	0	
			Total defective point(B,C)		3	
2	Black line, White line, and Particle Between Polarizer and glass, Scratch on glass		A	W≦0.01	Neglected	Neglected
			B	0.01<W≦0.03 L≦3.0	2	
			C	0.03<W≦0.05 L≦3.0	1	
			D	0.05<W	0	
			Total defective point(B,C)		3	
3	Contrast variation		A	Φ≦0.2	Neglected	Neglected
			B	0.2<Φ≦0.3	2	
			C	0.3<Φ≦0.4	1	
			D	0.4<Φ	0	
			Total defective point(B,C)		3	

<table>
<tr><td rowspan="11">4</td><td rowspan="11">Dot defect (if STN LCD is used)</td><td rowspan="5">STN LCD is smaller than 3 inches</td><td>LCD Class</td><td>Defect</td><td colspan="2">A area</td><td>B area</td></tr>
<tr><td rowspan="3">A</td><td>Bright dot</td><td colspan="2">1</td><td rowspan="5">Neglected</td></tr>
<tr><td>Dark dot</td><td colspan="2">2</td></tr>
<tr><td>Total</td><td colspan="2">2</td></tr>
<tr><td rowspan="3">B</td><td>Bright dot</td><td colspan="2">2</td></tr>
<tr><td>Dark dot</td><td colspan="2">3</td></tr>
<tr><td>Total</td><td colspan="2">4</td></tr>
<tr><td rowspan="5">STN LCD between 3~10.4 inches</td><td>LCD Class</td><td>Defect</td><td>A area</td><td>B area</td><td>C area</td></tr>
<tr><td rowspan="3">A</td><td>Bright dot</td><td>1</td><td>1</td><td rowspan="5">Neglected</td></tr>
<tr><td>Dark dot</td><td>1</td><td>2</td></tr>
<tr><td>Total</td><td colspan="2">4</td></tr>
<tr><td rowspan="3">B</td><td>Bright dot</td><td>2</td><td>2</td></tr>
<tr><td>Dark dot</td><td>2</td><td>3</td></tr>
<tr><td>Total</td><td colspan="2">6</td></tr>
<tr><td colspan="6">Notes:
Bright dot: in R、G、B or dark display figure, the pixel appears bright.
Dark dot: in R、G、B or white display figure, the pixel appears dark.
Defect area must be less than an half size of the dot.</td></tr>
<tr><td>5</td><td colspan="2">Bubble inside cell</td><td colspan="2">any size</td><td>none</td><td>none</td></tr>
<tr><td rowspan="4">6</td><td rowspan="4">Polarizer defect (if Polarizer is used)</td><td colspan="5">Scratch ,damage on polarizer, Particle on polarizer or between polarizer and glass.
Refer to item 1 and item 2.</td></tr>
<tr><td rowspan="3">Bubble, dent and convex</td><td>A</td><td>Φ≦0.3</td><td>Neglected</td><td rowspan="3">Neglected</td></tr>
<tr><td>B</td><td>0.3<Φ≦0.7</td><td>2</td></tr>
<tr><td>C</td><td>0.7<Φ</td><td>0</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">Surplus glass</td><td>Stage surplus glass
  </td><td colspan="4">b≦0.3mm</td></tr>
<tr><td>Surrounding surplus glass
  </td><td colspan="4">Should not influence outline dimension and assembling.</td></tr>
<tr><td>8</td><td colspan="2">Open segment or open common</td><td colspan="4">Not permitted</td></tr>
<tr><td>9</td><td colspan="2">Short circuit</td><td colspan="4">Not permitted</td></tr>
<tr><td>10</td><td colspan="2">False viewing direction</td><td colspan="4">Not permitted</td></tr>
<tr><td>11</td><td colspan="2">Contrast ratio uneven</td><td colspan="4">According to the limit specimen</td></tr>
<tr><td>12</td><td colspan="2">Crosstalk</td><td colspan="4">According to the limit specimen</td></tr>
<tr><td>13</td><td colspan="2">Black /White spot(display)</td><td colspan="4">Refer to item 1</td></tr>
<tr><td>14</td><td colspan="2">Black /White line(display)</td><td colspan="4">Refer to item 2</td></tr>
</table>

<table>
<tr><th colspan="3" rowspan="2">Inspection items</th><th colspan="2">Judgment standard</th><th rowspan="2">Acceptable number</th></tr>
<tr><th colspan="2">Category(application: B zone)</th></tr>
<tr><td rowspan="6">15</td><td rowspan="6">Glass defect crack</td><td rowspan="2">①The front of lead terminals
 
</td><td>A</td><td>a≤ t, b≤1/5W, c≤3mm</td><td rowspan="6">Max.3 defects allowed</td></tr>
<tr><td>B</td><td>Crack at two sides of lead terminals should not cover patterns and alignment mark</td></tr>
<tr><td>②Surrounding crack—non-contact side
 
</td><td colspan="2">b < Inner borderline of the seal</td></tr>
<tr><td>③ Surrounding crack— contact side
 
</td><td colspan="2">b < Outer borderline of the seal</td></tr>
<tr><td rowspan="2">④Corner
 
</td><td>A</td><td>a ≦ t, b ≦ 3.0, c ≦ 3.0</td></tr>
<tr><td>B</td><td>Glass crack should not cover patterns u and alignment mark and patterns.</td></tr>
</table>

Inspection items			Judgment standard Category(application: B zone)
16	PCB defect	Component soldering: No cold soldering、short、open circuit、burr、tin ball The flat encapsulation component position deviation must be less than 1/3 width of the pin (Pic.1)； the sheet component deviation: Pin deviates from the pad and contact with the near components is not permitted（Pic.2）	
		lead defect: The lead lack must be less than 1/3 of its width; The lead burr must be less than 1/3 of the seam; Impurities connect with the near leads is not permitted	
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted	
		Glue on root of the speaker receiver and motor lead: The insulative coat of the lead must join into the PCB; the protected glue must envelop to the insulative coat.	

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol

— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water

— Ketone

— Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct

assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.