TR7707

320 x240 dot Graphics Mono up to16 grayscale STN-LCD Driver/Controller

INTRODUCTION

The TR7707 is a single chip, 16-grayscale/Mono STN-LCD driver with controller for dot-matrix STN-LCD panel.

The TR7707 has 320 Segment outputs and 240 Common outputs, It can drives up to 320x240-dots STN-LCD panel.

The TR7707 provides 80/68-series 8/16-bit high-speed bus interface and 4-line Serial interface embedded bit-mapped display RAM, oscillator circuit and power circuit, so that it can minimize system's hardware effort with fewer components.

The TR7707 provides abundant commands for LCD display access, except the basic display functions.

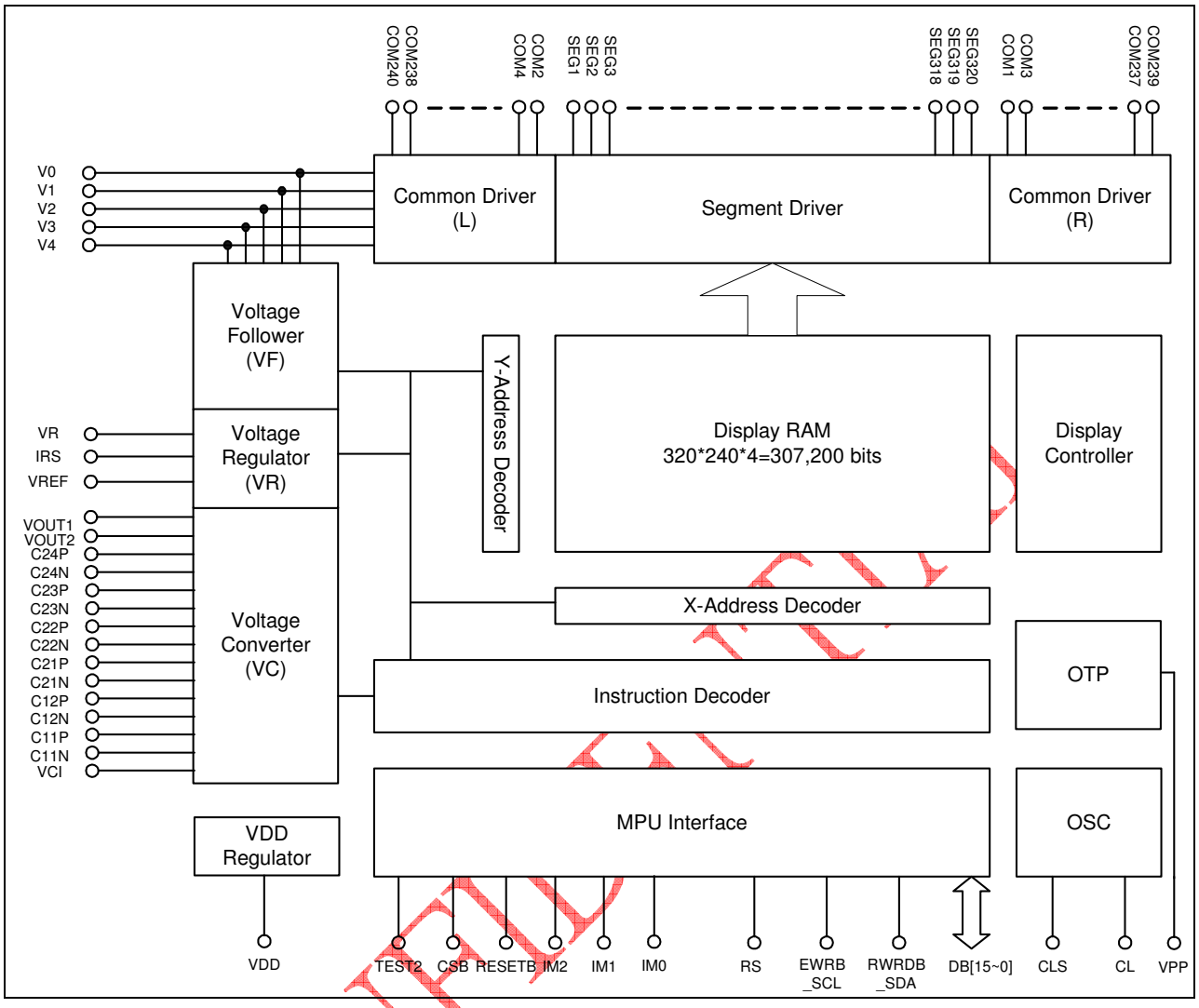
The TR7707 is especially designed for low power consumption application. It also provides Standby and Sleep mode allows for precise power saving control.

FEATURES

- **LCD Drive Output**
  - Segment outputs : 320 outputs
  - Common outputs : 240 outputs
- **Display Function**
  - Display RAM size : 320*240*4 Bits
  - Gray scale level : 16 level
  - Duty ratios : 1/128, 1/160, 1/240
- **Power Circuit**
  - Supply Power(VCC) : 2.4V ~ 3.3V
  - LCD drive voltage : 28V (max)
  - Boost circuit (step1) : x2
    (step2) : x2, x3, x4, x5
  - Temp. coefficient : 0.00%/℃, -0.05%/℃, -010%/℃,-015%/℃
  - Contrast adjust : 256 steps
  - Bias ratio : 1/9 ~ 1/16
  - Voltage follower : Generates V0 ~V4, based on the amplified internal reference voltage
- **Microprocessor Interface**
  - Parallel 68/80-series bi-directional 8/16 bit interface
  - 4-line serial interface
  - Min. Write cycle : 350 ns
  - Min Read cycle : 500 ns
- **Chip Outline**
  - Package : COG
  - Pad pitch (min) : 33um.

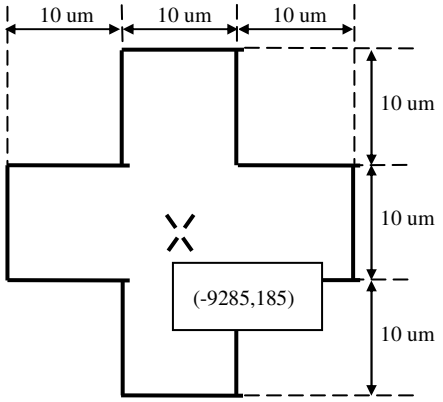
  Pad spacing (min) : 15um.
- **Oscillator Circuit**
  - On-chip RC oscillation circuit
- **LCD Drive Circuit**
  - Left-Right-interlaced COM disposition
  - Support vertical scroll display
- **Command Set**
  - Display data write/read
  - Addressing window auto-increment
  - Set display starting line
  - Set polarity alternated cycles
  - COM shift direction
  - SEG shift direction
  - Reverse display
  - Power saving mode
  - Internal register status read
- **Other**
  - OTP available for Contrast adjustment

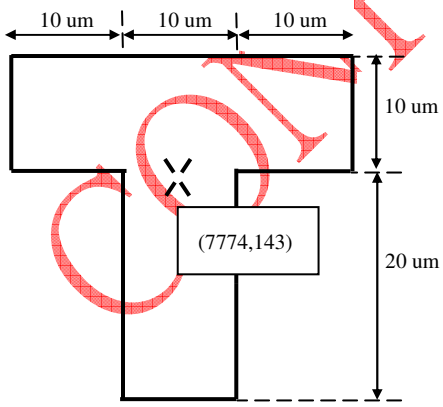
BLOCK DIAGRAM



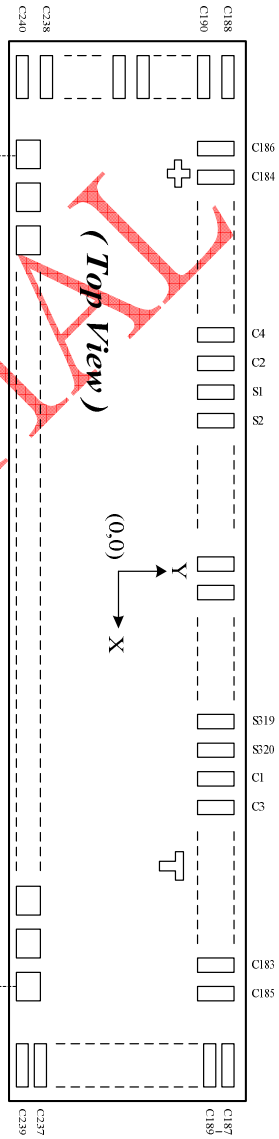
PAD ARRANGEMENT

Chip Size	19751 (X) * 1010.5 (Y) um^2
Chip Thickness	400 um
Pad Coordinate	Pad Centers
Coordinate origin	Chip center
Bump High	15 um
Au Bump Size	
(1) 80 * 40 um^2	Pad 1 ~ 188
(2) 89 * 18 um^2	Pad 189 ~ 215, 722 ~ 748
(3) 23 * 71 um^2	Pad 216 ~ 721
Alignment Mark	





PIN NO.	PIN NAME
1	DUMMY
2	DUMMY
3	DUMMY
4	TEST2
5	TEST1
6	DMYGND
7	DB15
8	DB14
9	DB13
10	DB12
11	DB11
12	DB10
13	DB9
14	DB8
15	DB7
16	DB6
17	DB5
18	DB4
19	DB3
20	DB2
21	DB1
22	DB0
23~42	GND (x20)
43	VREF
44	CLS
45	CE
46	IRS
47	VPP
48~63	VCC(x16)
64~67	VDD(x4)
68	DMYGND
69	CSB
70	IM2
71	IM1
72	IM0
73	EWRB_SCL
74	RESETB
75	RS
76	RWRDB_SDA
77	DMYVCC
78	REGON
79~96	VCI (x18)
97~100	C11P (x4)
101~104	C11M (x4)
105~108	C12P (x4)
109~112	C12M (x4)
113~122	VOUT1 (x10)
123	VR
124~127	C21P (x4)
128~131	C21M (x4)
132~135	C22P (x4)
136~139	C22M (x4)
140~143	C23P (x4)
144~147	C23M (x4)
148~151	C24P (x4)
152~155	C24M (x4)
156~165	VOUT2 (x10)
166~169	V0 (x4)
170~173	V1 (x4)
174~177	V2 (x4)
178~181	V3 (x4)
182~185	V4 (x4)
186	DUMMY
187	DUMMY
188	DUMMY



PAD COORDINATE

No	Name	X	Y	No	Name	X	Y
1	DUMMY	-9537.01	-418.00	51	VCC	-4437.01	-418.00
2	DUMMY	-9435.01	-418.00	52	VCC	-4335.01	-418.00
3	DUMMY	-9333.01	-418.00	53	VCC	-4233.01	-418.00
4	TEST2	-9231.01	-418.00	54	VCC	-4131.01	-418.00
5	TEST1	-9129.01	-418.00	55	VCC	-4029.01	-418.00
6	DMYGND	-9027.01	-418.00	56	VCC	-3927.01	-418.00
7	DB<15>	-8925.01	-418.00	57	VCC	-3825.01	-418.00
8	DB<14>	-8823.01	-418.00	58	VCC	-3723.01	-418.00
9	DB<13>	-8721.01	-418.00	59	VCC	-3621.01	-418.00
10	DB<12>	-8619.01	-418.00	60	VCC	-3519.01	-418.00
11	DB<11>	-8517.01	-418.00	61	VCC	-3417.01	-418.00
12	DB<10>	-8415.01	-418.00	62	VCC	-3315.01	-418.00
13	DB<9>	-8313.01	-418.00	63	VCC	-3213.01	-418.00
14	DB<8>	-8211.01	-418.00	64	VDD	-3111.01	-418.00
15	DB<7>	-8109.01	-418.00	65	VDD	-3009.01	-418.00
16	DB<6>	-8007.01	-418.00	66	VDD	-2907.01	-418.00
17	DB<5>	-7905.01	-418.00	67	VDD	-2805.01	-418.00
18	DB<4>	-7803.01	-418.00	68	DMYGND	-2703.01	-418.00
19	DB<3>	-7701.01	-418.00	69	CSB	-2601.01	-418.00
20	DB<2>	-7599.01	-418.00	70	IM2	-2499.01	-418.00
21	DB<1>	-7497.01	-418.00	71	IM1	-2397.01	-418.00
22	DB<0>	-7395.01	-418.00	72	IM0	-2295.01	-418.00
23	GND	-7293.01	-418.00	73	EWRB_SCL	-2193.01	-418.00
24	GND	-7191.01	-418.00	74	RESETB	-2091.01	-418.00
25	GND	-7089.01	-418.00	75	RS	-1989.01	-418.00
26	GND	-6987.01	-418.00	76	RWRDB_SDA	-1887.01	-418.00
27	GND	-6885.01	-418.00	77	DMYVCC	-1785.01	-418.00
28	GND	-6783.01	-418.00	78	REGON	-1683.01	-418.00
29	GND	-6681.01	-418.00	79	VCI	-1581.01	-418.00
30	GND	-6579.01	-418.00	80	VCI	-1479.01	-418.00
31	GND	-6477.01	-418.00	81	VCI	-1377.01	-418.00
32	GND	-6375.01	-418.00	82	VCI	-1275.01	-418.00
33	GND	-6273.01	-418.00	83	VCI	-1173.01	-418.00
34	GND	-6171.01	-418.00	84	VCI	-1071.01	-418.00
35	GND	-6069.01	-418.00	85	VCI	-969.01	-418.00
36	GND	-5967.01	-418.00	86	VCI	-867.01	-418.00
37	GND	-5865.01	-418.00	87	VCI	-765.01	-418.00
38	GND	-5763.01	-418.00	88	VCI	-663.01	-418.00
39	GND	-5661.01	-418.00	89	VCI	-561.01	-418.00
40	GND	-5559.01	-418.00	90	VCI	-459.01	-418.00
41	GND	-5457.01	-418.00	91	VCI	-357.01	-418.00
42	GND	-5355.01	-418.00	92	VCI	-255.01	-418.00
43	VREF	-5253.01	-418.00	93	VCI	-153.01	-418.00
44	CLS	-5151.01	-418.00	94	VCI	-51.01	-418.00
45	CL	-5049.01	-418.00	95	VCI	50.99	-418.00
46	IRS	-4947.01	-418.00	96	VCI	152.99	-418.00
47	VPP	-4845.01	-418.00	97	C11P	254.99	-418.00
48	VCC	-4743.01	-418.00	98	C11P	356.99	-418.00
49	VCC	-4641.01	-418.00	99	C11P	458.99	-418.00
50	VCC	-4539.01	-418.00	100	C11P	560.99	-418.00

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102	C11M	764.99	-418.00	152	C24M	5864.99	-418.00
103	C11M	866.99	-418.00	153	C24M	5966.99	-418.00
104	C11M	968.99	-418.00	154	C24M	6068.99	-418.00
105	C12P	1070.99	-418.00	155	C24M	6170.99	-418.00
106	C12P	1172.99	-418.00	156	VOUT2	6272.99	-418.00
107	C12P	1274.99	-418.00	157	VOUT2	6374.99	-418.00
108	C12P	1376.99	-418.00	158	VOUT2	6476.99	-418.00
109	C12M	1478.99	-418.00	159	VOUT2	6578.99	-418.00
110	C12M	1580.99	-418.00	160	VOUT2	6680.99	-418.00
111	C12M	1682.99	-418.00	161	VOUT2	6782.99	-418.00
112	C12M	1784.99	-418.00	162	VOUT2	6884.99	-418.00
113	VOUT1	1886.99	-418.00	163	VOUT2	6986.99	-418.00
114	VOUT1	1988.99	-418.00	164	VOUT2	7088.99	-418.00
115	VOUT1	2090.99	-418.00	165	VOUT2	7190.99	-418.00
116	VOUT1	2192.99	-418.00	166	V0	7292.99	-418.00
117	VOUT1	2294.99	-418.00	167	V0	7394.99	-418.00
118	VOUT1	2396.99	-418.00	168	V0	7496.99	-418.00
119	VOUT1	2498.99	-418.00	169	V0	7598.99	-418.00
120	VOUT1	2600.99	-418.00	170	V1	7700.99	-418.00
121	VOUT1	2702.99	-418.00	171	V1	7802.99	-418.00
122	VOUT1	2804.99	-418.00	172	V1	7904.99	-418.00
123	VR	2906.99	-418.00	173	V1	8006.99	-418.00
124	C21P	3008.99	-418.00	174	V2	8108.99	-418.00
125	C21P	3110.99	-418.00	175	V2	8210.99	-418.00
126	C21P	3212.99	-418.00	176	V2	8312.99	-418.00
127	C21P	3314.99	-418.00	177	V2	8414.99	-418.00
128	C21M	3416.99	-418.00	178	V3	8516.99	-418.00
129	C21M	3518.99	-418.00	179	V3	8618.99	-418.00
130	C21M	3620.99	-418.00	180	V3	8720.99	-418.00
131	C21M	3722.99	-418.00	181	V3	8822.99	-418.00
132	C22P	3824.99	-418.00	182	V4	8924.99	-418.00
133	C22P	3926.99	-418.00	183	V4	9026.99	-418.00
134	C22P	4028.99	-418.00	184	V4	9128.99	-418.00
135	C22P	4130.99	-418.00	185	V4	9230.99	-418.00
136	C22M	4232.99	-418.00	186	DUMMY	9332.99	-418.00
137	C22M	4334.99	-418.00	187	DUMMY	9434.99	-418.00
138	C22M	4436.99	-418.00	188	DUMMY	9536.99	-418.00
139	C22M	4538.99	-418.00	189	COM<239>	9762.00	-429.00
140	C23P	4640.99	-418.00	190	COM<237>	9762.00	-396.00
141	C23P	4742.99	-418.00	191	COM<235>	9762.00	-363.00
142	C23P	4844.99	-418.00	192	COM<233>	9762.00	-330.00
143	C23P	4946.99	-418.00	193	COM<231>	9762.00	-297.00
144	C23M	5048.99	-418.00	194	COM<229>	9762.00	-264.00
145	C23M	5150.99	-418.00	195	COM<227>	9762.00	-231.00
146	C23M	5252.99	-418.00	196	COM<225>	9762.00	-198.00
147	C23M	5354.99	-418.00	197	COM<223>	9762.00	-165.00
148	C24P	5456.99	-418.00	198	COM<221>	9762.00	-132.00
149	C24P	5558.99	-418.00	199	COM<219>	9762.00	-99.00
150	C24P	5660.99	-418.00	200	COM<217>	9762.00	-66.00

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201	COM<215>	9762.00	-33.00	251	COM<115>	8265.00	402.50
202	COM<213>	9762.00	0.00	252	COM<113>	8227.00	402.50
203	COM<211>	9762.00	33.00	253	COM<111>	8189.00	402.50
204	COM<209>	9762.00	66.00	254	COM<109>	8151.00	402.50
205	COM<207>	9762.00	99.00	255	COM<107>	8113.00	402.50
206	COM<205>	9762.00	132.00	256	COM<105>	8075.00	402.50
207	COM<203>	9762.00	165.00	257	COM<103>	8037.00	402.50
208	COM<201>	9762.00	198.00	258	COM<101>	7999.00	402.50
209	COM<199>	9762.00	231.00	259	COM<99>	7961.00	402.50
210	COM<197>	9762.00	264.00	260	COM<97>	7923.00	402.50
211	COM<195>	9762.00	297.00	261	COM<95>	7885.00	402.50
212	COM<193>	9762.00	330.00	262	COM<93>	7847.00	402.50
213	COM<191>	9762.00	363.00	263	COM<91>	7809.00	402.50
214	COM<189>	9762.00	396.00	264	COM<89>	7771.00	402.50
215	COM<187>	9762.00	429.00	265	COM<87>	7733.00	402.50
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226	COM<165>	9215.00	402.50	276	COM<65>	7315.00	402.50
227	COM<163>	9177.00	402.50	277	COM<63>	7277.00	402.50
228	COM<161>	9139.00	402.50	278	COM<61>	7239.00	402.50
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230	COM<157>	9063.00	402.50	280	COM<57>	7163.00	402.50
231	COM<155>	9025.00	402.50	281	COM<55>	7125.00	402.50
232	COM<153>	8987.00	402.50	282	COM<53>	7087.00	402.50
233	COM<151>	8949.00	402.50	283	COM<51>	7049.00	402.50
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250	COM<117>	8303.00	402.50	300	COM<17>	6403.00	402.50

No	Name	X	Y	No	Name	X	Y
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309	SEG<320>	6061.00	402.50	359	SEG<270>	4161.00	402.50
310	SEG<319>	6023.00	402.50	360	SEG<269>	4123.00	402.50
311	SEG<318>	5985.00	402.50	361	SEG<268>	4085.00	402.50
312	SEG<317>	5947.00	402.50	362	SEG<267>	4047.00	402.50
313	SEG<316>	5909.00	402.50	363	SEG<266>	4009.00	402.50
314	SEG<315>	5871.00	402.50	364	SEG<265>	3971.00	402.50
315	SEG<314>	5833.00	402.50	365	SEG<264>	3933.00	402.50
316	SEG<313>	5795.00	402.50	366	SEG<263>	3895.00	402.50
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319	SEG<310>	5681.00	402.50	369	SEG<260>	3781.00	402.50
320	SEG<309>	5643.00	402.50	370	SEG<259>	3743.00	402.50
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322	SEG<307>	5567.00	402.50	372	SEG<257>	3667.00	402.50
323	SEG<306>	5529.00	402.50	373	SEG<256>	3629.00	402.50
324	SEG<305>	5491.00	402.50	374	SEG<255>	3591.00	402.50
325	SEG<304>	5453.00	402.50	375	SEG<254>	3553.00	402.50
326	SEG<303>	5415.00	402.50	376	SEG<253>	3515.00	402.50
327	SEG<302>	5377.00	402.50	377	SEG<252>	3477.00	402.50
328	SEG<301>	5339.00	402.50	378	SEG<251>	3439.00	402.50
329	SEG<300>	5301.00	402.50	379	SEG<250>	3401.00	402.50
330	SEG<299>	5263.00	402.50	380	SEG<249>	3363.00	402.50
331	SEG<298>	5225.00	402.50	381	SEG<248>	3325.00	402.50
332	SEG<297>	5187.00	402.50	382	SEG<247>	3287.00	402.50
333	SEG<296>	5149.00	402.50	383	SEG<246>	3249.00	402.50
334	SEG<295>	5111.00	402.50	384	SEG<245>	3211.00	402.50
335	SEG<294>	5073.00	402.50	385	SEG<244>	3173.00	402.50
336	SEG<293>	5035.00	402.50	386	SEG<243>	3135.00	402.50
337	SEG<292>	4997.00	402.50	387	SEG<242>	3097.00	402.50
338	SEG<291>	4959.00	402.50	388	SEG<241>	3059.00	402.50
339	SEG<290>	4921.00	402.50	389	SEG<240>	3021.00	402.50
340	SEG<289>	4883.00	402.50	390	SEG<239>	2983.00	402.50
341	SEG<288>	4845.00	402.50	391	SEG<238>	2945.00	402.50
342	SEG<287>	4807.00	402.50	392	SEG<237>	2907.00	402.50
343	SEG<286>	4769.00	402.50	393	SEG<236>	2869.00	402.50
344	SEG<285>	4731.00	402.50	394	SEG<235>	2831.00	402.50
345	SEG<284>	4693.00	402.50	395	SEG<234>	2793.00	402.50
346	SEG<283>	4655.00	402.50	396	SEG<233>	2755.00	402.50
347	SEG<282>	4617.00	402.50	397	SEG<232>	2717.00	402.50
348	SEG<281>	4579.00	402.50	398	SEG<231>	2679.00	402.50
349	SEG<280>	4541.00	402.50	399	SEG<230>	2641.00	402.50
350	SEG<279>	4503.00	402.50	400	SEG<229>	2603.00	402.50

No	Name	X	Y	No	Name	X	Y
401	SEG<228>	2565.00	402.50	451	SEG<178>	665.00	402.50
402	SEG<227>	2527.00	402.50	452	SEG<177>	627.00	402.50
403	SEG<226>	2489.00	402.50	453	SEG<176>	589.00	402.50
404	SEG<225>	2451.00	402.50	454	SEG<175>	551.00	402.50
405	SEG<224>	2413.00	402.50	455	SEG<174>	513.00	402.50
406	SEG<223>	2375.00	402.50	456	SEG<173>	475.00	402.50
407	SEG<222>	2337.00	402.50	457	SEG<172>	437.00	402.50
408	SEG<221>	2299.00	402.50	458	SEG<171>	399.00	402.50
409	SEG<220>	2261.00	402.50	459	SEG<170>	361.00	402.50
410	SEG<219>	2223.00	402.50	460	SEG<169>	323.00	402.50
411	SEG<218>	2185.00	402.50	461	SEG<168>	285.00	402.50
412	SEG<217>	2147.00	402.50	462	SEG<167>	247.00	402.50
413	SEG<216>	2109.00	402.50	463	SEG<166>	209.00	402.50
414	SEG<215>	2071.00	402.50	464	SEG<165>	171.00	402.50
415	SEG<214>	2033.00	402.50	465	SEG<164>	133.00	402.50
416	SEG<213>	1995.00	402.50	466	SEG<163>	95.00	402.50
417	SEG<212>	1957.00	402.50	467	SEG<162>	57.00	402.50
418	SEG<211>	1919.00	402.50	468	SEG<161>	19.00	402.50
419	SEG<210>	1881.00	402.50	469	SEG<160>	-19.00	402.50
420	SEG<209>	1843.00	402.50	470	SEG<159>	-57.00	402.50
421	SEG<208>	1805.00	402.50	471	SEG<158>	-95.00	402.50
422	SEG<207>	1767.00	402.50	472	SEG<157>	-133.00	402.50
423	SEG<206>	1729.00	402.50	473	SEG<156>	-171.00	402.50
424	SEG<205>	1691.00	402.50	474	SEG<155>	-209.00	402.50
425	SEG<204>	1653.00	402.50	475	SEG<154>	-247.00	402.50
426	SEG<203>	1615.00	402.50	476	SEG<153>	-285.00	402.50
427	SEG<202>	1577.00	402.50	477	SEG<152>	-323.00	402.50
428	SEG<201>	1539.00	402.50	478	SEG<151>	-361.00	402.50
429	SEG<200>	1501.00	402.50	479	SEG<150>	-399.00	402.50
430	SEG<199>	1463.00	402.50	480	SEG<149>	-437.00	402.50
431	SEG<198>	1425.00	402.50	481	SEG<148>	-475.00	402.50
432	SEG<197>	1387.00	402.50	482	SEG<147>	-513.00	402.50
433	SEG<196>	1349.00	402.50	483	SEG<146>	-551.00	402.50
434	SEG<195>	1311.00	402.50	484	SEG<145>	-589.00	402.50
435	SEG<194>	1273.00	402.50	485	SEG<144>	-627.00	402.50
436	SEG<193>	1235.00	402.50	486	SEG<143>	-665.00	402.50
437	SEG<192>	1197.00	402.50	487	SEG<142>	-703.00	402.50
438	SEG<191>	1159.00	402.50	488	SEG<141>	-741.00	402.50
439	SEG<190>	1121.00	402.50	489	SEG<140>	-779.00	402.50
440	SEG<189>	1083.00	402.50	490	SEG<139>	-817.00	402.50
441	SEG<188>	1045.00	402.50	491	SEG<138>	-855.00	402.50
442	SEG<187>	1007.00	402.50	492	SEG<137>	-893.00	402.50
443	SEG<186>	969.00	402.50	493	SEG<136>	-931.00	402.50
444	SEG<185>	931.00	402.50	494	SEG<135>	-969.00	402.50
445	SEG<184>	893.00	402.50	495	SEG<134>	-1007.00	402.50
446	SEG<183>	855.00	402.50	496	SEG<133>	-1045.00	402.50
447	SEG<182>	817.00	402.50	497	SEG<132>	-1083.00	402.50
448	SEG<181>	779.00	402.50	498	SEG<131>	-1121.00	402.50
449	SEG<180>	741.00	402.50	499	SEG<130>	-1159.00	402.50
450	SEG<179>	703.00	402.50	500	SEG<129>	-1197.00	402.50

No	Name	X	Y	No	Name	X	Y
501	SEG<128>	-1235.00	402.50	551	SEG<78>	-3135.00	402.50
502	SEG<127>	-1273.00	402.50	552	SEG<77>	-3173.00	402.50
503	SEG<126>	-1311.00	402.50	553	SEG<76>	-3211.00	402.50
504	SEG<125>	-1349.00	402.50	554	SEG<75>	-3249.00	402.50
505	SEG<124>	-1387.00	402.50	555	SEG<74>	-3287.00	402.50
506	SEG<123>	-1425.00	402.50	556	SEG<73>	-3325.00	402.50
507	SEG<122>	-1463.00	402.50	557	SEG<72>	-3363.00	402.50
508	SEG<121>	-1501.00	402.50	558	SEG<71>	-3401.00	402.50
509	SEG<120>	-1539.00	402.50	559	SEG<70>	-3439.00	402.50
510	SEG<119>	-1577.00	402.50	560	SEG<69>	-3477.00	402.50
511	SEG<118>	-1615.00	402.50	561	SEG<68>	-3515.00	402.50
512	SEG<117>	-1653.00	402.50	562	SEG<67>	-3553.00	402.50
513	SEG<116>	-1691.00	402.50	563	SEG<66>	-3591.00	402.50
514	SEG<115>	-1729.00	402.50	564	SEG<65>	-3629.00	402.50
515	SEG<114>	-1767.00	402.50	565	SEG<64>	-3667.00	402.50
516	SEG<113>	-1805.00	402.50	566	SEG<63>	-3705.00	402.50
517	SEG<112>	-1843.00	402.50	567	SEG<62>	-3743.00	402.50
518	SEG<111>	-1881.00	402.50	568	SEG<61>	-3781.00	402.50
519	SEG<110>	-1919.00	402.50	569	SEG<60>	-3819.00	402.50
520	SEG<109>	-1957.00	402.50	570	SEG<59>	-3857.00	402.50
521	SEG<108>	-1995.00	402.50	571	SEG<58>	-3895.00	402.50
522	SEG<107>	-2033.00	402.50	572	SEG<57>	-3933.00	402.50
523	SEG<106>	-2071.00	402.50	573	SEG<56>	-3971.00	402.50
524	SEG<105>	-2109.00	402.50	574	SEG<55>	-4009.00	402.50
525	SEG<104>	-2147.00	402.50	575	SEG<54>	-4047.00	402.50
526	SEG<103>	-2185.00	402.50	576	SEG<53>	-4085.00	402.50
527	SEG<102>	-2223.00	402.50	577	SEG<52>	-4123.00	402.50
528	SEG<101>	-2261.00	402.50	578	SEG<51>	-4161.00	402.50
529	SEG<100>	-2299.00	402.50	579	SEG<50>	-4199.00	402.50
530	SEG<99>	-2337.00	402.50	580	SEG<49>	-4237.00	402.50
531	SEG<98>	-2375.00	402.50	581	SEG<48>	-4275.00	402.50
532	SEG<97>	-2413.00	402.50	582	SEG<47>	-4313.00	402.50
533	SEG<96>	-2451.00	402.50	583	SEG<46>	-4351.00	402.50
534	SEG<95>	-2489.00	402.50	584	SEG<45>	-4389.00	402.50
535	SEG<94>	-2527.00	402.50	585	SEG<44>	-4427.00	402.50
536	SEG<93>	-2565.00	402.50	586	SEG<43>	-4465.00	402.50
537	SEG<92>	-2603.00	402.50	587	SEG<42>	-4503.00	402.50
538	SEG<91>	-2641.00	402.50	588	SEG<41>	-4541.00	402.50
539	SEG<90>	-2679.00	402.50	589	SEG<40>	-4579.00	402.50
540	SEG<89>	-2717.00	402.50	590	SEG<39>	-4617.00	402.50
541	SEG<88>	-2755.00	402.50	591	SEG<38>	-4655.00	402.50
542	SEG<87>	-2793.00	402.50	592	SEG<37>	-4693.00	402.50
543	SEG<86>	-2831.00	402.50	593	SEG<36>	-4731.00	402.50
544	SEG<85>	-2869.00	402.50	594	SEG<35>	-4769.00	402.50
545	SEG<84>	-2907.00	402.50	595	SEG<34>	-4807.00	402.50
546	SEG<83>	-2945.00	402.50	596	SEG<33>	-4845.00	402.50
547	SEG<82>	-2983.00	402.50	597	SEG<32>	-4883.00	402.50
548	SEG<81>	-3021.00	402.50	598	SEG<31>	-4921.00	402.50
549	SEG<80>	-3059.00	402.50	599	SEG<30>	-4959.00	402.50
550	SEG<79>	-3097.00	402.50	600	SEG<29>	-4997.00	402.50

No	Name	X	Y	No	Name	X	Y
601	SEG<28>	-5035.00	402.50	651	COM<46>	-6935.00	402.50
602	SEG<27>	-5073.00	402.50	652	COM<48>	-6973.00	402.50
603	SEG<26>	-5111.00	402.50	653	COM<50>	-7011.00	402.50
604	SEG<25>	-5149.00	402.50	654	COM<52>	-7049.00	402.50
605	SEG<24>	-5187.00	402.50	655	COM<54>	-7087.00	402.50
606	SEG<23>	-5225.00	402.50	656	COM<56>	-7125.00	402.50
607	SEG<22>	-5263.00	402.50	657	COM<58>	-7163.00	402.50
608	SEG<21>	-5301.00	402.50	658	COM<60>	-7201.00	402.50
609	SEG<20>	-5339.00	402.50	659	COM<62>	-7239.00	402.50
610	SEG<19>	-5377.00	402.50	660	COM<64>	-7277.00	402.50
611	SEG<18>	-5415.00	402.50	661	COM<66>	-7315.00	402.50
612	SEG<17>	-5453.00	402.50	662	COM<68>	-7353.00	402.50
613	SEG<16>	-5491.00	402.50	663	COM<70>	-7391.00	402.50
614	SEG<15>	-5529.00	402.50	664	COM<72>	-7429.00	402.50
615	SEG<14>	-5567.00	402.50	665	COM<74>	-7467.00	402.50
616	SEG<13>	-5605.00	402.50	666	COM<76>	-7505.00	402.50
617	SEG<12>	-5643.00	402.50	667	COM<78>	-7543.00	402.50
618	SEG<11>	-5681.00	402.50	668	COM<80>	-7581.00	402.50
619	SEG<10>	-5719.00	402.50	669	COM<82>	-7619.00	402.50
620	SEG<9>	-5757.00	402.50	670	COM<84>	-7657.00	402.50
621	SEG<8>	-5795.00	402.50	671	COM<86>	-7695.00	402.50
622	SEG<7>	-5833.00	402.50	672	COM<88>	-7733.00	402.50
623	SEG<6>	-5871.00	402.50	673	COM<90>	-7771.00	402.50
624	SEG<5>	-5909.00	402.50	674	COM<92>	-7809.00	402.50
625	SEG<4>	-5947.00	402.50	675	COM<94>	-7847.00	402.50
626	SEG<3>	-5985.00	402.50	676	COM<96>	-7885.00	402.50
627	SEG<2>	-6023.00	402.50	677	COM<98>	-7923.00	402.50
628	SEG<1>	-6061.00	402.50	678	COM<100>	-7961.00	402.50
629	COM<2>	-6099.00	402.50	679	COM<102>	-7999.00	402.50
630	COM<4>	-6137.00	402.50	680	COM<104>	-8037.00	402.50
631	COM<6>	-6175.00	402.50	681	COM<106>	-8075.00	402.50
632	COM<8>	-6213.00	402.50	682	COM<108>	-8113.00	402.50
633	COM<10>	-6251.00	402.50	683	COM<110>	-8151.00	402.50
634	COM<12>	-6289.00	402.50	684	COM<112>	-8189.00	402.50
635	COM<14>	-6327.00	402.50	685	COM<114>	-8227.00	402.50
636	COM<16>	-6365.00	402.50	686	COM<116>	-8265.00	402.50
637	COM<18>	-6403.00	402.50	687	COM<118>	-8303.00	402.50
638	COM<20>	-6441.00	402.50	688	COM<120>	-8341.00	402.50
639	COM<22>	-6479.00	402.50	689	COM<122>	-8379.00	402.50
640	COM<24>	-6517.00	402.50	690	COM<124>	-8417.00	402.50
641	COM<26>	-6555.00	402.50	691	COM<126>	-8455.00	402.50
642	COM<28>	-6593.00	402.50	692	COM<128>	-8493.00	402.50
643	COM<30>	-6631.00	402.50	693	COM<130>	-8531.00	402.50
644	COM<32>	-6669.00	402.50	694	COM<132>	-8569.00	402.50
645	COM<34>	-6707.00	402.50	695	COM<134>	-8607.00	402.50
646	COM<36>	-6745.00	402.50	696	COM<136>	-8645.00	402.50
647	COM<38>	-6783.00	402.50	697	COM<138>	-8683.00	402.50
648	COM<40>	-6821.00	402.50	698	COM<140>	-8721.00	402.50
649	COM<42>	-6859.00	402.50	699	COM<142>	-8759.00	402.50
650	COM<44>	-6897.00	402.50	700	COM<144>	-8797.00	402.50

No	Name	X	Y	No	Name	X	Y
701	COM<146>	-8835.00	402.50				
702	COM<148>	-8873.00	402.50				
703	COM<150>	-8911.00	402.50				
704	COM<152>	-8949.00	402.50				
705	COM<154>	-8987.00	402.50				
706	COM<156>	-9025.00	402.50				
707	COM<158>	-9063.00	402.50				
708	COM<160>	-9101.00	402.50				
709	COM<162>	-9139.00	402.50				
710	COM<164>	-9177.00	402.50				
711	COM<166>	-9215.00	402.50				
712	COM<168>	-9253.00	402.50				
713	COM<170>	-9291.00	402.50				
714	COM<172>	-9329.00	402.50				
715	COM<174>	-9367.00	402.50				
716	COM<176>	-9405.00	402.50				
717	COM<178>	-9443.00	402.50				
718	COM<180>	-9481.00	402.50				
719	COM<182>	-9519.00	402.50				
720	COM<184>	-9557.00	402.50				
721	COM<186>	-9595.00	402.50				
722	COM<188>	-9762.00	429.00				
723	COM<190>	-9762.00	396.00				
724	COM<192>	-9762.00	363.00				
725	COM<194>	-9762.00	330.00				
726	COM<196>	-9762.00	297.00				
727	COM<198>	-9762.00	264.00				
728	COM<200>	-9762.00	231.00				
729	COM<202>	-9762.00	198.00				
730	COM<204>	-9762.00	165.00				
731	COM<206>	-9762.00	132.00				
732	COM<208>	-9762.00	99.00				
733	COM<210>	-9762.00	66.00				
734	COM<212>	-9762.00	33.00				
735	COM<214>	-9762.00	0.00				
736	COM<216>	-9762.00	-33.00				
737	COM<218>	-9762.00	-66.00				
738	COM<220>	-9762.00	-99.00				
739	COM<222>	-9762.00	-132.00				
740	COM<224>	-9762.00	-165.00				
741	COM<226>	-9762.00	-198.00				
742	COM<228>	-9762.00	-231.00				
743	COM<230>	-9762.00	-264.00				
744	COM<232>	-9762.00	-297.00				
745	COM<234>	-9762.00	-330.00				
746	COM<236>	-9762.00	-363.00				
747	COM<238>	-9762.00	-396.00				
748	COM<240>	-9762.00	-429.00				

PIN DESCRIPTION

Signals	Number of Pins	I/O	Connected to	Functions
IM2,IM1,IM0	3	I	GND or VCC	Selects the MPU interface mode IM2 IM1 IM0 MPU interface mode GND GND GND 68-system 16-bit bus interface GND GND VCC 68-system 8-bit bus interface GND VCC GND 80-system 16-bit bus interface GND VCC VCC 80-system 8-bit bus interface VCC GND GND 4-line serial interface
CSB	1	I	MPU	Chip select; Low: chip enabled High: Chip disabled Must be fixed at VCC level when chip is not active.
RS	1	I	MPU	Register select Low: Index/status select High: Command select
EWRB_SCL	1	I	MPU	For 68-system bus interface, serves as an enable signal to activate data read/write operation. For 80-system bus interface, serves as a write strobe signal and writes data at the low level. For 4-line serial interface, serves as a synchronized clock signal
RWRDB_SDA	1	I	MPU	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal and reads data at the low level For 4-line serial interface, serves as the serial data pin for data transformation.
DB0–DB15	16	I/O	MPU	Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8, fix unused DB7 ~ DB0 to the VCC or GND level. When in serial interface, fix unused DB15-DB0 to the VCC or GND level
RESETB	1	I	MPU or external RC circuit	Reset pin, Low active. The chip must be reset after power-on. ****A minimal 10ms wait period should be given after finish RESET action when send first command.**
IRS	1	I	GND or VCC	Internal resistor select pin, this pin selects the V0 voltage level Low: use external resistor High: use internal resistor
CLS	1	I	GND or VCC	Build-in oscillator circuit enable / disable select Low: disable High: enable (external display clock input CL pin)
CL	1	I	OPEN or external clock source	Display clock input/output pin
REGON	1	I	VCC	Internal regulator for digital core power, connects to VCC.
TEST1	1	I	OPEN	Test pin, keeps open.
TEST2	1	O	OPEN	Test pin, keeps open. (Built-in oscillator frequency can be measured in TEST2 pin.)

Signals	Number of Pins	I/O	Connected to	Functions
COM1 ~ COM240	240	O	LCD	Output signals for common drive. In the display-off period (D = 0), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The CMS bit will decide the shift direction of the COM outputs. SHL = 0, the shift direction is COM1 → COM240. SHL = 1, the shift direction is COM240 → COM1
SEG1 ~ SEG320	320	O	LCD	Output signals for segment driver. In the display-off period (D = 0), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The SGS bit will decide the image mapping of the SEG outputs. SGS = 0, the image mapping is normal SGS = 1, the image mapping is mirrored.
V0 ~ V4		I/O	Capacitors to GND	Built-in driver voltage sources output. These pins should be connected by capacitors to GND for voltage stabilization.
VCC		I	Power source	Power supply
VDD		I/O	Power source	Digital core power pad Connect them with the 1uF capacitor
GND		I	Ground	Ground
DMYVCC		O		Dummy VCC pin, use in ITO connection for chip configuration.
DMYGND		O		Dummy GND pin, use in ITO connection for chip configuration.
VREF		O	Open	For Testing. Please just keeps this pin open.
VR		I	Open or external Resistor	V0 voltage adjust pin It is valid only when internal voltage regulator resistors not used.(IRS = "L")
VCI		I	Power source	VCI is the reference voltage source of internal Booster circuit. When the internal Booster circuit is not used, must keep this pin open.
VOUT1, VOUT2		I/O	Capacitor to GND	VOUT1/2 is the internal booster output, step-up voltage based on the difference voltage of VCI & GND. VOUT1/2 can't over the defined absolute maximum rating
C11P, C11M		--	Capacitor +/-	Capacitor 1 positive/negative connection pin for booster1 circuit.
C12P, C12M		--	Capacitor +/-	Capacitor 2 positive/negative connection pin for booster1 circuit.
C21P, C21M		--	Capacitor +/-	Capacitor 3 positive/negative connection pin for booster2 circuit.
C22P, C22M		--	Capacitor +/-	Capacitor 4 positive/negative connection pin for booster2 circuit.
C23P, C23M		--	Capacitor +/-	Capacitor 5 positive/negative connection pin for booster2 circuit.
C24P, C24M		--	Capacitor +/-	Capacitor 6 positive/negative connection pin for booster2 circuit.
VPP		I	External power	VPP is the power pin of embedded OTP (One-Time-Programming) non-volatile memory circuit. Only during OTP programming cycle VPP should connect to an external power source (about 7.5V). On the other cases, just keep this pin open. (Please reserve ITO contact pad for OTP programming if using OTP function)

FUNCTION DESCRIPTION

System Interface

System interface configuration

- The TR7707 has three high-speed system interfaces: 80-system 16-bit/8-bit bus, 68-system 16-bit/8-bit bus and 4-line serial interface.
- The MPU interface mode is selected by the IM2-0 pins.
- For 8-bit interface, only the DB15-DB8 are activated, keep DB7-DB0 to GND or VCC.
- The TR7707 adopts 16-bit bus architecture. For 8-bit interface access, a 16-bit data (index or command) must be transferred by two times; the first is the high byte & the second is the low byte.

Command write

- The TR7707 adopts indirect command addressing mechanism, first must specify the command index, then write the command data into the index-addressed register.
- Command write flow

Step	RS	Description
1	0	Write Command index to IR (Index Register).
2	1	Write Command data into the command register indexed by IR.

RAM data write

- RAM data write flow

Step	RS	Description
1	0	Write Command index = R08H.
2	1	Write the initial RAM address.
3	0	Write Command index = R09H.
4	1	Write RAM data consecutively, the RAM address will be auto-incremented.

Status read

- Status read flow

Step	RS	Description
1	0	Read internal Status (dummy read is not needed).

RAM data read

- RAM data read flow

Step	RS	Description
1	0	Write Command index = R08H.
2	1	Write the target RAM address.
3	0	Write Command index = R09H.
4	1	Read RAM data; the first 16bit is dummy-read, the second 16bit is the real RAM data. The RAM address will be auto-incremented.
5	--	If want to read RAM another address data, then repeat Step 1 → 4.

RAM Addressing Mapping(Grayscale mode, DSPM=011)

Segment Driver		AY[7:0]	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	.....	SEG 8	SEG 9	.....	SEG 12	.....	SEG 317	.....	SGE 320
SGS =0	AX[6:0]		00H				01H			02H			.....	4FH		
	BIT		D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0				D15 ..... D0			D15 ..... D0				D15 ..... D0		
SGS =1	AX[6:0]		4FH				4EH			4DH			.....	00H		
	BIT		D3 D2 D1 D0 D7 D6 D5 D4 D11 D10 D9 D8 D15 D14 D13 D12				D3 ..... D12			D3 ..... D12			.....	D3 ..... D12		
COM1		00H	Address: "0000"H				"0001"H			"0002"H			.....	"004F"H		
COM2		01H	Address: "0100"H				"0101"H			"0102"H			.....	"014F"H		
COM3		02H	Address: "0200"H				"0201"H			"0202"H			.....	"024F"H		
COM4		03H	Address: "0300"H				"0301"H			"0302"H			.....	"034F"H		
COM5		04H	Address: "0400"H				"0401"H			"0402"H			.....	"044F"H		
COM6		05H	Address: "0500"H				"0501"H			"0502"H			.....	"054F"H		
COM7		06H	Address: "0600"H				"0601"H			"0602"H			.....	"064F"H		
COM8		07H	Address: "0700"H				"0701"H			"0702"H			.....	"074F"H		
COM9		08H	Address: "0800"H				"0801"H			"0802"H			.....	"084F"H		
COM10		09H	Address: "0900"H				"0901"H			"0902"H			.....	"094F"H		
COM11		0AH	Address: "0A00"H				"0A01"H			"0A02"H			.....	"0A4F"H		
COM12		0BH	Address: "0B00"H				"0B01"H			"0B02"H			.....	"0B4F"H		
COM13		0CH	Address: "0C00"H				"0C01"H			"0C02"H			.....	"0C4F"H		
COM14		0DH	Address: "0D00"H				"0D01"H			"0D02"H			.....	"0D4F"H		
COM15		0EH	Address: "0E00"H				"0E01"H			"0E02"H			.....	"0E4F"H		
COM16		0FH	Address: "0F00"H				"0F01"H			"0F02"H			.....	"0F4F"H		
COM17		10H	Address: "1000"H				"1001"H			"1002"H			.....	"104F"H		
COM18		11H	Address: "1100"H				"1101"H			"1102"H			.....	"114F"H		
COM19		12H	Address: "1200"H				"1201"H			"1202"H			.....	"124F"H		
COM20		13H	Address: "1300"H				"1301"H			"1302"H			.....	"134F"H		
.....		.....	.....				.....			.....			.....	.....		
COM237		ECH	Address: "EC00"H				"EC01"H			"EC02"H			.....	"EC4F"H		
COM238		EDH	Address: "ED00"H				"ED01"H			"ED02"H			.....	"ED4F"H		
COM239		EEH	Address: "EE00"H				"EE01"H			"EE02"H			.....	"EE4F"H		
COM240		EFH	Address: "EF00"H				"EF01"H			"EF02"H			.....	"EF4F"H		

MSB D[4n+3]	D[4n+2]	D[4n+1]	LSB D[4n]	LCD
0	0	0	0	Gary Scale 0 (Darkness)
0	0	0	1	Gary Scale 1
0	0	1	0	Gary Scale 2
0	0	1	1	Gary Scale 3
0	1	0	0	Gary Scale 4
0	1	0	1	Gary Scale 5
0	1	1	0	Gary Scale 6
0	1	1	1	Gary Scale 7
1	0	0	0	Gary Scale 8
1	0	0	1	Gary Scale 9
1	0	1	0	Gary Scale 10
1	0	1	1	Gary Scale 11
1	1	0	0	Gary Scale 12
1	1	0	1	Gary Scale 13
1	1	1	0	Gary Scale 14
1	1	1	1	Gary Scale 15 (Lightness)

Note : **n = 0, 1, 2, 3**

RAM Addressing Mapping (Mono mode, DSPM=100)

Segment Driver		AY[7:0]	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	SEG 8	SEG 9	SEG 10	SEG 11	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	.....	SEG 32	SEG 33	.....	SEG 48	.....	SEG 305	.....	SGE 320
SGS =0	AX[6:0]		00H																01H			02H			.....	13H		
	BIT		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	.....	D0	D15	.....	D0		D15	.....	D0
SGS =1	AX[6:0]		13H																12H			11H			.....	00H		
	BIT		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0		D15	D0		D15	.....	D0		D15
COM1		00H	Address: "0000"H																"0001"H			"0002"H			.....	"0013"H		
COM2		01H	Address: "0100"H																"0101"H			"0102"H			.....	"0113"H		
COM3		02H	Address: "0200"H																"0201"H			"0202"H			.....	"0213"H		
COM4		03H	Address: "0300"H																"0301"H			"0302"H			.....	"0313"H		
COM5		04H	Address: "0400"H																"0401"H			"0402"H			.....	"0413"H		
COM6		05H	Address: "0500"H																"0501"H			"0502"H			.....	"0513"H		
COM7		06H	Address: "0600"H																"0601"H			"0602"H			.....	"0613"H		
COM8		07H	Address: "0700"H																"0701"H			"0702"H			.....	"0713"H		
COM9		08H	Address: "0800"H																"0801"H			"0802"H			.....	"0813"H		
COM10		09H	Address: "0900"H																"0901"H			"0902"H			.....	"0913"H		
COM11		0AH	Address: "0A00"H																"0A01"H			"0A02"H			.....	"0A13"H		
COM12		0BH	Address: "0B00"H																"0B01"H			"0B02"H			.....	"0B13"H		
COM13		0CH	Address: "0C00"H																"0C01"H			"0C02"H			.....	"0C13"H		
COM14		0DH	Address: "0D00"H																"0D01"H			"0D02"H			.....	"0D13"H		
COM15		0EH	Address: "0E00"H																"0E01"H			"0E02"H			.....	"0E13"H		
COM16		0FH	Address: "0F00"H																"0F01"H			"0F02"H			.....	"0F13"H		
COM17		10H	Address: "1000"H																"1001"H			"1002"H			.....	"1013"H		
COM18		11H	Address: "1100"H																"1101"H			"1102"H			.....	"1113"H		
COM19		12H	Address: "1200"H																"1201"H			"1202"H			.....	"1213"H		
COM20		13H	Address: "1300"H																"1301"H			"1302"H			.....	"1313"H		
.....		.....	.....																.....			.....			.....	.....		
COM237		ECH	Address: "EC00"H																"EC01"H			"EC02"H			.....	"EC13"H		
COM238		EDH	Address: "ED00"H																"ED01"H			"ED02"H			.....	"ED13"H		
COM239		EEH	Address: "EE00"H																"EE01"H			"EE02"H			.....	"EE13"H		
COM240		EFH	Address: "EF00"H																"EF01"H			"EF02"H			.....	"EF13"H		

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of Vcc. This oscillator signal is used in the voltage converter and display timing generation circuit. The oscillator circuit is only enabled when CLS = “H”. When on-chip oscillator is not used, CLS pin must be “L” condition. In this time, external clock must be input from CL pin.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL generated by oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 320-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The LCD AC signal, M is generated from the display clock. 2-frame AC driver waveforms with internal timing signal are shown in figure 1. It can generate n-line reversal alternating drive waveforms by setting data (NW-1) to the n-line reversal drive register, the timing signal are shown in figure 2.

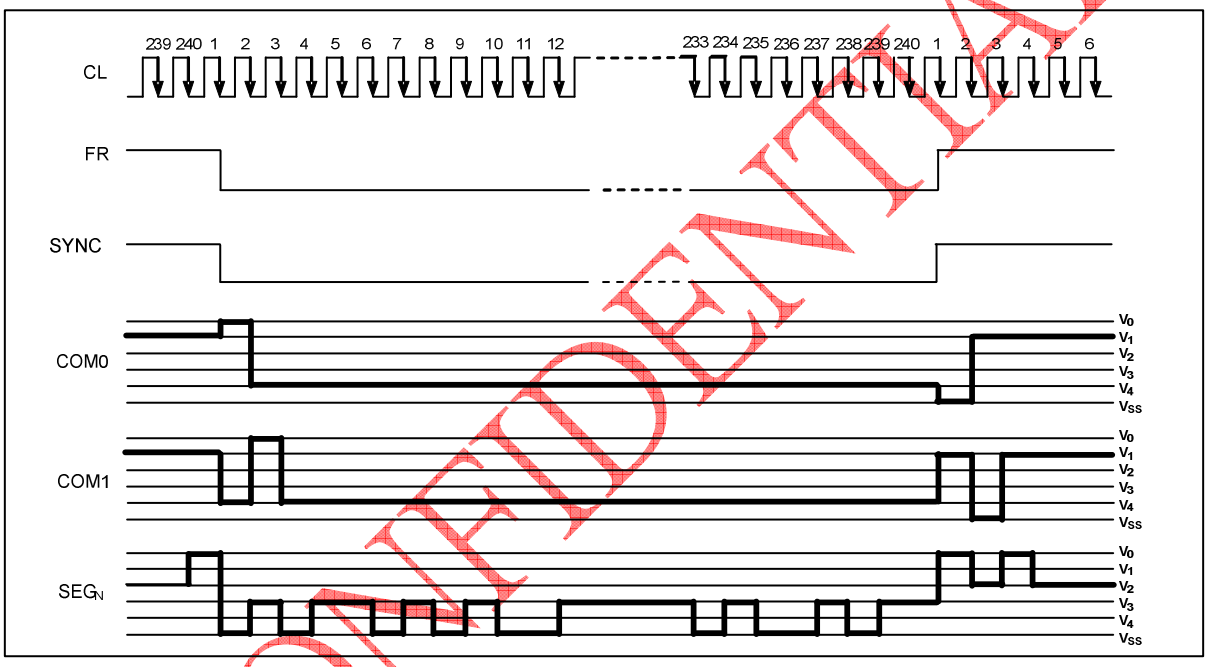


Figure 1. 2-frame Alternating Driving Waveform

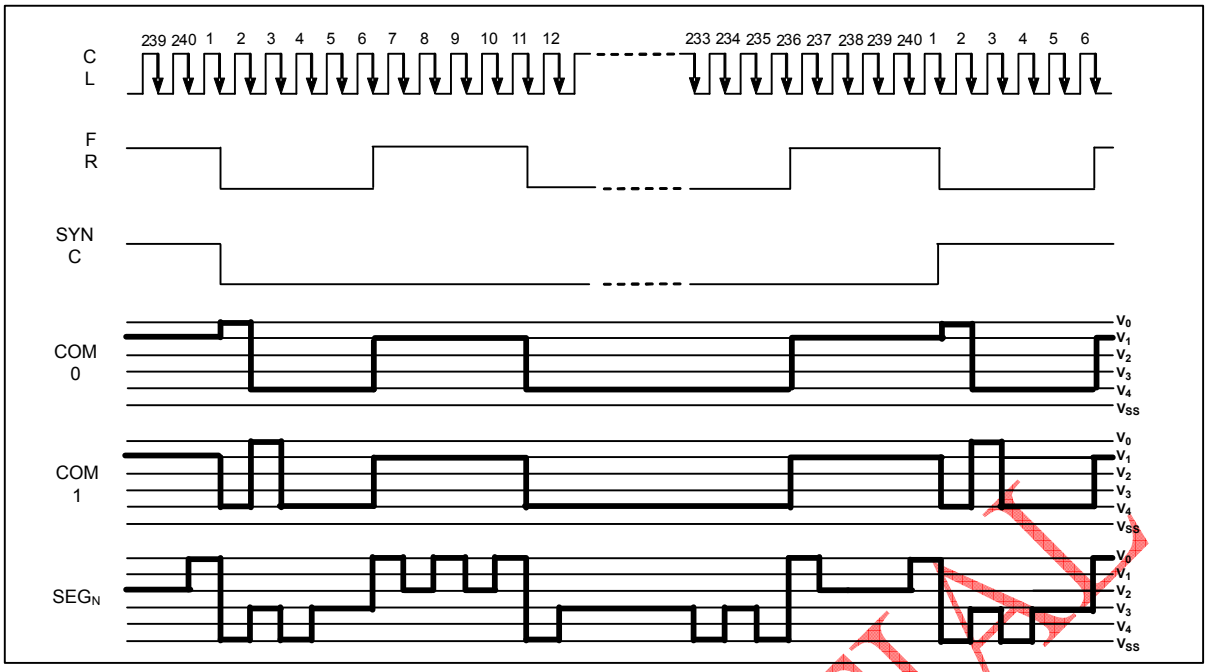


Figure 2. n-line Reversal Alternating Driving Waveform
(Example of NW = 5, when the line reversal register is set to 4)

LCD DRIVER CIRCUIT

This driver circuit is configured by 240-channel common driver and 320-channel segment driver. This LCD panel driver voltage Depends on the combination of display data and M signal.

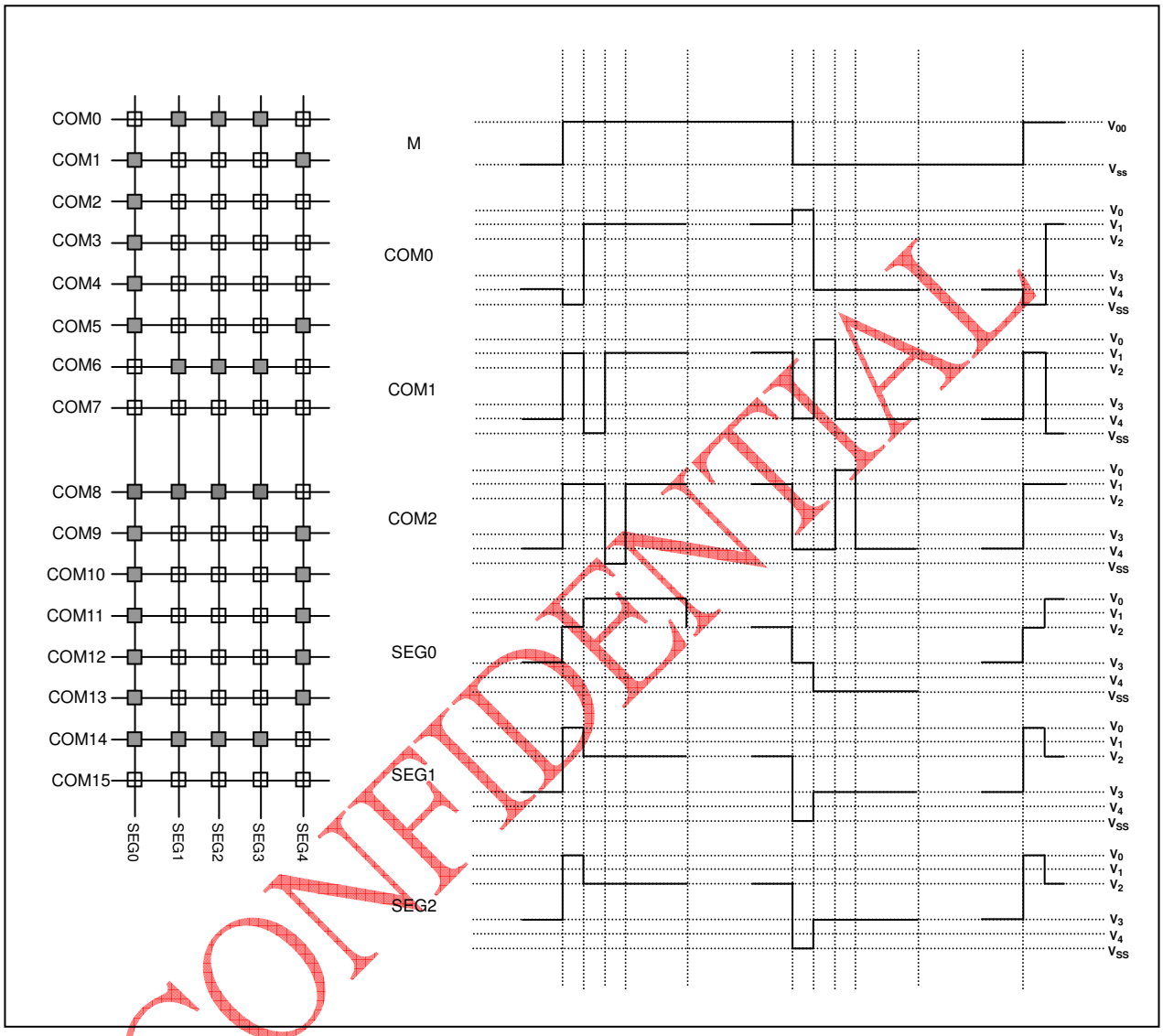


Figure 3. Segment and Common Timing

POWRE SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to “Instruction Description”. Figure. 10, 11, 12 and 13 shows the referenced combinations in using Power Supply circuits.

Table 1. Recommended Power Supply Combinations

User setup	Power Control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT1	VOUT2	V0	V1 to V4
Only the internal power supply circuits are used	111	ON	ON	ON	Open	Open (*1)	Open (*1)	Open (*1)
Only the voltage regulator circuits and voltage follower circuits are used	011	OFF	ON	ON	Connect VCC (*2)	External input	Open (*1)	Open (*1)
Only the voltage follower circuits are used	001	OFF	OFF	ON	Open	Connect V0	External input	Open (*1)
Only the external power supply circuits are used	000	OFF	OFF	OFF	Open	Connect V0	External input	External input

*1 : Connected to Capacitor.
*2 : VCC can’t be smaller than 3.0V.

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and GND to 4, 6, 8 or 10 times toward positive side and boosted voltage is outputted from VOUT2 pin.

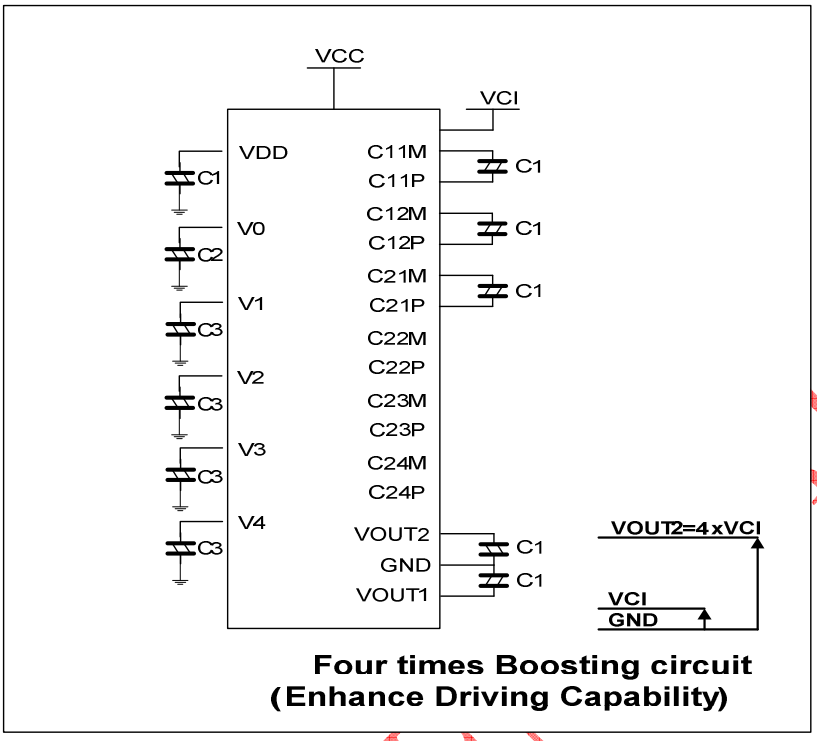


Figure 4. x4 Boosting Circuit

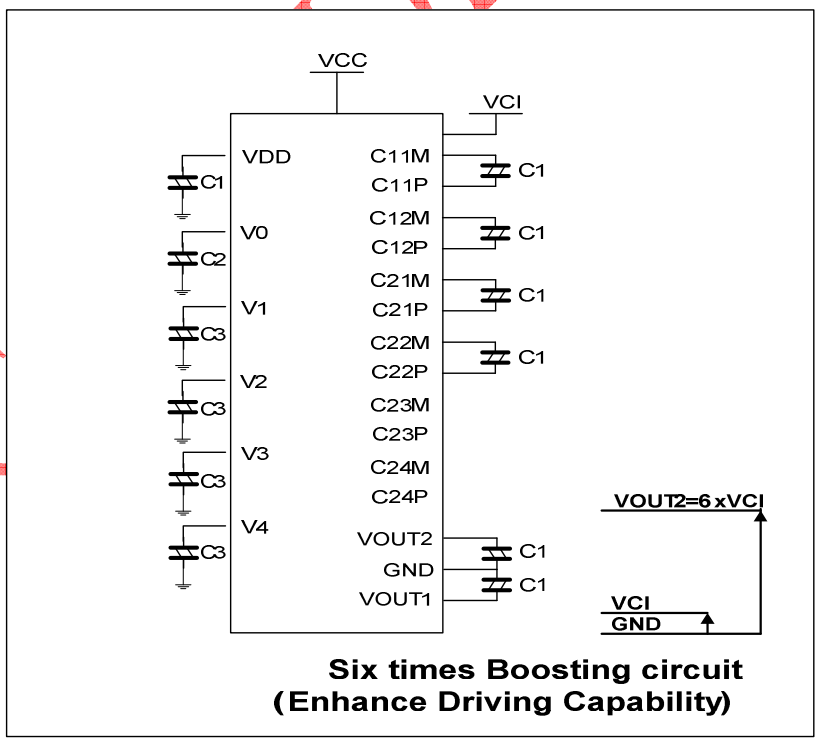


Figure 5. x6 Boosting Circuit

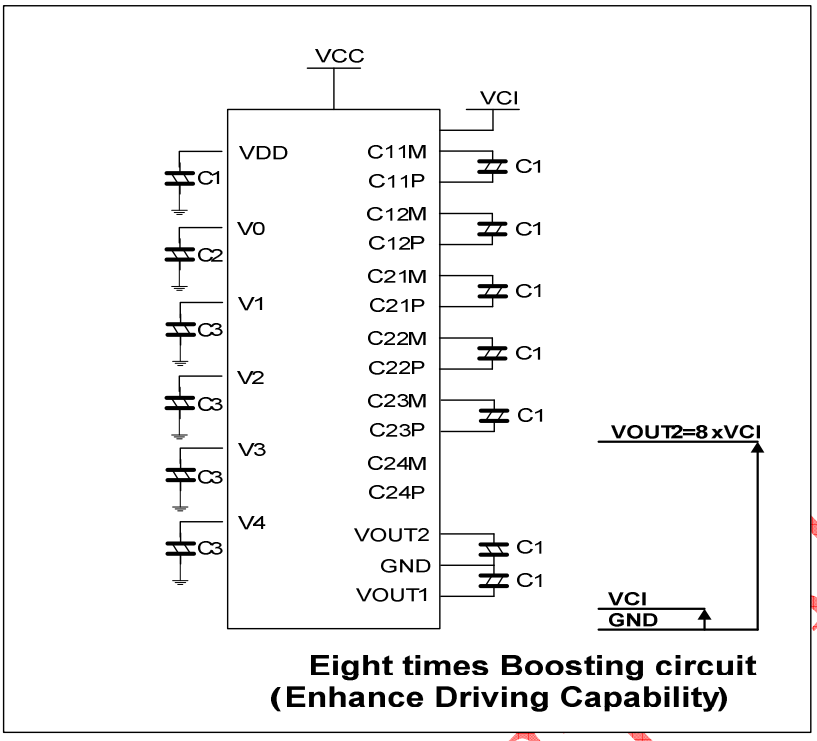


Figure 6. x8 Boosting Circuit

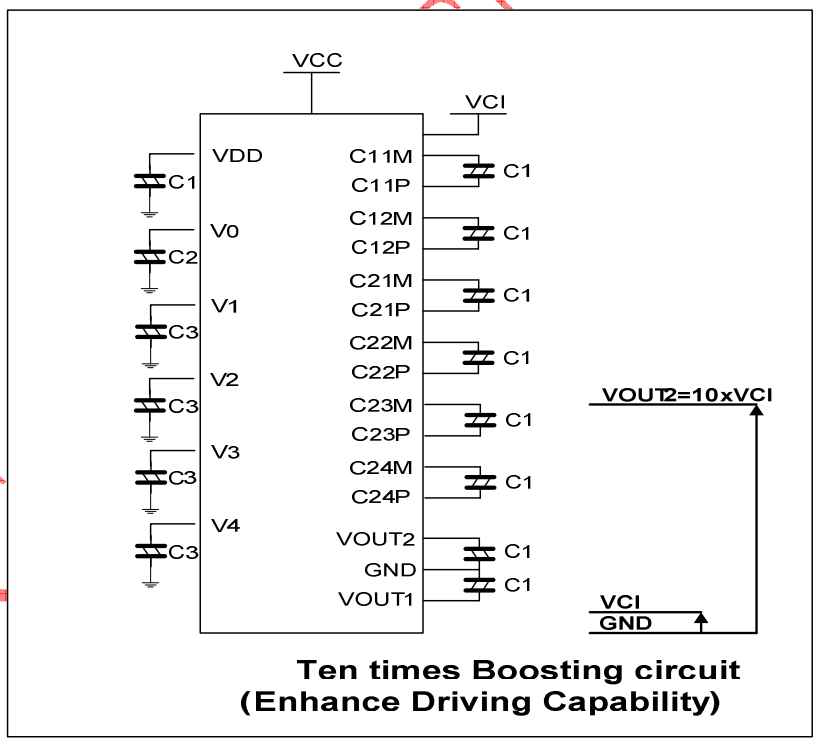


Figure 7. x10 Boosting Circuit

*The VCI voltage range must be set so that the VOUT2 voltage does not exceed 32V.
*C1, C2 and C3 are determined by the size of the LCD being driven, select a value that will stabilize the liquid crystal drive voltage.
*C1 = 1.0 to 4.7µF, C2 = 2.2 to 4.7µF, C3 = 0.47 to 1.0µF.

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting internal or external resistors, Ra and Rb, within the range of |V0| < |VOUT2|. Because VOUT2 is the operating Voltage of operational-amplifier circuits shown in Figure 10, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by external Ra and External Rb and V_{REF} when IRS="L". The Ra and Rb are connected externally to VR pin. V_{REF} is the internal reference voltage at Table 2. For the Eq. 2 and 3, we determine V0 by internal Ra and Rb and V_{REF} when IRS="H". Internal Ra and Rb can be controlled by CT and write to Electronic Contrast Control Register (8 bit) at Table. 3 and VRG, where the parameter α is the value selected by instruction, "Set Contrast Control Register", within the range 0 to 255. V_{REF} voltage at Ta=25℃ is shown in Table 2.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{REF} \ [V] \quad \text{---- (Eq. 1)}$$

$$V0 = (4 + \alpha \times 0.025) \times V_{REF} \ [V] \quad \text{for VRG=0 ---- (Eq. 2)}$$

$$V0 = (8 + \alpha \times 0.025) \times V_{REF} \ [V] \quad \text{for VRG=1 ---- (Eq. 3)}$$

Table 2. V_{REF} Voltage at Ta = 25℃

Device	TC[1:0]	Temp. coefficient	V_{REF} [V]
Internal Reference Voltage	00	-0.00%/℃	1.80
	01	-0.05%/℃	1.80
	10	-0.10%/℃	1.80
	11	-0.15%/℃	1.80

Table 3. Electronic Contrast Control Register (256 Steps)

CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Reference voltage Parameter (α)	V0	Contrast
0	0	0	0	0	0	0	0	0(default)	Minimum	Low
0	0	0	0	0	0	0	1	1	:	:
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	254	:	:
1	1	1	1	1	1	1	1	255	Maximum	High

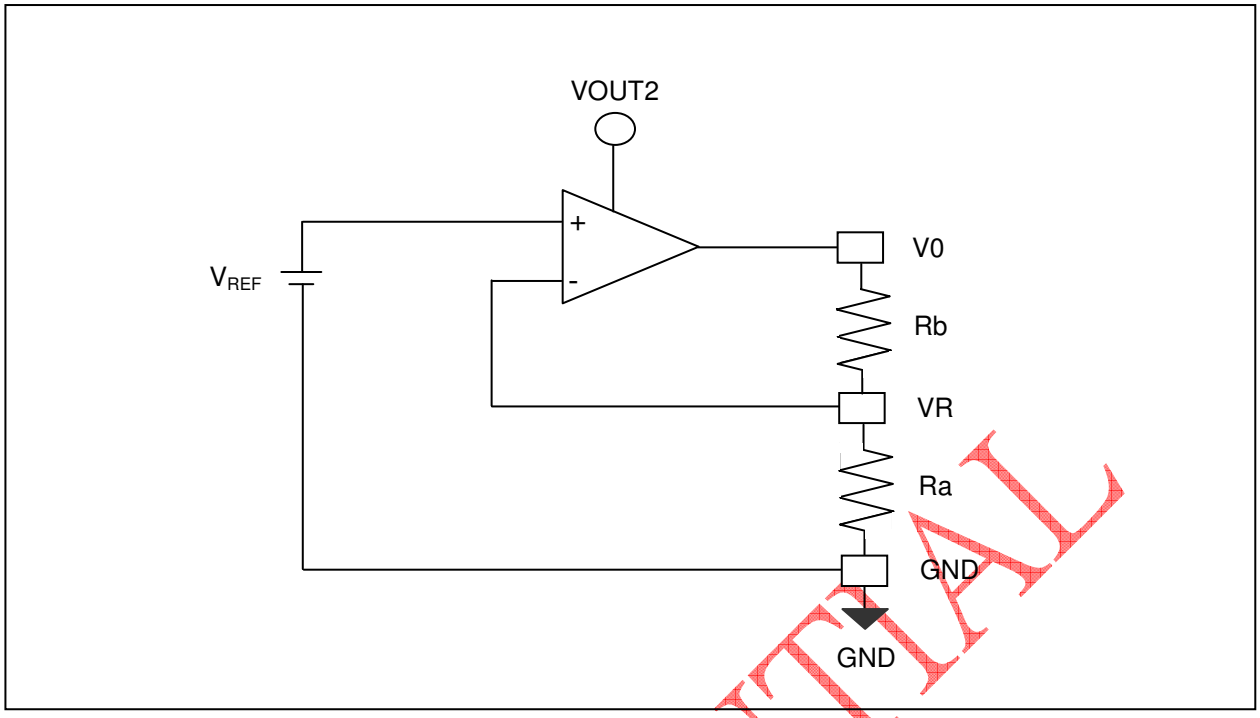


Figure 8. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb. (IRS = “H”)

When IRS bit is “H”, resistor Ra is connected internally between VR pin and GND, and Rb is connected between V0 and VR. We determine V0 by Electronic Contrast Control Register (8 bit) at Table. 3 and VRG.

The following Figure. 9 shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 8 bit Electronic Contrast Control registers for zero temperature coefficient at Ta = 25℃.

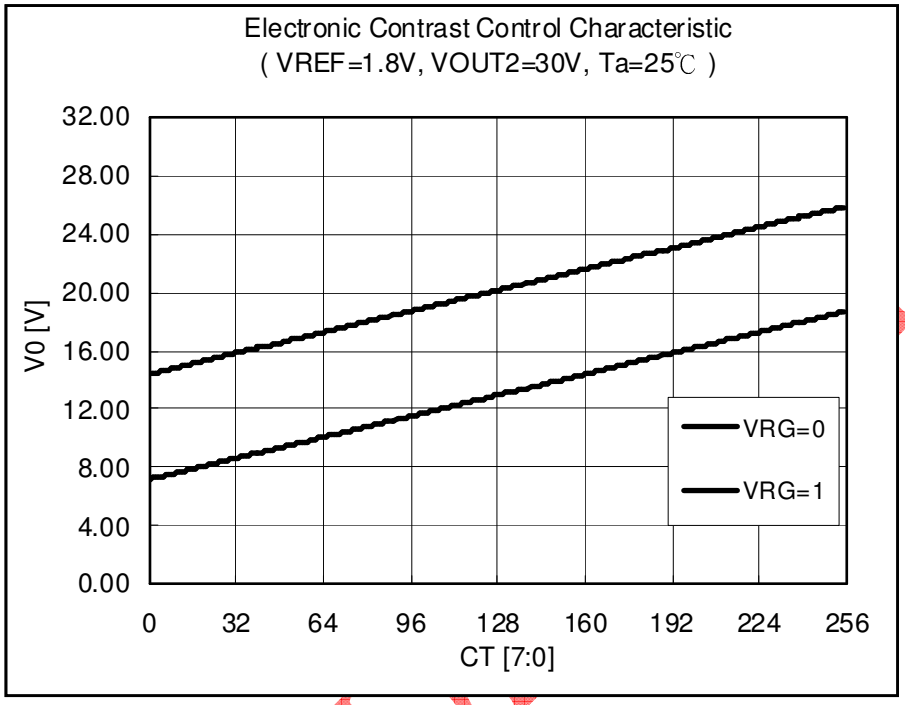


Figure 9. Electronic Contrast Control Level

In Case of Using External Resistors, Ra and Rb. (IRS = “L”)

When IRS bit is “L”, it is necessary to connect external regulator resistor Ra between VR and GND, and Rb between V0 and VR.

Example : For the following requirements

1. LCD driver voltage, V0 = 18V
2. Maximum current flowing Ra, Rb = 1 µA

From Eq. 1

$$18 = \left(1 + \frac{Rb}{Ra} \right) \times V_{REF} \quad [V] \text{ ---- (Eq. 3)}$$

From Table. 2

V_{REF} = 1.80 [V] ---- (Eq. 4)

From requirement 2.

$$\frac{18}{Ra + Rb} = 1 \ [\mu A] \text{ ---- (Eq. 5)}$$

From equations Eq. 3, 4 and 5

Ra 1.8 [MΩ]

Rb 16.2 [MΩ]

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the Voltage Follower for increasing are capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 4. The Relationship between V1 to V4 Level and Duty Ratio

LCD bias	V1	V2	V3	V4
1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0
1/10	(9/10) x V0	(8/10) x V0	(2/10) x V0	(1/10) x V0
1/11	(10/11) x V0	(9/11) x V0	(2/11) x V0	(1/11) x V0
1/12	(11/12) x V0	(10/12) x V0	(2/12) x V0	(1/12) x V0
1/13	(12/13) x V0	(11/13) x V0	(2/13) x V0	(1/13) x V0
1/14	(13/14) x V0	(12/14) x V0	(2/14) x V0	(1/14) x V0
1/15	(14/15) x V0	(13/15) x V0	(2/15) x V0	(1/15) x V0
1/16	(15/16) x V0	(14/16) x V0	(2/16) x V0	(1/16) x V0

REFERENCE CIRCUIT EXAMPLES

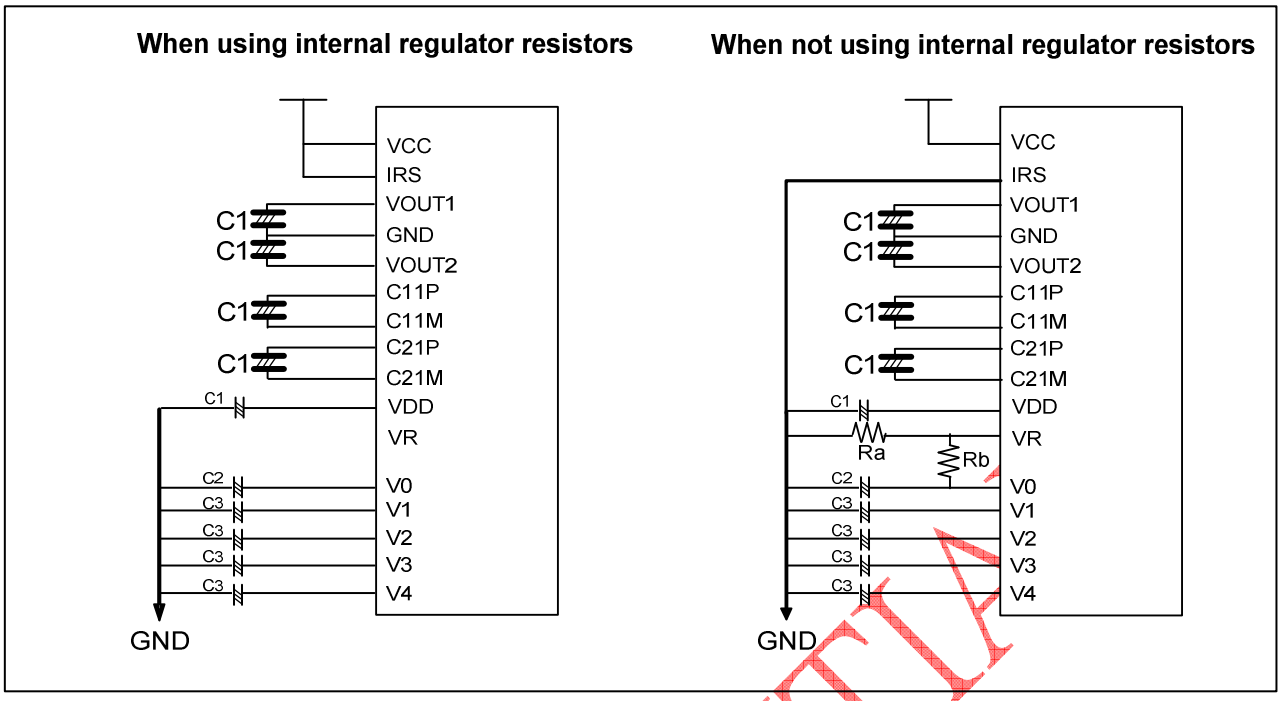


Figure 10. When Using all Internal LCD Power Circuits (4-time V/C : ON, V/R : ON, V/F : ON)

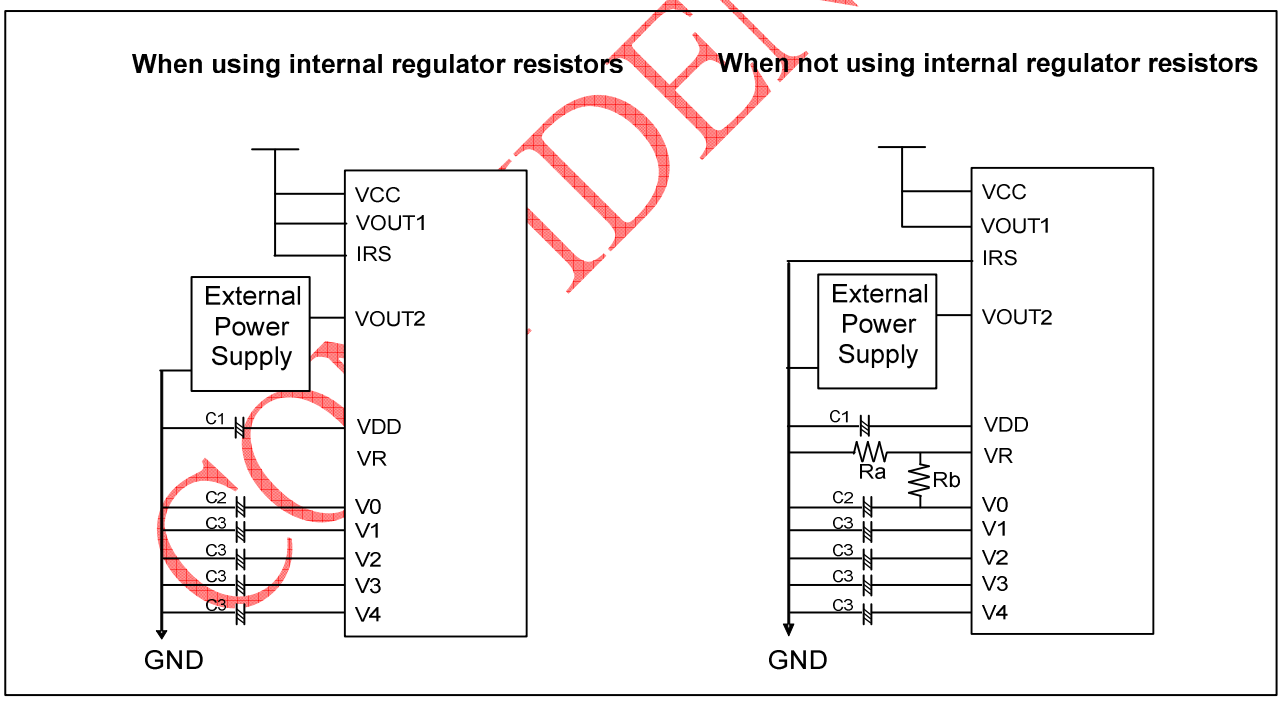


Figure 11. When Using some Internal LCD Power Circuits (V/C : OFF, V/R : ON, V/F : ON)

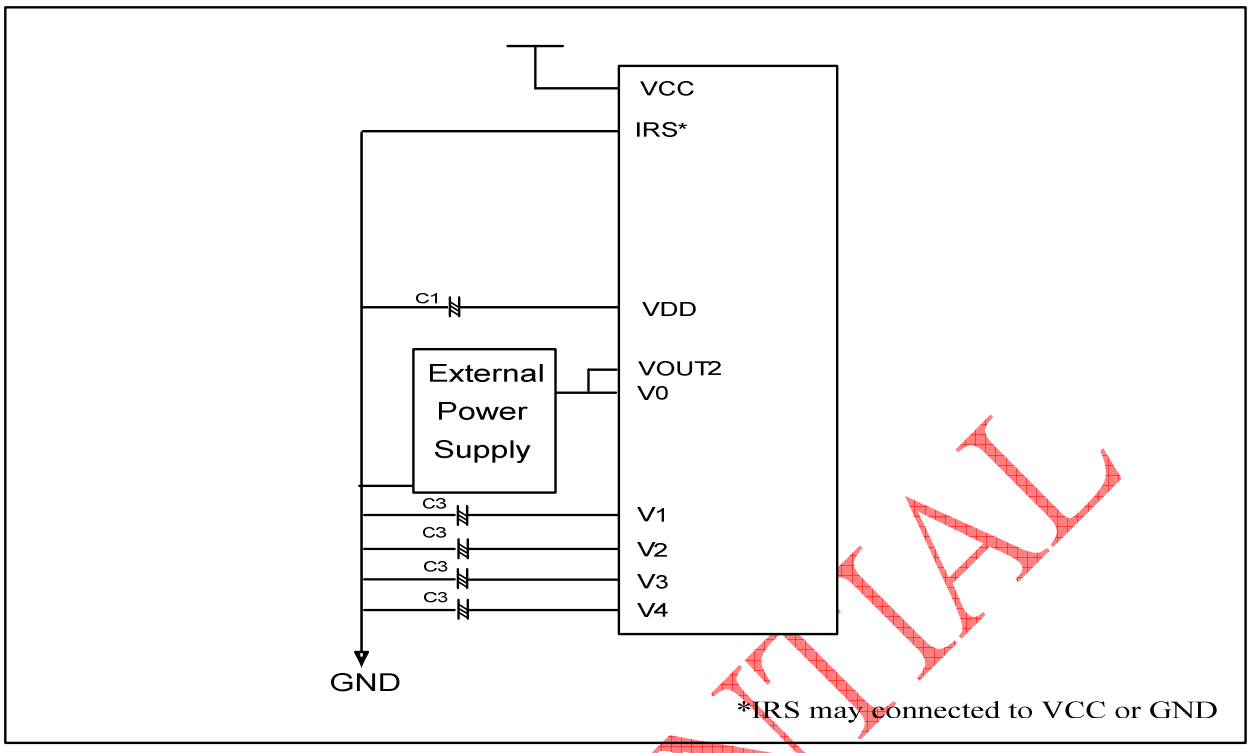


Figure 12. When Using some Internal LCD Power Circuits (V/C : OFF, V/R : OFF, V/F : ON)

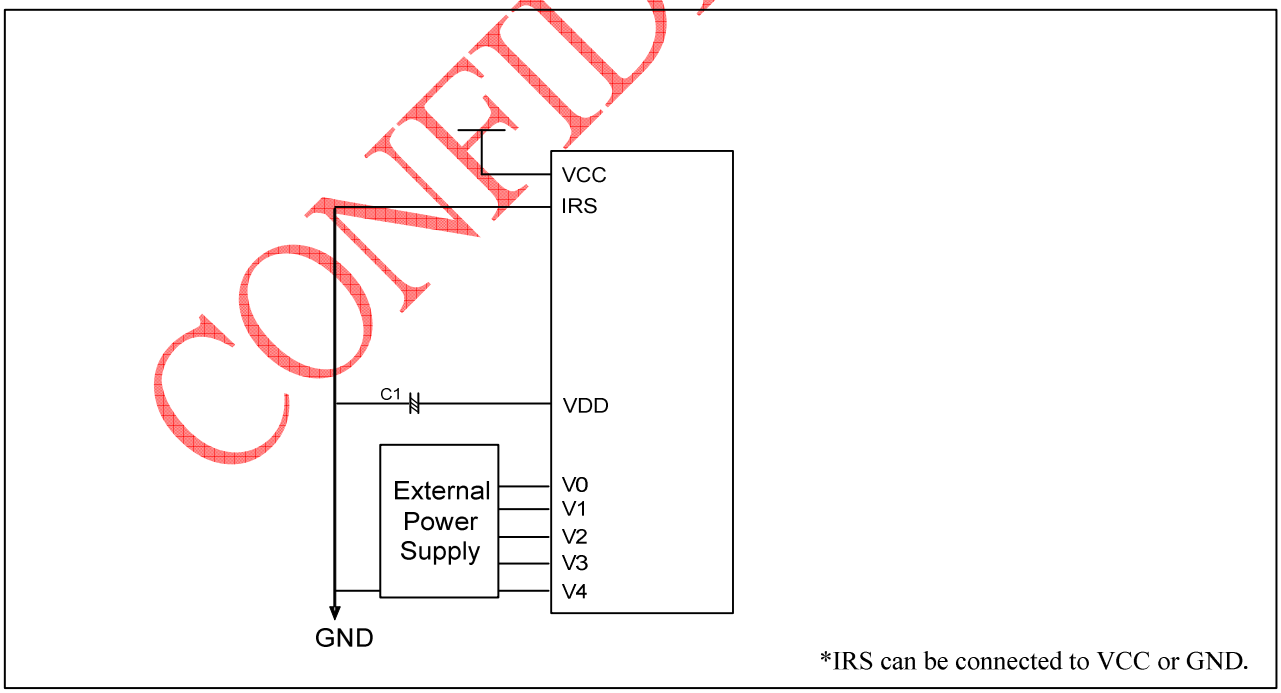


Figure 13. When Not Using any Internal LCD Power Circuits (V/C : OFF, V/R : OFF, V/F : OFF)

*C1, C2 and C3 are determined by the size of the LCD being driven, select a value that will stabilize the liquid crystal drive voltage.
*C1 = 1.0 to 4.7µF, C2 = 2.2 to 4.7µF, C3 = 0.47 to 1.0µF.

Command Table

ID	Command	R=1 W=0	RS	Upper Byte								Lower Byte							
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IR	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R01h	Driver control	0/1	1	0	0	0	0	0	0	0	0	0	0	SHL	SGS	0	0	NL1	NL0
R02h	Polarity control	0/1	1	0	0	0	0	0	0	EOR	BC	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
R03h	Power control (1)	0/1	1	0	0	0	0	0	0	0	0	0	VC	VR	VF	0	0	SLP	STB
R04h	Power control (2)	0/1	1	0	0	TC1	TC0	0	BS2	BS1	BS0	0	BT2	BT1	BT0	0	0	0	VRG
R05h	Contrast control	0/1	1	0	0	0	0	0	0	0	0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
R06h	Entry mode	0/1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	AM	ID1	ID0
R07h	Display control	0/1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	BW	REV	D
R08h	RAM Address	0/1	1	AY7	AY6	AY5	AY4	AY3	AY2	AY1	AY0	0	AX6	AX5	AX4	AX3	AX2	AX1	AX0
R09h	RAM data	0/1	1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0Ah	Starting address	0/1	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R0Dh	RAM Window H-start/end	0/1	1	0	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	0	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R0Eh	RAM Window V-start/end	0/1	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R23h	Display Mode Control	0/1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	DSPM2	DSPM1	DSPM0
R24h	Test instruction (1)	0/1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TEST
R28h	Frame Rate Control	0/1	1	0	0	0	0	0	0	0	CSEL2	CTN1	CTN0	CSEL1	CSEL0	1	0	0	0
R2Ah	Test instruction (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TEST	TEST
R30h	OTP program enable	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTE
R31h	OTP program start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PGM
R36h	Contrast offset	0/1	1	0	0	0	0	0	0	0	0	0	CTO6	CTO5	CTO4	CTO3	CTO2	CTO1	CTO0
R37h	V1/V4 level adjustment	0/1	1	0	0	0	VFR44	VFR43	VFR42	VFR41	VFR40	0	0	0	VFR14	VFR13	VFR12	VFR11	VFR10

Command Initialization

ID	Command	Initialization						
ID	Index	ID=00000000						
R01h	Driver control	SHL=0	SGS=0	NL=11				
R02h	Polarity control	EOR=0	BC=0	NW=00000000				
R03h	Power control (1)	VC=0	VR=0	VF=0	SLP=0	STB=0		
R04h	Power control (2)	TC=00	BS=000	BT=000	VRG=0			
R05h	Contrast control	CT=00000000						
R06h	Entry mode	AM=0	ID=11					
R07h	Display control	BW=0	REV=0	D=0				
R08h	RAM Address	AY=00000000	AX=0000000					
R09h	RAM data	DB=0						
R0Ah	Starting address	VL=00000000						
R0Dh	RAM Window H-start/end	HEA=1001111	HAS=0000000					
R0Eh	RAM Window V-start/end	VEA=11101111	VSA=00000000					
R23h	Display Mode control	DSPM=011						
R24h	Test instruction (1)	TEST=0						
R28h	Frame Rate control	CTN=0	CSEL=00	CSEL2=0				
R2Ah	Test instruction (2)	TEST=00						
R30h	OTP program enable	CTE=0						
R31h	OTP program start	PGM=0						
R36h	Contrast offset	CTO=0000000						
R37h	V1/V4 level adjustment	VFR4=00000	VFR1=00000					

INSTRUCTION DESCRIPTION

Index

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IR	0	0	0	0	0	0	0	0	0	0	ID							

ID Select the register are used to access by MPU, the ID provide 128 register number (00H ~ FFH), TR7707 only used 16 registers.

Driver control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
01	0	0/1	0	0	0	0	0	0	0	0	0	0	SHL	SGS	0	0	NL	

SHL This command is used to set common shift format and direction according to module.

SHL	**0**	COM1→COM2…COM239→COM240→COM1→COM2…COM239→COM240→COM1
	1	COM240→COM239…COM2→COM1→COM240→COM239…COM2→COM1→COM240

SGS Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.
SGS = 0 : normal direction (SEG1 to SEG320)
SGS = 1 : reverse direction (SEG320 to SEG1)

NL Duty Select

NL1	NL0	DUTY
0	0	1/240
0	1	1/128
1	0	1/160
1	1	NA

Polarity Control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
02	0	0/1	0	0	0	0	0	0	EOR	BC	NW							

Polarity alternating pattern select.

BC	EOR	Pattern	Description
0	X	B-pattern	Polarity alternating by frame
1	0	C-pattern	Polarity alternating by line(1~256), which is specified by NW
1	1	C-pattern	B-pattern & C-pattern EXOR to generate the alternating timing control

Power Control (1)

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
03	0	0/1	0	0	0	0	0	0	0	0	0	VC	VR	VF	0	0	SLP	STB

VC/VR/VF Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

SLP/STB The power save mode consists of the sleep and stand-by mode. The operating mode before the display data and power save activation is held in the sleep and stand-by modes, and the display data RAM can also be accessed from the MPU.

Function	SLP=1	STB=1
Display circuit	Turn-off	Turn-off
Power circuit	Turn-off	Turn-off
Oscillator	Normally	Turn-off

Power Control (2)

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
04	0	0/1	0	0	TC		0	BS			0	BT			0	0	0	VRG

Temperature coefficient curve select

TC1	TC0	V_{REF}	T.C curve
0	0	1.80v	-0.00 %/℃
0	1	1.80v	-0.05 %/℃
1	0	1.80v	-0.10 %/℃
1	1	1.80v	-0.15 %/℃

Bias select

BS2	BS1	BS0	Bias
0	0	0	1/9
0	0	1	1/10
0	1	0	1/11
0	1	1	1/12
1	0	0	1/13
1	0	1	1/14
1	1	0	1/15
1	1	1	1/16

Booster multiple select

BT2	BT1	BT0	Boost1 (Vout1)	Boost2 (Vout2)
0	0	0	Vci x 2	Vout1 x 2
0	1	0	Vci x 2	Vout1 x 3
1	0	0	Vci x 2	Vout1 x 4
1	1	0	Vci x 2	Vout1 x 5
X	X	1	NA	

Regulator gain select

VRG	V0 Voltage
0	V0 = (4 + α x 0.025) x V_{REF}
1	V0 = (8 + α x 0.025) x V_{REF}

Contrast Control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
05	0	0/1	0	0	0	0	0	0	0	0	CT							

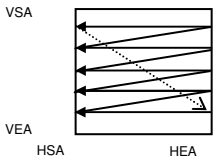
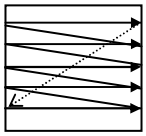
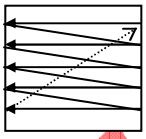
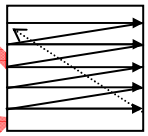
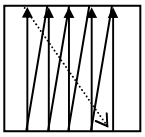
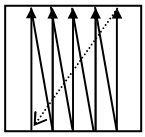
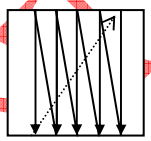
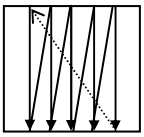
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Reference voltage Parameter (α)	V0	Contrast
0	0	0	0	0	0	0	0	0 (default)	Minimum	Low
0	0	0	0	0	0	0	1	1	:	:
:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	128	:	:
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	254	:	:
1	1	1	1	1	1	1	1	255	Maximum	High

Entry mode

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
06	0	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	AM	ID	

ID AX/AY address auto-increment/decrement control after data is written to display RAM. AX/AY address will auto back to the confront corner of the addressing window set by HEA, HSA & VEA, VSA.

AM Horizontal/Vertical mode select. When AM=0/1, the data is continuously written in horizontal/vertical direction.

	ID = "00" H: Decrement V: Decrement	ID= "01" H: Increment V: Decrement	ID = "10" H: Decrement V: Increment	ID = "11" H: Increment V: Increment
AM=0				
AM=1				

Display control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
07	0	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	BW	REV	D

BW All display shows black On/Off. When BW=1 all the display images will shows deepest grayscale.

REV Reverse display On /Off. When REV=1 all the display images will reverse the grayscale.

D This bit is used to turn on the LCD state, When D=1, LCD will be drived.

RAM address

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
08	0	0/1	AY								0	AX						

This command is used to specify a row address (AY) and column address (AX) of internal RAM. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

AY7	AY6	AY5	AY4	AY3	AY2	AY1	AY0	Row address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	1	1	0	1	1	1	0	238
1	1	1	0	1	1	1	1	239

AX6	AX5	AX4	AX3	AX2	AX1	AX0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79

RAM data

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
09	0	0/1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

This command is used to write/read data to the display RAM.
When the display RAM data is accessed, the column or row address is incremented by one. To exit the state specified with this command, input another command.

Starting address

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0A	0	0/1	0	0	0	0	0	0	0	0	VL							

VL Sets the line address of the Display RAM to determine the initial display line. The display data of the specified line address is displayed at the COM0 of the LCD panel , the range is 0 to 239.

RAM window horizontal start/end

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0D	0	0/1	0	HEA							0	HSA						

HSA/HEA Horizontal addressing window range define. HSA defines the AX starting position, HEA defines the AX ending position. When AX is automatically incremented or decremented, if AX reaches the boundary (HEA or HSA), it will automatically back to the opposite starting position.

RAM window vertical start/end

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0E	0	0/1	VEA								VSA							

VSA/VEA Vertical addressing window range define. VSA defines the AY starting position, VEA defines the AY ending position. When AY is automatically incremented or decremented, if AY reaches the boundary (VEA or VSA), it will automatically back to the opposite starting position.

Display Mode control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
23	0	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	DSPM		

DSPM It offers a flexible display type and supports a variety of display interface, the 16 gray levels are formed by pure FRC, please setup the type before display on command. see below as type selection

DSPM	Display type
011	Pure FRC (gray levels)
100	Mono

Test Instruction (1)

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
24	0	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TEST	

TEST Test function, don't use.

Frame rate control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
28	0	0/1	0	0	0	0	0	0	0	CSEL 2	CTN		CSEL		1	0	0	0

CTN/CSEL The frame rate adjust depends on duty selection(NL), CTN and CSEL, see the below mapping table.

$$f_{Frame}(Hz) = \frac{f_{osc}}{duty \times factor \times 64}$$

CSEL2	CSEL	factor
0	00	1.5
0	01	2.0
0	10	2.5
0	11	3.0
1	xx	1.0

Test Instruction (2)

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
2A	0	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TEST

TEST Test function, don't use.

OTP program enable

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTE

CTE It identified contrast offset parameters for OTP to program.

OTP program start

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PGM

PGM When PGM enable, the OTP control logic enters the programming state and the BUSY flag immediately toggle to high until program done, the duration of program about 10ms

Electronic contrast offset adjustment

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
36	0	0/1	0	0	0	0	0	0	0	0	0	CTO						

CTO this offset parameters that is more flexible to adjust the electronic contrast level, the total of 128 steps can cover the range from +63 to -64, the actual contrast level as CT (base level) + CTO (offset level). **Notice that the CTO only supply for two times to program, when it was programmed, the last contents of CTO was ignored.**

CTO6	CTO5	CTO4	CTO3	CTO2	CTO1	CTO0	Offset level
0	1	1	1	1	1	1	+63
0	1	1	1	1	1	0	+62
:	:	:	:	:	:	:	:
0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	-1
:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	-63
1	0	0	0	0	0	0	-64

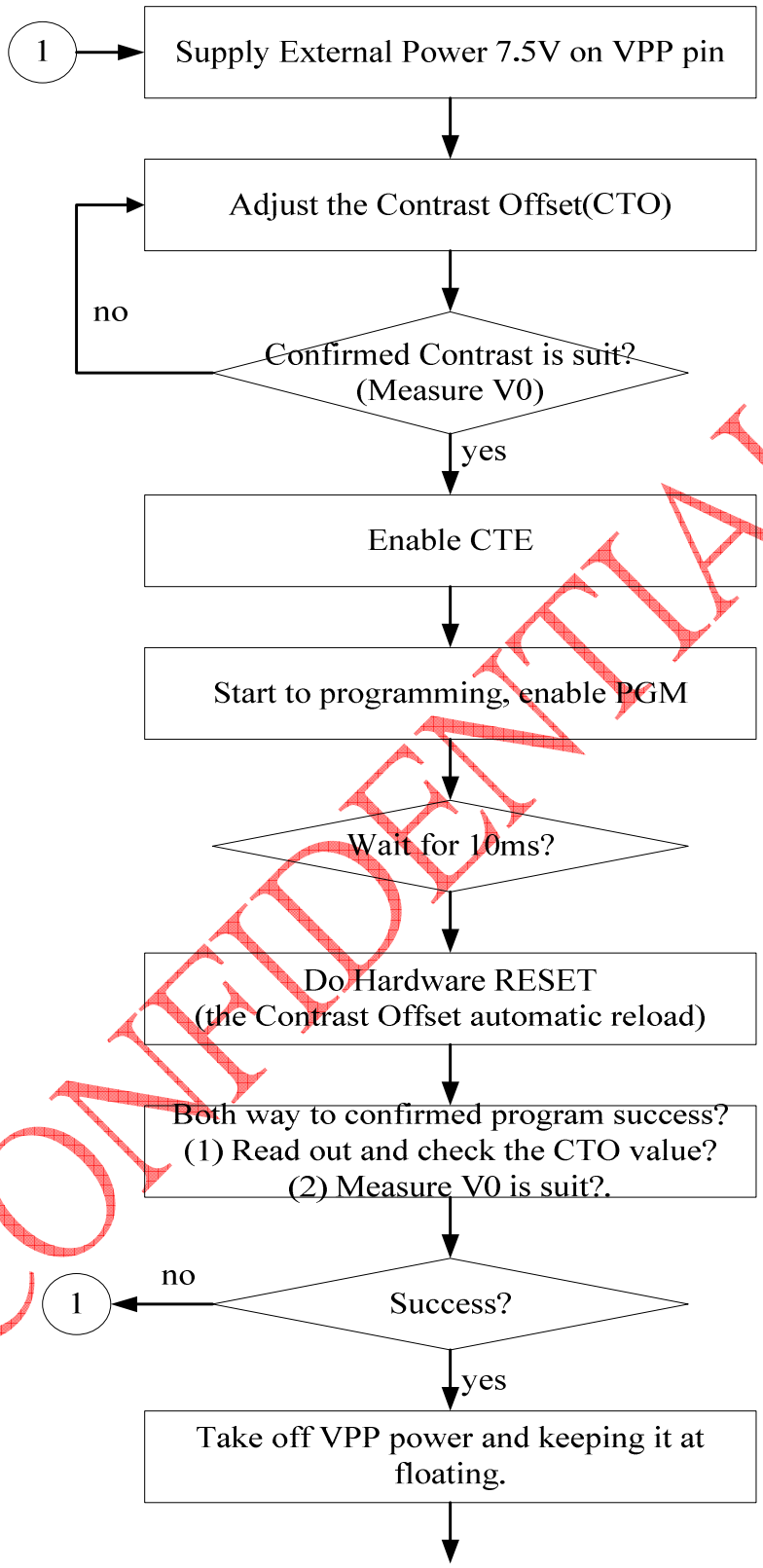
V1/V4 level adjustment

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
37	0	0	0	0	0	VFR4					0	0	0	VFR1				

VFR1/VFR4 The TR7707 provides additional V1 and V4 level adjustment parameters (VFR1 and VFR4) for user to fine tune the V1 and V4 output levels. It can be used to improve the display quality and reduce the cross-talk phenomenon.

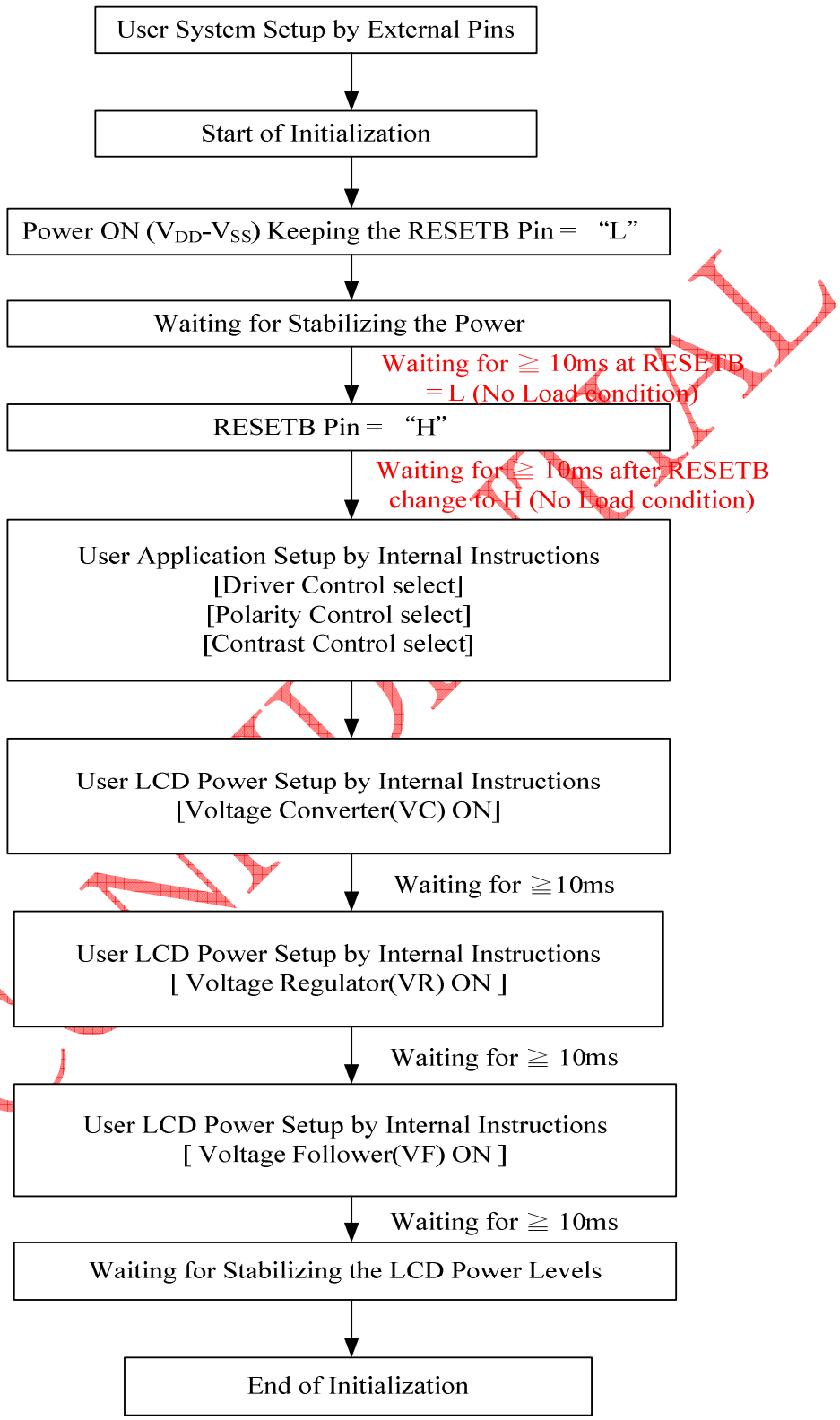
VFR4[4:0] / VFR1[4:0]					V1/V4	VFR4[4:0] / VFR1[4:0]					V1 /V4
1	0	0	0	0	+0mV	0	0	0	0	0	-0mV
1	0	0	0	1	+25mV	0	0	0	0	1	-25mV
1	0	0	1	0	+50mV	0	0	0	1	0	-50mV
1	0	0	1	1	+75mV	0	0	0	1	1	-75mV
1	0	1	0	0	+100mV	0	0	1	0	0	-100mV
1	0	1	0	1	+125mV	0	0	1	0	1	-125mV
1	0	1	1	0	+150mV	0	0	1	1	0	-150mV
1	0	1	1	1	+175mV	0	0	1	1	1	-175mV
1	1	0	0	0	+200mV	0	1	0	0	0	-200mV
1	1	0	0	1	+225mV	0	1	0	0	1	-225mV
1	1	0	1	0	+250mV	0	1	0	1	0	-250mV
1	1	0	1	1	+275mV	0	1	0	1	1	-275mV
1	1	1	0	0	+300mV	0	1	1	0	0	-300mV
1	1	1	0	1	+325mV	0	1	1	0	1	-325mV
1	1	1	1	0	+350mV	0	1	1	1	0	-350mV
1	1	1	1	1	+375mV	0	1	1	1	1	-375mV

OTP Programming Flow

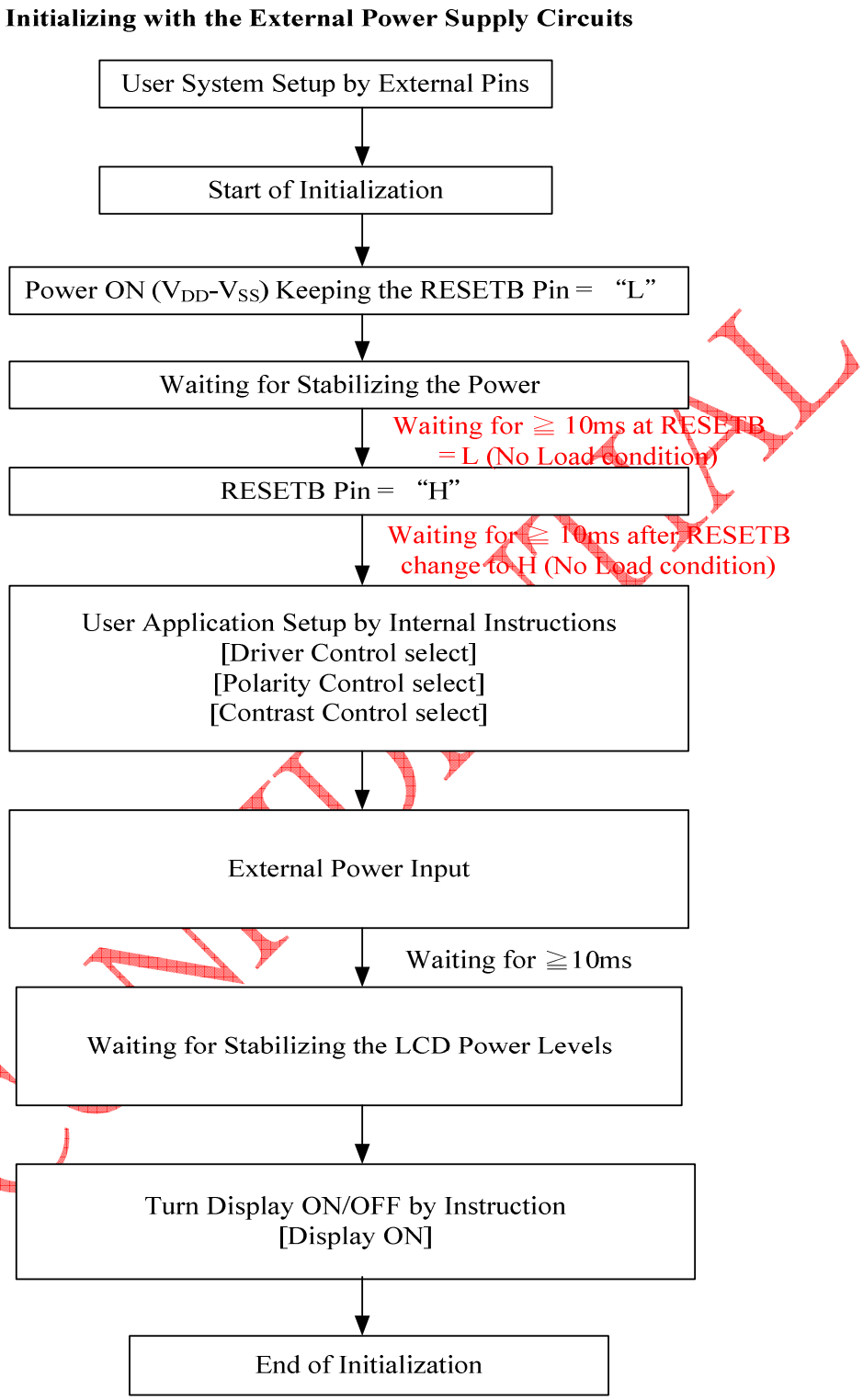


Power On Sequence (1)

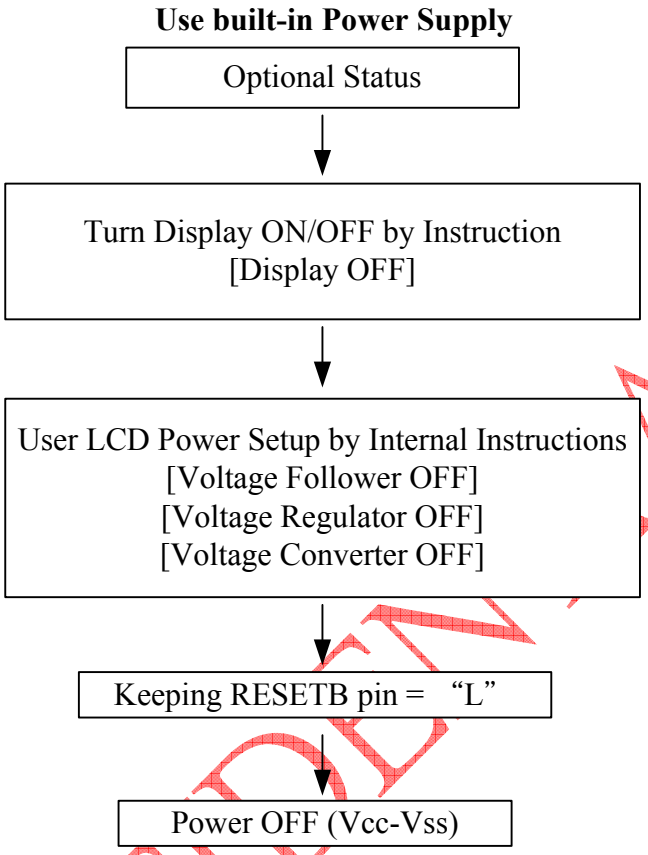
Initializing with the Built-in Power Supply Circuits



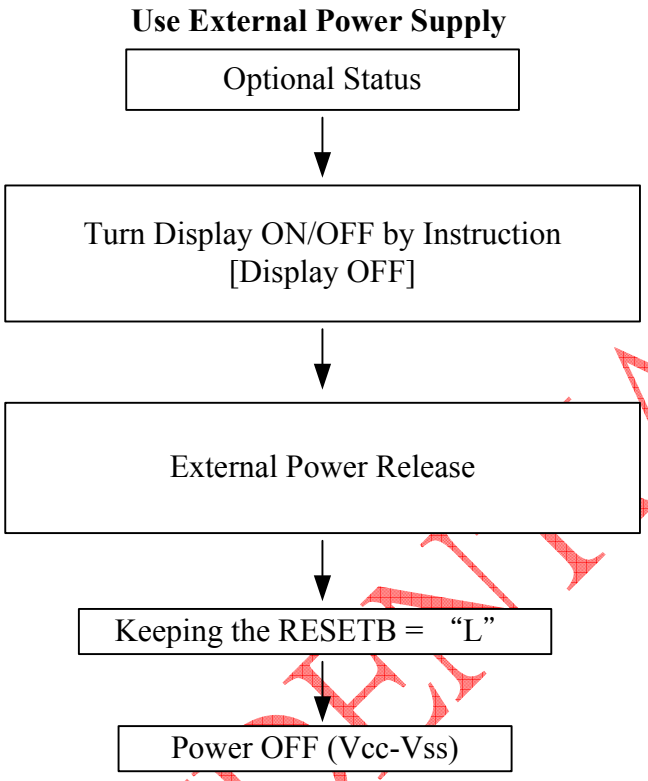
Power On Sequence (2)



Power Off Sequence (1)



Power Off Sequence (2)



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	VCC	-0.3 to +8.0	V
	V0/VOUT	-0.3 to +40	V
	V1/V2/V3/V4	-0.3 to V0	V
Operating temperature range	TOPR	-40 to +85	℃
Storage temperature range	TSTR	-55 to +110	℃

NOTES

1. VCC and VOUT are measured based on GND = 0V
2. Voltages V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ GND must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.
4. It is desirable to use this LSI under electrical characteristic conditions during general operation, otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERS

(Ta = -30 ~ 80℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin
Operating Voltage	V_{CC}		2.4	-	3.3	V	VCC
Input voltage	V_{IH}		0.8 * V_{CC}	-	V_{CC}	V	RESETB, IM2-0, DB15-0, EWRB_SCL, RWRDB_SDA, RS, CSB, IRS, CLS, REGON
	V_{IL}		GND	-	0.2 * V_{CC}		
Output voltage	V_{OH}	I_{OH} = -0.4mA	0.8 * V_{CC}	-	V_{CC}	V	DB15-0
	V_{OL}	I_{OL} = 0.4mA	GND	-	0.2 * V_{CC}		
Input leakage current	I_{IL}	V_{IN} = V_{CC} or GND	-1.0		1.0	µA	RESETB, IM2-0, DB15-0, EWRB_SCL, RWRDB_SDA, RS, CSB, IRS, CLS, REGON
LCD driver ON Resistance	R_{ON}				2	kΩ	COMn, SEGn (*1)
Oscillator frequency	Fosc	CLS = 1, CTN = 00	1440	1800	2160	KHz	
		CLS = 1, CTN = 01	2160	2700	3240		
		CLS = 1, CTN = 10	2800	3500	4200		
		CLS = 1, CTN = 11	3440	4300	5100		
Voltage converter input voltage	VCI		2.4	-	3.3	V	VCI (*2)
Voltage converter operating voltage	VOUT2			-	32	V	VOUT2
Reference voltage	VREF	VCC = 3.0v TC=00	1.7	1.8	1.9	V	VREF (Ta=25℃)
		VCC = 3.0v TC=01	1.7	1.8	1.9		
		VCC = 3.0v TC=10	1.7	1.8	1.9		
		VCC = 3.0v TC=11	1.7	1.8	1.9		
Driver Operating Voltage	V0			-	28	V	V0
Dynamic current consumption	Idy	V_{CC} = 3.0V (VCI = Vcc, x10 boost) V0 – GND = 25.0V 1/240 duty ratio Internal Power on CLS = 1, CTN = 00 Display pattern Checker	-	-	3	mA	COMn, SEGn floating (no load) (Ta=25℃)
Static current consumption	Istat	V_{CC} = 3.0V Display OFF Power OFF OSC OFF	-	-	20	µA	(Ta=25℃)

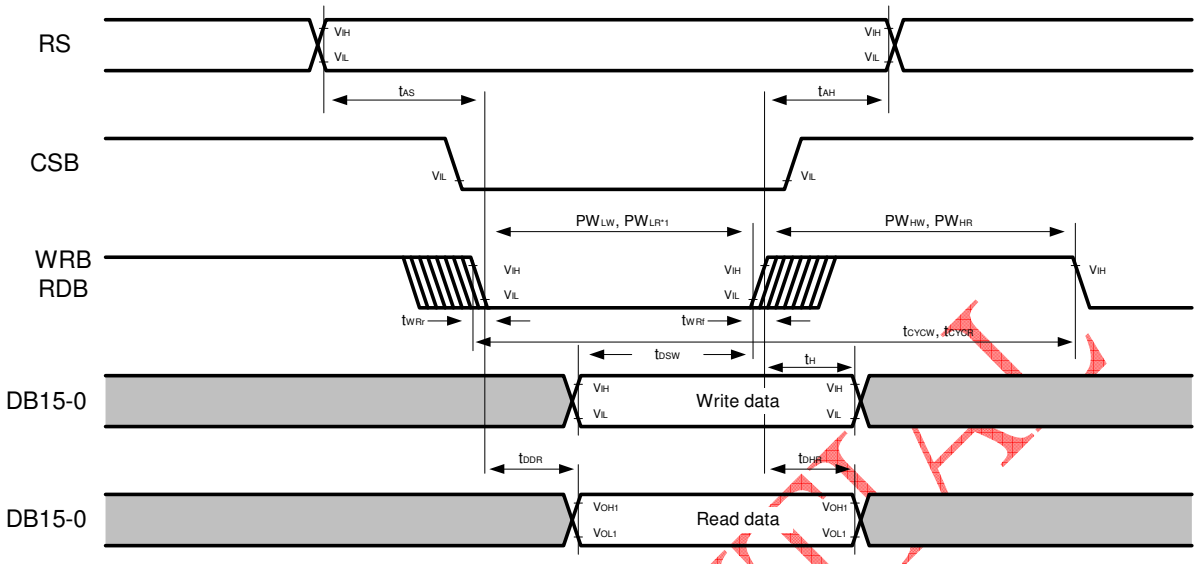
Note:

(1) Resistance value when +/- 0.1mA is applied during the ON status of the output pins SEGn & COMn
R_{ON} = ΔV / 0.1 (KΩ) (ΔV: voltage change when +/- 0.1mA is applied)

(2) VCI x Boost gain must lower than 32.0V (VOUT2).

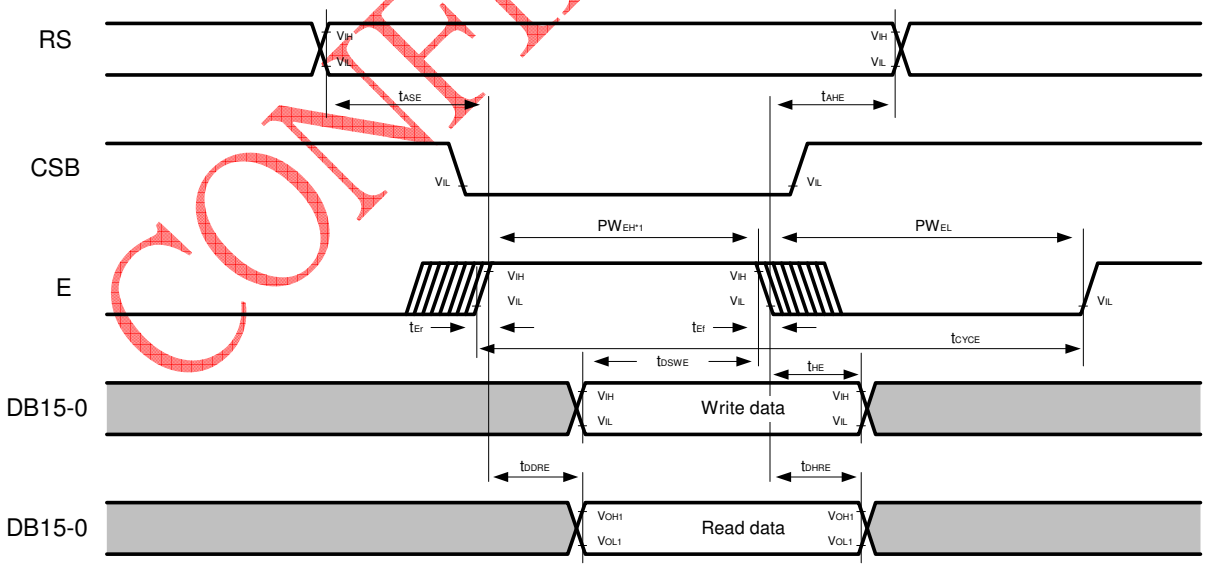
AC CHARACTERS

80-System Bus Operation



Note : PW_{LW} and PW_{HR} are specified in the overlapped period when CSB is low and WRB or RDB is low.

68-System Bus Operation



Note : PW_{EH} is specified in the overlapped period when CSB is low and E is high.

80-System Bus Interface Timing Characteristics

Vcc = 2.4 to 3.3 V **Temp = -30 to +80℃**

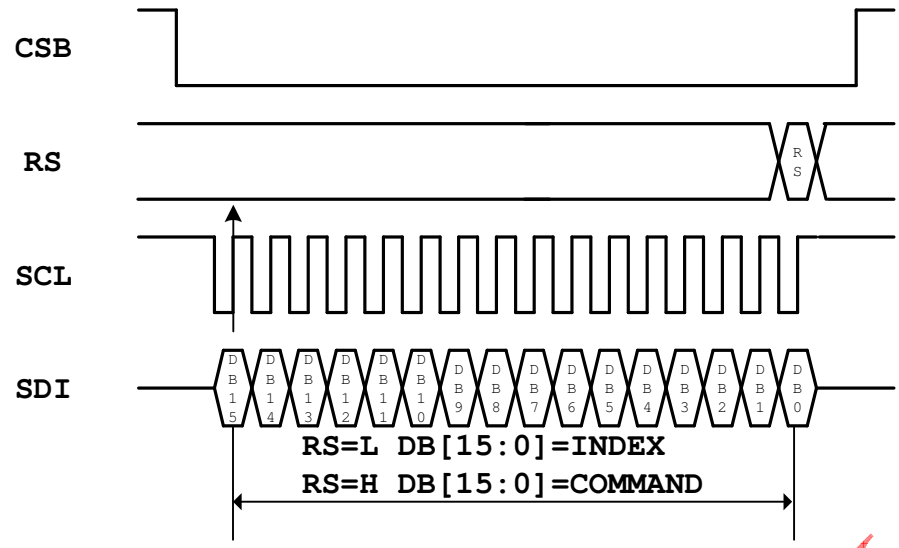
Item		Symbol	Min	Typ	Max	Unit
Bus cycle time	Write	t_{CYCW}	350			ns
	Read	t_{CYCR}	500			ns
Write low-level pulse width		PW_{LW}	170			ns
Read low-level pulse width		PW_{LR}	250			ns
Write high-level pulse width		PW_{HW}	180			ns
Read high-level pulse width		PW_{HR}	250			ns
Write/Read rise/fall time		t_{WRr} , $_{WRf}$			15	ns
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50			ns
Address hold time		t_{AH}	20			ns
Write data setup time		t_{DSW}	70			ns
Write data hold time		t_{H}	60			ns
Read data delay time		t_{DDR}			200	ns
Read data hold time		t_{DHR}	5			ns

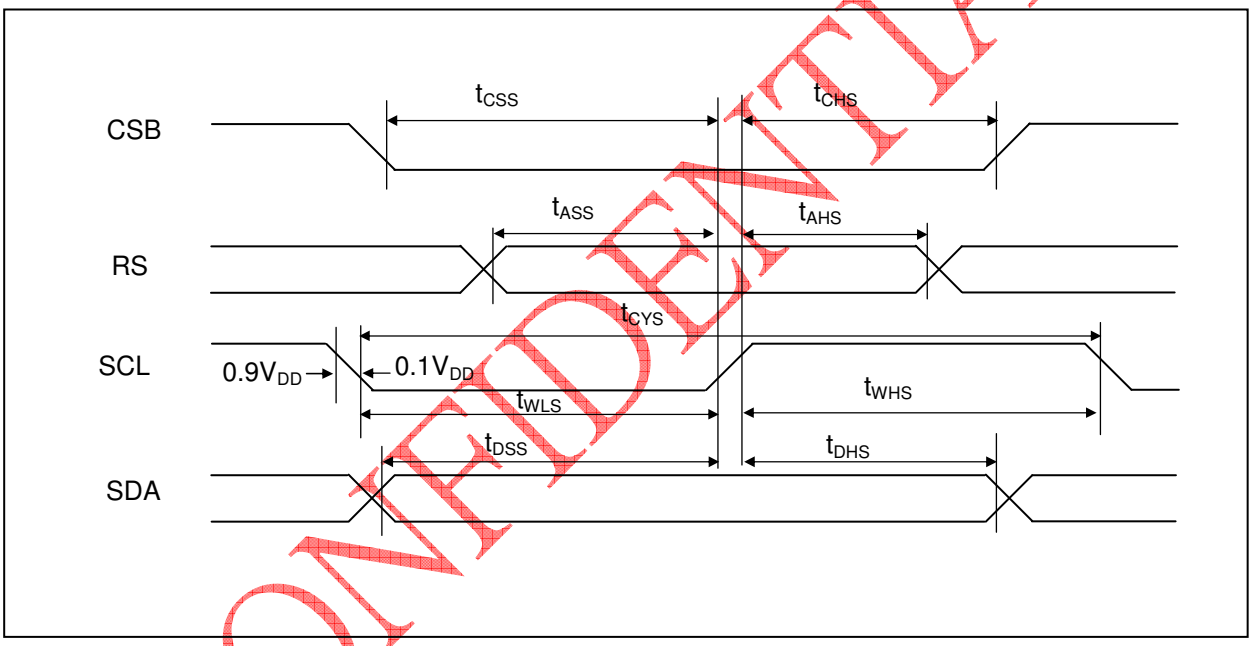
68-System Bus Interface Timing Characteristics

Vcc = 2.4 to 3.3 V **Temp = -30 to +80℃**

Item		Symbol	Min	Typ	Max	Unit
Bus cycle time	Write	t_{CYCE}	350			ns
	Read	t_{CYCE}	500			ns
Enable high-level pulse width	Write	PW_{EH}	170			ns
	Read	PW_{EH}	250			ns
Enable low-level pulse width	Write	PW_{EL}	180			ns
	Read	PW_{EL}	250			ns
Enable rise/fall tiem		t_{WRr} , $_{WRf}$			15	ns
Setup time (RS to CS*, WR*, RD*)		t_{ASE}	50			ns
Address hold time		t_{AHE}	20			ns
Write data setup time		t_{DSWE}	70			ns
Write data hold time		t_{HE}	60			ns
Read data delay time		t_{DDRE}			200	ns
Read data hold time		t_{DHRE}	5			ns

4 Line Serial Interface Timing Characteristics

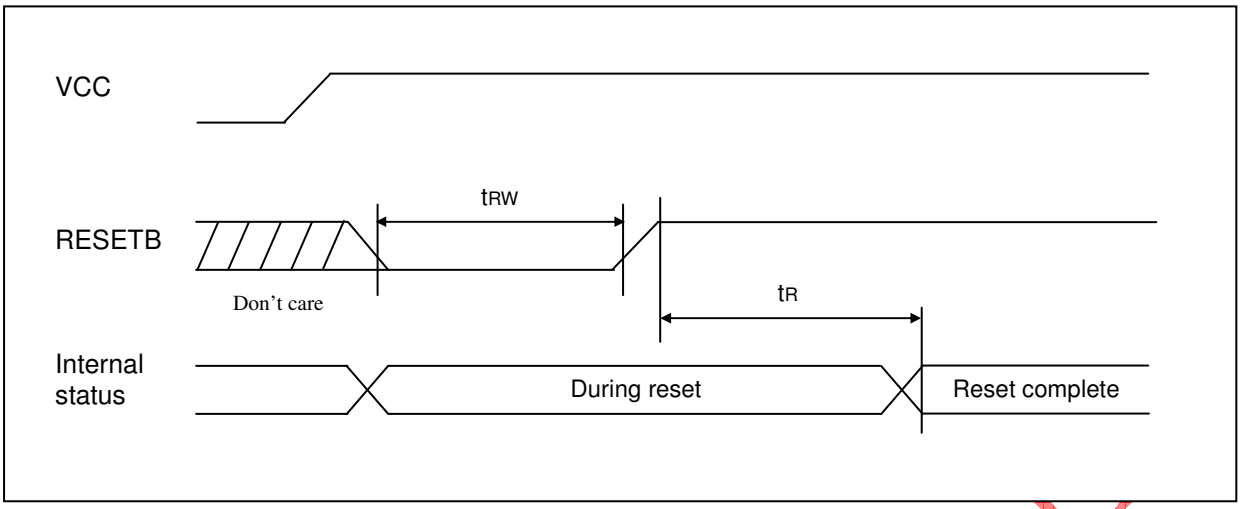




VCC = 2.4 to 3.3V **Temp = -30 to +80℃**

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	SCL	t_{CYS}	250	-	-	ns	
SCLK high pulse width	SCL	t_{WHS}	125	-	-		
SCLK low pulse width	SCL	t_{WLS}	125	-	-		
RS setup time	RS	t_{ASS}	110	-	-	ns	
RS hold time	RS	t_{AHS}	110	-	-		
Data setup time	SDA	t_{DSS}	110	-	-	ns	
Data hold time	SDA	t_{DHS}	110	-	-		
CSB setup time	CSB	t_{CSS}	110	-	-	ns	
CSB hold time	CSB	t_{CHS}	110	-	-		

Reset Input Timing

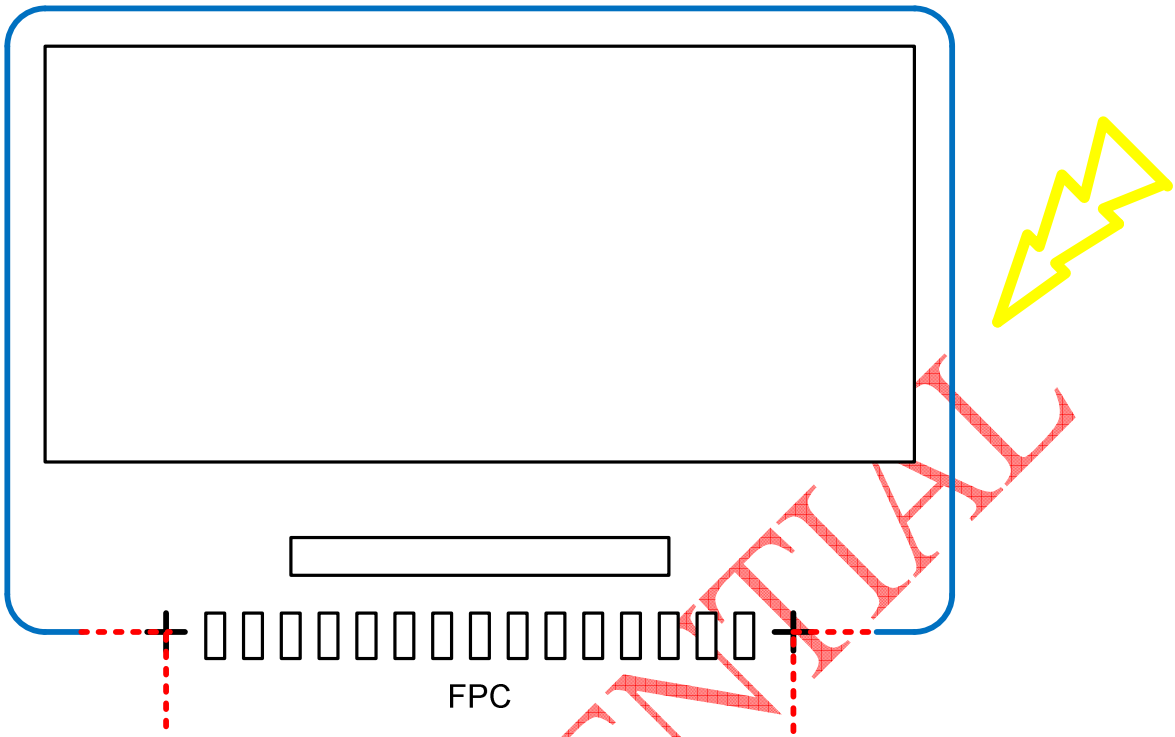


VCC = 2.4 to 3.3V **Temp = -30 to +80℃**

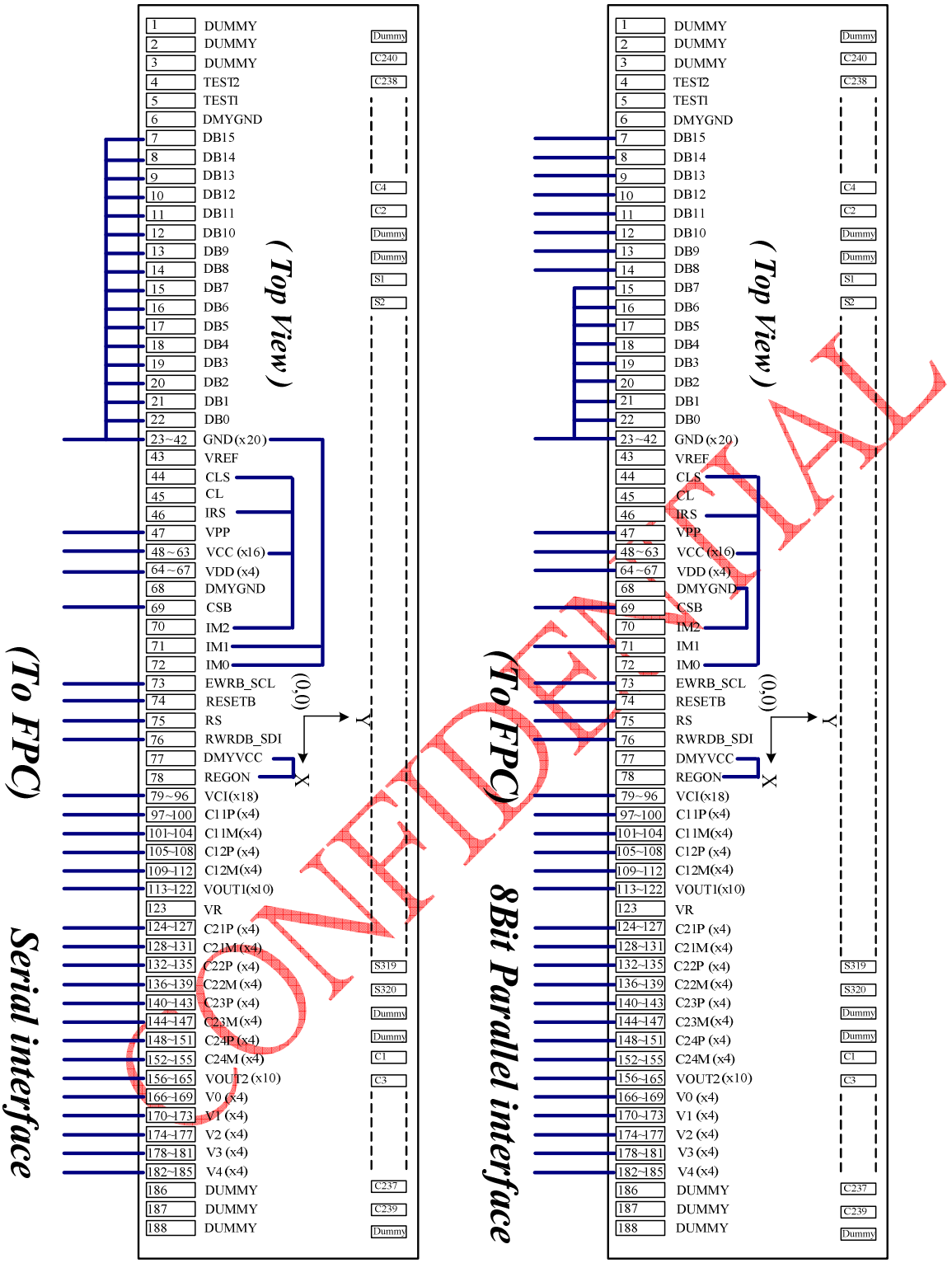
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	2	-	-	us	
Reset time	-	t_R	10	-	-	ms	

Application Note

1. Add ESD protection ring

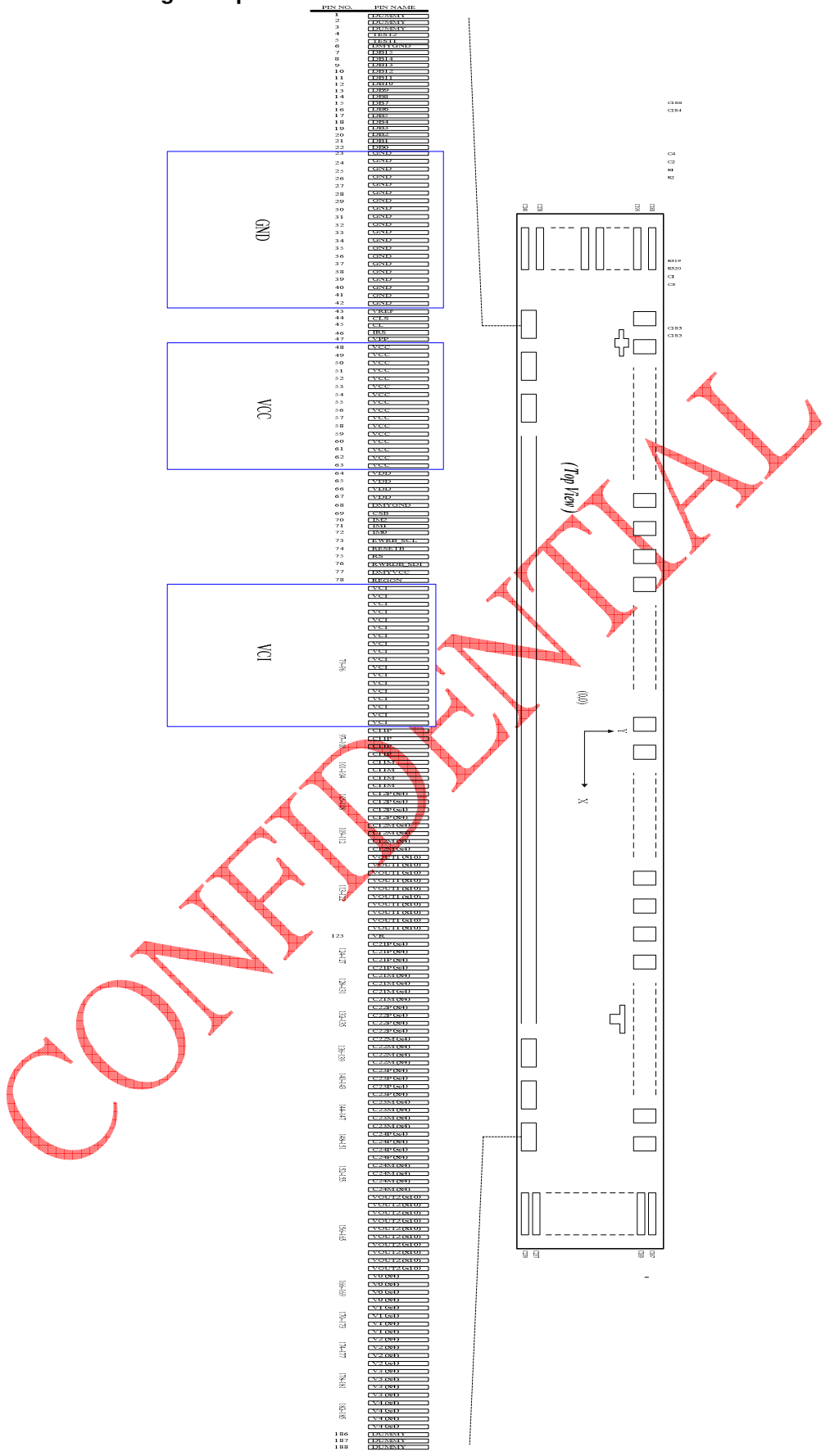


2. ITO connection example



- **ITO Resister Limitation**
  - **VCC,VCI,GND < 50ohm**
  - **VDD,V0,V1,V2,V3,V4,VOUT1,VOUT2,C11P~C12P,C11M~C12M,C21P~C24P,C21M~C24M< 100 ohm**
  - **RSTB < 10K ohm**
  - **Other < 500 ohm**

3. Power system ITO routing example



- Please make sure the “VCC”, “GND”, “VCI” main power ITO resistance as small as possi bl