ST7793

240RGB x 432 dot 262 Color with Frame Memory Single-Chip TFT Controller/Driver

Datasheet

Version 1.2
2014/08

Sitronix Technology Corporation

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1 GENERAL DESCRIPTION

The ST7793 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 720 source lines and 432 gate lines driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts 8-bit/9-bit/16-bit/18-bit parallel interface, SPI, and MDDI. Display data can be stored in the on-chip display data RAM of 240x432x18 bits. It can perform display data RAM read-/write-operation with no external clock to minimize power consumption. In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with fewest components.

2 FEATURES

- Single chip TFT-LCD Controller/Driver with On-chip Frame Memory
- Display Resolution: 240*RGB (H) *432(V)
- Frame Memory Size: 240 x 432 x 18-bit = 1,866,240 bits
- LCD Driver Output Circuits
  - Source Outputs: 240 RGB Channels
  - Gate Outputs: 432 Channels
  - Common Electrode Output
- Display Colors (Color Mode)
  - Full Color: 262K, RGB=(666) max., Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- Programmable Pixel Color Format (Color Depth) for Various Display Data Input Format
  - 16-bit/pixel: RGB=(565)
  - 18-bit/pixel: RGB=(666)
- Interface
  - Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit, and 18-bit)
  - 16/18 RGB Interface (VSYNCX, HSYNCX, DOTCLK, ENABLE, DB[17:0])
  - Serial Peripheral Interface (SPI Interface)
  - VSYNC Interface (8080-series MCU Interface + VSYNCX)
  - FMARK Interface (8080-series MCU Interface + FMARK)
  - MDDI (Type 1)
- Display Features
  - Partial Display Function
  - 8-color Display Function
  - Vertical Scroll Function
- Support LC Type Option
  - MVA LC Type
  - Transflective LC Type
  - Transmissive LC Type
- On Chip Build-In Circuits
  - DC/DC Converter
  - Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
  - Internal Oscillator for Display Clock Generation
  - Timing Controller
- Build-In NV Memory for LCD Initial Register Setting
  - 8-bit for ID

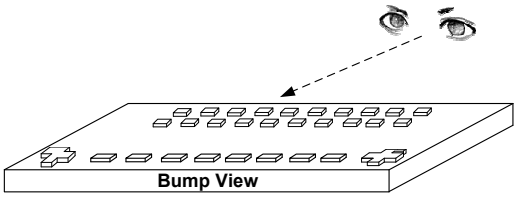
- 7-bit for flicker adjustment

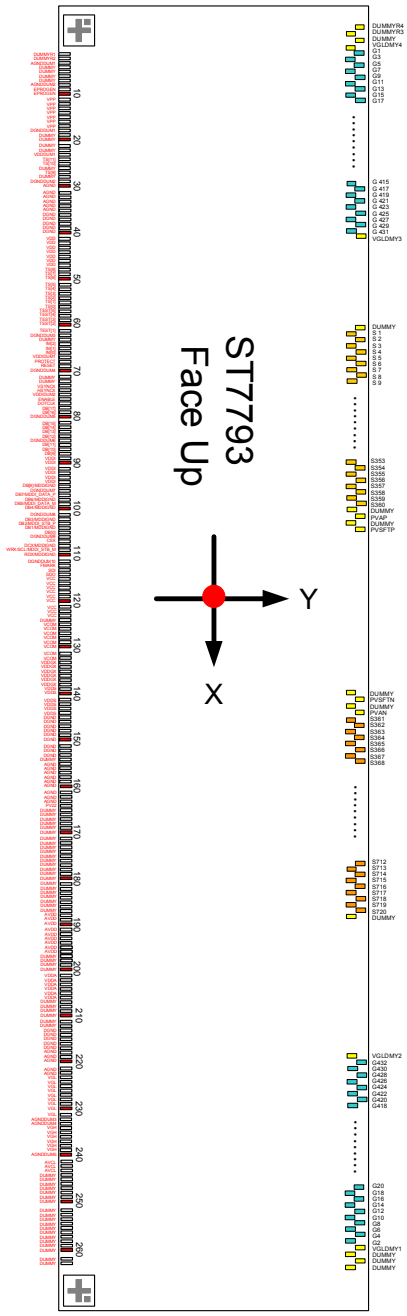
- Driving Algorithm
  - Dot Inversion
  - Column Inversion
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ VDD
  - Voltage for Digital Circuit (VDD to DGND): 2.5V ~ 3.3V
  - Voltage for Analog Circuit (VDDA to AGND): 2.5V ~ 3.3V
- On-Chip Power System
  - Source Voltage: +6.4 ~ -4.2
  - VCOM Level: AGND
  - Gate Driver HIGH Level (VGH to AGND): +12.16V ~ +15.05V
  - Gate Driver LOW Level (VGL to AGND): -12.37V ~ -7.7V
  - Max. VGH – VGL: 27.4V
- Optimized layout for COG Assembly
- Operate temperature range: −30ºC to +85 ºC
- Lower Power Consumption

3 PAD ARRANGEMENT

3.1.. Output Bump Dimension

Au bump height	9 μm
Au bump size	15μmx100μm Gate : G1~G432 Source : S1~S720 (Pad263 to Pad1434)
	50μmx90μm (Pad1 to Pad262)

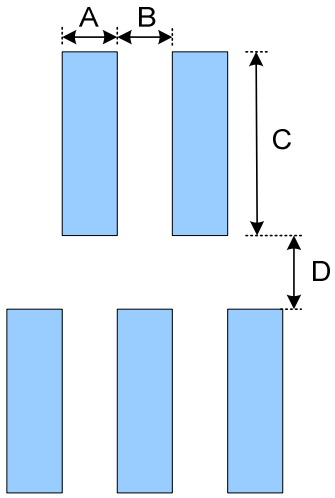




3.2.. Bump Dimension

- **Output Pads**

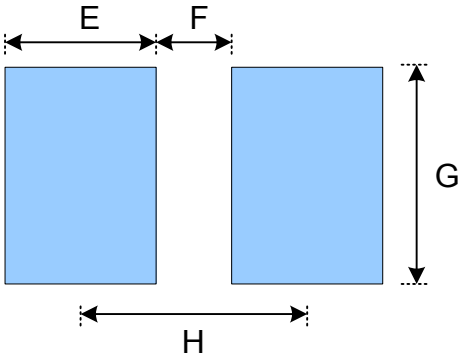
  Pad No.263~1434



Symbol	Item	Size
A	Bump Width	15 um
B	Bump Gap 1 (Horizontal)	15 um
C	Bump Height	100 um
D	Bump Gap 2 (Vertical)	19 um

- **Input Pads**

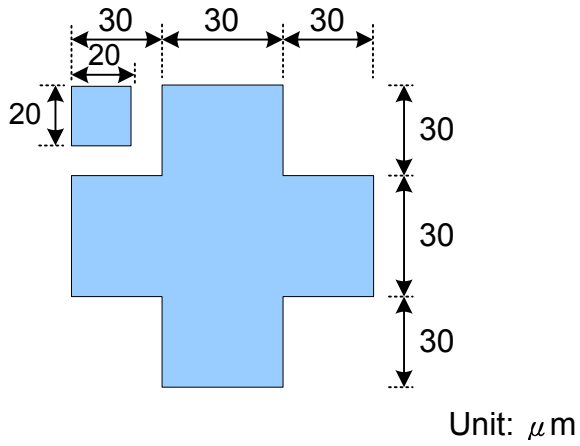
  Pad No.1~262



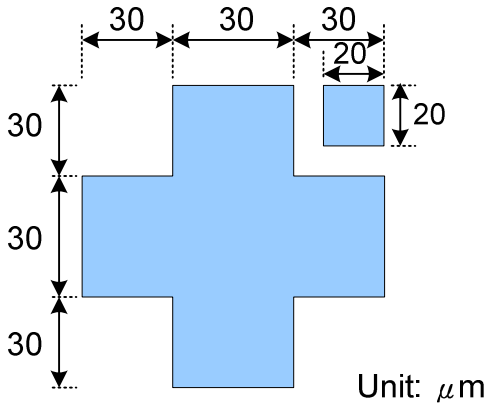
Symbol	Item	Size
E	Bump Width	50 um
F	Bump Gap	20 um
G	Bump Height	90 um
H	Bump Pitch	70 um

3.3.. Alignment Mark Dimension

- **Alignment Mark: A1(X,Y)=(-9381,-208)**



- **Alignment Mark: A2(X,Y)=(9381,-208)**



3.4.. Chip Information

Chip size	19030μm x 837μm
Chip thickness	280μm
Pad Location	Pad center
Coordinate Origin	Chip center

4 PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DUMMYR1	-9135	-301	34	AGND	-6825	-301
2	DUMMYR2	-9065	-301	35	AGND	-6755	-301
3	AGNDDUM1	-8995	-301	36	DGND	-6685	-301
4	DUMMY	-8925	-301	37	DGND	-6615	-301
5	DUMMY	-8855	-301	38	DGND	-6545	-301
6	DUMMY	-8785	-301	39	DGND	-6475	-301
7	DUMMY	-8715	-301	40	DGND	-6405	-301
8	AGNDDUM2	-8645	-301	41	VDD	-6335	-301
9	EPROGEN	-8575	-301	42	VDD	-6265	-301
10	EPROGEN	-8505	-301	43	VDD	-6195	-301
11	VPP	-8435	-301	44	VDD	-6125	-301
12	VPP	-8365	-301	45	VDD	-6055	-301
13	VPP	-8295	-301	46	VDD	-5985	-301
14	VPP	-8225	-301	47	VDD	-5915	-301
15	VPP	-8155	-301	48	TS[8]	-5845	-301
16	VPP	-8085	-301	49	TS[7]	-5775	-301
17	VPP	-8015	-301	50	TS[6]	-5705	-301
18	DGNDDUM1	-7945	-301	51	TS[5]	-5635	-301
19	DUMMY	-7875	-301	52	TS[4]	-5565	-301
20	DUMMY	-7805	-301	53	TS[3]	-5495	-301
21	DUMMY	-7735	-301	54	TS[2]	-5425	-301
22	DUMMY	-7665	-301	55	TS[1]	-5355	-301
23	VDDDUM1	-7595	-301	56	TS[0]	-5285	-301
24	TS[11]	-7525	-301	57	TEST[5]	-5215	-301
25	TS[10]	-7455	-301	58	TEST[4]	-5145	-301
26	DUMMY	-7385	-301	59	TEST[3]	-5075	-301
27	TS[9]	-7315	-301	60	TEST[2]	-5005	-301
28	DUMMY	-7245	-301	61	TEST[1]	-4935	-301
29	DGNDDUM2	-7175	-301	62	DGNDDUM3	-4865	-301
30	AGND	-7105	-301	63	DUMMY	-4795	-301
31	AGND	-7035	-301	64	IM2	-4725	-301
32	AGND	-6965	-301	65	IM1	-4655	-301
33	AGND	-6895	-301	66	IM0	-4585	-301

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	VDDIDUM1	-4515	-301	**101**	DGNDDUM8	-2135	-301
68	PROTECT	-4445	-301	**102**	DB[3]/MDDIGND	-2065	-301
69	RESET	-4375	-301	**103**	DB[2]/MDDI_STB_P	-1995	-301
70	DGNDDUM4	-4305	-301	**104**	DB[1]/MDDIGND	-1925	-301
71	DUMMY	-4235	-301	**105**	DB[0]	-1855	-301
72	DUMMY	-4165	-301	**106**	DGNDDUM9	-1785	-301
73	VSYNCX	-4095	-301	**107**	CSX	-1715	-301
74	HSYNCX	-4025	-301	**108**	DCX/MDDIGND	-1645	-301
75	VDDIDUM2	-3955	-301	**109**	WRX/SCL/MDDI_STB_M	-1575	-301
76	ENABLE	-3885	-301	**110**	RDX/MDDIGND	-1505	-301
77	DOTCLK	-3815	-301	**111**	DGNDDUM10	-1435	-301
78	DB[17]	-3745	-301	**112**	FMARK	-1365	-301
79	DB[16]	-3675	-301	**113**	SDI	-1295	-301
80	DGNDDUM5	-3605	-301	**114**	SDO	-1225	-301
81	DB[15]	-3535	-301	**115**	VCC	-1155	-301
82	DB[14]	-3465	-301	**116**	VCC	-1085	-301
83	DB[13]	-3395	-301	**117**	VCC	-1015	-301
84	DB[12]	-3325	-301	**118**	VCC	-945	-301
85	DGNDDUM6	-3255	-301	**119**	VCC	-875	-301
86	DB[11]	-3185	-301	**120**	VCC	-805	-301
87	DB[10]	-3115	-301	**121**	VCC	-735	-301
88	DB[9]	-3045	-301	**122**	VCC	-665	-301
89	VDDI	-2975	-301	**123**	VCC	-595	-301
90	VDDI	-2905	-301	**124**	DUMMY	-525	-301
91	VDDI	-2835	-301	**125**	VCOM	-455	-301
92	VDDI	-2765	-301	**126**	VCOM	-385	-301
93	VDDI	-2695	-301	**127**	VCOM	-315	-301
94	VDDI	-2625	-301	**128**	VCOM	-245	-301
95	DB[8]/MDDIGND	-2555	-301	**129**	VCOM	-175	-301
96	DGNDDUM7	-2485	-301	**130**	VCOM	-105	-301
97	DB[7]/MDDI_DATA_P	-2415	-301	**131**	VCOM	-35	-301
98	DB[6]/MDDIGND	-2345	-301	**132**	VCOM	35	-301
99	DB[5]/MDDI_DATA_M	-2275	-301	**133**	VDDGX	105	-301
100	DB[4]/MDDIGND	-2205	-301	**134**	VDDGX	175	-301

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
135	VDDGX	245	-301	**169**	DUMMY	2625	-301
136	VDDGX	315	-301	**170**	DUMMY	2695	-301
137	VDDGX	385	-301	**171**	DUMMY	2765	-301
138	VDDGX	455	-301	**172**	DUMMY	2835	-301
139	VDDS	525	-301	**173**	DUMMY	2905	-301
140	VDDS	595	-301	**174**	DUMMY	2975	-301
141	VDDS	665	-301	**175**	DUMMY	3045	-301
142	VDDS	735	-301	**176**	DUMMY	3115	-301
143	VDDS	805	-301	**177**	DUMMY	3185	-301
144	VDDS	875	-301	**178**	DUMMY	3255	-301
145	DGND	945	-301	**179**	DUMMY	3325	-301
146	DGND	1015	-301	**180**	DUMMY	3395	-301
147	DGND	1085	-301	**181**	DUMMY	3465	-301
148	DGND	1155	-301	**182**	DUMMY	3535	-301
149	DGND	1225	-301	**183**	DUMMY	3605	-301
150	DGND	1295	-301	**184**	DUMMY	3675	-301
151	DGND	1365	-301	**185**	DUMMY	3745	-301
152	DGND	1435	-301	**186**	DUMMY	3815	-301
153	DGND	1505	-301	**187**	DUMMY	3885	-301
154	DUMMY	1575	-301	**188**	AVDD	3955	-301
155	AGND	1645	-301	**189**	AVDD	4025	-301
156	AGND	1715	-301	**190**	AVDD	4095	-301
157	AGND	1785	-301	**191**	AVDD	4165	-301
158	AGND	1855	-301	**192**	AVDD	4235	-301
159	AGND	1925	-301	**193**	AVDD	4305	-301
160	AGND	1995	-301	**194**	AVDD	4375	-301
161	AGND	2065	-301	**195**	AVDD	4445	-301
162	AGND	2135	-301	**196**	AVDD	4515	-301
163	AGND	2205	-301	**197**	DUMMY	4585	-301
164	PV22	2275	-301	**198**	DUMMY	4655	-301
165	DUMMY	2345	-301	**199**	DUMMY	4725	-301
166	DUMMY	2415	-301	**200**	DUMMY	4795	-301
167	DUMMY	2485	-301	**201**	VDDA	4865	-301
168	DUMMY	2555	-301	**202**	VDDA	4935	-301

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
203	VDDA	5005	-301	**237**	VGH	7385	-301
204	VDDA	5075	-301	**238**	VGH	7455	-301
205	VDDA	5145	-301	**239**	VGH	7525	-301
206	VDDA	5215	-301	**240**	AGNDDUM5	7595	-301
207	DUMMY	5285	-301	**241**	AVCL	7665	-301
208	DUMMY	5355	-301	**242**	AVCL	7735	-301
209	DUMMY	5425	-301	**243**	AVCL	7805	-301
210	DUMMY	5495	-301	**244**	DUMMY	7875	-301
211	DUMMY	5565	-301	**245**	DUMMY	7945	-301
212	DUMMY	5635	-301	**246**	DUMMY	8015	-301
213	DGND	5705	-301	**247**	DUMMY	8085	-301
214	DGND	5775	-301	**248**	DUMMY	8155	-301
215	DGND	5845	-301	**249**	DUMMY	8225	-301
216	DGND	5915	-301	**250**	DUMMY	8295	-301
217	DGND	5985	-301	**251**	DUMMY	8365	-301
218	AGND	6055	-301	**252**	DUMMY	8435	-301
219	AGND	6125	-301	**253**	DUMMY	8505	-301
220	AGND	6195	-301	**254**	DUMMY	8575	-301
221	AGND	6265	-301	**255**	DUMMY	8645	-301
222	AGND	6335	-301	**256**	DUMMY	8715	-301
223	VGL	6405	-301	**257**	DUMMY	8785	-301
224	VGL	6475	-301	**258**	DUMMY	8855	-301
225	VGL	6545	-301	**259**	DUMMY	8925	-301
226	VGL	6615	-301	**260**	DUMMY	8995	-301
227	VGL	6685	-301	**261**	DUMMY	9065	-301
228	VGL	6755	-301	**262**	DUMMY	9135	-301
229	VGL	6825	-301	**263**	DUMMY	9397.5	200
230	VGL	6895	-301	**264**	DUMMY	9382.5	319
231	VGL	6965	-301	**265**	DUMMY	9367.5	200
232	AGNDDUM3	7035	-301	**266**	VGLDMY1	9352.5	319
233	AGNDDUM4	7105	-301	**267**	G2	9337.5	200
234	VGH	7175	-301	**268**	G4	9322.5	319
235	VGH	7245	-301	**269**	G6	9307.5	200
236	VGH	7315	-301	**270**	G8	9292.5	319

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
271	G10	9277.5	200	**305**	G78	8767.5	200
272	G12	9262.5	319	**306**	G80	8752.5	319
273	G14	9247.5	200	**307**	G82	8737.5	200
274	G16	9232.5	319	**308**	G84	8722.5	319
275	G18	9217.5	200	**309**	G86	8707.5	200
276	G20	9202.5	319	**310**	G88	8692.5	319
277	G22	9187.5	200	**311**	G90	8677.5	200
278	G24	9172.5	319	**312**	G92	8662.5	319
279	G26	9157.5	200	**313**	G94	8647.5	200
280	G28	9142.5	319	**314**	G96	8632.5	319
281	G30	9127.5	200	**315**	G98	8617.5	200
282	G32	9112.5	319	**316**	G100	8602.5	319
283	G34	9097.5	200	**317**	G102	8587.5	200
284	G36	9082.5	319	**318**	G104	8572.5	319
285	G38	9067.5	200	**319**	G106	8557.5	200
286	G40	9052.5	319	**320**	G108	8542.5	319
287	G42	9037.5	200	**321**	G110	8527.5	200
288	G44	9022.5	319	**322**	G112	8512.5	319
289	G46	9007.5	200	**323**	G114	8497.5	200
290	G48	8992.5	319	**324**	G116	8482.5	319
291	G50	8977.5	200	**325**	G118	8467.5	200
292	G52	8962.5	319	**326**	G120	8452.5	319
293	G54	8947.5	200	**327**	G122	8437.5	200
294	G56	8932.5	319	**328**	G124	8422.5	319
295	G58	8917.5	200	**329**	G126	8407.5	200
296	G60	8902.5	319	**330**	G128	8392.5	319
297	G62	8887.5	200	**331**	G130	8377.5	200
298	G64	8872.5	319	**332**	G132	8362.5	319
299	G66	8857.5	200	**333**	G134	8347.5	200
300	G68	8842.5	319	**334**	G136	8332.5	319
301	G70	8827.5	200	**335**	G138	8317.5	200
302	G72	8812.5	319	**336**	G140	8302.5	319
303	G74	8797.5	200	**337**	G142	8287.5	200
304	G76	8782.5	319	**338**	G144	8272.5	319

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
339	G146	8257.5	200	**373**	G214	7747.5	200
340	G148	8242.5	319	**374**	G216	7732.5	319
341	G150	8227.5	200	**375**	G218	7717.5	200
342	G152	8212.5	319	**376**	G220	7702.5	319
343	G154	8197.5	200	**377**	G222	7687.5	200
344	G156	8182.5	319	**378**	G224	7672.5	319
345	G158	8167.5	200	**379**	G226	7657.5	200
346	G160	8152.5	319	**380**	G228	7642.5	319
347	G162	8137.5	200	**381**	G230	7627.5	200
348	G164	8122.5	319	**382**	G232	7612.5	319
349	G166	8107.5	200	**383**	G234	7597.5	200
350	G168	8092.5	319	**384**	G236	7582.5	319
351	G200	8077.5	200	**385**	G238	7567.5	200
352	G172	8062.5	319	**386**	G240	7552.5	319
353	G174	8047.5	200	**387**	G242	7537.5	200
354	G176	8032.5	319	**388**	G244	7522.5	319
355	G178	8017.5	200	**389**	G246	7507.5	200
356	G180	8002.5	319	**390**	G248	7492.5	319
357	G182	7987.5	200	**391**	G250	7477.5	200
358	G184	7972.5	319	**392**	G252	7462.5	319
359	G186	7957.5	200	**393**	G254	7447.5	200
360	G188	7942.5	319	**394**	G256	7432.5	319
361	G190	7927.5	200	**395**	G258	7417.5	200
362	G192	7912.5	319	**396**	G260	7402.5	319
363	G194	7897.5	200	**397**	G262	7387.5	200
364	G196	7882.5	319	**398**	G264	7372.5	319
365	G198	7867.5	200	**399**	G266	7357.5	200
366	G200	7852.5	319	**400**	G268	7342.5	319
367	G202	7837.5	200	**401**	G270	7327.5	200
368	G204	7822.5	319	**402**	G272	7312.5	319
369	G206	7807.5	200	**403**	G274	7297.5	200
370	G208	7792.5	319	**404**	G276	7282.5	319
371	G210	7777.5	200	**405**	G278	7267.5	200
372	G212	7762.5	319	**406**	G280	7252.5	319

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
407	G282	7237.5	200	**441**	G350	6727.5	200
408	G284	7222.5	319	**442**	G352	6712.5	319
409	G286	7207.5	200	**443**	G354	6697.5	200
410	G288	7192.5	319	**444**	G356	6682.5	319
411	G290	7177.5	200	**445**	G358	6667.5	200
412	G292	7162.5	319	**446**	G360	6652.5	319
413	G294	7147.5	200	**447**	G362	6637.5	200
414	G296	7132.5	319	**448**	G364	6622.5	319
415	G298	7117.5	200	**449**	G366	6607.5	200
416	G300	7102.5	319	**450**	G368	6592.5	319
417	G302	7087.5	200	**451**	G370	6577.5	200
418	G304	7072.5	319	**452**	G372	6562.5	319
419	G306	7057.5	200	**453**	G374	6547.5	200
420	G308	7042.5	319	**454**	G376	6532.5	319
421	G310	7027.5	200	**455**	G378	6517.5	200
422	G312	7012.5	319	**456**	G380	6502.5	319
423	G314	6997.5	200	**457**	G382	6487.5	200
424	G316	6982.5	319	**458**	G384	6472.5	319
425	G318	6967.5	200	**459**	G386	6457.5	200
426	G320	6952.5	319	**460**	G388	6442.5	319
427	G322	6937.5	200	**461**	G390	6427.5	200
428	G324	6922.5	319	**462**	G392	6412.5	319
429	G326	6907.5	200	**463**	G394	6397.5	200
430	G328	6892.5	319	**464**	G396	6382.5	319
431	G330	6877.5	200	**465**	G398	6367.5	200
432	G332	6862.5	319	**466**	G400	6352.5	319
433	G334	6847.5	200	**467**	G402	6337.5	200
434	G336	6832.5	319	**468**	G404	6322.5	319
435	G338	6817.5	200	**469**	G406	6307.5	200
436	G340	6802.5	319	**470**	G408	6292.5	319
437	G342	6787.5	200	**471**	G410	6277.5	200
438	G344	6772.5	319	**472**	G412	6262.5	319
439	G346	6757.5	200	**473**	G414	6247.5	200
440	G348	6742.5	319	**474**	G416	6232.5	319

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
475	G418	6217.5	200	**509**	S696	5512.5	319
476	G420	6202.5	319	**510**	S695	5497.5	200
477	G422	6187.5	200	**511**	S694	5482.5	319
478	G424	6172.5	319	**512**	S693	5467.5	200
479	G426	6157.5	200	**513**	S692	5452.5	319
480	G428	6142.5	319	**514**	S691	5437.5	200
481	G430	6127.5	200	**515**	S690	5422.5	319
482	G432	6112.5	319	**516**	S689	5407.5	200
483	VGLDMY2	6097.5	200	**517**	S688	5392.5	319
484	DUMMY	5887.5	200	**518**	S687	5377.5	200
485	S720	5872.5	319	**519**	S686	5362.5	319
486	S719	5857.5	200	**520**	S685	5347.5	200
487	S718	5842.5	319	**521**	S684	5332.5	319
488	S717	5827.5	200	**522**	S683	5317.5	200
489	S716	5812.5	319	**523**	S682	5302.5	319
490	S715	5797.5	200	**524**	S681	5287.5	200
491	S714	5782.5	319	**525**	S680	5272.5	319
492	S713	5767.5	200	**526**	S679	5257.5	200
493	S712	5752.5	319	**527**	S678	5242.5	319
494	S711	5737.5	200	**528**	S677	5227.5	200
495	S710	5722.5	319	**529**	S676	5212.5	319
496	S709	5707.5	200	**530**	S675	5197.5	200
497	S708	5692.5	319	**531**	S674	5182.5	319
498	S707	5677.5	200	**532**	S673	5167.5	200
499	S706	5662.5	319	**533**	S672	5152.5	319
500	S705	5647.5	200	**534**	S671	5137.5	200
501	S704	5632.5	319	**535**	S670	5122.5	319
502	S703	5617.5	200	**536**	S669	5107.5	200
503	S702	5602.5	319	**537**	S668	5092.5	319
504	S701	5587.5	200	**538**	S667	5077.5	200
505	S700	5572.5	319	**539**	S666	5062.5	319
506	S699	5557.5	200	**540**	S665	5047.5	200
507	S698	5542.5	319	**541**	S664	5032.5	319
508	S697	5527.5	200	**542**	S663	5017.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
543	S662	5002.5	319	**577**	S628	4492.5	319
544	S661	4987.5	200	**578**	S627	4477.5	200
545	S660	4972.5	319	**579**	S626	4462.5	319
546	S659	4957.5	200	**580**	S625	4447.5	200
547	S658	4942.5	319	**581**	S624	4432.5	319
548	S657	4927.5	200	**582**	S623	4417.5	200
549	S656	4912.5	319	**583**	S622	4402.5	319
550	S655	4897.5	200	**584**	S621	4387.5	200
551	S654	4882.5	319	**585**	S620	4372.5	319
552	S653	4867.5	200	**586**	S619	4357.5	200
553	S652	4852.5	319	**587**	S618	4342.5	319
554	S651	4837.5	200	**588**	S617	4327.5	200
555	S650	4822.5	319	**589**	S616	4312.5	319
556	S649	4807.5	200	**590**	S615	4297.5	200
557	S648	4792.5	319	**591**	S614	4282.5	319
558	S647	4777.5	200	**592**	S613	4267.5	200
559	S646	4762.5	319	**593**	S612	4252.5	319
560	S645	4747.5	200	**594**	S611	4237.5	200
561	S644	4732.5	319	**595**	S610	4222.5	319
562	S643	4717.5	200	**596**	S609	4207.5	200
563	S642	4702.5	319	**597**	S608	4192.5	319
564	S641	4687.5	200	**598**	S607	4177.5	200
565	S640	4672.5	319	**599**	S606	4162.5	319
566	S639	4657.5	200	**600**	S605	4147.5	200
567	S638	4642.5	319	**601**	S604	4132.5	319
568	S637	4627.5	200	**602**	S603	4117.5	200
569	S636	4612.5	319	**603**	S602	4102.5	319
570	S635	4597.5	200	**604**	S601	4087.5	200
571	S634	4582.5	319	**605**	S600	4072.5	319
572	S633	4567.5	200	**606**	S599	4057.5	200
573	S632	4552.5	319	**607**	S598	4042.5	319
574	S631	4537.5	200	**608**	S597	4027.5	200
575	S630	4522.5	319	**609**	S596	4012.5	319
576	S629	4507.5	200	**610**	S595	3997.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
611	S594	3982.5	319	**645**	S560	3472.5	319
612	S593	3967.5	200	**646**	S559	3457.5	200
613	S592	3952.5	319	**647**	S558	3442.5	319
614	S591	3937.5	200	**648**	S557	3427.5	200
615	S590	3922.5	319	**649**	S556	3412.5	319
616	S589	3907.5	200	**650**	S555	3397.5	200
617	S588	3892.5	319	**651**	S554	3382.5	319
618	S587	3877.5	200	**652**	S553	3367.5	200
619	S586	3862.5	319	**653**	S552	3352.5	319
620	S585	3847.5	200	**654**	S551	3337.5	200
621	S584	3832.5	319	**655**	S550	3322.5	319
622	S583	3817.5	200	**656**	S549	3307.5	200
623	S582	3802.5	319	**657**	S548	3292.5	319
624	S581	3787.5	200	**658**	S547	3277.5	200
625	S580	3772.5	319	**659**	S546	3262.5	319
626	S579	3757.5	200	**660**	S545	3247.5	200
627	S578	3742.5	319	**661**	S544	3232.5	319
628	S577	3727.5	200	**662**	S543	3217.5	200
629	S576	3712.5	319	**663**	S542	3202.5	319
630	S575	3697.5	200	**664**	S541	3187.5	200
631	S574	3682.5	319	**665**	S540	3172.5	319
632	S573	3667.5	200	**666**	S539	3157.5	200
633	S572	3652.5	319	**667**	S538	3142.5	319
634	S571	3637.5	200	**668**	S537	3127.5	200
635	S570	3622.5	319	**669**	S536	3112.5	319
636	S569	3607.5	200	**670**	S535	3097.5	200
637	S568	3592.5	319	**671**	S534	3082.5	319
638	S567	3577.5	200	**672**	S533	3067.5	200
639	S566	3562.5	319	**673**	S532	3052.5	319
640	S565	3547.5	200	**674**	S531	3037.5	200
641	S564	3532.5	319	**675**	S530	3022.5	319
642	S563	3517.5	200	**676**	S529	3007.5	200
643	S562	3502.5	319	**677**	S528	2992.5	319
644	S561	3487.5	200	**678**	S527	2977.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
679	S526	2962.5	319	**713**	S492	2452.5	319
680	S525	2947.5	200	**714**	S491	2437.5	200
681	S524	2932.5	319	**715**	S490	2422.5	319
682	S523	2917.5	200	**716**	S489	2407.5	200
683	S522	2902.5	319	**717**	S488	2392.5	319
684	S521	2887.5	200	**718**	S487	2377.5	200
685	S520	2872.5	319	**719**	S486	2362.5	319
686	S519	2857.5	200	**720**	S485	2347.5	200
687	S518	2842.5	319	**721**	S484	2332.5	319
688	S517	2827.5	200	**722**	S483	2317.5	200
689	S516	2812.5	319	**723**	S482	2302.5	319
690	S515	2797.5	200	**724**	S481	2287.5	200
691	S514	2782.5	319	**725**	S480	2272.5	319
692	S513	2767.5	200	**726**	S479	2257.5	200
693	S512	2752.5	319	**727**	S478	2242.5	319
694	S511	2737.5	200	**728**	S477	2227.5	200
695	S510	2722.5	319	**729**	S476	2212.5	319
696	S509	2707.5	200	**730**	S475	2197.5	200
697	S508	2692.5	319	**731**	S474	2182.5	319
698	S507	2677.5	200	**732**	S473	2167.5	200
699	S506	2662.5	319	**733**	S472	2152.5	319
700	S505	2647.5	200	**734**	S471	2137.5	200
701	S504	2632.5	319	**735**	S470	2122.5	319
702	S503	2617.5	200	**736**	S469	2107.5	200
703	S502	2602.5	319	**737**	S468	2092.5	319
704	S501	2587.5	200	**738**	S467	2077.5	200
705	S500	2572.5	319	**739**	S466	2062.5	319
706	S499	2557.5	200	**740**	S465	2047.5	200
707	S498	2542.5	319	**741**	S464	2032.5	319
708	S497	2527.5	200	**742**	S463	2017.5	200
709	S496	2512.5	319	**743**	S462	2002.5	319
710	S495	2497.5	200	**744**	S461	1987.5	200
711	S494	2482.5	319	**745**	S460	1972.5	319
712	S493	2467.5	200	**746**	S459	1957.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
747	S458	1942.5	319	**781**	S424	1432.5	319
748	S457	1927.5	200	**782**	S423	1417.5	200
749	S456	1912.5	319	**783**	S422	1402.5	319
750	S455	1897.5	200	**784**	S421	1387.5	200
751	S454	1882.5	319	**785**	S420	1372.5	319
752	S453	1867.5	200	**786**	S419	1357.5	200
753	S452	1852.5	319	**787**	S418	1342.5	319
754	S451	1837.5	200	**788**	S417	1327.5	200
755	S450	1822.5	319	**789**	S416	1312.5	319
756	S449	1807.5	200	**790**	S415	1297.5	200
757	S448	1792.5	319	**791**	S414	1282.5	319
758	S447	1777.5	200	**792**	S413	1267.5	200
759	S446	1762.5	319	**793**	S412	1252.5	319
760	S445	1747.5	200	**794**	S411	1237.5	200
761	S444	1732.5	319	**795**	S410	1222.5	319
762	S443	1717.5	200	**796**	S409	1207.5	200
763	S442	1702.5	319	**797**	S408	1192.5	319
764	S441	1687.5	200	**798**	S407	1177.5	200
765	S440	1672.5	319	**799**	S406	1162.5	319
766	S439	1657.5	200	**800**	S405	1147.5	200
767	S438	1642.5	319	**801**	S404	1132.5	319
768	S437	1627.5	200	**802**	S403	1117.5	200
769	S436	1612.5	319	**803**	S402	1102.5	319
770	S435	1597.5	200	**804**	S401	1087.5	200
771	S434	1582.5	319	**805**	S400	1072.5	319
772	S433	1567.5	200	**806**	S399	1057.5	200
773	S432	1552.5	319	**807**	S398	1042.5	319
774	S431	1537.5	200	**808**	S397	1027.5	200
775	S430	1522.5	319	**809**	S396	1012.5	319
776	S429	1507.5	200	**810**	S395	997.5	200
777	S428	1492.5	319	**811**	S394	982.5	319
778	S427	1477.5	200	**812**	S393	967.5	200
779	S426	1462.5	319	**813**	S392	952.5	319
780	S425	1447.5	200	**814**	S391	937.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
815	S390	922.5	319	**849**	PVSFTP	-427.5	319
816	S389	907.5	200	**850**	DUMMY	-442.5	200
817	S388	892.5	319	**851**	PVAP	-457.5	319
818	S387	877.5	200	**852**	DUMMY	-472.5	200
819	S386	862.5	319	**853**	S360	-487.5	319
820	S385	847.5	200	**854**	S359	-502.5	200
821	S384	832.5	319	**855**	S358	-517.5	319
822	S383	817.5	200	**856**	S357	-532.5	200
823	S382	802.5	319	**857**	S356	-547.5	319
824	S381	787.5	200	**858**	S355	-562.5	200
825	S380	772.5	319	**859**	S354	-577.5	319
826	S379	757.5	200	**860**	S353	-592.5	200
827	S378	742.5	319	**861**	S352	-607.5	319
828	S377	727.5	200	**862**	S351	-622.5	200
829	S376	712.5	319	**863**	S350	-637.5	319
830	S375	697.5	200	**864**	S349	-652.5	200
831	S374	682.5	319	**865**	S348	-667.5	319
832	S373	667.5	200	**866**	S347	-682.5	200
833	S372	652.5	319	**867**	S346	-697.5	319
834	S371	637.5	200	**868**	S345	-712.5	200
835	S370	622.5	319	**869**	S344	-727.5	319
836	S369	607.5	200	**870**	S343	-742.5	200
837	S368	592.5	319	**871**	S342	-757.5	319
838	S367	577.5	200	**872**	S341	-772.5	200
839	S366	562.5	319	**873**	S340	-787.5	319
840	S365	547.5	200	**874**	S339	-802.5	200
841	S364	532.5	319	**875**	S338	-817.5	319
842	S363	517.5	200	**876**	S337	-832.5	200
843	S362	502.5	319	**877**	S336	-847.5	319
844	S361	487.5	200	**878**	S335	-862.5	200
845	PVAN	472.5	319	**879**	S334	-877.5	319
846	DUMMY	457.5	200	**880**	S333	-892.5	200
847	PVSFTN	442.5	319	**881**	S332	-907.5	319
848	DUMMY	427.5	200	**882**	S331	-922.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
883	S330	-937.5	319	**917**	S296	-1447.5	319
884	S329	-952.5	200	**918**	S295	-1462.5	200
885	S328	-967.5	319	**919**	S294	-1477.5	319
886	S327	-982.5	200	**920**	S293	-1492.5	200
887	S326	-997.5	319	**921**	S292	-1507.5	319
888	S325	-1012.5	200	**922**	S291	-1522.5	200
889	S324	-1027.5	319	**923**	S290	-1537.5	319
890	S323	-1042.5	200	**924**	S319	-1552.5	200
891	S322	-1057.5	319	**925**	S288	-1567.5	319
892	S321	-1072.5	200	**926**	S287	-1582.5	200
893	S320	-1087.5	319	**927**	S286	-1597.5	319
894	S319	-1102.5	200	**928**	S285	-1612.5	200
895	S318	-1117.5	319	**929**	S284	-1627.5	319
896	S317	-1132.5	200	**930**	S283	-1642.5	200
897	S316	-1147.5	319	**931**	S282	-1657.5	319
898	S315	-1162.5	200	**932**	S281	-1672.5	200
899	S314	-1177.5	319	**933**	S280	-1687.5	319
900	S313	-1192.5	200	**934**	S279	-1702.5	200
901	S312	-1207.5	319	**935**	S278	-1717.5	319
902	S311	-1222.5	200	**936**	S277	-1732.5	200
903	S310	-1237.5	319	**937**	S276	-1747.5	319
904	S309	-1252.5	200	**938**	S275	-1762.5	200
905	S308	-1267.5	319	**939**	S274	-1777.5	319
906	S307	-1282.5	200	**940**	S273	-1792.5	200
907	S306	-1297.5	319	**941**	S272	-1807.5	319
908	S305	-1312.5	200	**942**	S271	-1822.5	200
909	S304	-1327.5	319	**943**	S270	-1837.5	319
910	S303	-1342.5	200	**944**	S269	-1852.5	200
911	S302	-1357.5	319	**945**	S268	-1867.5	319
912	S301	-1372.5	200	**946**	S267	-1882.5	200
913	S300	-1387.5	319	**947**	S266	-1897.5	319
914	S299	-1402.5	200	**948**	S265	-1912.5	200
915	S298	-1417.5	319	**949**	S264	-1927.5	319
916	S297	-1432.5	200	**950**	S263	-1942.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
951	S262	-1957.5	319	**985**	S228	-2467.5	319
952	S261	-1972.5	200	**986**	S227	-2482.5	200
953	S260	-1987.5	319	**987**	S226	-2497.5	319
954	S259	-2002.5	200	**988**	S225	-2512.5	200
955	S258	-2017.5	319	**989**	S224	-2527.5	319
956	S257	-2032.5	200	**990**	S223	-2542.5	200
957	S256	-2047.5	319	**991**	S222	-2557.5	319
958	S255	-2062.5	200	**992**	S221	-2572.5	200
959	S254	-2077.5	319	**993**	S220	-2587.5	319
960	S253	-2092.5	200	**994**	S219	-2602.5	200
961	S252	-2107.5	319	**995**	S218	-2617.5	319
962	S251	-2122.5	200	**996**	S217	-2632.5	200
963	S250	-2137.5	319	**997**	S216	-2647.5	319
964	S249	-2152.5	200	**998**	S215	-2662.5	200
965	S248	-2167.5	319	**999**	S214	-2677.5	319
966	S247	-2182.5	200	**1000**	S213	-2692.5	200
967	S246	-2197.5	319	**1001**	S212	-2707.5	319
968	S245	-2212.5	200	**1002**	S211	-2722.5	200
969	S244	-2227.5	319	**1003**	S210	-2737.5	319
970	S243	-2242.5	200	**1004**	S209	-2752.5	200
971	S242	-2257.5	319	**1005**	S208	-2767.5	319
972	S241	-2272.5	200	**1006**	S207	-2782.5	200
973	S240	-2287.5	319	**1007**	S206	-2797.5	319
974	S239	-2302.5	200	**1008**	S205	-2812.5	200
975	S238	-2317.5	319	**1009**	S204	-2827.5	319
976	S237	-2332.5	200	**1010**	S203	-2842.5	200
977	S236	-2347.5	319	**1011**	S202	-2857.5	319
978	S235	-2362.5	200	**1012**	S201	-2872.5	200
979	S234	-2377.5	319	**1013**	S200	-2887.5	319
980	S233	-2392.5	200	**1014**	S199	-2902.5	200
981	S232	-2407.5	319	**1015**	S198	-2917.5	319
982	S231	-2422.5	200	**1016**	S197	-2932.5	200
983	S230	-2437.5	319	**1017**	S196	-2947.5	319
984	S229	-2452.5	200	**1018**	S195	-2962.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1019	S194	-2977.5	319	**1053**	S160	-3487.5	319
1020	S193	-2992.5	200	**1054**	S159	-3502.5	200
1021	S192	-3007.5	319	**1055**	S158	-3517.5	319
1022	S191	-3022.5	200	**1056**	S157	-3532.5	200
1023	S190	-3037.5	319	**1057**	S156	-3547.5	319
1024	S189	-3052.5	200	**1058**	S155	-3562.5	200
1025	S188	-3067.5	319	**1059**	S154	-3577.5	319
1026	S187	-3082.5	200	**1060**	S153	-3592.5	200
1027	S186	-3097.5	319	**1061**	S152	-3607.5	319
1028	S185	-3112.5	200	**1062**	S151	-3622.5	200
1029	S184	-3127.5	319	**1063**	S150	-3637.5	319
1030	S183	-3142.5	200	**1064**	S149	-3652.5	200
1031	S182	-3157.5	319	**1065**	S148	-3667.5	319
1032	S181	-3172.5	200	**1066**	S147	-3682.5	200
1033	S180	-3187.5	319	**1067**	S146	-3697.5	319
1034	S179	-3202.5	200	**1068**	S145	-3712.5	200
1035	S178	-3217.5	319	**1069**	S144	-3727.5	319
1036	S177	-3232.5	200	**1070**	S143	-3742.5	200
1037	S176	-3247.5	319	**1071**	S142	-3757.5	319
1038	S175	-3262.5	200	**1072**	S141	-3772.5	200
1039	S174	-3277.5	319	**1073**	S140	-3787.5	319
1040	S173	-3292.5	200	**1074**	S139	-3802.5	200
1041	S172	-3307.5	319	**1075**	S138	-3817.5	319
1042	S171	-3322.5	200	**1076**	S137	-3832.5	200
1043	S200	-3337.5	319	**1077**	S136	-3847.5	319
1044	S169	-3352.5	200	**1078**	S135	-3862.5	200
1045	S168	-3367.5	319	**1079**	S134	-3877.5	319
1046	S167	-3382.5	200	**1080**	S133	-3892.5	200
1047	S166	-3397.5	319	**1081**	S132	-3907.5	319
1048	S165	-3412.5	200	**1082**	S131	-3922.5	200
1049	S164	-3427.5	319	**1083**	S130	-3937.5	319
1050	S163	-3442.5	200	**1084**	S129	-3952.5	200
1051	S162	-3457.5	319	**1085**	S128	-3967.5	319
1052	S161	-3472.5	200	**1086**	S127	-3982.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1087	S126	-3997.5	319	**1121**	S92	-4507.5	319
1088	S125	-4012.5	200	**1122**	S91	-4522.5	200
1089	S124	-4027.5	319	**1123**	S90	-4537.5	319
1090	S123	-4042.5	200	**1124**	S89	-4552.5	200
1091	S122	-4057.5	319	**1125**	S88	-4567.5	319
1092	S121	-4072.5	200	**1126**	S87	-4582.5	200
1093	S120	-4087.5	319	**1127**	S86	-4597.5	319
1094	S119	-4102.5	200	**1128**	S85	-4612.5	200
1095	S118	-4117.5	319	**1129**	S84	-4627.5	319
1096	S117	-4132.5	200	**1130**	S83	-4642.5	200
1097	S116	-4147.5	319	**1131**	S82	-4657.5	319
1098	S115	-4162.5	200	**1132**	S81	-4672.5	200
1099	S114	-4177.5	319	**1133**	S80	-4687.5	319
1100	S113	-4192.5	200	**1134**	S79	-4702.5	200
1101	S112	-4207.5	319	**1135**	S78	-4717.5	319
1102	S111	-4222.5	200	**1136**	S77	-4732.5	200
1103	S110	-4237.5	319	**1137**	S76	-4747.5	319
1104	S109	-4252.5	200	**1138**	S75	-4762.5	200
1105	S108	-4267.5	319	**1139**	S74	-4777.5	319
1106	S107	-4282.5	200	**1140**	S73	-4792.5	200
1107	S106	-4297.5	319	**1141**	S72	-4807.5	319
1108	S105	-4312.5	200	**1142**	S71	-4822.5	200
1109	S104	-4327.5	319	**1143**	S70	-4837.5	319
1110	S103	-4342.5	200	**1144**	S69	-4852.5	200
1111	S102	-4357.5	319	**1145**	S68	-4867.5	319
1112	S101	-4372.5	200	**1146**	S67	-4882.5	200
1113	S100	-4387.5	319	**1147**	S66	-4897.5	319
1114	S99	-4402.5	200	**1148**	S65	-4912.5	200
1115	S98	-4417.5	319	**1149**	S64	-4927.5	319
1116	S97	-4432.5	200	**1150**	S63	-4942.5	200
1117	S96	-4447.5	319	**1151**	S62	-4957.5	319
1118	S95	-4462.5	200	**1152**	S61	-4972.5	200
1119	S94	-4477.5	319	**1153**	S60	-4987.5	319
1120	S93	-4492.5	200	**1154**	S59	-5002.5	200

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1155	S58	-5017.5	319	**1189**	S24	-5527.5	319
1156	S57	-5032.5	200	**1190**	S23	-5542.5	200
1157	S56	-5047.5	319	**1191**	S22	-5557.5	319
1158	S55	-5062.5	200	**1192**	S21	-5572.5	200
1159	S54	-5077.5	319	**1193**	S20	-5587.5	319
1160	S53	-5092.5	200	**1194**	S19	-5602.5	200
1161	S52	-5107.5	319	**1195**	S18	-5617.5	319
1162	S51	-5122.5	200	**1196**	S17	-5632.5	200
1163	S50	-5137.5	319	**1197**	S16	-5647.5	319
1164	S49	-5152.5	200	**1198**	S15	-5662.5	200
1165	S48	-5167.5	319	**1199**	S14	-5677.5	319
1166	S47	-5182.5	200	**1200**	S13	-5692.5	200
1167	S46	-5197.5	319	**1201**	S12	-5707.5	319
1168	S45	-5212.5	200	**1202**	S11	-5722.5	200
1169	S44	-5227.5	319	**1203**	S10	-5737.5	319
1170	S43	-5242.5	200	**1204**	S9	-5752.5	200
1171	S42	-5257.5	319	**1205**	S8	-5767.5	319
1172	S41	-5272.5	200	**1206**	S7	-5782.5	200
1173	S40	-5287.5	319	**1207**	S6	-5797.5	319
1174	S39	-5302.5	200	**1208**	S5	-5812.5	200
1175	S38	-5317.5	319	**1209**	S4	-5827.5	319
1176	S37	-5332.5	200	**1210**	S3	-5842.5	200
1177	S36	-5347.5	319	**1211**	S2	-5857.5	319
1178	S35	-5362.5	200	**1212**	S1	-5872.5	200
1179	S34	-5377.5	319	**1213**	DUMMY	-5887.5	319
1180	S33	-5392.5	200	**1214**	VGLDMY3	-6097.5	319
1181	S32	-5407.5	319	**1215**	G431	-6112.5	200
1182	S31	-5422.5	200	**1216**	G429	-6127.5	319
1183	S30	-5437.5	319	**1217**	G427	-6142.5	200
1184	S29	-5452.5	200	**1218**	G425	-6157.5	319
1185	S28	-5467.5	319	**1219**	G423	-6172.5	200
1186	S27	-5482.5	200	**1220**	G421	-6187.5	319
1187	S26	-5497.5	319	**1221**	G419	-6202.5	200
1188	S25	-5512.5	200	**1222**	G417	-6217.5	319

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1223	G415	-6232.5	200	**1257**	G347	-6742.5	200
1224	G413	-6247.5	319	**1258**	G345	-6757.5	319
1225	G411	-6262.5	200	**1259**	G343	-6772.5	200
1226	G409	-6277.5	319	**1260**	G341	-6787.5	319
1227	G407	-6292.5	200	**1261**	G339	-6802.5	200
1228	G405	-6307.5	319	**1262**	G337	-6817.5	319
1229	G403	-6322.5	200	**1263**	G335	-6832.5	200
1230	G401	-6337.5	319	**1264**	G333	-6847.5	319
1231	G399	-6352.5	200	**1265**	G331	-6862.5	200
1232	G397	-6367.5	319	**1266**	G329	-6877.5	319
1233	G395	-6382.5	200	**1267**	G327	-6892.5	200
1234	G393	-6397.5	319	**1268**	G325	-6907.5	319
1235	G391	-6412.5	200	**1269**	G323	-6922.5	200
1236	G389	-6427.5	319	**1270**	G321	-6937.5	319
1237	G387	-6442.5	200	**1271**	G319	-6952.5	200
1238	G385	-6457.5	319	**1272**	G317	-6967.5	319
1239	G383	-6472.5	200	**1273**	G315	-6982.5	200
1240	G381	-6487.5	319	**1274**	G313	-6997.5	319
1241	G379	-6502.5	200	**1275**	G311	-7012.5	200
1242	G377	-6517.5	319	**1276**	G309	-7027.5	319
1243	G375	-6532.5	200	**1277**	G307	-7042.5	200
1244	G373	-6547.5	319	**1278**	G305	-7057.5	319
1245	G371	-6562.5	200	**1279**	G303	-7072.5	200
1246	G369	-6577.5	319	**1280**	G301	-7087.5	319
1247	G367	-6592.5	200	**1281**	G299	-7102.5	200
1248	G365	-6607.5	319	**1282**	G297	-7117.5	319
1249	G363	-6622.5	200	**1283**	G295	-7132.5	200
1250	G361	-6637.5	319	**1284**	G293	-7147.5	319
1251	G359	-6652.5	200	**1285**	G291	-7162.5	200
1252	G357	-6667.5	319	**1286**	G319	-7177.5	319
1253	G355	-6682.5	200	**1287**	G287	-7192.5	200
1254	G353	-6697.5	319	**1288**	G285	-7207.5	319
1255	G351	-6712.5	200	**1289**	G283	-7222.5	200
1256	G349	-6727.5	319	**1290**	G281	-7237.5	319

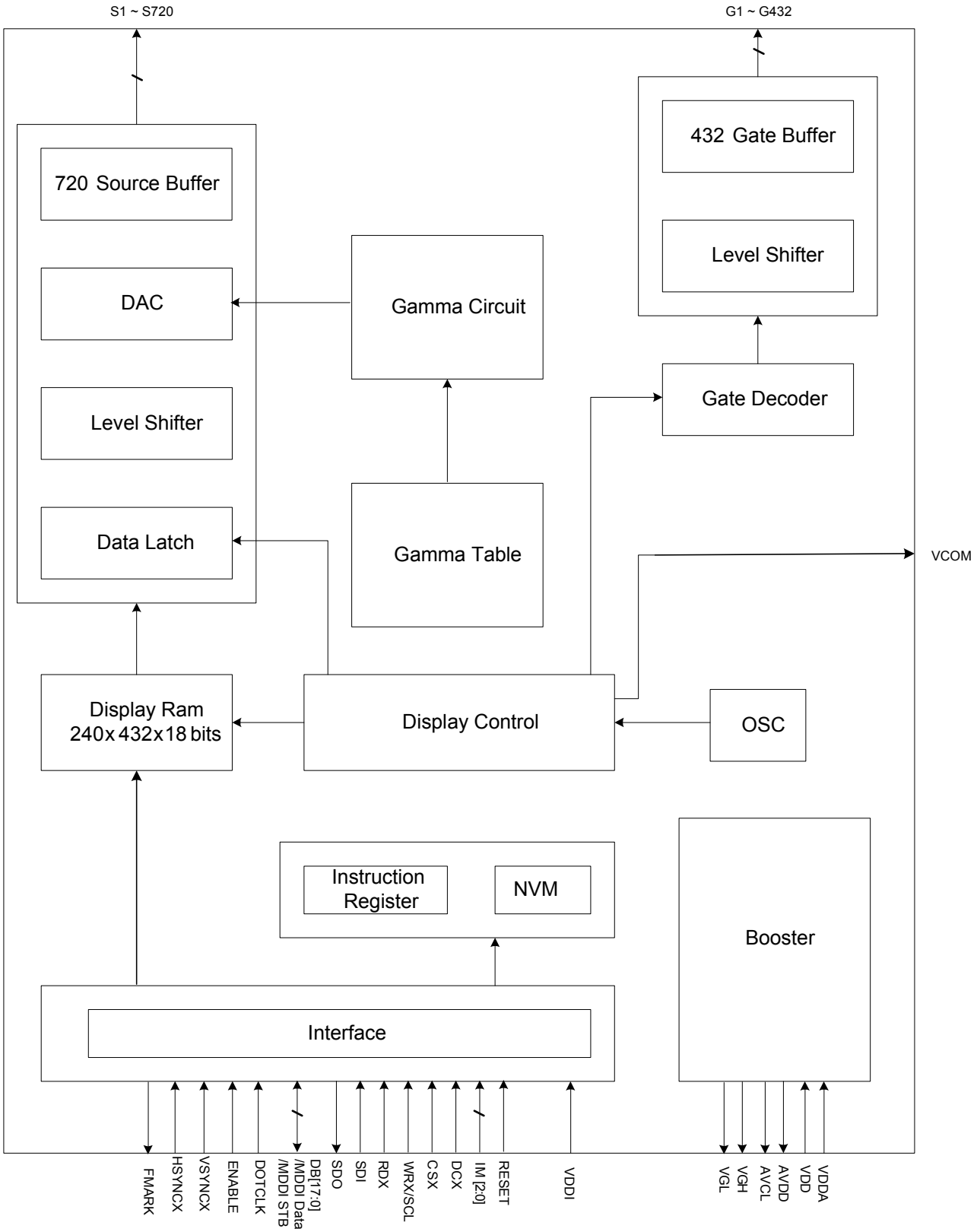
PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1291	G279	-7252.5	200	**1325**	G211	-7762.5	200
1292	G277	-7267.5	319	**1326**	G209	-7777.5	319
1293	G275	-7282.5	200	**1327**	G207	-7792.5	200
1294	G273	-7297.5	319	**1328**	G205	-7807.5	319
1295	G271	-7312.5	200	**1329**	G203	-7822.5	200
1296	G269	-7327.5	319	**1330**	G201	-7837.5	319
1297	G267	-7342.5	200	**1331**	G199	-7852.5	200
1298	G265	-7357.5	319	**1332**	G197	-7867.5	319
1299	G263	-7372.5	200	**1333**	G195	-7882.5	200
1300	G261	-7387.5	319	**1334**	G193	-7897.5	319
1301	G259	-7402.5	200	**1335**	G191	-7912.5	200
1302	G257	-7417.5	319	**1336**	G189	-7927.5	319
1303	G255	-7432.5	200	**1337**	G187	-7942.5	200
1304	G253	-7447.5	319	**1338**	G185	-7957.5	319
1305	G251	-7462.5	200	**1339**	G183	-7972.5	200
1306	G249	-7477.5	319	**1340**	G181	-7987.5	319
1307	G247	-7492.5	200	**1341**	G179	-8002.5	200
1308	G245	-7507.5	319	**1342**	G177	-8017.5	319
1309	G243	-7522.5	200	**1343**	G175	-8032.5	200
1310	G241	-7537.5	319	**1344**	G173	-8047.5	319
1311	G239	-7552.5	200	**1345**	G171	-8062.5	200
1312	G237	-7567.5	319	**1346**	G169	-8077.5	319
1313	G235	-7582.5	200	**1347**	G167	-8092.5	200
1314	G233	-7597.5	319	**1348**	G165	-8107.5	319
1315	G231	-7612.5	200	**1349**	G163	-8122.5	200
1316	G229	-7627.5	319	**1350**	G161	-8137.5	319
1317	G227	-7642.5	200	**1351**	G159	-8152.5	200
1318	G225	-7657.5	319	**1352**	G157	-8167.5	319
1319	G223	-7672.5	200	**1353**	G155	-8182.5	200
1320	G221	-7687.5	319	**1354**	G153	-8197.5	319
1321	G219	-7702.5	200	**1355**	G151	-8212.5	200
1322	G217	-7717.5	319	**1356**	G149	-8227.5	319
1323	G215	-7732.5	200	**1357**	G147	-8242.5	200
1324	G213	-7747.5	319	**1358**	G145	-8257.5	319

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1359	G143	-8272.5	200	**1393**	G75	-8782.5	200
1360	G141	-8287.5	319	**1394**	G73	-8797.5	319
1361	G139	-8302.5	200	**1395**	G71	-8812.5	200
1362	G137	-8317.5	319	**1396**	G69	-8827.5	319
1363	G135	-8332.5	200	**1397**	G67	-8842.5	200
1364	G133	-8347.5	319	**1398**	G65	-8857.5	319
1365	G131	-8362.5	200	**1399**	G63	-8872.5	200
1366	G129	-8377.5	319	**1400**	G61	-8887.5	319
1367	G127	-8392.5	200	**1401**	G59	-8902.5	200
1368	G125	-8407.5	319	**1402**	G57	-8917.5	319
1369	G123	-8422.5	200	**1403**	G55	-8932.5	200
1370	G121	-8437.5	319	**1404**	G53	-8947.5	319
1371	G119	-8452.5	200	**1405**	G51	-8962.5	200
1372	G117	-8467.5	319	**1406**	G49	-8977.5	319
1373	G115	-8482.5	200	**1407**	G47	-8992.5	200
1374	G113	-8497.5	319	**1408**	G45	-9007.5	319
1375	G111	-8512.5	200	**1409**	G43	-9022.5	200
1376	G109	-8527.5	319	**1410**	G41	-9037.5	319
1377	G107	-8542.5	200	**1411**	G39	-9052.5	200
1378	G105	-8557.5	319	**1412**	G37	-9067.5	319
1379	G103	-8572.5	200	**1413**	G35	-9082.5	200
1380	G101	-8587.5	319	**1414**	G33	-9097.5	319
1381	G99	-8602.5	200	**1415**	G31	-9112.5	200
1382	G97	-8617.5	319	**1416**	G29	-9127.5	319
1383	G95	-8632.5	200	**1417**	G27	-9142.5	200
1384	G93	-8647.5	319	**1418**	G25	-9157.5	319
1385	G91	-8662.5	200	**1419**	G23	-9172.5	200
1386	G89	-8677.5	319	**1420**	G21	-9187.5	319
1387	G87	-8692.5	200	**1421**	G19	-9202.5	200
1388	G85	-8707.5	319	**1422**	G17	-9217.5	319
1389	G83	-8722.5	200	**1423**	G15	-9232.5	200
1390	G81	-8737.5	319	**1424**	G13	-9247.5	319
1391	G79	-8752.5	200	**1425**	G11	-9262.5	200
1392	G77	-8767.5	319	**1426**	G9	-9277.5	319

PAD No.	PIN Name	X	Y
1427	G7	-9292.5	200
1428	G5	-9307.5	319
1429	G3	-9322.5	200
1430	G1	-9337.5	319
1431	VGLDMY4	-9352.5	200
1432	DUMMY	-9367.5	319
1433	DUMMYR3	-9382.5	200
1434	DUMMYR4	-9397.5	319

Unit: μm

5 BLOCK DIAGRAM



6 DISPLAY RAM ADDRESS MAP

GS = '1'	GS = '0'	SS = '0'	S1	S2	S3	S4	S5	S6	------	S715	S716	S717	S718	S719	S720
		SS = '1'	S718	S719	S720	S715	S716	S717	-------	S4	S5	S6	S1	S2	S3
		BGR='0'	R	G	B	R	G	B	-------	R	G	B	R	G	B
		BGR='1'	B	G	R	B	G	R		B	G	R	B	G	R
G432	G1	X Address	"0000"h			"0001"h			-------	"00EE"h			"00EF"h		
		Y Address	"0000"h			"0000"h				"0000"h			"0000"h		
G431	G2	X Address	"0000"h			"0001"h			-------	"00EE"h			"00EF"h		
		Y Address	"0001"h			"0001"h				"0001"h			"0001"h		
|	|	|	|			|			-------	|			|		
|	|	|	|			|				|			|		
|	|	|	|			|				|			|		
|	|	|	|			|				|			|		
G2	G431	X Address	"0000"h			"0001"h			-------	"00EE"h			"00EF"h		
		Y Address	"01AE"h			"01AE"h				"01AE"h			"01AE"h		
G1	G432	X Address	"0000"h			"0001"h			-------	"00EE"h			"00EF"h		
		Y Address	"01AF"h			"01AF"h				"01AF"h			"01AF"h		

Figure 1 Display RAM Address Map Table

Note:

X Address Start Instruction：R210h

X Address End Instruction：R211h

Y Address Start Instruction：R212h

Y Address End Instruction：R213h

SS Setting Instruction：R001h

GS Setting Instruction：R400h

BGR Setting Instruction：R003h

7 PIN DESCRIPTION

7.1.. Power Supply Pins

Name	I/O	Description	Connect Pin
VDDI	I	- Power supply for I/O system. - VDDI must be lower than or equal to VDD.	VDDI
VDD	I	- Power supply for digital system. Input voltage level should be the same as VDDA.	VDD
VDDA	I	- Power supply for analog and booster circuits. Input voltage level should be the same as VDD.	VDDA
AGND	I	- System ground for analog system and booster circuit.	GND
DGND	I	- System ground for I/O system and digital system.	GND
VPP	I	- Power supply for internal NVM. - When writing NVM, it needs external power supply voltage (7.5V/10mA). - Leaves these pins open if not used.	-

7.2.. Interface Logic Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>IM2, IM1, IM0/ID</td><td>I</td><td>- The MCU interface mode select.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8080 18-bit Interface</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8080 9-bit Interface</td><td>DB[17:9]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8080 16-bit Interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8080 8-bit Interface</td><td>DB[17:10],</td></tr>
<tr><td>1</td><td>0</td><td>ID</td><td>SPI</td><td>SDI, SDO</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MDDI</td><td rowspan="2">MDDI_DATA
MDDI_STB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>MDDI with Sub-panel Support</td></tr>
</table>
- When the SPI interface is selected, IM0 pin is used for the ID setting.</td><td>GND / VDDI</td></tr>
<tr><td>PROTECT</td><td>I</td><td>Reset protect pin. The ST7793 enters a reset protect status by fixing PROTECT to GND level to prevent hardware reset from noise.
Low: Hardware reset is disabled (Reset protect status)
High: Hardware reset is enabled. (Normal status)</td><td>VDDI</td></tr>
<tr><td>RESET</td><td>I</td><td>- This signal will reset the device and it must be applied to properly initialize the chip.
- Signal is active low.</td><td>MCU</td></tr>
<tr><td>CSX</td><td>I</td><td>- Chip selection pin. Low-active.
- If not used, please fix this pin at VDDI level.</td><td>MCU</td></tr>
<tr><td>DCX (MDDIGND)</td><td>I</td><td>- Display data/command selection (RS) pin in MCU interface.
DCX=’1’: display data or parameter.
DCX=’0’: register index / command.
- In MDDI mode, connect this pin to DGND.
- If not used, please fix this pin at VDDI or DGND level.</td><td>MCU / GND</td></tr>
<tr><td>RDX (MDDIGND)</td><td>I</td><td>- Read enable in 8080 MCU parallel interface. Low-active.
- In MDDI mode, connect this pin to DGND.
- If not used, please fix this pin at VDDI or DGND level.</td><td>MCU / GND</td></tr>
<tr><td>WRX (SCL / MDDI_STB_M)</td><td>I</td><td>- Write enable in MCU parallel interface.
- In SPI mode, this pin is used as SCL.
- MDDI mode, this pin is used as MDDI_STB_M.
- If not used, please fix this pin at VDDI level.</td><td>MCU</td></tr>
<tr><td>VSYNCX</td><td>I</td><td>- Vertical (Frame) synchronizing input signal for RGB interface</td><td>MCU</td></tr>
</table>

Name	I/O	Description	Connect Pin
		operation. VSPL = “0”: Low-active. VSPL = “1”: High-active. - When using MDDI Sub-Display function, this pin is used as CSX for Sub-Display. - Fix to the GND level when not in use.	
HSYNCX	I	- Horizontal (Line) synchronizing input signal for RGB interface operation. HSPL = “0”: Low-active. HSPL = “1”: High-active. - When using MDDI Sub-Display function, this pin is used as DCX for Sub-Display. - Fix to the VDDI or GND level when not in use	MCU
ENABLE	I	- Data enable signal for RGB interface operation. Low: Select (access enabled) High: Not select (access disabled) The EPL bit inverts the polarity of the ENABLE signal. - When using MDDI Sub-Display function, this pin is used as write-strobe for Sub-Display. - If not used, please fix this pin at VDDI or DGND level.	MCU
DOTCLK	I	- Dot clock signal for RGB interface operation. DPL = “0”: Input data on the rising edge of DOTCLK DPL = “1”: Input data on the falling edge of DOTCLK -If not used, please fix this pin at VDDI or DGND level.	MCU
SDI	I	- SPI interface input pin. - The data is latched on the rising edge of the SCL signal. - If not used, please fix this pin at VDDI or DGND level.	MCU
SDO	O	- SPI interface output pin. - The data is outputted on the falling edge of the SCL signal. If not used, please fix this pin at floating.	MCU
DB[17:0]	I/O	- In MCU 8080 parallel interface, DB[17:0] are used as data bus. 8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. - In RGB interface, DB[17:0] are used as data bus.	MCU / MDDI / GND

Name	I/O	Description	Connect Pin
		16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. - In MDDI mode MDDIGND(DB[8, 6, 4, 3, 1]): connect these to VDDI or DGND level.. MDDI_DATA_P(DB[7]) MDDI_DATA_M(DB[5]) MDDI_STB_P(DB[2]) - In MDDI mode with 8-/16-bit Sub-Display DB[17:10] is used as data[7:0] for sub-display. - In MDDI mode with 9-/18-bit Sub-Display DB[17:9] is used as data[8:0] for sub-display/ - If not used, please fix this pin at VDDI or DGND level.	
FMARK	O	- Output a frame head pulse signal is used as synchronies MCU to frame rate - If not used, leave this pin open	MCU
EPROGEN	I	- NVM write enable. When EPROGEN = 1, NVM can be written. - If not used, leave it open	

Note1. "1" = VDDI level, "0" = DGND level.

Note2. When in parallel mode, unused data pins must be connected to "1" or "0".

Note3. When CSX="1", there is no influence to the parallel and serial interface.

7.3.. Driver Output Pins

Name	I/O	Description	Connect pin
S1 to S720	O	- Source driver output pins - To change the shift direction of signal outputs, use the SS bit. SS = “0”, the data in the RAM address “00000h” is output from S1. SS = “1”, the data in the RAM address “00000h” is output from S720. - When SS=”0” S1, S4, S7, … display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9 ... display blue (B)	LCD
G1 to G432	O	- Gate driver output pins. VGH: Selecting Gate Lines Level. VGL: Non-selecting Gate Lines Level.	LCD
AVDD	O	- Power output pin for monitoring analogy circuit. - Leave open when not in use.	-
AVCL	O	- Power output pin for monitoring analogy circuit. - Leave open when not in use.	-
VGH	O	- Power output pin for gate driver - Leave open when not in use.	-
VGL	O	- Power output (Negative) pin for gate driver - Leave open when not in use.	-
VCC	O	- Monitoring pin of internal digital reference voltage. - Leave open when not in use.	-
VCOM	O	- A power supply for the TFT-LCD common electrode.	Common Electrode

7.4.. Test and Other Pins

Name	I/O	Description	Connect pin
DGNDDUM1-10 AGNDDUM1-5 VDDDUM1 VDDIDUM1-2	O	- Use these pins to fix the electrical potentials of unused interface and test pins. - Leave open when not in use.	-
DUMMYR1-4	-	- For use of COG contact resistance measurement. - Leave open when not in use.	-
VGLDMY1-4	O	- Output VGL level. - Used for fixing unused gate line of the panel. - Leave open when not in use.	Unused Gate Lines
PVAN, PVSFTN, PVSFTP, PVAP	O	- Used for monitoring - Leave open.	-
TS[11:0]	O	- In MDDI mode with 16-bit Sub-Display TS[11:9] & TS[5:1] are used as data[15:8] for sub-display. - In MDDI mode with 18-bit Sub-Display TS[11:9] & TS[5:0] are used as data[17:9] for sub-display. - Leave open when not in use.	-
TEST[5:1]	I	- Used for Driver vender test. - Leave open.	-
VDDS PV22 VDDGX	O	- Used for monitoring - Leave open	-
Dummy	-	- These pins are dummy - Leave open	-

8 DRIVER ELECTRICAL CHARACTERISTICS

8.1.. Absolute Operation Range

Item	Symbol	Range	Unit
Supply Voltage (Analog)	VDDA	- 0.3 ~ +4.6	V
Supply Voltage (I/O)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VDD	- 0.3 ~ +4.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
NVM Supply Voltage (Write)	VPP	-0.3 ~ +8.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +110	℃

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

8.2.. DC Characteristics

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD / VDDA	Operating voltage	2.5	2.75	3.3	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	VDD	V	
Gate Driver High Voltage	VGH		12.16	-	15.05	V	
Gate Driver Low Voltage	VGL		-12.37	-	-7.7	V	
Gate Driver Supply Voltage		| VGH-VGL |	-	-	27.4	V	
Current consumption Shoutdown operation	IDDA	VDDI=VDD=2.8v	12	--	30		
Input / Output							
Logic-High Input Voltage	VIH		0.8VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.2VDDI	V	Note 1
Differential Input High Threshold Voltage	VIT+			0	50	mV	MDDI_STB, MDDI_DATA
Differential Input Low Threshold Voltage	VIT-		-50	0		mV	
Single-ended Receiver Input Operation Voltage Range	VIR		0.5		1.2	V	
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	ILI	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM Voltage	VCOM		-	0	-	V	
Source Driver							
Source Output Range	VSout		-4.2		+6.4	V	
Source Output Settling Time	Tr	Below with 99% precision			20	us	Note 2
Output Offset Voltage	VOFFSET				35	mV	Note 3

Table 2 Basic DC Characteristics

Notes:

1. TA= -30 to 85℃.

2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

3. The max. value is between measured point of source output and gamma setting value.

8.3.. AC Characteristics

8.3.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

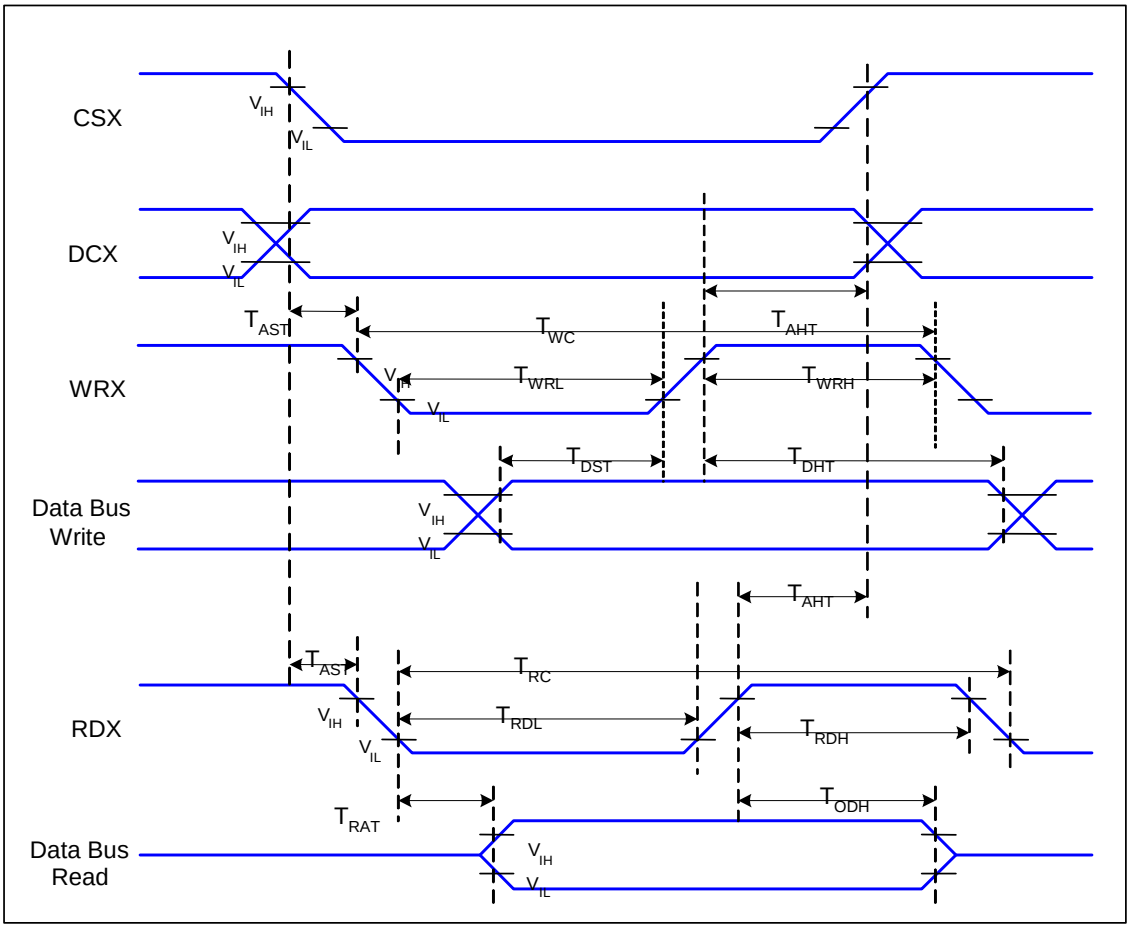


Figure 2 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
DCX	TAST	Address Setup Time	0	--	ns	
	TAHT	Address Hold Time (Write/Read)	2	--	ns	
WRX	TWC	Write Cycle	75	--	ns	
	TWRH	Control Pulse “H” Duration	25	--	ns	
	TWRL	Control Pulse “L” Duration	30	--	ns	
RDX	TRC	Read Cycle (ID)	450	--	ns	When Read ID Data
	TRDH	Control Pulse “H” Duration (ID)	250	--	ns	
	TRDL	Control Pulse “L” Duration (ID)	170	--	ns	

Signal	Symbol	Parameter	Min	Max	Unit	Description
DB[17:0]	TDST	Data Setup Time	20	--	ns	TRAT, TRATFM: 3K ohm Pull up or Down and 30pF Parallel Cap. To GND. TODH: 3K ohm Pull up or Down.
	TDHT	Data Hold Time	10	--	ns	
	TRAT	Read Access Time (ID)	--	150	ns	
	TODH	Output Disable Time	10	--	ns	

Table 3 8080 Parallel Interface Characteristics

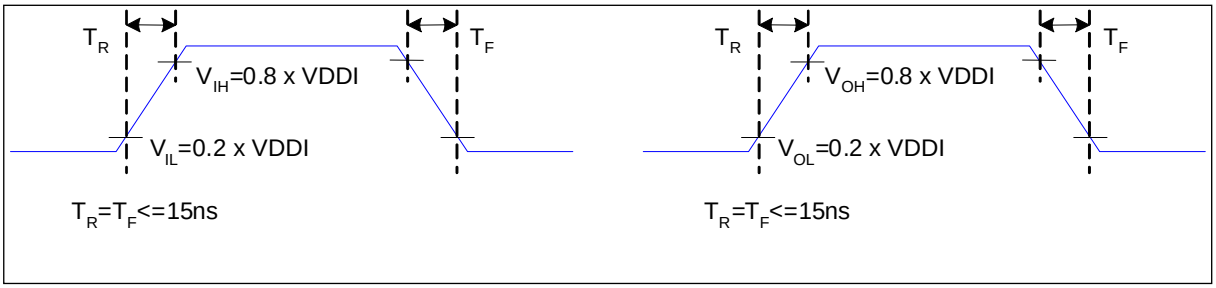


Figure 3 Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

8.3.2 Serial Data Transfer Interface Characteristics:

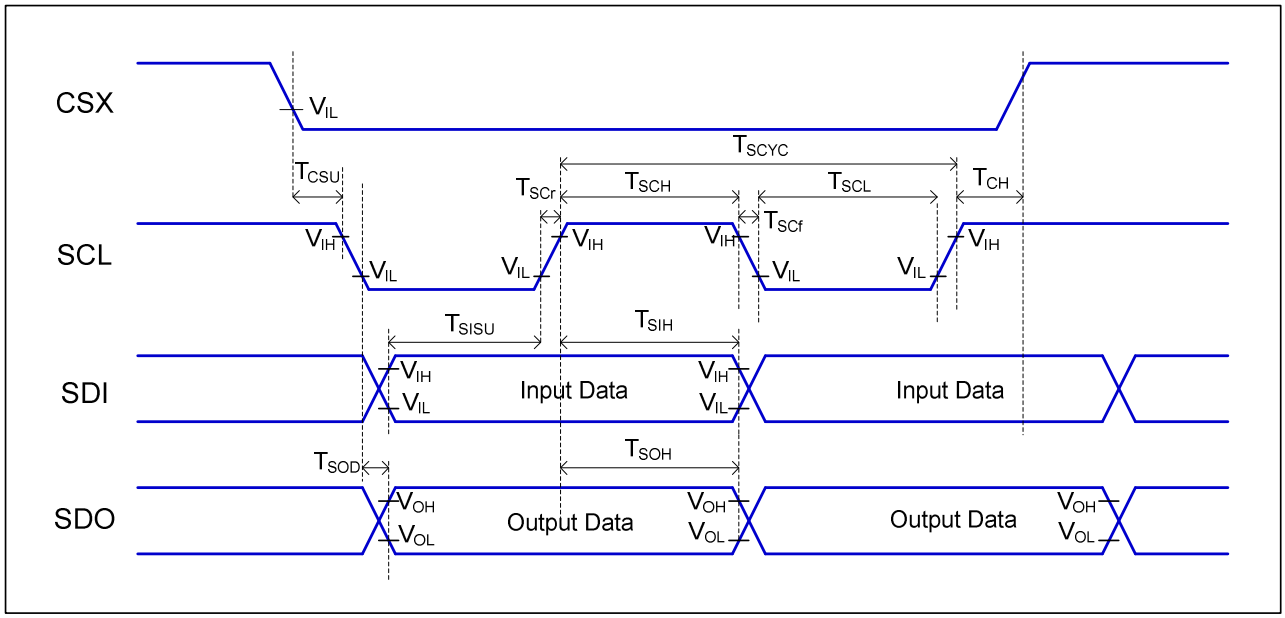


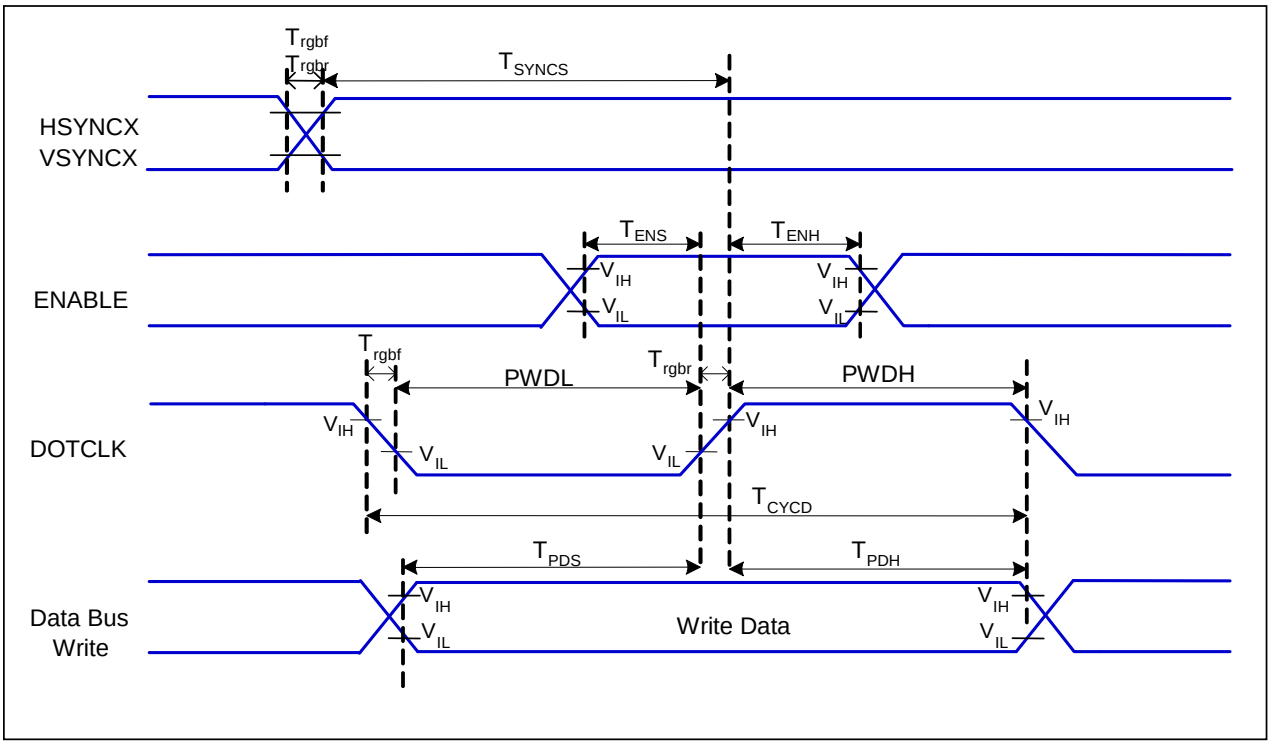
Figure 4 SPI Interface Timing Characteristics

VDDI=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	TCSU	Chip Select Setup Time	20		ns	-
	TCH	Chip Select Hold Time	60		ns	
SCL	TSCH	SCL “H” pulse width (Write)	40		ns	
	TSCH	SCL “H” pulse width (Read)	150		ns	
	TSCYC	Serial clock cycle (Write)	100		ns	
	TSCYC	Serial clock cycle (Read)	350		ns	
	TSCL	SCL “L” pulse width (Write)	40		ns	
	TSCL	SCL “L” pulse width (Read)	150		ns	
SDI	TSISU	Serial Input Data Setup Time	30		ns	
	TSIH	Serial Input Data Hold Time	30		ns	
SDO	TSOD	Serial Output Data Setup Time	--	130	ns	
	TSOH	Serial Output Data Hold Time	10	--	ns	

Table 4 SPI Interface Characteristics

8.3.3 RGB Interface Characteristics:



VDDI=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNCX VSYNCX	TSYNCS	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	TENS	Enable Setup Time	30	-	ns	
	TENH	Enable Hold Time	30	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	40	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	40	-	ns	
	TCYCD	DOTCLK Cycle Time	100	-	ns	
DB	TPDS	PD Data Setup Time	40	-	ns	
	TPDH	PD Data Hold Time	40	-	ns	

Table 5 RGB Interface Timing Characteristics

9 INTERFACE

9.1.. MPU Interface Type Selection

For communicating with MCU, ST7793 supports 8-/9-/16-/18-bit 8080-series interface, SPI, and MDDI. Selection of these interfaces are set by IM[2:0] pins as shown below.

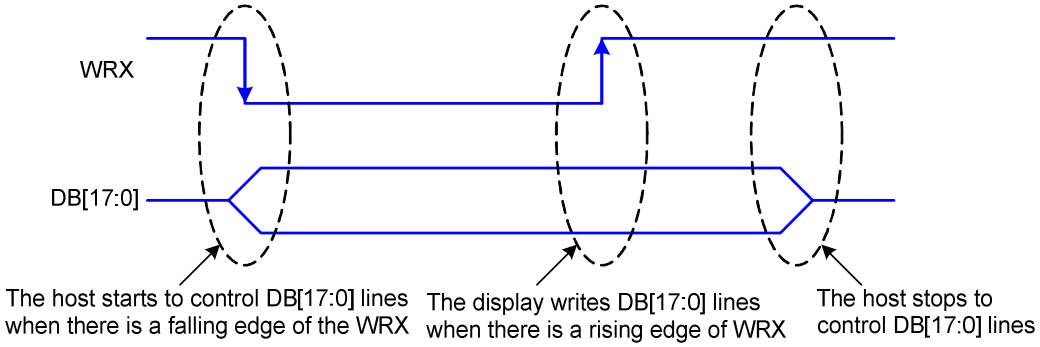
IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	8080-series MCU 18-bit	Pixel Data: 18-bit, Parameter: 16-bit
0	0	1	8080-series MCU 9-bit	Pixel Data: 9-bit, Parameter: 8-bit
0	1	0	8080-series MCU 16-bit	Pixel Data: 16-bit, Parameter: 16-bit
0	1	1	8080-series MCU 8-bit	Pixel Data: 8-bit, Parameter: 8-bit
1	0	ID	Serial Peripheral Interface(SPI)	Pixel Data: 16-bit, Parameter: 16-bit
1	1	0	MDDI	N/A
1	1	1	MDDI with Sub-panel Support	N/A

Table 6 Interface Type Selection

9.2.. 8080-Series MCU Interface

9.2.1 8080-Series MCU Write Cycle Sequence

The write cycle means that the host writes information (register index / parameter) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[17:0]). DCX is a control signal, which tells if the data is an index or a parameter. The data signals represent index number if the signal is low (DCX='0') and vice versa the data signals represent parameter (DCX='1').



Note: WRX is an synchronized signal (It can be stopped).

Figure 6 8080-Series WRX Protocol

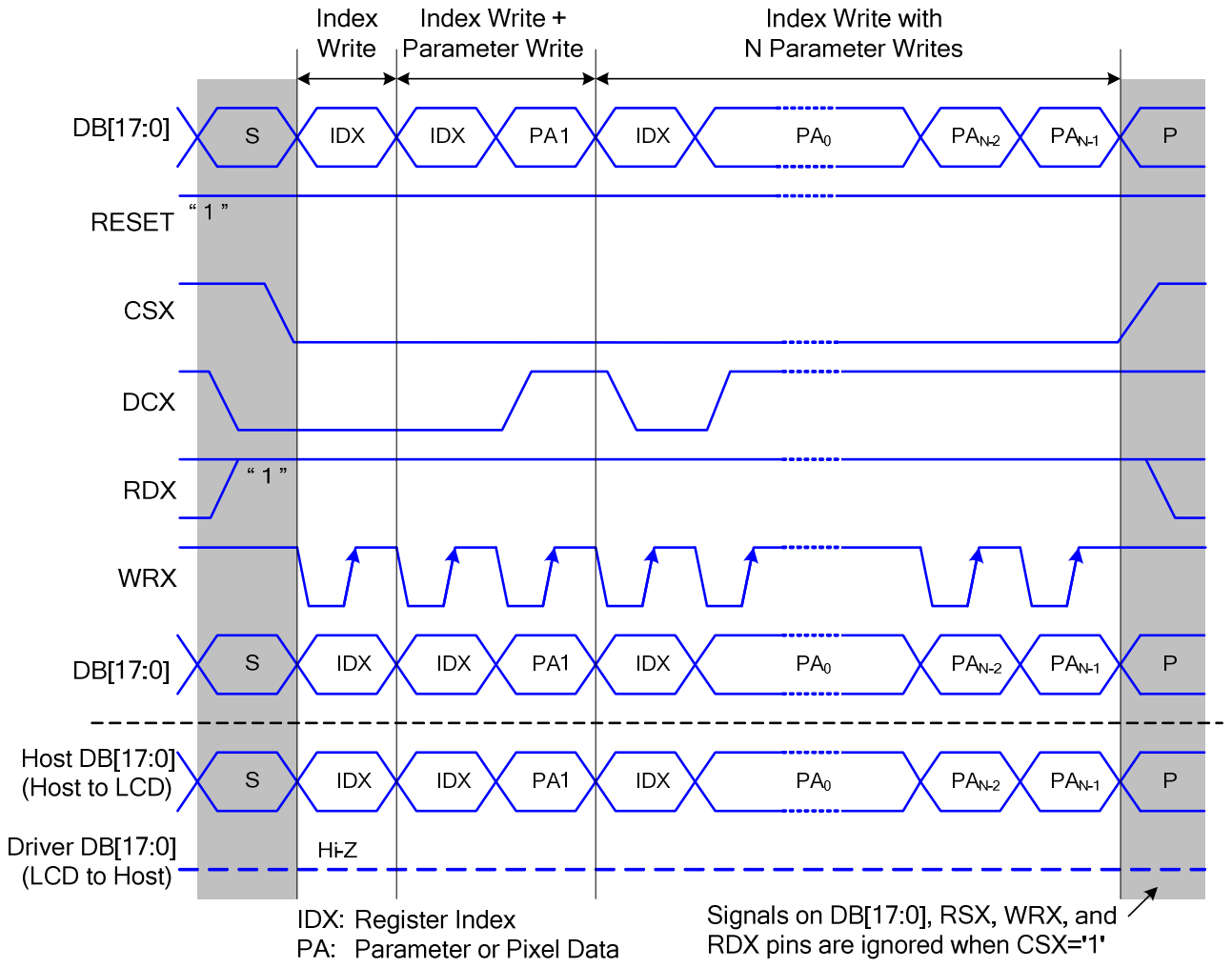


Figure 7 8080-Series Parallel Bus Protocol, Write to Register or Display RAM

9.2.2 18-bit 8080-Series Interface Write Format

The 18-bit 8080-series interface is selected by setting the IM [2:0] =”000”.

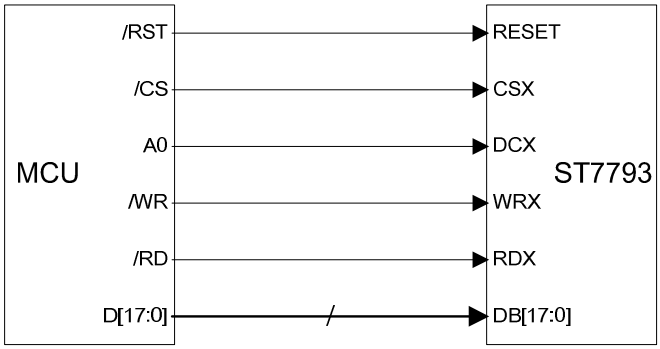


Figure 8 18-bit 8080-Series Interface Connection

This mode accepts only 262k colors format in display. In this interface, index, parameter, and pixel-data

should be written according to the following figures.

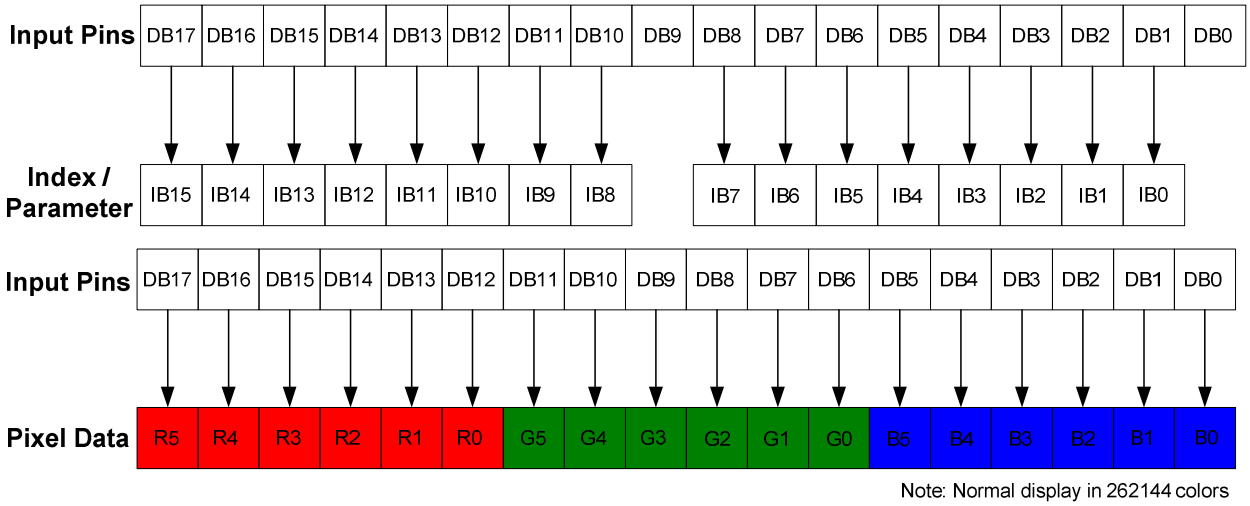


Figure 9 18-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)

9.2.3 16-bit 8080-Series Interface Write Format

The 16-bit 8080-series interface is selected by setting IM[2:0]=”010”.

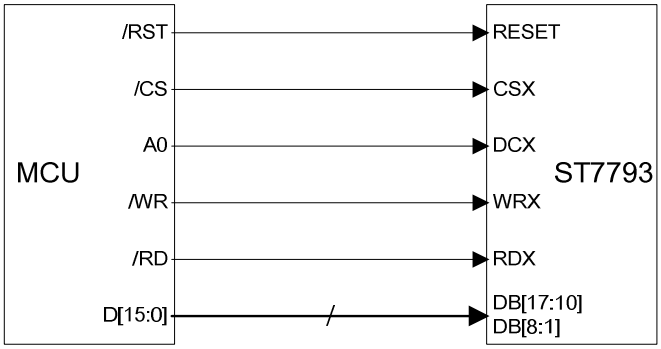
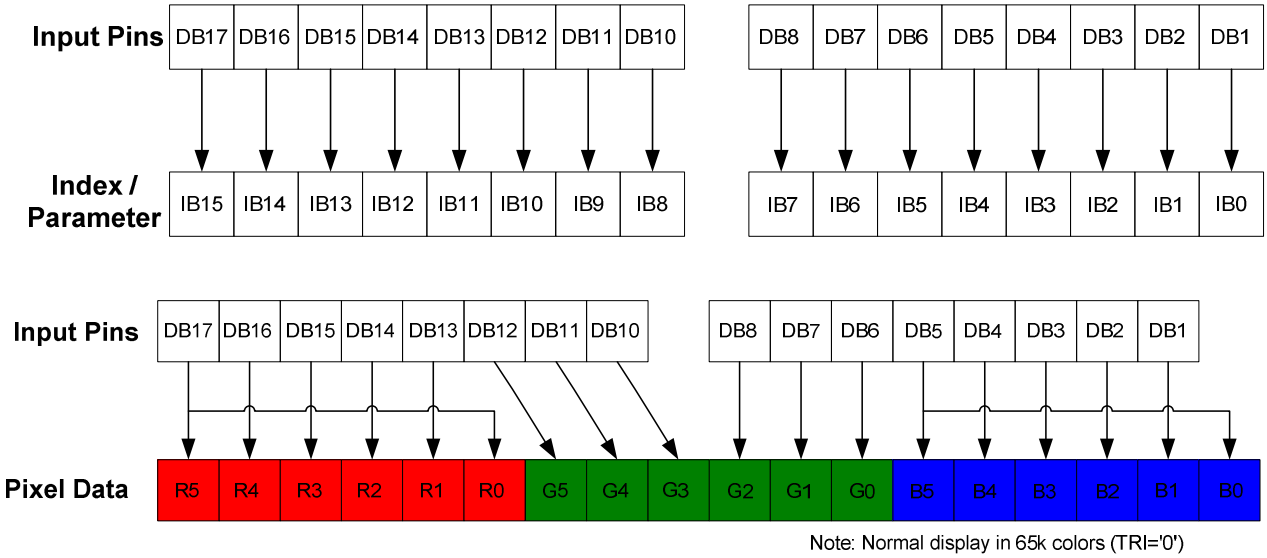


Figure 10 16-bit 8080-Series Interface Connection

ST7793 accepts 262k-color or 65k-color format in this mode. When the 262k-color format is used, two transfers for each pixel are required.



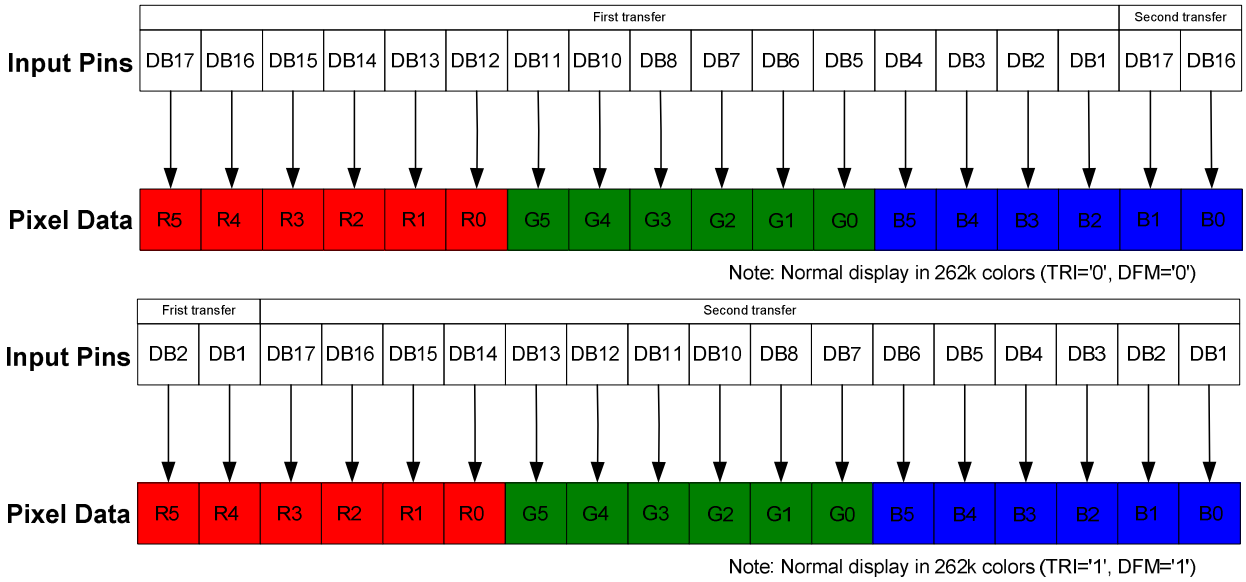


Figure 11 16-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)

9.2.4 9-bit 8080-Series Interface Write Format

The 9-bit 8080-series interface is selected by setting the IM [2:0] = “011” and the DB [17:9] pins are used to transfer data. Since the register data-width is 16-bit, the data is divided into upper byte and lower byte, and the upper byte is transferred first. The display data is also divided into upper part and lower part (9-bit for each part), and the upper part is transferred first. The unused DB [8:0] pins must be tied to either VDDI or DGND.

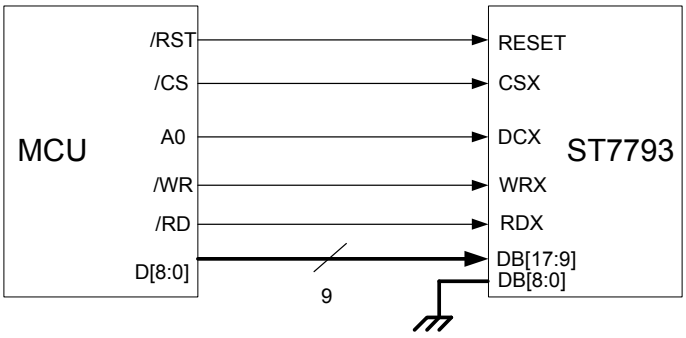
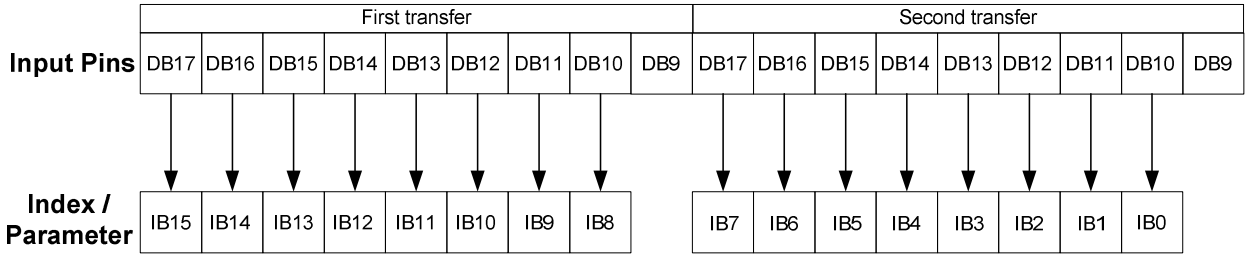


Figure 12 9-bit 8080-Series Interface Connection



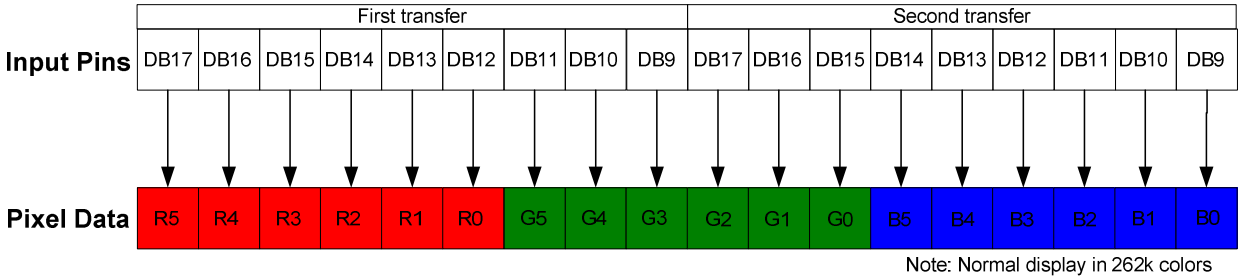


Figure 13 9-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)

9.2.5 8-bit 8080-Series Interface Write Format

The 8080 8-bit interface is selected by setting the IM [2:0] as “011” and the DB [17:10] pins are used to transfer data. The mode accepts 262k-color or 65k-color format. When writing the 16-bit register, the data is divided into two bytes and the upper byte is transferred first. The display data is also divided into upper byte and lower byte, and the upper byte is transferred first. The written data is expanded into 18-bit internally (see the figure below) and then written into DRAM. The unused DB [9:0] pins must be tied to either VDDI or DGND.

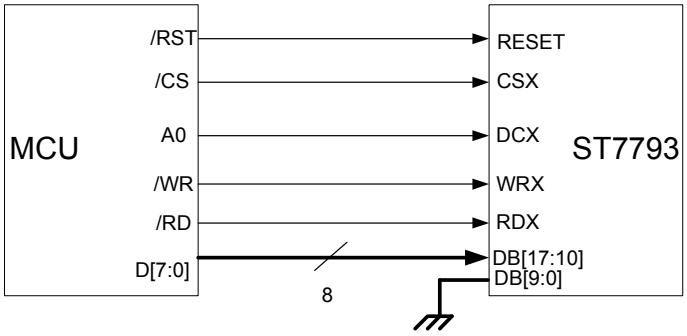


Figure 14 8-bit 8080-Series Interface Connection

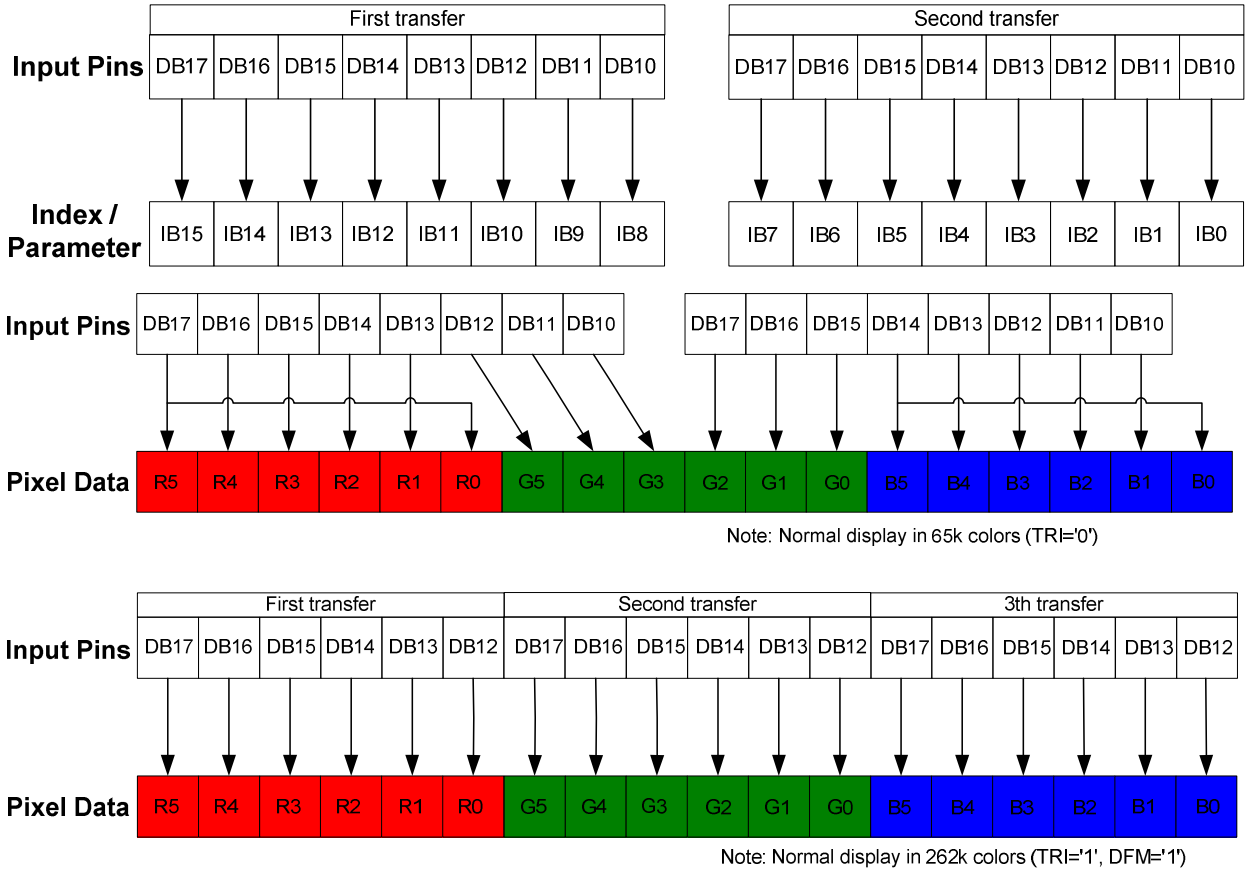
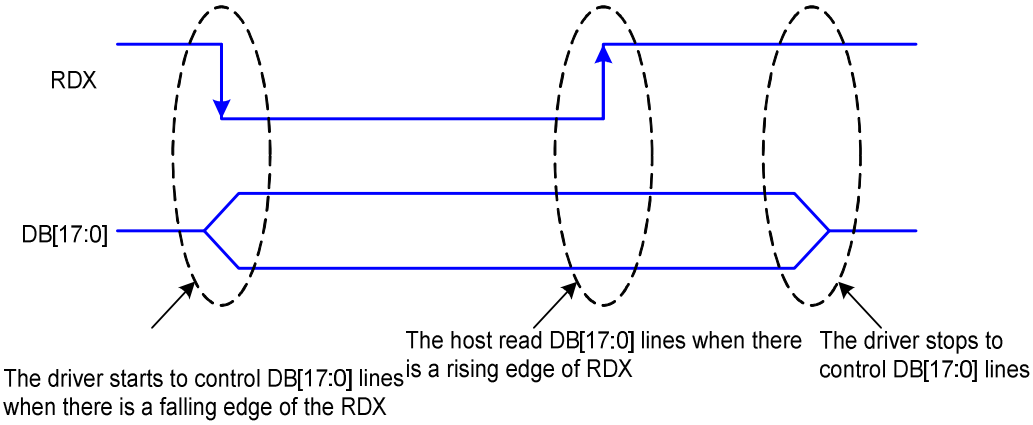


Figure 15 8-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)

9.2.6 8080-series MCU Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The driver sends data (DB [17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



Note1: RDX is an unsynchronized signal (It can be stopped)

Figure 16 8080-Series RDX Protocol

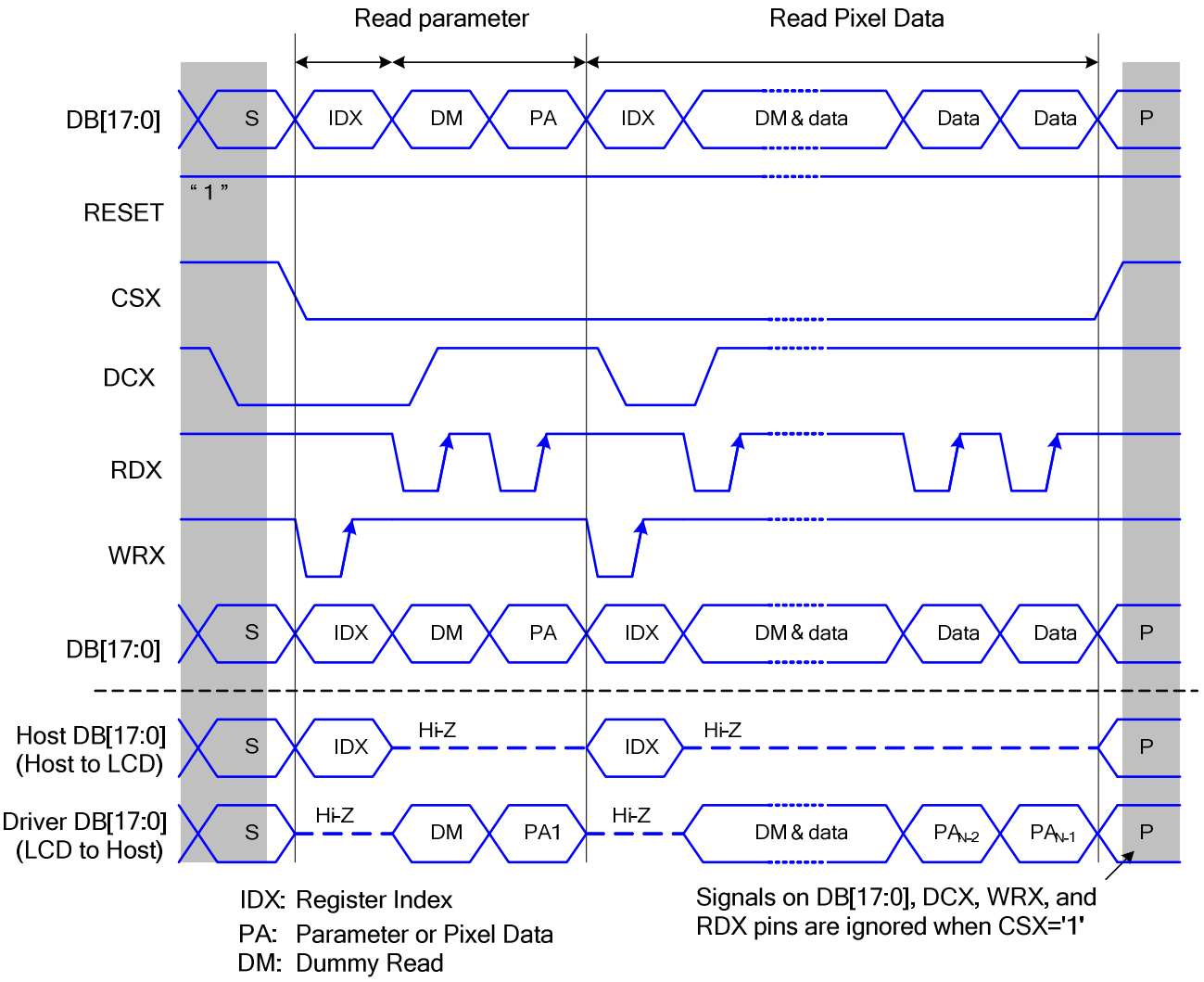


Figure 17 8080-Series Parallel Bus Protocol, Read from Register or Display RAM

9.2.7 18-bit 8080-Series Interface Read Format

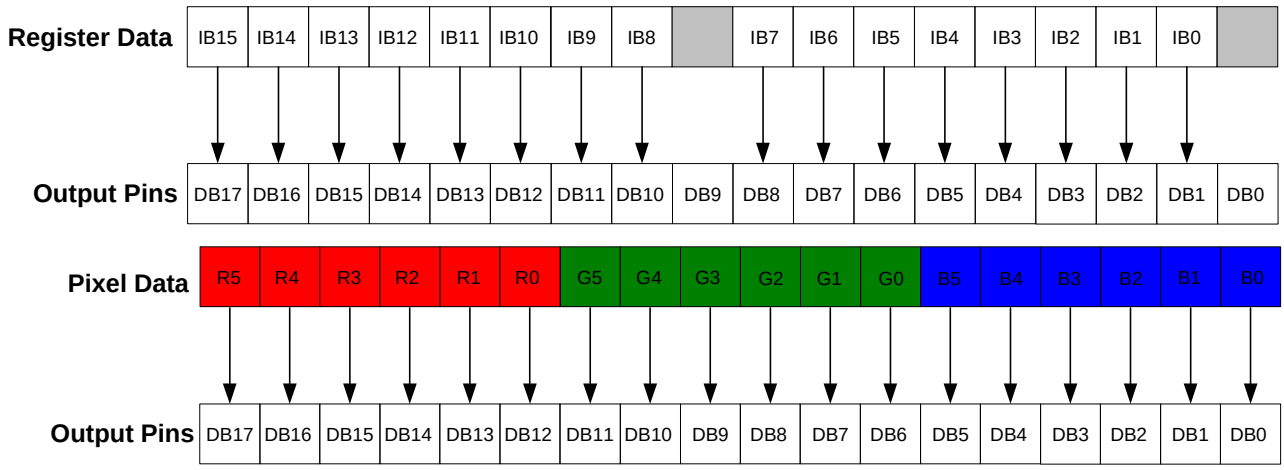


Figure 18 18-bit 8080-Series Interface Data Format (Register/Pixel Data Read)

9.2.8 16-bit 8080-Series Interface Read Format

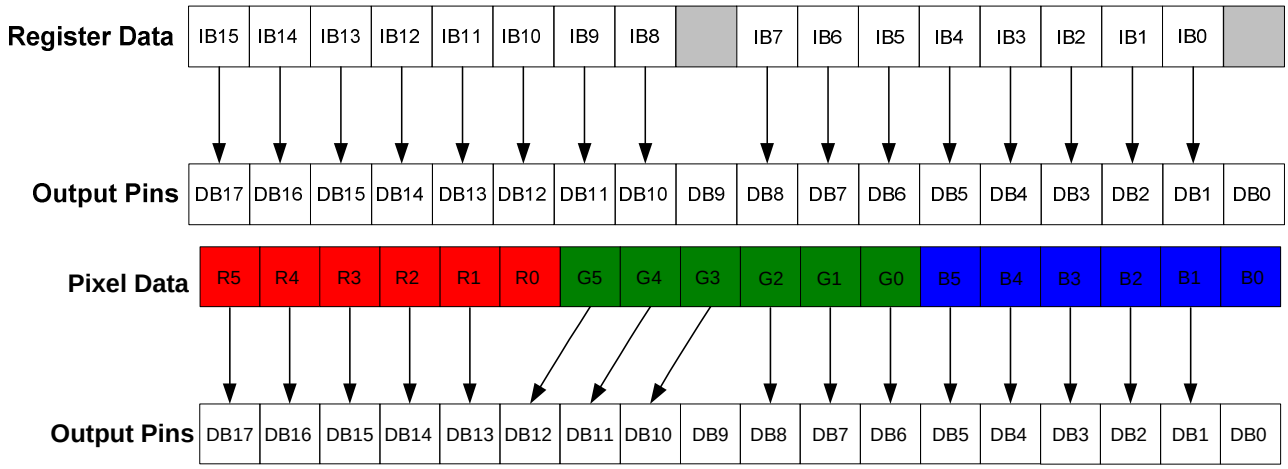


Figure 19 16-bit 8080-Series Interface Data Format (Register/Pixel Data Read)

9.2.9 9-bit 8080-Series Interface Read Format

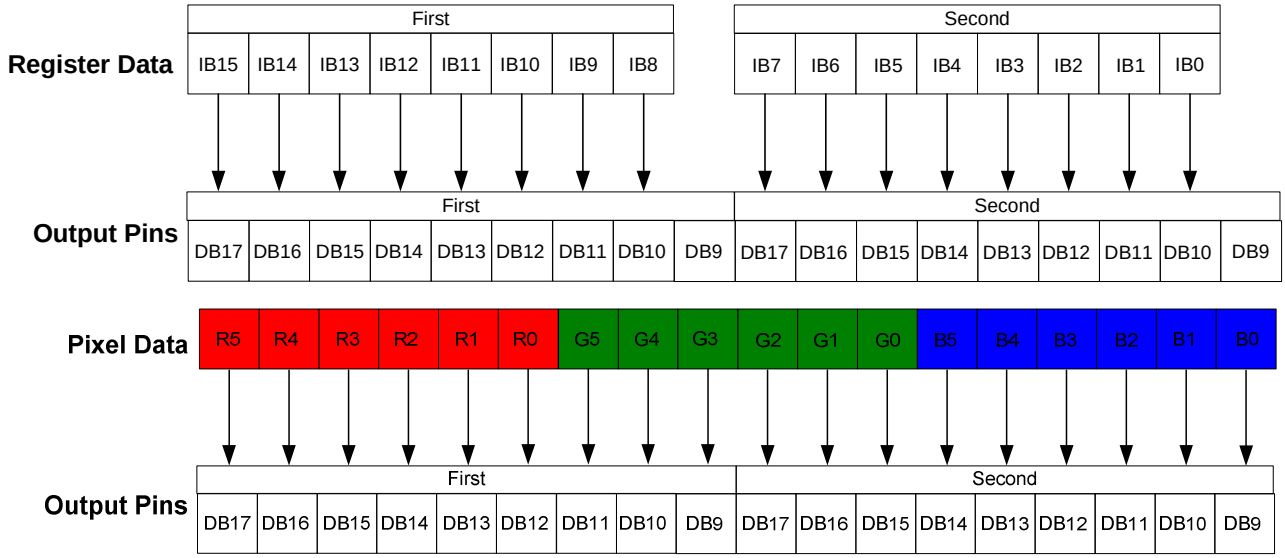


Figure 20 9-bit 8080-Series Interface Data Format (Register/Pixel Data Read)

9.2.10 8-bit 8080-Series Interface Read Format

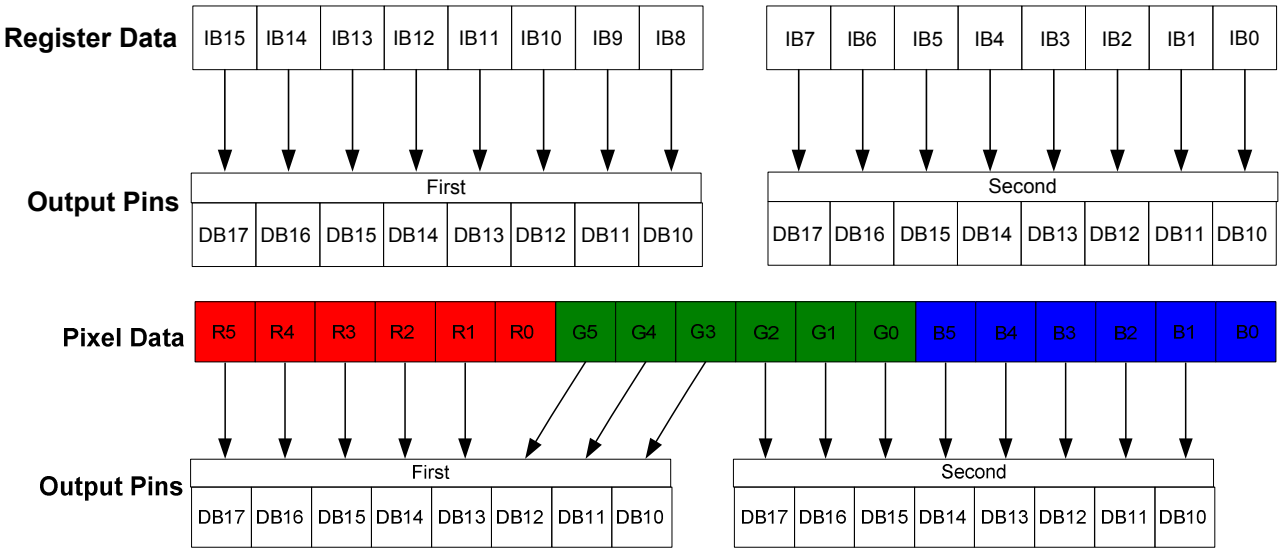


Figure 21 8-bit 8080-Series Interface Data Format (Register/Pixel Data Read)

9.3.. RGB Interface

9.3.1 RGB Interface Display Operation

The display operation via the RGB interface is synchronized with the VSYNCX, HSYNCX, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing. Polarities of VSYNCX, HSYNCX, ENABLE, and DOTCLK can be changed by setting the DPL, EPL, HSPL, and VSPL bits (R00Fh). When RGB interface is used, instructions should be transferred via SPI interface. RGB and 8080-series interface cannot be used simultaneously.

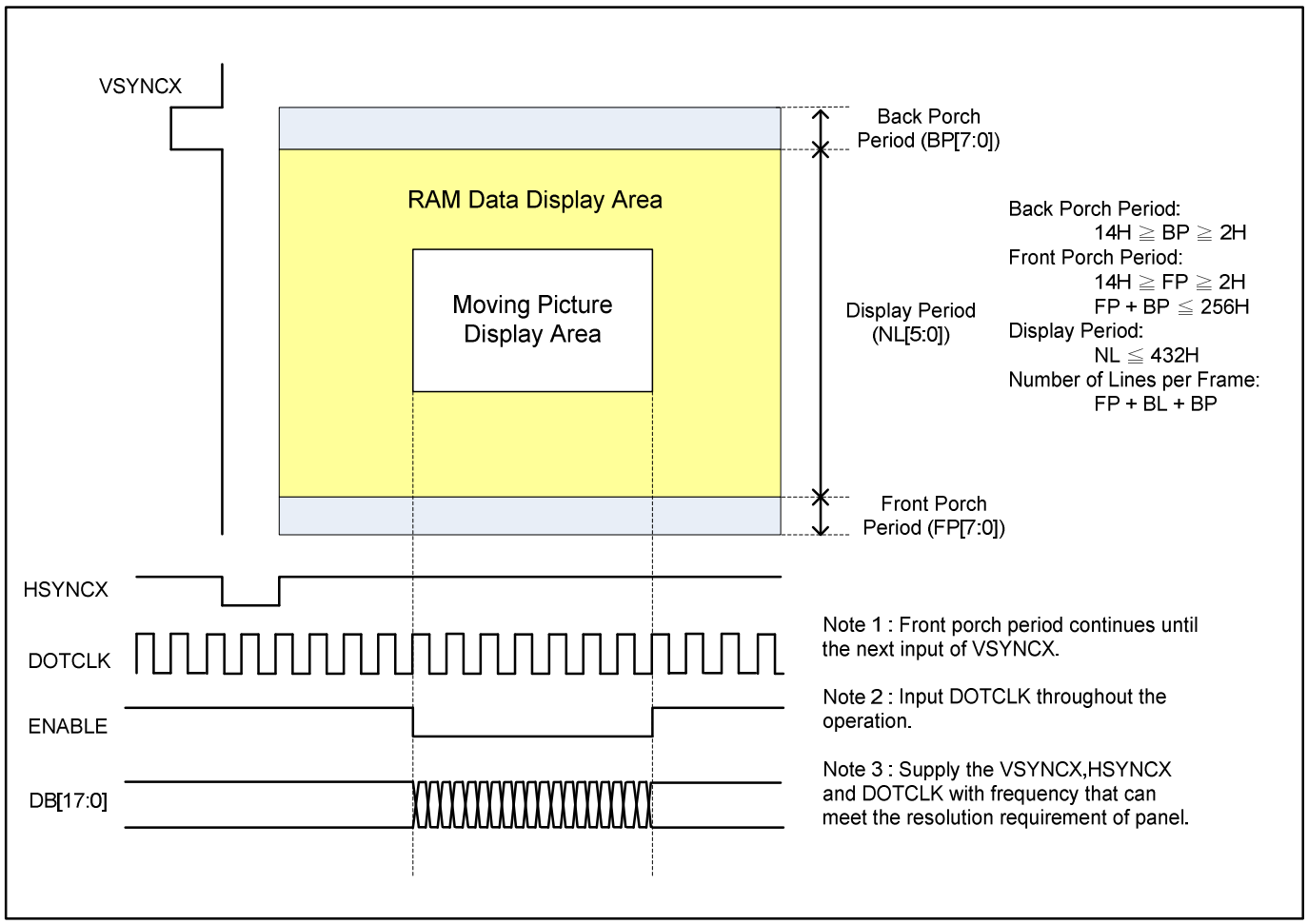


Figure 22 Display RAM Access Area via RGB Interface

9.3.2 RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as the following.

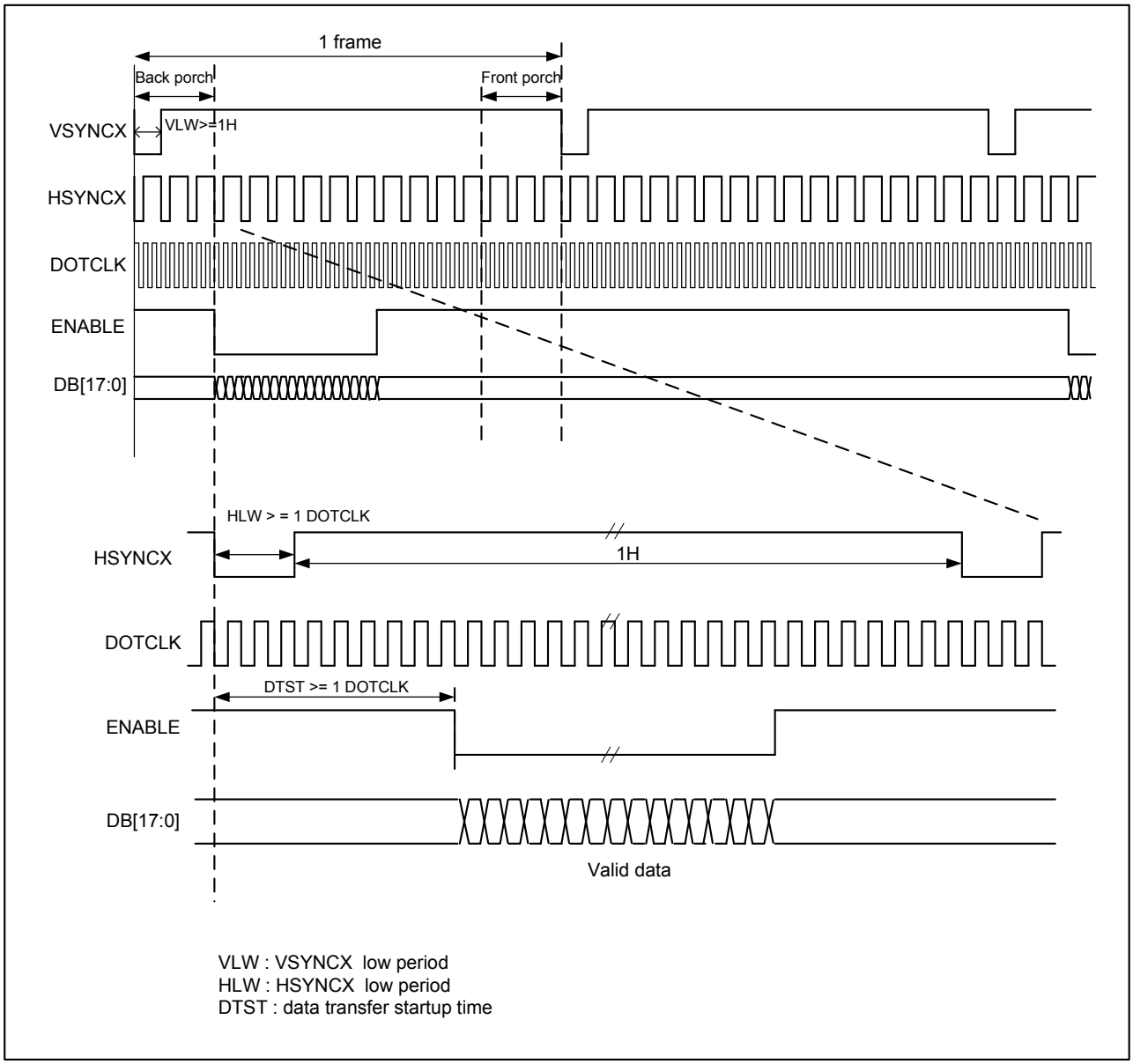


Figure 23 18-/16-bit RGB Interface Signal Relationship

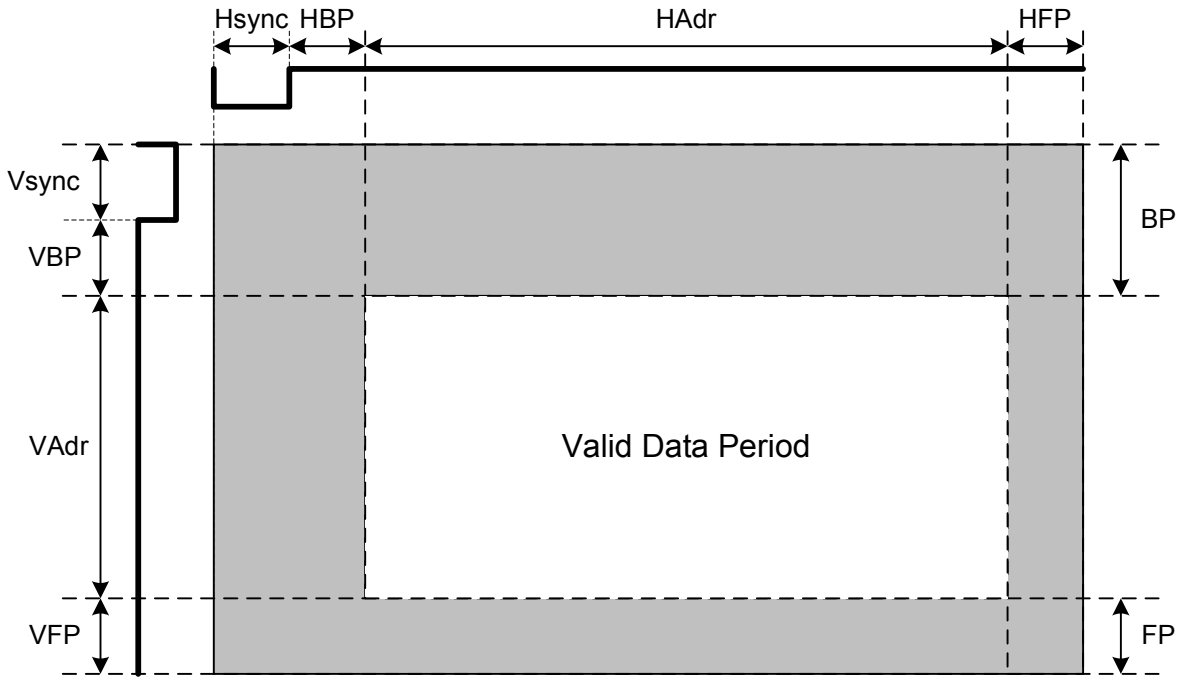


Figure 24 RGB Interface Timing Chart

The timing chart of RGB interface must meet the following table:

Parameters	Symbols	Min.	Typ.	Max.	Unit
Horizontal Synchronization	Hsync	2	10	16	DOTCLK
Horizontal Back Porch	HBP	2	20	24	DOTCLK
Horizontal Address	HAdr	-	240	-	DOTCLK
Horizontal Front Porch	HFP	2	10	16	DOTCLK
Vertical Synchronization	Vsync	1	2	4	Line
Vertical Back Porch	VBP	1	2	-	Line
Vertical Address	VAdr	-	432	-	Line
Vertical Front Porch	VFP	3	4	-	Line

9.3.3 Moving Picture Mode

ST7793 has the RGB interface to display moving picture and incorporates Display RAM to store display data (DRAM), which has following merits in displaying a moving picture.

- The window address function defined the update area of Display RAM.
- The Display RAM is updated only the moving picture area.
- It can contribute to lower the power consumption of the system by reducing data transfer.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched to system interface (8080-series) to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

ST7793 allows Display RAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal Display RAM in synchronization with DOTCLK while ENABLE signal is “Low”. When write data to the internal Display RAM by the system interface, set ENABLE(“High”) to stop write data via RGB interface. Then set RM = ‘0’ to enable RAM access via system interface. When restarting DRAM access in RGB interface mode, wait for one read/write cycle, set RM = ‘1’ and then the index register (R202h) to start accessing RAM via the RGB interface. If Display RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal Display RAM.

The following figure illustrates the operation of the ST7793 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

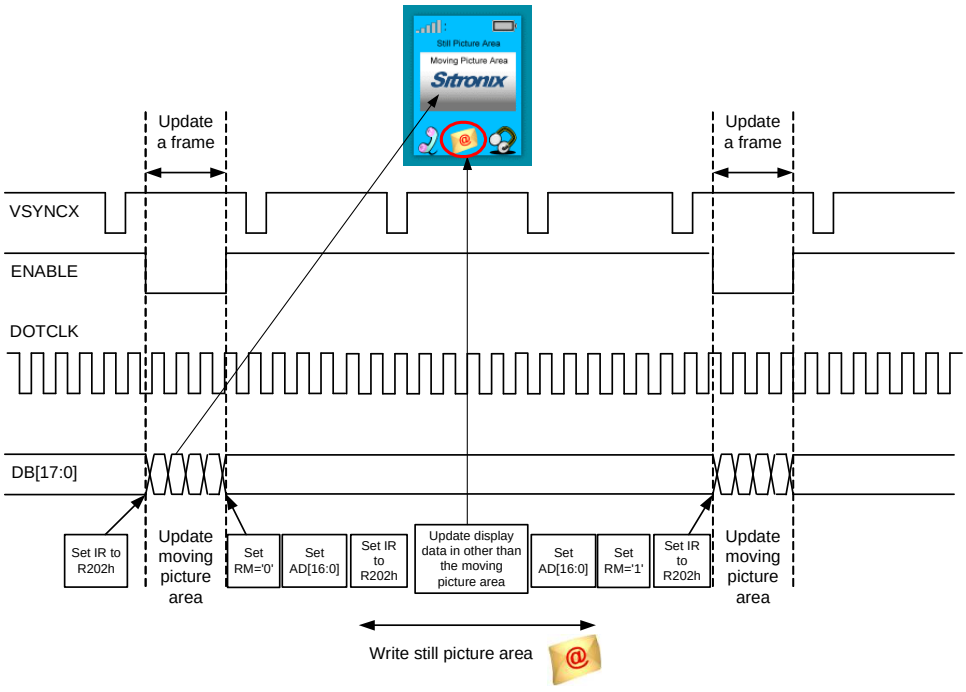


Figure 25 Example of updating the still and moving pictures

9.3.4 18-bit RGB Interface

The RGB Interface mode for ST7793 is selected by setting the RIM bit as following table.

RIM	RGB Interface Mode	Data Pins
0	18-bit RGB Interface	DB[17:0]
1	16-bit RGB Interface	DB[17:13], DB[11:1]

The 18-bit RGB interface is selected by setting the RIM bits to '0'. The display operation is synchronized with VSYNCX, HSYNCX, and DOTCLK signals. Display data are transferred to the Display RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.

When RIM='0', the display data format is as the following figure

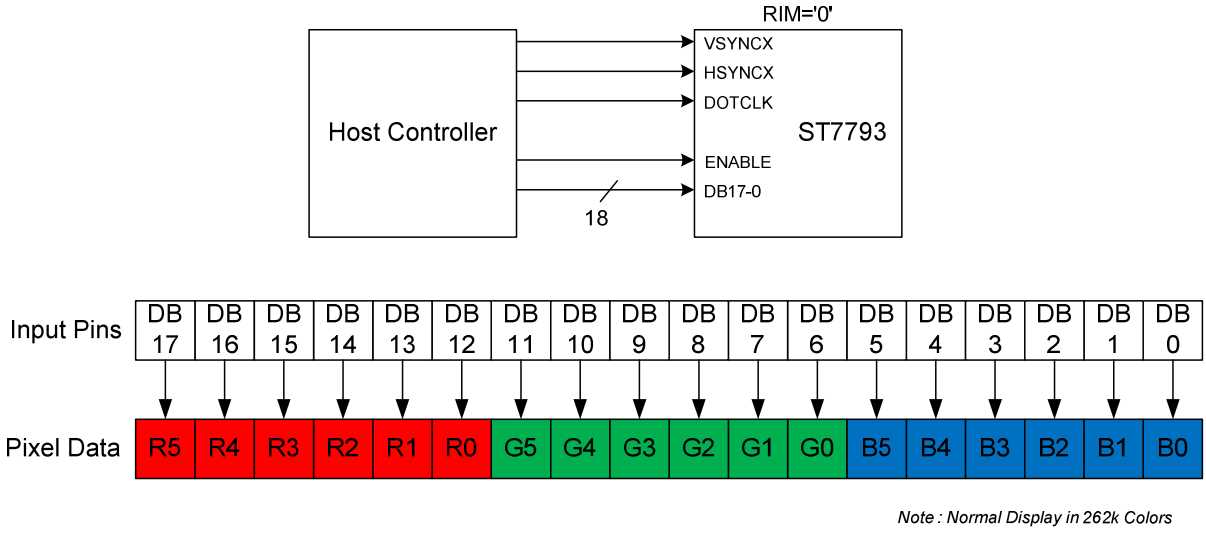


Figure 26 18-bit RGB Interface Data Format

9.3.5 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM bits to '1'. The display operation is synchronized with VSYNCX, HSYNCX, and DOTCLK signals. Display data are transferred to the Display RAM in synchronization with the display operation via 16-bit RGB data bus (DB[17:13], DB[11:1]) according to the data enable signal (ENABLE). Registers are set only via the system interface.

When RIM='1', the display data format is as the following figure:

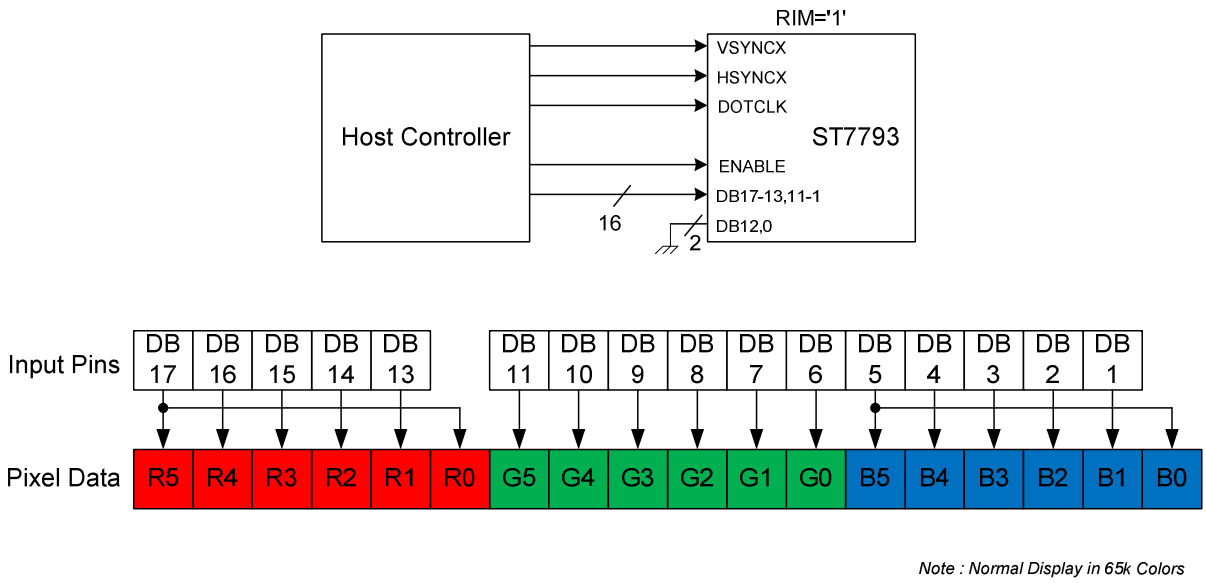


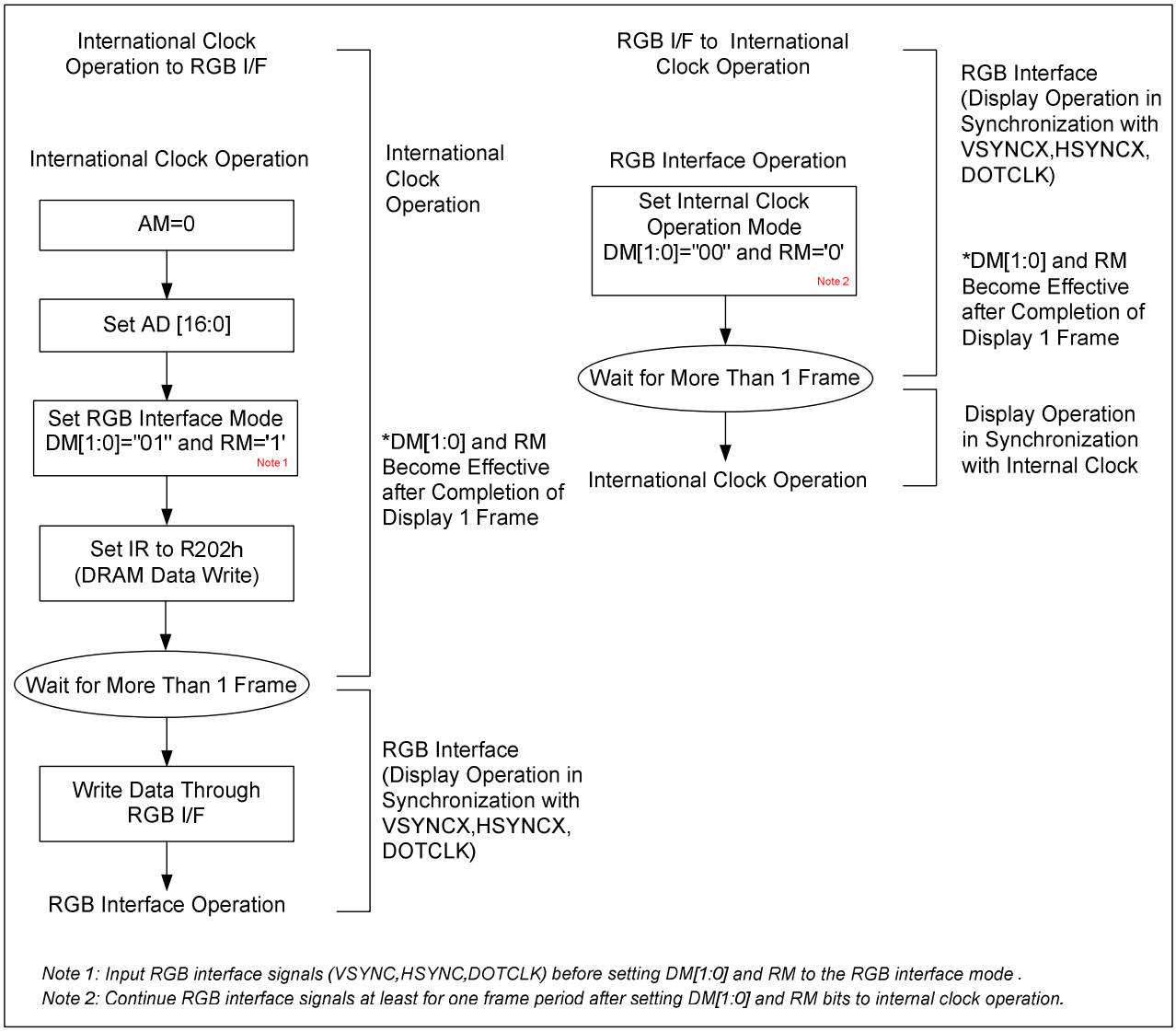
Figure 27 16-bit RGB Interface Data Format

Notes to external display in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available

2. VSYNCX, HSYNCX, and DOTCLK signals must be supplied during a display operation period.
3. In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.
4. In RGB interface mode, the front porch period continues until the next VSYNCX input is detected after drawing one frame.
5. In RGB interface mode, a RAM address (AD[16:0]) is set in the address counter every frame on the falling edge of VSYNCX.
6. When switching between the internal operation mode and the external display interface operation mode, the sequences below should be followed.



Note 1: Input RGB interface signals (VSYNC,HSYNC,DOTCLK) before setting DM[1:0] and RM to the RGB interface mode .
Note 2: Continue RGB interface signals at least for one frame period after setting DM[1:0] and RM bits to internal clock operation.

Figure 28 Internal Clock Operation / RGB Interface Mode Switching Sequences

9.4.. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[2:0] pins as “10x” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND.

The SPI interface operation enables from the falling edge of CSX and ends of data transfer on the rising edge of CSX. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ST7793.

The seventh bit of start byte is RS bit. When RS = ‘0’, either index write operation or status read operation is executed. When RS = ‘1’, either parameter write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is ‘0’ and read back when the R/W bit is ‘1’.

After receiving the start byte, ST7793 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ST7793 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

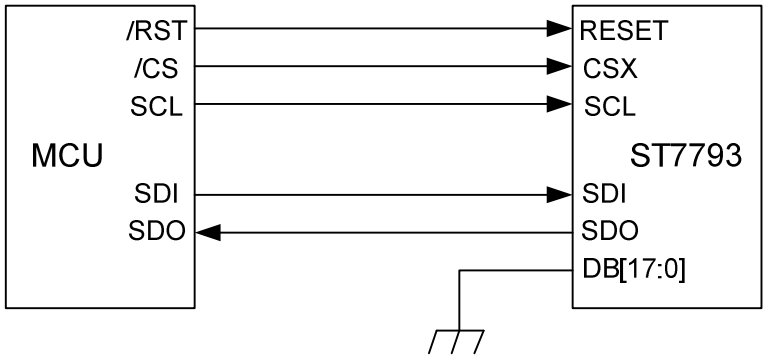
Start Byte Format

Transfer Bit-Order	S	1	2	3	4	5	6	7	8
Start Byte Format	Transfer Starts	Device ID Code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

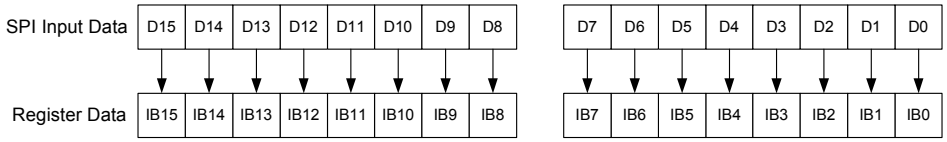
Notes: ID bit is selected by setting the IM0/ID pin

RS and R/W Bit Function

RS	R/W	Function
0	0	Set index register
0	1	(Setting inhibited)
1	0	Write to register or Display RAM
1	1	Read from register or Display RAM



Register Access in Serial Peripheral Interface (Index / Parameter)



Display RAM Write in Serial Peripheral Interface

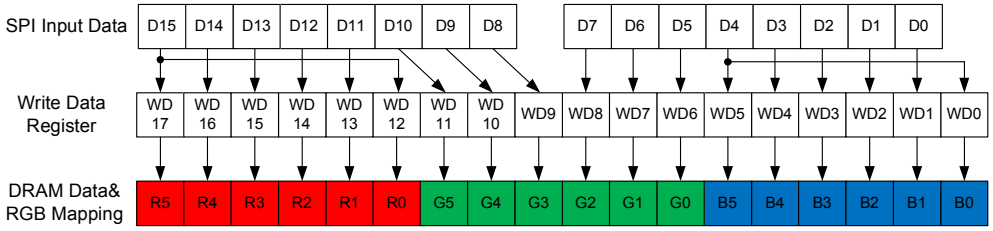


Figure 29 Data Format of SPI Interface

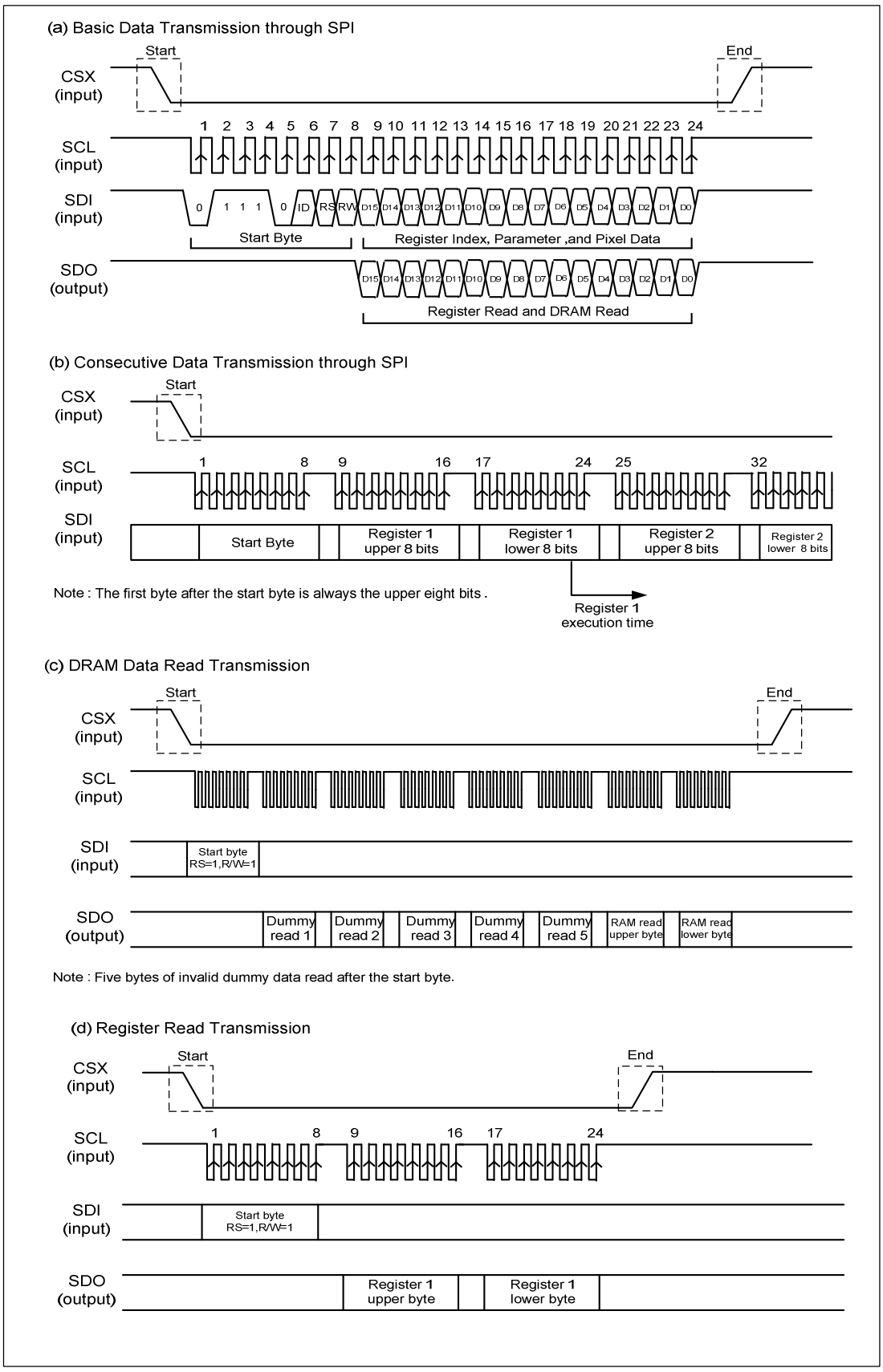
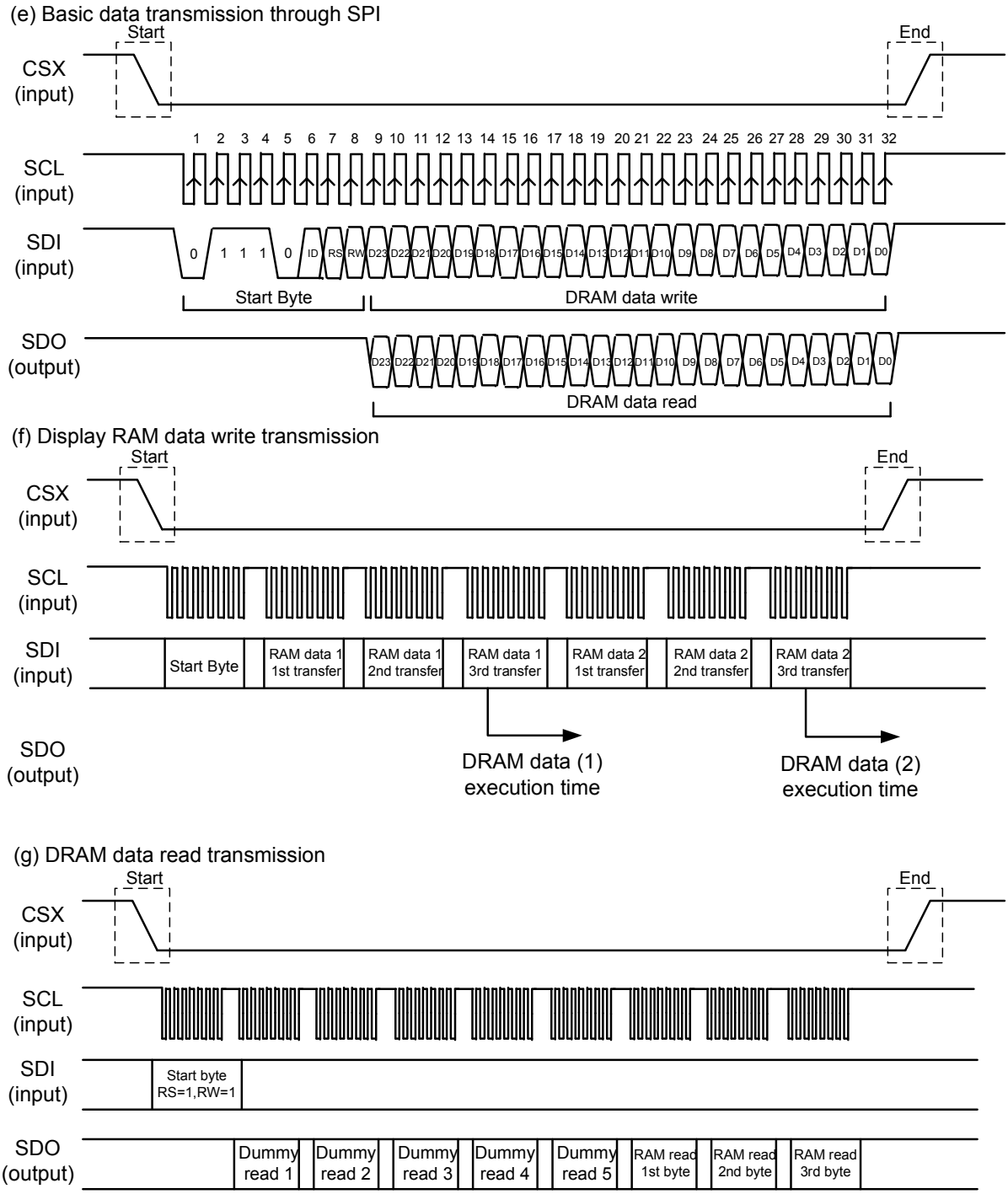


Figure 30 Data transmission through serial peripheral interface (SPI)



Note : Five bytes of invalid dummy data read after the start byte.

RAM data transfer in SPI mode when TRI = 1 and DFM = 1 or 0

Figure 31 Data transmission through serial peripheral interface (SPI, TRI="1" and DFM="1 or 0")

9.5.. VSYNC Interface

9.5.1 VSYNC Interface Operation

The ST7793 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

When DM[1:0]=”10” and RM=’0’, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables tearing-free display of motion pictures with the conventional interface.

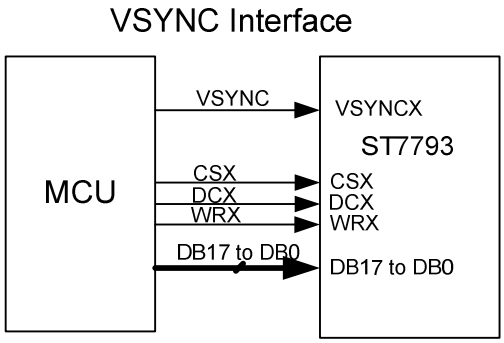


Figure 32 VSYNC Interface Connection

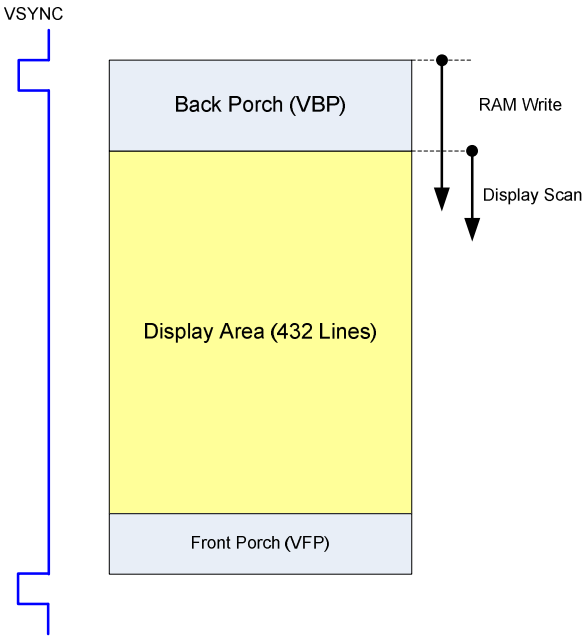


Figure 33 VSYNC Interface Operation

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

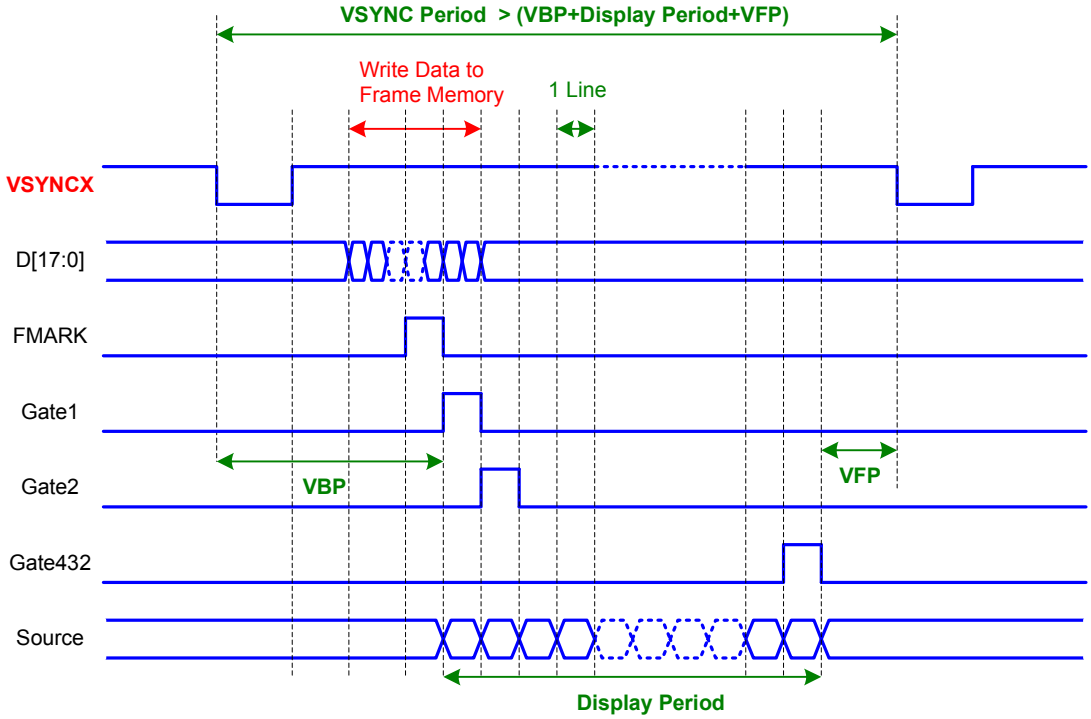


Figure 34 Timing Diagram of VSYNC Interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writes should be performed with higher speed than the result obtained from the calculation shown below. The internal RAM address counter is reset by VSYNC. So, insure interval time between VSYNC falling and DISPLAY RAM data writing.

Note:

1. VSYNC period should always be constant. If not, some degradation of display such as flicker may occur in LCD system.

2. Display data don't need to be written for every VSYNC period. For example, any system is working under 60Hz frame rate and 30-fps motion picture condition. So being written display data for every other frame would be enough.

9.5.2 VSYNC Interface Modes

9.5.2.1 Leading Mode

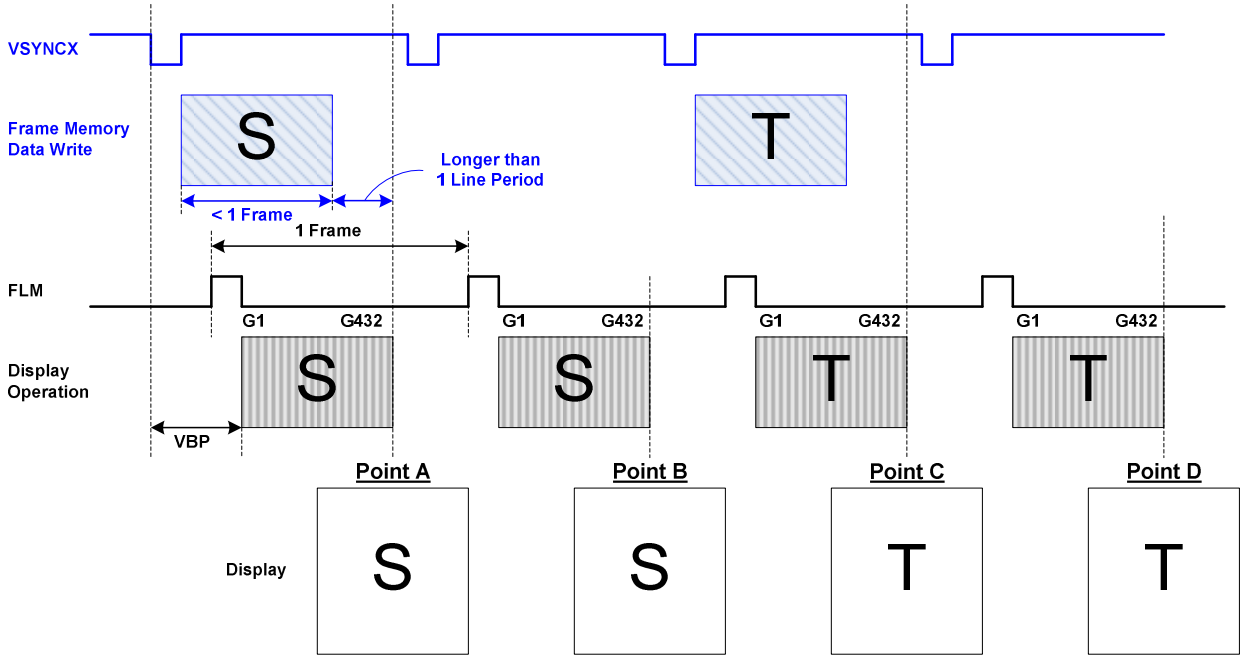


Figure 35 Operation for Leading Mode of VSYNC Interface

9.5.2.2 Lagging Mode

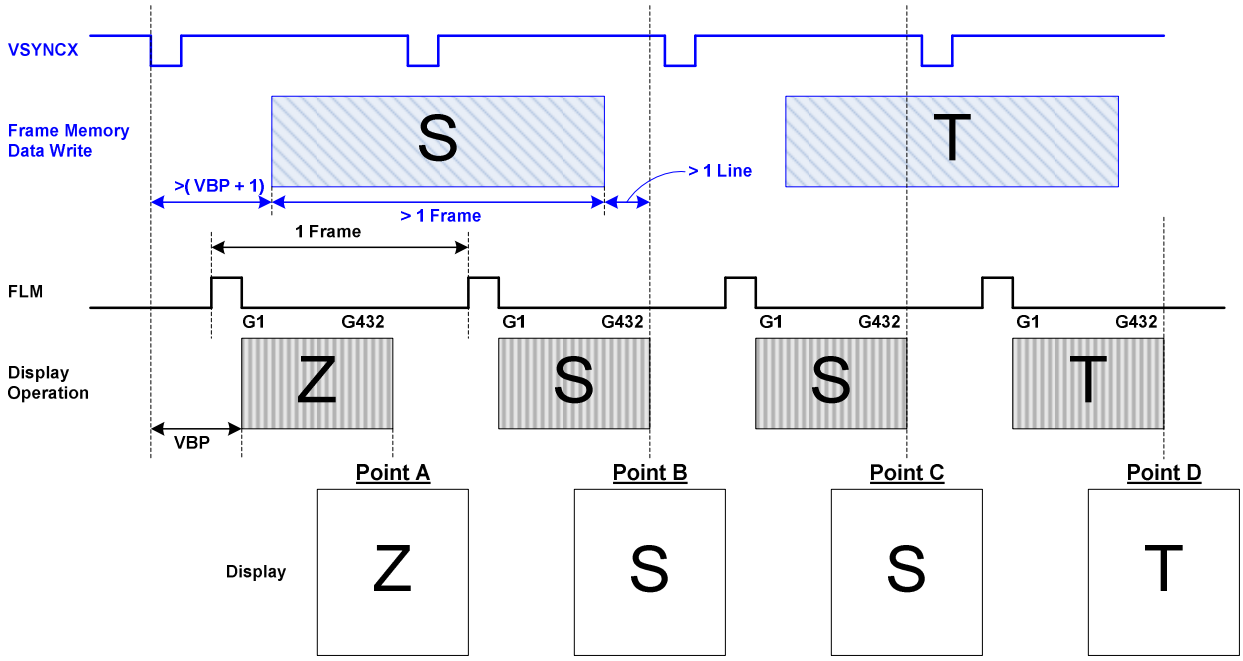


Figure 36 Operation for Lagging Mode of VSYNC Interface

Notes:

1. When RAM writing does not start immediately after the falling edge of VSYNCX, the time between the falling edge of VSYNCX and the RAM writing start timing must also be considered.

1. The minimum Display RAM write speed must be satisfied and the frequency variation must be taken into consideration.

2. The display frame rate is determined by the VSYNCX signal and the period of VSYNCX must be longer than the scan period of an entire display.

3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display and vertical scroll functions are not available in VSYNC interface mode.

5. Set the AM bit to '0' to transfer display data correctly in VSYNC interface.

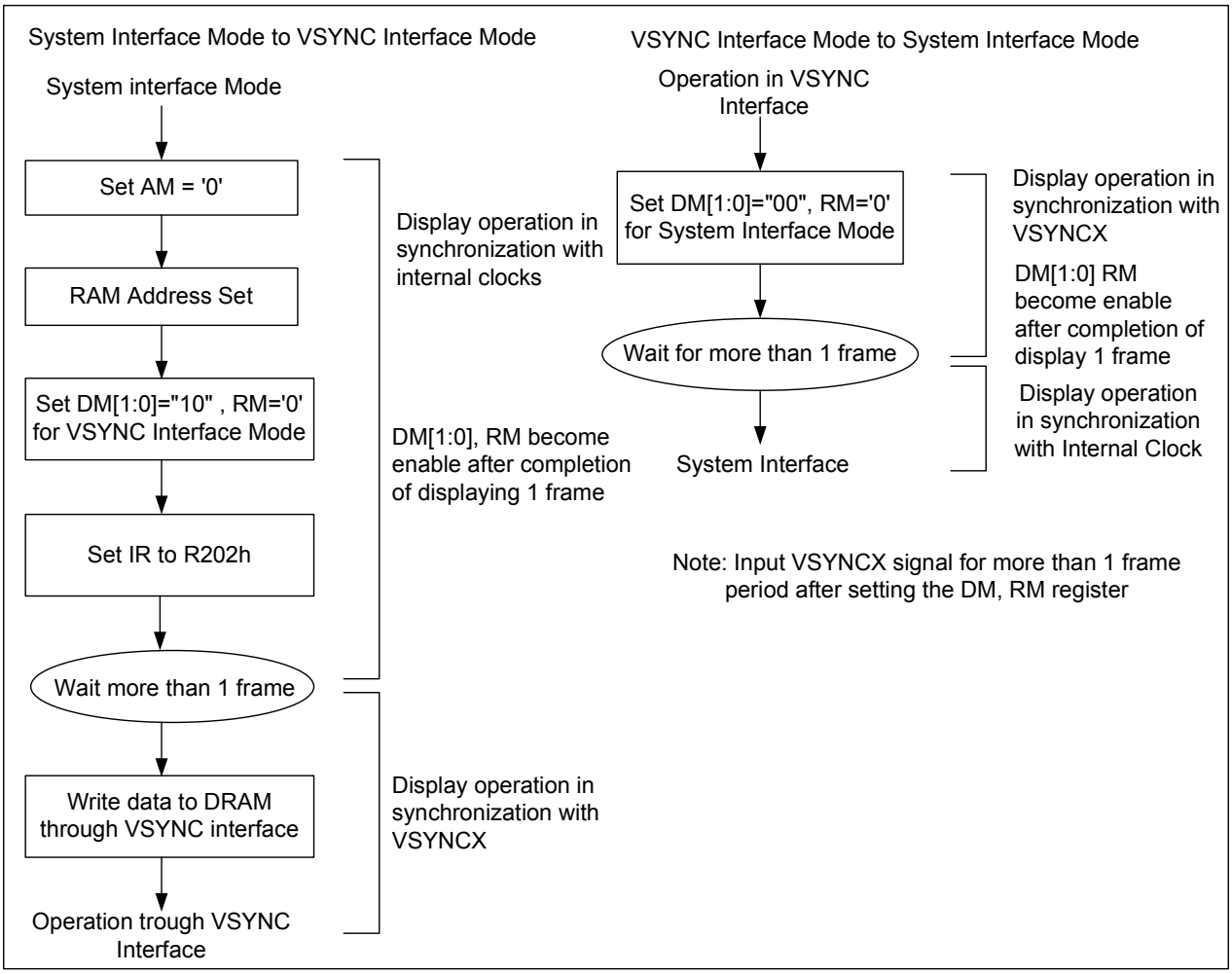


Figure 37 VSYNC and Internal Clock Operation Mode Switching Sequences

9.6.. Mobile Display Digital Interface (MDDI)

MDDI (Mobile display digital interface) is a differential small amplitude serial interface for high-speed data transfer via following 4 lines: Stb+/- (MDDI_STBP_B, MDDI_STB_M_B), Data+/- (MDDI_DATA_P_B, MDDI_DATA_M_B).

The specifications of MDDI supported by the ST7793 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the ST7793 MDDI.

9.6.1 ST7793 MDDI Specification

- MDDI Type-I
- High-speed, differential, small-amplitude data transfer via Stb+/-, Data+/- lines
- MDDI client: the ST7793 enables direct connection to the base band (BB) chip without bridge chip
- Cost-performance optimized interface for mobile display systems

1. Only internal mode (one client) and Forward Link are supported
2. Hibernation mode to save power consumption
3. Tearing-free moving picture display via FMARK/VSYNC interface
4. Moving picture display with low power consumption, realized by the features 2 ~ 3
5. Shutdown mode for saving power consumption in the standby state

ST7793 incorporates an output port for sub-display interface or peripheral control providing single-chip solution for MDDI mobile display systems.

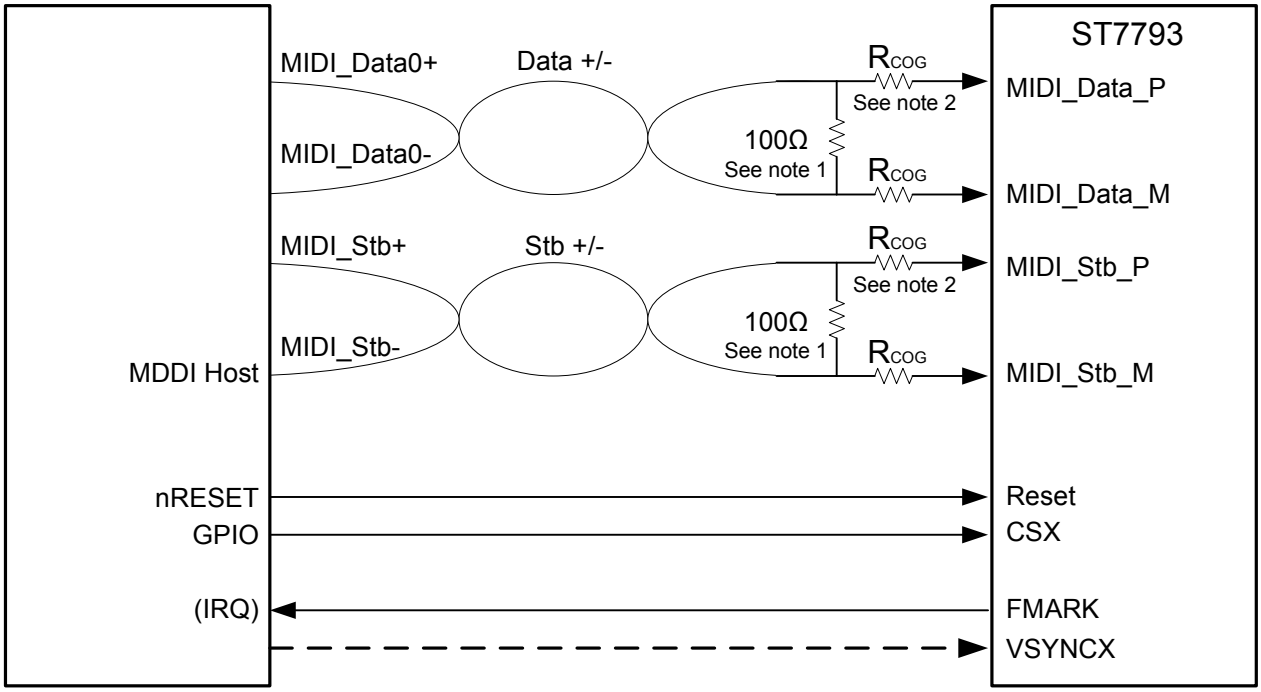


Figure 38 MDDI Interface Connection

Notes :

1. An external termination resistor of 100 ohm between Data+ and Data- lines is necessary.

2. Make the COG wiring resistances of Data+/-, Stb+/- lines as small as possible (RCOG < 10 ohm).

3. The max transmission rate is 130 Mbps!

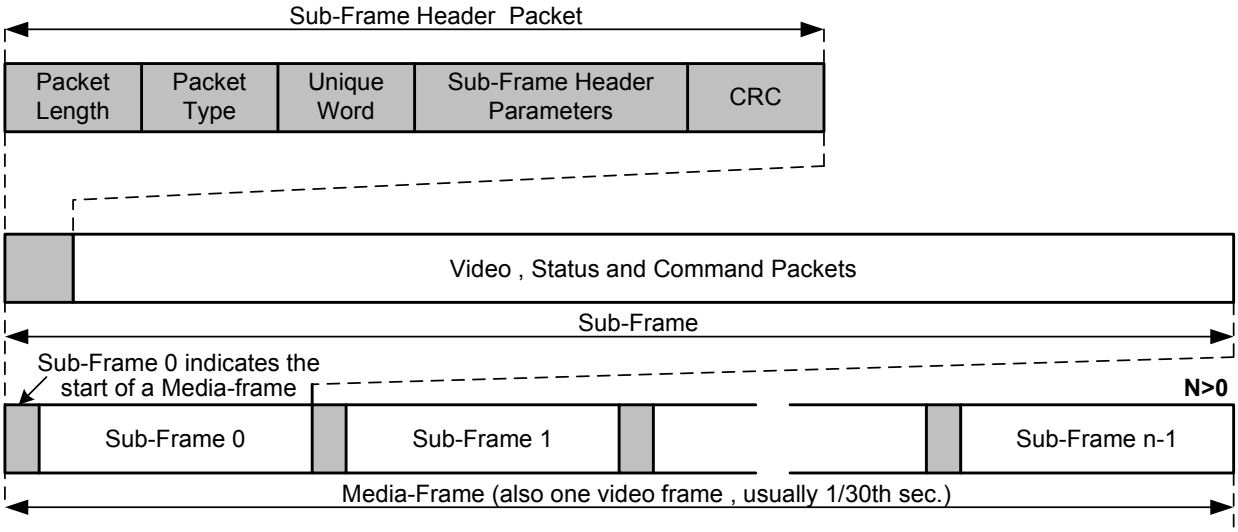
9.6.2 Supported MDDI Packets

The MDDI Link Protocol of the ST7793 is in line with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the ST7793 are as follows. Do not send packets which are not supported by ST7793.

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame and some sub-frame construct media-frame together. The following table describes 5 types of packet which is supported in ST7793.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Link shut down packet	End of frame	Forward



Packet Structure

Packet Length	Packet Type	Data Bytes	CRC

Figure 39 MDDI Frame and Packet Structure

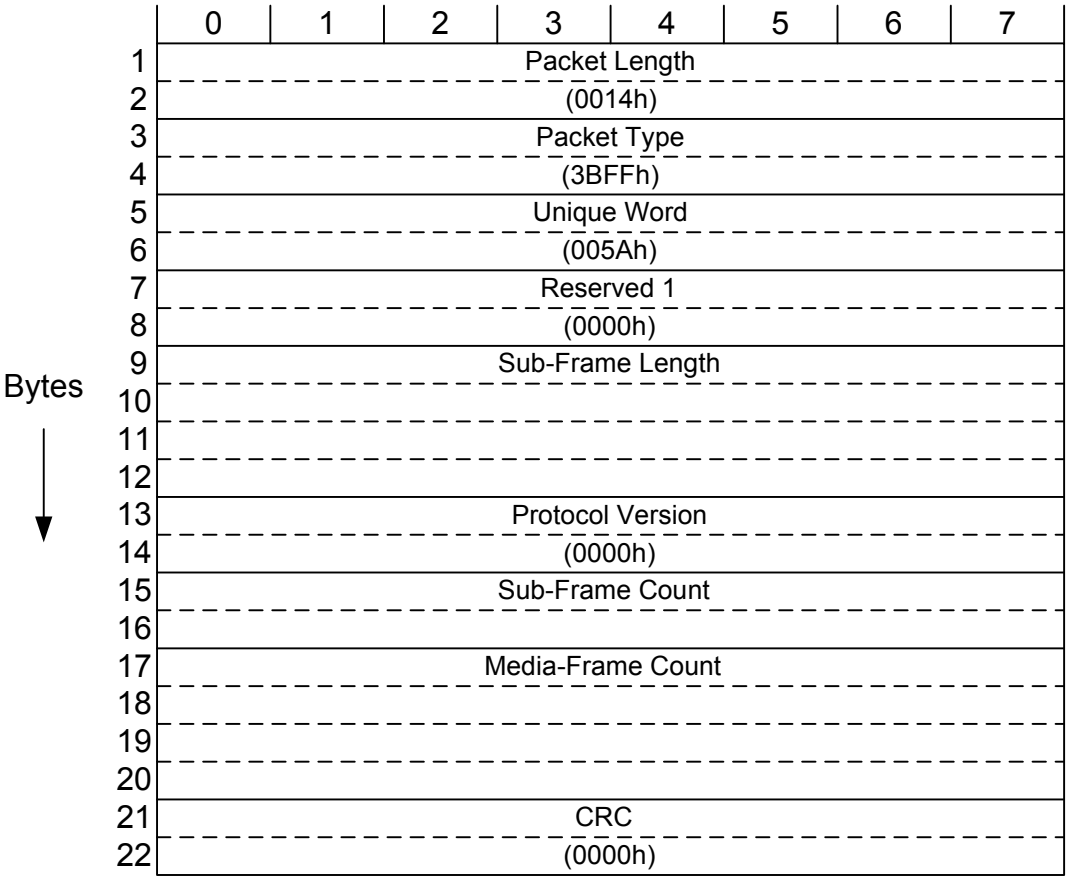
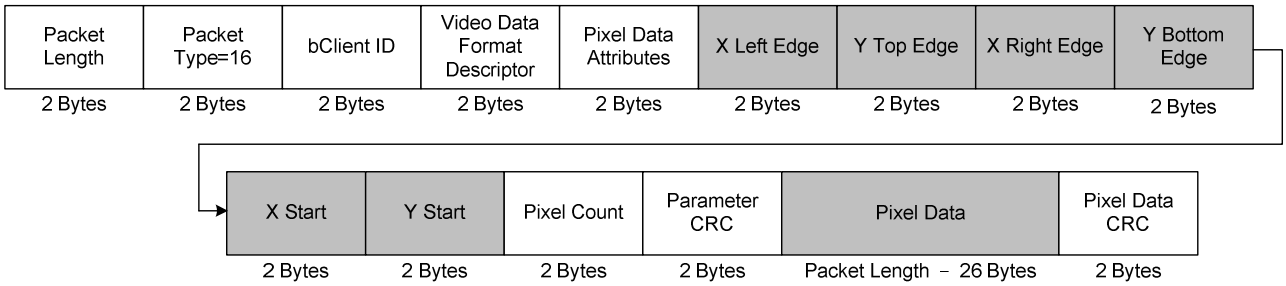
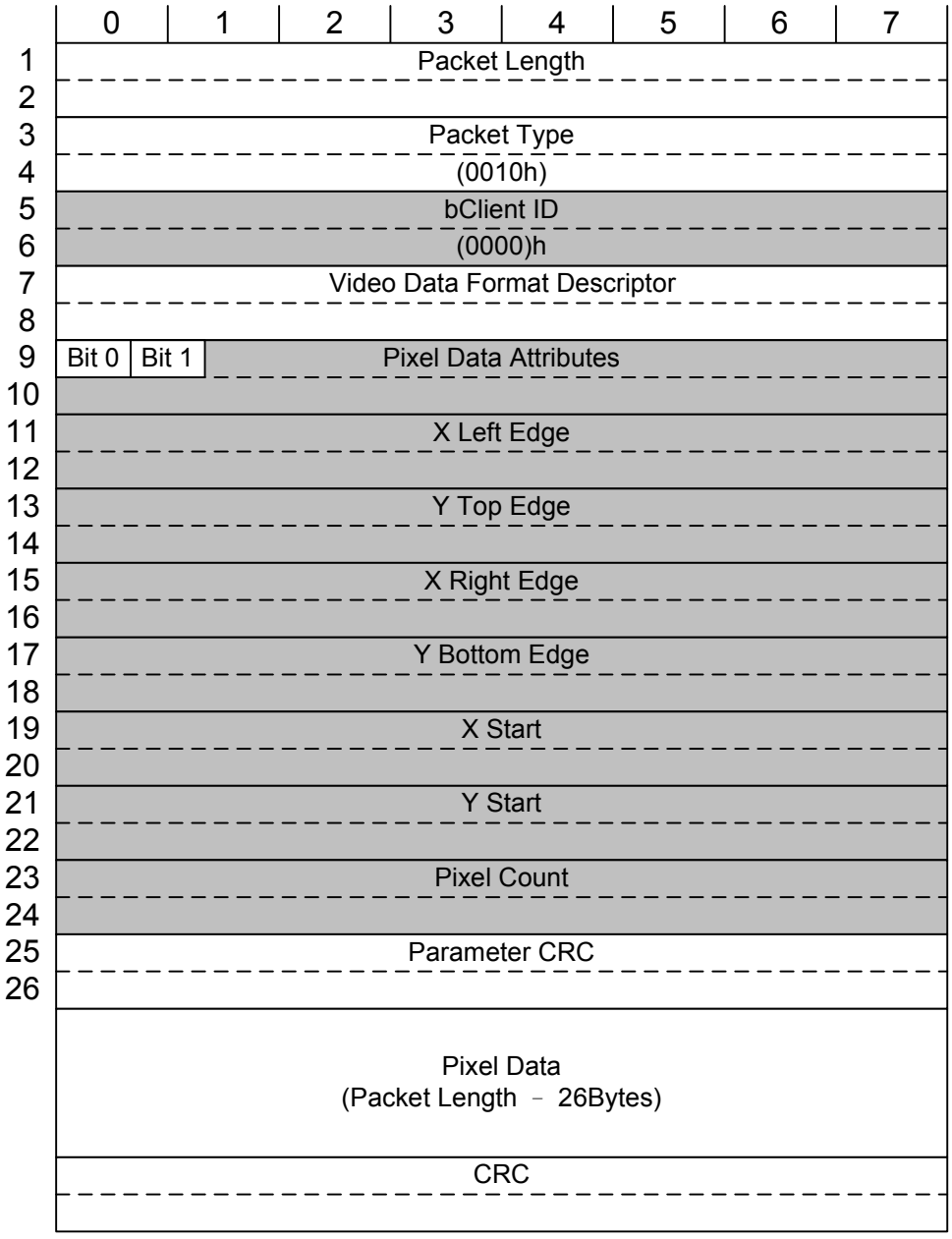


Figure 40 Sub-Frame Header Packet

9.6.2.1 Video Stream Packet

The ST7793 writes pixel data to Display RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.





Note:The parameters colored in gray are not supported by the ST7793.

Video Data Format Descriptor: Sets the pixel data format. ST7793 supports only the following format. Set the same pixel format (bpp) as selected by DSS[1:0] in Video Data Format Descriptor.

[15:13]	[12]	[11:8]	[7:4]	[3:0]	
"010"	1	5h	6h	5h	Packed 16bpp RGB Format (R:G:B = 5:6:5)
"010"	1	6h	6h	6h	Packed 18bpp RGB Format (R:G:B = 6:6:6)
Others					Setting Prohibited

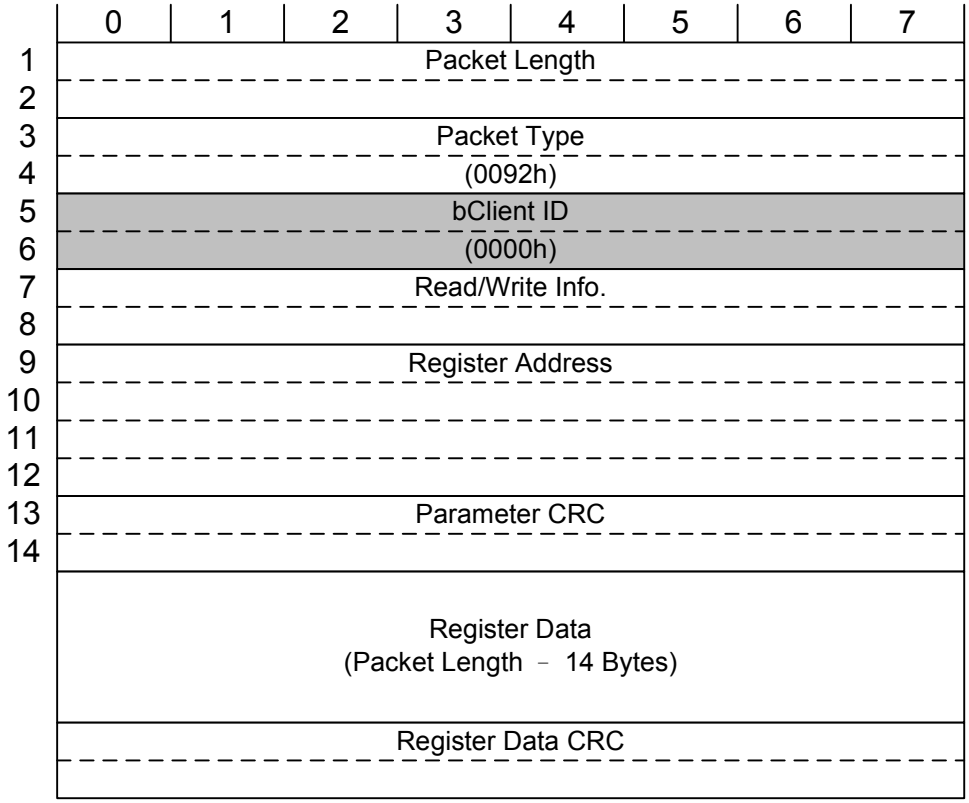
	MDDI Bytes n								MDDI Bytes (n+1)								MDDI Bytes (n+2)							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packet 16bpp	0	1	2	3	4	0	1	2	3	4	5	0	1	2	3	4	0	1	2	3	4	0	1	2
	Pixel 1 Blue					Pixel 1 Green						Pixel 1 Red					Pixel 2 Blue					Pixel 2		
Packet 18bpp	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
	Pixel 2 Blue						Pixel 2 Green						Pixel 2 Red						Pixel 2 Blue					

Pixel Data Attributes: the image data sent vial Video Stream Packet is recognized as either the data for the main-panel or for the sub-panel according to the setting in [1:0] bits in this field.

Pixel Data Attributes	Bits[1:0]	Description
0000h	00	The video stream packet data is recognized as the sub-panel data so that it is outputted via sub-display interface and not written to the ST7793.
0001h	01	Setting Prohibited
0002h	10	Setting Prohibited
0003h	11	The video stream packet data is recognized as the data written to the ST7793. The Video stream packet data is written to the ST7793 and not outputted via sub-display interface.
Others		

9.6.2.2 Register Access Packet

Register Access Packet is used when setting instruction to the ST7793.



Note : The parameters colored in gray are not supported by the ST7793.

Read/Write Info: Read or Write information in register access. ST7793 supports the following access setting.

Bits[15:14]	Bits[13:0]	Description
”00”	0001h	Write one register by register access packet
Others	-	Setting Prohibited

Register Address: The index of the register to be accessed is set in Register Address area and the Register Address Packet is directed to the ST7793 or the sub display is determined by the setting in Register Address area.

Bits[31:16]	Description
0000h	The Register Access Packet is directed to the ST7793 via main-display interface.
0001h	The Register Access Packet is directed to the sub display via sub-display interface.
0002h~7FFFh	Setting disable

Bits[15:0]	Description
0000h~FFFFh	Bits[15:0] are used as register index [15:0].

Register Data: The data for register access is written in Register Data. The length of Register Data depends on the parameter length of command.

Example of Register Access Packet (e.g. write to the ST7793)

	0	1	2	3	4	5	6	7
1	Packet Length							(12h)
2								(00h)
3	Packet Type							(92h)
4								(00h)
5	bClient ID							(00h)
6								(00h)
7	Read/Write Info.							(01h)
8								(00h)
9	Register Address							(Index ID[7:0])
10								(Index ID[15:8])
11								(00h) -> Main Display (ST7793) (01h) -> Sub Display
12								(00h)
13	Parameter CRC							
14								
15	Register Data List (Variable Length)							1st Parameter
16								2nd Parameter
17								3rd Parameter
18								(00h)
19	Parameter CRC							
20								

Note: The parameters colored in gray are not supported by the ST7793.

Register Access Packet Restrictions: ST7793's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

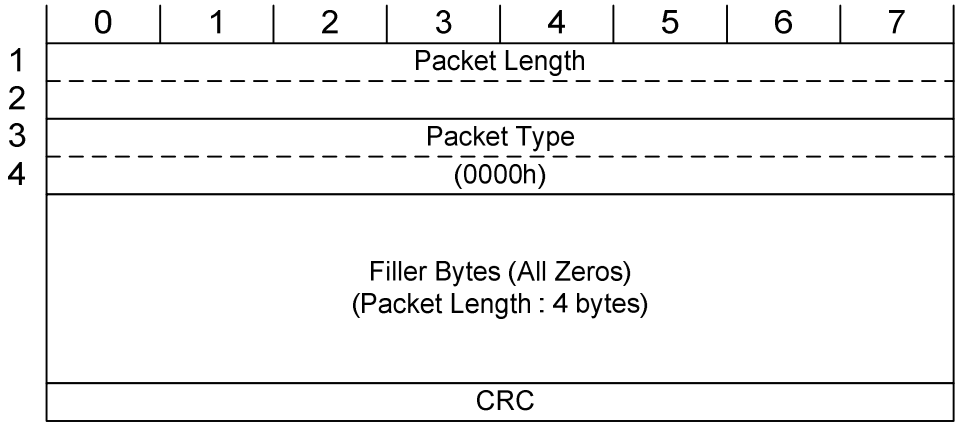
9.6.2.3 Link Shutdown Packet

This packet is used to bring Link to the Hibernation state.

	0	1	2	3	4	5	6	7
1	Packet Length							
2	(0014h)							
3	Packet Type							
4	(0045h)							
5	Parameter CRC							
6								
7	All Zeros (Type-I : 16 Bytes)							
22								

Note: The parameters colored in gray are not supported by the ST7793.

9.6.2.4 Filler Packet

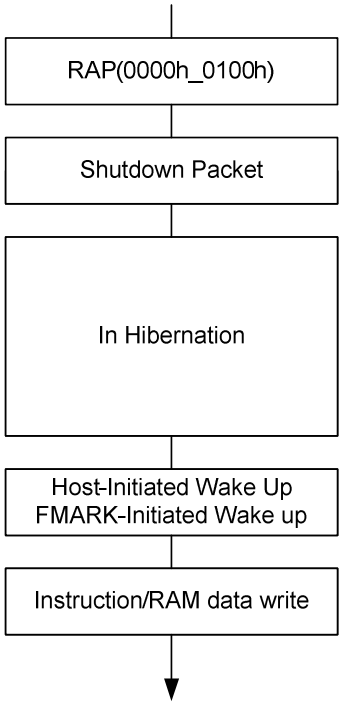


9.6.3 Hibernation Setting

The ST7793 Client MDDI supports Hibernation setting. There are two ways to cancel the Hibernation setting, which can be selected according to the condition of use.

Hibernation Cancellation	
Host-Initiated Wake Up	In Power-Saving Mode Such as Standby
TE-Initiated Wake Up	Save power consumption in transferring moving picture data host-initiated wake up triggered by the output from TE.

The Hibernation setting and cancellation sequence must be compatible with the VESA-MDDI specifications.

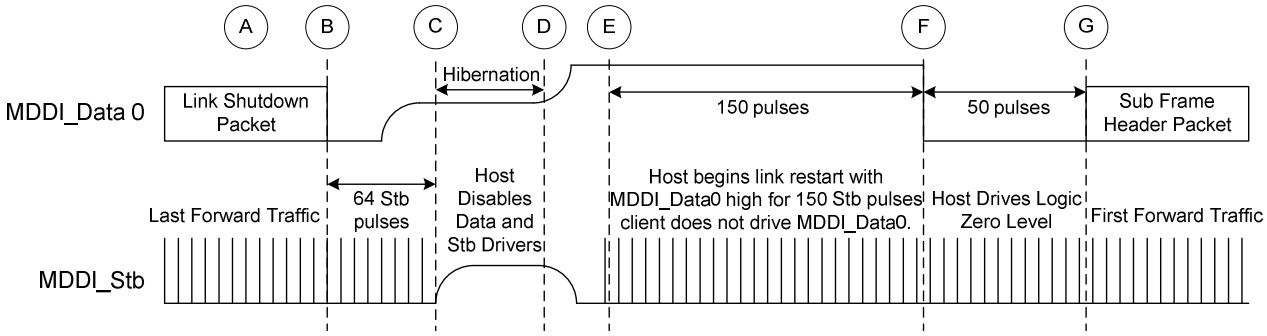


Host-Initiated Wake up from Hibernation

The host initialed wake up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the figures below!

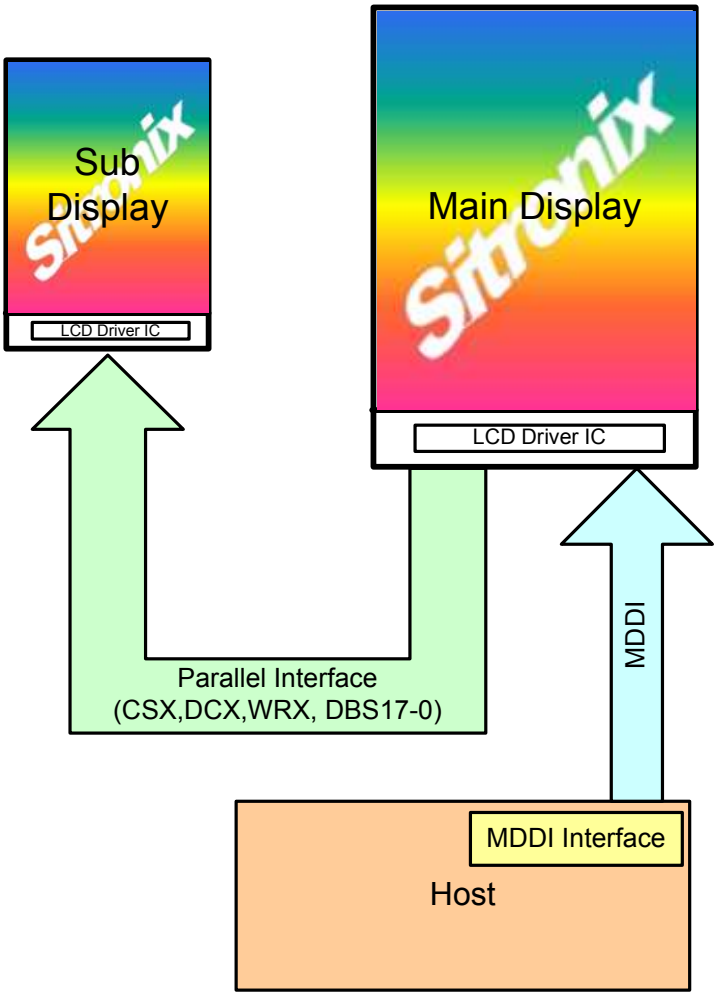
- The host sends a Link Shutdown Packet to inform the client that the link will transition to the low power hibernation state.
- Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. During the interval the host initially sets MDDI_Data0 to a logic zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.
- The host enters the low power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low power hibernation state. It is also allowable for MDDI_Stb to be driven to logic zero level or to continue toggling during hibernation. The client is also in the low power hibernation state.
- After a while, the host begins the line restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drivers MDDI_Data0 to a logic one level and MDDI_Stb to logic zero level for at least 200ns after MDDI_Data0 reaches a valid logic one level and MDDI_Stb reaches a valid logic zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high speed pulses on MDDI_Stb. The client first detects the wake up pulse using a low power differential receiver having a +125mV input offset voltage.

- The host drivers are fully enabled and MDDI_Data0 is being driven to a logic one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.
  - The host drives MDDI_Data0 to a logic zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub frame Header Packet after MDDI_Data0 is at a logic zero level for 40 MDDI_Stb cycles.
  - The host begins to transmit data on the forward link by sending a Sub-frame Header packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences form point G.



9.6.4 Sub-Display Interface

The ST7793 supports the sub-display interface which connects to sub-display driver IC with parallel interface. Depending on the packet header, ST7793 automatically receive and convert MDDI packet to parallel data and send to sub panel driver IC.

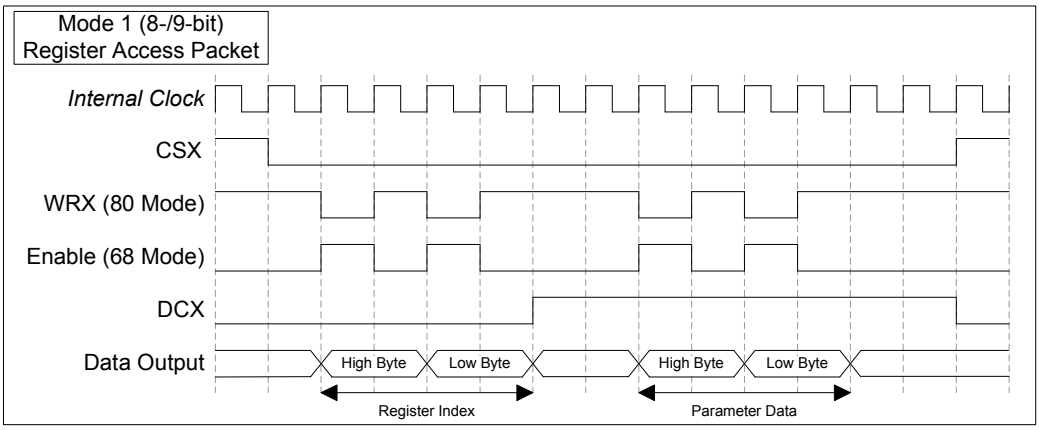


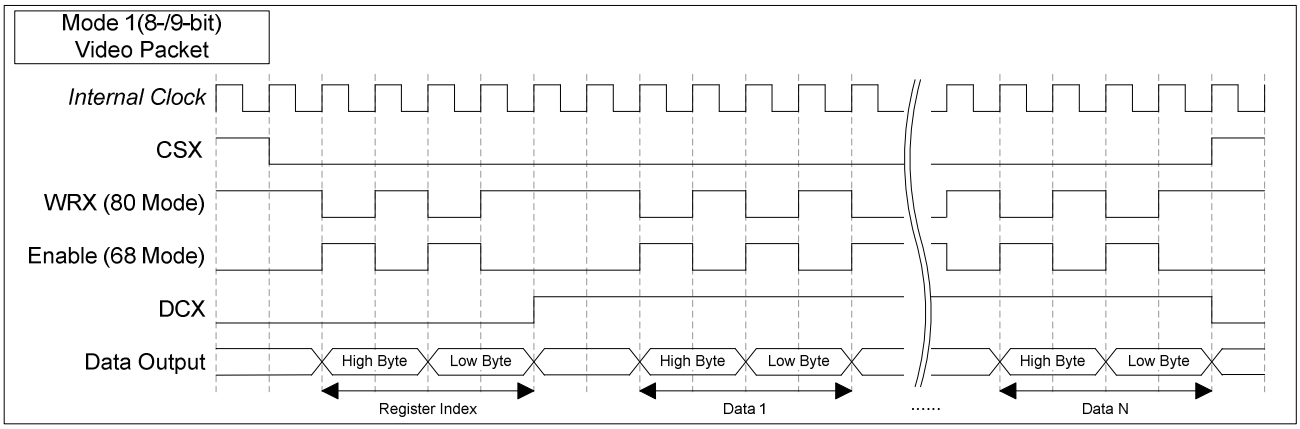
9.6.4.1 Sub-Display Interface Timing

Internal Clock for Sub-Panel Signal Generation

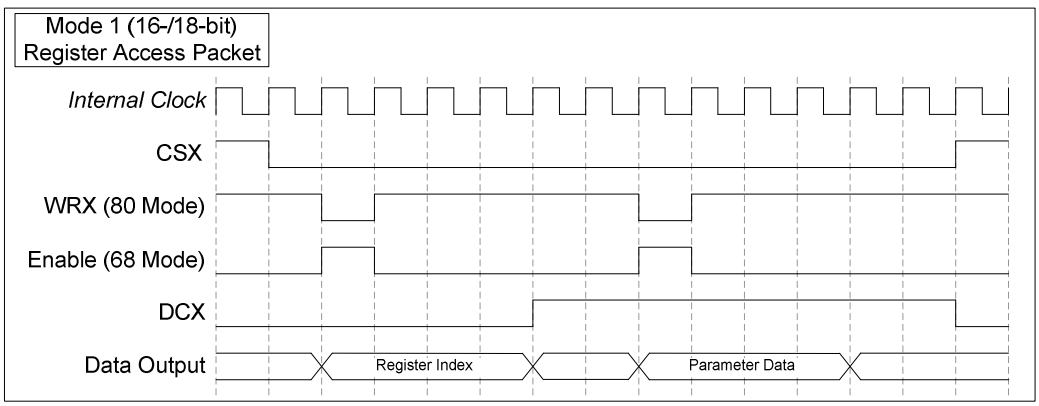
The Sub-Display interface is driven by an internal clock which is generated from MDDI interface data transmission. Once there are four bits transmitted via MDDI, one cycle of internal clock for sub-display interface is generated.

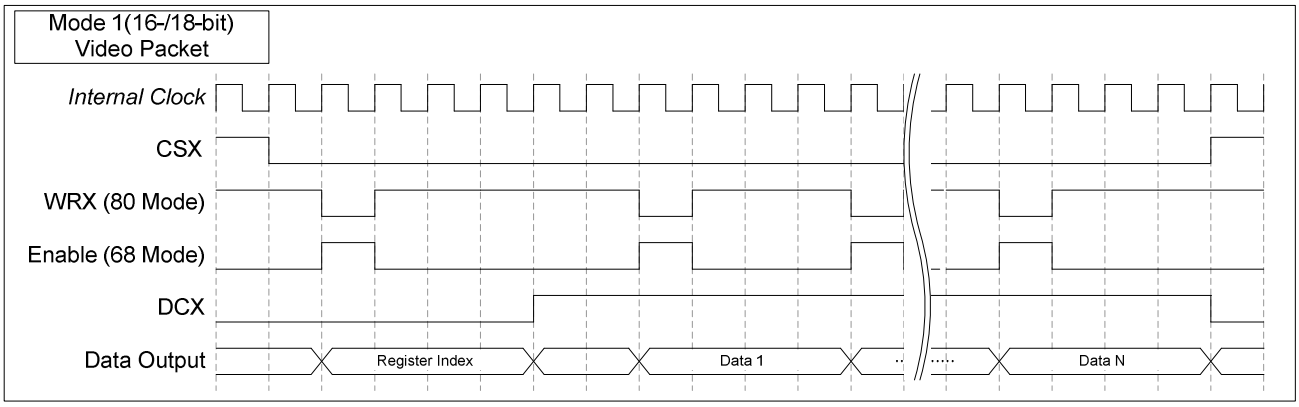
Mode 1 Sub-Display Interface Timing (8-/9-bit)



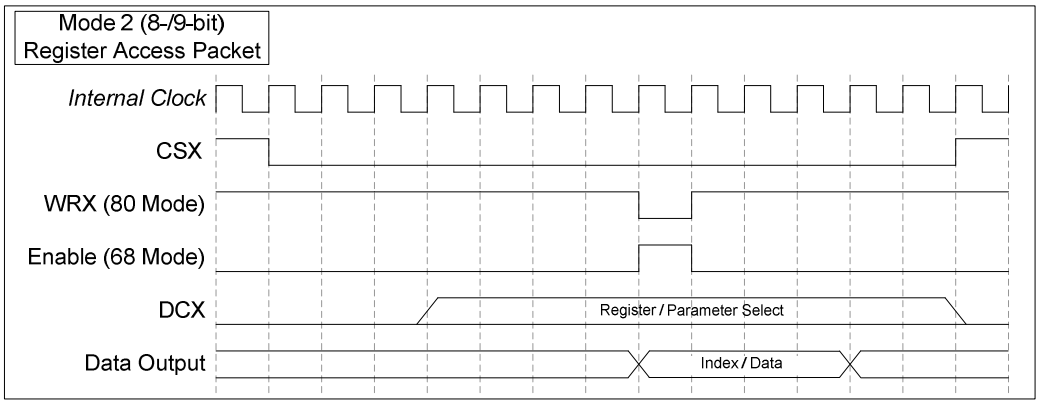


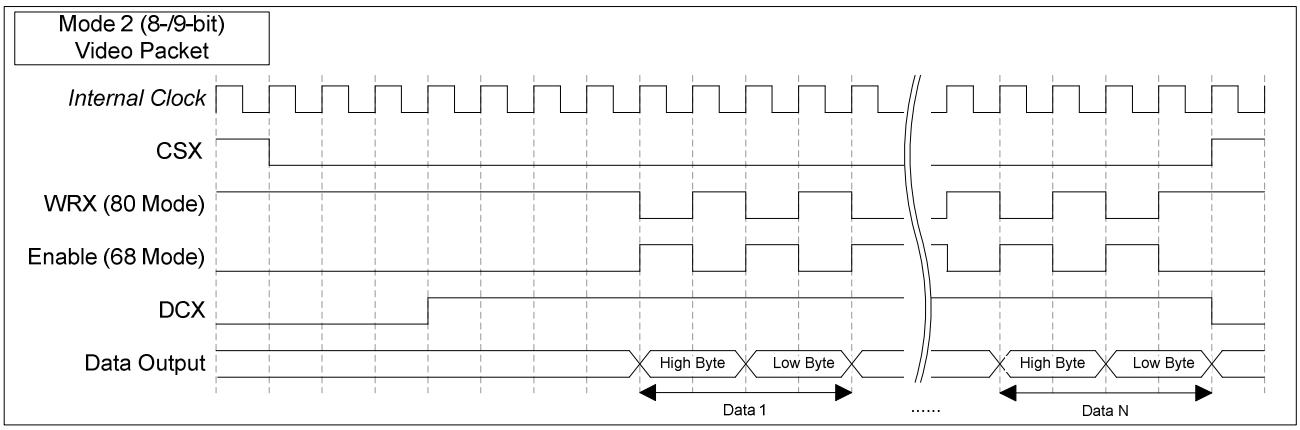
Mode 1 Sub-Display Interface Timing (16-/18-bit)



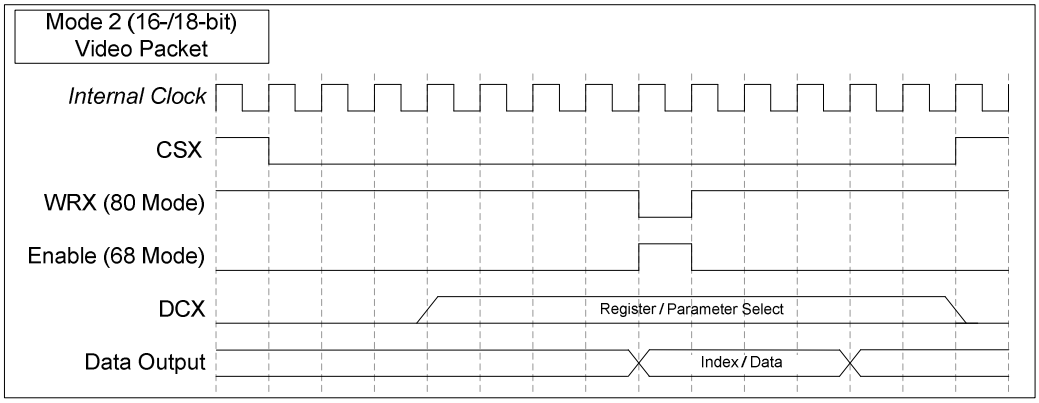


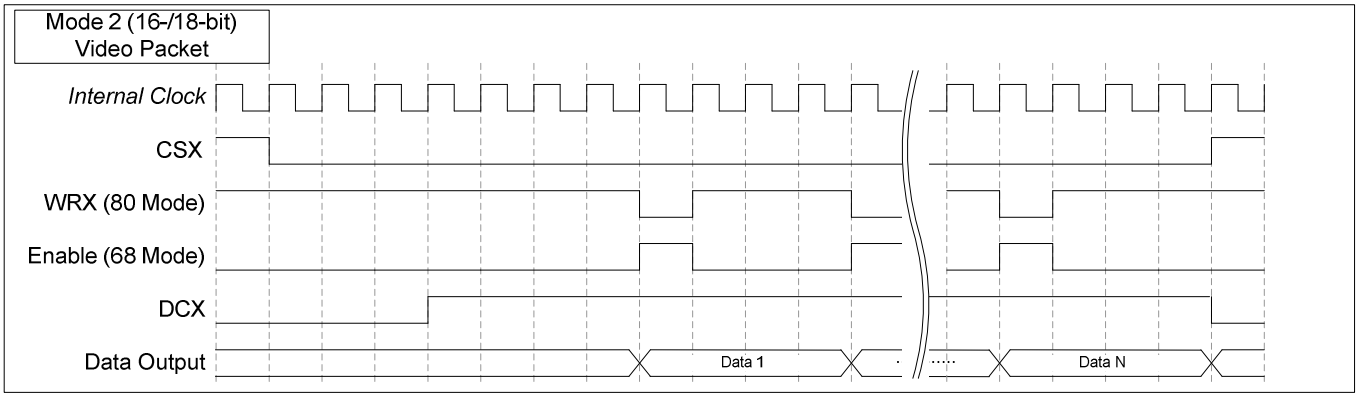
Mode 2 Sub-Display Interface Timing (8-/9-bit)





Mode 2 Sub-Display Interface Timing (16-/18-bit)





10 REGISTER

10.1.. Register List

No	Registers	W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
000h	Driver Code	R	1	0	1	1	1	0	1	1	1	1	0	0	1	0	0	1	1
001h	Driver Output Control	W/R	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
003h	Entry Mode	W/R	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D[1:0]		AM	0	0	0
007h	Display Control 1	W/R	1	0	0	0	PTDE	0	0	0	BASEE	0	0	0	0	0	0	0	0
008h	Display Control 2	W/R	1	FP[7:0]								BP[7:0]							
00Bh	8-Color Control	W/R	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	COL
00Ch	External Display Interface Control 1	W/R	1	0	ENC[2:0]		0	0	0	RM	0	0	DM[1:0]		0	0	0	RIM	
00Fh	External Display Interface Control 2	W/R	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
090h	Frame Marker Control	W/R	1	FMKM	FMI[2:0]			0	0	0	FMP[8:0]								
0FFh	Ext Register Control	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CMD2_EN
100h	Power Control 1	W/R	1	0	0	0	0	0	0	1	1	0	0	1	1	0	DSTB	0	0
102h	Power Control 3	W/R	1	0	0	0	0	0	0	0	1	1	0	PSON	PON	0	0	0	0
200h	Horizontal DRAM Address Set	W/R	1	0	0	0	0	0	0	0	0	AD[7:0]							
201h	Vertical DRAM Address Set	W/R	1	0	0	0	0	0	0	0	AD[16:8]								
202h	Write Data to DRAM	W	1	DRAM Write Data (WD[17:0]) / Read Data (RD[17:0])															
202h	Read Data from DRAM	R	1																
210h	Horizontal Address Start Position	W/R	1	0	0	0	0	0	0	0	0	HAS[7:0]							
211h	Horizontal Address End Position	W/R	1	0	0	0	0	0	0	0	0	HEA[7:0]							
212h	Vertical Address Start Position	W/R	1	0	0	0	0	0	0	0	VSA[8:0]								
213h	Vertical Address End Position	W/R	1	0	0	0	0	0	0	0	VEA[8:0]								
280h	NVM Data Read / Write	W/R	1	1	VCM[6:0]							0	0	0	UID[4:0]				
380h	Gamma Control 1	W	1	0	0	0	PR0P01[4:0]					0	0	0	PR0P00[4:0]				
381h	Gamma Control 2	W	1	PR0P04[3:0]			PR0P03[3:0]					0	0	0	PR0P02[4:0]				
382h	Gamma Control 3	W	1	0	0	0	PR0P06[4:0]					0	0	0	0	PR0P05[3:0]			
383h	Gamma Control 4	W	1	0	0	0	PR0P08[4:0]					0	0	0	PR0P07[4:0]				
384h	Gamma Control 5	W	1	0	0	PI0P3[1:0]		0	0	PI0P2[1:0]		0	0	PI0P1[1:0]		0	0	PI0P0[1:0]	
385h	Gamma Control 6	W	1	0	0	0	PR0N01[4:0]					0	0	0	PR0N00[4:0]				
386h	Gamma Control 7	W	1	PR0N04[3:0]			PR0N03[3:0]					0	0	0	PR0N02[4:0]				
387h	Gamma Control 8	W	1	0	0	0	PR0N06[4:0]					0	0	0	0	PR0N05[3:0]			

388h	Gamma Control 9	W	1	0	0	0	PR0N08[4:0]					0	0	0	PR0N07[4:0]				
389h	Gamma Control 10	W	1	0	0	PI0N3[1:0]		0	0	PI0N2[1:0]		0	0	PI0N1[1:0]		0	0	PI0N0[1:0]	
400h	Base Image Number of Line	W/R	1	GS	NL[5:0]						0	0	SCN[5:0]						0
401h	Base Image Display Control	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
404h	Base Image Vertical Scroll Control	W/R	1	0	0	0	0	0	0	0	VL[8:0]								
500h	Partial Display Position	W/R	1	0	0	0	0	0	0	0	PTDP[8:0]								
501h	Partial Display Start Line Address	W/R	1	0	0	0	0	0	0	0	PTSA[8:0]								
502h	Partial Display End Line Address	W/R	1	0	0	0	0	0	0	0	PTEA[8:0]								
600h	Test Register (S/W Reset)	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TRST
6F0h	NVM Access Control	W/R	1	0	0	0	0	0	0	0	0	0	CALB	0	0	0	0	0	0
702h	VCOM Control	W/R	1	0	0	0	0	0	0	0	0	0	VCM[6:0]						
708h	ID2	W/R	1	0	0	0	0	0	0	0	0	0	0	0	ID2[4:0]				
709h	NVM VCMWREN Setting	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VC_N
710h	Source Control 1	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH[3:0]			
712h	Source Control 2	W/R	1	0	0	0	0	0	0	0	0	0	0	0	VDV[4:]				
713h	Gate Control	W/R	1	0	0	0	0	0	0	0	0	VGHS[3:0]			VGLS[3:0]				
724h	Frame Rate Control	W/R	1	0	0	0	0	0	0	0	0	DIVI[1:0]		0	RTNI[4:0]				
752h	Source Driving Control	W/R	1	0	0	0	0	0	0	0	0	0	0	SD[1:0]		1	1	1	1
754h	Gate turn on Timing Control	W/R	1	0	0	0	0	0	0	0	0	0	0	TGO[5]	TGO[4]	TGO[3]	TGO[2]	TGO[1]	TGO[0]
7E1h	NVM Write Control	W	1	0	0	0	0	0	0	0	0	WCMD[7:0]							

Table 7 Register List

10.2.. Register Definition

10.2.1 Index (IR)

Note: "-"Don't care

Index(IR)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	↑	1	0	0	0	0	0	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Description	The index register specifies the index R000h to R7FFh of the control register or RAM control to be accessed. The access to unassigned registers and instruction bits is prohibited.																	

10.2.2 Device ID Code Read (R000h)

Device ID Code Read Out (R000h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	1	↑	0	1	1	1	0	1	1	1	1	0	0	1	0	0	1	1
Description	When read this register, the device output device ID code (7793h)																	

10.2.3 Device Output Control (R001h)

Device Output Control (R001h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description	**SS**: Select the shift direction of outputs from the source driver. When SS = 0, the shift direction of outputs is from S1 to S720 When SS = 1, the shift direction of outputs is from S720 to S1. In addition to the shift direction, the settings for both SS and BGR bits are required to change the Assignment of R, G, B dots to the source driver pins. To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0 and RGB = 0. To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1 and RGB = 1. *Note: When changing SS or BGR bits, DRAM data must be rewritten.* **SM**: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.																

10.2.4 Entry Mode (R003h)

Entry Mode (R003h)

RS	WRX	RDX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	↑	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
Default value			0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Description

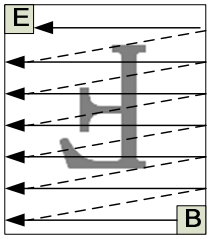
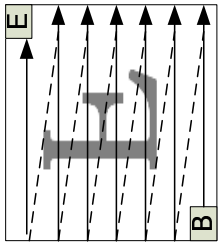
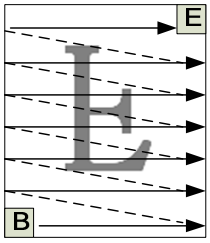
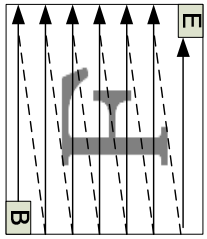
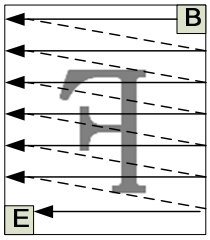
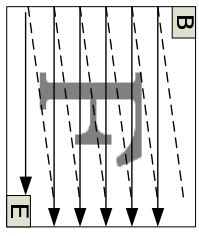
AM: Sets the Display RAM Update Direction

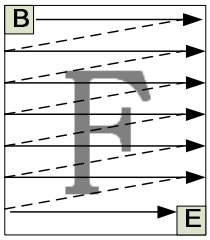
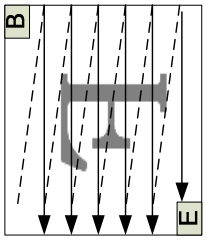
When AM = 0, set the horizontal writing direction.

When AM = 1, set the vertical writing direction.

When a window area is set, only the addressed DRAM area is updated based on I/D [1:0] and AM bits setting.

I/D [1:0]: Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data.

AM	ID[1:0]	Write DRAM Direction	AM	ID[1:0]	Write DRAM Direction
0	"00"		1	"00"	
0	"01"		1	"01"	
0	"10"		1	"10"	

0	"11"		1	"11"	

ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the DRAM address map within the window address area.
ORG = 1: The original address 00000h moves according to the I/D[1:0] setting.

Note 1: When ORG=1, only the origin address 00000h can be set in the RAM address set registers R200h, and R201h.

Note2: In RAM read operation, make sure to set ORG=0.

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the DRAM.
BGR = 0: Write data in the order of RGB to the DRAM.

BGR=0																	
D17	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

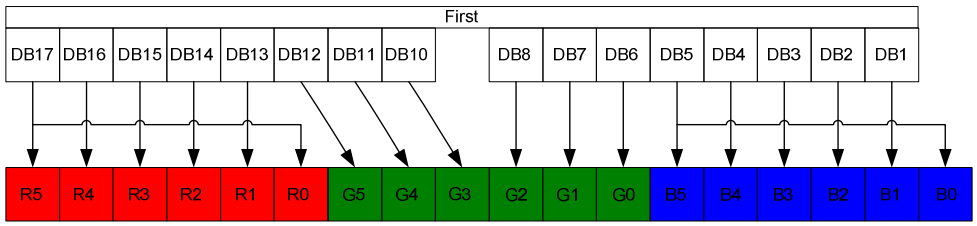
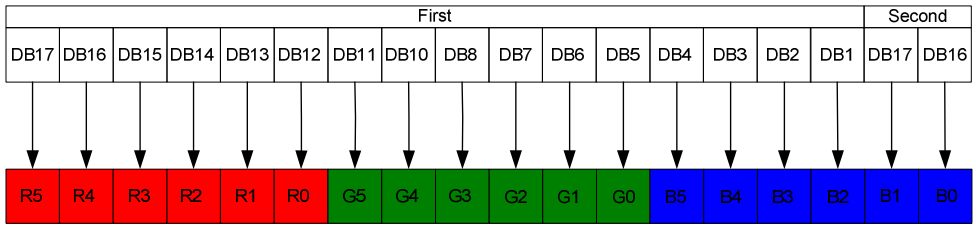
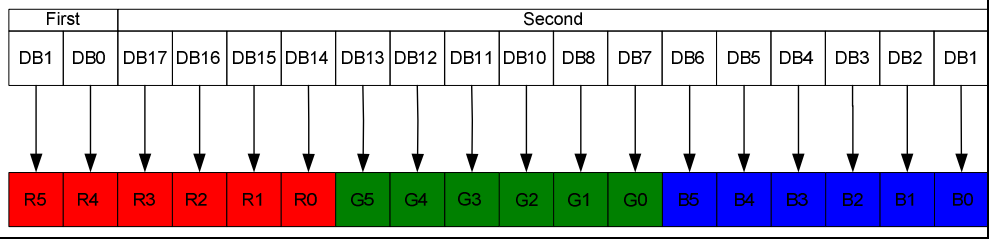
BGR = 1: Reverse the order from RGB to BGR in writing data to the DRAM.

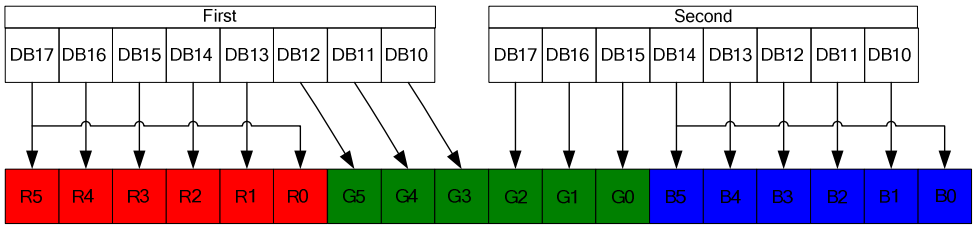
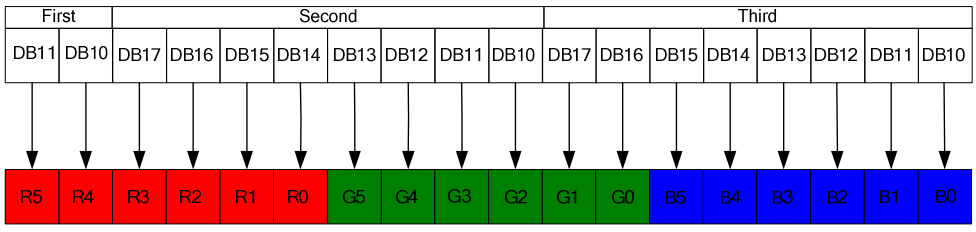
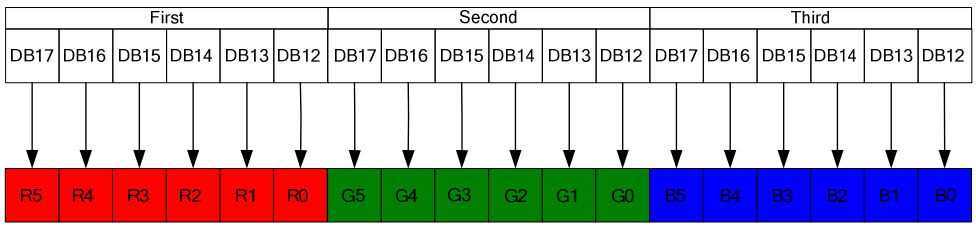
BGR=1																	
D17	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

TRI: When TRI = 1, data are transferred to the internal DRAM in 8-bit x 3 transfers mode via the 8-bit interface and in. It is also possible to send data via the 16-bit interface in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = 0.

DFM: Set the mode of transferring data to the internal RAM when TRI = 1.

TRI	**DFM**	**16-bit 8080-Series Interface Color Format**

0	*	
1	0	
1	1	

TRI	DFM	8-bit 8080-Series Interface Color Format
0	*	
1	0	
1	1	

10.2.5 Display Control 1 (R007h)

Display Control 1 (R007h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	PTDE	0	0	0	BASEE	0	0	0	0	0	0	0	0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description			**BASEE**: Base image display enable bit. BASEE = 0: No base image is displayed. The ST7793 drives liquid crystal with non-lit display level or drives only partial image display areas. BASEE = 1: A base image is displayed on the screen. **PTDE** : Partial display enable bits PTDE = 0: turns off partial image. Only base image is displayed. PTDE = 1: turns on partial image. Please set BASEE = 0 to turn off base image.															

10.2.6 Display Control 2 (R008h)

Display Control 2 (R008h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	FP[7:0]								BP[7:0]							
Default value			0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Description

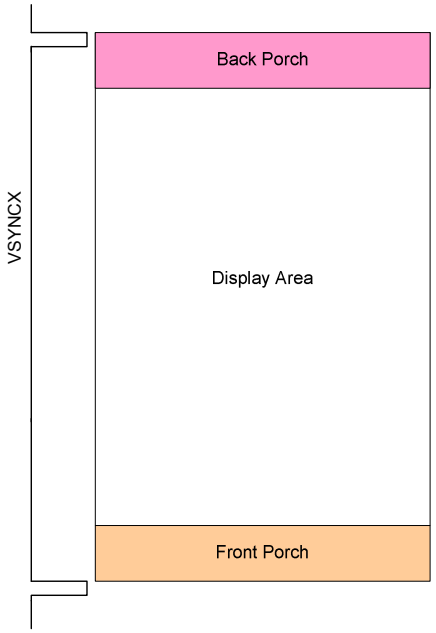
BP [7:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

FP [7:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

Note: Make sure that BP+FP must be even number of lines and BP+FP ≤ 256 lines

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNCX signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNCX input is detected.

FP[7:0] BP[7:0]	Front Porch Lines	Back Porch Lines
00h	Setting Prohibited	Setting Prohibited
01h	Setting Prohibited	Setting Prohibited
02h	Setting Prohibited	2 lines
03h	3 lines	3 lines
04h	4 lines	4 lines
05h	5 lines	5 lines
06h	6 lines	6 lines
⋮	⋮	⋮
7Fh	127 lines	127 lines
80h	128 lines	128 lines
81h	Setting Prohibited	Setting Prohibited
⋮	⋮	⋮
FFh	Setting Prohibited	Setting Prohibited



Note:The output timing to the LCD is delayed by 1 lines period from the input VSYNCX signal.

10.2.7 Eight Color Control (R00Bh)

Eight Color Control (R00Bh)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	COL
Default value			0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Description			**COL**: When COL = 1, the ST7793 enters 8-color display mode. No RAM-rewrite is required for 8-color display mode.															

10.2.8 External Display Interface Control 1 (R00Ch)

External Display Interface Control 1 (R00Ch)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	ENC[2:0]			0	0	0	RM	0	0	DM[1:0]		0	0	0	RIM
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

RIM: Select the RGB interface data format. Set RIM bit one or more frames before starting display operation via external display interface

RIM	RGB Interface Mode
0	18-bit RGB interface (1 transfer/pixel), DB[17:0], 262,144 colors
1	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1], 65,536 colors

Note1: Registers are set only by the system interface.

Note2: Be sure that previous pixel data transfer is completed before interface switch.

DM [1:0]: Select the display operation mode.

DM[1:0]	Display Interface
“00”	Internal Clock Operation
“01”	RGB interface
“10”	VSYNC interface
“11”	Setting prohibited

Note: The DM[1:0] setting allows switching between internal clock operation mode and external display interface only. i.e. switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM: Select the interface to access the RAM. When RM = 1, display data is written via RGB interface. When RM = 0, display data is written via system interface or VSYNC interface.

ENC [2:0]: Set the RAM write cycle through the RGB interface

ENC[2:0]	RAM Write Cycle(Frame periods)
000	1 Frame

001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

10.2.9 External Display Interface Control 2 (R00Fh)

External Display Interface Control (R00Fh)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description			**DPL** : Sets the signal polarity of the DOTCLK pin. DPL = 0: The data is input on the rising edge of DOTCLK DPL = 1: The data is input on the falling edge of DOTCLK **EPL** : Sets the signal polarity of the ENABLE pin. EPL = 0: The data DB17-0 is written when ENABLE = 0. Disable data write operation when ENABLE = 1. EPL = 1: The data DB17-0 is written when ENABLE = 1. Disable data write operation when ENABLE = 0. **HSPL** : Sets the signal polarity of the HSYNCX pin. HSPL= 0: Low active HSPL= 1: High active **VSPL** : Sets the signal polarity of the VSYNCX pin. VSPL= 0: Low active VSPL= 1: High active																

10.2.10 Frame Marker Control (R090h)

Frame Marker Control 4 (R090h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	FMKM	FMI[2:0]			0	0	0	FMP[8:0]								
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

FMP [8:0]: Sets the output position of FMARK signal. A pulse (FMARK) is output by starting from back porch during a 1H period when FMP[8:0] = 000h. FMP setting must meet the following constraint: 000h ≤ FMP ≤ BP + NL + FP.

FMP[8:0]	FMARK output position
000h	0
001h	1
⋮	⋮
1BEh	446
1BFh	447
Others	Setting Prohibited

FMI [2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMI[2:0]	Output Interval
“000”	1 Frame
“001”	2 Frames
“011”	4 Frames
“101”	6 Frames
Others	Setting Prohibited

FMKM: Set FMKM = 1 when FMARK signal is output from FMARK pin.

10.2.11 Ext Register Control (R0FFh)

Ext Command Control (R0FFh)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CMD2_EN
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description			**CMD2_EN** : Set to '1' to enable access to extended registers, including R380h~R389h, R702h, R708h, R710h, R712h, R713h, R724h, and R7E1h.															

10.2.12 Power Control 1 (R100h)

Power Control 1 (R100h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	1	1	0	0	1	1	0	DSTB	0	0
Default value			0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0
Description			**DSTB**: When DSTB = 1, ST7793 enters the shutdown mode and stops display. In the shutdown mode, the internal logic power supply is turned off to reduce power consumption. The RAM data and register settings are not maintained while in the shutdown mode. Set this register again after the shutdown mode is exited.															

10.2.13 Power Control 3 (R102h)

Power Control 3 (R102h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	1	1	0	PSON	PON	0	0	0	0
Default value			0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
Description			**PON, PSON**: Turn on power supply. PON and PSON must be written to start the internal power supply operation.															

10.2.14 DRAM Horizontal/Vertical Address Set (R200h, R201h)

DRAM Horizontal/Vertical Address Set (R200h,R201h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	AD[7:0]							
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	↑	1	0	0	0	0	0	0	0	AD[16:8]								
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

AD [16:0]: A DRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the ST7793 writes data to the internal DRAM so that data can be written consecutively without resetting the address in the AC.

Note 1: In RGB interface operation (RM = 1), the AD[16:0] is set to address counter every frame on the falling edge of VSYNCX

Note 2: In internal clock operation and VSYNC interface operation (RM = 0), the AD[16:0] is set to address counter when the R200h and R201h are executed.

AD[16:0]	RAM Data Map
00000h~000EFh	1st line DRAM Data
00100h~001EFh	2nd line DRAM Data
00200h~002EFh	3rd line DRAM Data
00300h~003EFh	4th line DRAM Data
⋮	⋮
1AD00h~1ADEFh	430th line DRAM Data
1AE00h~1AEEFh	431th line DRAM Data
1AF00h~1AFEFh	432h line DRAM Data

10.2.15 Write Data to DRAM (R202h)

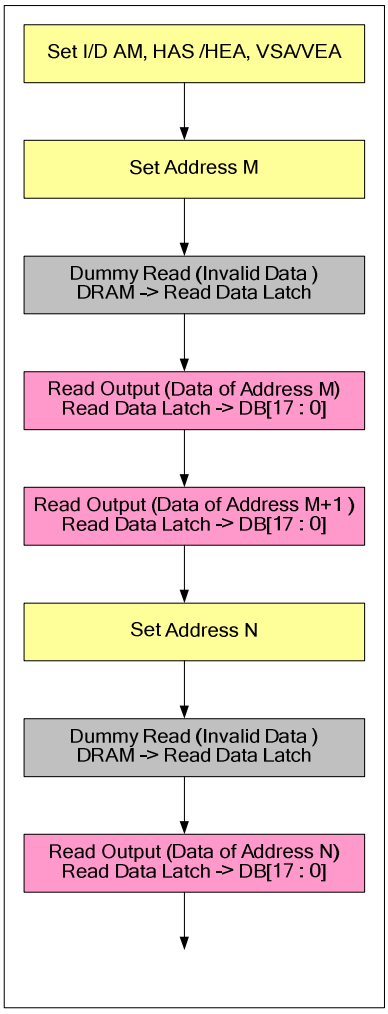
Write Data to DRAM (R202h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	WD [17:0] - DRAM Write Data															
Description			**WD [17:0]**: The ST7793 develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation. The DRAM data represents the grayscale level. The DRAM data represents the grayscale level. ST7793 automatically updates the address to the begin point according to AM and I/D[1:0] settings as it is written to this register. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.															

10.2.16 Read Data from DRAM (R202h)

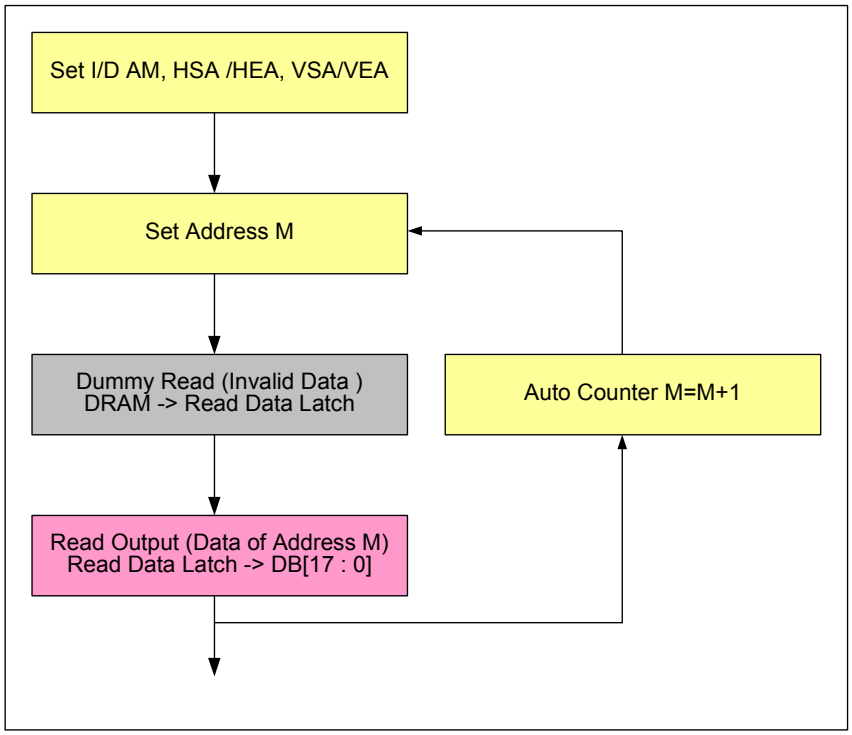
Read Data from DRAM (R202h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	1	↑	RD [17:0] – Display RAM Read Data															

Description

RD [17:0]: 18-bit data read from the Display RAM. RAM read data RD [17:0] is transferred via different data bus in different interface operation. When the ST7793 reads data from the Display RAM to the microcomputer, the first word read immediately after RAM address set is executed is taken in the internal read-data latch and invalid data is sent to the data bus. Valid data is sent to the data bus when the ST7793 reads out the second and subsequent words. When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

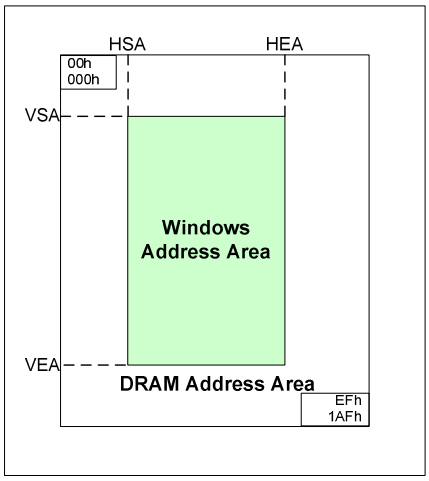


The ST7793 also supports function that automatically updates the address according to AM and I/D[1:0] settings when reading data of continuously addresses in the Display RAM



10.2.17 Horizontal and Vertical Window Address Position (R210h, R211h, R212h, R213h)

Horizontal and Vertical Window Address Position(R210h,R211h,R212h,R213h)																			
R210h	**RS**	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	1	↑	1	0	0	0	0	0	0	0	0	HSA[7:0]							
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R211h	1	↑	1	0	0	0	0	0	0	0	0	HEA[7:0]							
Default value				0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R212h	1	↑	1	0	0	0	0	0	0	0	VSA[8:0]								
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R213h	1	↑	1	0	0	0	0	0	0	0	VEA[8:0]								
Default value				0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	1

Description	**HSA [7:0], HEA [7:0], HSA [7:0],** and **HEA [7:0]** are the start and end addresses of the window address area in horizontal direction, respectively. HSA [7:0] and HEA [7:0] specify the horizontal range to write data. Set HSA [7:0] and HEA [7:0] before starting RAM write operation. In setting, make sure that 00h ≤ HSA < HEA ≤ EFh. **VSA [8:0], VEA [8:0], VSA [8:0],** and **VEA [8:0]** are the start and end addresses of the window address area in vertical direction, respectively. VSA [8:0] and VEA [8:0] specify the vertical range to write data. Set VSA [8:0] and VEA [8:0] before starting RAM write operation. In setting, make sure that 000h ≤ VSA < VEA ≤ 1AFh.  **00h ≤ HSA[7:0] ≤ HEA[7:0] ≤ EFh** **4 ≤ HEA – HSA** **000h ≤ VSA[7:0] ≤ VEA[7:0] ≤ 1AFh** *Note1. The window address range must be within the DRAM address space.* *Note2. Address must be set within the window.*

10.2.18 NVM Data Read / NVM Data Write (R280h)

NVM Data Read / NVM Data Write (R280h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	1	VCM[6:0]							0	0	0	UID[4:0]				
Default value			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Description			**VCM[6:0], UID[4:0]**: Used to temporarily store NVM data. The write data is loaded to NVM data write register (NVDAT[4:0]) and then is written to NVM. NVM data is loaded to UID[4:0] when power-on reset, when shutdown mode is exited, or when CALB = 1 is written.															

10.2.19 Gamma Control (R380h~R389h)

Gamma Control (R380h~R389h)																			
	RS	WRX	RDX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R380h	1	↑	1	0	0	0	PR0P01[4:0]					0	0	0	PR0P00[4:0]				
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R381h	1	↑	1	PR0P04[3:0]				PR0P03[3:0]				0	0	0	PR0P02[4:0]				
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R382h	1	↑	1	0	0	0	PR0P06[4:0]					0	0	0	0	PR0P05[3:0]			
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R383h	1	↑	1	0	0	0	PR0P08[4:0]					0	0	0	PR0P07[4:0]				
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R384h	1	↑	1	0	0	PI0P3[1:0]		0	0	PI0P2[1:0]		0	0	PI0P1[1:0]		0	0	PI0P0[1:0]	
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R385h	1	↑	1	0	0	0	PR0N01[4:0]					0	0	0	PR0N00[4:0]				
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R386h	1	↑	1	PR0N04[3:0]				PR0N03[3:0]				0	0	0	PR0N02[4:0]				
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R387h	1	↑	1	0	0	0	PR0N06[4:0]					0	0	0	0	PR0N05[3:0]			
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R388h	1	↑	1	0	0	0	PR0N08[4:0]					0	0	0	PR0N07[4:0]				
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R389h	1	↑	1	0	0	PI0N03[1:0]		0	0	PI0N02[1:0]		0	0	PI0N01[1:0]		0	0	PI0N00[1:0]	
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

PR0P00[4:0]: Adjusts reference level for positive polarity output R0

PR0N00[4:0]: Adjusts reference level for negative polarity output R0

PR0P01[4:0]: Adjusts reference level for positive polarity output R1

PR0N01[4:0]: Adjusts reference level for negative polarity output R1

PR0P02[4:0]: Adjusts reference level for positive polarity output R2

PR0N02[4:0]: Adjusts reference level for negative polarity output R2

PR0P03[3:0]: Adjusts reference level for positive polarity output R3

PR0N03[3:0]: Adjusts reference level for negative polarity output R3

PR0P04[3:0]: Adjusts reference level for positive polarity output R4

	PR0N04[3:0]: Adjusts reference level for negative polarity output R4 **PR0P05[3:0]:** Adjusts reference level for positive polarity output R5 **PR0N05[3:0]:** Adjusts reference level for negative polarity output R5 **PR0P06[4:0]:** Adjusts reference level for positive polarity output R6 **PR0N06[4:0]:** Adjusts reference level for negative polarity output R6 **PR0P07[4:0]:** Adjusts reference level for positive polarity output R7 **PR0N07[4:0]:** Adjusts reference level for negative polarity output R7 **PR0P08[4:0]:** Adjusts reference level for positive polarity output R8 **PR0N08[4:0]:** Adjusts reference level for negative polarity output R8 **PI0P0~1[1:0]:** Adjusts interpolation level for positive polarity output (V2~V7) **PI0N0~1[1:0]:** Adjusts interpolation level for negative polarity output (V2~V7) **PI0P2~3[1:0]:** Adjusts interpolation level for positive polarity output (V56~V61) **PI0N2~3[1:0]:** Adjusts interpolation level for negative polarity output (V56~V61) *Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.*

10.2.20 Base Image Display Control (R400h, R401h, R404h)

Base Image Display Control (R400h,R401h, R404h)																		
R400h	**RS**	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	1	↑	1	GS	NL[5:0]						0	0	SCN[5:0]						0
Default value				0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
R401h	1	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R404h	1	↑	1	0	0	0	0	0	0	0	VL[8:0]								
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

SCN [5:0]: Specifies the gate line where the gate driver starts scan.

SCN[5:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G(N)	G1	G(2N-432)
01h	G9	G(N+8)	G17	G(2N-416)
02h	G17	G(N+16)	G33	G(2N-400)
03h	G25	G(N+24)	G49	G(2N-384)
04h	G33	G(N+32)	G65	G(2N-368)
05h	G41	G(N+40)	G81	G(2N-352)
06h	G49	G(N+48)	G97	G(2N-336)
07h	G57	G(N+56)	G113	G(2N-320)
08h	G65	G(N+64)	G129	G(2N-304)
09h	G73	G(N+72)	G145	G(2N-288)
0Ah	G81	G(N+80)	G161	G(2N-272)
0Bh	G89	G(N+88)	G177	G(2N-256)
0Ch	G97	G(N+96)	G193	G(2N-240)
0Dh	G105	G(N+104)	G209	G(2N-224)
0Eh	G113	G(N+112)	G225	G(2N-208)
0Fh	G121	G(N+120)	G241	G(2N-192)
10h	G129	G(N+128)	G257	G(2N-176)
11h	G137	G(N+136)	G273	G(2N-160)
12h	G145	G(N+144)	G289	G(2N-144)
13h	G153	G(N+152)	G305	G(2N-128)
14h	G161	G(N+160)	G321	G(2N-112)
15h	G169	G(N+168)	G337	G(2N-96)

16h	G177	G(N+176)	G353	G(2N-80)
17h	G185	G(N+184)	G369	G(2N-64)
18h	G193	G(N+192)	G385	G(2N-48)
19h	G201	G(N+200)	G401	G(2N-32)
1Ah	G209	G(N+208)	G417	G(2N-16)
1Bh	G217	G(N+216)	G2	G(2N-431)
1Ch	G225	G(N+224)	G18	G(2N-415)
1Dh	G233	G(N+232)	G34	G(2N-399)
1Eh	G241	G(N+240)	G50	G(2N-383)
1Fh	G249	G(N+248)	G66	G(2N-367)
20h	G257	G(N+256)	G82	G(2N-351)
21h	G265	G(N+264)	G98	G(2N-335)
22h	G273	G(N+272)	G114	G(2N-319)
23h	G281	G(N+280)	G130	G(2N-303)
24h	G289	G(N+288)	G146	G(2N-287)
25h	G297	G(N+296)	G162	G(2N-271)
26h	G305	G(N+304)	G178	G(2N-255)
27h	G313	G(N+312)	G194	G(2N-239)
28h	G321	G(N+320)	G210	G(2N-223)
29h	G329	G(N+328)	G226	G(2N-207)
2Ah	G337	G(N+336)	G242	G(2N-191)
2Bh	G345	G(N+344)	G258	G(2N-175)
2Ch	G353	G(N+352)	G274	G(2N-159)
2Dh	G361	G(N+360)	G290	G(2N-143)
2Eh	G369	G(N+368)	G306	G(2N-127)
2Fh	G377	G(N+376)	G322	G(2N-111)
30h	G385	G(N+384)	G338	G(2N-95)
31h	G393	G(N+392)	G354	G(2N-79)
32h	G401	G(N+400)	G370	G(2N-63)
33h	G409	G(N+408)	G386	G(2N-47)
34h	G417	G(N+416)	G402	G(2N-31)
35h ~ 3Fh	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited

Note: "N" is the number of line decided by NL[5:].Make sure that "Gate scan start position + NL " does not exceed 432 lines.

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The DRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the

same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line	NL[5:0]	LCD Drive Line
00h	Setting inhibited	1Dh	240 lines
01h	16 lines	1Eh	248 lines
02h	24 lines	1Fh	256 lines
03h	32 lines	20h	264 lines
04h	40 lines	21h	272 lines
05h	48 lines	22h	280 lines
06h	56 lines	23h	288 lines
07h	64 lines	24h	296 lines
08h	72 lines	25h	304 lines
09h	80 lines	26h	312 lines
0Ah	88 lines	27h	320 lines
0Bh	96 lines	28h	328 lines
0Ch	104 lines	29h	336 lines
0Dh	112 lines	2Ah	344 lines
0Eh	120 lines	2Bh	352 lines
0Fh	128 lines	2Ch	360 lines
10h	136 lines	2Dh	368 lines
11h	144 lines	2Eh	376 lines
12h	152 lines	2Fh	384 lines
13h	160 lines	30h	392 lines
14h	168 lines	31h	400 lines
15h	176 lines	32h	408 lines
16h	184 lines	33h	416 lines
17h	192 lines	34h	424 lines
18h	200 lines	35h	432 lines
19h	208 lines	Others	Setting inhibited
1Ah	216 lines		
1Bh	224 lines		
1Ch	232 lines		

GS: Sets the direction of scan of the gate driver. Set GS bit in combination with SM bit for the convenience of the display module configuration and the display direction.

When GS=0, the scan direction is from G1 to G432

When GS=1, the scan direction is from G432 to G1

NDL: Sets the source output level in non display area in partial mode.

NDL	Non- Display Area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the ST7793 to display the same image from the same set of data whether the liquid crystal panel is normally black or white.

REV	DRAM Data	Display Area	
		Positive Polarity	Negative Polarity
0	00000h	V63	V0
	.	.	.
	.	.	.
	.	.	.
	3FFFFh	V0	V63
1	00000h	V0	V63
	.	.	.
	.	.	.
	.	.	.
	3FFFFh	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the ST7793 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = 0”

VLE	Base Image Display
0	Fixed
1	Enable Scrolling

VL[8:0]: Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0] $\leq$432.

10.2.21 Partial Display Control (R500h, R501h, R502h)

Partial Display Control (R500h,R501h, R502h)																			
R500h	**RS**	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	1	↑	1	0	0	0	0	0	0	0	PTDP[8:0]								
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R501h	1	↑	1	0	0	0	0	0	0	0	PTSA[8:0]								
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R502h	1	↑	1	0	0	0	0	0	0	0	PTEA[8:0]								
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description				**PTDP [8:0]**: Sets the display position of partial image. **PTSA [8:0] and PTEA [8:0]**: Sets the start line and end line addresses of the RAM area, respectively for the partial image. In setting, make sure that PTSA ≤ PTEA.															

10.2.22 Test Register (R600h)

Test Register (R600h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TRST
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description			**TRST**: When TRST=1, settings for R380h~R389h, R710h, R712h, R713h, and R724h are reset to default values. When finished, please set TRST to 0.																

10.2.23 NVM Access Control (R6F0h)

NVM Access Control (R6F0h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	CALB	0	0	0	0	0	0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description	**CALB**: When CALB=1, all data in NVM is read out and written to internal registers. When finished, CALB is set to 0.																	

10.2.24 VCOM Control (R702h)

VCOM Control (R702h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	VCMS[6:0]						
Default value			0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Description

VCMS[6:0]: Set the relative VCOM offset.

VCMWREN: Selection the VCM setting. When the NV memory is programmed, the VCMWREN will be set as '1'automatically.

VCMWREN =1 Register 702h for VCM setting

VCMWREN =0 NV Memory selected for VCM setting

VCMS[6:0]	Offset
00h~21h	420 mV
22h	440 mV
23h	460 mV
…	…
41h	1060 mV
…	…
5Eh	1640 mV
5Fh	1660 mV
60h~7Fh	1680 mV

Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.

VCMWREN is set by R709h.

10.2.25 ID2 (R708h)

ID2 (R708h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	1	1	1	ID2[4:0]				
Default value			0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Description			**ID2[4:0]**: 5-bit NVM for ID usage. *Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.*															

10.2.26 NVM VCMWREN Setting (R709h)

VCMWREN Setting (R709h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VCMWREN
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Description			**VCMWREN:** Selection the VCM setting. When the NV memory is programmed, the VCMWREN will be set as '1'automatically. VCMWREN =1 Register 702h for VCM setting VCMWREN =0 NV Memory selected for VCM setting *Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.*															

10.2.27 Source Control 1 (R710h)

Source Control 1 (R710h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	VRH[4:0]				
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

VRH[3:0] : Sets amplitude of VAP to VBP and VAN to VBN.

VRH[4:0]	Amplitude	VRH[4:0]	Amplitude
00h~0Fh	Setting Prohibited	18h	4.489 V
10h	4.034 V	19h	4.553 V
11h	4.086 V	1Ah	4.619 V
12h	4.139 V	1Bh	4.687 V
13h	4.194 V	1Ch	4.757 V
14h	4.250 V	1Dh	4.829 V
15h	4.307 V	1Eh	4.903 V
16h	4.366 V	1Fh	4.980 V
17h	4.427 V	-	-

Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.

10.2.28 Source Control 2 (R712h)

Source Control 2 (R712h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	VDV[4:0]				
Default value			0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Description

VDV[4:0] : Sets the voltage difference between VBP and VBN.

VDV [4:0]	VBP - VBN
00~0Eh	Setting Prohibited
0Fh	0 mV
10h	40mV
11h	80mV
12h	120mV
13h	160mV
14h	200mV
15h	240mV
16h	280mV
17h	320mV
18h	360mV
19h	400mV
1Ah	440mV
1Bh	480mV
1Ch	520mV
1Dh	560mV
1Eh	600mV
1Fh	640mV

Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.

10.2.29 Gate Control (R713h)

Gate Control (R713h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	VGHS[3:0]				VGLS[3:0]			
Default value			0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

Description

VGLS[3:0] : VGL voltage level selection.

VGLS[3:0]	VGL Voltage	VGLS[3:0]	VGL Voltage
0h	-12.87 V	8h	-10.38 V
1h	-12.56 V	9h	-10.07 V
2h	-12.25 V	Ah	-9.75 V
3h	-11.94 V	Bh	-9.44 V
4h	-11.52 V	Ch	-9.13 V
5h	-11.31 V	Dh	-8.82 V
6h	-11.00 V	Eh	-8.51 V
7h	-10.69 V	Fh	-8.20 V

VGHS[3:0] : VGH voltage level selection.

VGHS[3:0]	VGH Voltage	VGHS[3:0]	VGH Voltage
0h	12.16 V	8h	13.70 V
1h	12.36 V	9h	13.89 V
2h	12.55 V	Ah	14.09 V
3h	12.74 V	Bh	14.28 V
4h	12.93 V	Ch	14.47 V
5h	13.13 V	Dh	14.66 V
6h	13.32 V	Eh	14.86 V
7h	13.51 V	Fh	15.05 V

Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.

10.2.30 Frame Rate Control (R724h)

Frame Rate Control (R724h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	DIVI[1:0]		0	RTNI[4:0]				
Default value			0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1

Description

RTNI[4:0] : Sets the fOSC value so that the line period will be affected.

RTNI[4:0]	fOSC Value (MHz)	1 Line Period (μs)
00h~0Fh	Setting Prohibited	
10h	5.38	23.8
11h	5.06	25.3
12h	4.78	26.8
13h	4.53	28.3
14h	4.30	29.8
15h	4.10	31.2
16h	3.91	32.7
17h	3.74	34.2
18h	3.58	35.8
19h	3. 4	37.2
1Ah	3.31	38.7
1Bh	3.19	40.1
1Ch	3.07	41.7
1Dh	2.97	43.1
1Eh	2.87	44.6
1Fh	2.77	46.2

DIVI[1:0] : Sets the division ratio of internal clock frequency.

DIVI[1:0]	Division Ratio
0h	1
1h	2
2h	4
3h	8

Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.

10.2.31 Source Driving Control (R752h)

Source Driving Control (R752h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	SD[1]	SD[0]	1	1	1	1
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

SD[1:0] : Source Driving Control

WCMD[7:0]	Driving
0Fh	Small
1Fh	Medium
2Fh	Medium High
3Fh	Large

Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.

10.2.32 Gate Turn on Timing Control (R754)

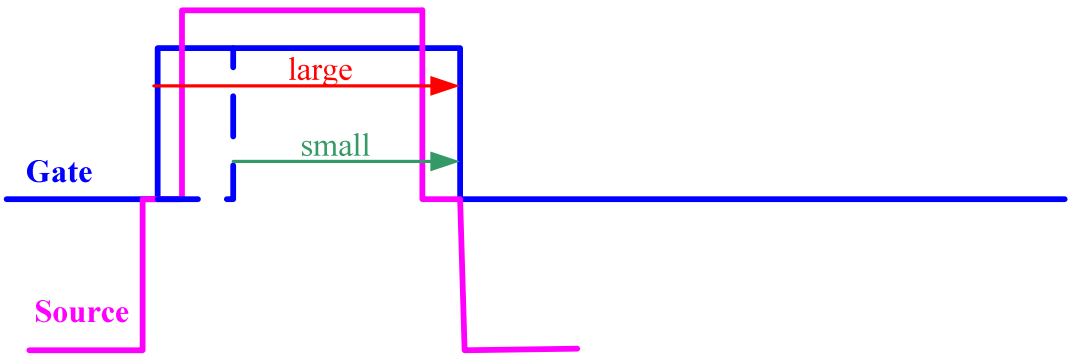
Gate Turn on Timing Control (R754h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	TGO[5]	TGO[4]	TGO[3]	TGO[2]	TGO[1]	TGO[0]
Default value			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Description

TGO[5:0] : Gate turn Timing Control

TGO[5:0]	Turn on Timing
00h	Large
|	|
3Fh	Small

Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.



10.2.33 NVM Write Control (R7E1h)

NVM Write Control (R7E1h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	WCMD[7:0]							
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

RCMD[7:0] : NVM Write Operation Selection

WCMD[7:0]	Function
3Ah	Program
A5h	Active Code
C5h	Erase
Others	Setting Prohibited

After writing Program (3Ah) / Erase (C5h) parameter, Active Code (A5h) must be appended as the second parameter to activate the operation specified by the first parameter.

Note: CMD2_EN (R0FFh) must be set to '1' before accessing this register.

11 RESET FUNCTION

The ST7793 is initialized by the RESET input. During reset period, the ST7793 is in a busy state and instruction from the MCU and DRAM access are not accepted. The ST7793's internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, DRAM access and initial instruction setting are prohibited.

11.1.. Register Values

See the Instruction description. The default value is shown in the parenthesis of each instruction bit cell.

11.2.. Display RAM Data Initialization

The Display RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period (BASEE=0).

11.3.. Reset Timing Characteristic

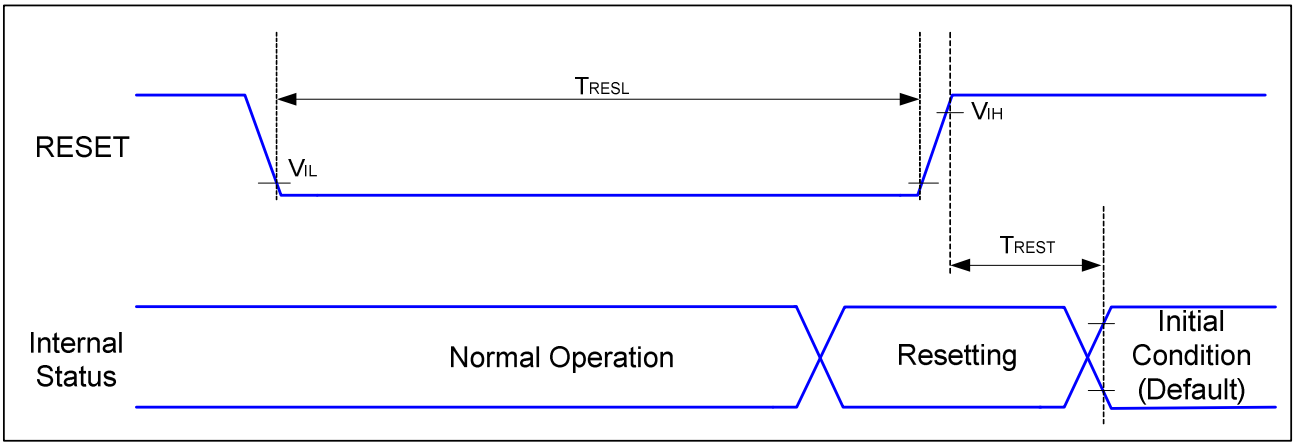


Figure 41 Reset Timing

VDDI=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
RESET	TRESL	Reset Low Level Width	1	-	ms	-
	TREST	Reset Complete Time	1		ms	

Table 8 Reset timing Characteristics

12 FMARK FUNCTION

The ST7793 outputs an FMARK pulse when the ST7793 is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

FMI[2:0]	Output Interval
“000”	1 Frame
“001”	2 Frame
“011”	4 Frame
“101”	6 Frame
Others	Setting Prohibited

Table 9 FMARK Interval

FMP[8:0]	FMARK Output Position
000h	0 th line
001h	1 st line
002h	2 nd line
003h	3 rd line
. . .	. . .
1BDh	445 th line
1BEh	446 th line
1BFh	447 th line
177h	Setting Prohibited

Table 10 FMARK Output Position

12.1.. FMP Setting Example

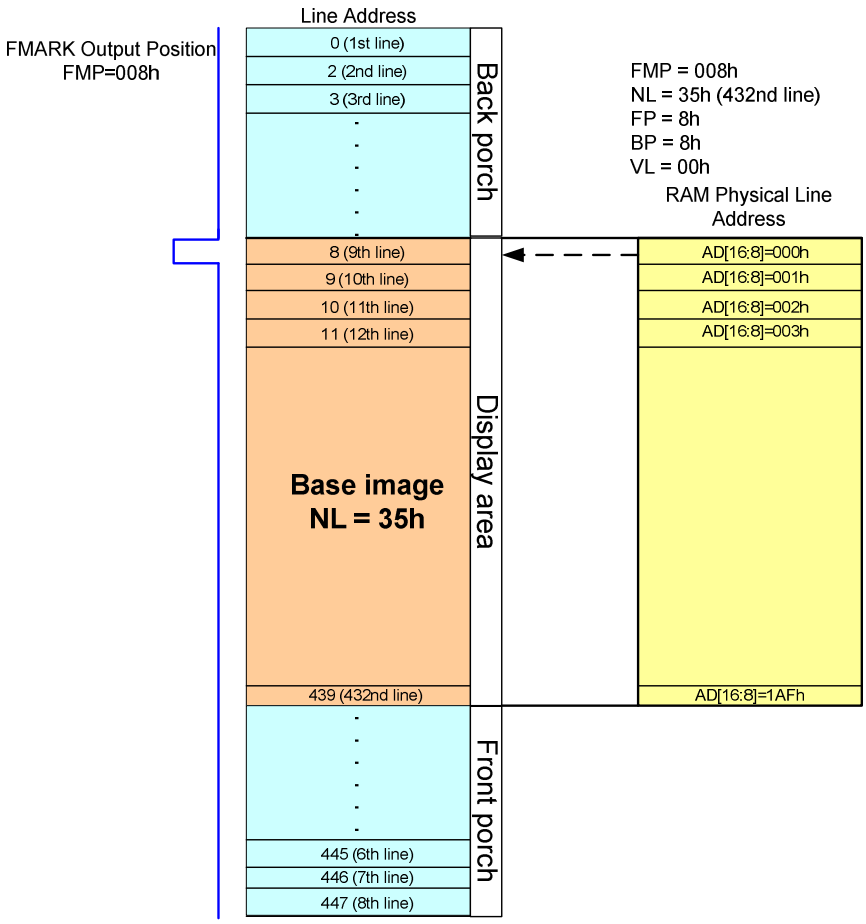


Figure 42 FMARK Setting Example

12.2.. Display Operation Synchronous Data Transfer Using FMARK

The ST7793 uses FMARK signal as a trigger output for indicating the start of data-writing to the internal DRAM in synchronization with display scan operation.

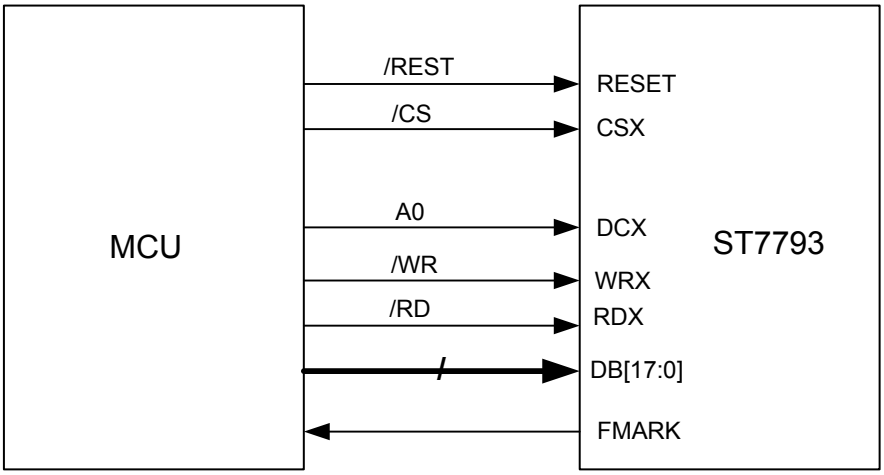


Figure 43 FMARK Interface Connection

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture DRAM area without causing flicker on the display. The data is written in the internal RAM in order to transfer only the data written over the moving picture display area and minimize the data transfer required for moving picture display.

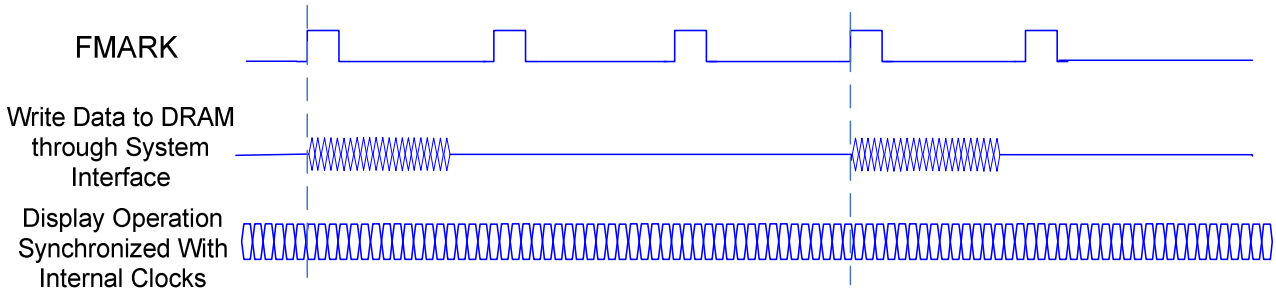


Figure 44 Moving Picture Data Transfers via FMARK Function

When transferring data in synchronization with FMARK signal, frame frequency and minimum DRAM data write speed must be taken into consideration. First, all DRAM writes must be completed within one frame. Secondly, each write operation of pixel data must be done within the minimum DRAM Write Speed. They can be calculated from the following equations.

$$Frame\ \ Period\ = \frac{(DisplayLin\ \ es(NL) + FrontPorch\ \ (FP) + BackPorch\ \ (BP)) \times 128}{fOSC\ [Hz\ ](RTNI\ )}$$

$$DRAM\ \ Write\ \ Speed\ (\min .)[Hz\ ] > \frac{fOSC\ [Hz\ ](RTNI\ ) \times 240}{128}$$

Note: When RAM write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

Examples of DRAM writes speed and the frequency of the internal clocks are as follows.

Example:

Display size 240 RGB x 432 lines,

Total number of lines (NL) 432 lines

Back/Front porch: 13/3 lines

Internal Clock Frequency (RTNI[4:0]): 3.44MHz

Frame Data Update Period < $\frac{(432 + 3 + 13) \times 128}{3.44 \times 10^6} = 16.669\ ms$

Note1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one FMARK cycle.

Note2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum Speed for DRAM Writing [Hz] > $\frac{3.44 \times 10^6 \times 240}{128} = 6.45\ MHz$

Note1. In this example, it is assumed that the ST7793 starts writing data in the internal DRAM on the rising edge of FMARK.

Note2. There must be at least a margin of 2 lines between the line to which the ST7793 has just written data and the line where display operation on the LCD is performed.

Note3. The FMARK signal output position is set to the line specified by FMP[8:0] bits.

In this example, DRAM write operation at a speed of 6.45MHz or more, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the ST7793 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

13 8 - COLOR DISPLAY MODE

The ST7793 has a function to display in 8 colors. In this display mode, only V0 and V63 are used and power supplies to other grayscales are turned off to reduce power consumption. The ST7793 does not need DRAM data rewrite for 8-color display. ST7793 uses the MSB of each sub-pixel as the rest part in each dot data to display in 8 colors.

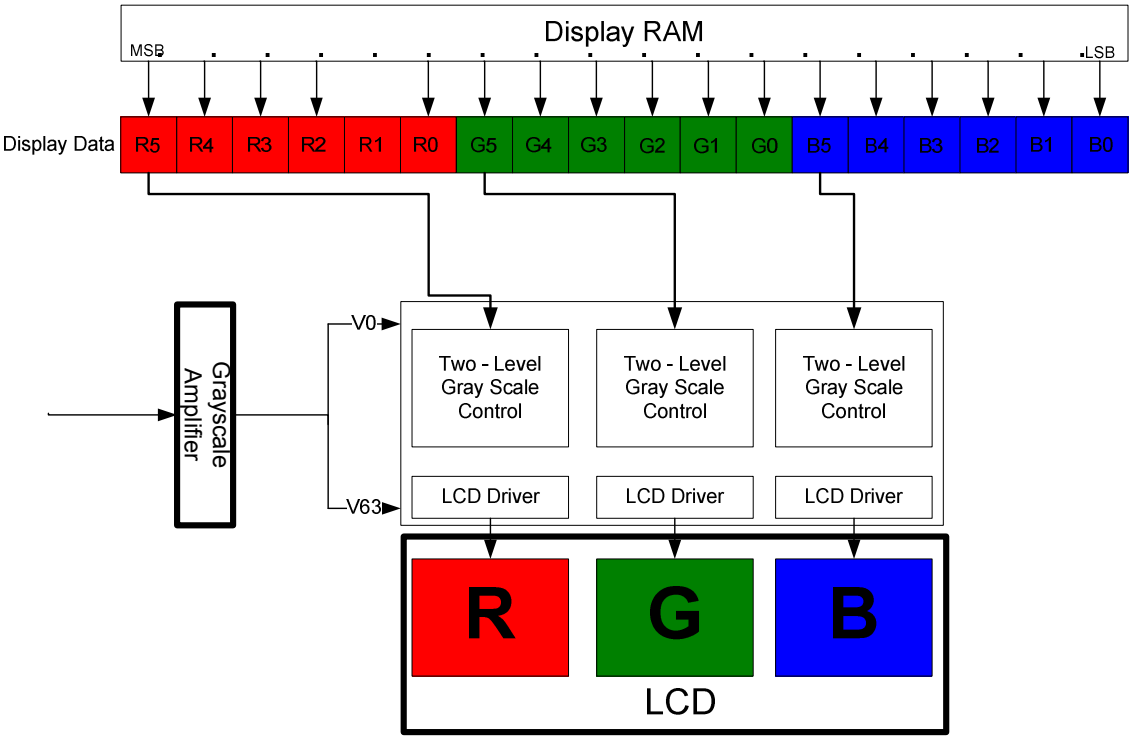


Figure 45 8-Color Display Mode

Follow the figures below to switch between 8-color display mode and 262k-color display mode.

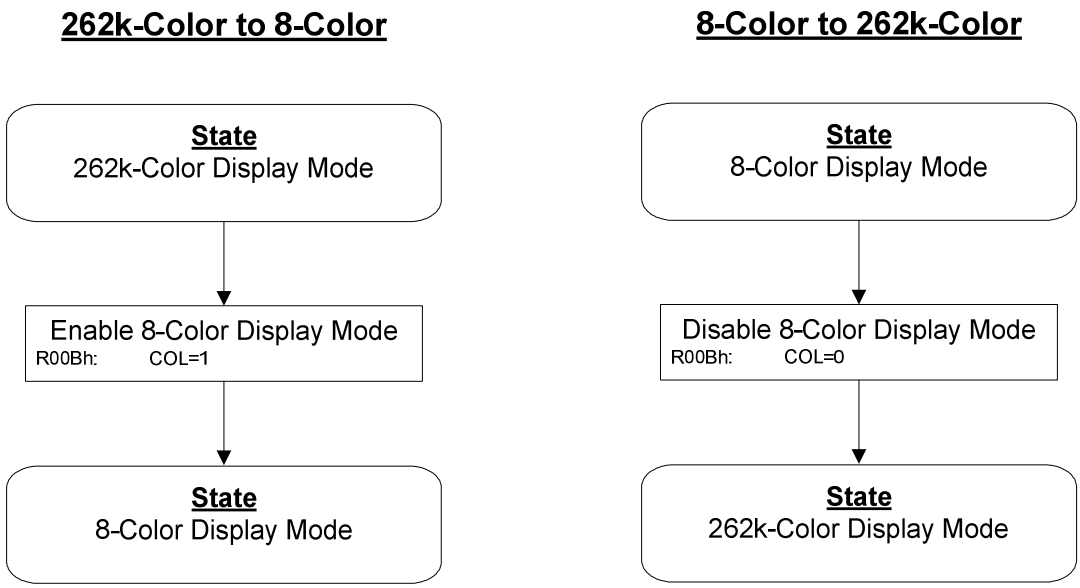


Figure 46 8-Color / 262k-Color Switch Sequences

14 PARTIAL DISPLAY FUNCTION

The ST7793 allows selectively driving partial image on the screen at arbitrary positions set in the screen drive position registers. To switch between full-screen display and partial display mode, follow the sequences below.

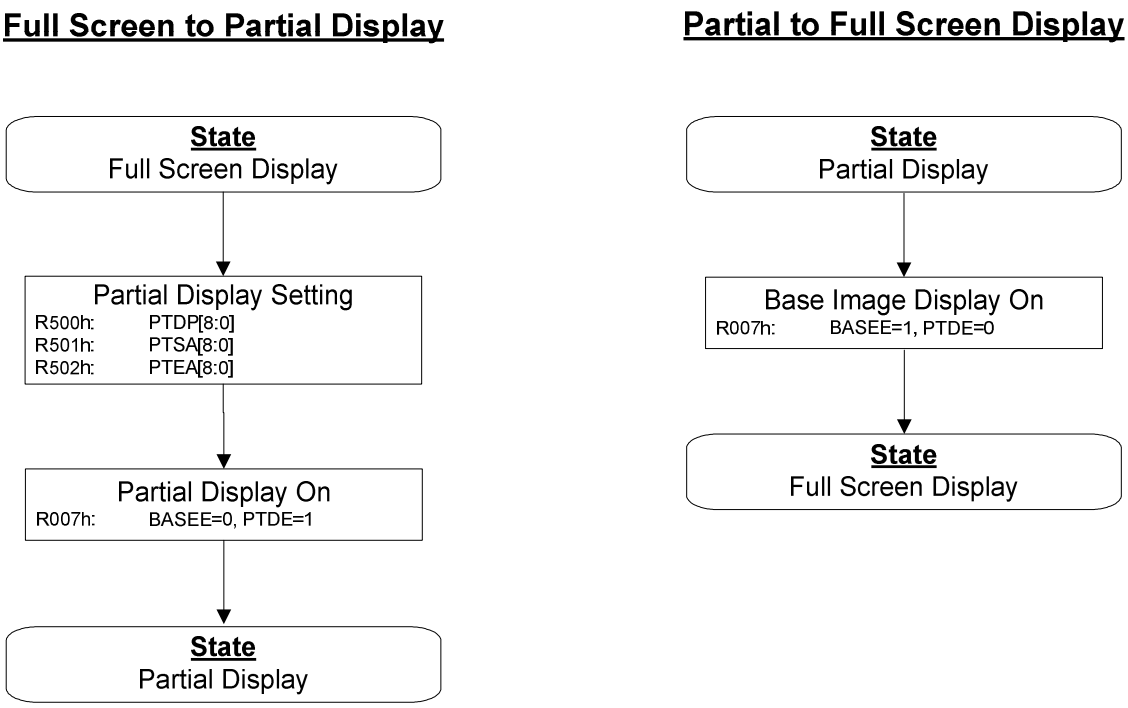


Figure 47 Shutdown Mode Enter/Exit Sequences

The following example shows the setting for partial display function:

Base Image Display Setting	
BASEE	1
PTDE	0
Partial Image Display Setting	
BASEE	0
PTDE	1
PTSA[8:0]	020h
PTEA[8:0]	02Fh
PTDP[8:0]	0C0h

Table 11 Partial Setting Example

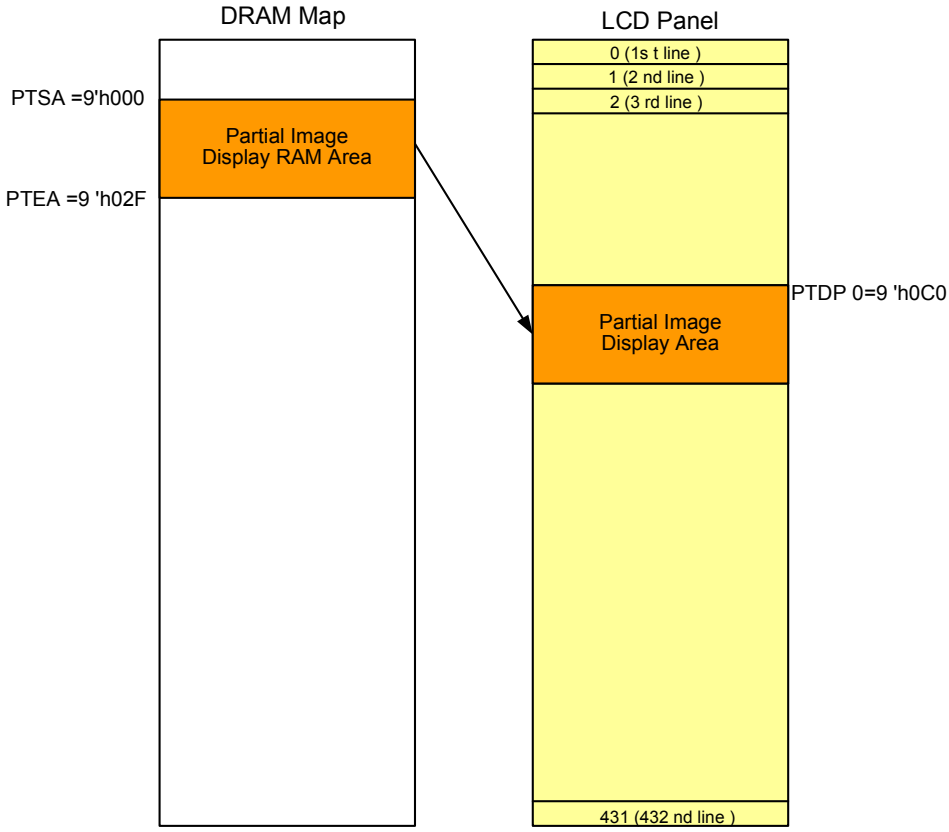
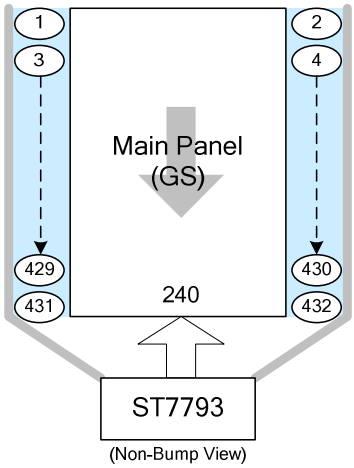
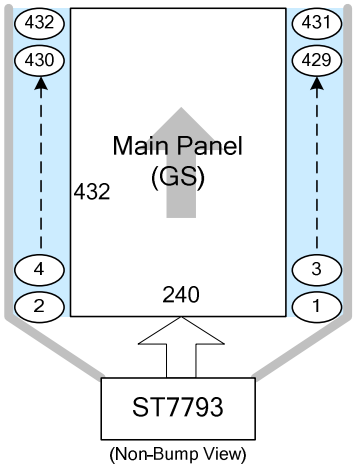


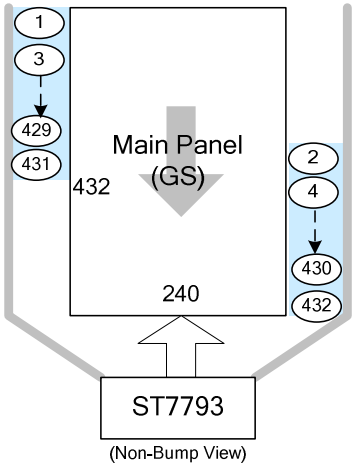
Figure 48 Partial Display Example

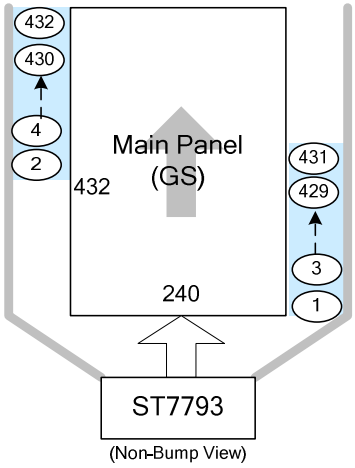
15 SCAN MODE

The ST7793 can set the gate pin assignment and the scan direction in the following 4 ways by setting SM and GS bits to meet various connections between the ST7793 and the LCD panel.

<table>
<tr><th>SM</th><th>Scan Direction</th><th></th></tr>
<tr><td>0</td><td>Interchanging Forward Direction (GS=0)
 

Scan Order (Gate Line No.)
G1=>G2=>G3=>G4...G429=>G430=>G431=>G432</td><td>Interchanging Backward Direction (GS=1)
 

Scan Order (Gate Line No.)
G432=>G431=>G430=>G429...G4=>G3=>G2=>G1</td></tr>
<tr><td>1</td><td>Left/Right Forward Direction (GS=0)
 

Scan Order (Gate Line No.)
G1=>G3...G429=>G431=>G2=>G4...G430=>G432</td><td>Left/Right Forward Direction (GS=1)
 

Scan Order (Gate Line No.)
G432=>G430...G4=>G2=>G431=>G429...G3=>G1</td></tr>
</table>

Figure 49 Scan Mode Settings

16 WINDOW ADDRESS FUNCTION

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal Display RAM. The window address area is made by setting the horizontal address register (star: HSA [7:0], end HEA [7:0] bits) and the vertical address register (start: VSA [8:0], end: VEA [8:0] bits) The AM and ID bits sets the transition direction of RAM address (either increment or decrement, horizontal or vertical). These bits enable the ST7793 to write data including image data consecutively without taking data wrap positions into account.

The window address area must be made within the DRAM address map area. Also, DRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]
(Horizontal direction) 00H ≦ HSA[7:0] ≦ HEA[7:0] ≦ EFh
(Vertical direction) 00H ≦VSA[8:0] ≦ VEA[8:0] ≦ 1AFh
[RAM address, AD (an address within a window address area)]
(RAM address) HSA[7:0] ≦AD[7:0] ≦HEA[7:0]
VSA[8:0] ≦AD[16:8] ≦VEA[8:0]

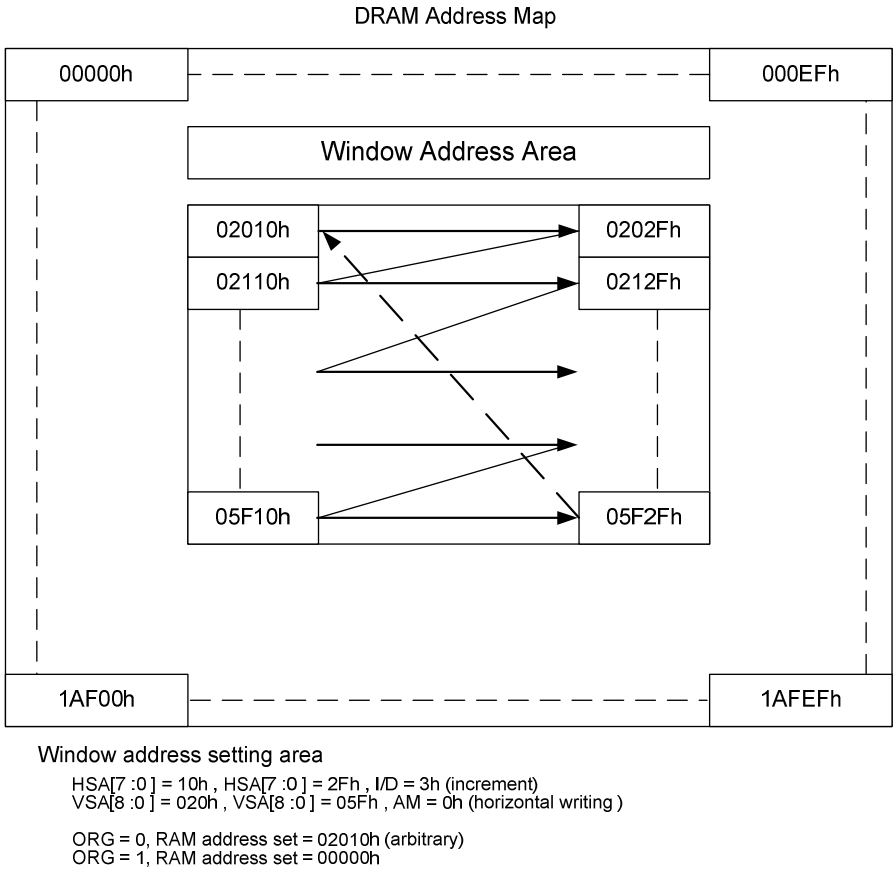


Figure 50 Display RAM Access Window Map

17 GAMMA CORRECTION

The ST7793 supports γ-correction function to make the optimal colors according to the characteristics of the panel. The ST7793 has registers for positive and negative polarities.

17.1.. Gamma Correction Circuits

The following figure shows the γ-correction circuit. According to the settings of variable resistors R0 to R8, the voltage level, the difference between VAP/VBP and VAN/VBN, is evenly divided into 8 grayscale reference voltages (V0, V1, V8, V20, V43, V55, V62, and V63). Other 56-grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltage, see “Grayscale Voltage Calculation Formula”.

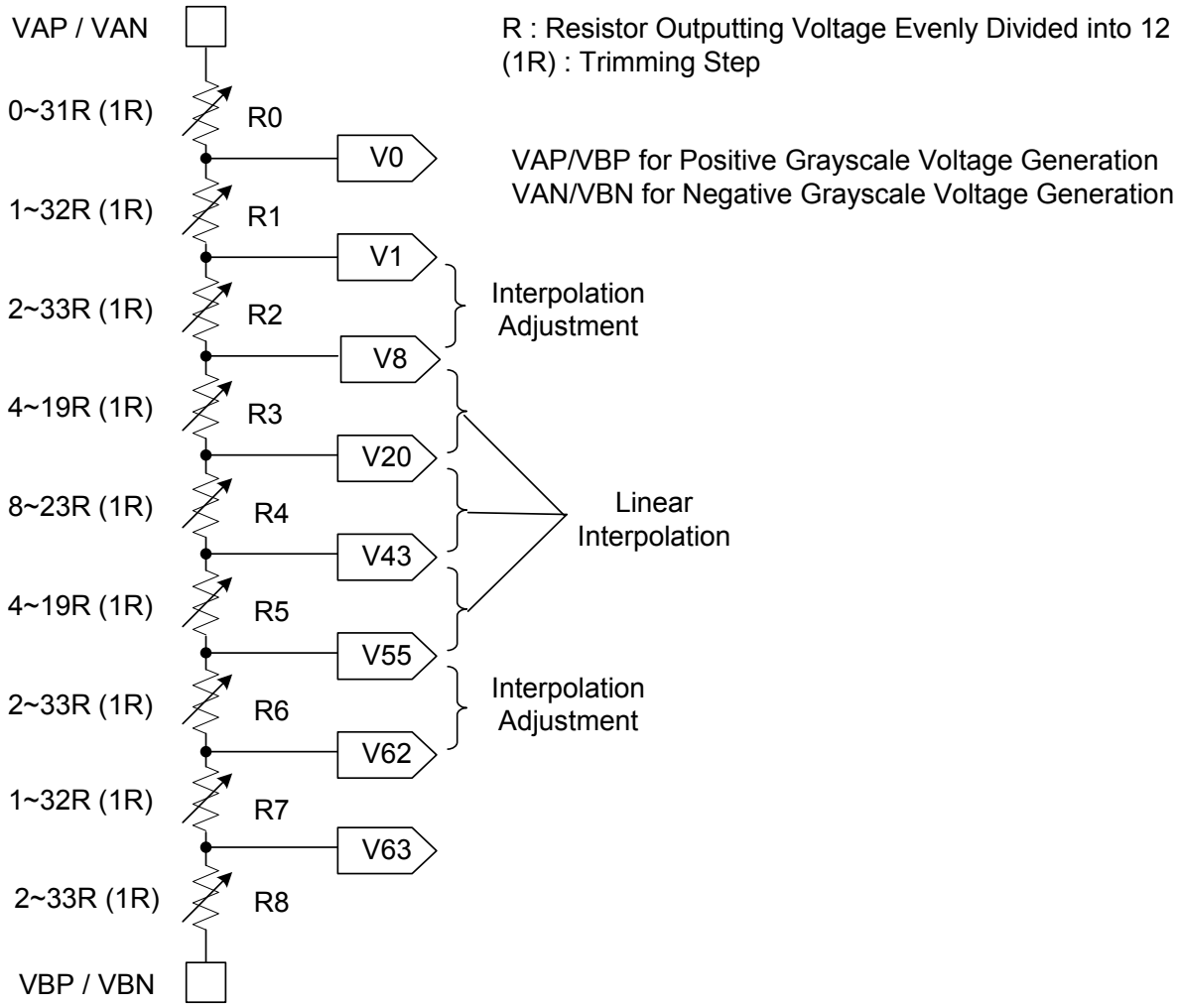


Figure 51 Grayscale Voltage Generation

17.2.. Gamma Correction Registers

The γ-correction registers include 42 bits for each of R, G, and B dots and 8-bit interpolation adjustment registers.

1. Reference Level Adjustment Registers

Resistor	Positive Polarity	Negative Polarity
R0	PR0P00[4:0]	PR0N00[4:0]
R1	PR0P01[4:0]	PR0N01[4:0]
R2	PR0P02[4:0]	PR0N02[4:0]
R3	PR0P03[3:0]	PR0N03[3:0]
R4	PR0P04[3:0]	PR0N04[3:0]
R5	PR0P05[3:0]	PR0N05[3:0]
R6	PR0P06[4:0]	PR0N06[4:0]
R7	PR0P07[4:0]	PR0N07[4:0]
R8	PR0P08[4:0]	PR0N08[4:0]

Table 12 Reference Level Adjustment Registers

Resistor	Register		Resistance	Resistor	Register		Resistance
	Name	Value			Name	Value	
R0	PR0*00[4:0]	00h 01h … 1Fh	0R 1R … 31R	R5	PR0*05[3:0]	0h 1h … Fh	4R 5R … 19R
R1	PR0*01[4:0]	00h 01h … 1Fh	1R 2R … 32R	R6	PR0*06[4:0]	00h 01h … 1Fh	2R 3R … 33R
R2	PR0*02[4:0]	00h 01h … 1Fh	2R 3R … 33R	R7	PR0*07[4:0]	00h 01h … 1Fh	1R 2R … 32R
R3	PR0*03[3:0]	0h 1h … Fh	4R 5R … 19R	R8	PR0*08[4:0]	00h 01h … 1Fh	2R 3R … 33R

R4	PR0*04[3:0]	0h 1h … Fh	8R 9R … 23R	-	-	-	-

*Note: * could be P or N.*

Table 13 Reference Level Adjustment Registers and Resistors

2. Interpolation Registers

Interpolation Adjustment	Positive Polarity	Negative Polarity
V2~V7	PI0P0[1:0]	PI0N0[1:0]
	PI0P1[1:0]	PI0N1[1:0]
V56~V61	PI0P2[1:0]	PI0N2[1:0]
	PI0P3[1:0]	PI0N3[1:0]

Table 14 Interpolation Registers

PI0*0[1:0]	PI0*1[1:0]	IPV2	IPV3	IPV4	IPV5	IPV6	IPV7
0h	0h	81%	67%	52%	39%	26%	13%
	1h	78%	61%	43%	33%	22%	11%
	2h	73%	52%	31%	23%	15%	8%
	3h	72%	50%	28%	21%	14%	7%
1h	0h	80%	68%	56%	42%	28%	14%
	1h	76%	62%	48%	36%	24%	12%
	2h	70%	52%	35%	26%	17%	9%
	3h	69%	50%	31%	23%	16%	8%
2h	0h	78%	70%	61%	46%	30%	15%
	1h	74%	63%	53%	39%	26%	13%
	2h	66%	53%	39%	29%	20%	10%
	3h	64%	50%	36%	27%	18%	9%
3h	0h	78%	70%	63%	47%	31%	16%
	1h	73%	64%	54%	41%	27%	14%
	2h	65%	53%	41%	31%	20%	10%
	3h	63%	50%	37%	28%	19%	9%

*Note: * could be P or N.*

Table 15 Interpolation Factor for V2 to V7

PI0*3[1:0]	PI0*2[1:0]	IPV56	IPV57	IPV58	IPV59	IPV60	IPV61
0h	0h	87%	74%	61%	48%	33%	19%
	1h	89%	78%	67%	57%	39%	22%
	2h	92%	85%	77%	69%	48%	27%
	3h	93%	86%	79%	72%	50%	28%
1h	0h	86%	72%	58%	44%	32%	20%
	1h	88%	76%	64%	52%	38%	24%
	2h	91%	83%	74%	65%	48%	30%
	3h	92%	84%	77%	69%	50%	31%
2h	0h	85%	70%	54%	39%	30%	22%
	1h	87%	74%	61%	47%	37%	26%
	2h	90%	80%	71%	61%	47%	34%
	3h	91%	82%	73%	64%	50%	36%
3h	0h	84%	69%	53%	38%	30%	22%
	1h	86%	73%	59%	46%	36%	27%
	2h	90%	80%	69%	59%	47%	35%
	3h	91%	81%	72%	63%	50%	37%

*Note: * could be P or N.*

Table 16 Interpolation Factor for V56 to V61

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	ΔV x Σ(R1…R8) / SUMR	V32	V43 + (V20 - V43) x 11/23
V1	ΔV x Σ(R2…R8) / SUMR	V33	V43 + (V20 - V43) x 10/23
V2	V8 + (V1 - V8) x IPV2	V34	V43 + (V20 - V43) x 9/23
V3	V8 + (V1 - V8) x IPV3	V35	V43 + (V20 - V43) x 8/23
V4	V8 + (V1 - V8) x IPV4	V36	V43 + (V20 - V43) x 7/23
V5	V8 + (V1 - V8) x IPV5	V37	V43 + (V20 - V43) x 6/23
V6	V8 + (V1 - V8) x IPV6	V38	V43 + (V20 - V43) x 5/23
V7	V8 + (V1 - V8) x IPV7	V39	V43 + (V20 - V43) x 4/23
V8	ΔV x Σ(R3…R8) / SUMR	V40	V43 + (V20 - V43) x 3/23
V9	V20 + (V8 - V20) x 11/12	V41	V43 + (V20 - V43) x 2/23
V10	V20 + (V8 - V20) x 10/12	V42	V43 + (V20 - V43) x 1/23
V11	V20 + (V8 - V20) x 9/12	V43	ΔV x Σ(R5…R8) / SUMR
V12	V20 + (V8 - V20) x 8/12	V44	V55 + (V43 - V55) x 11/12
V13	V20 + (V8 - V20) x 7/12	V45	V55 + (V43 - V55) x 10/12
V14	V20 + (V8 - V20) x 6/12	V46	V55 + (V43 - V55) x 9/12
V15	V20 + (V8 - V20) x 5/12	V47	V55 + (V43 - V55) x 8/12
V16	V20 + (V8 - V20) x 4/12	V48	V55 + (V43 - V55) x 7/12
V17	V20 + (V8 - V20) x 3/12	V49	V55 + (V43 - V55) x 6/12
V18	V20 + (V8 - V20) x 2/12	V50	V55 + (V43 - V55) x 5/12
V19	V20 + (V8 - V20) x 1/12	V51	V55 + (V43 - V55) x 4/12
V20	ΔV x Σ(R4…R8) / SUMR	V52	V55 + (V43 - V55) x 3/12
V21	V43 + (V20 - V43) x 22/23	V53	V55 + (V43 - V55) x 2/12
V22	V43 + (V20 - V43) x 21/23	V54	V55 + (V43 - V55) x 1/12
V23	V43 + (V20 - V43) x 20/23	V55	ΔV x Σ(R6…R8) / SUMR
V24	V43 + (V20 - V43) x 19/23	V56	V62 + (V55 - V62) x IPV56
V25	V43 + (V20 - V43) x 18/23	V57	V62 + (V55 - V62) x IPV57
V26	V43 + (V20 - V43) x 17/23	V58	V62 + (V55 - V62) x IPV58
V27	V43 + (V20 - V43) x 16/23	V59	V62 + (V55 - V62) x IPV59
V28	V43 + (V20 - V43) x 15/23	V60	V62 + (V55 - V62) x IPV60
V29	V43 + (V20 - V43) x 14/23	V61	V62 + (V55 - V62) x IPV61
V30	V43 + (V20 - V43) x 13/23	V62	ΔV x (R7 + R8) / SUMR
V31	V43 + (V20 - V43) x 12/23	V63	ΔV x R8 / SUMR

Note: *⊿V = GVDD – GND when calculating positive grayscale voltage*

⊿V = GVCL – GND when calculating negative grayscale voltage

SUMR = ∑(R0…R8) ≥ 70R

V63 ≥ 0.2V

Table 17 Grayscale Voltage Calculation Formula

3. Display RAM Data and the Grayscale Voltage

Frame Memory Data	Grayscale Voltage				Frame Memory Data	Grayscale Voltage			
	REV = 1		REV = 0			REV = 1		REV = 0	
	Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity		Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity
00h	V0	V63	V63	V0	20h	V32	V31	V31	V32
01h	V1	V62	V62	V1	21h	V33	V30	V30	V33
02h	V2	V61	V61	V2	22h	V34	V29	V29	V34
03h	V3	V60	V60	V3	23h	V35	V28	V28	V35
04h	V4	V59	V59	V4	24h	V36	V27	V27	V36
05h	V5	V58	V58	V5	25h	V37	V26	V26	V37
06h	V6	V57	V57	V6	26h	V38	V25	V25	V38
07h	V7	V56	V56	V7	27h	V39	V24	V24	V39
08h	V8	V55	V55	V8	28h	V40	V23	V23	V40
09h	V9	V54	V54	V9	29h	V41	V22	V22	V41
0Ah	V10	V53	V53	V10	2Ah	V42	V21	V21	V42
0Bh	V11	V52	V52	V11	2Bh	V43	V20	V20	V43
0Ch	V12	V51	V51	V12	2Ch	V44	V19	V19	V44
0Dh	V13	V50	V50	V13	2Dh	V45	V18	V18	V45
0Eh	V14	V49	V49	V14	2Eh	V46	V17	V17	V46
0Fh	V15	V48	V48	V15	2Fh	V47	V16	V16	V47
10h	V16	V47	V47	V16	30h	V48	V15	V15	V48
11h	V17	V46	V46	V17	31h	V49	V14	V14	V49
12h	V18	V45	V45	V18	32h	V50	V13	V13	V50
13h	V19	V44	V44	V19	33h	V51	V12	V12	V51
14h	V20	V43	V43	V20	34h	V52	V11	V11	V52
15h	V21	V42	V42	V21	35h	V53	V10	V10	V53
16h	V22	V41	V41	V22	36h	V54	V9	V9	V54
17h	V23	V40	V40	V23	37h	V55	V8	V8	V55
18h	V24	V39	V39	V24	38h	V56	V7	V7	V56
19h	V25	V38	V38	V25	39h	V57	V6	V6	V57
1Ah	V26	V37	V37	V26	3Ah	V58	V5	V5	V58

1Bh	V27	V36	V36	V27	3Bh	V59	V4	V4	V59
1Ch	V28	V35	V35	V28	3Ch	V60	V3	V3	V60
1Dh	V29	V34	V34	V29	3Dh	V61	V2	V2	V61
1Eh	V30	V33	V33	V30	3Eh	V62	V1	V1	V62
1Fh	V31	V32	V32	V31	3Fh	V63	V0	V0	V63

Table 18 Mapping of Frame Memory Data and Grayscale Voltage

18 APPLICATION

18.1.. Configuration of Power Supply Circuit

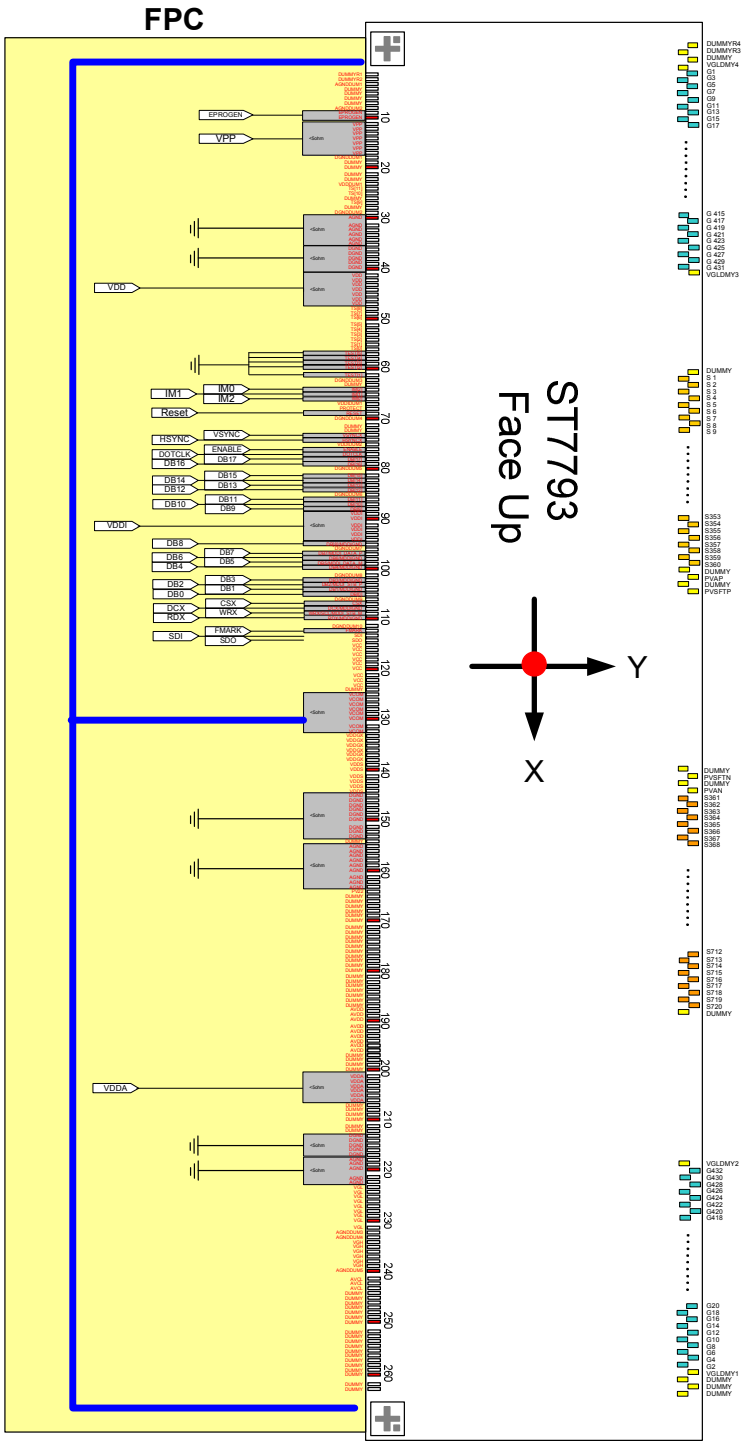


Figure 52 Power Supply Circuit Connection

18.2.. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ST7793 are as follows.

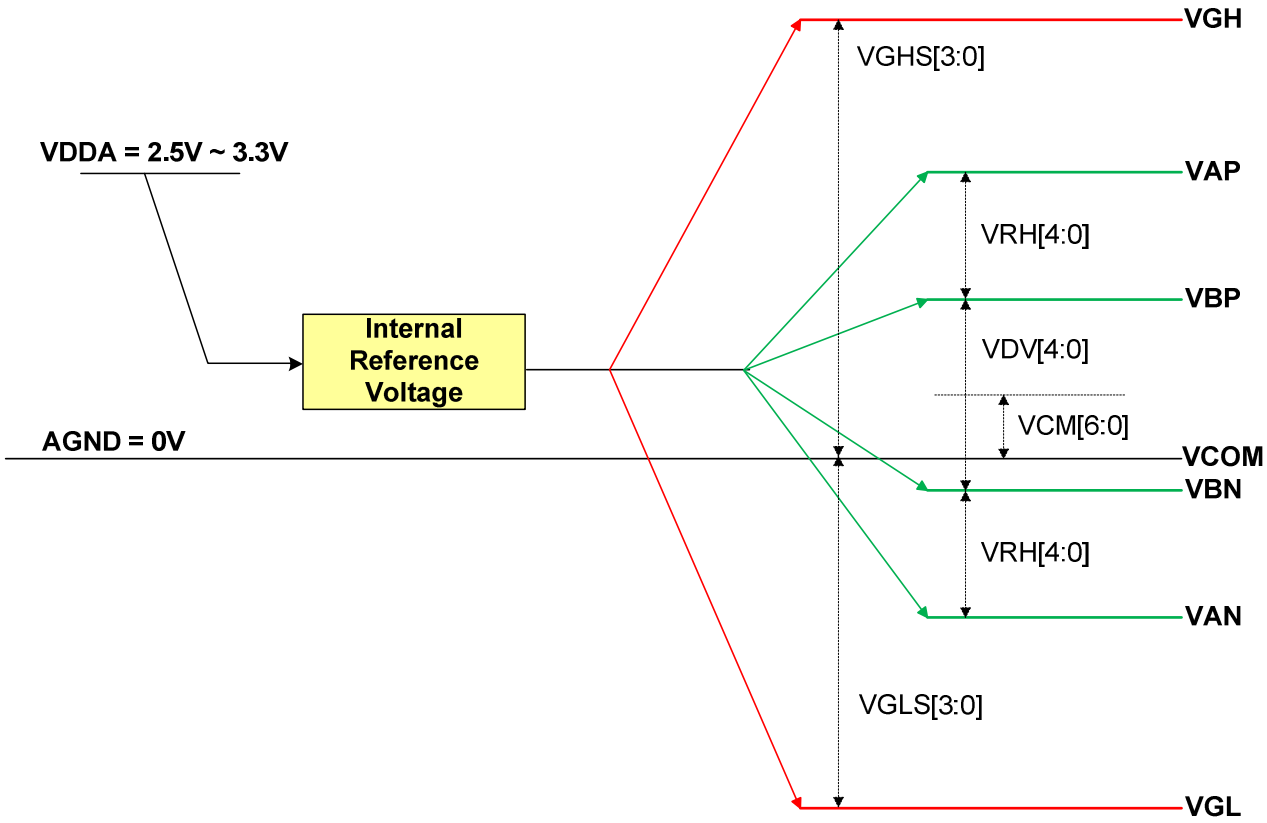


Figure 53 Power Booster Level

18.3.. Applied Voltage to the TFT panel

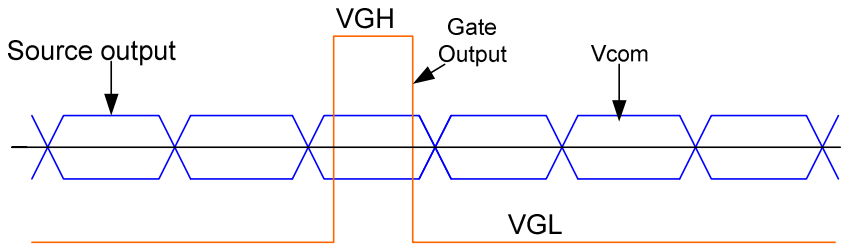


Figure 54 Voltage Output to TFT LCD Panel

18.4.. Power Supply Configuration

When supplying and cutting off power, the sequences below must be followed.

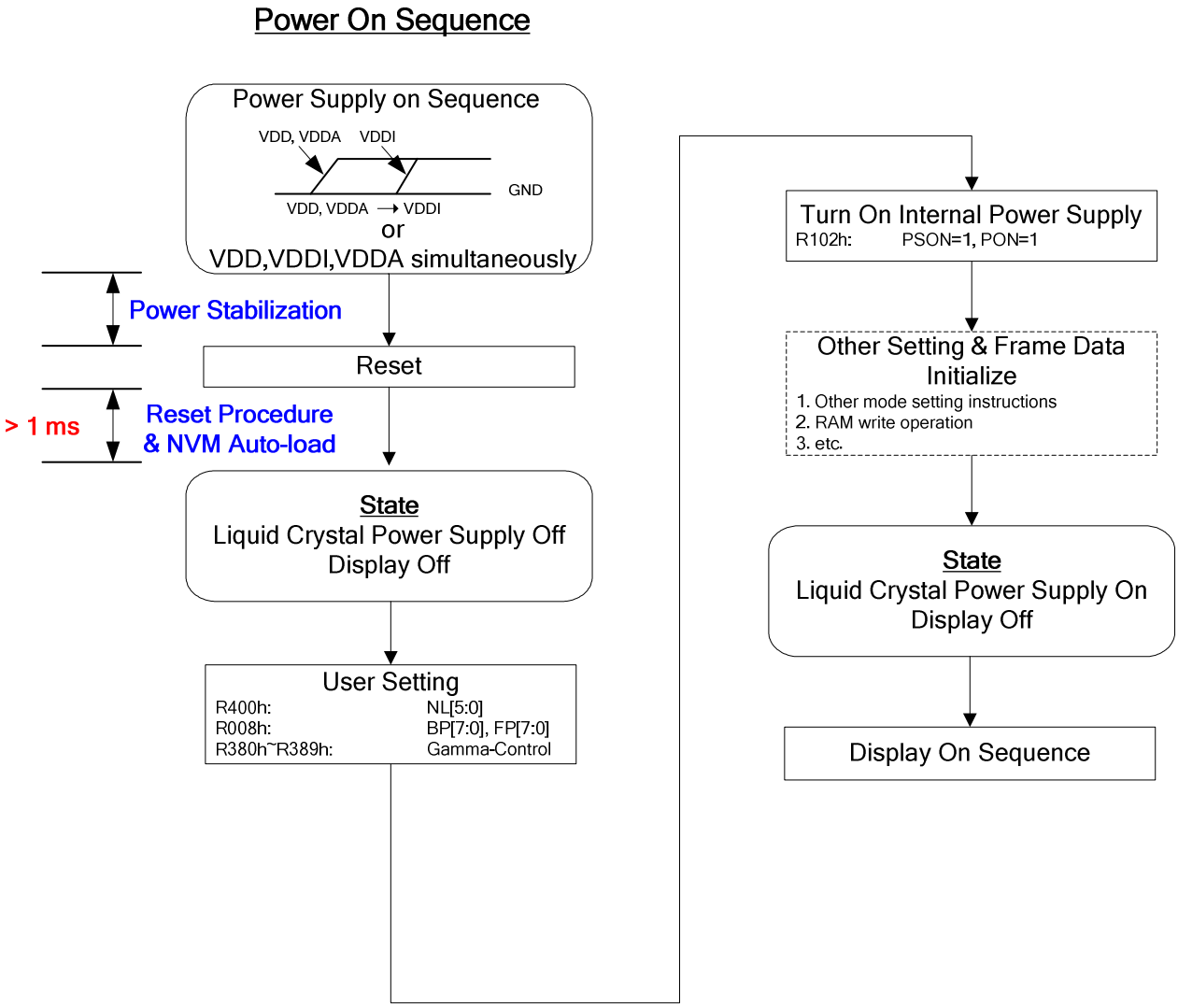


Figure 55 Power Supply On Sequence

Power Off Sequence

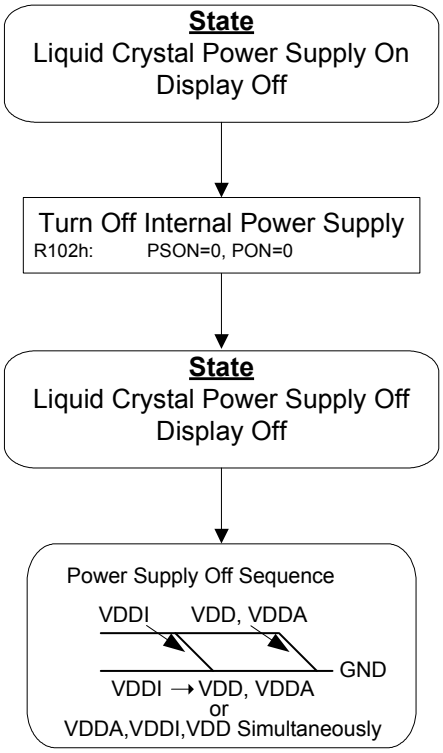


Figure 56 Power Supply Off Sequence

18.5.. Display On/Off Sequences

To switch between display-on and display-off mode, follow the sequences below.

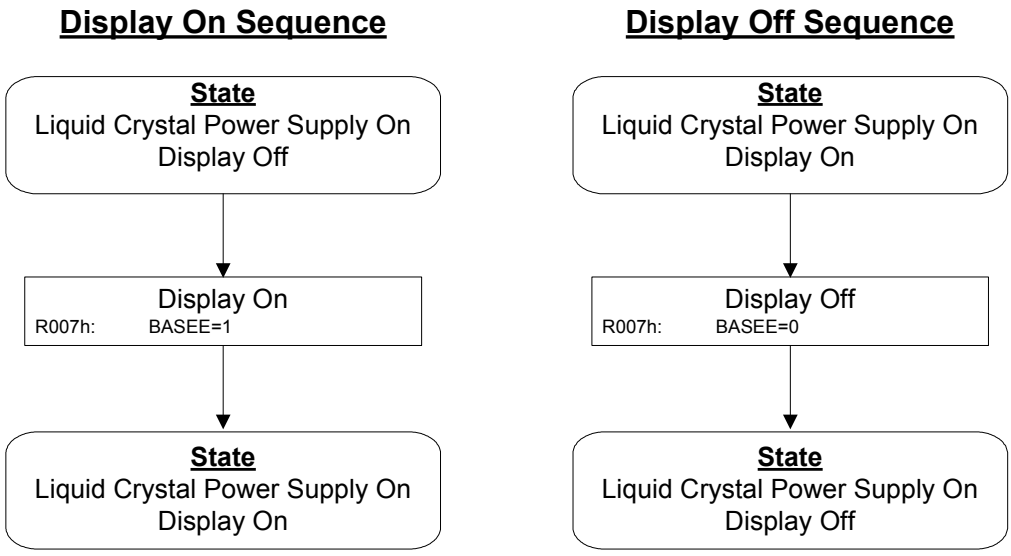


Figure 57 Display On/Off Sequences

18.6.. Refresh Sequences

To reduce malfunction caused by noise, execute refresh sequence 1 regularly. To exit shutdown mode, execute refresh sequence 2.

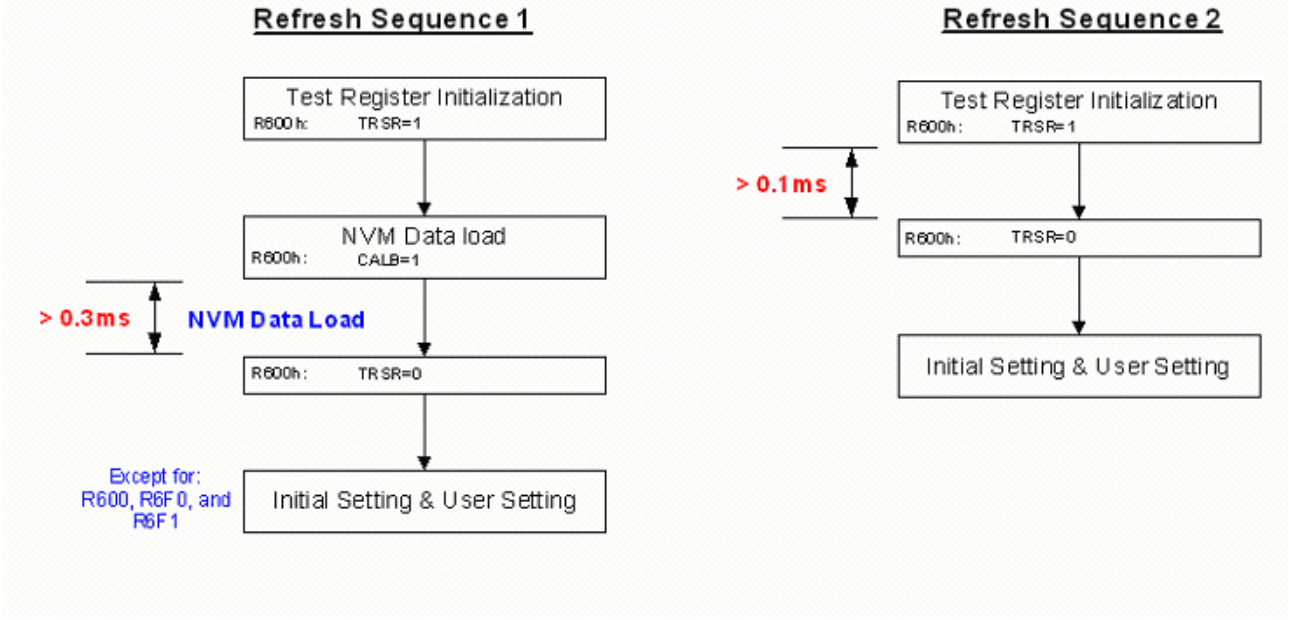


Figure 58 Refresh Sequences

18.7.. Shutdown Mode Sequences

Shutdown mode can be used to save power when display function is not required. To enter or exit from shutdown mode, refer to the following sequence.

Enter and Exit Shutdown Mode Sequence

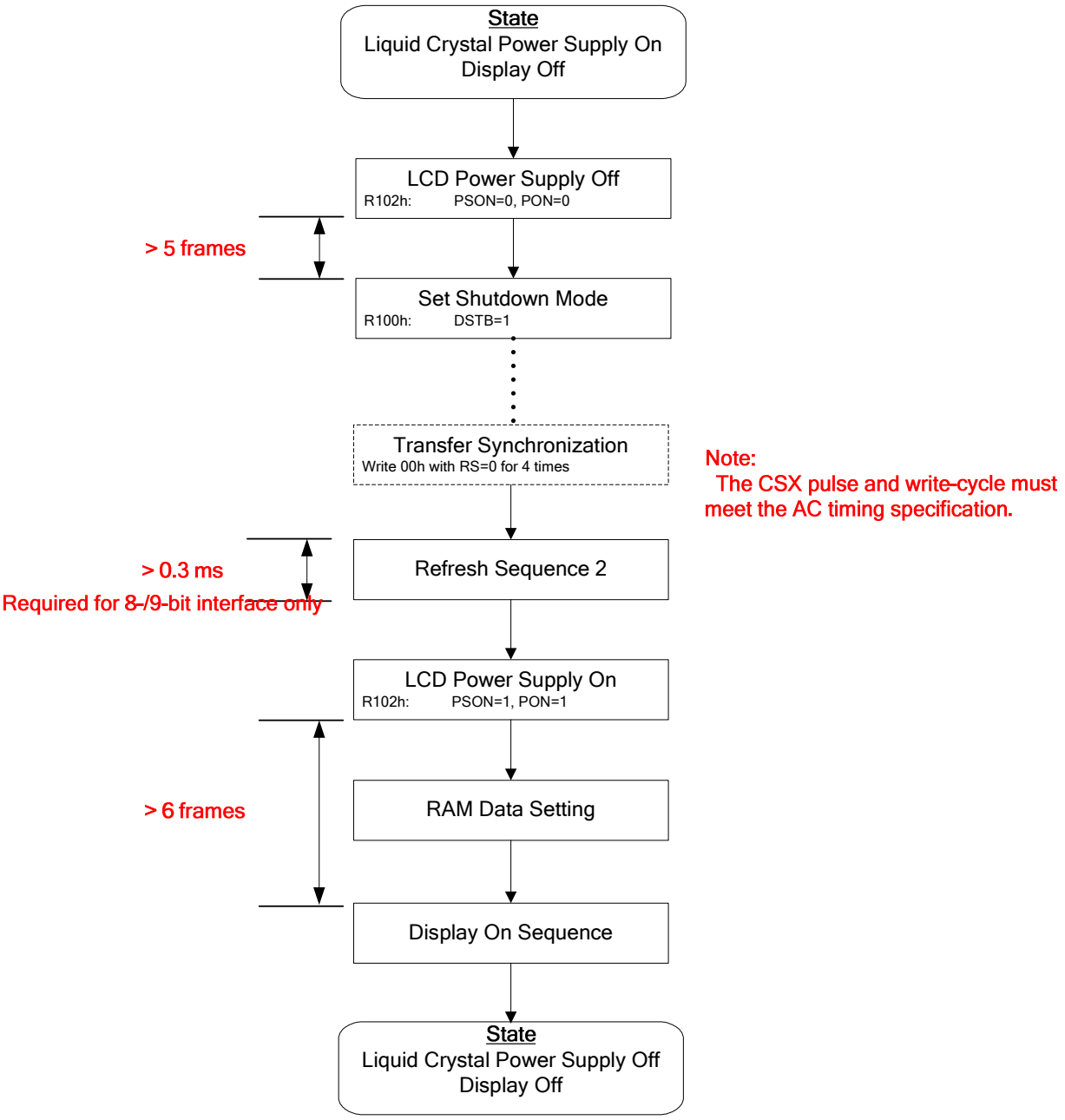


Figure 59 Shutdown Mode Enter/Exit Sequences

19 REVISION HISTORY

Version	Date	Description
V0.0	2010/11/11	Draft
V0.1	2011/11	Modified scan mode block / function default value
V0.2	2012/01	Modified the Alignment Mark pad location
V1.0	2012/04	Addition 709h & 752h Command Addition 754 Gate turn on Timing control Modify the Au bump height to 9um Modify the VGL Voltage
V1.1	2014/06	Modify Register 708h & 280h Modify the TSCL timing for SPI interface
V1.2	2014/08	Modify Chip thickness