Sitronix

ST7773

262K Color Single-Chip TFT Controller/Driver

1. Introduction

The ST7773 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 528 source line and 220 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts Serial Peripheral Interface (SPI), 8-bits/9-bits/16-bits/18-bits parallel interface. Display data can be stored in the on-chip display data RAM of 176 x 220 x 18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

2. Features

- Single chip TFT-LCD controller/driver with display data RAM
- Display resolution: 176 (H) x RGB x 220 (V)
- Display data RAM (frame memory): 176 x 220 x 18-bits = 696,960 bits
- Output:
  - 176 ch source outputs (176 x RGB)
  - 220 ch gate outputs
  - Common electrode output
- Display mode (color mode)
  - Full color mode (idle mode off): 262K-colors
  - Reduce color mode (idle mode on): 8-colors (1-bit for individual R, G, B color depth)
- Display resolution option
  - 176 x 220 display with 176 x 18-bits x 220 display RAM
- Supported LC type
  - Normally white LC-type
  - Normally black LC-type
- Supported data format on display host interface
  - 12-bits/pixel: RGB= (444) using the 384k-bits frame memory and LUT
  - 16-bits/pixel: RGB= (565) using the 384k-bits frame memory and LUT
  - 18-bits/pixel: RGB= (666) using the 384k-bits frame memory
- Supported MCU Interface
  - 3-line serial interface
  - 4-line serial interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 6800-series MCU
  - 8-bits, 16-bits, 18-bits RGB interface with graphic controller
- Display features
  - Area scrolling
  - Partial display mode
  - Software programmable color depth mode
- Build-in circuit
  - DC/DC converter
  - Adjustable VCOM generation
  - Non-volatile (NV) memory to store initial register setting
  - Oscillator for display clock generation
  - Timing controller
  - 4 preset gamma curves (from gamma=1.0 to 2.5)
  - Line inversion, frame inversion
- NV Memory
  - 7-bits for ID2
  - 7-bits for VCOM adjustment

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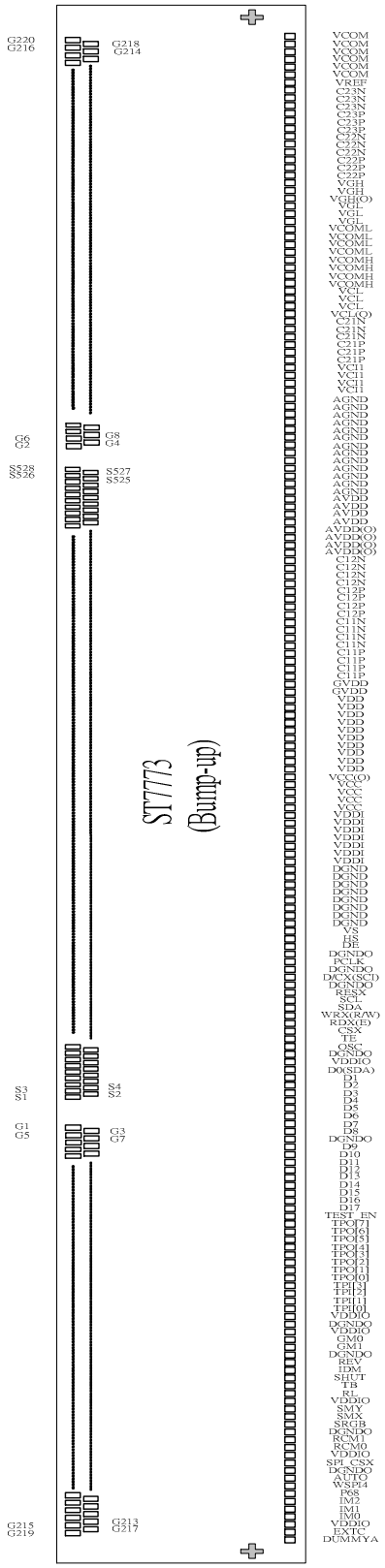
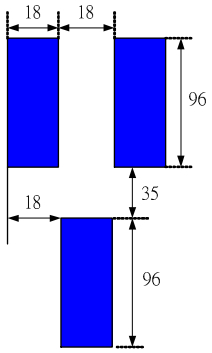
- Supply voltage range
  - Analog supply voltage range for VDD to AGND: 2.7V to 3.5V
  - I/O supply voltage range for VDDI to DGND: 1.6V to 3.6V
- Output voltage level
  - Source output voltage range (GVDD to AGND): 4.0V to 5.3V
  - Power supply range for driver circuit (AVDD to AGND): 4.8V to 5.3V
  - Output range of HIGH level of VCOM (VCOMH to AGND): 2.5V to 5.0V
  - Output range of LOW level of VCOM (VCOML to AGND): -2.5V to 0.0V
  - Output range of HIGH level of gate driver (VGH to AGND): +10.0V to 16.5V
  - Output range of LOW level of gate driver (VGL to AGND): -13.5V to –6V
- Lower power consumption, suitable for battery operated systems
  - CMOS compatible inputs
  - Optimized layout for COG assembly
  - Operate temperature range: -30℃ to +70℃

3. Pad arrangement

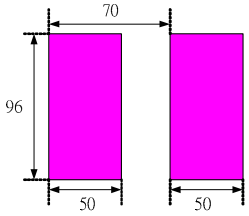


View point: bump view
Chip size (um): 17370x820
PAD coordinate: pad center
Coordinate origin: chip center
Chip thickness (um): 300±15
Bump height (um): 15±3
Bump hardness (HV): 75±25

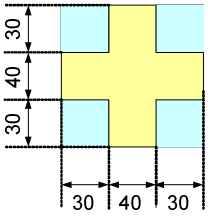
Pad arrangement (Unit: um):
Output: pad No. 1 ~ 751 = 18 x 96



Input: pad No. 752 ~ 947 = 50 x 96



Alignment mark (unit: um):
Left align mark (-8120.58, -300**)**
Left align mark (8080.6, -300**)**



Alignment mark

4. Pad Center Coordinates

PAD No.	PIN Name	X	Y
1	G220	7028	299
2	G218	7010	168
3	G216	6992	299
4	G214	6974	168
5	G212	6956	299
6	G210	6938	168
7	G208	6920	299
8	G206	6902	168
9	G204	6884	299
10	G202	6866	168
11	G200	6848	299
12	G198	6830	168
13	G196	6812	299
14	G194	6794	168
15	G192	6776	299
16	G190	6758	168
17	G188	6740	299
18	G186	6722	168
19	G184	6704	299
20	G182	6686	168
21	G180	6668	299
22	G178	6650	168
23	G176	6632	299
24	G174	6614	168
25	G172	6596	299
26	G170	6578	168
27	G168	6560	299
28	G166	6542	168
29	G164	6524	299
30	G162	6506	168
31	G160	6488	299
32	G158	6470	168
33	G156	6452	299
34	G154	6434	168
35	G152	6416	299
36	G150	6398	168
37	G148	6380	299
38	G146	6362	168
39	G144	6344	299
40	G142	6326	168

PAD No.	PIN Name	X	Y
41	G140	6308	299
42	G138	6290	168
43	G136	6272	299
44	G134	6254	168
45	G132	6236	299
46	G130	6218	168
47	G128	6200	299
48	G126	6182	168
49	G124	6164	299
50	G122	6146	168
51	G120	6128	299
52	G118	6110	168
53	G116	6092	299
54	G114	6074	168
55	G112	6056	299
56	DUMMYA	6038	168
57	G110	6020	299
58	G108	6002	168
59	G106	5984	299
60	G104	5966	168
61	G102	5948	299
62	G100	5930	168
63	G98	5912	299
64	G96	5894	168
65	G94	5876	299
66	G92	5858	168
67	G90	5840	299
68	G88	5822	168
69	G86	5804	299
70	G84	5786	168
71	G82	5768	299
72	G80	5750	168
73	G78	5732	299
74	G76	5714	168
75	G74	5696	299
76	G72	5678	168
77	G70	5660	299
78	G68	5642	168
79	G66	5624	299
80	G64	5606	168

PAD No.	PIN Name	X	Y
81	G62	5588	299
82	G60	5570	168
83	G58	5552	299
84	G56	5534	168
85	G54	5516	299
86	G52	5498	168
87	G50	5480	299
88	G48	5462	168
89	G46	5444	299
90	G44	5426	168
91	G42	5408	299
92	G40	5390	168
93	G38	5372	299
94	G36	5354	168
95	G34	5336	299
96	G32	5318	168
97	G30	5300	299
98	G28	5282	168
99	G26	5264	299
100	G24	5246	168
101	G22	5228	299
102	G20	5210	168
103	G18	5192	299
104	G16	5174	168
105	G14	5156	299
106	G12	5138	168
107	G10	5120	299
108	G8	5102	168
109	G6	5084	299
110	G4	5066	168
111	G2	5048	299
112	S528	4437	299
113	S527	4419	168
114	S526	4401	299
115	S525	4383	168
116	S524	4365	299
117	S523	4347	168
118	S522	4329	299
119	S521	4311	168
120	S520	4293	299

PAD No.	PIN Name	X	Y
121	S519	4275	168
122	S518	4257	299
123	S517	4239	168
124	S516	4221	299
125	S515	4203	168
126	S514	4185	299
127	S513	4167	168
128	S512	4149	299
129	S511	4131	168
130	S510	4113	299
131	S509	4095	168
132	S508	4077	299
133	S507	4059	168
134	S506	4041	299
135	S505	4023	168
136	S504	4005	299
137	S503	3987	168
138	S502	3969	299
139	S501	3951	168
140	S500	3933	299
141	S499	3915	168
142	S498	3897	299
143	S497	3879	168
144	S496	3861	299
145	S495	3843	168
146	S494	3825	299
147	S493	3807	168
148	S492	3789	299
149	S491	3771	168
150	S490	3753	299
151	S489	3735	168
152	S488	3717	299
153	S487	3699	168
154	S486	3681	299
155	S485	3663	168
156	S484	3645	299
157	S483	3627	168
158	S482	3609	299
159	S481	3591	168
160	S480	3573	299

PAD No.	PIN Name	X	Y
161	S479	3555	168
162	S478	3537	299
163	S477	3519	168
164	S476	3501	299
165	S475	3483	168
166	S474	3465	299
167	S473	3447	168
168	S472	3429	299
169	S471	3411	168
170	S470	3393	299
171	S469	3375	168
172	S468	3357	299
173	S467	3339	168
174	S466	3321	299
175	S465	3303	168
176	S464	3285	299
177	S463	3267	168
178	S462	3249	299
179	S461	3231	168
180	S460	3213	299
181	S459	3195	168
182	S458	3177	299
183	S457	3159	168
184	S456	3141	299
185	S455	3123	168
186	S454	3105	299
187	S453	3087	168
188	S452	3069	299
189	S451	3051	168
190	S450	3033	299
191	S449	3015	168
192	S448	2997	299
193	S447	2979	168
194	S446	2961	299
195	S445	2943	168
196	S444	2925	299
197	S443	2907	168
198	S442	2889	299
199	S441	2871	168
200	S440	2853	299

PAD No.	PIN Name	X	Y
201	S439	2835	168
202	S438	2817	299
203	S437	2799	168
204	S436	2781	299
205	S435	2763	168
206	S434	2745	299
207	S433	2727	168
208	S432	2709	299
209	S431	2691	168
210	S430	2673	299
211	S429	2655	168
212	S428	2637	299
213	S427	2619	168
214	S426	2601	299
215	S425	2583	168
216	S424	2565	299
217	S423	2547	168
218	S422	2529	299
219	S421	2511	168
220	S420	2493	299
221	S419	2475	168
222	S418	2457	299
223	S417	2439	168
224	S416	2421	299
225	S415	2403	168
226	S414	2385	299
227	S413	2367	168
228	S412	2349	299
229	S411	2331	168
230	S410	2313	299
231	S409	2295	168
232	S408	2277	299
233	S407	2259	168
234	S406	2241	299
235	S405	2223	168
236	S404	2205	299
237	S403	2187	168
238	S402	2169	299
239	S401	2151	168
240	S400	2133	299

PAD No.	PIN Name	X	Y
241	S399	2115	168
242	S398	2097	299
243	S397	2079	168
244	S396	2061	299
245	S395	2043	168
246	S394	2025	299
247	S393	2007	168
248	S392	1989	299
249	S391	1971	168
250	S390	1953	299
251	S389	1935	168
252	S388	1917	299
253	S387	1899	168
254	S386	1881	299
255	S385	1863	168
256	S384	1845	299
257	S383	1827	168
258	S382	1809	299
259	S381	1791	168
260	S380	1773	299
261	S379	1755	168
262	S378	1737	299
263	S377	1719	168
264	S376	1701	299
265	S375	1683	168
266	S374	1665	299
267	S373	1647	168
268	S372	1629	299
269	S371	1611	168
270	S370	1593	299
271	S369	1575	168
272	S368	1557	299
273	S367	1539	168
274	S366	1521	299
275	S365	1503	168
276	S364	1485	299
277	S363	1467	168
278	S362	1449	299
279	S361	1431	168
280	S360	1413	299

PAD No.	PIN Name	X	Y
281	S359	1395	168
282	S358	1377	299
283	S357	1359	168
284	S356	1341	299
285	S355	1323	168
286	S354	1305	299
287	S353	1287	168
288	S352	1269	299
289	S351	1251	168
290	S350	1233	299
291	S349	1215	168
292	S348	1197	299
293	S347	1179	168
294	S346	1161	299
295	S345	1143	168
296	S344	1125	299
297	S343	1107	168
298	S342	1089	299
299	S341	1071	168
300	S340	1053	299
301	S339	1035	168
302	S338	1017	299
303	S337	999	168
304	S336	981	299
305	S335	963	168
306	S334	945	299
307	S333	927	168
308	S332	909	299
309	S331	891	168
310	S330	873	299
311	S329	855	168
312	S328	837	299
313	S327	819	168
314	S326	801	299
315	S325	783	168
316	S324	765	299
317	S323	747	168
318	S322	729	299
319	S321	711	168
320	S320	693	299

PAD No.	PIN Name	X	Y
321	S319	675	168
322	S318	657	299
323	S317	639	168
324	S316	621	299
325	S315	603	168
326	S314	585	299
327	S313	567	168
328	S312	549	299
329	S311	531	168
330	S310	513	299
331	S309	495	168
332	S308	477	299
333	S307	459	168
334	S306	441	299
335	S305	423	168
336	S304	405	299
337	S303	387	168
338	S302	369	299
339	S301	351	168
340	S300	333	299
341	S299	315	168
342	S298	297	299
343	S297	279	168
344	S296	261	299
345	S295	243	168
346	S294	225	299
347	S293	207	168
348	S292	189	299
349	S291	171	168
350	S290	153	299
351	S289	135	168
352	S288	117	299
353	S287	99	168
354	S286	81	299
355	S285	63	168
356	S284	45	299
357	S283	27	168
358	S282	9	299
359	S281	-9	168
360	S280	-27	299

PAD No.	PIN Name	X	Y
361	S279	-45	168
362	S278	-63	299
363	S277	-81	168
364	S276	-99	299
365	S275	-117	168
366	S274	-135	299
367	S273	-153	168
368	S272	-171	299
369	S271	-189	168
370	S270	-207	299
371	S269	-225	168
372	S268	-243	299
373	S267	-261	168
374	S266	-279	299
375	S265	-297	168
376	DUMMYA	-315	299
377	S264	-333	168
378	S263	-351	299
379	S262	-369	168
380	S261	-387	299
381	S260	-405	168
382	S259	-423	299
383	S258	-441	168
384	S257	-459	299
385	S256	-477	168
386	S255	-495	299
387	S254	-513	168
388	S253	-531	299
389	S252	-549	168
390	S251	-567	299
391	S250	-585	168
392	S249	-603	299
393	S248	-621	168
394	S247	-639	299
395	S246	-657	168
396	S245	-675	299
397	S244	-693	168
398	S243	-711	299
399	S242	-729	168
400	S241	-747	299

PAD No.	PIN Name	X	Y	S2	PAD No.	PIN Name	X	Y
401	S240	-765	168		441	S200	-1485	168
402	S239	-783	299		442	S199	-1503	299
403	S238	-801	168		443	S198	-1521	168
404	S237	-819	299		444	S197	-1539	299
405	S236	-837	168		445	S196	-1557	168
406	S235	-855	299		446	S195	-1575	299
407	S234	-873	168		447	S194	-1593	168
408	S233	-891	299		448	S193	-1611	299
409	S232	-909	168		449	S192	-1629	168
410	S231	-927	299		450	S191	-1647	299
411	S230	-945	168		451	S190	-1665	168
412	S229	-963	299		452	S189	-1683	299
413	S228	-981	168		453	S188	-1701	168
414	S227	-999	299		454	S187	-1719	299
415	S226	-1017	168		455	S186	-1737	168
416	S225	-1035	299		456	S185	-1755	299
417	S224	-1053	168		457	S184	-1773	168
418	S223	-1071	299		458	S183	-1791	299
419	S222	-1089	168		459	S182	-1809	168
420	S221	-1107	299		460	S181	-1827	299
421	S220	-1125	168		461	S180	-1845	168
422	S219	-1143	299		462	S179	-1863	299
423	S218	-1161	168		463	S178	-1881	168
424	S217	-1179	299		464	S177	-1899	299
425	S216	-1197	168		465	S176	-1917	168
426	S215	-1215	299		466	S175	-1935	299
427	S214	-1233	168		467	S174	-1953	168
428	S213	-1251	299		468	S173	-1971	299
429	S212	-1269	168		469	S172	-1989	168
430	S211	-1287	299		470	S171	-2007	299
431	S210	-1305	168		471	S170	-2025	168
432	S209	-1323	299		472	S169	-2043	299
433	S208	-1341	168		473	S168	-2061	168
434	S207	-1359	299		474	S167	-2079	299
435	S206	-1377	168		475	S166	-2097	168
436	S205	-1395	299		476	S165	-2115	299
437	S204	-1413	168		477	S164	-2133	168
438	S203	-1431	299		478	S163	-2151	299
439	S202	-1449	168		479	S162	-2169	168
440	S201	-1467	299		480	S161	-2187	299

PAD No.	PIN Name	X	Y
481	S160	-2205	168
482	S159	-2223	299
483	S158	-2241	168
484	S157	-2259	299
485	S156	-2277	168
486	S155	-2295	299
487	S154	-2313	168
488	S153	-2331	299
489	S152	-2349	168
490	S151	-2367	299
491	S150	-2385	168
492	S149	-2403	299
493	S148	-2421	168
494	S147	-2439	299
495	S146	-2457	168
496	S145	-2475	299
497	S144	-2493	168
498	S143	-2511	299
499	S142	-2529	168
500	S141	-2547	299
501	S140	-2565	168
502	S139	-2583	299
503	S138	-2601	168
504	S137	-2619	299
505	S136	-2637	168
506	S135	-2655	299
507	S134	-2673	168
508	S133	-2691	299
509	S132	-2709	168
510	S131	-2727	299
511	S130	-2745	168
512	S129	-2763	299
513	S128	-2781	168
514	S127	-2799	299
515	S126	-2817	168
516	S125	-2835	299
517	S124	-2853	168
518	S123	-2871	299
519	S122	-2889	168
520	S121	-2907	299

PAD No.	PIN Name	X	Y
521	S120	-2925	168
522	S119	-2943	299
523	S118	-2961	168
524	S117	-2979	299
525	S116	-2997	168
526	S115	-3015	299
527	S114	-3033	168
528	S113	-3051	299
529	S112	-3069	168
530	S111	-3087	299
531	S110	-3105	168
532	S109	-3123	299
533	S108	-3141	168
534	S107	-3159	299
535	S106	-3177	168
536	S105	-3195	299
537	S104	-3213	168
538	S103	-3231	299
539	S102	-3249	168
540	S101	-3267	299
541	S100	-3285	168
542	S99	-3303	299
543	S98	-3321	168
544	S97	-3339	299
545	S96	-3357	168
546	S95	-3375	299
547	S94	-3393	168
548	S93	-3411	299
549	S92	-3429	168
550	S91	-3447	299
551	S90	-3465	168
552	S89	-3483	299
553	S88	-3501	168
554	S87	-3519	299
555	S86	-3537	168
556	S85	-3555	299
557	S84	-3573	168
558	S83	-3591	299
559	S82	-3609	168
560	S81	-3627	299

PAD No.	PIN Name	X	Y
561	S80	-3645	168
562	S79	-3663	299
563	S78	-3681	168
564	S77	-3699	299
565	S76	-3717	168
566	S75	-3735	299
567	S74	-3753	168
568	S73	-3771	299
569	S72	-3789	168
570	S71	-3807	299
571	S70	-3825	168
572	S69	-3843	299
573	S68	-3861	168
574	S67	-3879	299
575	S66	-3897	168
576	S65	-3915	299
577	S64	-3933	168
578	S63	-3951	299
579	S62	-3969	168
580	S61	-3987	299
581	S60	-4005	168
582	S59	-4023	299
583	S58	-4041	168
584	S57	-4059	299
585	S56	-4077	168
586	S55	-4095	299
587	S54	-4113	168
588	S53	-4131	299
589	S52	-4149	168
590	S51	-4167	299
591	S50	-4185	168
592	S49	-4203	299
593	S48	-4221	168
594	S47	-4239	299
595	S46	-4257	168
596	S45	-4275	299
597	S44	-4293	168
598	S43	-4311	299
599	S42	-4329	168
600	S41	-4347	299

PAD No.	PIN Name	X	Y
601	S40	-4365	168
602	S39	-4383	299
603	S38	-4401	168
604	S37	-4419	299
605	S36	-4437	168
606	S35	-4455	299
607	S34	-4473	168
608	S33	-4491	299
609	S32	-4509	168
610	S31	-4527	299
611	S30	-4545	168
612	S29	-4563	299
613	S28	-4581	168
614	S27	-4599	299
615	S26	-4617	168
616	S25	-4635	299
617	S24	-4653	168
618	S23	-4671	299
619	S22	-4689	168
620	S21	-4707	299
621	S20	-4725	168
622	S19	-4743	299
623	S18	-4761	168
624	S17	-4779	299
625	S16	-4797	168
626	S15	-4815	299
627	S14	-4833	168
628	S13	-4851	299
629	S12	-4869	168
630	S11	-4887	299
631	S10	-4905	168
632	S9	-4923	299
633	S8	-4941	168
634	S7	-4959	299
635	S6	-4977	168
636	S5	-4995	299
637	S4	-5013	168
638	S3	-5031	299
639	S2	-5049	168
640	S1	-5067	299

PAD No.	PIN Name	X	Y
641	G1	-5678	299
642	G3	-5696	168
643	G5	-5714	299
644	G7	-5732	168
645	G9	-5750	299
646	G11	-5768	168
647	G13	-5786	299
648	G15	-5804	168
649	G17	-5822	299
650	G19	-5840	168
651	G21	-5858	299
652	G23	-5876	168
653	G25	-5894	299
654	G27	-5912	168
655	G29	-5930	299
656	G31	-5948	168
657	G33	-5966	299
658	G35	-5984	168
659	G37	-6002	299
660	G39	-6020	168
661	G41	-6038	299
662	G43	-6056	168
663	G45	-6074	299
664	G47	-6092	168
665	G49	-6110	299
666	G51	-6128	168
667	G53	-6146	299
668	G55	-6164	168
669	G57	-6182	299
670	G59	-6200	168
671	G61	-6218	299
672	G63	-6236	168
673	G65	-6254	299
674	G67	-6272	168
675	G69	-6290	299
676	G71	-6308	168
677	G73	-6326	299
678	G75	-6344	168
679	G77	-6362	299
680	G79	-6380	168

PAD No.	PIN Name	X	Y
681	G81	-6398	299
682	G83	-6416	168
683	G85	-6434	299
684	G87	-6452	168
685	G89	-6470	299
686	G91	-6488	168
687	G93	-6506	299
688	G95	-6524	168
689	G97	-6542	299
690	G99	-6560	168
691	G101	-6578	299
692	G103	-6596	168
693	G105	-6614	299
694	G107	-6632	168
695	G109	-6650	299
696	DUMMYA	-6668	168
697	G111	-6686	299
698	G113	-6704	168
699	G115	-6722	299
700	G117	-6740	168
701	G119	-6758	299
702	G121	-6776	168
703	G123	-6794	299
704	G125	-6812	168
705	G127	-6830	299
706	G129	-6848	168
707	G131	-6866	299
708	G133	-6884	168
709	G135	-6902	299
710	G137	-6920	168
711	G139	-6938	299
712	G141	-6956	168
713	G143	-6974	299
714	G145	-6992	168
715	G147	-7010	299
716	G149	-7028	168
717	G151	-7046	299
718	G153	-7064	168
719	G155	-7082	299
720	G157	-7100	168

PAD No.	PIN Name	X	Y
721	G159	-7118	299
722	G161	-7136	168
723	G163	-7154	299
724	G165	-7172	168
725	G167	-7190	299
726	G169	-7208	168
727	G171	-7226	299
728	G173	-7244	168
729	G175	-7262	299
730	G177	-7280	168
731	G179	-7298	299
732	G181	-7316	168
733	G183	-7334	299
734	G185	-7352	168
735	G187	-7370	299
736	G189	-7388	168
737	G191	-7406	299
738	G193	-7424	168
739	G195	-7442	299
740	G197	-7460	168
741	G199	-7478	299
742	G201	-7496	168
743	G203	-7514	299
744	G205	-7532	168
745	G207	-7550	299
746	G209	-7568	168
747	G211	-7586	299
748	G213	-7604	168
749	G215	-7622	299
750	G217	-7640	168
751	G219	-7658	299
752	DUMMYA	-8028.58	-299
753	EXTC	-7958.58	-299
754	VDDIO	-7888.58	-299
755	IM0	-7818.58	-299
756	IM1	-7748.58	-299
757	IM2	-7678.58	-299
758	P68	-7608.58	-299
759	WSPI4	-7538.58	-299
760	AUTO	-7468.58	-299

PAD No.	PIN Name	X	Y
761	DGNDO	-7398.58	-299
762	SPI_CSX	-7328.58	-299
763	VDDIO	-7258.58	-299
764	RCM0	-7188.58	-299
765	RCM1	-7118.58	-299
766	DGNDO	-7048.58	-299
767	SRGB	-6978.58	-299
768	SMX	-6908.58	-299
769	SMY	-6838.58	-299
770	VDDIO	-6768.58	-299
771	RL	-6698.58	-299
772	TB	-6628.58	-299
773	SHUT	-6558.58	-299
774	IDM	-6488.58	-299
775	REV	-6418.58	-299
776	DGNDO	-6348.58	-299
777	GM1	-6278.58	-299
778	GM0	-6208.58	-299
779	VDDIO	-6138.58	-299
780	DGNDO	-6068.58	-299
781	VDDIO	-5998.58	-299
782	TPI[0]	-5928.58	-299
783	TPI[1]	-5858.58	-299
784	TPI[2]	-5788.58	-299
785	TPI[3]	-5718.58	-299
786	TPO[0]	-5648.58	-299
787	TPO[1]	-5578.58	-299
788	TPO[2]	-5508.58	-299
789	TPO[3]	-5438.58	-299
790	TPO[4]	-5368.58	-299
791	TPO[5]	-5298.58	-299
792	TPO[6]	-5228.58	-299
793	TPO[7]	-5158.58	-299
794	TEST_EN	-5088.58	-299
795	D17	-5018.58	-299
796	D16	-4948.58	-299
797	D15	-4878.58	-299
798	D14	-4808.58	-299
799	D13	-4738.58	-299
800	D12	-4668.58	-299

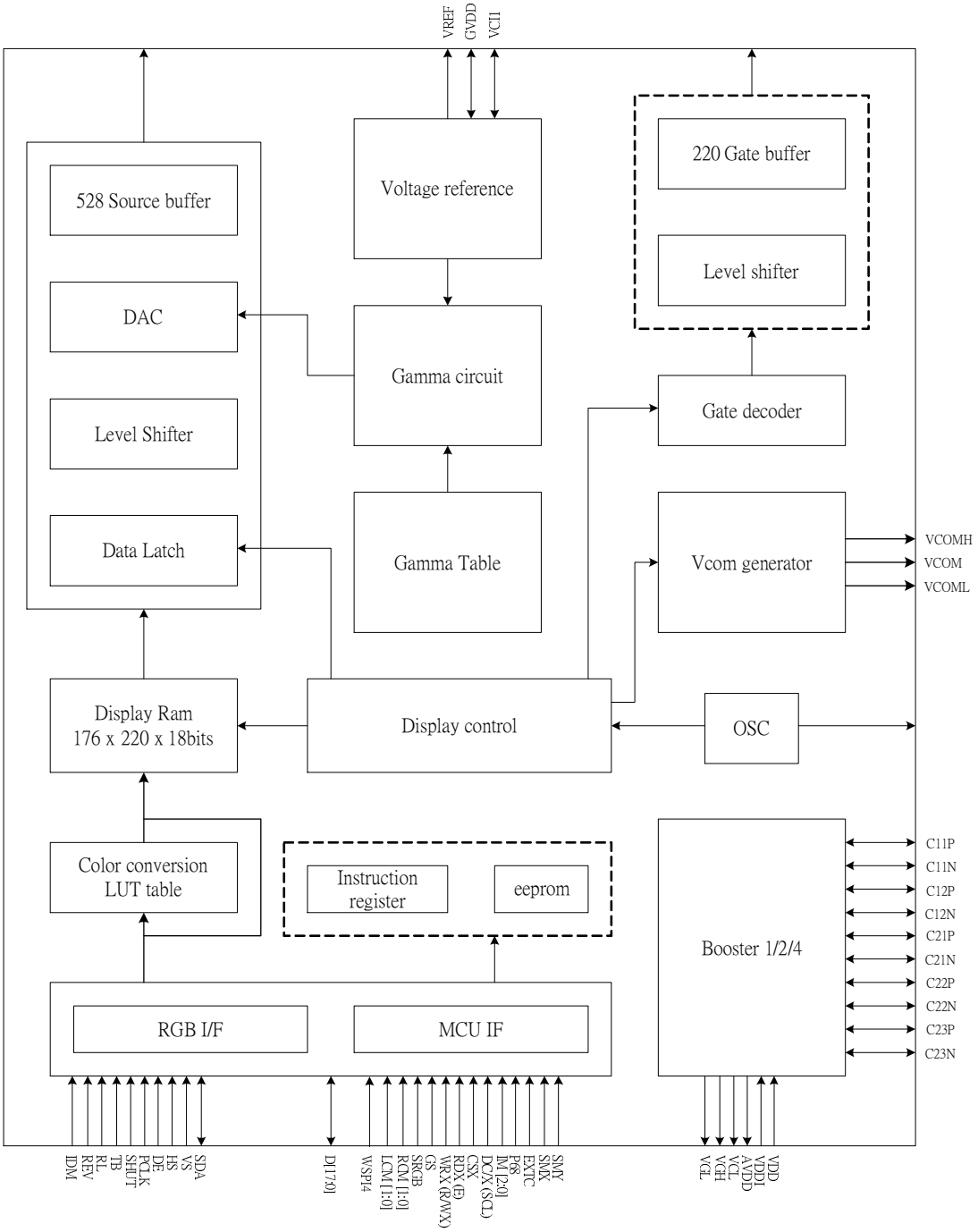
PAD No.	PIN Name	X	Y
801	D11	-4598.58	-299
802	D10	-4528.58	-299
803	D9	-4458.58	-299
804	DGNDO	-4388.58	-299
805	D8	-4318.58	-299
806	D7	-4248.58	-299
807	D6	-4178.58	-299
808	D5	-4108.58	-299
809	D4	-4038.58	-299
810	D3	-3968.58	-299
811	D2	-3898.58	-299
812	D1	-3828.58	-299
813	D0(SDA)	-3758.58	-299
814	VDDIO	-3688.58	-299
815	DGNDO	-3618.58	-299
816	OSCP	-3548.58	-299
817	TEP	-3478.58	-299
818	CSX	-3408.58	-299
819	RDX(E)	-3338.58	-299
820	WRX(R/Wx)	-3268.58	-299
821	SDA	-3198.58	-299
822	SCL	-3128.58	-299
823	RESX	-3058.58	-299
824	DGNDO	-2988.58	-299
825	D/CX(SCI)	-2918.58	-299
826	DGNDO	-2848.58	-299
827	PCLK	-2778.58	-299
828	DGNDO	-2708.58	-299
829	DE	-2638.58	-299
830	HS	-2568.58	-299
831	VS	-2498.58	-299
832	DGND	-2428.58	-299
833	DGND	-2358.58	-299
834	DGND	-2288.58	-299
835	DGND	-2218.58	-299
836	DGND	-2148.58	-299
837	DGND	-2078.58	-299
838	DGND	-2008.58	-299
839	DGND	-1938.58	-299
840	VDDI	-1868.58	-299

PAD No.	PIN Name	X	Y
841	VDDI	-1798.58	-299
842	VDDI	-1728.58	-299
843	VDDI	-1658.58	-299
844	VDDI	-1588.58	-299
845	VDDI	-1518.58	-299
846	VDDI	-1448.58	-299
847	VCC	-673.45	-299
848	VCC	-603.45	-299
849	VCC	-533.45	-299
850	VCC	-463.45	-299
851	VCCO	-393.45	-299
852	VDD	88.26	-299
853	VDD	158.26	-299
854	VDD	228.26	-299
855	VDD	298.26	-299
856	VDD	368.26	-299
857	VDD	438.26	-299
858	VDD	508.26	-299
859	VDD	578.26	-299
860	VDD	648.26	-299
861	VDD	718.26	-299
862	GVDD	788.26	-299
863	GVDD	858.26	-299
864	C11P	2232.71	-299
865	C11P	2302.71	-299
866	C11P	2372.71	-299
867	C11P	2442.71	-299
868	C11N	2512.71	-299
869	C11N	2582.71	-299
870	C11N	2652.71	-299
871	C11N	2722.71	-299
872	C12P	2792.71	-299
873	C12P	2862.71	-299
874	C12P	2932.71	-299
875	C12P	3002.71	-299
876	C12N	3072.71	-299
877	C12N	3142.71	-299
878	C12N	3212.71	-299
879	C12N	3282.71	-299
880	AVDDO	3352.71	-299

PAD No.	PIN Name	X	Y
881	AVDDO	3422.71	-299
882	AVDDO	3492.71	-299
883	AVDDO	3562.71	-299
884	AVDD	3632.71	-299
885	AVDD	3702.71	-299
886	AVDD	3772.71	-299
887	AVDD	3842.71	-299
888	AGND	3912.71	-299
889	AGND	3982.71	-299
890	AGND	4052.71	-299
891	AGND	4122.71	-299
892	AGND	4192.71	-299
893	AGND	4262.71	-299
894	AGND	4332.71	-299
895	AGND	4402.71	-299
896	AGND	4472.71	-299
897	AGND	4542.71	-299
898	AGND	4612.71	-299
899	AGND	4682.71	-299
900	AGND	4752.71	-299
901	VCI1	4822.71	-299
902	VCI1	4892.71	-299
903	VCI1	4962.71	-299
904	VCI1	5032.71	-299
905	C21P	5102.71	-299
906	C21P	5172.71	-299
907	C21P	5242.71	-299
908	C21N	5312.71	-299
909	C21N	5382.71	-299
910	C21N	5452.71	-299
911	VCLO	5522.71	-299
912	VCL	5592.71	-299
913	VCL	5662.71	-299
914	VCL	5732.71	-299
915	VCOMH	5802.71	-299
916	VCOMH	5872.71	-299
917	VCOMH	5942.71	-299
918	VCOMH	6012.71	-299
919	VCOML	6082.71	-299
920	VCOML	6152.71	-299

PAD No.	PIN Name	X	Y
921	VCOML	6222.71	-299
922	VCOML	6292.71	-299
923	VGL	6362.71	-299
924	VGL	6432.71	-299
925	VGL	6502.71	-299
926	VGHO	6572.71	-299
927	VGH	6642.71	-299
928	VGH	6712.71	-299
929	C22P	6782.71	-299
930	C22P	6852.71	-299
931	C22P	6922.71	-299
932	C22N	6992.71	-299
933	C22N	7062.71	-299
934	C22N	7132.71	-299
935	C23P	7202.71	-299
936	C23P	7272.71	-299
937	C23P	7342.71	-299
938	C23N	7412.71	-299
939	C23N	7482.71	-299
940	C23N	7552.71	-299
941	VREF	8172.06	-299
942	VCOM	8242.06	-299
943	VCOM	8312.06	-299
944	VCOM	8382.06	-299
945	VCOM	8452.06	-299
946	VCOM	8522.06	-299
947	VCOM	8592.06	-299

5. Block diagram



6. Pin description

6.1 Power supply pin

Name	I/O	Description	Count	Connect pin
VDD	I	Power supply for analog, digital system and booster circuit.		VDD
VDDI	I	Power supply for I/O system.		VDDI
AGND	I	System ground for analog system and booster circuit.		GND
DGND	I	System ground for I/O system and digital system.		GND

6.2 Interface logic pin

Name	I/O	Description	Count	Connect pin
P68	I	-8080/6800 MCU interface mode select. -P68='1', select 6800 MCU parallel interface. -P68='0', select 8080 MCU parallel interface. -If not used, please connect this pin to VDDI or DGND level.	1	DGND/VDDI
IM0~IM2	I	-Selection for MCU parallel interface or serial interface. -If not used, please connect this pin to VDDI or DGND.	3	DGND/VDDI
WSPI4	I	-When in serial interface, this pin can be used to choose 3-line or 4-line SPI. -If not used, please fix this pin to DGND.	1	DGND/VDDI
RESX	I	-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.	1	MCU
CSX	I	-Chip selection pin ("Low" is enable). -This pin can be permanently fixed "Low" in MCU interface mode only.	1	MCU
D/CX (SCI)	I	-Display data/command selection pin in MCU interface. -D/CX='1': display data or parameter. -D/CX='0': command data. -In serial interface, this is used as SCL. -If not used, please connect this pin to VDDI or DGND.	1	MCU
RDX (E)	I	-Read enable in 8080 MCU parallel interface. -Read/write operation enable pin in 6800 MCU parallel interface. -If not used, please connect this pin to VDDI or DGND.	1	MCU
WRX (R/W)	I	-Write enable in MCU parallel interface. -In 4-line serial interface, this pin is used as D/CX (data/ command selection). -If not used, please connect this pin to VDDI or DGND.	1	MCU
SPI_CSX	I	-When RCM1, RCM0="01"(MCU interface2), this pin is used as serial input pin -When RCM1, RCM0='00' or '1X' , this pin is not used and please connect to VDDI or DGND level.	1	MCU DGND/VDDI
SCL	I	-When RCM1, RCM0="01"(MCU interface2), this pin is used as serial input pin -When RCM1, RCM0='00' or '1X' , this pin is not used and please connect to VDDI or DGND level.	1	MCU DGND/VDDI
SDA	I	-When RCM1, RCM0='1X' (RGB interface) or '01'(MCU interface2), this pin is used as serial input/output pin. -When RCM1, RCM0='00' (MCU interface), this pin is not used and please connect to VDDI or DGND level. The serial input/output pin in MCU interface mode is D0.	1	MCU DGND/VDDI
OSC	O	-Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command. -When this pin is inactive (function OFF), this pin is DGND level. -If not used, please open this pin.	1	-
D[17:0]	I/O	-When RCM="1" (RGB interface), D[17:0] are used as RGB interface data bus. -When RCM="0" (MCU interface), D[17:0] are used as MCU parallel interface data bus. -D0 is the serial input/output signal in serial interface mode. -In serial interface, D[17:1] are not used and should be connected to VDDI or DGND.	18	MCU
TE	O	-Tearing effect output pin to synchronies MCU to frame rate, activated by S/W command. -When this pin is inactive, this pin is DGND level. -If not used, please open this pin.	1	MCU
PCLK	I	-Pixel clock signal in RGB interface mode. -If not used, please fix this pin at VDDI or DGND.	1	RGB interface

VS	I	-Vertical sync. signal in RGB interface mode. -If not used, please fix this pin at VDDI or DGND.	1	RGB interface
HS	I	-Horizontal sync. signal in RGB interface mode. -If not used, please fix this pin at VDDI or DGND.	1	RGB interface
DE	I	-Data enable signal in RGB interface mode. -If not used, please fix this pin at VDDI or DGND.	1	RGB interface

Note1. If CSX is connected to ground in parallel interface mode, there will be no abnormal visible effect on the display module. Also there will be no restriction on using the parallel Read/Write protocols, power On/Off sequences or other functions. Furthermore, there will be no influence to the power consumption of the display module.

Note2. When in 8-line parallel mode (IM2, IM1, IM0 ="001") and if some data or signal appears on D[17:8], then it will have no influence to the system. (D[17:8] can be connected to"1" or "0")

Note3. When CSX="1", there is no influence to the parallel and serial interface.

Note4. "1" ="HIGH"= VDDI level, "0" ="LOW"= DGND level.

6.3 Mode selection pin

Name	I/O	Description	Count	Connect pin
EXTC	I	-To use extended command set, please connect this pin to VDDI. -During normal operation, please open this pin (internal $R_{pull\text{-}down}$=2MΩ). EXTC: Enable/disable modification of extend command 0: Only use default command set 1: Use extended command set	1	VDDI/DGND
IDM	I	-Normal mode and idle mode selection pin. IDM: Enable/disable idle mode 0: Normal display (can be changed to Idle mode by S/W) 1: Idle mode enable	1	VDDI/DGND
GM1, GM0	I	-Please connect to DGND	2	DGND
RCM1, RCM0	I	-RGB or MCU interface mode selection pins. RCM[1:0] / Selection of MCU or RGB interface 00 / 0: MCU Interface(1) 01 / 1: MCU Interface(2) 10 / 2: RGB Interface (1) 11 / 3: RGB Interface (2)	2	VDDI/DGND
SRGB	I	-RGB arrangement selection pin for color filter design. SRGB: RGB arrangement 0: S1, S2, S3 filter order = 'R', 'G', 'B' 1: S1, S2, S3 filter order = 'B', 'G', 'R'	1	VDDI/DGND
SMX	I	-Scanning direction of source output selection pin. SMX: Scanning direction of source output 0: S1->S528 1: S528->S1	1	VDDI/DGND
SMY	I	-Scanning direction of gate output selection pin. SMY: Scanning direction of gate output 0: G1->G220 1: G220->G1	1	VDDI/DGND
REV	I	-Polarity of source output selection pin. REV / Command / Polarity of source output 0 / INVON(21h) / Data reverse 0 / INVOFF(20h) / Data not reverse 1 / INVON(21h) / Data not reverse 1 / INVOFF(20h) / Data reverse	1	VDDI/DGND
SHUT	I	-Display On/Off control pin In RGB interface. SHUT: Display On/Off 0: Display On 1: Display Off	1	VDDI/DGND
RL	I	-Scanning direction of source output selection pin in RGB interface. RL / SMX / Scanning direction of source output 0 / 0: S1->S528 0 / 1: S528->S1 1 / 0: S528->S1 1 / 1: S1->S528	1	VDDI/DGND

<table>
<tr><td>TB</td><td>I</td><td>-Scanning direction of gate output selection pin in RGB interface.
<table>
<tr><th>TB</th><th>SMY</th><th>Scanning direction of gate output</th></tr>
<tr><td>0</td><td>0</td><td>G1->G220</td></tr>
<tr><td>0</td><td>1</td><td>G220->G1</td></tr>
<tr><td>1</td><td>0</td><td>G220->G1</td></tr>
<tr><td>1</td><td>1</td><td>G1->G220</td></tr>
</table></td><td>1</td><td>VDDI/DGND</td></tr>
<tr><td>AUTO</td><td>I</td><td>-Please connect this pin to VDDI.</td><td>1</td><td>VDDI</td></tr>
<tr><td>TEST_EN</td><td>I</td><td>-Enable/disable the test mode
<table>
<tr><th>TEST_EN</th><th>Test mode enable/disable</th></tr>
<tr><td>0</td><td>Not in TEST mode</td></tr>
<tr><td>1</td><td>In TEST mode</td></tr>
</table></td><td>1</td><td>VDDI/DGND</td></tr>
</table>

6.4 Driver output pin

Name	I/O	Description	Count	Connect pin
S1 to S528	O	- Source driver output pins.	528	-
G1 to G220	O	- Gate driver output pins.	220	-
VCI1	I/O	- A reference voltage for step-up circuit 1. - Connect a capacitor for stabilization.	4	Capacitor
AVDD	I	- Power input pin for analog circuits. - In normal usage, connect it to AVDDO.	4	AVDDO
AVDDO	O	- Output of step-up circuit 1 - Connect a capacitor for stabilization.	4	Capacitor
VCL	I	- Power input pin for VCOM circuit. - In normal usage, connect it to VCLO.	3	VCLO
VCLO	O	- A power output pin of step-up circuit 4. - When VCOML is higher than AGND, VCLO=AGND. - Connect a capacitor for stabilization.	1	Capacitor
VGH	I	- Power input pin for gate driver circuit. - In normal usage, connect it to VGHO.	2	VGHO
VGHO	O	- Positive output pin of the step-up circuit 2. - Connect a capacitor for stabilization.	1	Capacitor
VGL	I	- Power input pin for gate driver circuit. - Negative output of the step-up circuit 2 is connected inside the driver. - Connect a capacitor for stabilization.	3	VGLO
VREF	O	- A reference voltage for power system. - Connect a capacitor for stabilization.	1	Capacitor
GVDD	O	- A power output of grayscale voltage generator. - Connect a capacitor for stabilization. - When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin.	2	Capacitor
VCOMH	O	- Positive voltage output of VCOM. - Connect a capacitor for stabilization.	4	Capacitor
VCOML	O	- Negative voltage output of VCOM. - Connect a capacitor for stabilization.	4	Capacitor
VCOM	O	- A power supply for the TFT-LCD common electrode.	6	Common electrode
C11P, C11N C12P, C12N	O	- Capacitor connecting pins for step-up circuit 1 (for AVDDO)	16	Step-up Capacitor
C21P, C21N C22P, C22N C23P, C23N	O	- Capacitor connecting pins for step-up circuit 2 and 4 (for VGHO, VGLO, VCLO)	18	Step-up Capacitor
VDDIO	O	-VDDI voltage output level for monitoring.	6	-
DGNDO	O	-DGND voltage output level for monitoring.	9	-
VCCO	O	-Monitoring pin of internal digital reference voltage. -Connect a capacitor for stabilization.	5	Capacitor

6.5 Test pin

Name	I/O	Description	Count	Connect pin
TPI[3]~[0]	I	-Please open these pins.	4	DGND
TPO[7]~[0]	O	-Please open these pins.	8	Open
Dummy	-	-These pins are dummy (have no function inside). -Can allow signal traces pass through these pads on TFT glass.	4	Open

7. Driver electrical characteristics

7.1 Absolute operation range

Item	Symbol	Rating	Unit
Supply voltage	VDD	- 0.3 ~ +4.6	V
Supply voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Supply voltage (Digital)	VCC	-0.3 ~ +4.6	V
Driver supply voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic input voltage range	V_{IN}	0.3 ~ VDDI + 0.3	V
Logic output voltage range	V_O	0.3 ~ VDDI + 0.3	V
Operating temperature range	T_{OPR}	-40 ~ +85	℃
Storage temperature range	T_{STG}	-55 ~ +125	℃

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC characteristic

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			Min	TYP	Max		
Power & operation voltage							
System voltage	VDD	Operating voltage	2.7	2.8	3.5	V	
Interface operation voltage	VDDI	I/O supply voltage	1.6	1.8/2.8	3.6	V	
Digital operating voltage	VCC	Digital supply voltage	1.6		1.8	V	
Gate driver high voltage	VGH		10		16.5	V	
Gate driver low voltage	VGL		-13.5		-5.5	V	
Gate driver supply voltage		| VGH-VGL |	15.5		30.0	V	
Input / Output							
Logic-high input voltage	V_{IH}		0.7VDDI		VDDI	V	Note 1
Logic-low input voltage	V_{IL}		VSS		0.3VDDI	V	Note 1
Logic-high output voltage	V_{OH}	I_{OH} = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-low output voltage	V_{OL}	I_{OL} = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-high input current	I_{IH}	VIN = VDDI			1	uA	Note 1
Logic-low input current	I_{IL}	VIN = VSS	-1			uA	Note 1
Input leakage current	I_{IL}	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM voltage							
VCOM high voltage	VCOMH	Ccom=22nF	2.5		5.0	V	
VCOM low voltage	VCOML	Ccom=22nF	-2.5		0.0	V	
VCOM amplitude	VCOMAC	|VCOMH-VCOML|	4.0		6.0	V	
Source driver							
Source output range	Vsout		0.1		AVDD-0.1	V	
Gamma reference voltage	GVDD		3.0		5.0	V	
Source output settling time	Tr	Below with 99% precision		25	30	us	Note 2
Output deviation voltage (Source output channel)	Vdev	Sout >=4.2V, Sout<=0.8V			20	mV	Note 2
		4.2V>Sout>0.8V			15	mV	
Output offset voltage	V_{OFSET}				35	mV	Note 3
Step-up circuit							
Internal reference voltage	V_{REF}		0		1	%	
1st step-up voltage	AVDD		5.0		5.3	V	Note 4,5
1st step-up (VDDx2) drop voltage	VDDx2,dorp	I AVDD = 1.0mA (include panel loading)			5%	%	
Linear range	V_{Linear}		0.2		AVDD-0.2	V	

Note 1: VDDI=1.6 to 3.5V, VDD=2.7 to 3.5V, AGND=DGND=0V, T_A=-30 to 70 ℃
Note 2, Source channel loading= 10pF/channel, Gate channel loading=50pF/channel.
Note 3, The Max. value is between measured point of note 4 and gamma setting value.
Note 4, VDD=2.7V
Note 5, VDD=3.5V

7.3 Power consumption

Operation mode	Inversion mode	Image	Current consumption			
			Typical		Maximum	
			IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
-Normal mode	One Line	Note 1	0.01	2.5	0.01	2.8
	One Line	Note 2	0.01	2.2	0.01	2.4
-Partial + Idle mode (40 lines)	Frame	Note 3	0.01	0.5	0.01	0.6
-Sleep-in mode	N/A	N/A	8uA	2uA	15uA	5uA

Notes:
1. All pixels black.
2. Grayscale from top to bottom.
3. Black & white checker board 8 by 8.

8. Timing chart

8.1 Parallel interface characteristics: 18, 16, 9 or 8-bits bus (8080-series MCU interface)

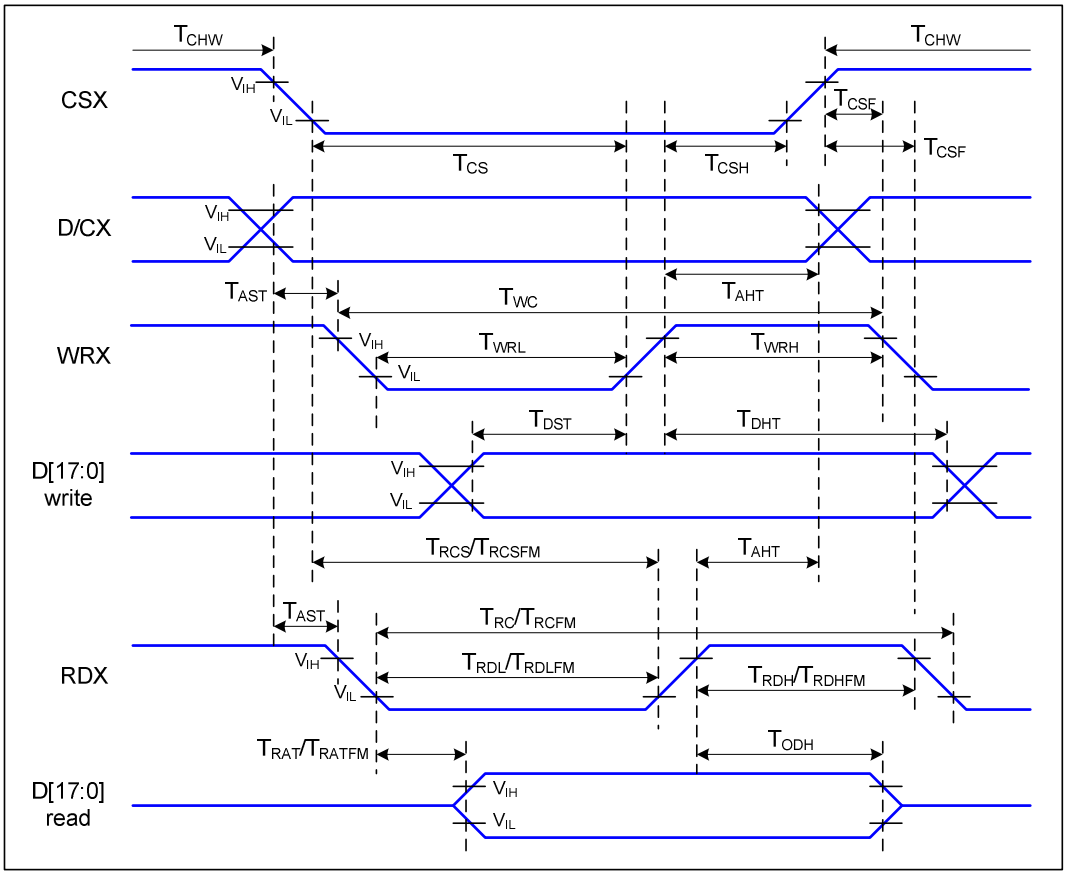


Fig. 8.1.1 Parallel interface timing characteristics (8080-series MCU interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-(3-transfer for one pixel)
	T_{CS}	Chip select setup time (Write)	30		ns	
	T_{RCS}	Chip select setup time (Read ID)	35		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	320		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	100		ns	10MHz
	T_{WRH}	Control pulse "H" duration	20		ns	
	T_{WRL}	Control pulse "L" duration	20		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Note 1: VDDI=1.6 to 3.6V, VDD=2.7 to 3.5V, AGND=DGND=0V, Ta=-30 to 70 ℃

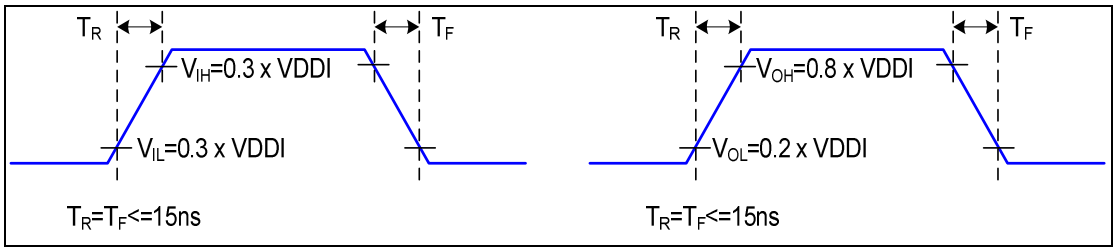


Fig. 8.1.2 Rising and falling timing for input and output signal

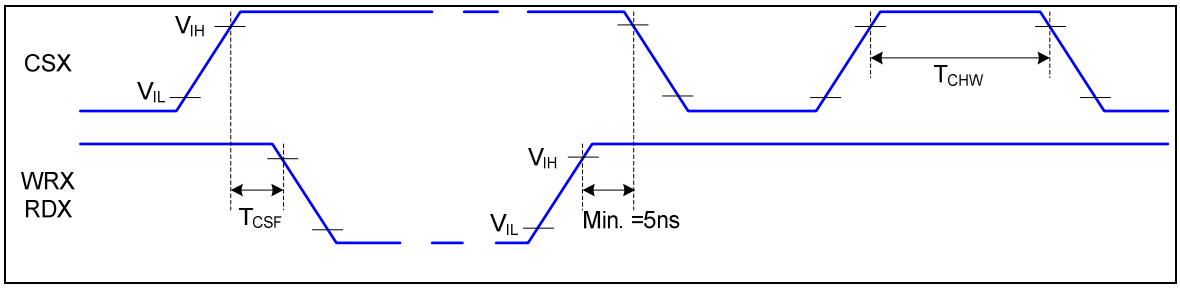


Fig.8.1.3 Chip selection (CSX) timing

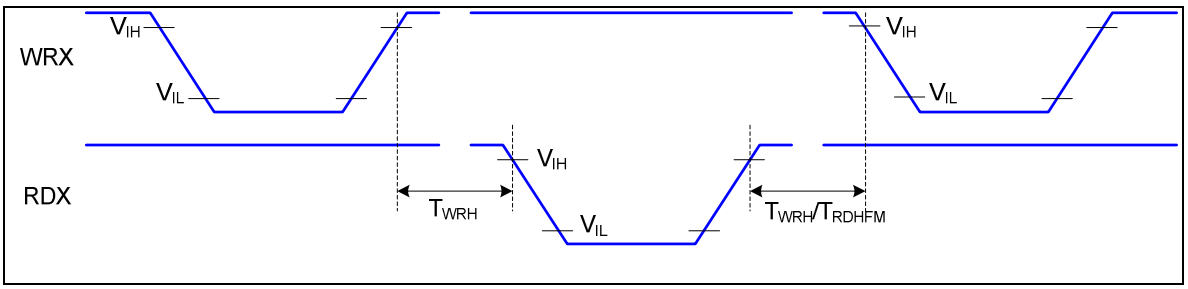


Fig. 8.1.4 Write-to-read and read-to-write timing

NOTE: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.2 Parallel interface characteristics: 18, 16, 9 or 8-bits bus (6800-series MCU interface)

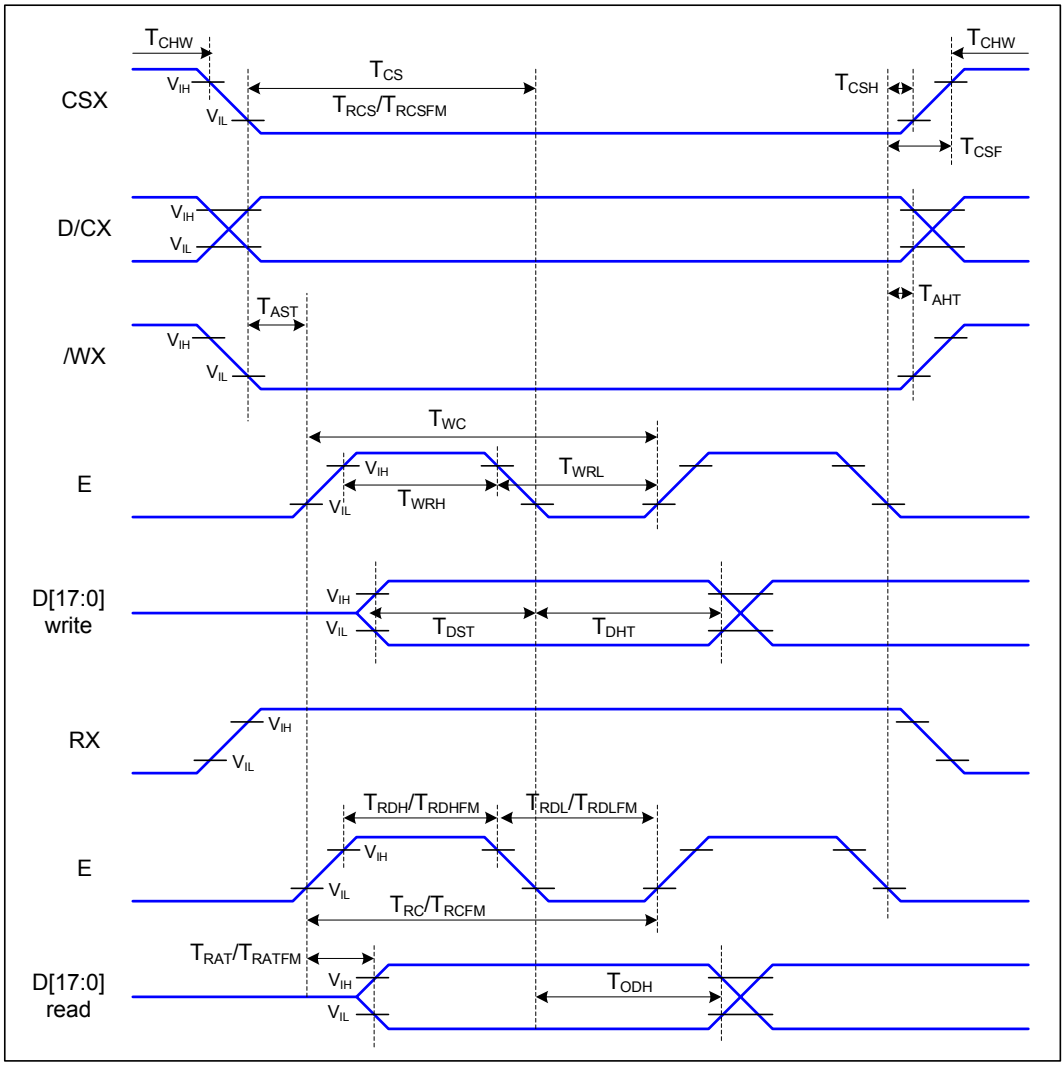


Fig. 8.2.1 Parallel interface timing characteristics (6800-series MCU interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	30		ns	
	T_{RCS}	Chip select setup time (Read ID)	35		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	320		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	100		ns	10MHz
	T_{WRH}	Control pulse "H" duration	20		ns	
	T_{WRL}	Control pulse "L" duration	20		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Note 1: VDDI=1.6 to 3.6V, VDD=2.7 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃

Note 2: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.3 Serial interface characteristics (3-line serial)

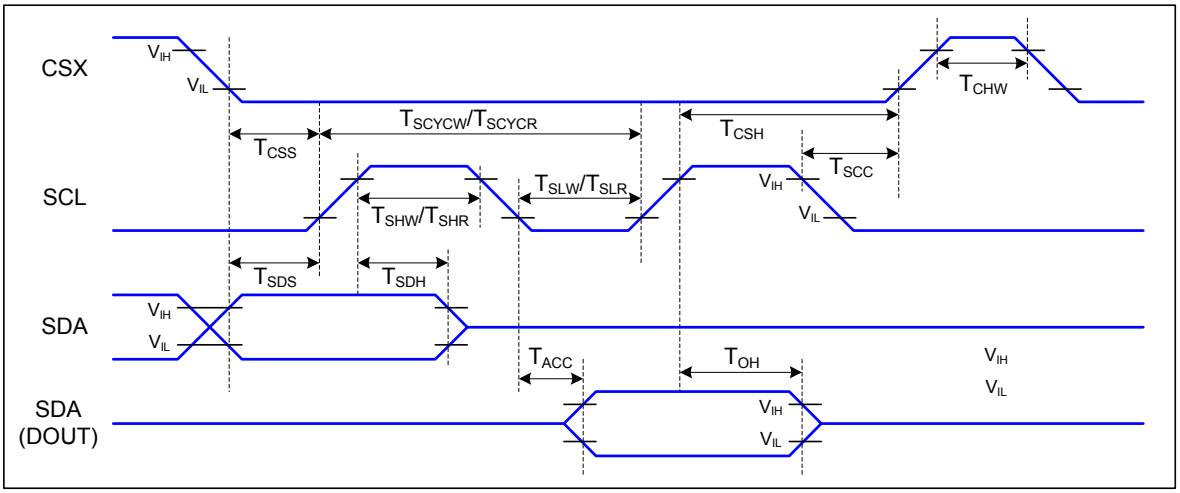


Fig. 8.3.1 3-line serial interface timing

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time	60		ns	
	T_{CSH}	Chip select hold time	60		ns	
	T_{SCC}	Chip select setup time	20		ns	
	T_{CHW}	Chip select setup time	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	65		ns	
	T_{SHW}	SCL “H” pulse width (Write)	20		ns	
	T_{SLW}	SCL “L” pulse width (Write)	20		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN) (DOUT)	T_{SDS}	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	T_{SDH}	Data hold time	10		ns	
	T_{ACC}	Access time	15		ns	
	T_{OH}	Output disable time	20		ns	

Table 8.3: 3-line Serial Interface Characteristics

Note 1: VDDI=1.6 to 3.6V, VDD=2.7 to 3.5V, AGND=DGND=0V, Ta=-30 to 70℃
Note 2: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.4 Serial interface characteristics (4-line serial)

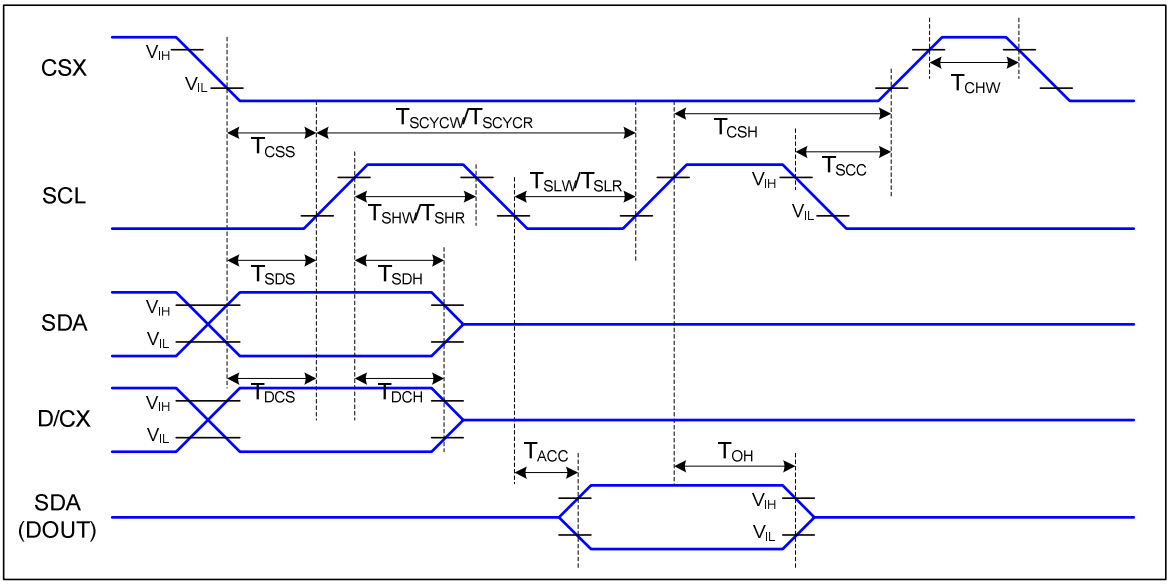


Fig. 8.4.1 4-line serial interface timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	60		ns	
	T_{CSH}	Chip select hold time	60		ns	
	T_{SCC}	Chip select setup time	20		ns	
	T_{CHW}	Chip select setup time	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	65		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	20		ns	
	T_{SLW}	SCL "L" pulse width (Write)	20		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		Ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN) (DOUT)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
	T_{ACC}	Access time	15		ns	For maximum CL=30pF
	T_{OH}	Output disable time	20		ns	For minimum CL=8pF

Table 8.4: 4-line Serial Interface Characteristics

Note 1: VDDI=1.6 to 3.6V, VDD=2.7 to 3.5V, AGND=DGND=0V, Ta=-30 to 70 ℃

Note 2: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

9. Function description

9.1 Interface type selection

The selection of given interfaces are done by setting P68, IM2, IM1, and IM0 pins as shown in following table.

Table 9.1.1 Selection of MCU interface

P68	IM2	IM1	IM0	Interface	Read back selection
-	0	-	-	3/4-line serial interface	Via the read instruction
0	1	0	0	8080 MCU 8-bit parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	1	0	1	8080 MCU 16-bit parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	1	1	0	8080 MCU 9-bit parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	1	1	1	8080 MCU 18-bit parallel	RDX strobe (18-bit read data and 8-bit read parameter)
-	0	-	-	3/4-line serial interface	Via the read instruction
1	1	0	0	6800 MCU 8-bit parallel	E strobe (8-bit read data and 8-bit read parameter)
1	1	0	1	6800 MCU 16-bit parallel	E strobe (16-bit read data and 8-bit read parameter)
1	1	1	0	6800 MCU 9-bit parallel	E strobe (9-bit read data and 8-bit read parameter)
1	1	1	1	6800 MCU 18-bit parallel	E strobe (18-bit read data and 8-bit read parameter)

Table 9.1.2 Pin connection according to various MCU interface 1

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
-	0	-	-	3-line serial interface	Note1	Note1	SCL	D[17:1]: unused, D0: SDA
				4-line serial interface		D/CX	SCL	D[17:1]: unused, D0: SDA
0	1	0	0	8080 8-bit parallel	RDX	WRX	D/CX	D[17:8]: unused, D7-D0: 8-bit data
0	1	0	1	8080 16-bit parallel	RDX	WRX	D/CX	D[17:16]: unused, D15-D0: 16-bit data
0	1	1	0	8080 9-bit parallel	RDX	WRX	D/CX	D[17:9]: unused, D8-D0: 9-bit data
0	1	1	1	8080 18-bit parallel	RDX	WRX	D/CX	D17-D0: 18-bit data
-	0	-	-	3-line serial interface	Note1	Note1	SCL	D[17:1]: unused, D0: SDA
				4-line serial interface		D/CX	SCL	D[17:1]: unused, D0: SDA
1	1	0	0	6800 8-bit parallel	E	R/WX	D/CX	D[17:8]: unused, D7-D0: 8-bit data
1	1	0	1	6800 16-bit parallel	E	R/WX	D/CX	D[17:16]: unused, D15-D0: 16-bit data
1	1	1	0	6800 9-bit parallel	E	R/WX	D/CX	D[17:9]: unused, D8-D0: 9-bit data
1	1	1	1	6800 18-bit parallel	E	R/WX	D/CX	D17-D0: 18-bit data

Table 9.1.3 Pin connection according to various MCU interface 2

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
-	0	-	-	3-line serial interface	Note1	Note1	Note1	D[17:0] : unused, SPI_CSX, SDA, SCL
				4-line serial interface		D/CX		D[17:0] : unused, SPI_CSX, SDA, SCL
0	1	0	0	8080 8-bit parallel	RDX	WRX	D/CX	D[17:8]:unused, D7-D0: 8-bit data
0	1	0	1	8080 16-bit parallel	RDX	WRX	D/CX	D[17:16]: unused, D15-D0: 16-bit data
0	1	1	0	8080 9-bit parallel	RDX	WRX	D/CX	D[17:9]: unused, D8-D0: 9-bit data
0	1	1	1	8080 18-bit parallel	RDX	WRX	D/CX	D17-D0: 18-bit data
-	0	-	-	3-line serial interface	Note1	Note1	Note1	D[17:0] : unused, SPI_CSX, SDA, SCL
				4-line serial interface		D/CX		D[17:0] : unused, SPI_CSX, SDA, SCL
1	1	0	0	6800 8-bit parallel	E	R/WX	D/CX	D[17:8]: unused, D7-D0: 8-bit data
1	1	0	1	6800 16-bit parallel	E	R/WX	D/CX	D[17:16]: unused, D15-D0: 16-bit data
1	1	1	0	6800 9-bit parallel	E	R/WX	D/CX	D[17:9]: unused, D8-D0: 9-bit data
1	1	1	1	6800 18-bit parallel	E	R/WX	D/CX	D17-D0: 18-bit data

Note 1. Unused pins can be open, or connected to DGND or VDDI.

9.2 8080-series MCU parallel interface (P68='0')

The MCU can use one of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-line with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver. The selection of this interface is done when P68 pin is in low state (DGND). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 8080-series parallel interface are given in following table.

Table 9.2.1 The function of 8080-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read back selection
0	1	0	0	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	↑	1	Read 8-bit display data (D7 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	0	1	16-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	↑	1	Read 16-bit display data (D15 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	1	0	9-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	↑	1	Read 9-bit display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	1	1	18-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	↑	1	Read 18-bit display data (D17 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh

9.2.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low ('0') and vice versa it is data ('1').

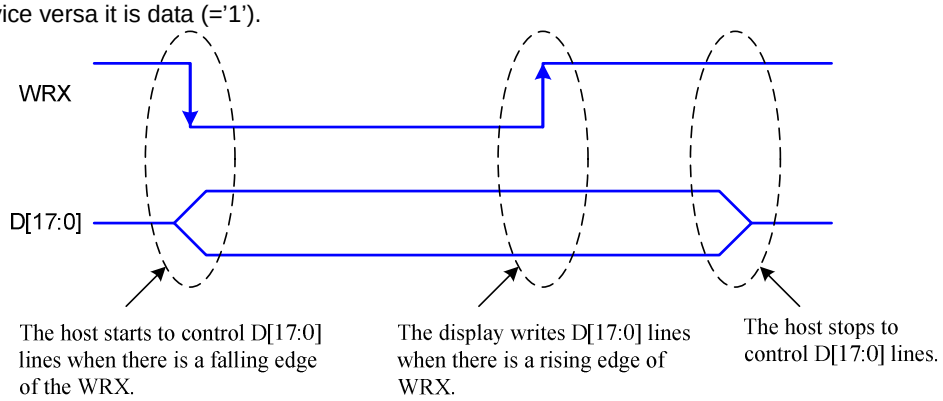


Fig. 9.2.1 8080-series WRX protocol

Note: WRX is an unsynchronized signal (It can be stopped).

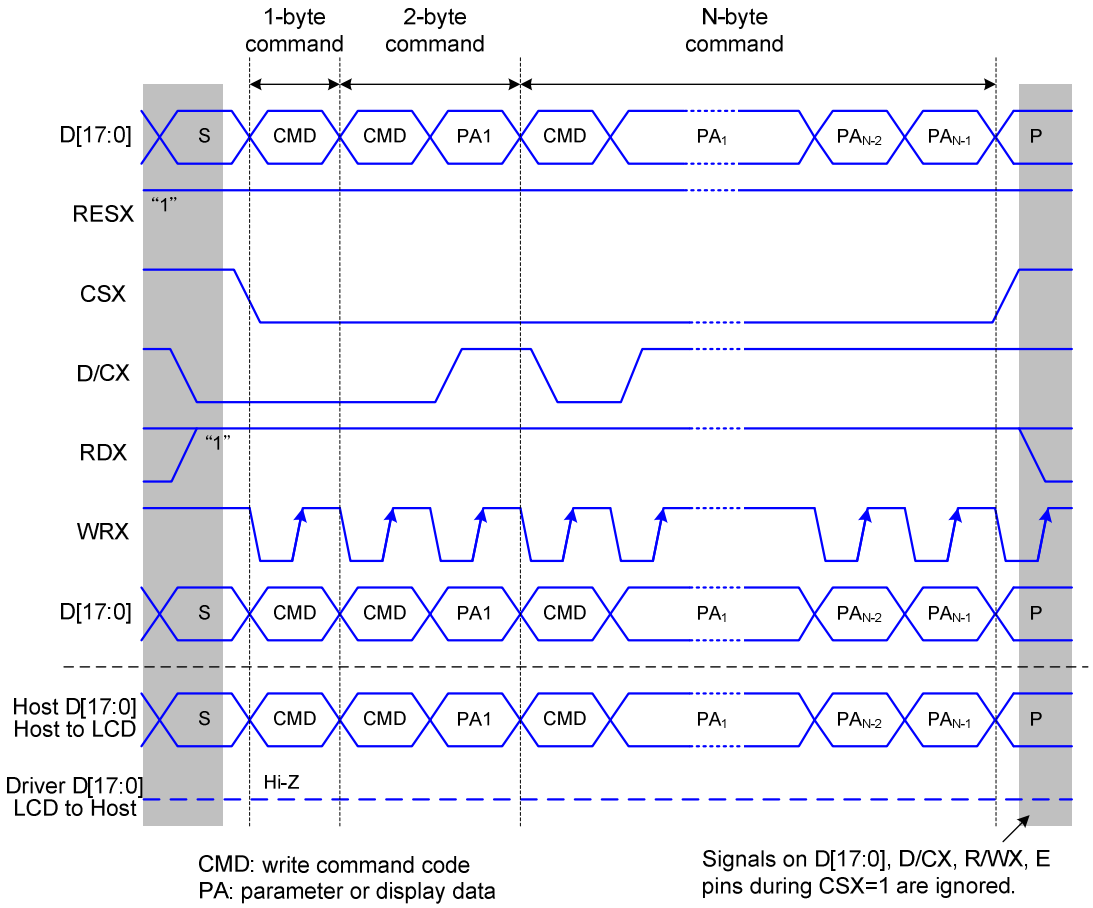


Fig. 9.2.2 8080-series parallel bus protocol, write to register or display RAM

9.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

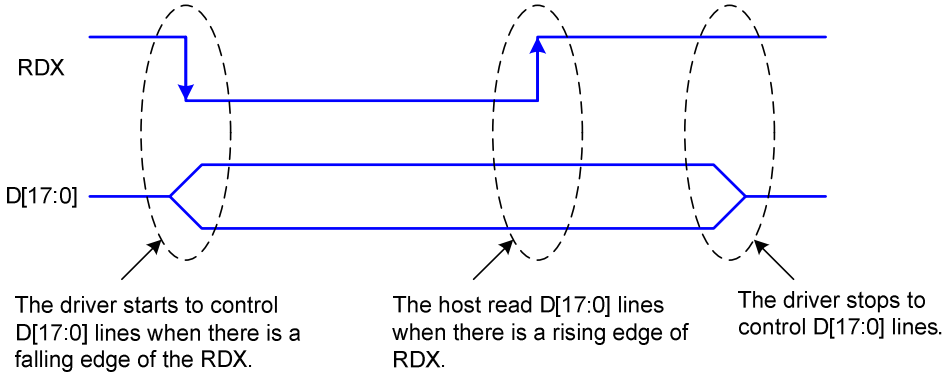


Fig. 9.2.3 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

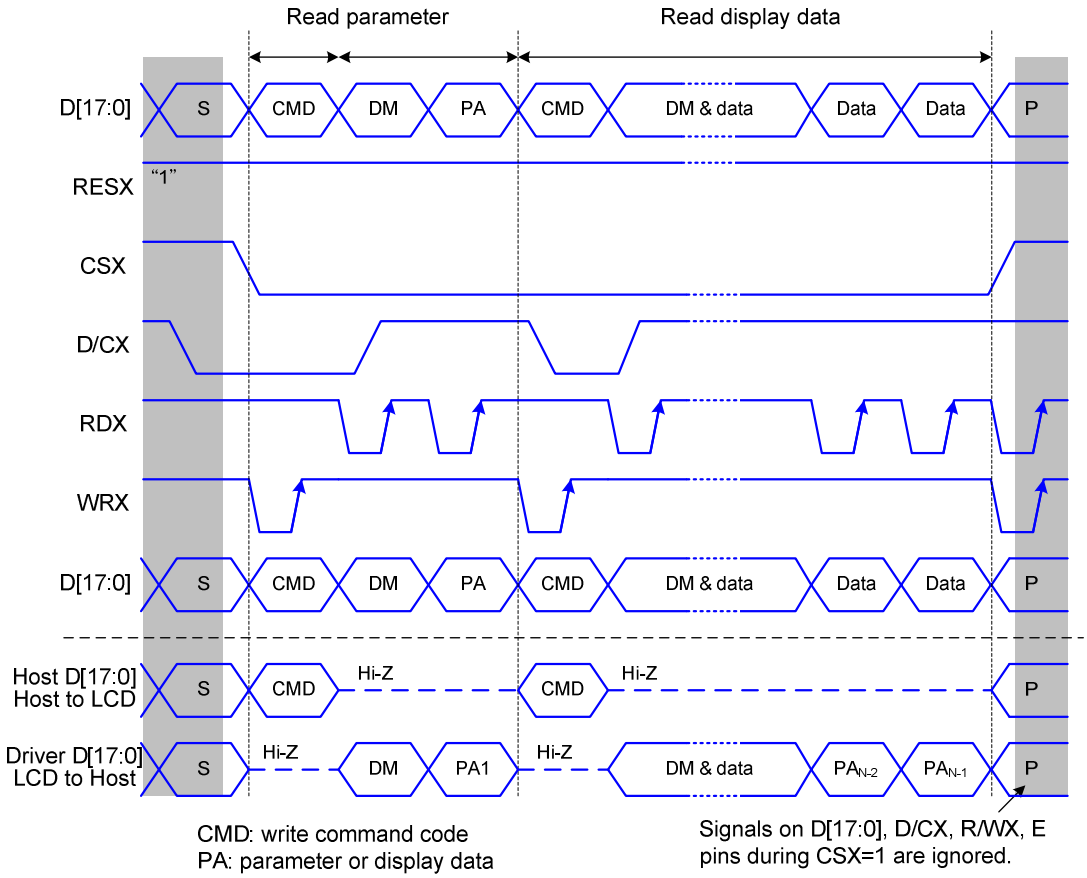


Fig. 9.2.4 8080-series parallel bus protocol, read data from register or display RAM

9.3 6800-Series Parallel Interface (P68='1')

The MCU uses one of following interface: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-lines with 16-data parallel interface, or 21-lines with 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data bus.

The LCD driver reads the data at the falling edge of E signal when R/WX= '1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C= '0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 6800-series parallel interface are given in Table 9.3.1.

Table 9.3.1 The function of 6800-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	1	↓	Read 8-bit Display data (D7 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	0	1	16-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	1	↓	Read 16-bit Display data (D15 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	0	9-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	1	↓	Read 9-bit Display data (D8 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)
1	1	1	1	18-bit Parallel	0	0	↓	Write 8-bit command (D7 to D0)
					1	0	↓	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	1	↓	Read 18-bit Display data (D17 to D0)
					1	1	↓	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

9.3.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control signals (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

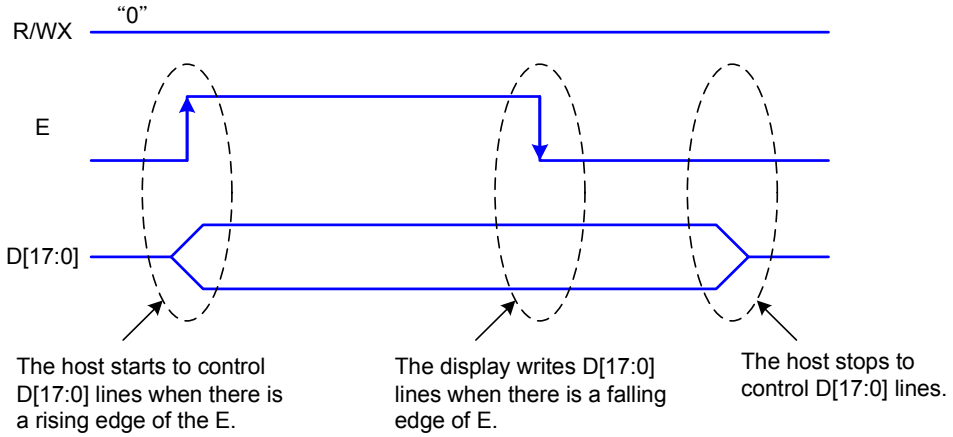


Fig. 9.3.1 6800-Series Write Protocol

Note: E is an unsynchronized signal (It can be stopped)

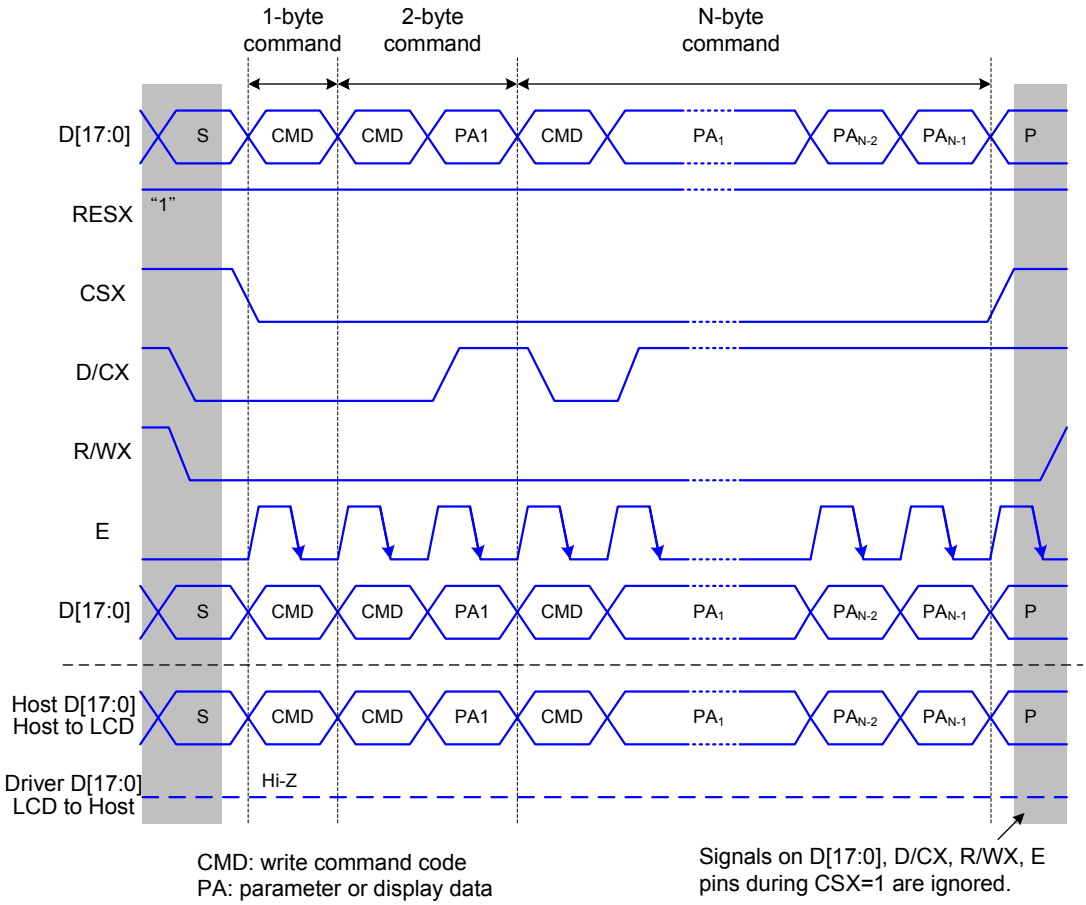


Fig. 9.3.2 6800-series parallel bus protocol, write to register or display RAM

9.3.2 Read cycle sequence

The read cycle (E low-high-low sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a rising edge of E and the host reads data when there is a falling edge of E.

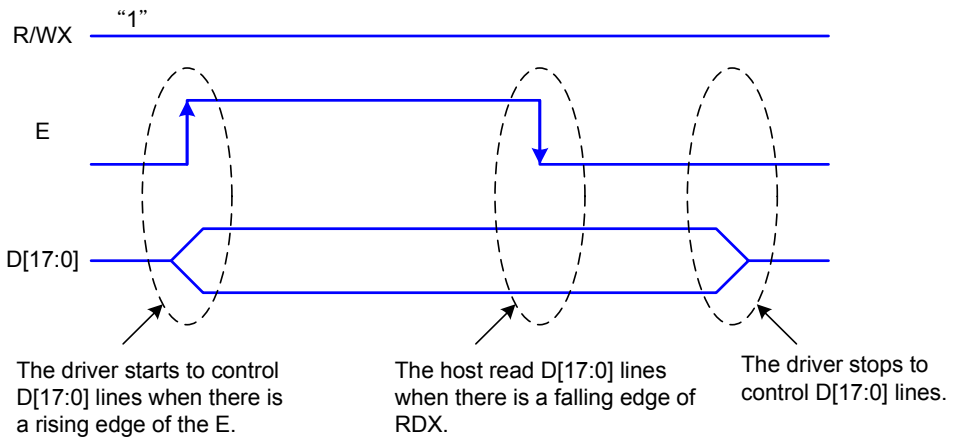


Fig. 9.3.3 6800-series read protocol

Note: E is an unsynchronized signal (It can be stopped)

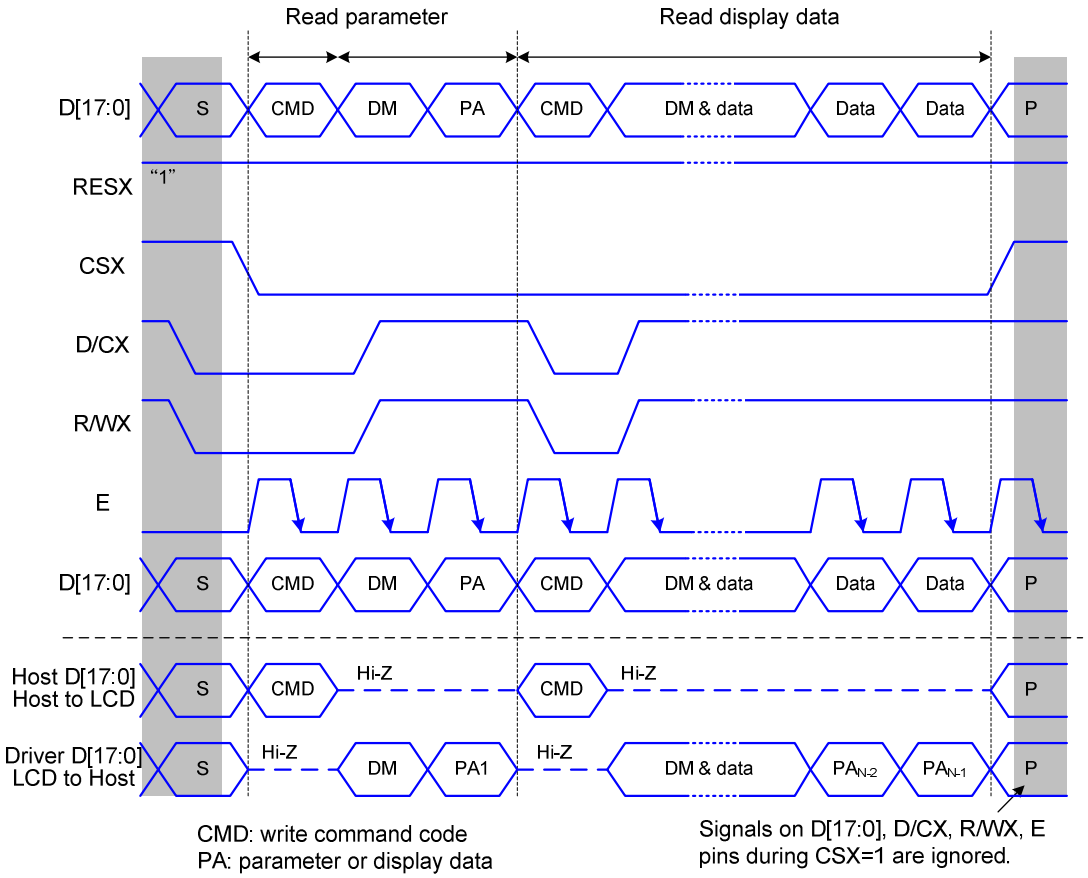


Fig. 9.3.4 6800-series parallel bus protocol, read data form register or display RAM

9.4 Serial interface

The selection of this interface is done by IM2. See the Table 9.4.1.

Table 9.4.1 Selection of serial interface

IM2	4WSPI	Interface	Read back selection
0	0	3-line serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	1	4-line serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)

The serial interface is either 3-lines/9-bits or 4-lines/8-bts bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

9.4.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

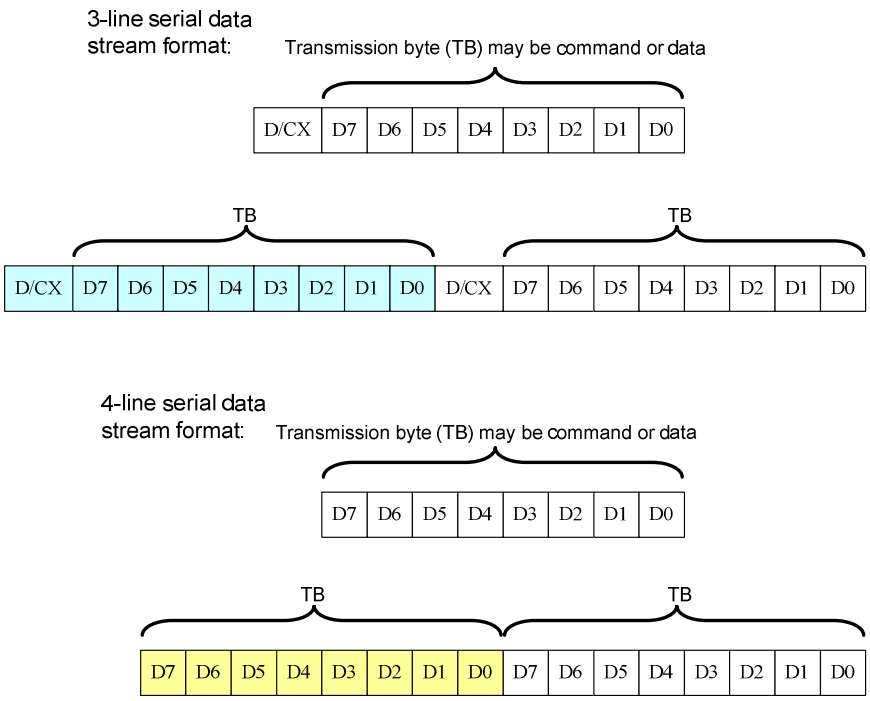


Fig. 9.4.1 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Fig 9.4.2). SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-lines serial interface) or 8th rising edge of SCL (4-lines serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-lines serial interface) or D7 (4-lines serial interface) of the next byte at the next rising edge of SCL.

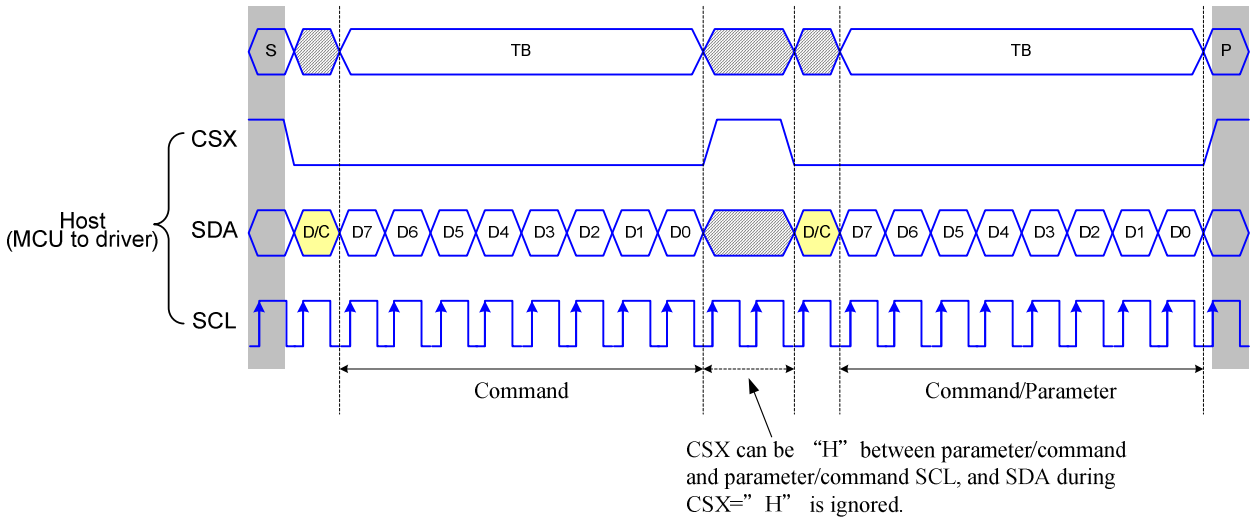


Fig. 9.4.2 3-line serial interface write protocol (write to register with control bit in transmission)

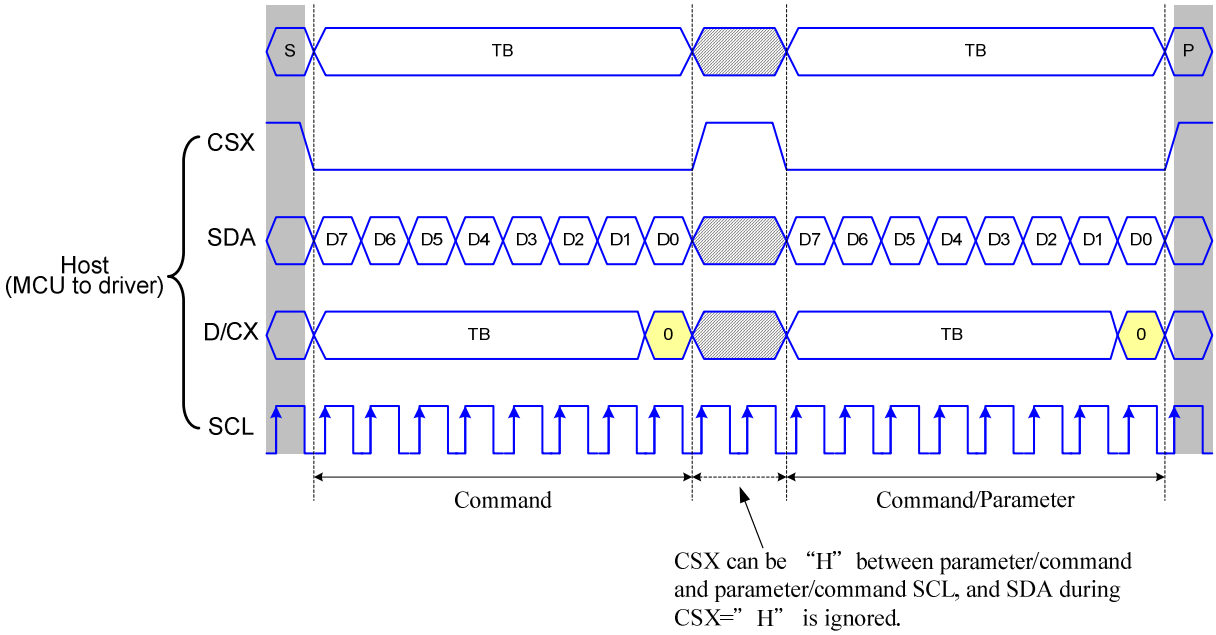


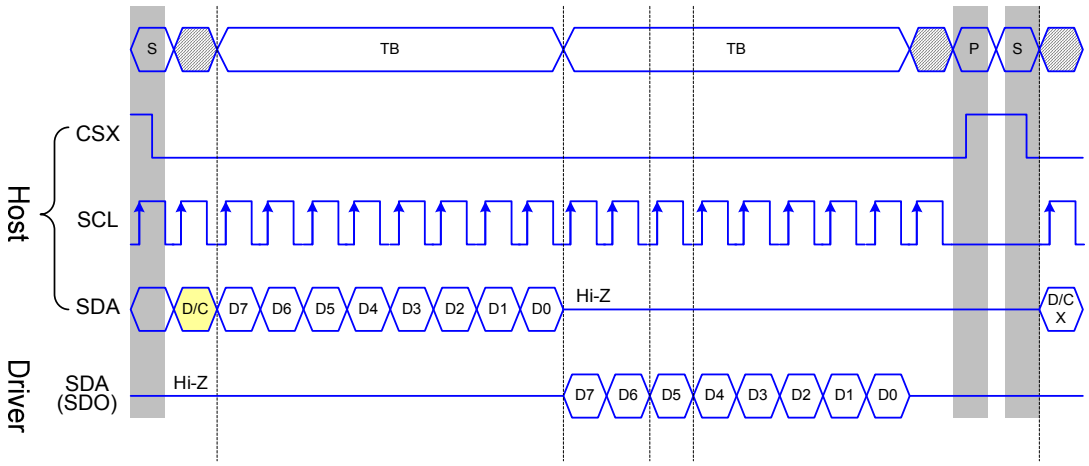
Fig. 9.4.3 4-line serial interface write protocol (write to register with control bit in transmission)

9.4.2 Read Functions

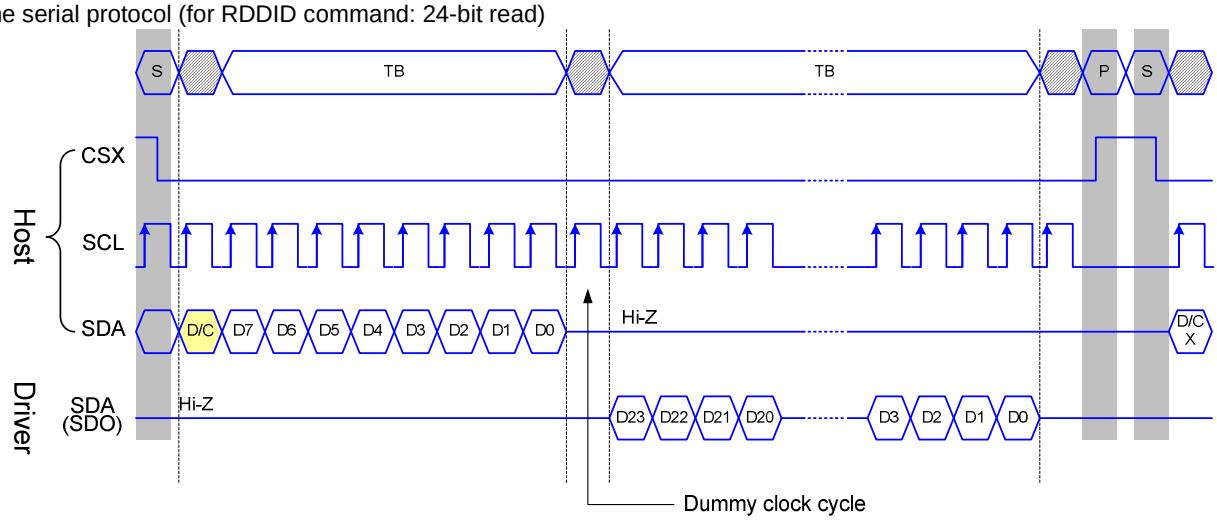
The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

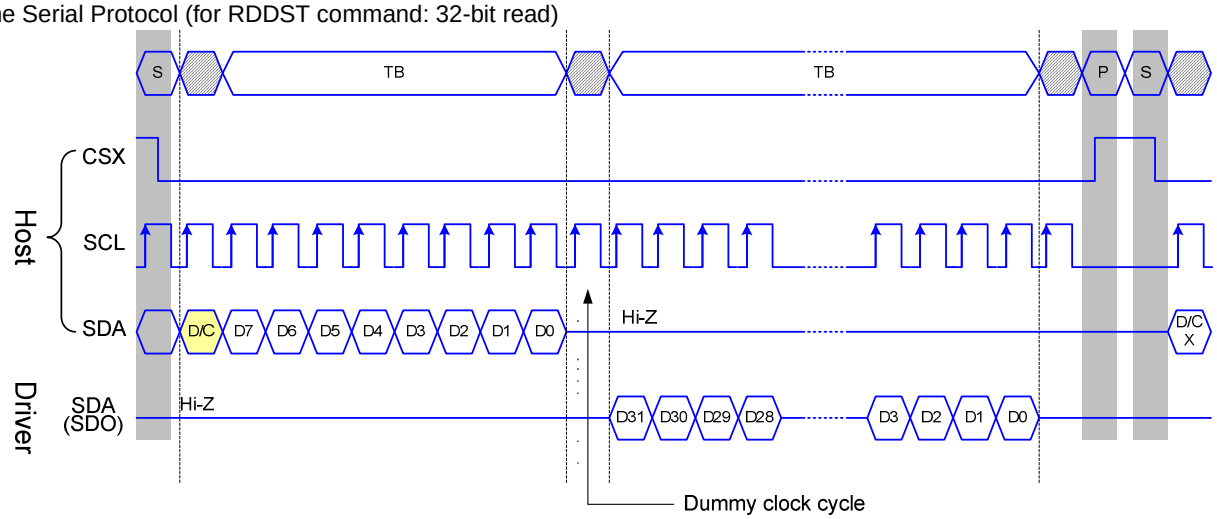
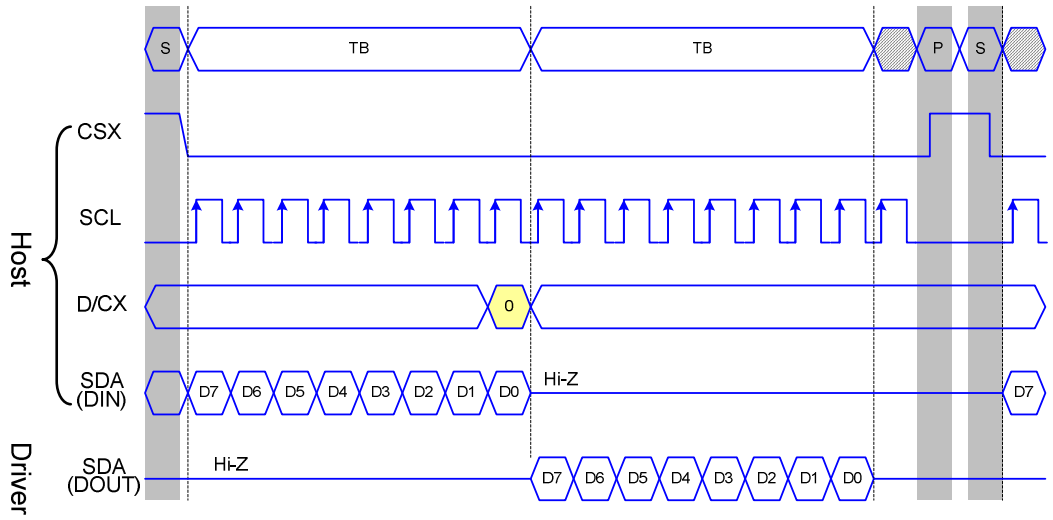
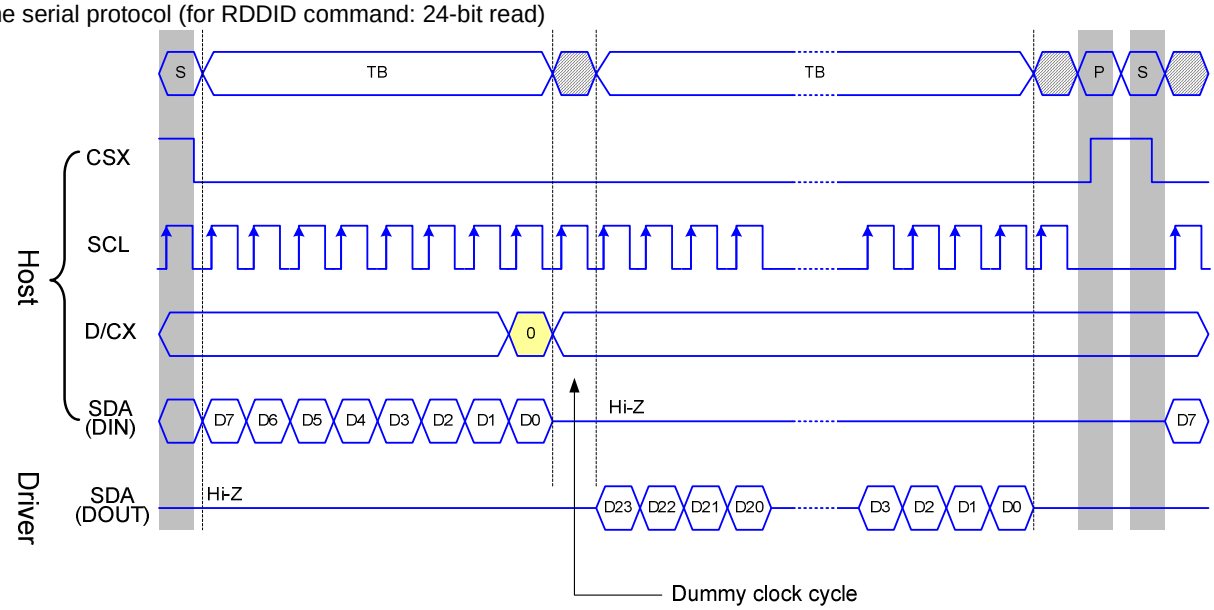


Fig. 9.4.4 3-line serial interface read protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

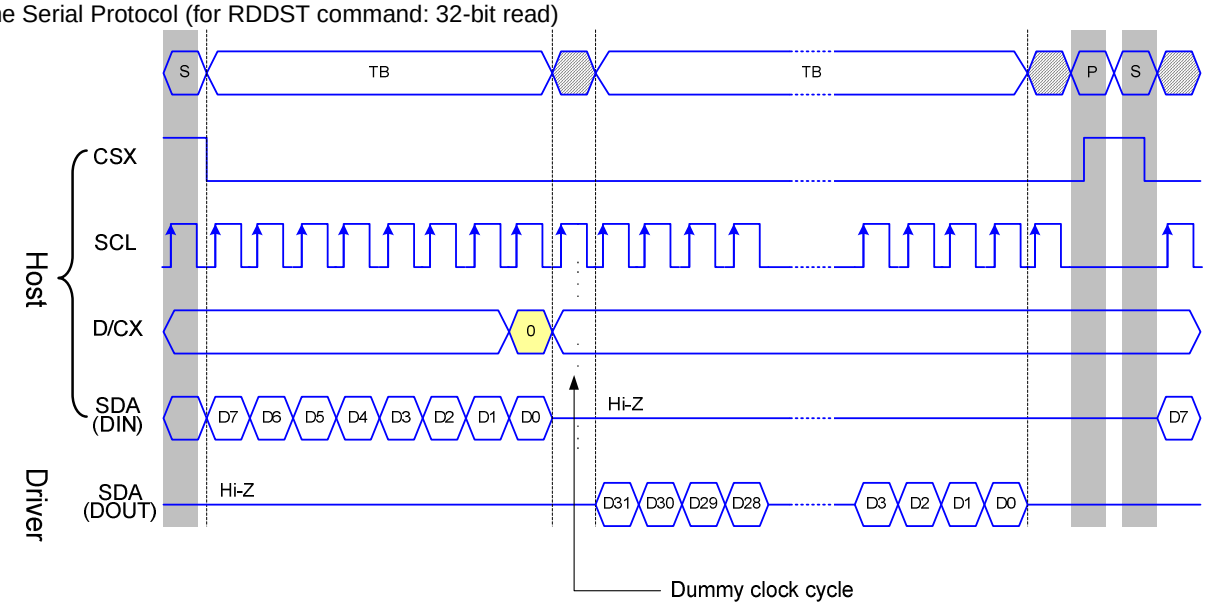


Fig. 9.4.5 4-line serial interface read protocol

9.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state. See the following example

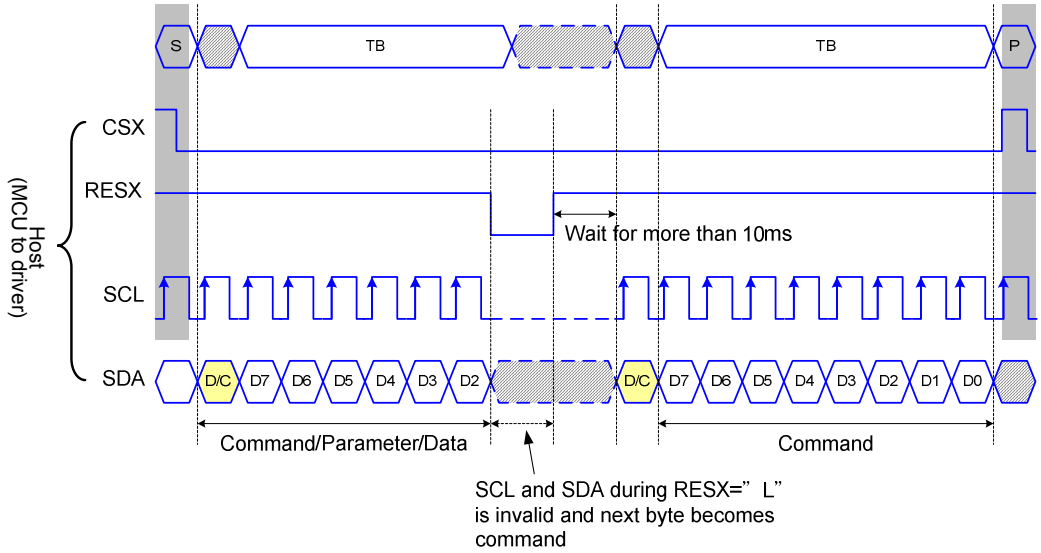


Fig. 9.5.1 Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

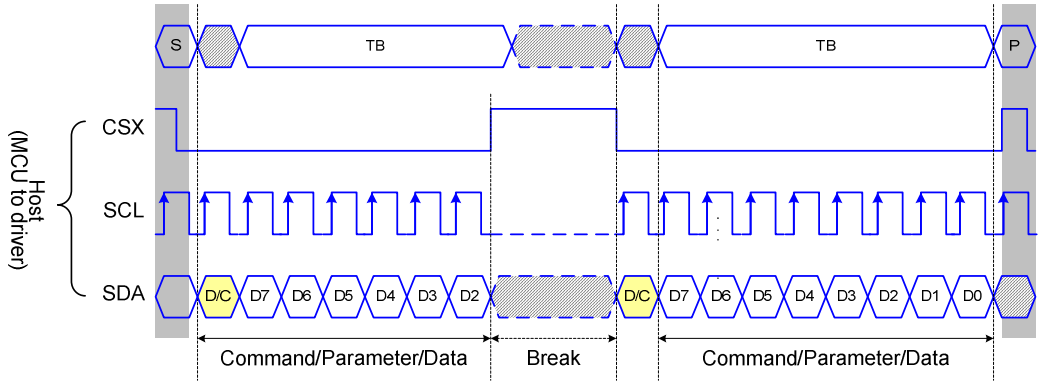


Fig. 9.5.2 Serial bus protocol, write mode – interrupted by CSX

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

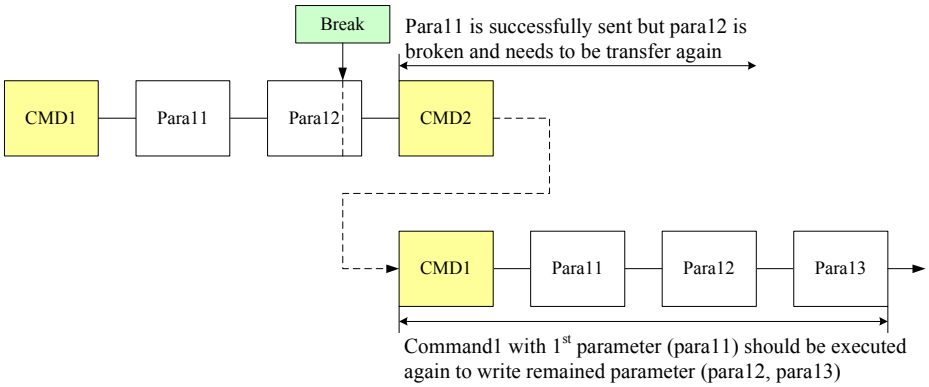


Fig.9.5.3 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

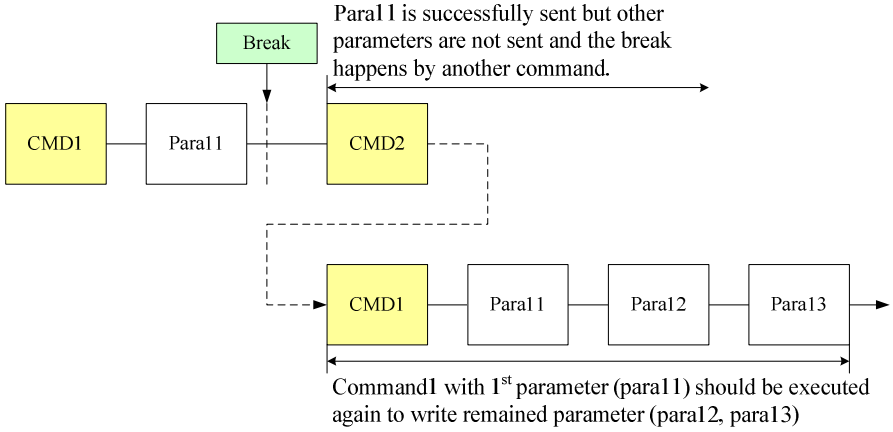


Fig. 9.5.4 Write interrupts recovery (both serial and parallel Interface)

9.6 Data transfer pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command‘s parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

9.6.1 Serial interface pause

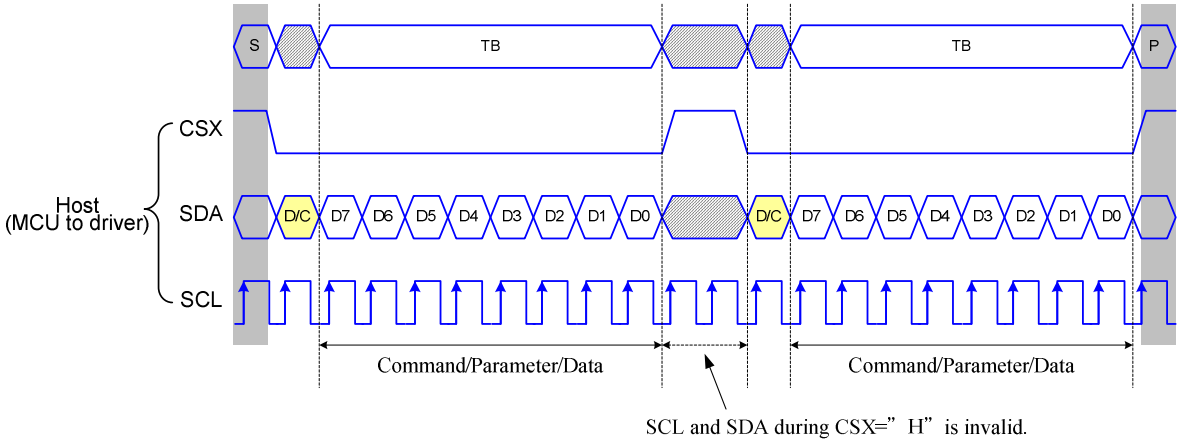


Fig. 9.6.1 Serial interface pause protocol (pause by CSX)

9.6.2 Parallel interface pause

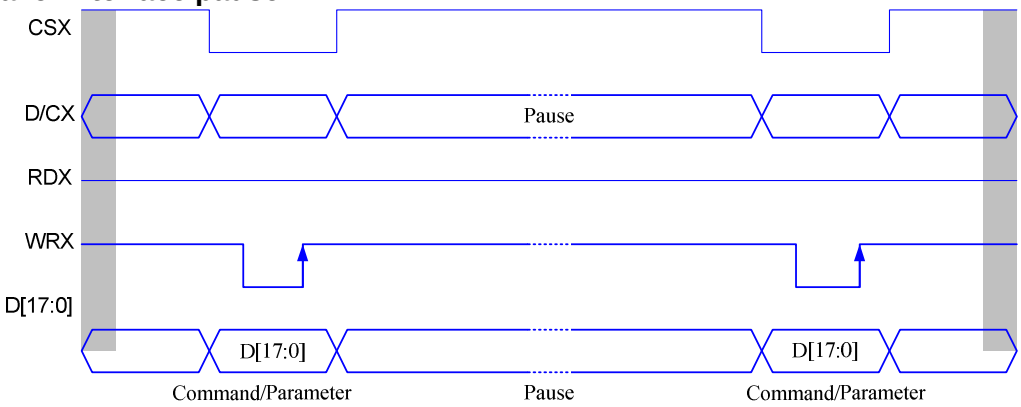


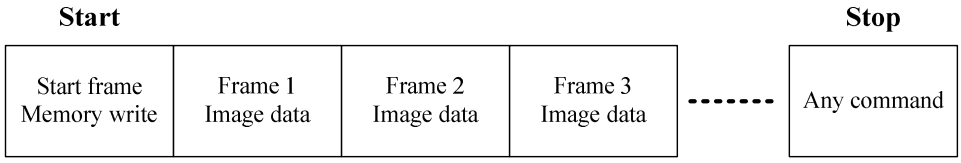
Fig. 9.6.2 Parallel bus pause protocol (paused by CSX)

9.7 Data Transfer Modes

The module has three kinds color modes for transferring data to the display RAM. These are 12-bits color per pixel, 16-bits color per pixel and 18-bits color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

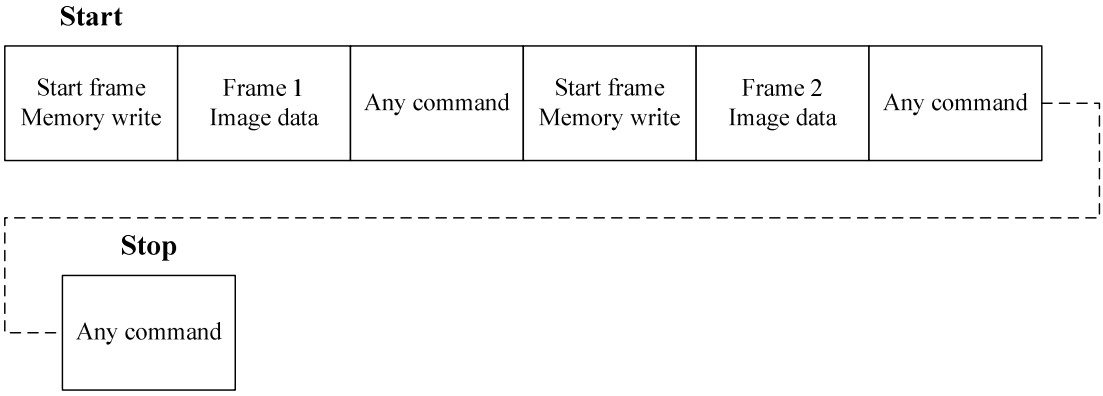
9.7.1 Method 1

The Image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



9.7.2 Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note:
1) These apply to all data transfer Color modes on both serial and parallel interfaces.
2) The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

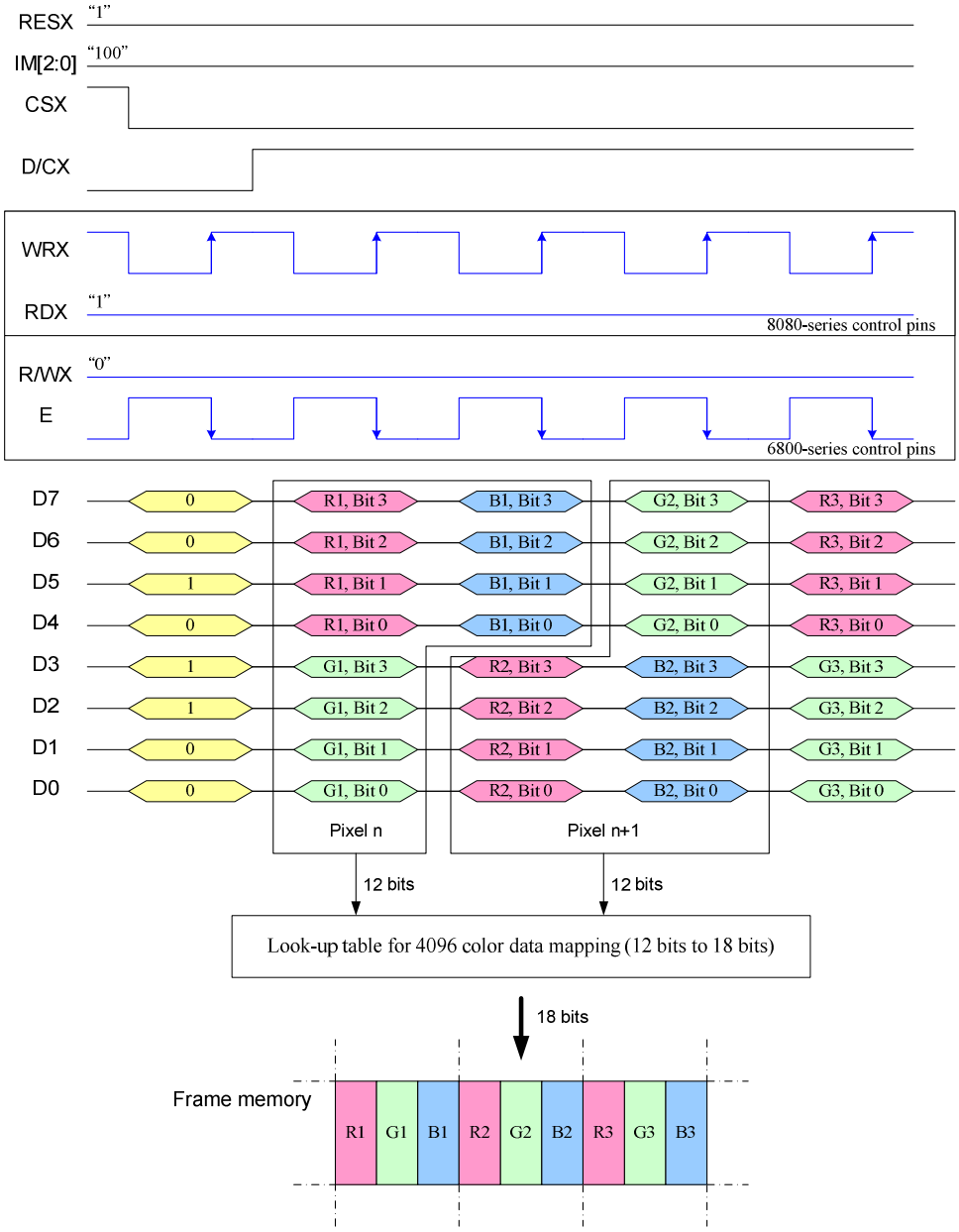
9.8 Data Color Coding

9.8.1 8-bit Parallel Interface (IM2, IM1, IM0= “100”)

Different display data formats are available for three Colors depth supported by listed below.
- 4k Colors, RGB 4,4,4-bit input,
- 65k Colors, RGB 5,6,5-bit input,.
- 262k Colors, RGB 6,6,6-bit input,

9.8.1.1 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= “03h”

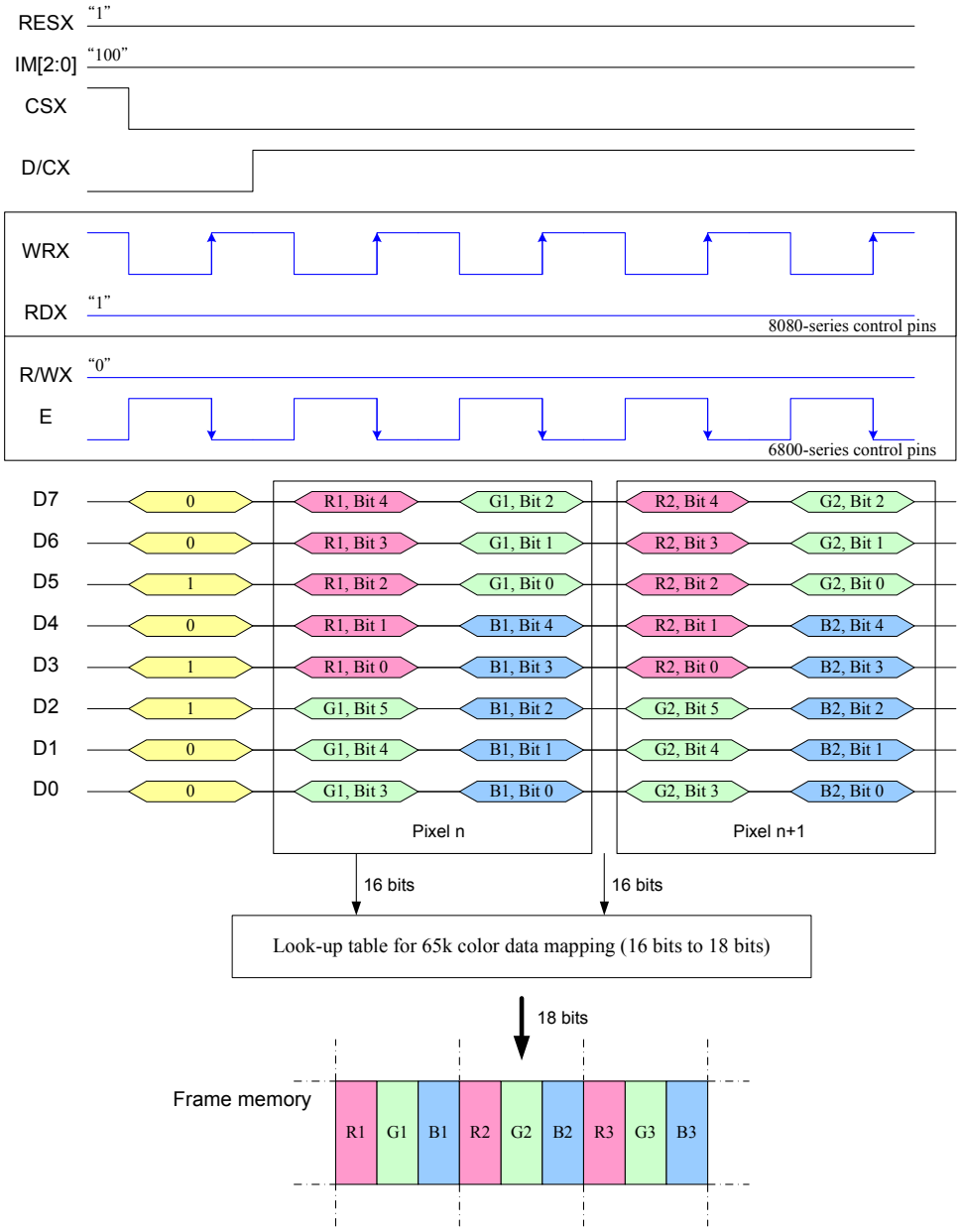
There are 2 pixels (6 sub-pixels) per 3-bytes.



Note1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2. 3-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.
Note 3. ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.1.2 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= “05h”

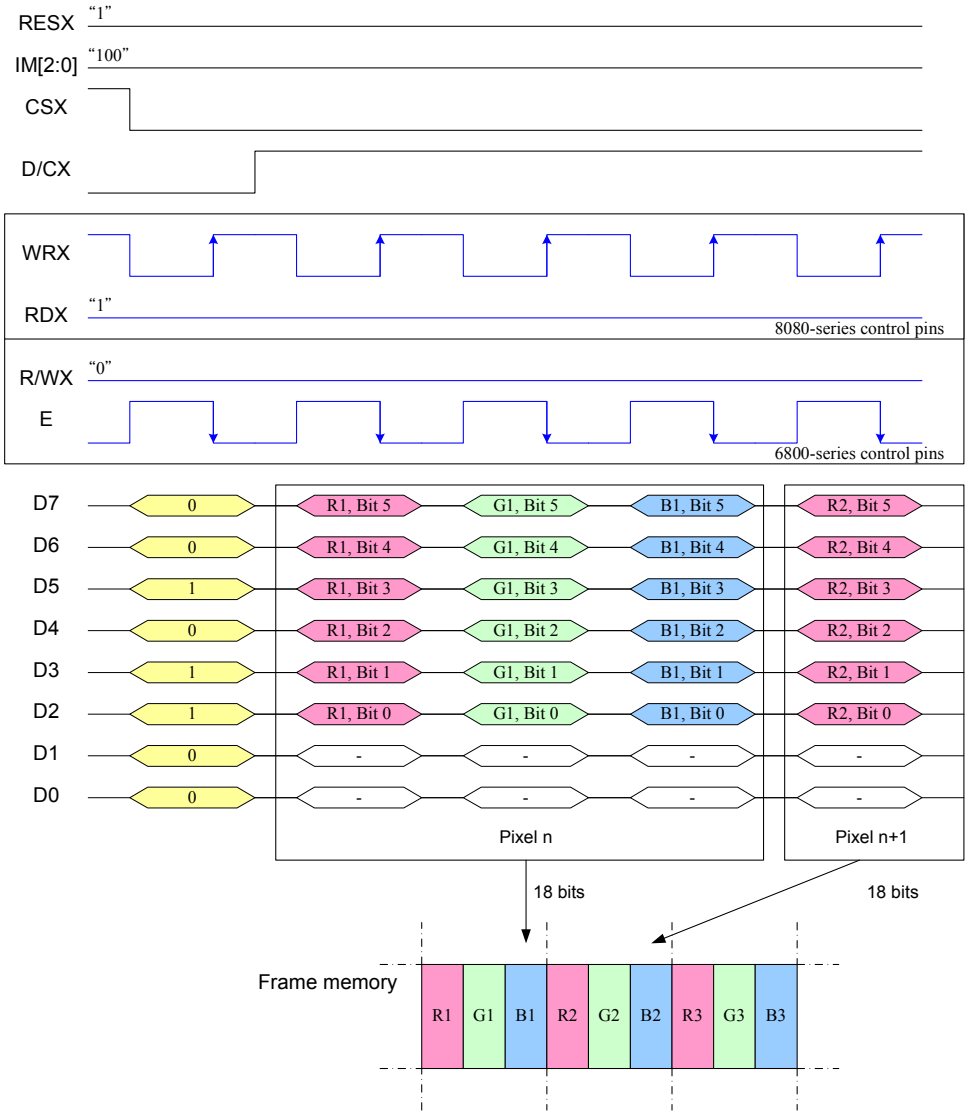
There is 1 pixel (3 sub-pixels) per 2-bytes.



Note1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
Note 2.2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.
Note 3. ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.1.3 8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= “06h”

There is 1 pixel (3 sub-pixels) per 3-bytes.



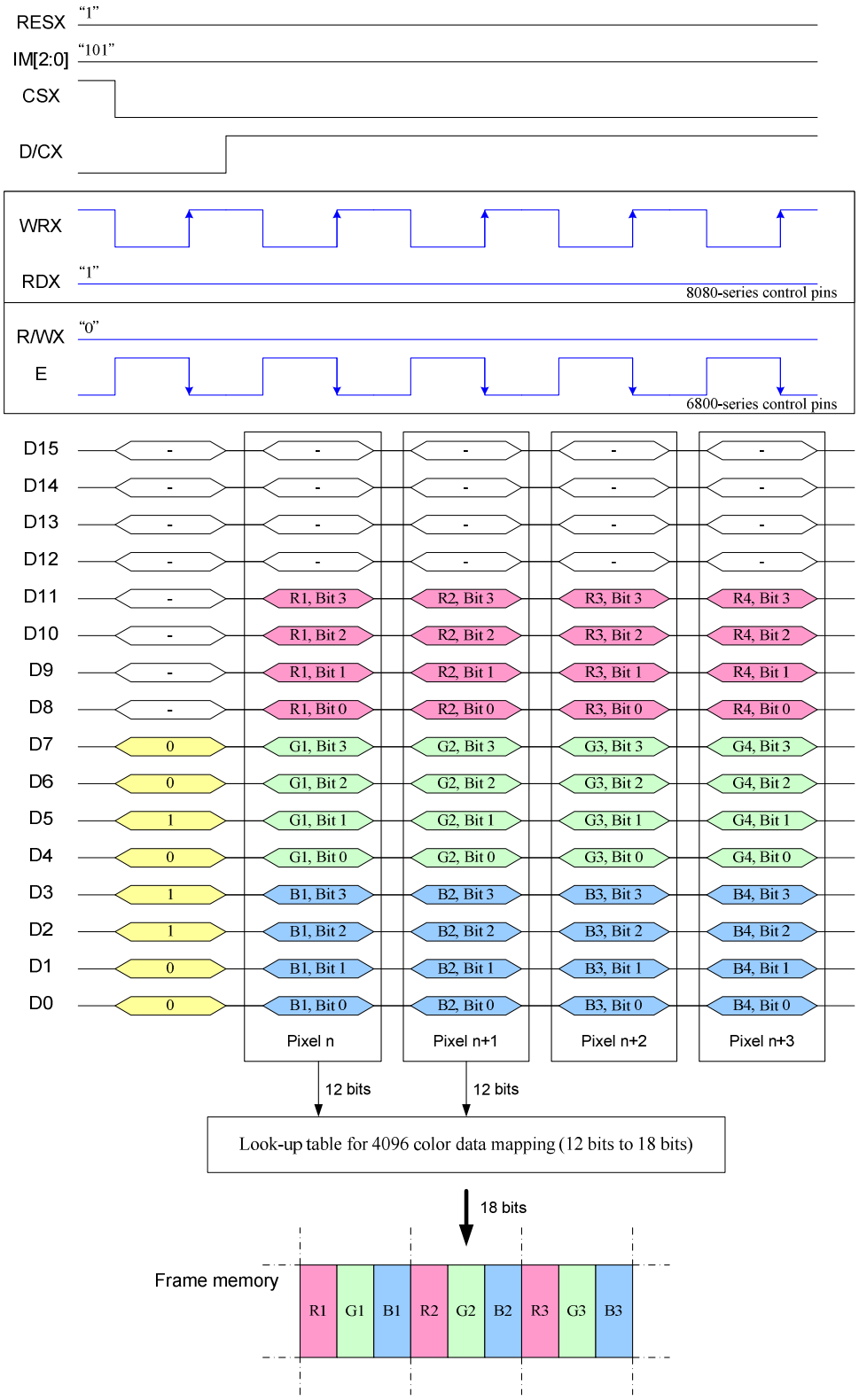
Note1. The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3. ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.2 16-Bit Parallel Interface (IM2,IM1, IM0= “101”)

Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

9.8.2.1 16-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= “03h”

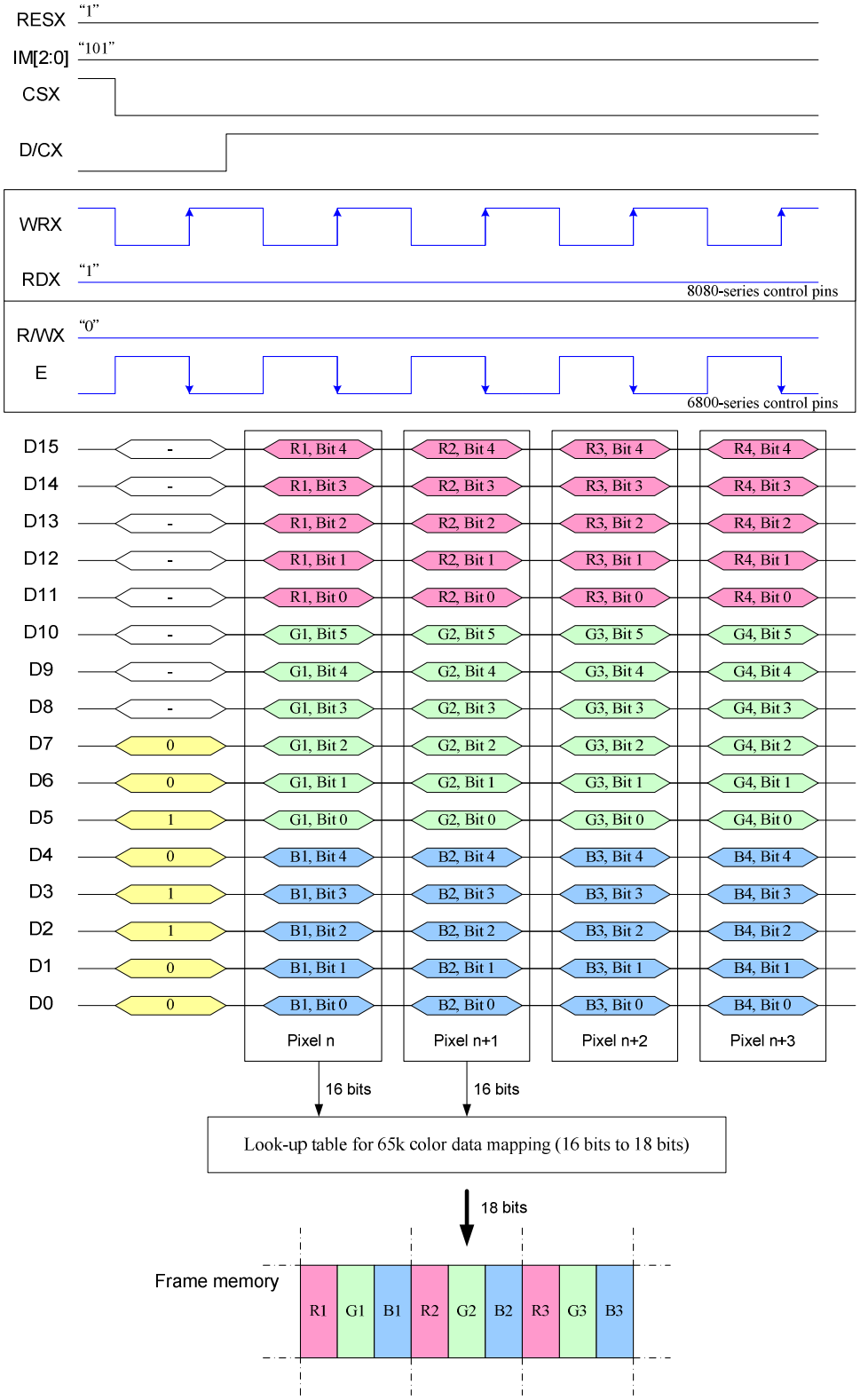
There is 1 pixel (3 sub-pixels) per 1 bytes, 12-bit/pixel.



Note1. The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2.1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

9.8.2.2 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= “05h”

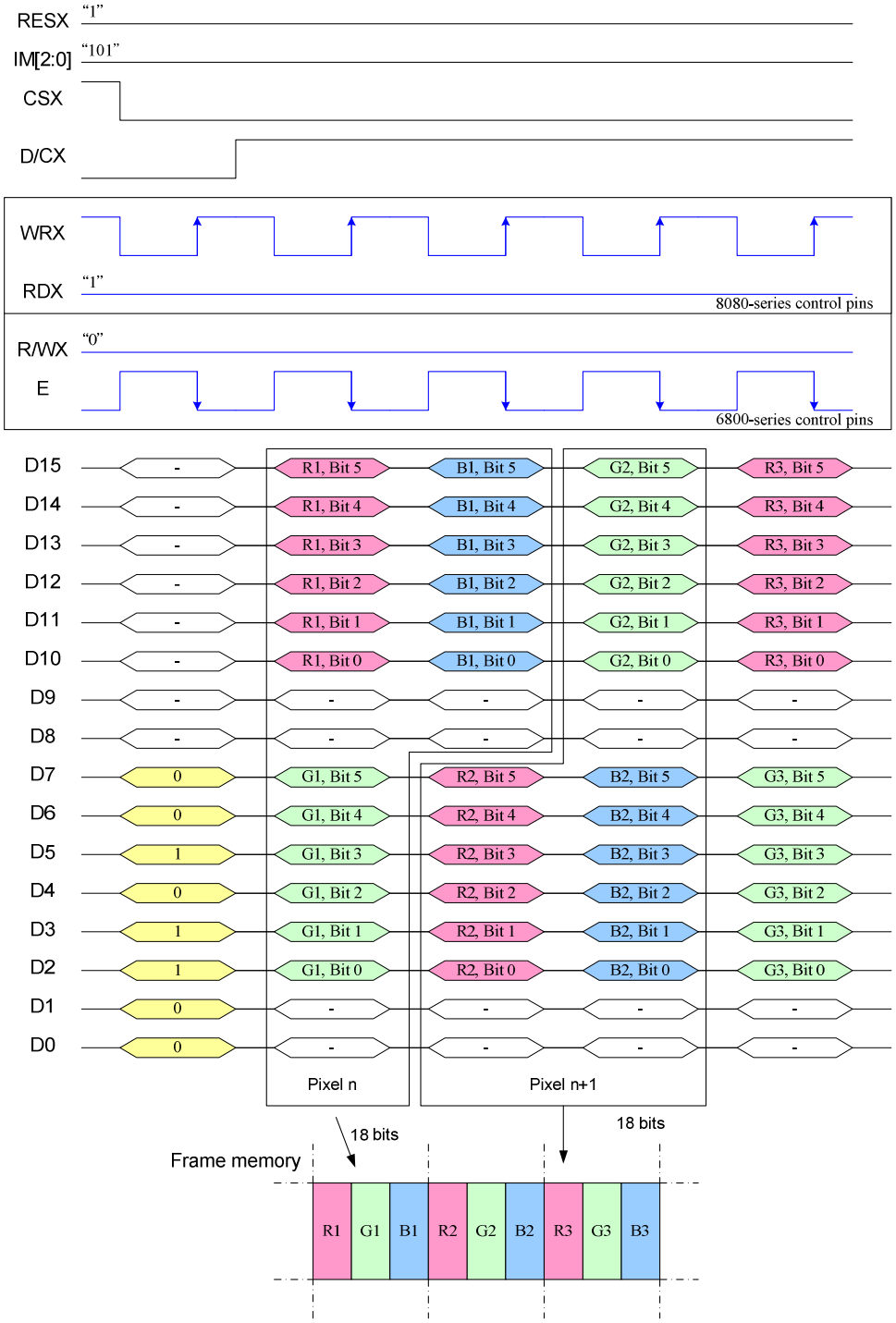
There is 1 pixel (3 sub-pixels) per 1 bytes, 16-bit/pixel.



Note1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
Note 2.1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.
Note 3. ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.2.3 16-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= “06h”

There are 2 pixel (6 sub-pixels) per 3 bytes, 18-bit/pixel.



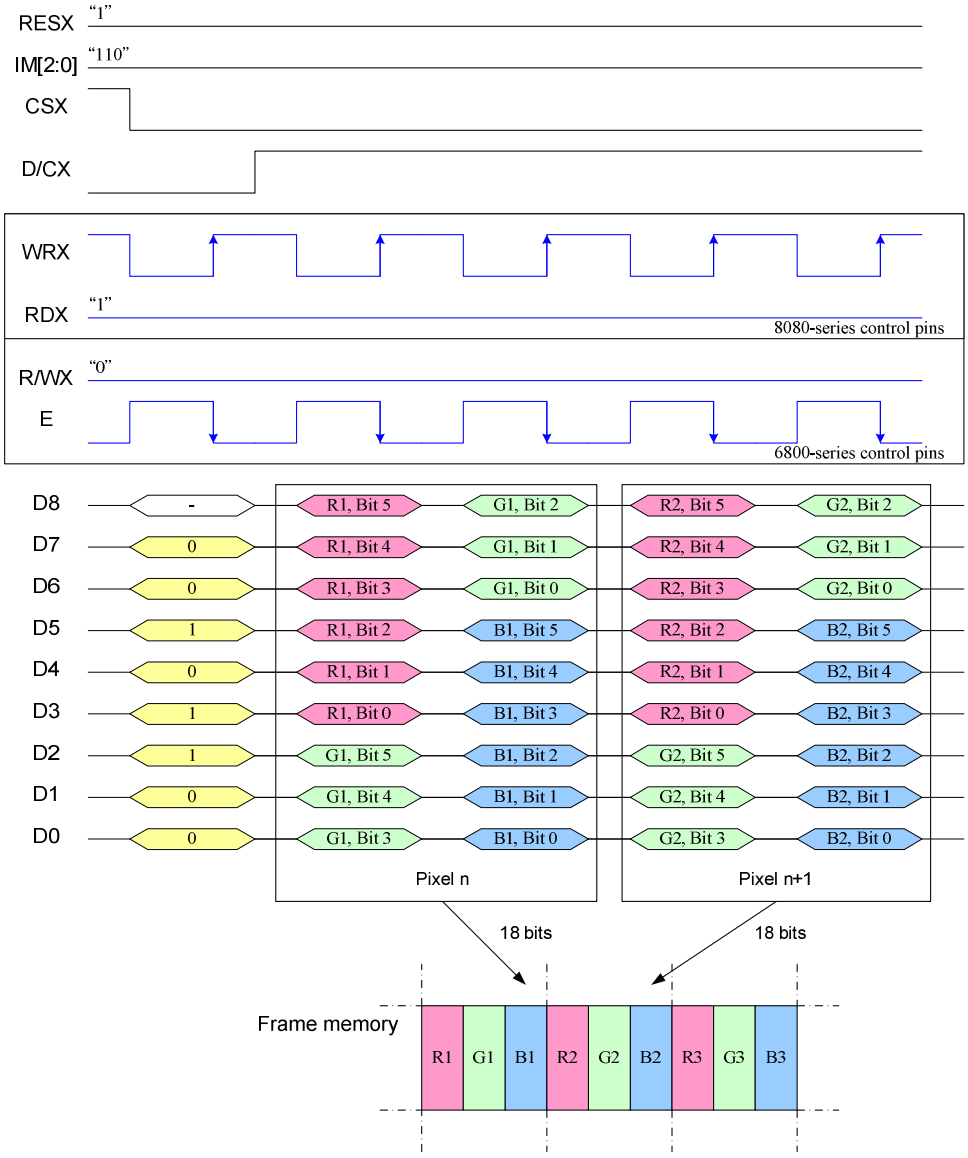
Note1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3. ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.3 9-Bit Parallel Interface (IM2, IM1, IM0=“110”)

Different display data formats are available for three colors depth supported by listed below.
- 262k colors, RGB 6,6,6-bit input

9.8.3.1 Write 9-bit data for RGB 6-6-6-bit input (262k-color)

There are 1 pixel (6 sub-pixels) per 3 bytes, 18-bit/pixel.



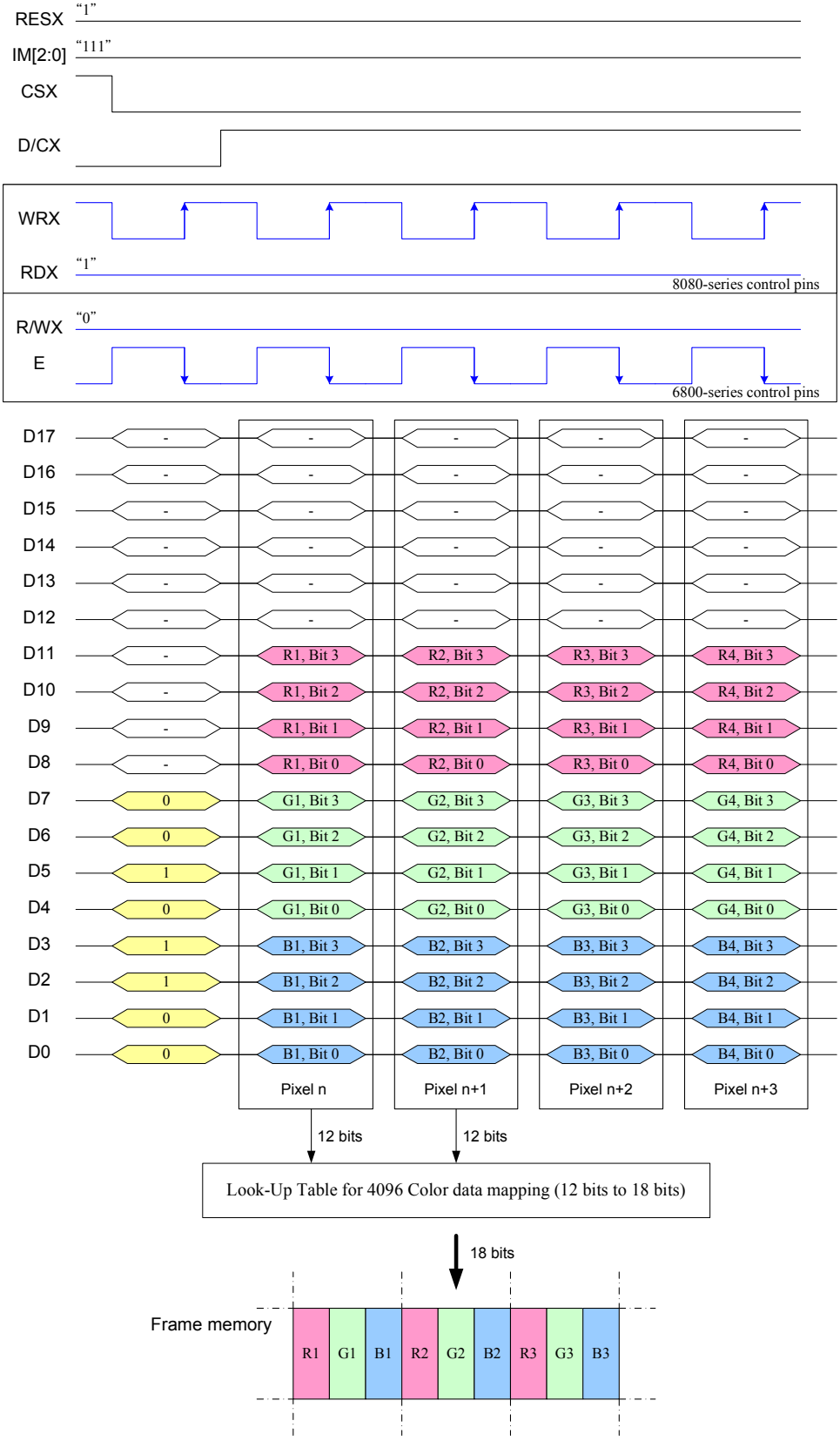
Note1. The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3. ‘-‘ = Don't care - Can be set to '0' or '1'

9.8.4 18-Bit Parallel Interface (IM2, IM1, IM0="111")

Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

9.8.4.1 18-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

There are 1 pixel (3 sub-pixels) per 1 byte, 12-bit/pixel.

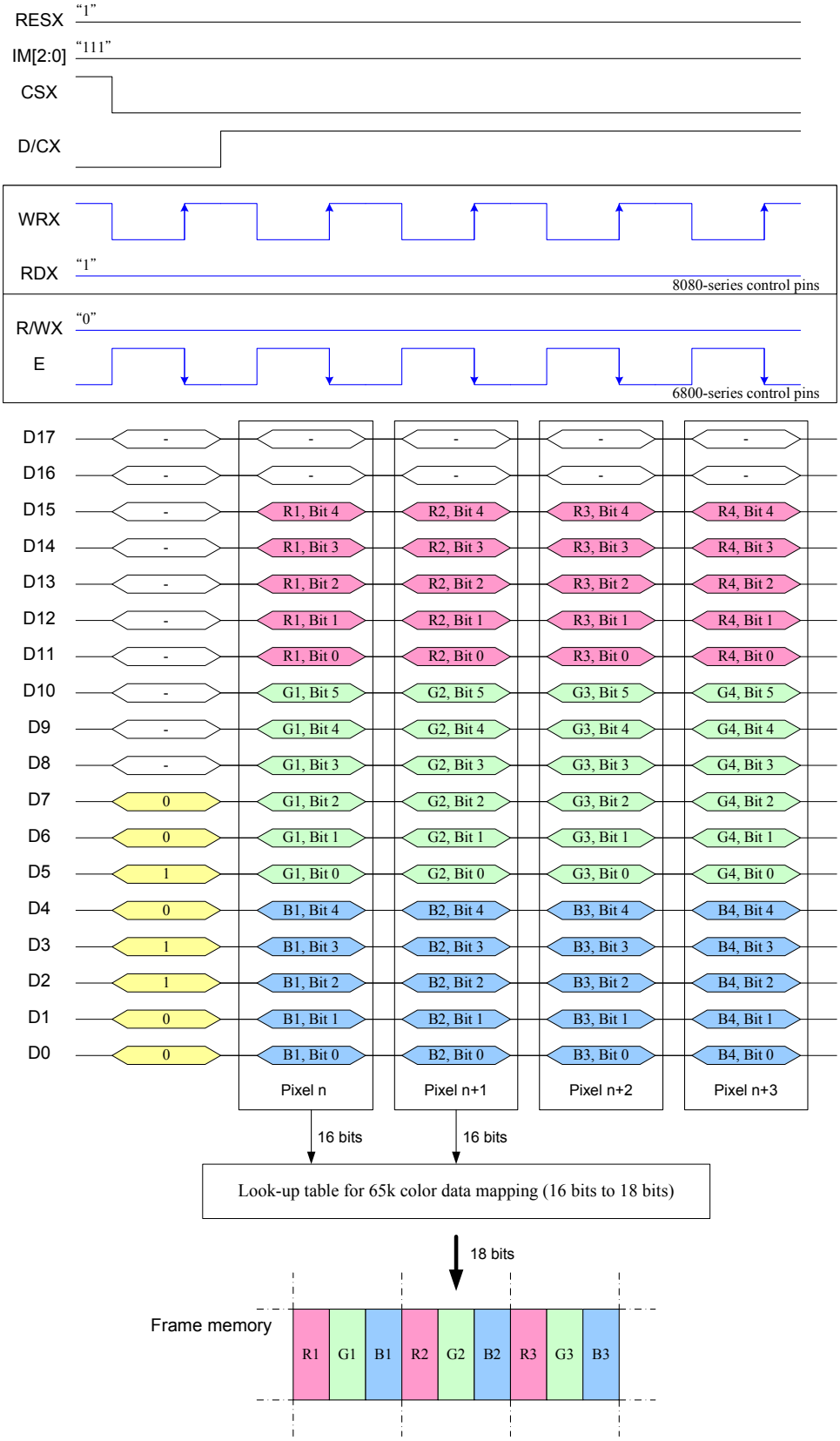


Note1. The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue

data.
Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

9.8.4.2 18-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"

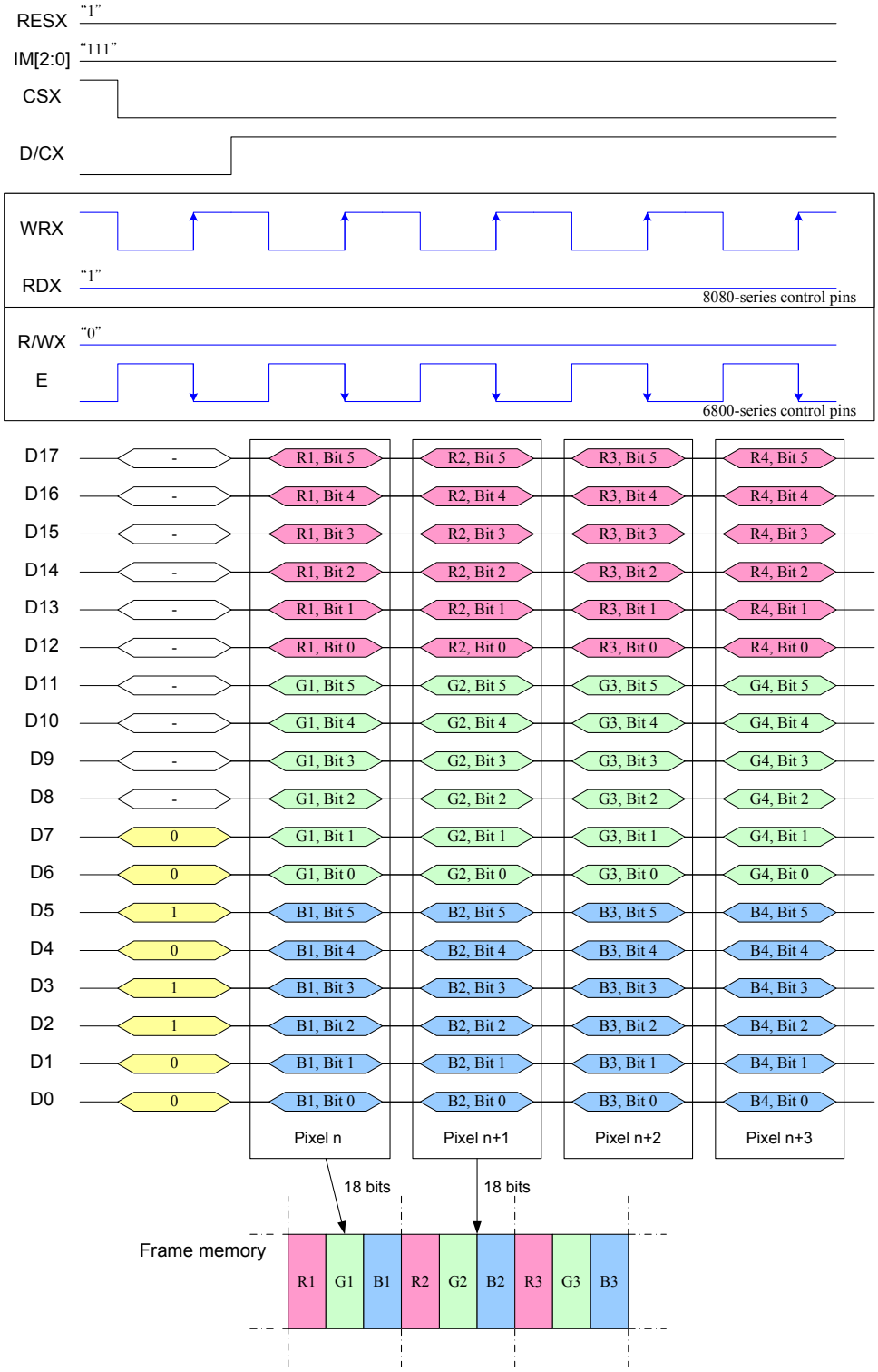
There are 1 pixel (3 sub-pixels) per 1 byte, 16-bit/pixel.



Note1. The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

9.8.4.3 18-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

There are 1 pixel (3 sub-pixels) per 1 bytes, 18-bit/pixel.

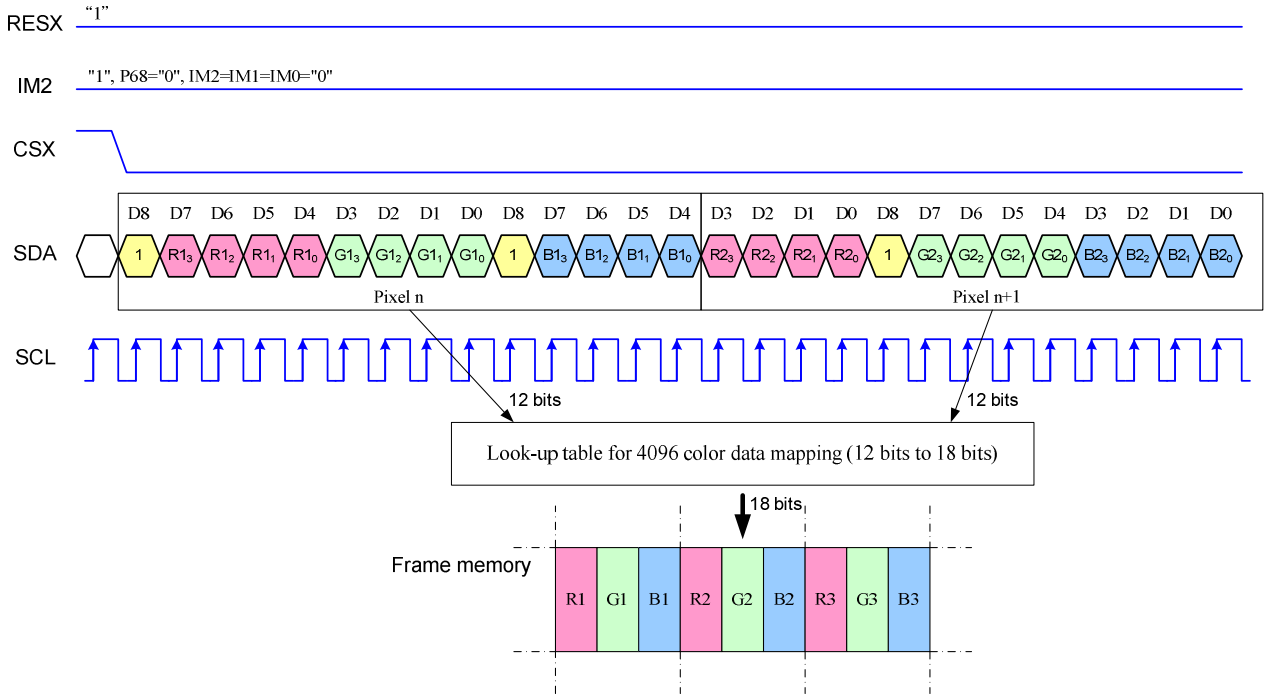


Note1. The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.
Note 2.1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.
N

9.8.5 3-line serial Interface(4WSPI='0')

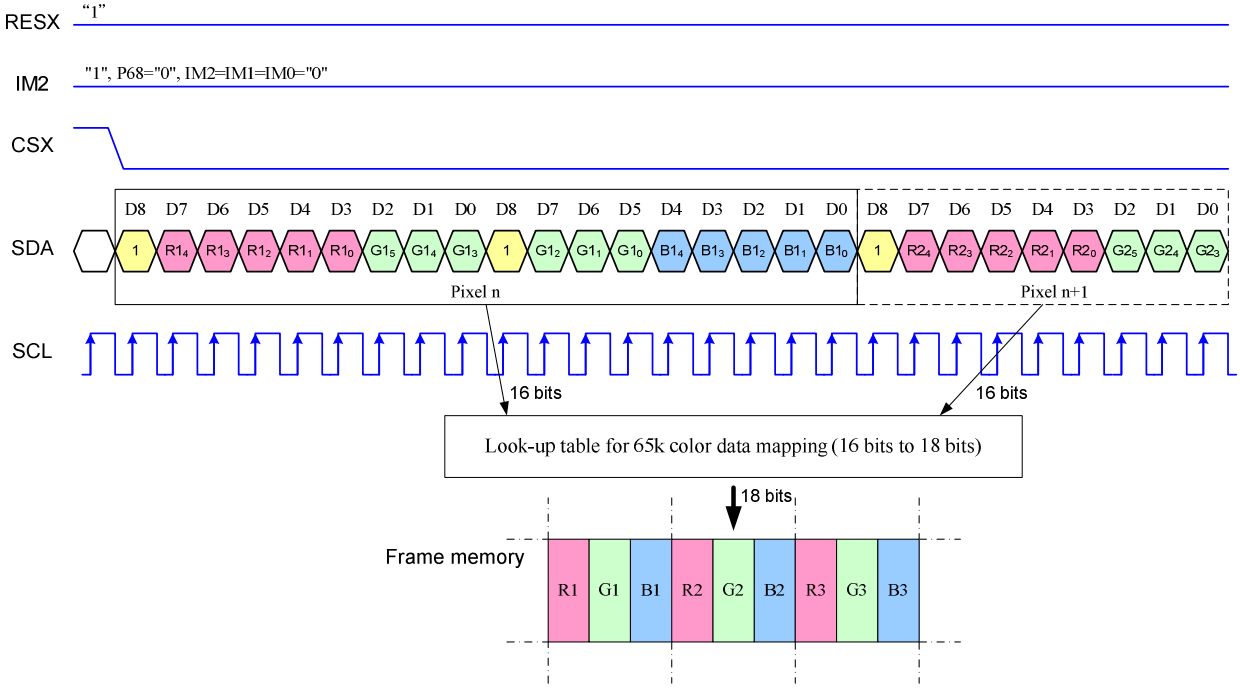
Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

9.8.5.1 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"



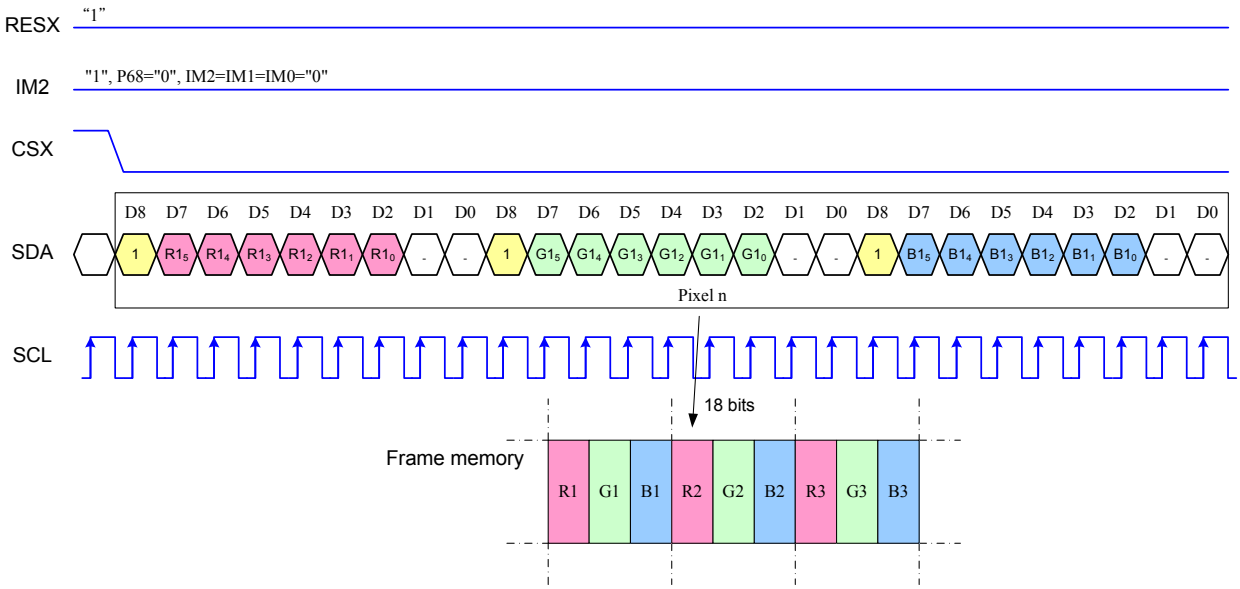
Note 1. pixel data with the 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.5.2 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"



Note 1. pixel data with the 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.5.3 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

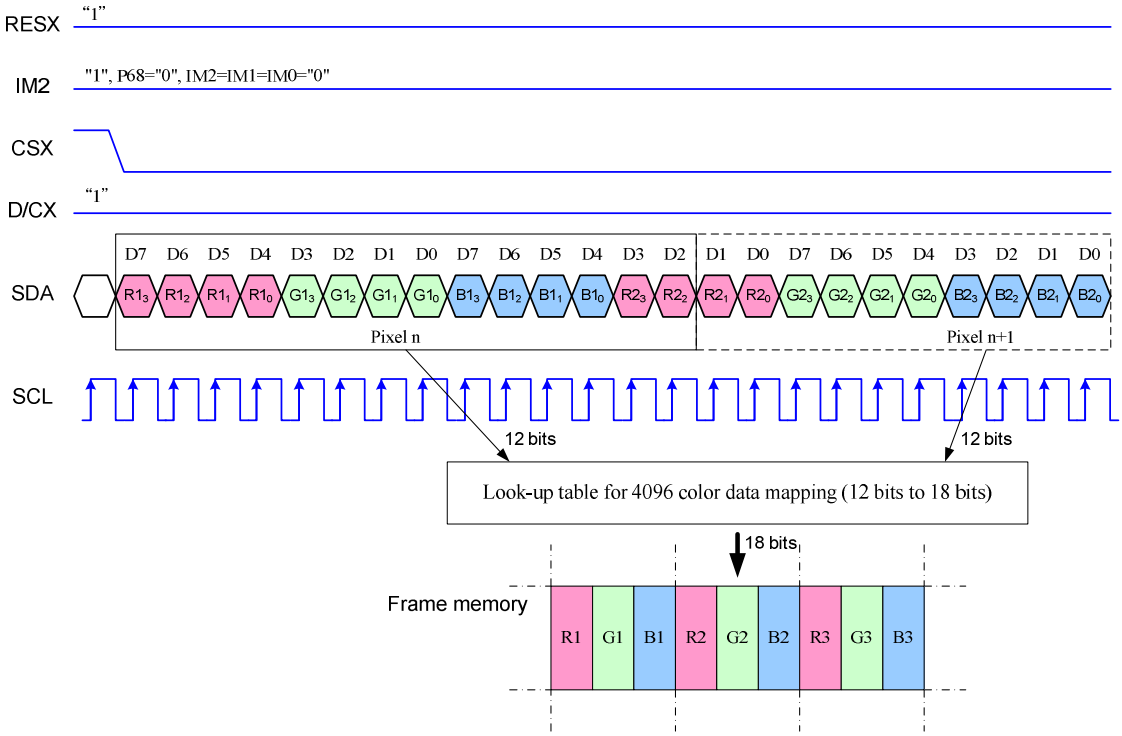


Note 1. pixel data with the 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.6 4-line serial Interface(4WSPI='1')

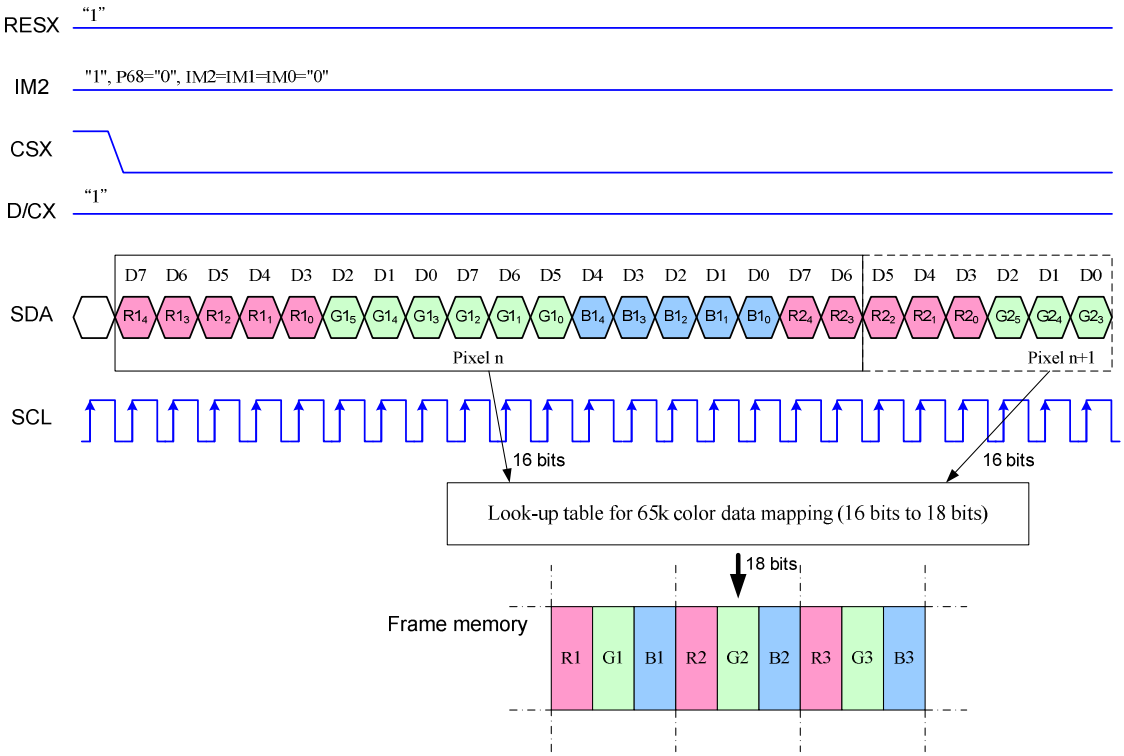
Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

9.8.6.1 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"



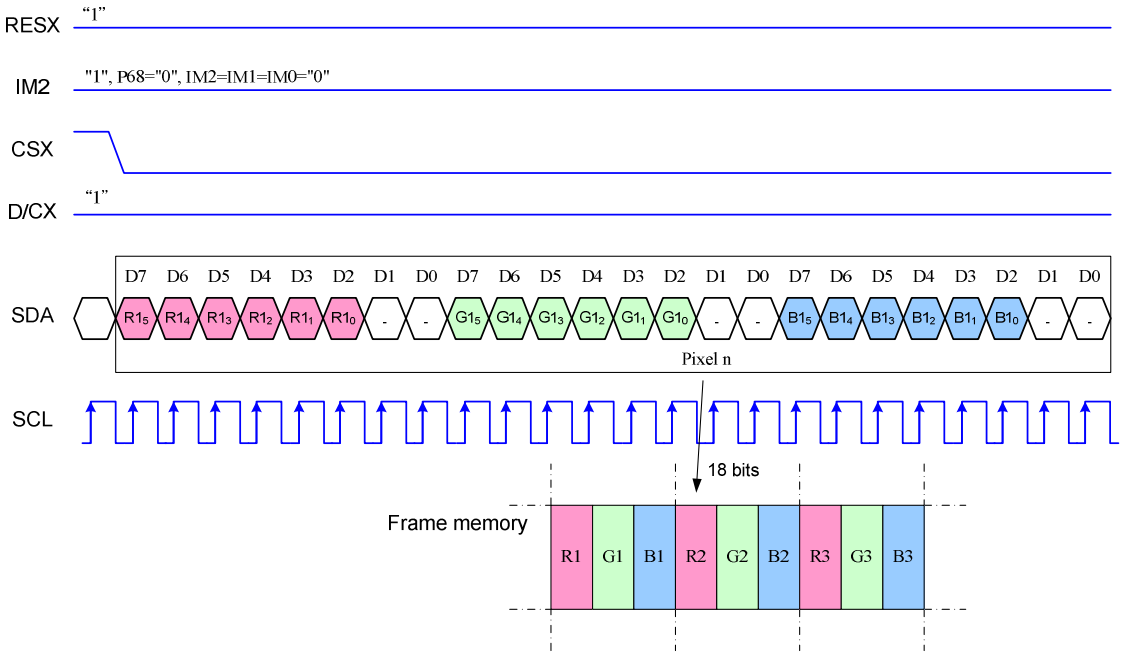
Note 1. pixel data with the 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.6.2 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"



Note 1. pixel data with the 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.6.3 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"



Note 1. pixel data with the 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.9 RGB interface

9.9.1 General Description

The module uses 6, 16 and 18-bit parallel RGB interface which includes: VS, HS, DE, PCLK, D[17:0]. The interface is activated after Power-On sequence (See section Power-On/Off Sequence)

Pixel clock (PCLK) is running all the time without stopping and it is used to enter VS, HS, DE and D[17:0] states at the rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep-In mode etc.

Vertical synchronization (VS) is used to tell the driver when a new frame of the display is beginning. This is negative ('0', low) active and its state is read by the driver at the rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell the driver when a new line of the frame is beginning. This is negative ('0', low) active and its state is read by the driver at the rising edge of the PCLK signal.

Data Enable (DE) is used to tell the driver when the RGB information will be transferred ti the driver. This is a positive ('1', high) active and its state is read by the driver at the rising edge of the PCLK signal.

D[17:0] (18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE='1' and at the rising edge of PCLK). D[17:0] can be '0' (low) or '1' (high). These lines are read by the driver at the rising edge of the PCLK signal.

The PCLK cycle is described in the following figure.

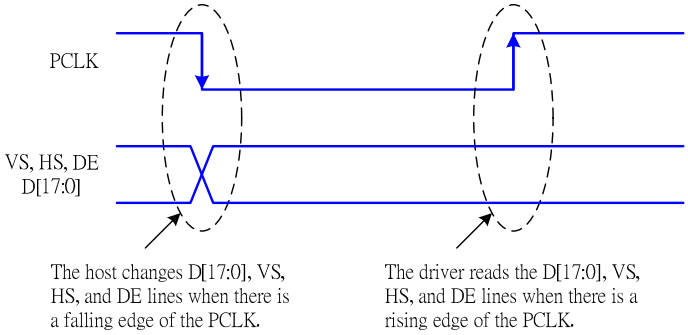


Fig. 9.9.1 PCLK cycle

Note: PCLK is an unsynchronized signal (It can be stopped).

9.9.2 General timing diagram

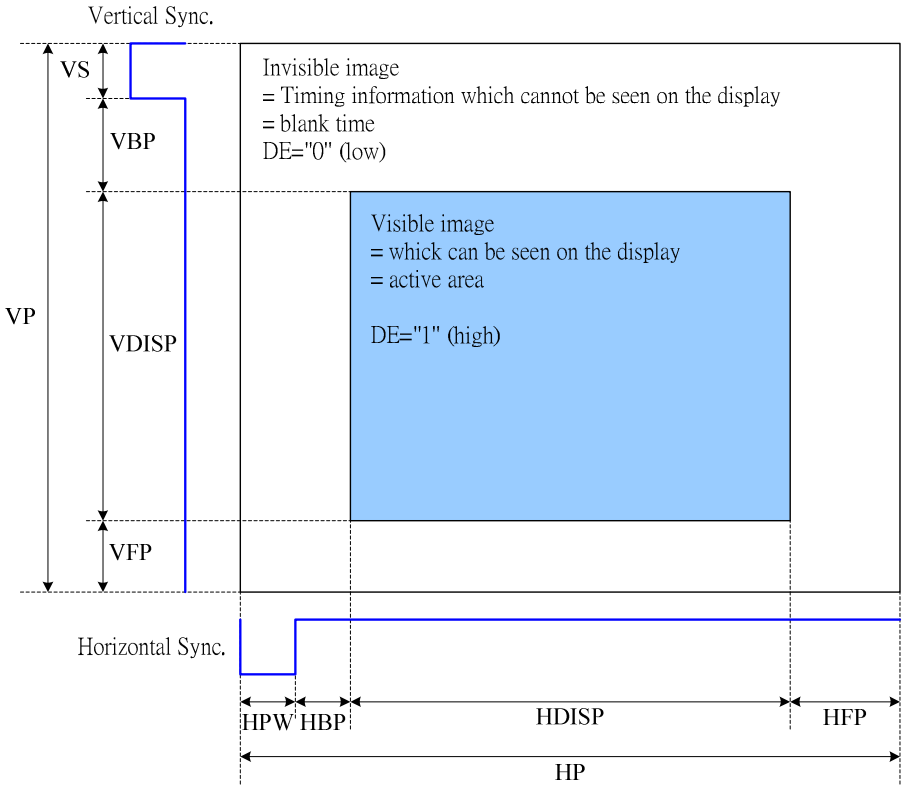


Fig. 9.9.2 RGB general timing diagram

The image information must be correct on the display, when the timings conforms the spec of the RGB interface.

However, the image information can be incorrect on the display temporarily when timing is out of spec. The correct image information must be displayed automatically (by the display module) in the next frame period as the timing recovers from out of spec to within spec.

9.9.3 Updating order on display active area (normal display mode On + sleep out)

There are different kinds of updating orders for the display. These updating orders are controlled by H/W (SMX, SMY) and S/W (MX, MY, MV) bits.

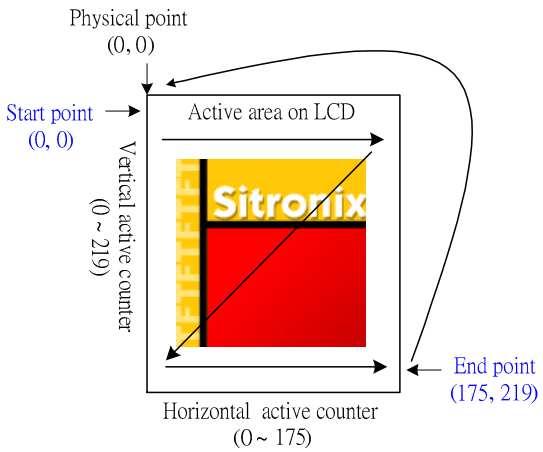


Fig. 9.9.3 Updating order when MADCTL's MX="0" and MY="0"

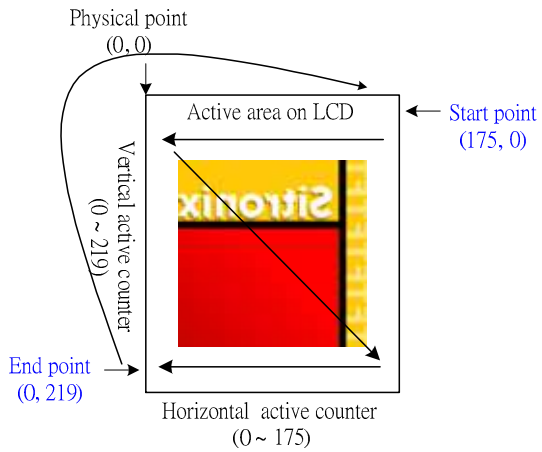


Fig. 9.9.4 Updating order when MADCTL's MX="1" and MY="0"

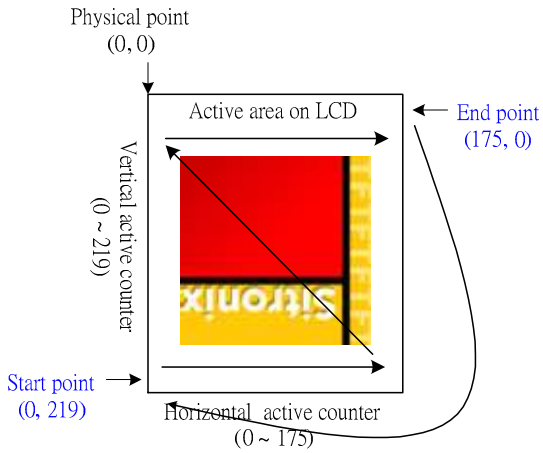


Fig. 9.9.5 Updating order when MADCTL's MX="0" and MY="1"

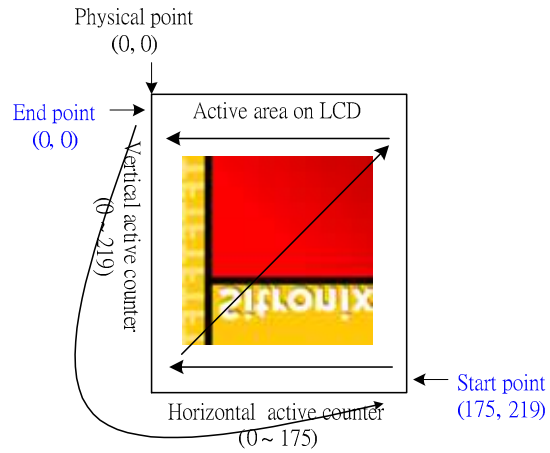


Fig. 9.9.6 Updating order when MADCTL's MX="1" and MY="1"

Table 9.9.1 Rules for updating order

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Signal pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The horizontal counter is larger than 175 and the vertical counter is larger than 219	Return to 0	Return to 0

Note 1. Pixel order is RGB on the display.
Note 2. Data streaming direction from the host to the display is described in the following figure.

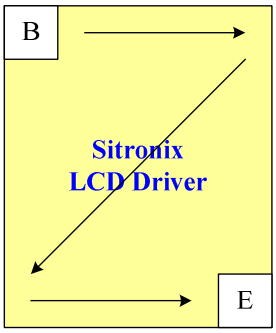


Fig. 9.9.3 Data streaming order for RGB interface

9.9.4 RGB Interface Bus Width set

All 4-kinds of bus width can be available in RGB interface mode (selected by COLMOD (3Ah) command for 6-bit, 16-bit and 18-bit data width)

VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
0101	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bit data
0110	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit data
1110	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bit data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note 1: When VIPF[3:0]="1110", 6-bit data width of 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 2: Only VIPF[3:0]= "0101" , "0110" and "1110" are valid on RGB I/F, Others are invalid.
Note 3. 'x' Don't care, but need to set VDDI or DGND level.

9.9.5 RGB Interface Mode Set

Table 9.9.5.1 RGB Interface Mode Setting

RGB I/F Mode	PCLK	DE	VS	HS	Video Data bus D[17:0]	Register for Blanking Porch setting	Reference clock for Display
RGB Mode 1	Used	Used	Used	Used	Used	Not Used	Internal Oscillator
RGB Mode 2	Used	Used	Used	Used	Used	Used	Internal Oscillator

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

In RGB Mode 1 (RCM1, RCM0 = "10"), writing data to frame memory is done by PCLK and data bus (D[17:0]), when DE is in high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to driver.

In RGB Mode 2 (RCM1, RCM0 = "11"), blanking porch setting of VS and HS signals are defined by RGBBPCTR (B5h) command. DE pin is used for data making. When DE pin is high, valid data is directly stored to frame memory. In the contrast, if DE pin is low the data of frame memory will keep same status.

9.9.6 RGB Interface Timing Diagram
9.9.6.1 General Timings for RGB I/F

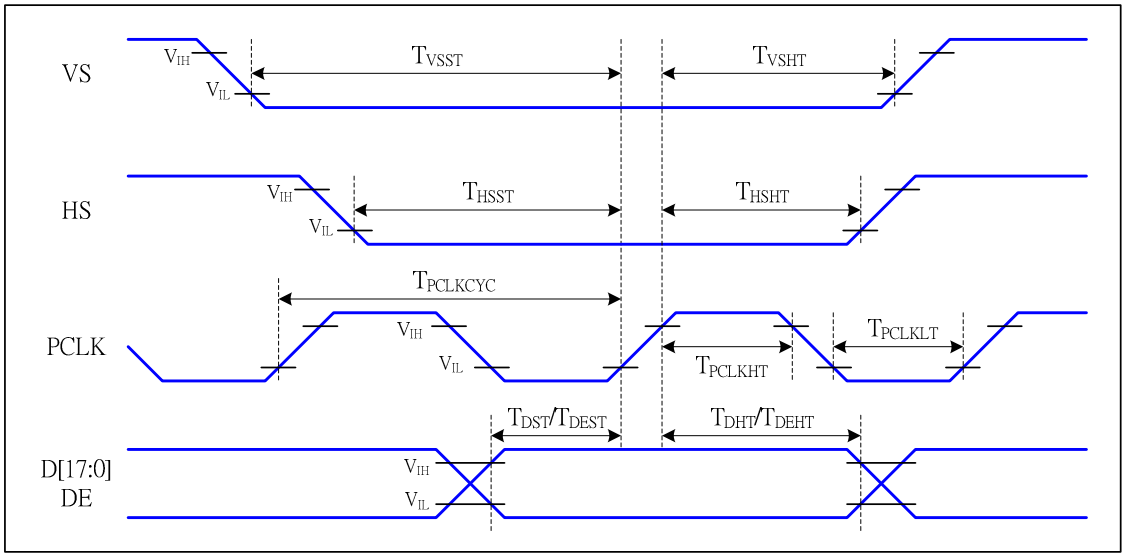


Fig. 9.9.6 General timing of RGB interface

Table 9.9.6.1 General Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Pixel low pulse width	T_{PCLKLT}		15			
Pixel high pulse width	T_{PCLKHT}		15			
Vertical Sync. set-up time	T_{VSST}		15			ns
Vertical Sync. hold time	T_{VSSHT}		15			ns
Horizontal Sync. set-up time	T_{HSST}		15			ns
Horizontal Sync. hold time	T_{VSSHT}		15			ns
Data Enable set-up time	T_{DEST}		15			
Data Enable hold time	T_{DEHT}		15			
Data set-up time	T_{DST}		15			
Data hold time	T_{DHT}		15			

Note 1: VDDI=1.6 to 3.0V, VDD=2.7 to 3.0V, AGND=DGND=0V, Ta=-30 to 70 ℃ (to +85℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Note 3: Data lines can be set to "High" or "Low" during blanking time – Don't care.
Note 4: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.
Note 5: HP is multiples of eight PCLK.

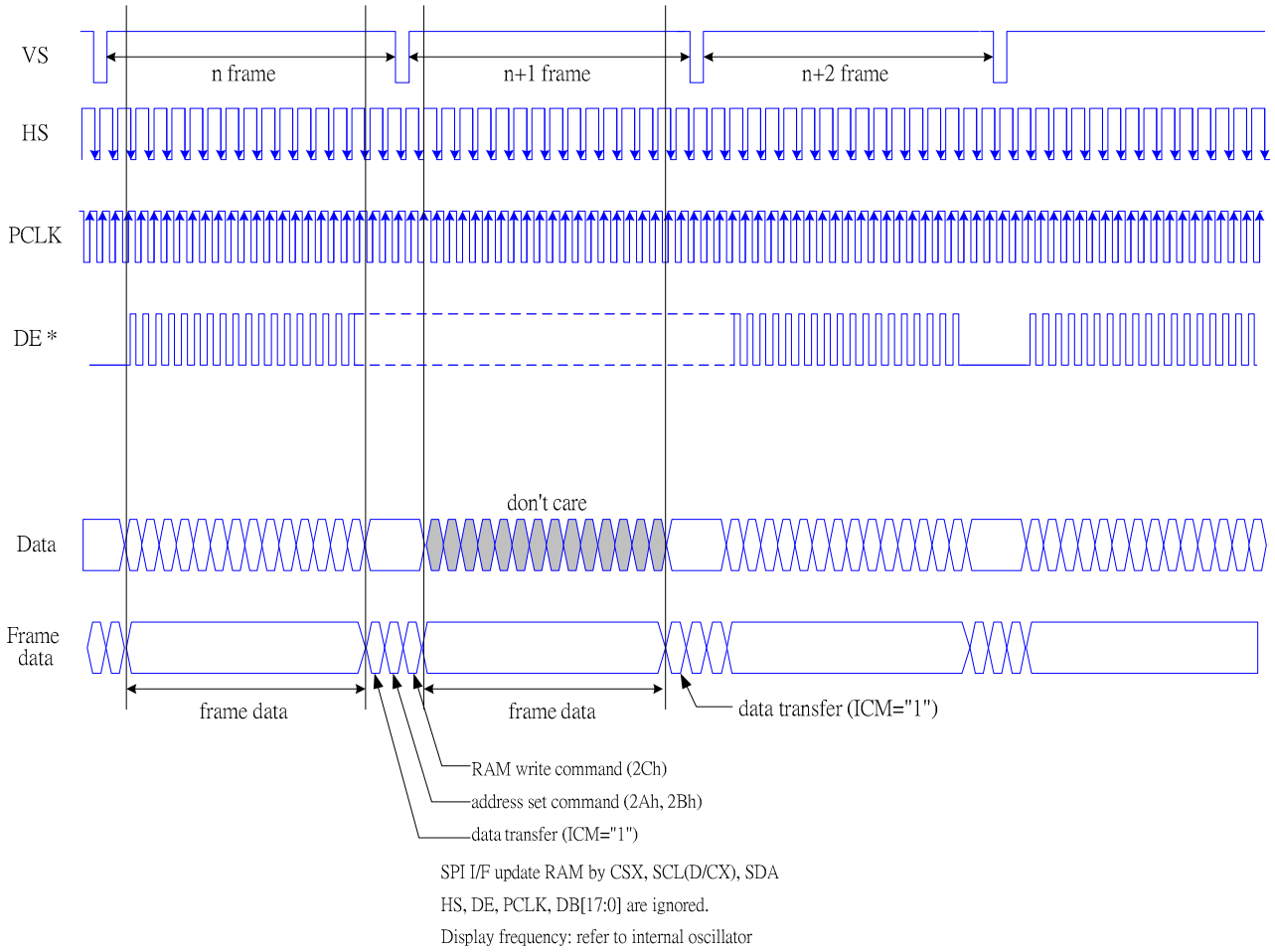


Fig. 9.9.7 RAM access via SPI interface in RGB mode

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

9.9.6.2 RGB Interface Mode 1 Timing Diagram

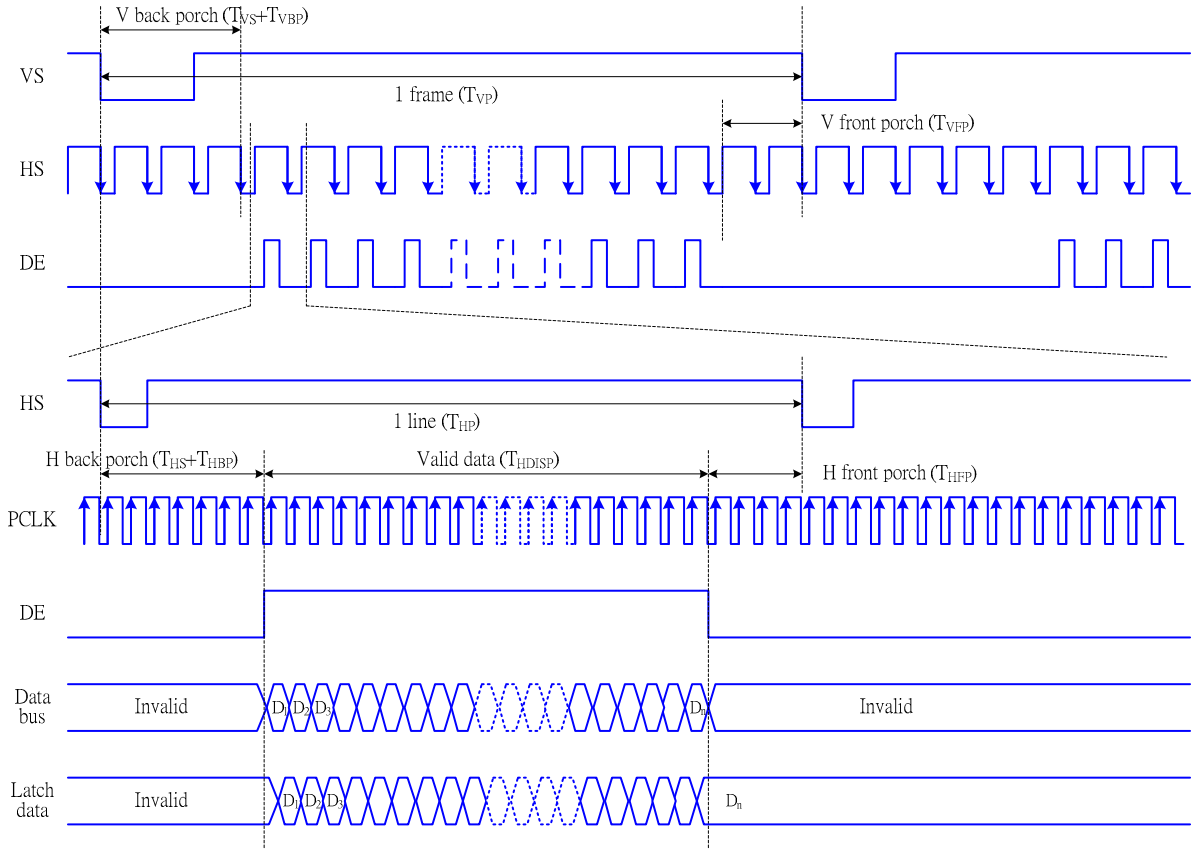


Fig. 9.9.8 RGB mode 1 timing diagram

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

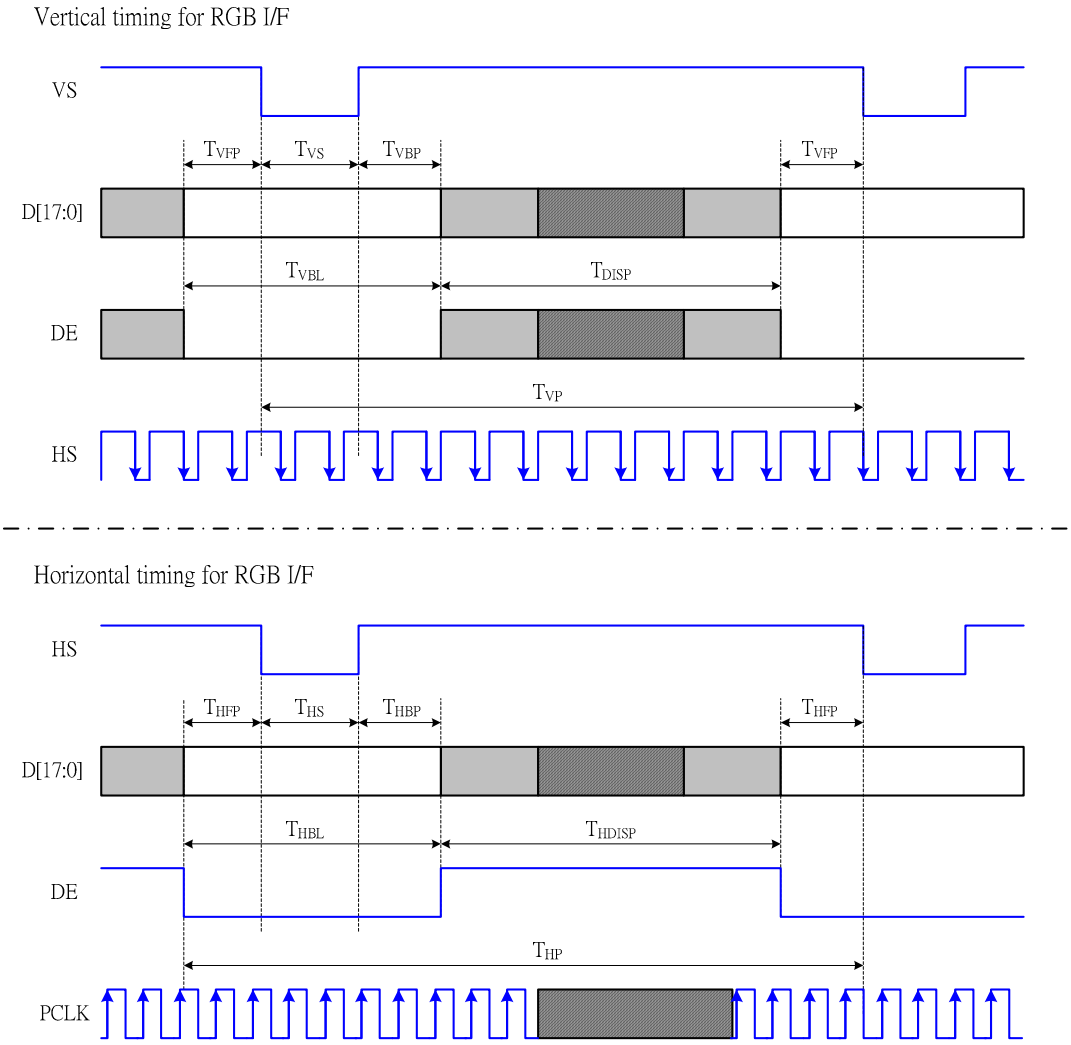


Fig. 9.9.9 Vertical and horizontal timing of RGB interface

Table 9.9.6.2 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	-	226		230	HS
Vertical low pulse width	T_{VS}		2		4	HS
Vertical front porch	T_{VFP}		2		4	HS
Vertical back porch	T_{VBP}		2		4	HS
Vertical data start line		$T_{VS} + T_{VBP}$	4		8	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	6		10	HS
Vertical active area	T_{VDISP}	-		220		HS
Vertical refresh rate	T_{VRR}	Frame rate	57	60	63	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	208		512	PCLK
Horizontal low pulse width	T_{HS}		2		256	PCLK
Horizontal front porch	T_{HFP}		2		256	PCLK
Horizontal back porch	T_{HBP}		2		256	PCLK
Horizontal data start point		$T_{HS} + T_{HBP}$	30		256	PCLK
		$ff_{HS} + f_{HBP}$	1.0			us
Horizontal blanking period	T_{HBL}		32		256	PCLK
Horizontal active area	T_{HDISP}	-		176		PCLK
Pixel clock cycle	$T_{PCLKCYC}$	TVRR=60Hz	2.27		355	ns
	$f_{PCLKCYC}$		100		10	MHz

Note 1. VDDI=1.6 to 3.0V, VDD=2.7 to 3.0V, AGND=DGND=0V, Ta=-30 to 70℃
Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.
Note 3. HP is multiples of eight PCLK.

9.9.6.3 RGB Interface Mode 2 Timing Diagram

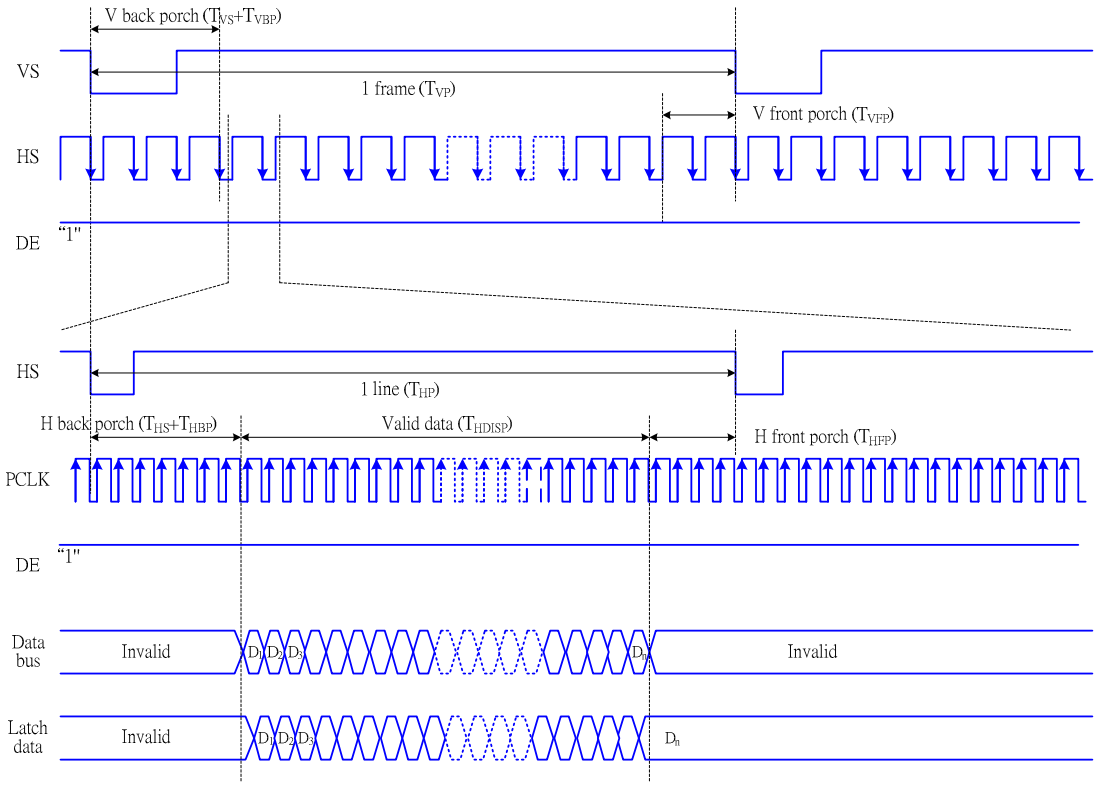


Fig. 9.9.10 RGB mode 2 timing diagram

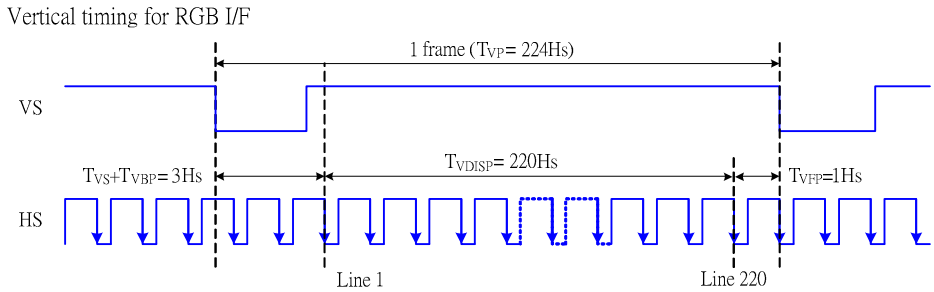


Fig. 9.9.11 RGB mode 2 vertical timing diagram

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

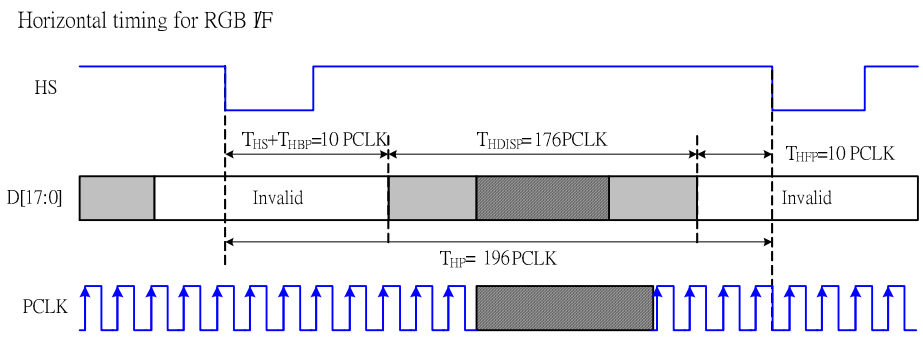


Fig. 9.9.12 RGB mode 2

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

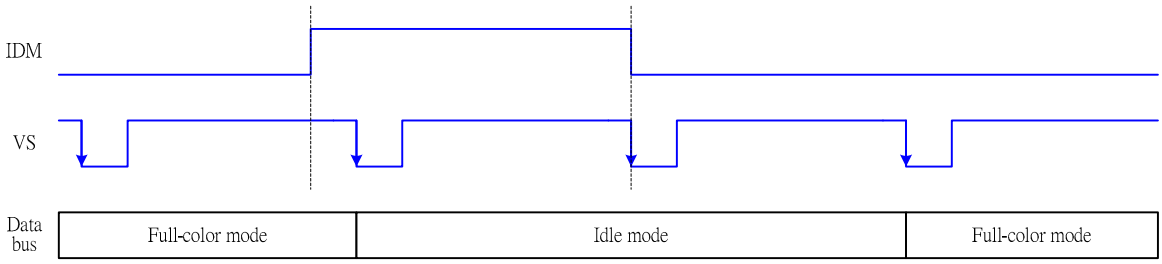


Fig. 9.9.13 RGB mode 2 idle mode timing diadram

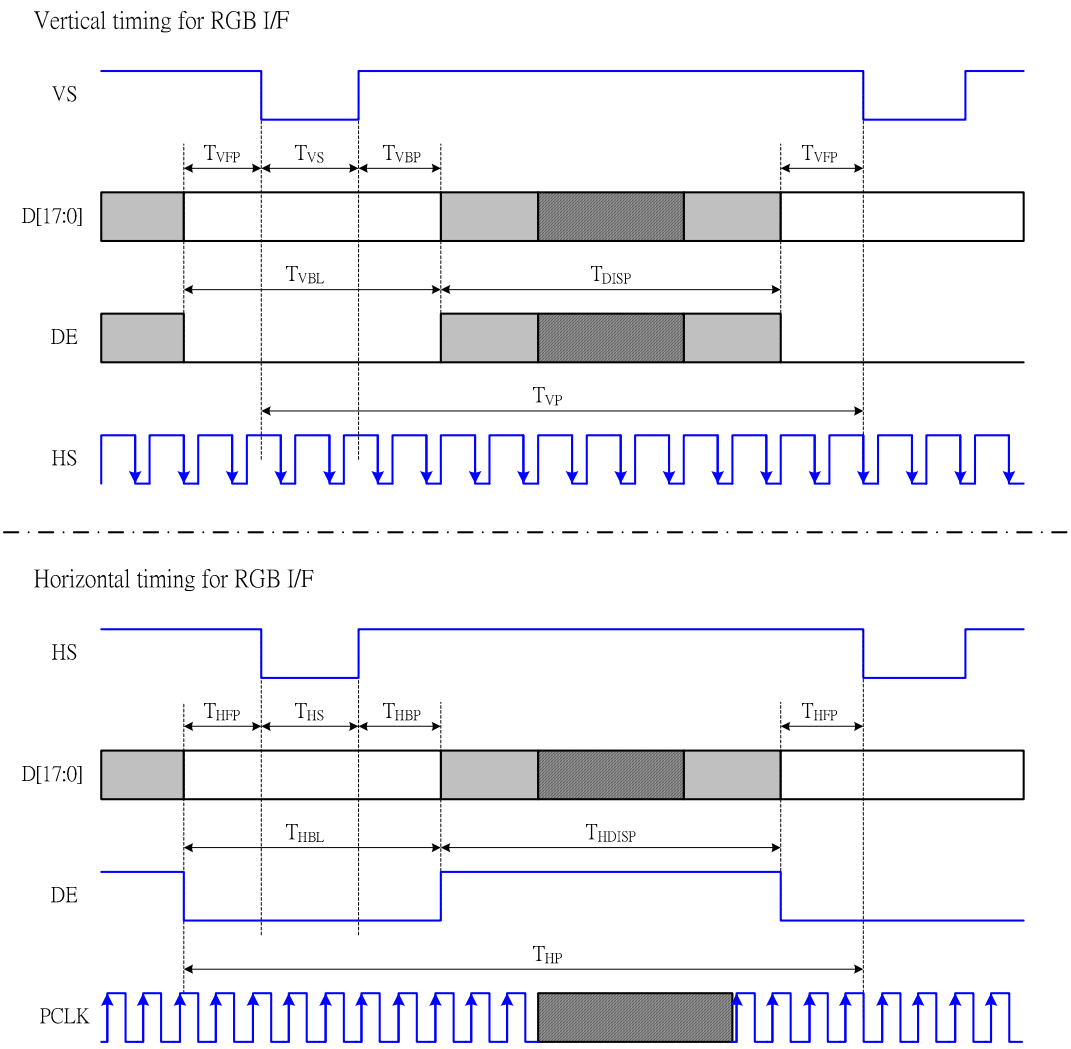


Fig. 9.9.14 Vertical and Horizontal in RGB interface

Table 9.9.6.3 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	-	223	224		HS
Vertical low pulse width	T_{VS}		1		4	HS
Vertical front porch	T_{VFP}		1	1	1023	HS
Vertical back porch	T_{VBP}		1		1023	HS
Vertical data start line		$T_{VS} + T_{VBP}$	2	3	1023	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	3	4	1023	HS
Vertical active area	T_{VDISP}	-		220		HS
Vertical refresh rate	TVRR	Frame rate	57	60	63	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	179	196	511	PCLK
Horizontal low pulse width	T_{HS}		1		63	PCLK
Horizontal front porch	T_{HFP}		1		63	PCLK
Horizontal back porch	T_{HBP}		1		63	PCLK
Horizontal data start point		$T_{HS} + T_{HBP}$	2	10	63	PCLK
		$ff_{HS} + f_{HBP}$	TBD			us
Horizontal blanking period	T_{HBL}		3	20	256	PCLK
Horizontal active area	T_{HDISP}	-		176		PCLK
Pixel clock cycle	$T_{PCLKCYC}$	-	100	380	418	ns
	$f_{PCLKCYC}$		2.40	2.63	10	MHz

Note 1. VDDI=1.6 to 3.0V, VDD=2.7 to 3.0V, AGND=DGND=0V, Ta=-30 to 70℃
Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.
Note 3. HP is multiples of eight PCLK.

9.9.6.4 Power On Sequence on RGB Mode 2

The Driver operates power up and display ON by VDD, VDDI, SHUT, VS, HS, DE, PCLK on RGB mode 2 as show as following figure.

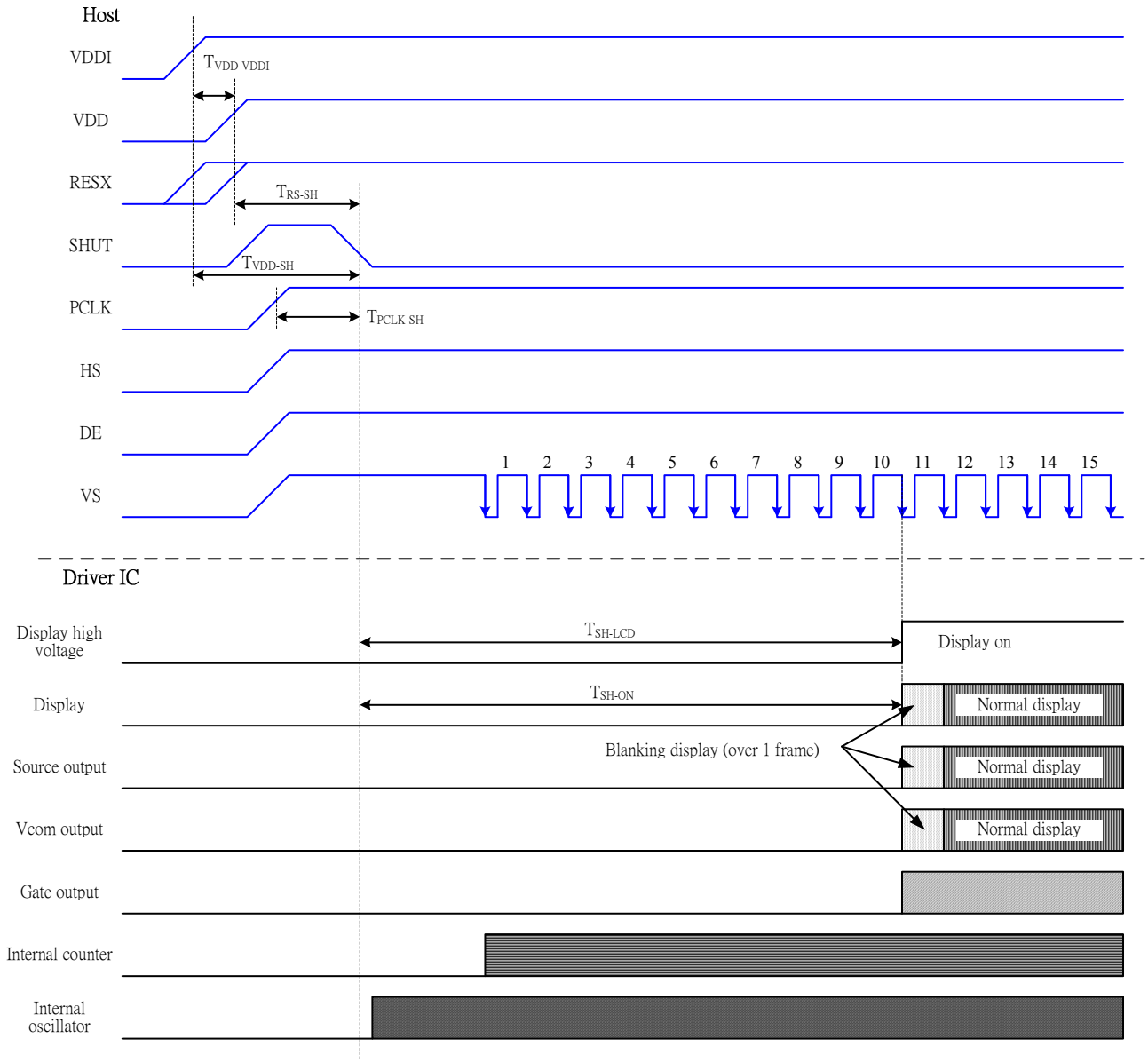


Fig. 9.9.15 Power-ON sequence in RGB mode 2

Table 9.9.6.4 Power ON AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	TVDDI-VDD	0			ns	Note1
VDDI/VDD on to falling edge of SHUT	TVDD-SH	1			ms	
RESX to falling of SHUT	TRS-SH	10			us	
Signals input to falling edge of SHUT *	TCLK-SH	1			PCLK	Note2
Falling edge of SHUT to LCD power ON	TSH-LCD			120	ms	
Falling edge of SHUT to Display start	TSH-ON		10		VS	

Note 1: TVDDI-VDD can be <=0ns, >0ns. In any case, VDDI and VDD power up sequence should not have any impact on the driver / display functionalities / performance.
Note 2: Signals mean VS, HS, DE and PCLK signal.
Note 3: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

9.9.6.5 Power OFF Sequence on RGB Mode 2

The Driver operates power off and display OFF by VDD, VDDI, SHUT, VS, HS and DE on RGB mode 2 as show as following figure.

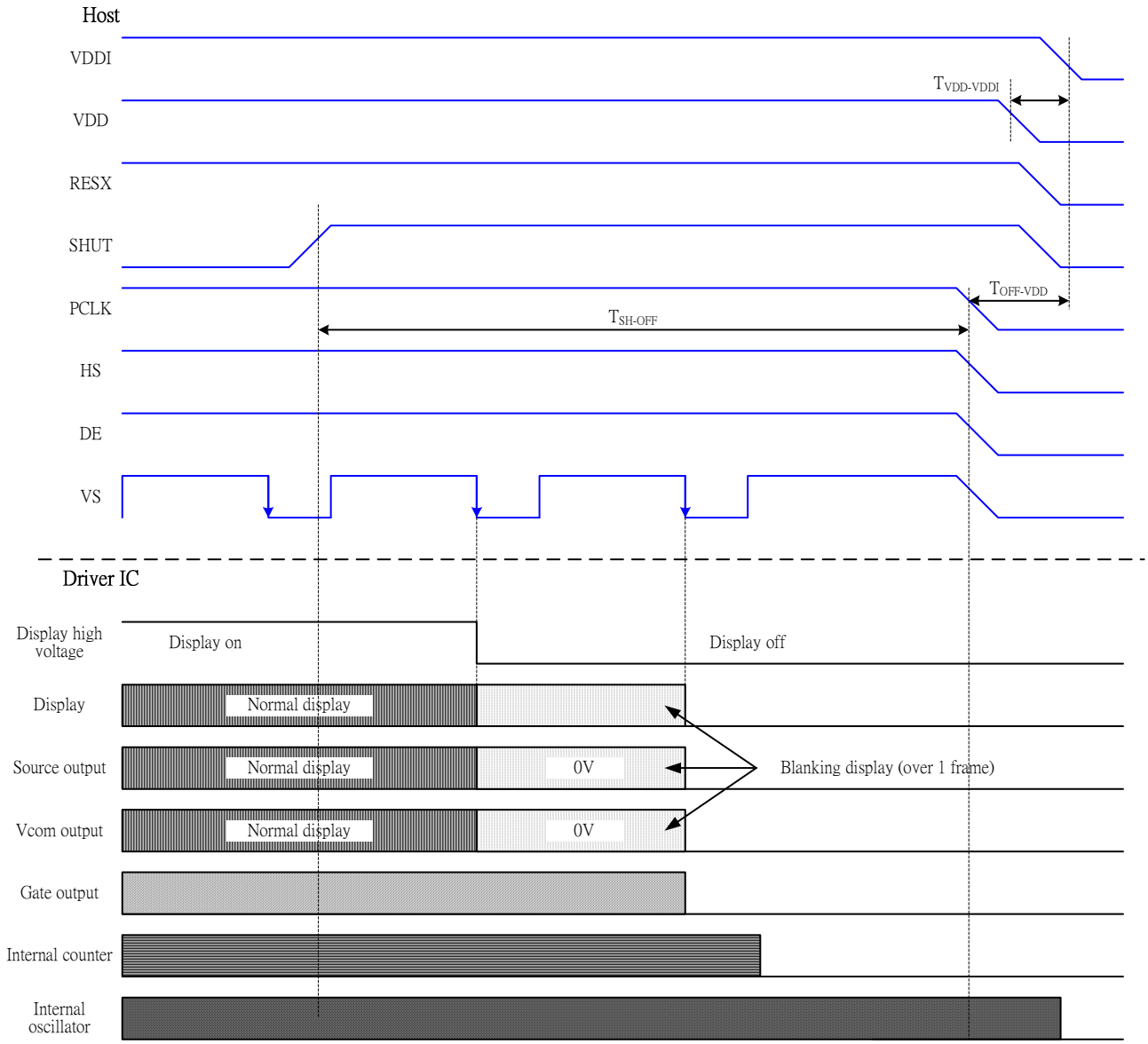


Fig. 9.9.16 Power-OFF seqnence in RGB mode 2

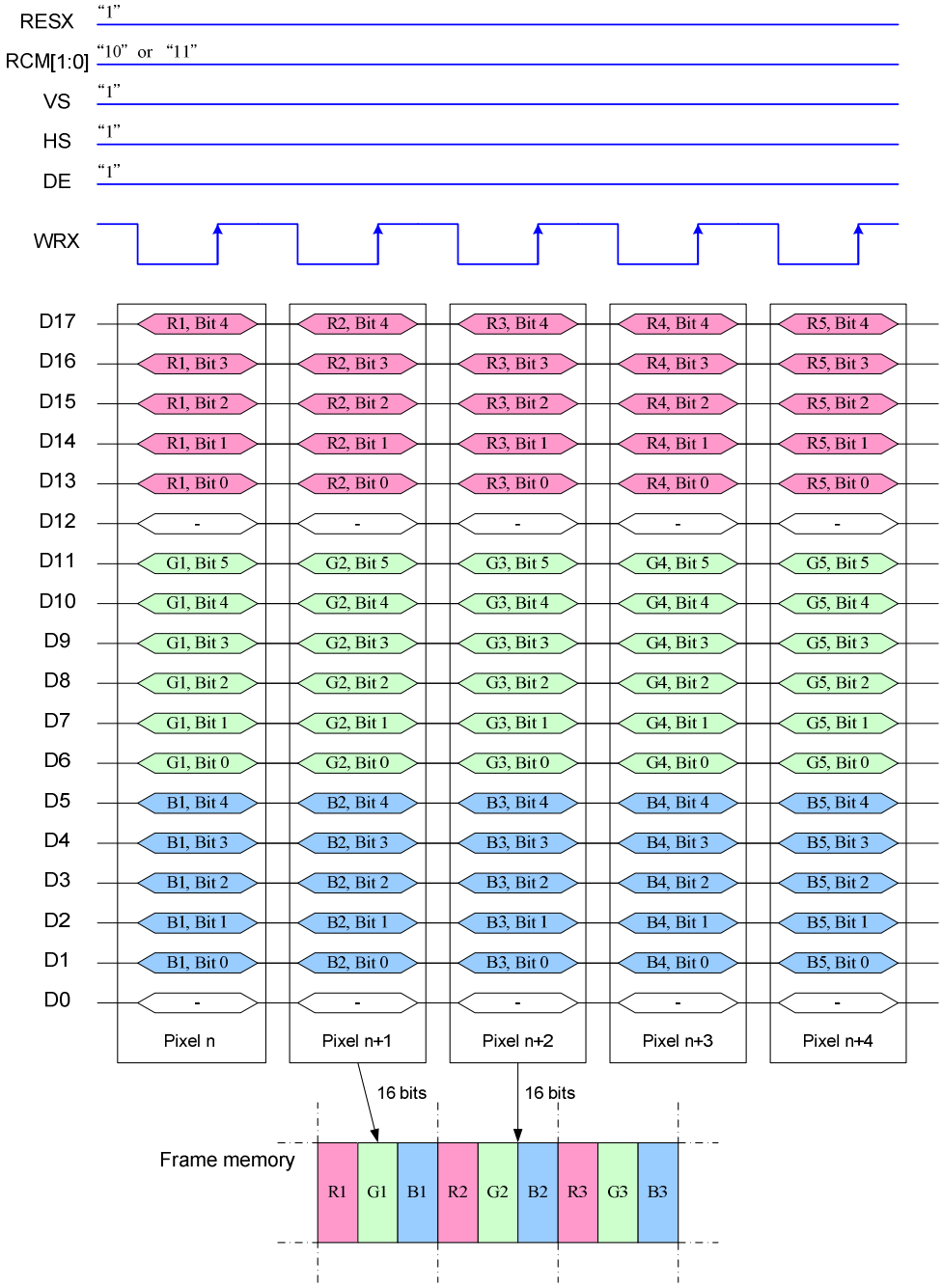
Table 9.9.6.5 Power OFF AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDI On to VDD On	TVDDI-VDD	0			ns	Note1
Signals input to VDDI/VDD off	TSH-OFF	1			us	Note2
Rising edge of SHUT to Display off	TSH-OFF	2			VS	

Note 1: TVDDI-VDD can be <=0ns, >0ns. In any case, VDDI and VDD power up sequence should not have any impact on the driver / display functionalities / performance.
Note 2: Signals mean VS, HS, DE and PCLK signal.
Note 3: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

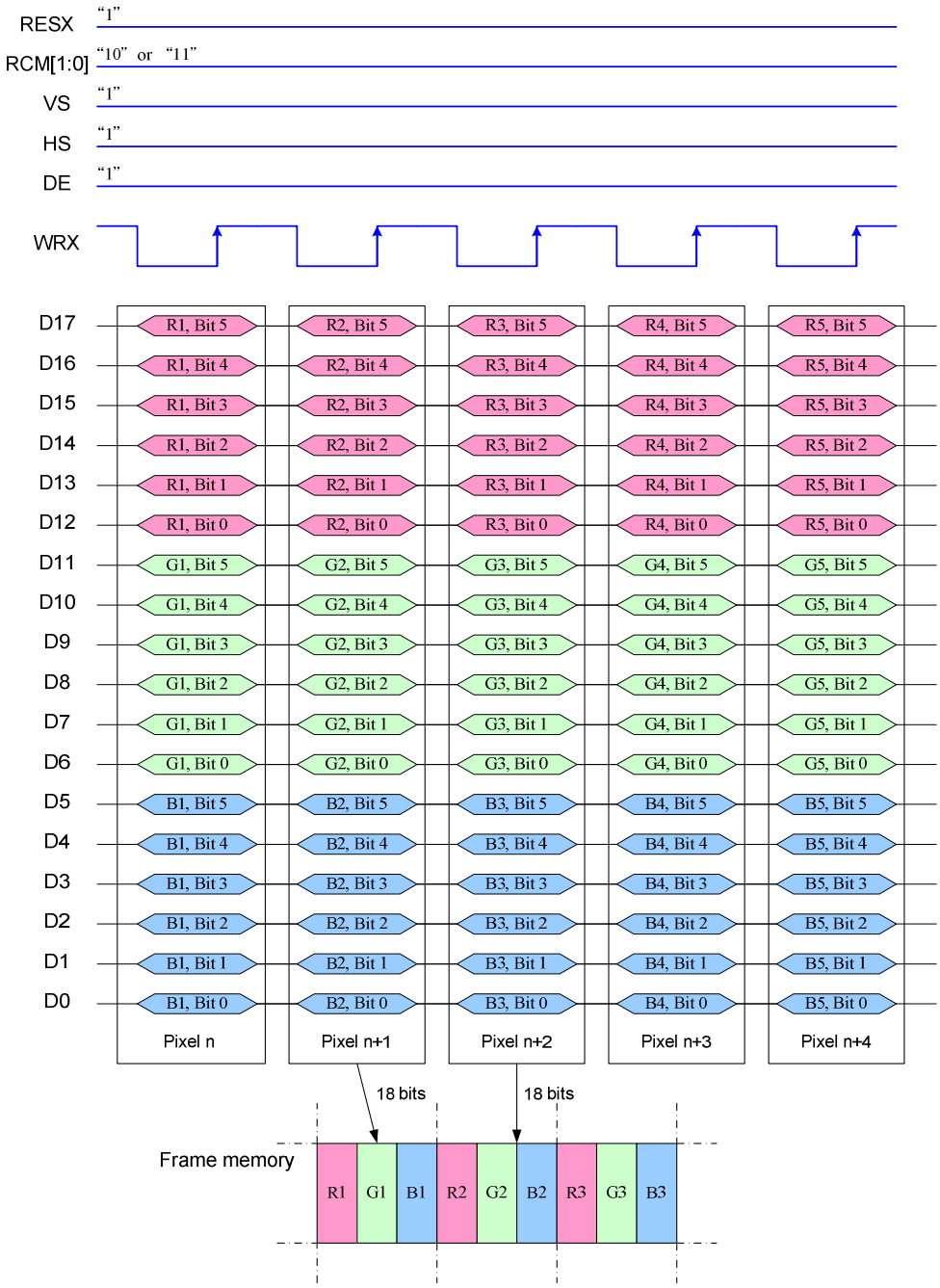
9.9.7 RGB Data Color Coding

9.9.7.1 16-bit/pixel Color Order on the RGB Interface



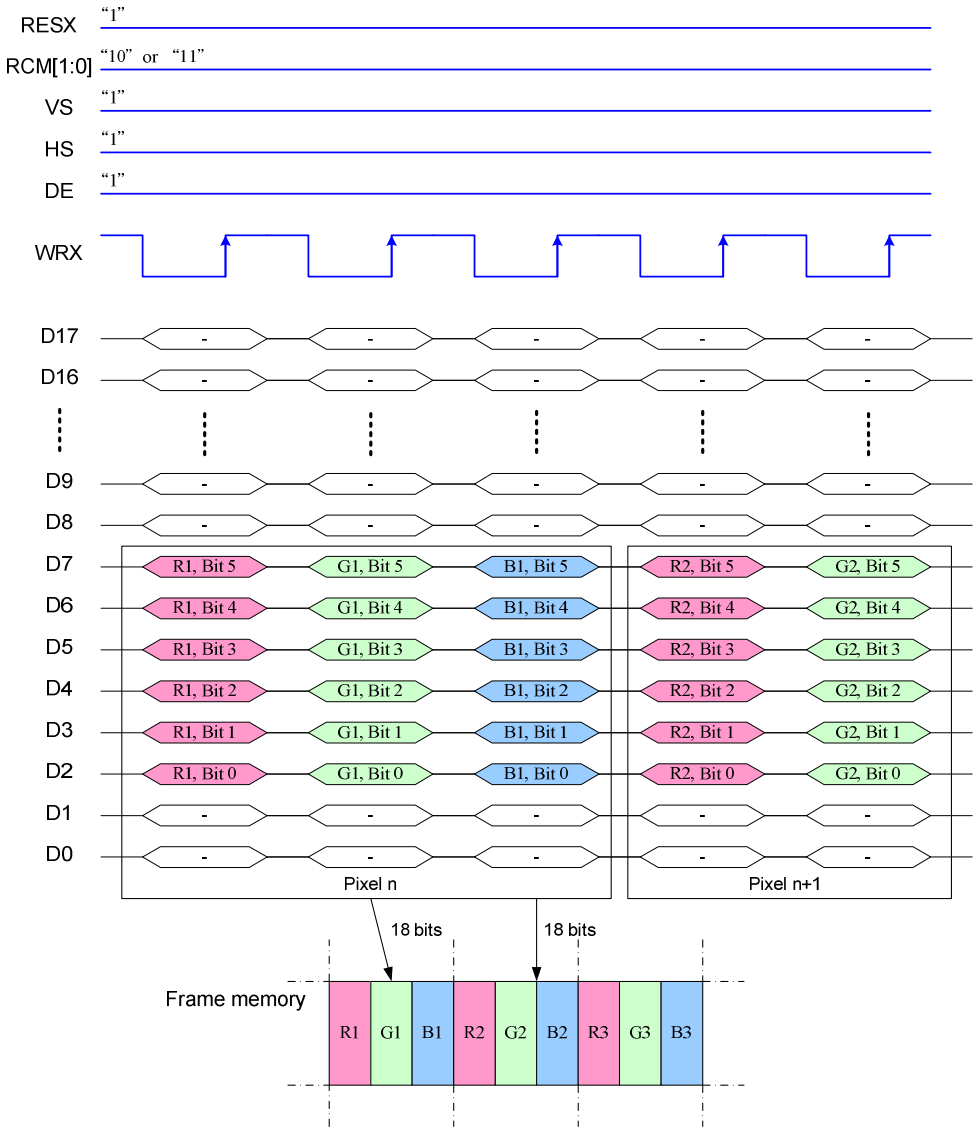
Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.
Note 2: '-' Don't care, but need set to VDDI or DGND level.

9.9.7.2 18-bit/pixel Color Order on the RGB Interface



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.
Note 2: '-' Don't care, but need set to VDDI or DGND level.

9.9.7.3 6-bit/pixel Color Order on the RGB Interface



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.
Note 2: '-' Don't care, but need set to VDDI or DGND level.

9.10 Display Data RAM

9.10.1 Configuration (When GM="00")

The display module has an integrated 176x220x18-bit graphic type static RAM. This 696,960-bit memory allows to store on-chip a 176xRGBx220 image with an 18-bpp resolution (262K-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

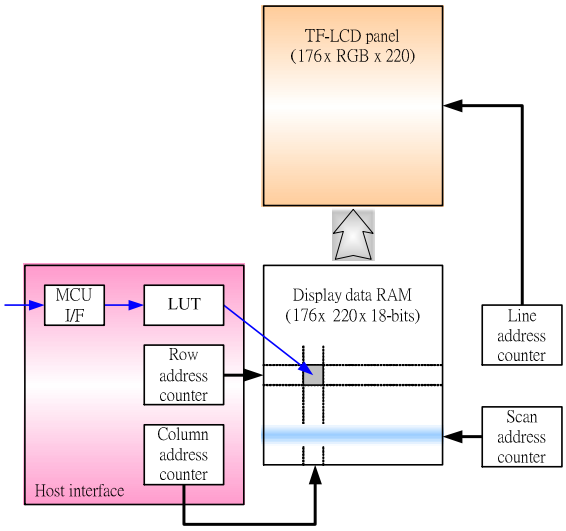


Fig. 9.10.1 Display data RAM organization

9.10.2 Memory to Display Address Mapping

			Pixel 1			Pixel 2			--------	Pixel 175			Pixel 176				
Gate Out	Source Out		S1	S2	S3	S4	S5	S6	--------	S523	S524	S525	S526	S527	S528		
	RA		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=' 0 '	MY=' 1 '														ML=' 0 '	ML=' 1 '
1	0	219	R0	G0	B0	R1	G1	B1	--------	R174	G174	B174	R175	G175	B175	0	219
2	1	218							--------							1	218
3	2	217							--------							2	217
4	3	216							--------							3	216
5	4	215							--------							4	215
6	5	214							--------							5	214
7	6	213							--------							6	213
8	7	212							--------							7	212
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
213	212	7							--------							212	7
214	213	6							--------							213	6
215	214	5							--------							214	5
216	215	4							--------							215	4
217	216	3							--------							216	3
218	217	2							--------							217	2
219	218	1							--------							218	1
220	219	0							--------							219	0
	CA	MX=' 0 '	0			1			--------	174			175				
		MX=' 1 '	175			174			--------	1			0				

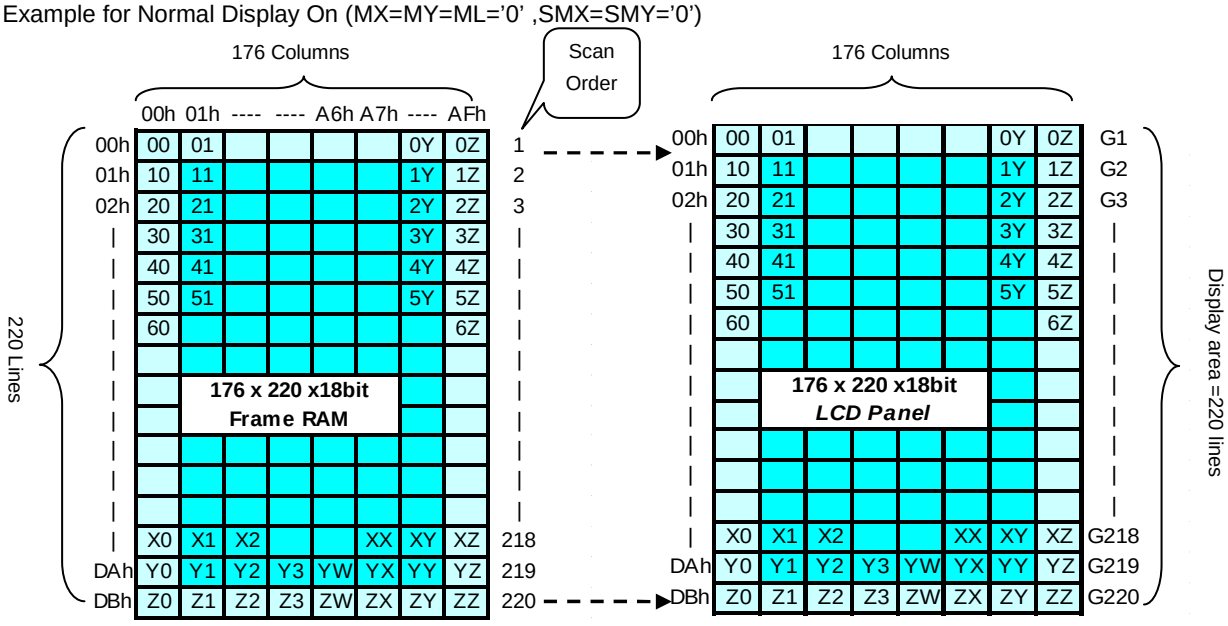
Note
RA = Row Address,
CA = Column Address
SA = Scan Address
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
MX =Scan direction parameter, D4 parameter of MADCTL command
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

9.10.3 Normal Display On or Partial Mode On, Vertical Scroll Off

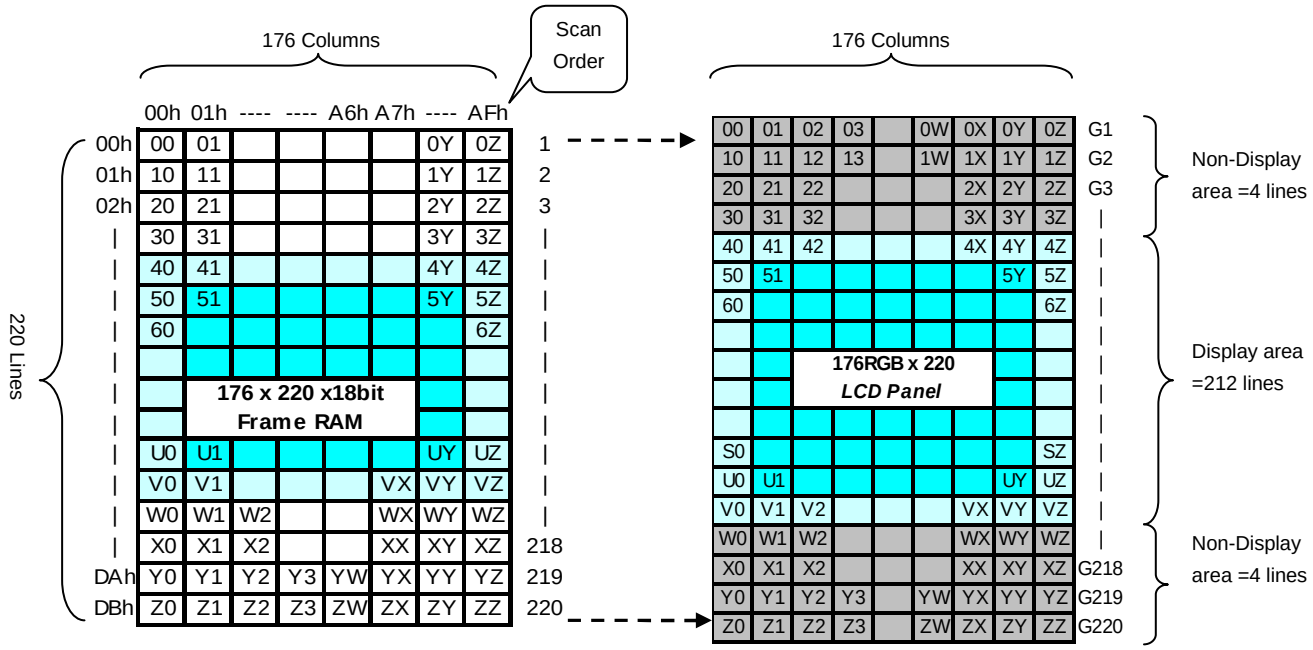
In this mode, contents of the frame memory within an area where column pointer is 00h to AFh and page pointer is 00h to DBh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML='0' ,SMX=SMY='0')



2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=D7h, MX=MV=ML='0' ,SMX=SMY='0')



9.10.4 Vertical Scroll Mode

There is vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and Vertical Scrolling Start Address” (37h).

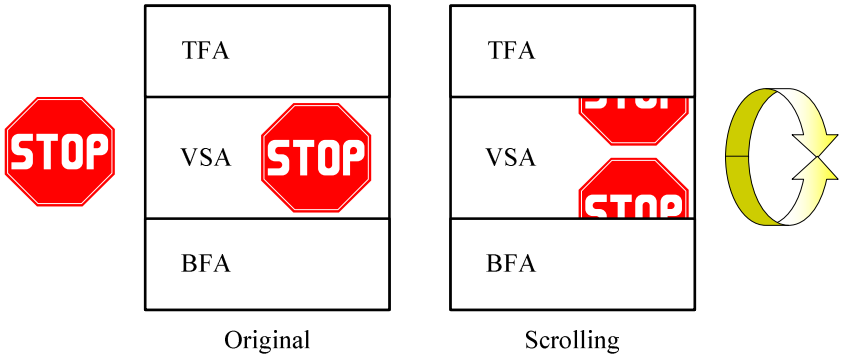
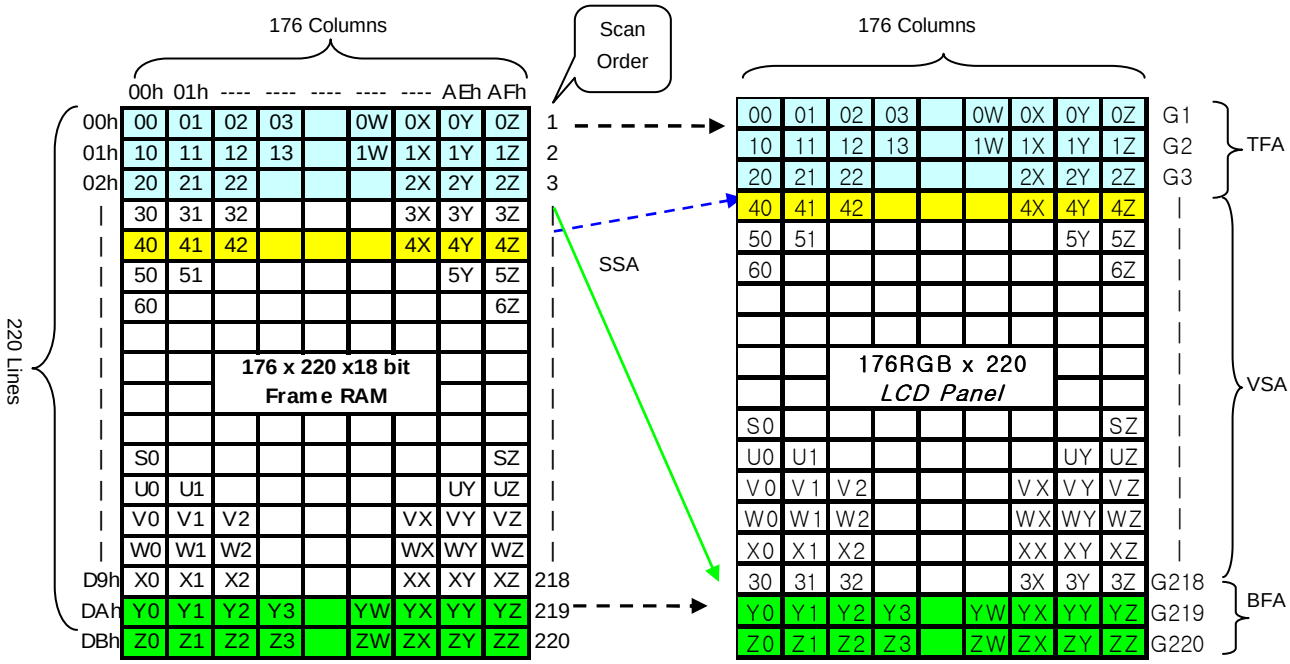


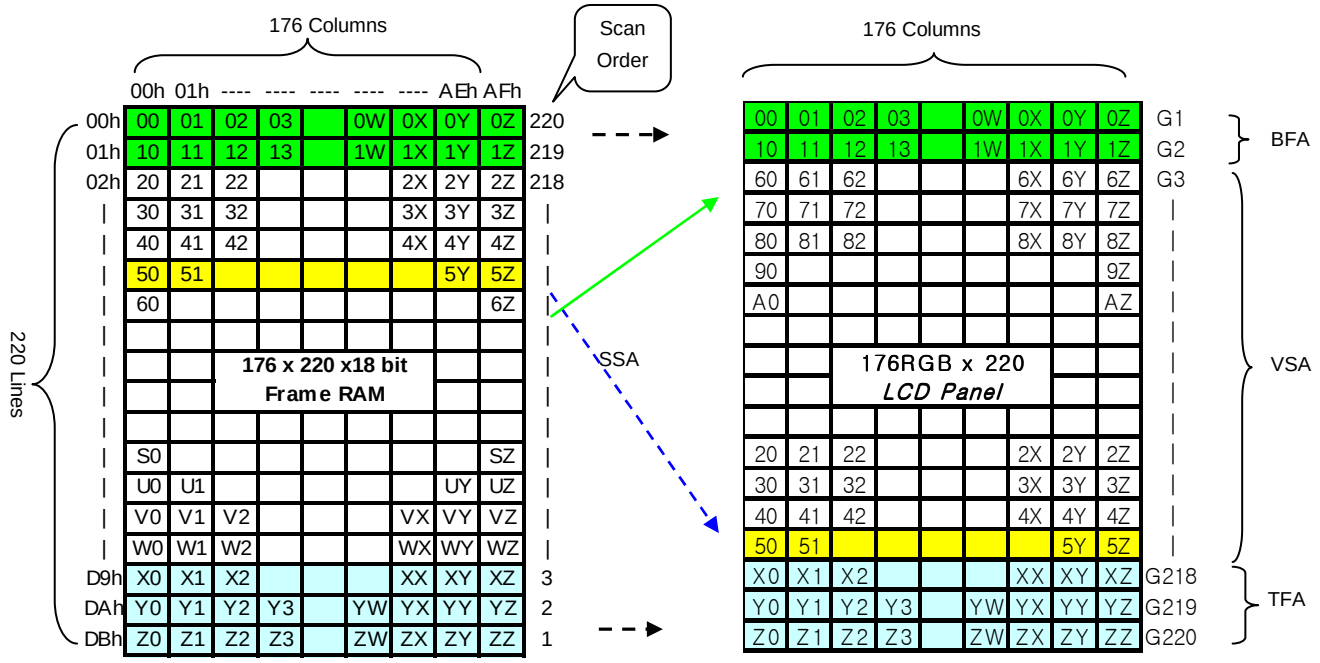
Fig. 9.10.2 Difference between Scrolling and original

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=220. In this case, scrolling is applied as shown below.

1). Example for TFA =3, VSA=215, BFA=2, SSA=4, ML=0: Scrolling



2). Example for TFA =3, VSA=215, BFA=2, SSA=215, ML=1: Scrolling: TFA and BFT are exchanged

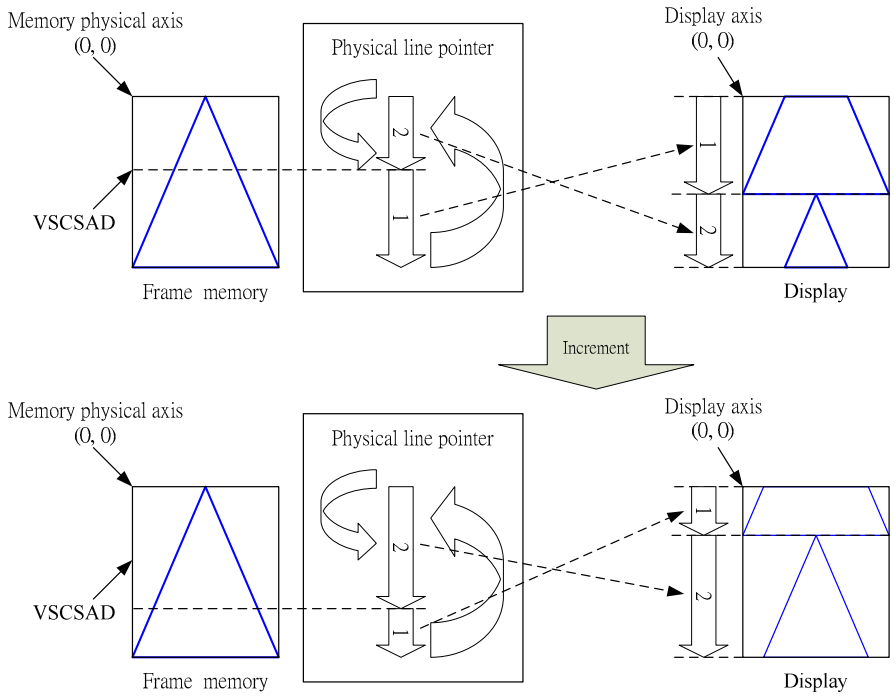


9.10.5 Vertical Scroll Example

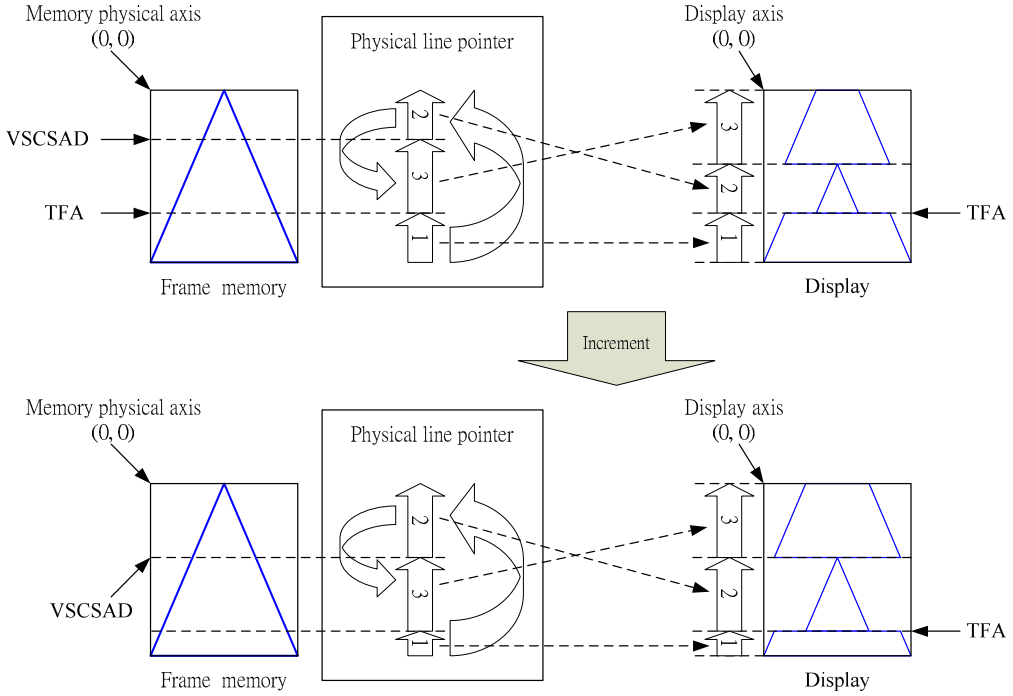
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA≠220
N/A. Do not set TFA + VSA + BFA≠220. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=220 (Scrolling)
Example1) When MADCTL parameter ML=”0”, TFA=0, VSA=220, BFA=0 and VSCSAD=80.



Example2) When MADCTL parameter ML=”1”, TFA=30, VSA=190, BFA=0 and VSCSAD=80.



9.11 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.
Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=175 (AFh) and Y=0 to Y=219 (DBh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=175(AFh), YE=219 (DBh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTL" (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.12 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.12 below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

9.12. Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

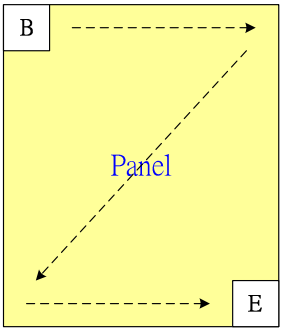
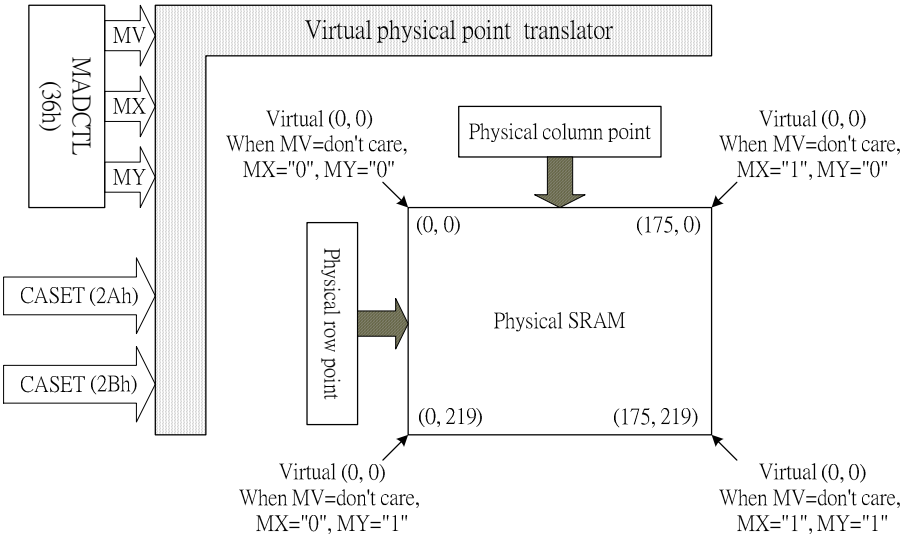


Fig. 9.12.1 Data streaming order



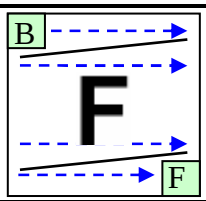
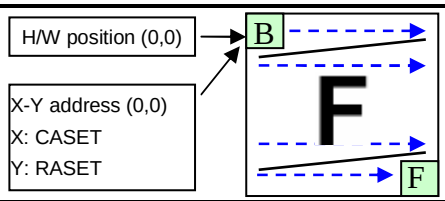
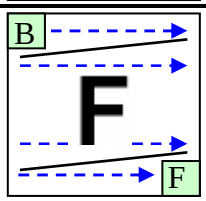
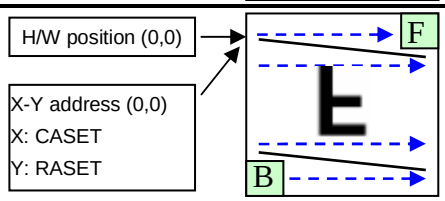
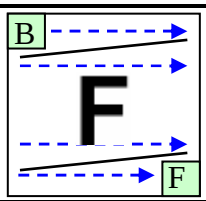
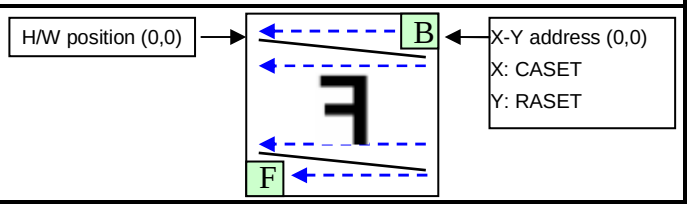
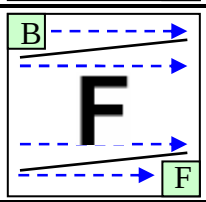
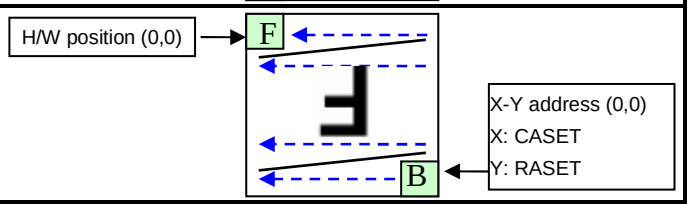
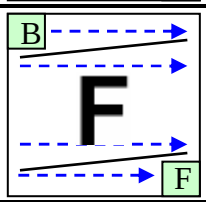
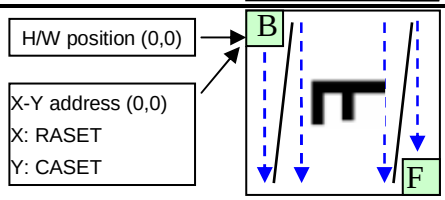
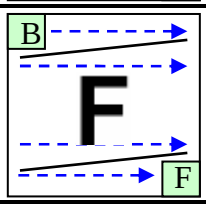
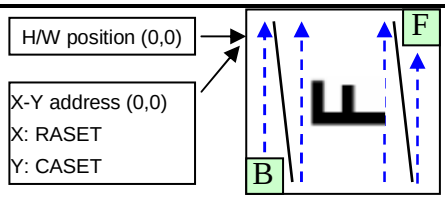
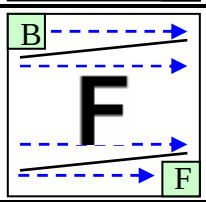
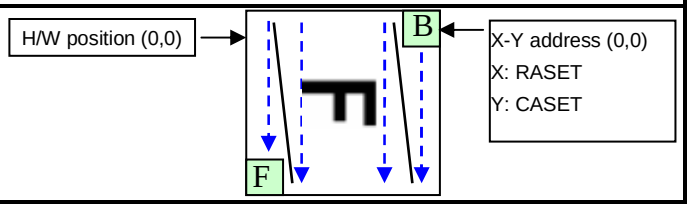
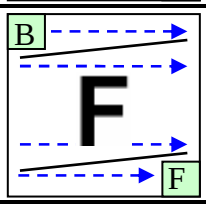
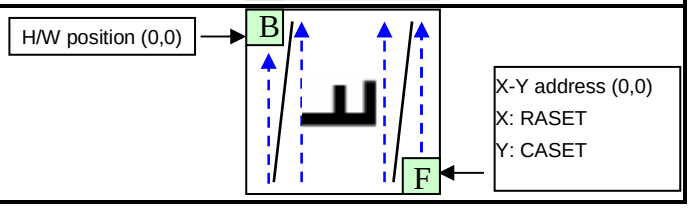
MV	MX	MV	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (219-Physical Row Pointer)
0	1	0	Direct to (175-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (175-Physical Column Pointer)	Direct to (219-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (219-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (175-Physical Column Pointer)
1	1	1	Direct to (219-Physical Row Pointer)	Direct to (175-Physical Column Pointer)

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

9.12.2 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

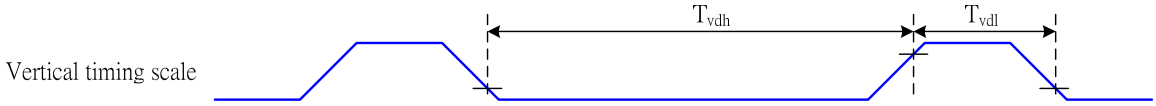
Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

9.13 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

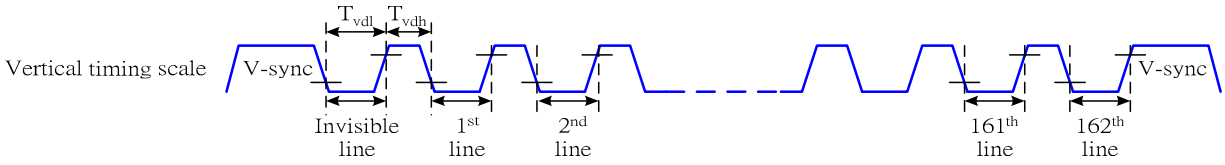
9.13.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

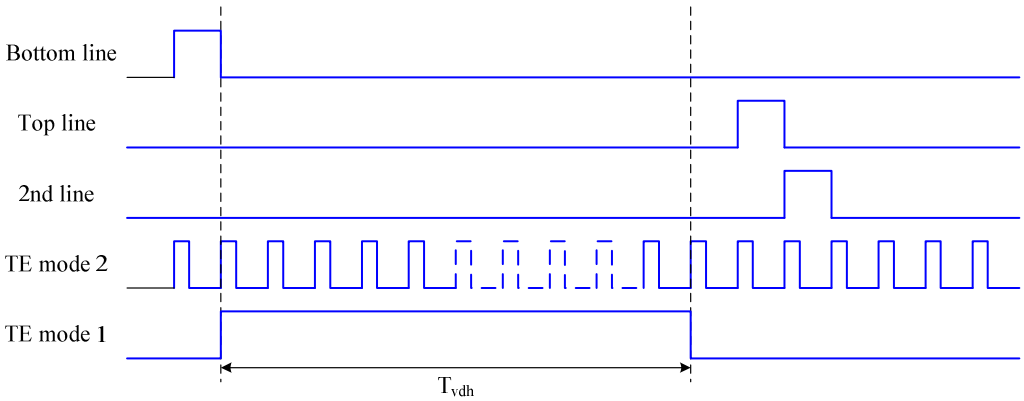


tvdh= The LCD display is not updated from the Frame Memory
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 220 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

9.13.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

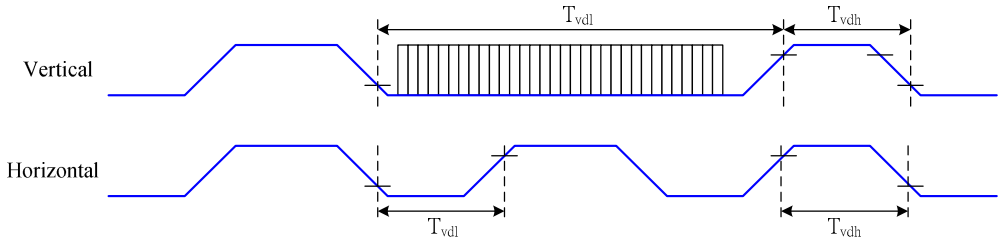
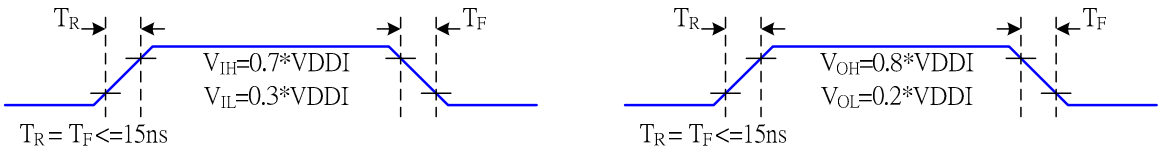


Table 9.13.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 58.9 Hz)

Symbol	Parameter	min	max	unit	description
t_{vdl}	Vertical Timing Low Duration	13	-	ms	
t_{vdh}	Vertical Timing High Duration	1000	-	μs	
t_{hdl}	Horizontal Timing Low Duration	33	-	μs	
t_{hdh}	Horizontal Timing Low Duration	25	500	μs	

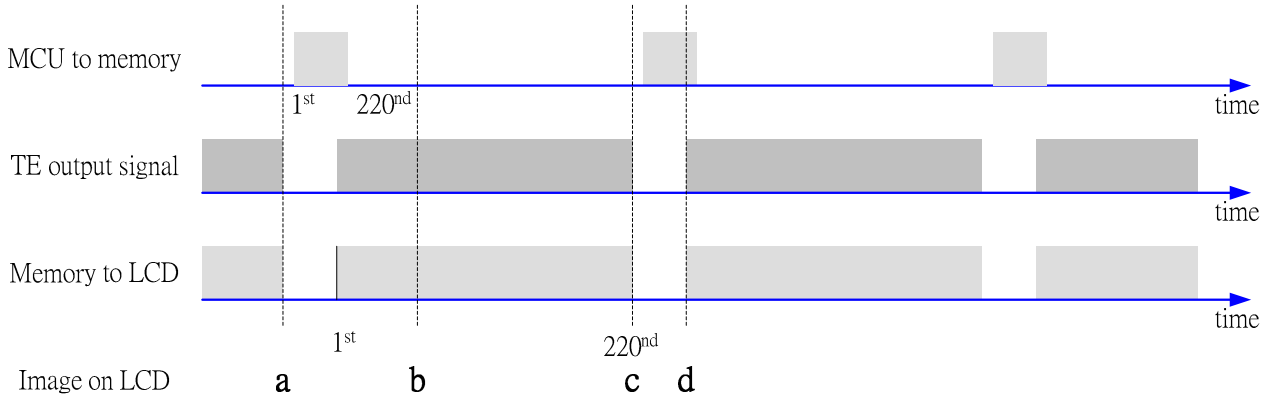
NOTE: The timings in Table 9.3.1 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

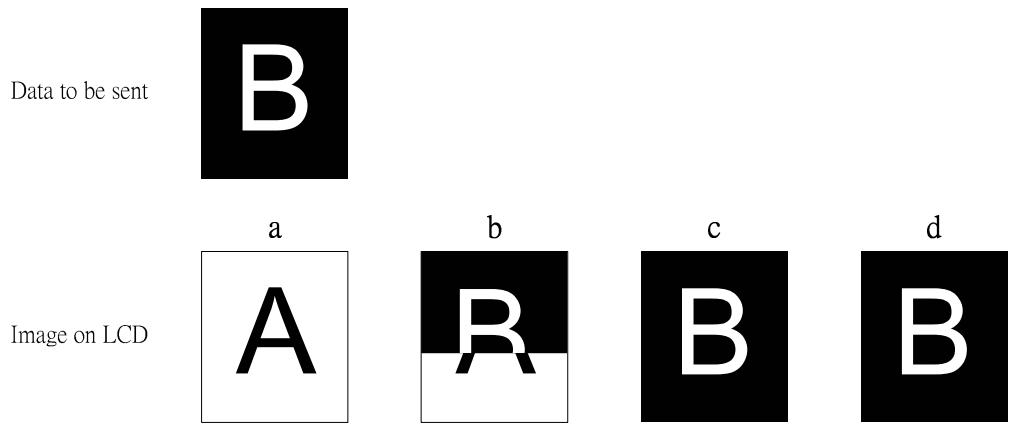


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

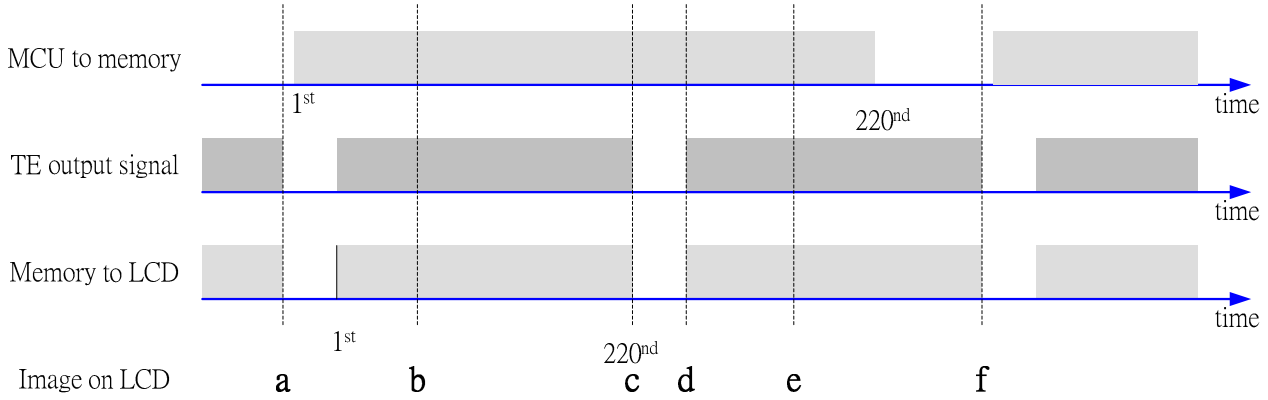
9.13.3 Example 1: MPU Write is faster than panel read



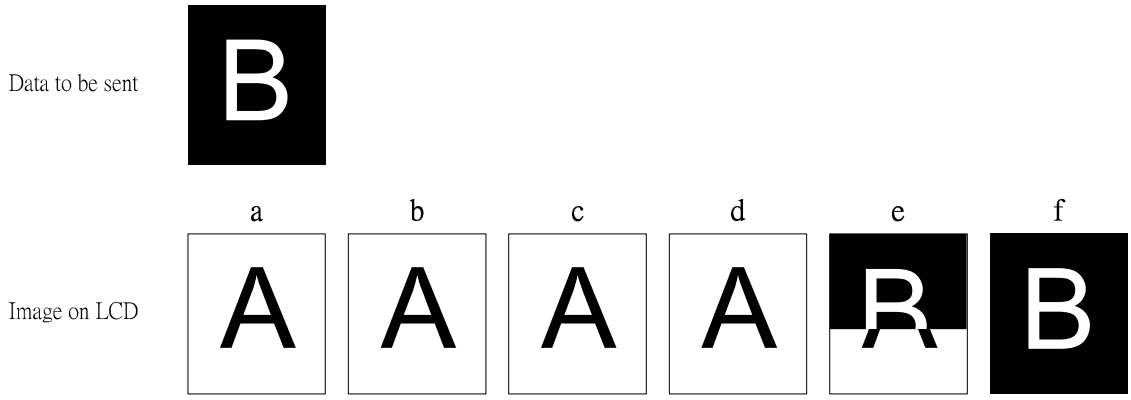
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



9.13.4 Example 2: MPU write is slower than panel read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



9.14 Preset Values

ST7773 will set preset values on our production line for each display module. Any of these preset values do not need customer's SW support.

9.15 Power ON/OFF Sequence

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

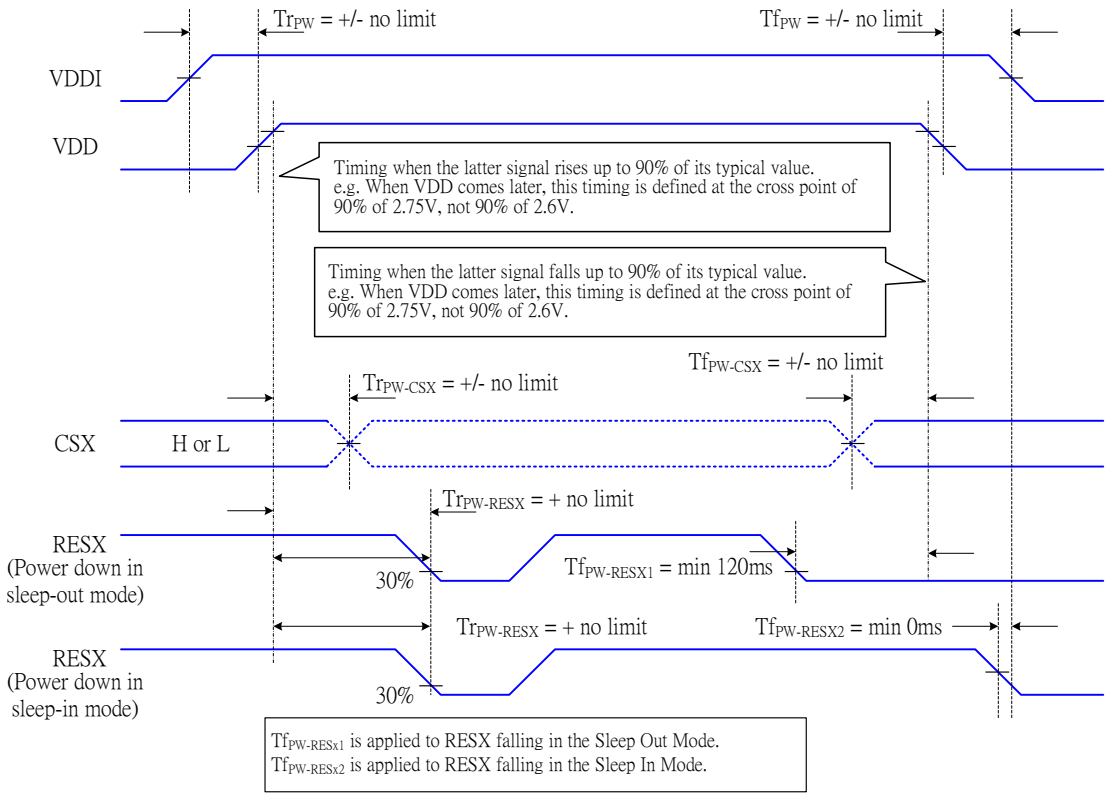
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 9.15.1 and 9.15.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

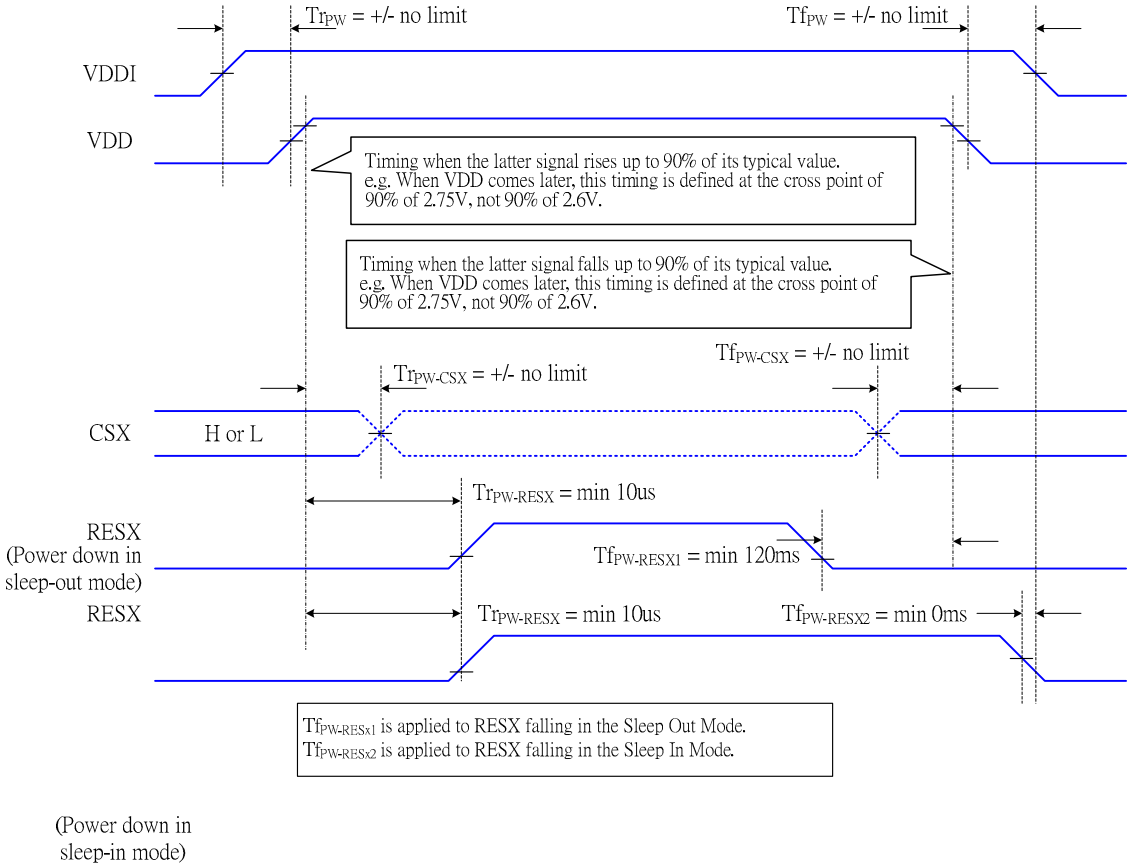
9.15.1 Case 1 – RESX Line is held High or Unstable by Host at Power On

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



9.15.2 Case 2 – RESX Line is Held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10sec after both VDD and VDDI have been applied.



9.15.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

2. At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

9.16 Power Level Definition

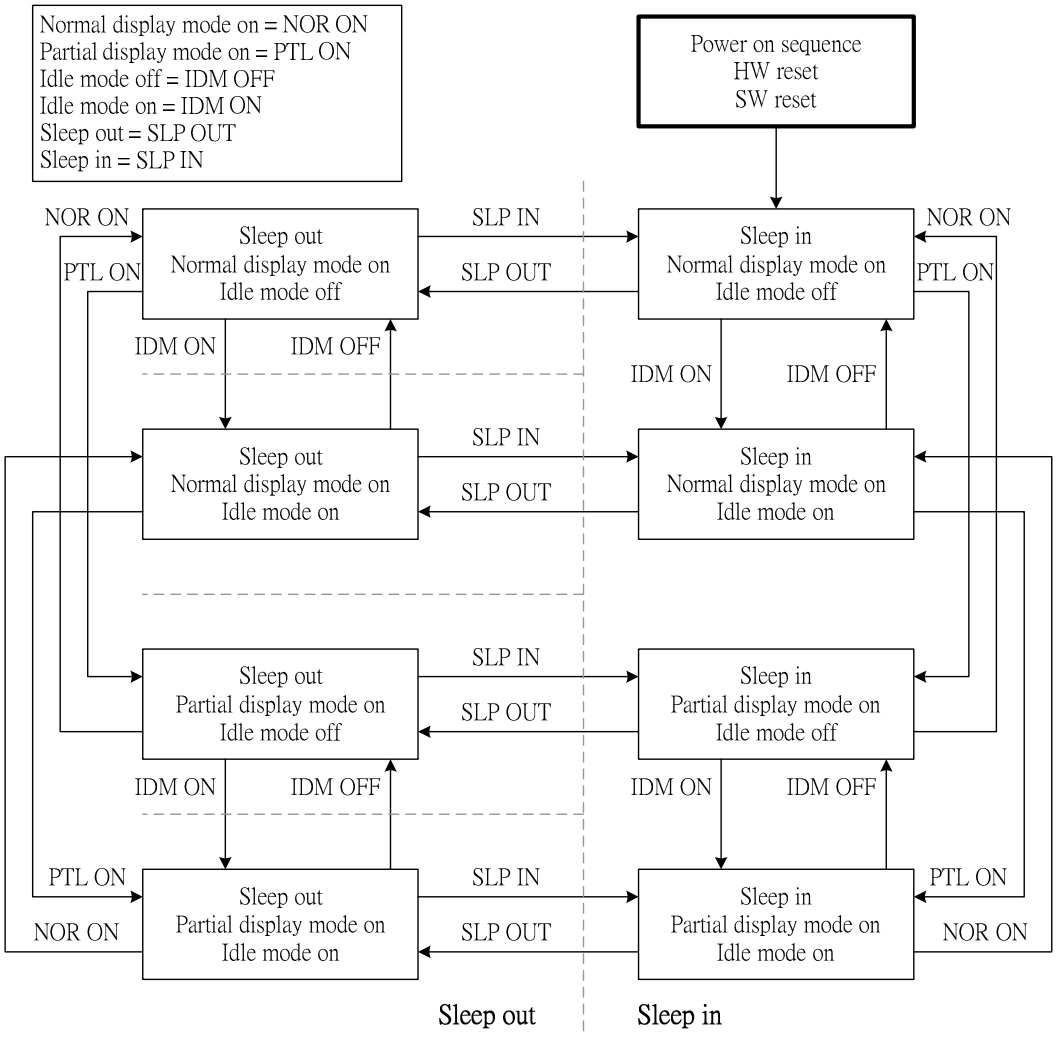
9.16.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode
In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode
In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

9.16.2 Power Flow Chart



9.17 Reset Table

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	00AFh	00AFh	00AFh (175d) (when MV=0) 00DBh (219d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00DBh	00DBh	00DBh (219d) (when MV=0) 00AFh (175d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 9.19	See Section 9.19	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00DBh	00DBh	00DBh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00DCh	00DCh	00DCh
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note1. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

9.18.1 Module Input/Output Pins

9.18.1.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

9.18.1.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 9.15	Input valid	Input valid	Input valid	See 9.15
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D17 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid
P/SX	Input invalid	Input valid	Input valid	Input valid	Input invalid

9.18.2 Reset Timing

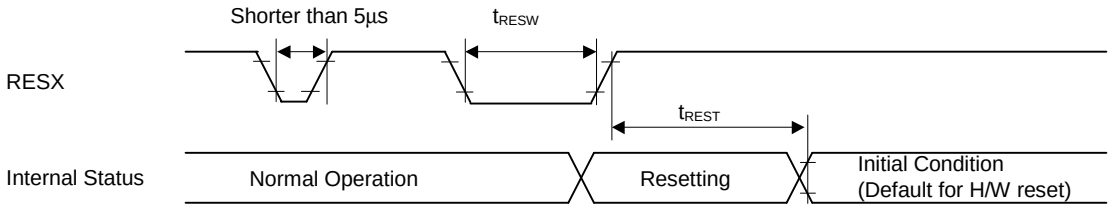


Table 9.18.2.1 Reset input timing
VSS=0V, VDDI=1.6 to 3.6V, VDD=2.7 to 3.5V, Ta = -30 to 70℃)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	s
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

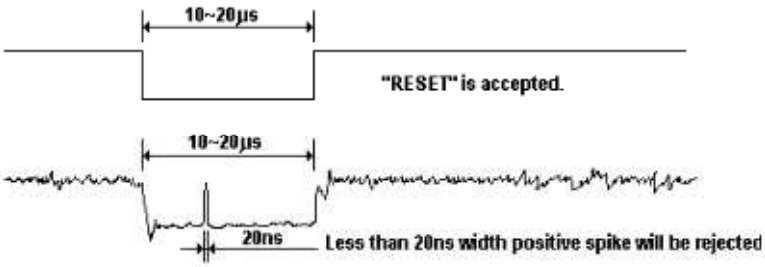
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID2 and VCOMOF value in MTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9.19 Color Depth Conversion Look Up Tables

9.19.1 65536 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
RED	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	000000	1	00000
	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	000010	2	00001
	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	000100	3	00010
	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	000110	4	00011
	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	001000	5	00100
	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	001010	6	00101
	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	001100	7	00110
	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	001110	8	00111
	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	010000	9	01000
	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	010010	10	01001
	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	010100	11	01010
	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	010110	12	01011
	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	011000	13	01100
	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	011010	14	01101
	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	011100	15	01110
	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	011110	16	01111
	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	100001	17	10000
	R_{175} R_{174} R_{173} R_{172} R_{171} R_{170}	100011	18	10001
	R_{185} R_{184} R_{183} R_{182} R_{181} R_{180}	100101	19	10010
	R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}	100111	20	10011
	R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}	101001	21	10100
	R_{215} R_{214} R_{213} R_{212} R_{211} R_{210}	101011	22	10101
	R_{225} R_{224} R_{223} R_{222} R_{221} R_{220}	101101	23	10110
	R_{235} R_{234} R_{233} R_{232} R_{231} R_{230}	101111	24	10111
	R_{245} R_{244} R_{243} R_{242} R_{241} R_{240}	110001	25	11000
	R_{255} R_{254} R_{253} R_{252} R_{251} R_{250}	110011	26	11001
	R_{265} R_{264} R_{263} R_{262} R_{261} R_{260}	110101	27	11010
	R_{275} R_{274} R_{273} R_{272} R_{271} R_{270}	110111	28	11011
	R_{285} R_{284} R_{283} R_{282} R_{281} R_{280}	111001	29	11100
	R_{295} R_{294} R_{293} R_{292} R_{291} R_{290}	111011	30	11101
	R_{305} R_{304} R_{303} R_{302} R_{301} R_{300}	111101	31	11110
	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	111111	32	11111

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
GREEN	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	000000	33	000000
	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	000001	34	000001
	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	000010	35	000010
	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	000011	36	000011
	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	000100	37	000100
	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	000101	38	000101
	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	000110	39	000110
	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	000111	40	000111
	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	001000	41	001000
	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	001001	42	001001
	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	001010	43	001010
	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	001011	44	001011
	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	001100	45	001100
	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	001101	46	001101
	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	001110	47	001110
	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	001111	48	001111
	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	010000	49	010000
	G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}	010001	50	010001
	G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}	010010	51	010010
	G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}	010011	52	010011
	G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}	010100	53	010100
	G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}	010101	54	010101
	G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}	010110	55	010110
	G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}	010111	56	010111
	G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}	011000	57	011000
	G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}	011001	58	011001
	G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}	011010	59	011010
	G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}	011011	60	011011
	G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}	011100	61	011100
	G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}	011101	62	011101
	G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}	011110	63	011110
	G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}	011111	64	011111

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
GREEN	G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}	100000	65	100000
	G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}	100001	66	100001
	G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}	100010	67	100010
	G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}	100011	68	100011
	G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}	100100	69	100100
	G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}	100101	70	100101
	G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}	100110	71	100110
	G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}	100111	72	100111
	G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}	101000	73	101000
	G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}	101001	74	101001
	G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}	101010	75	101010
	G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}	101011	76	101011
	G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}	101100	77	101100
	G_{455} G_{454} G_{453} G_{452} G_{451} G_{450}	101101	78	101101
	G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}	101110	79	101110
	G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}	101111	80	101111
	G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}	110000	81	110000
	G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}	110001	82	110001
	G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}	110010	83	110010
	G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}	110011	84	110011
	G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}	110100	85	110100
	G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}	110101	86	110101
	G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}	110110	87	110110
	G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}	110111	88	110111
	G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}	111000	89	111000
	G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}	111001	90	111001
	G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}	111010	91	111010
	G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}	111011	92	111011
	G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}	111100	93	111100
	G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}	111101	94	111101
	G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}	111110	95	111110
	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}	111111	96	111111

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
BLUE	B_{005} B_{004} B_{003} B_{002} B_{001} B_{000}	000000	97	00000
	B_{015} B_{014} B_{013} B_{012} B_{011} B_{010}	000010	98	00001
	B_{025} B_{024} B_{023} B_{022} B_{021} B_{020}	000100	99	00010
	B_{035} B_{034} B_{033} B_{032} B_{031} B_{030}	000110	100	00011
	B_{045} B_{044} B_{043} B_{042} B_{041} B_{040}	001000	101	00100
	B_{055} B_{054} B_{053} B_{052} B_{051} B_{050}	001010	102	00101
	B_{065} B_{064} B_{063} B_{062} B_{061} B_{060}	001100	103	00110
	B_{075} B_{074} B_{073} B_{072} B_{071} B_{070}	001110	104	00111
	B_{085} B_{084} B_{083} B_{082} B_{081} B_{080}	010000	105	01000
	B_{095} B_{094} B_{093} B_{092} B_{091} B_{090}	010010	106	01001
	B_{105} B_{104} B_{103} B_{102} B_{101} B_{100}	010100	107	01010
	B_{115} B_{114} B_{113} B_{112} B_{111} B_{110}	010110	108	01011
	B_{125} B_{124} B_{123} B_{122} B_{121} B_{120}	011000	109	01100
	B_{135} B_{134} B_{133} B_{132} B_{131} B_{130}	011010	110	01101
	B_{145} B_{144} B_{143} B_{142} B_{141} B_{140}	011100	111	01110
	B_{155} B_{154} B_{153} B_{152} B_{151} B_{150}	011110	112	01111
	B_{165} B_{164} B_{163} B_{162} B_{161} B_{160}	100001	113	10000
	B_{175} B_{174} B_{173} B_{172} B_{171} B_{170}	100011	114	10001
	B_{185} B_{184} B_{183} B_{182} B_{181} B_{180}	100101	115	10010
	B_{195} B_{194} B_{193} B_{192} B_{191} B_{190}	100111	116	10011
	B_{205} B_{204} B_{203} B_{202} B_{201} B_{200}	101001	117	10100
	B_{215} B_{214} B_{213} B_{212} B_{211} B_{210}	101011	118	10101
	B_{225} B_{224} B_{223} B_{222} B_{221} B_{220}	101101	119	10110
	B_{235} B_{234} B_{233} B_{232} B_{231} B_{230}	101111	120	10111
	B_{245} B_{244} B_{243} B_{242} B_{241} B_{240}	110001	121	11000
	B_{255} B_{254} B_{253} B_{252} B_{251} B_{250}	110011	122	11001
	B_{265} B_{264} B_{263} B_{262} B_{261} B_{260}	110101	123	11010
	B_{275} B_{274} B_{273} B_{272} B_{271} B_{270}	110111	124	11011
	B_{285} B_{284} B_{283} B_{282} B_{281} B_{280}	111001	125	11100
	B_{295} B_{294} B_{293} B_{292} B_{291} B_{290}	111011	126	11101
	B_{305} B_{304} B_{303} B_{302} B_{301} B_{300}	111101	127	11110
	B_{315} B_{314} B_{313} B_{312} B_{311} B_{310}	111111	128	11111

9.19.1 4096 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data 4k Color (4-bits)
RED	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	000000	1	0000
	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	000100	2	0001
	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	001000	3	0010
	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	001100	4	0011
	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	010001	5	0100
	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	010101	6	0101
	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	011001	7	0110
	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	011101	8	0111
	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	100010	9	1000
	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	100110	10	1001
	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	101010	11	1010
	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	101110	12	1011
	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	110011	13	1100
	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	110111	14	1101
	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	111011	15	1110
	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	111111	16	1111
	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	------	17	Not used
	|	|	|	
	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	------	32	

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data 4k Color (4-bits)
GREEN	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	000000	33	0000
	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	000100	34	0001
	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	001000	35	0010
	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	001100	36	0011
	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	010001	37	0100
	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	010101	38	0101
	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	011001	39	0110
	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	011101	40	0111
	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	100010	41	1000
	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	100110	42	1001
	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	101010	43	1010
	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	101110	44	1011
	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	110011	45	1100
	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	110111	46	1101
	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	111011	47	1110
	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	111111	48	1111
	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	------	49	Not used
	|	|	|	
	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}	------	96	

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data 4k Color (4-bits)
BLUE	B_{005} B_{004} B_{003} B_{002} B_{001} B_{000}	000000	97	0000
	B_{015} B_{014} B_{013} B_{012} B_{011} B_{010}	000100	98	0001
	B_{025} B_{024} B_{023} B_{022} B_{021} B_{020}	001000	99	0010
	B_{035} B_{034} B_{033} B_{032} B_{031} B_{030}	001100	100	0011
	B_{045} B_{044} B_{043} B_{042} B_{041} B_{040}	010001	101	0100
	B_{055} B_{054} B_{053} B_{052} B_{051} B_{050}	010101	102	0101
	B_{065} B_{064} B_{063} B_{062} B_{061} B_{060}	011001	103	0110
	B_{075} B_{074} B_{073} B_{072} B_{071} B_{070}	011101	104	0111
	B_{085} B_{084} B_{083} B_{082} B_{081} B_{080}	100010	105	1000
	B_{095} B_{094} B_{093} B_{092} B_{091} B_{090}	100110	106	1001
	B_{105} B_{104} B_{103} B_{102} B_{101} B_{100}	101010	107	1010
	B_{115} B_{114} B_{113} B_{112} B_{111} B_{110}	101110	108	1011
	B_{125} B_{124} B_{123} B_{122} B_{121} B_{120}	110011	109	1100
	B_{135} B_{134} B_{133} B_{132} B_{131} B_{130}	110111	110	1101
	B_{145} B_{144} B_{143} B_{142} B_{141} B_{140}	111011	111	1110
	B_{155} B_{154} B_{153} B_{152} B_{151} B_{150}	111111	112	1111
	B_{165} B_{164} B_{163} B_{162} B_{161} B_{160}	------	113	Not used
	|	|	|	
	B_{315} B_{314} B_{313} B_{312} B_{311} B_{310}	------	128	

9.21 External Light Source
The operation of the module can meet customer's Environmental reliability requirements.

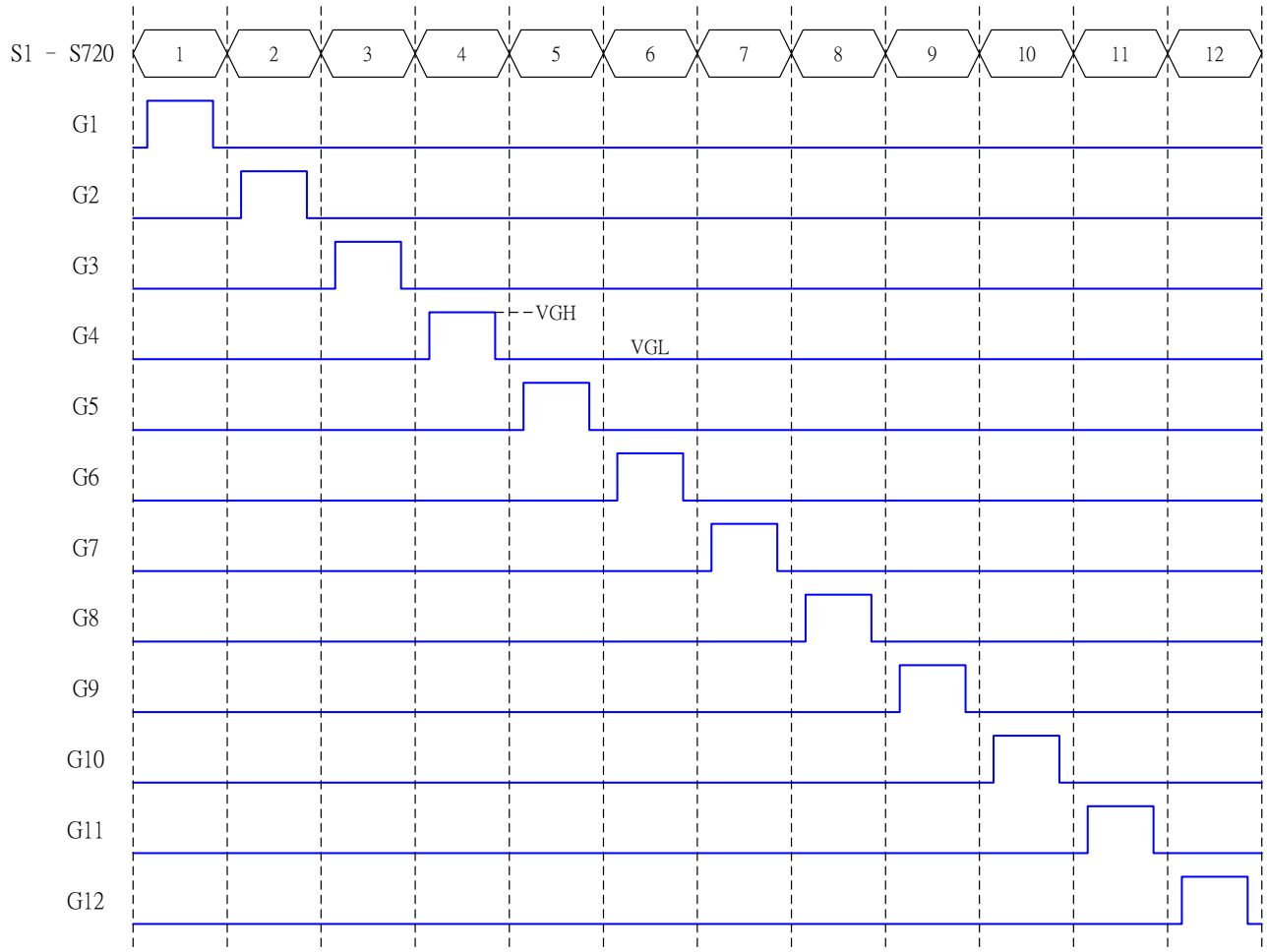
9.22 Oscillator
The chip has on-chip oscillator that does not require external components. This oscillator output signal is used for system clock generation for internal display operation.

9.23 System Clock Generator
The timing generator produces the various signals to driver the internal circuitty. Internal chip operation is not affected by operations on the data bus.

9.24 Instruction Decoder and Register
The instruction decoder indentifies command words arriving at the interface and routes the following data bytes to their destination. The command set can be found in "Command" section.

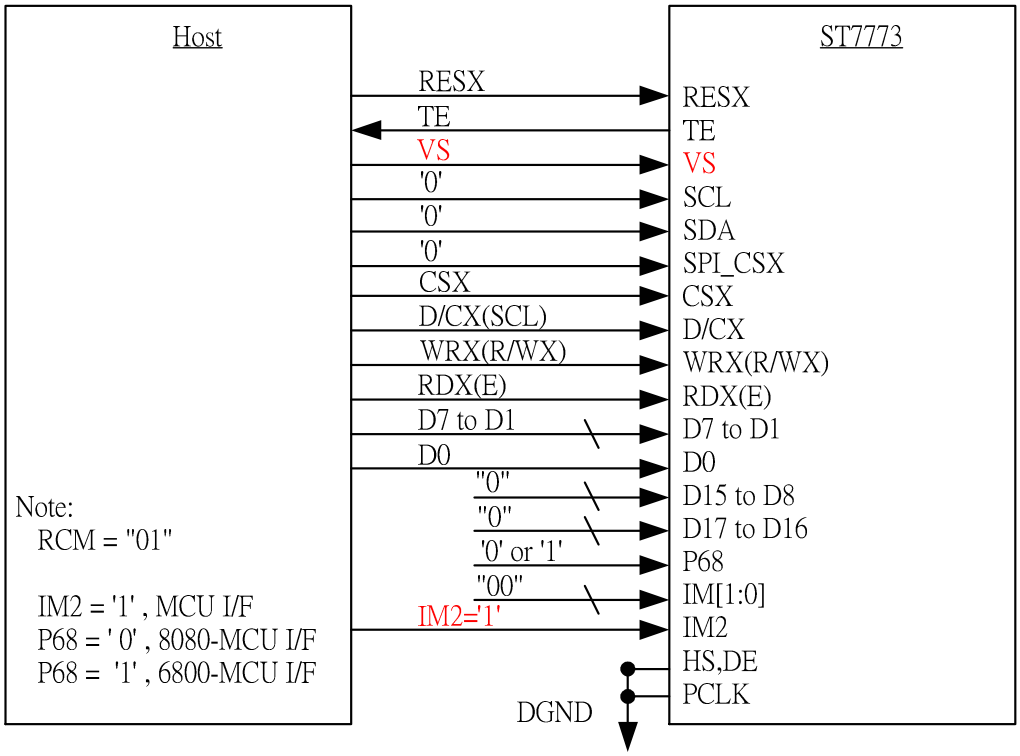
9.25 Source Driver
The source driver block includes 176x3 source outputs (S1 to S528), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simulatance selected rows.

9.26 Gate Driver
The gate driver block includes 220 channel gate output (G0 to G219) which should be connected directly to the TFT-LCD.



9.27 VSYNC Interface

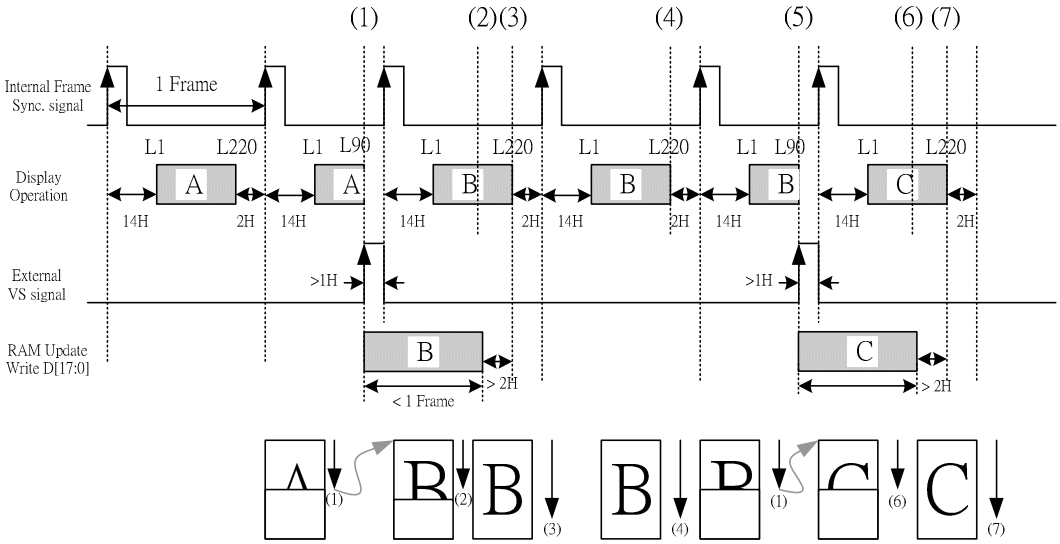
The ST7773 incorporates a VSYNC I/F, which enables to display a moving picture which only a system interface and frame-synchronizing signal (VS). The interface enables to display moving pictures with minimum modification to a conventional systern.



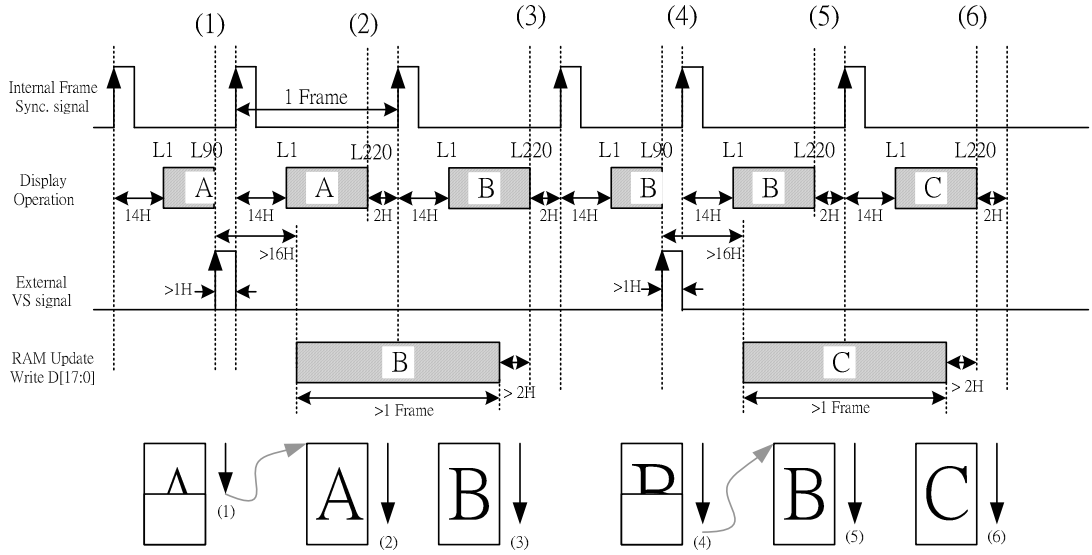
The VSYNC-I/F is turned ON by ***VSYNC-I/F ON(ADH)*** command and turned OFF by ***VSYNC-I/F(ACH)*** command. In VSYNC-I/F mode, internal display operations are synchronized with VS. The VSYNC-I/F enables to display a moving picture through a system interface in higher speed than the internal display operations by some degree.

The VSYNC-I/F executes display operations only with internal clocks generated by internal oscillators and VS input. All display data are stored in RAM so that only the data relevant to updating a screen are transferred to minimize data transmission while displaying a moving picture.

-Leading Mode



-Lagging Mode



1、In RCM[1:0]="01" mode, writing data to RAM on rising edge of VS signal.
2、If high pulse of VS signal should large than 1-lines.
3、The BP and FP should follow conditions: BP≧2-lines, FP≧2-lines and BP+FP =16-lines
4、The signals (CSX, WRX, D/CX and VS) of VSYNC I/F should follow MCU Parallel Interface AC timing.

The VSYNC-I/F has limits on the minimum RAM write speed through the system interface and the frequency of the internal clocks. It requires a RAM write speed more than the calculated result from the following formula.

-Internal clock frequency(fosc)[Hz]

= Frame Frequency x (DisplayLines +Front Porch(VSFP)+BackPorch(VSBP)) x 16(clocks) x fluctuation

Note 1: When RAM write does not start right affer the falling edge of VS, the time from the falling edge of VS until RAM write starts must also be taken into account.

Example of RAMs writes speed and the frequency of the internal clocks in VSYNC-I/F mode is as follows.

Example:

Display size: 176 RGB x 220 lines

Raster-rows: 220 lines

Back/Front porch: 14/2 lines (VSBP = 1110/ VSFP = 0010 of AFH)

-When Frame frequency:60 Hz

Internal clock frequency(fosc)[Hz] =

60Hz x (220+2+14) x 16 clocks x 1.1/0.9 = 277kHz

When calculating an internal clock frequency, possible causes of fluctuations must also be taken into consideration. In this example, the allowance for the fluctuation is x10% from the center value, and the frequency must be within a VS cycle.

Also in this example, variations attributed to LSI fabrication and room temperature are taken into consideration as causes of fluctuations. Other possible causes of fluctuations, such as variations in external resistors or voltage changes are not considered in this example. It is necessary to make a setting with enough margins to accommodate

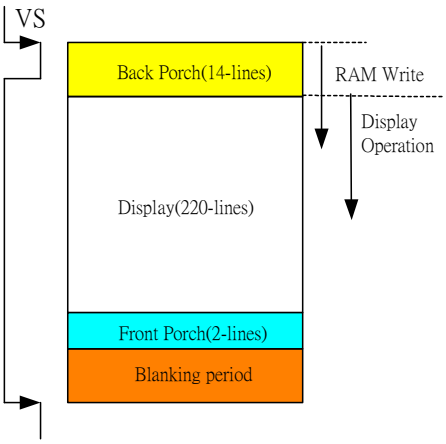
-When Frame frequency: 60Hz

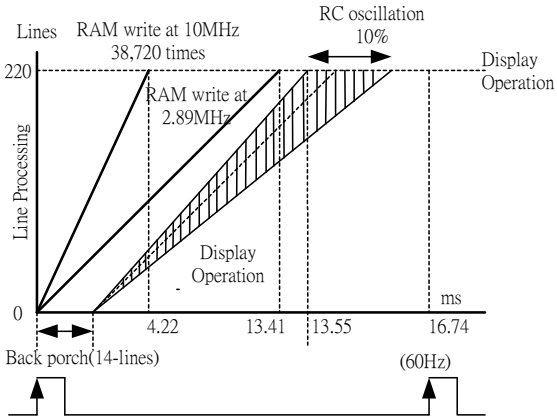
Minimum speed for RAM writing[Hz]>

176x200/{((14+220-2)lines x 16 clock)/300kHz}=2.89MHz

Note 2 : The above calculation is premised on the case of writing data to RAM on the falling edge of VS.
Note 3 : There must atleast be a margin of 2 processing lines when all one-frame data are written to RAM before the ST7773 starts processing display llines

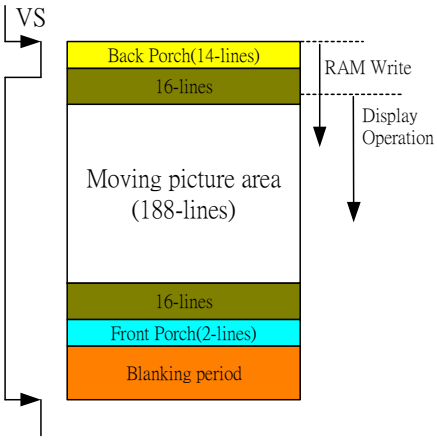
By writing data to RAM on rising edge of VS signal at speed of 2.89MHz(Frame rate =60Hz) or more, it is possible to overwrite an entire screen without flicker by completing dta write operatipon of a line before it starts display operation of that line

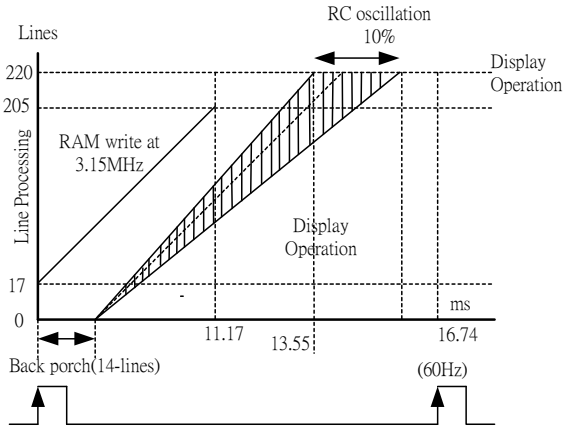




Notes to then VSYNC Interface

1. The aforementioned example of calculation is just a result of calculation. In actual settings, possible causes of fluctuations should be taken into comsideration. It is necessary to give enough margins when setting a RAM writing speed.
2. The aforementioned example of calculation is the value in case of overwriting full screen. If a moving picture display area is limited, it will result in more margins between RAMs write and display operations.





3. A front porch period continues after completion of 1 frame and until the next input of VS.
4. The partial display and vertical scroll functions are not available with then VSYNC-I/F.

10. Command

10.1 System function Command List and Description

Table 10.1.1 System Function command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
NOP	10.1.1	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	10.1.2	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	10.1.3	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
		1	1	↑	-	‘1’	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
RDDST	10.1.4	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
		1	1	↑	-	VSSON	ST14	INVON	ST21	ST11	DISON	TEON	GCS2		-
		1	1	↑	-	GCS1	GCS0	TELON	HSON	VSON	PCKON	DEON	ST0		-
RDDPM	10.1.5	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0		-
RDD MADCTL	10.1.6	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh	Read Display MADCTL
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	D1	D0		-
RDD COLMOD	10.1.7	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	IFPF2	IFPF1	IFPF0		-
RDDIM	10.1.8	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0		-
RDDSM	10.1.9	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	TEON	TELON	HSON	VSON	PCKON	DEON	D1	D0		-

“-“: Don’t care

Table 10.1.2 System Function command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
SLPIN	10.1.11	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	10.1.12	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	10.1.13	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	10.1.14	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial mode off (Normal)
INVOFF	10.1.15	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off (normal)
INVON	10.1.16	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	10.1.17	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
		1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0		-
DISPOFF	10.1.18	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	10.1.19	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	10.1.20	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0≦S≦X
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address end: XS≦XE≦X
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	10.1.21	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0≦YS≦Y
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address end: YS≦YE≦Y
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	10.1.22	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
		1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RAMRD	10.1.23	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		Read data

"-": Don't care

Table 10.1.3 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PTLAR	10.1.24	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address (0,1,2, ..P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0,1,2, .., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
SCRLAR	10.1.25	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
		1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		Top fixed area (0,1,2, .., S)
		1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
		1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		Vertical scroll area (0,1,2, .., S)
		1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
		1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		Bottom fixed area (0,1,2, .., S)
		1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	10.1.26	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	10.1.27	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
		1	↑	1	-	-	-	-	-	-	-	-	M		M="0": Mode1, M="1": Mode2
MADCTL	10.1.28	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0		-
VSCSAD	10.1.29	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll start address of RAM
		1	↑	1	-	-	-	-	-	-	-	-	SSA8		SSA = 0, 1, 2, …, 175
		1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		
IDMOFF	10.1.30	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	10.1.31	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	10.1.32	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
		1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	0	IFPF2	IFPF1	IFPF0		Interface format
RDID1	10.1.33	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	10.1.34	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	10.1.35	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter
RDID3	10.1.36	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID4
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40		Read parameter
VSCTRI	10.1.37	0	↑	1	-	1	0	1	0	1	1	1	0	(AEh)	VSYNC interface porch setting
		1	↑	1	-	VSFP3	VSFP2	VSFP1	VSFP0	VSBP3	VSBP2	VSBP1	VSBP0		

"-": Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: B0 to D9 and DE to FF are for factory use of driver supplier.

Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

10.2 Panel Function Command List and Description

Table 10.2.1 Panel Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
RGBCTR	10.2.1	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	Set RGB signal control
		1	↑	1	-	0	0	SWX	ICM	DP	EP	HSP	VSP		ICM: RGB data ascess select DP, HSP, VSP: PCLK, HS, VS polarity set
					-	0	0	0	0	0	0	0	0		
FRMCTR1	10.2.2	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode (Full colors)
		1	↑	1	-	RTNA[7:0]									RTNA_VSYNC setting for VSYNC mode
					-	0	0	1	1	1	0	1	1		
						0	0	0	FPA[4:0]						
					-	0	0	0	0	0	1	0	0		
					-	0	0	0	BPA[4:0]						
					-	0	0	0	0	0	0	1	1		
						RTNA_VSYNC[7:0]									
						0	0	1	1	1	0	0	0		
FRMCTR2	10.2.3	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle mode (8 colors)
		1	↑	1		RTNB[7:0]									
						0	0	1	1	1	0	1	1		
						0	0	0	FPB[4:0]						
						0	0	0	0	0	1	0	0		
									BPB[4:0]						
									0	0	0	1	1		
FRMCTR3	10.2.4	0	↑	1	-	1	0	1	1	0	0	1	0	(B3h)	In partial mode (Full colors)
		1	↑	1		RTNC[7:0]									
						0	0	1	1	1	0	1	1		
						0	0	0	FPC[4:0]						
						0	0	0	0	0	1	0	0		
									BPC[4:0]						
									0	0	0	1	1		
INVCTR	10.2.5	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control
		1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		NLA:,NLB,NLC set inversion
					-	0	0	0	0	0	0	0	0		
RGB PRCTR	10.2.6	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	RGB I/F Blanking porch setting
		1	↑	1	-	VFPR[7:0]									
						0	0	0	0	0	0	0	1		
						VBPR[7:0]									
					-	0	0	0	0	0	0	1	1		
						0	0	HFPR[5:0]							
						0	0	0	0	1	0	1	0		
						0	0	HBPR[5:0]							
						0	0	0	0	1	0	1	0		
DISSET5	10.2.7	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)	Display function setting
		1	↑	1	-	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ0		NO: the amount of non-overlap SDT: set amount of source delay PT: No display area source/ VCOM/ Gate output control EQ: set EQ period
					-	0	0	0	1	0	1	0	1		
						0	0	0	0	PTG1	PTG0	PT1	PT0		
						0	0	0	0	0	0	0	0		
VSYNCOFF	10.2.8	0	↑	1	-	1	0	1	0	1	1	0	0	(BCh)	VSYNC interface function off
VSYNCON	10.2.9	0	↑	1	-	1	0	1	0	1	1	0	1	(BDh)	VSYNC interface function on

Table 10.2.2 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PWCTR1	10.2.10	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	Power control setting
		1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0		VRH: Set the GVDD voltage
					-	0	0	0	0	0	1	0	1		
					-	0	0	0	0	0	VC2	VC1	VC0		VC: Set the VCI1 voltage
					-	0	0	0	0	0	0	0	1		
PWCTR2	10.2.11	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	Power control setting
		1	↑	1	-	VGH3	VGH2	VGH1	VGH0	VGL3	VGL2	VGL1	VGL0		VGH: set VGH voltage VGL: set VGL voltage
						1	0	1	1	1	0	1	1		
PWCTR3	10.2.12	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	In normal mode (Full colors)
		1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0		AP: adjust the operational amplifier DC: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	1	0	0		
PWCTR4	10.2.13	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)	In Idle mode (8-colors)
		1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0		AP: adjust the operational amplifier DCT: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	0	1	0		
PWCTR5	10.2.14	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	In partial mode + Full colors
		1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0		AP: adjust the operational amplifier DCT: adjust the booster circuit for Idle mode
					-	0	0	0	0	0	1	0	0		
VMCTR1	10.2.15	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOM control 1
		1	↑	1	-	0	VMH6	VMH 5	VMH4	VMH3	VMH2	VMH1	VMH0		VMH: VCOMH voltage control VML: VCOML voltage control
					-	0	0	1	1	1	1	0	0		
		1	↑	1	-	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0		
					-	0	0	1	1	1	1	0	0		
VMOFCTR	10.2.16	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	VCOM offset control
		1	↑	1	-	nVM*	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0		
					-	0	0	1	1	1	1	0	0		
STEP CTR	10.2.17	0	1	↑	-	1	1	0	0	1	0	0	1	(C9h)	Step124 setup
		1	↑	↑	-	DUAL_EN	STEP_DIV_EN	1	0	0	CP1_FREQ_SEL[2:0]				Adjust step1/2/4 booster frequency
						1	0	1	0	0	1	0	0		
					-	NW_MODE	0	0	0	0	CP2_FREQ_SEL[2:0]				
					-	0	0	0	0	0	1	0	0		
					-	0	0	0	0	0	CP4_FREQ_SEL[2:0]				
					-	0	0	0	0	0	1	0	0		
8-color CTR	10.2.18	0	↑	1	-	1	1	1	1	1	0	0	0	(F8h)	
		1	↑	1	-	0	0	0	0	0	8-color	0	0		8-color detect function
					-	0	0	0	0	0	1	0	0		
PWCTR6	10.2.19	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)	Gate operational amplifier control
		1	↑	1	-	0	0	1	1	1	SAPA[2:0]				SAPA.: Normal mode SAPB : Idle mode SAPC : Partial mode
					-	0	0	1	1	1	1	0	0		
					-	0	1	1	1	1	SAPB[2:0]				
					-	0	1	1	1	1	1	0	0		
					-	0	0	0	0	0	SAPC[2:0]				
					-	0	0	0	0	0	1	0	0		

"-": Don't care

Note 1: C0h to C8h are fixed for about power controller.

Table 10.2.3 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
WRID2	10.2.20	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	LCM version code
		1	↑	1	-	0	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Write ID2 value to NV memory Set the LCM version code at ID2
					-	1	0	0	0	0	0	0	0		
WRID3	10.2.21	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Customer Project code
		1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Write ID3 value to NV memory Set the project code at ID3
					-	0	0	0	0	0	0	0	0		
RDID4	10.2.22	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)	IC Vender Coder
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
					-	-	-	-	-	-	-	-	-		
		1	1	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410		ID41:IC Vender Code ID42: IC Part Number Code ID43 & ID44: Chip version coder
					-	0	0	0	0	0	0	0	0		
		1	1	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420		
					-	0	0	0	0	0	0	0	0		
		1	1	↑	-	ID437	ID436	ID435	ID434	ID43 0	ID432	ID431	ID430		
					-	0	0	0	0	0	0	0	0		
		1	1	↑	-	ID447	ID446	ID445	ID444	ID443	ID442	ID441	ID440		
					-	0	0	0	0	0	0	0	0		
NVCTR2	10.2.23	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	MTP read command
		1	↑	1	-	1	0	1	0	1	0	1	0	75	
NVCTR3	10.2.24	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	MTP write command
		1	↑	1	-	0	1	0	1	0	1	0	1	55	
		1	↑	1	-	1	1	1	1	0	0	0	0	F0	
		1	↑	1	-	0	1	0	1	1	0	1	0	5A	

"-": Don't care

Note 1: The D1h to D3h registers are fixed for about ID code setting.

Note 2: The D9h, DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)

Table 10.2.4 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRP1		0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set Gamma correction
		1	↑	1	-	---	---	VRF0P[5:0]							Postiive Polarity
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	VOS0P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK0P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK1P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK2P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK3P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK4P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK5P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK6P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK7P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK8P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK9P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	SELV0P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	SELV1P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	SELV62P[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	SELV63P[5:0]							
					-	0	0	0	0	0	0	0	0		
GAMCTRN1		0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Set Gamma correction
		1	↑	1	-	---	---	VRF0N[5:0]							Negative Polarity
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	VOS0N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK0N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK1N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK2N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK3N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK4N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK5N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK6N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK7N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK8N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	PK9N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	SELV0N[5:0]							
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	---	---	SELV1N[5:0]							
					-	0	0	0	0	0	0	0	0		

GAMCTRN1		1	↑	1	-	---	---	SELV62N[5:0]								Negative Polariy
					-	0	0	0	0	0	0	0	0			
		1	↑	1	-	---	---	SELV63N[5:0]								
					-	0	0	0	0	0	0	0	0			

"-": Don't care

Note 1: E0-E1 registers are fixed for about Gamma adjusting.

Table 10.2.5 Panel Function Command List (5)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
Special/Test Command		0	↑	1	-	1	1	1	1	0	0	0	0	(F0h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	0	0	0	1	(F1h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	0	0	1	0	(F2h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	0	0	1	1	(F3h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	0	1	0	0	(F4h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
		0	↑	1	-	1	1	1	1	0	1	0	1	(F5h)	Special/Test Command
Special/Test Command		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	0	1	1	0	(F6h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	0	1	1	1	(F7h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	1	0	0	1	(F9h)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	1	0	1	0	(FAh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
		0	↑	1	-	1	1	1	1	1	0	1	1	(FBh)	Special/Test Command
Special/Test Command		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	1	1	0	1	(FDh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	1	1	1	1	0	(FEh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		
Special/Test Command		0	↑	1	-	1	1	1	0	1	1	1	1	(FFh)	Special/Test Command
		1	↑	1	-										
					-	0	0	0	0	0	0	0	0		

"-": Don't care

Note 1: F6h to FFh registers are reserved for about special or chip test using

Note 2: The F0h to F5h registers are reserved for future using

10.1.1 NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-

NOTE: "-" Don't care

Description	-This command is empty command.

10.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-

NOTE: "-" Don't care

Description	-When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). -It will be necessary to wait 5msec before sending new command following software reset. -The display module loads all default values to the registers during 5msec. -If Software Reset is applied during Sleep Out mode, it will be necessary to wait *120msec* before sending Sleep Out command. -Software Reset command cannot be sent during Sleep Out sequence.

10.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3rt Parameter	1	1	↑	-	'1'	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

NOTE: "-" Don't care

Description	-This read byte returns 24-bit display identification information. -The 1st parameter is dummy data -The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. -The 3rd parameter (ID27 to ID20): LCD module/driver version ID -The 4th parameter (ID37 to UD30): LCD module/driver ID. *NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.*
Default	

Status	Default Value	
	ID1	ID2
Power On Sequence	-	-
S/W Reset	-	-
H/W Reset	-	-

10.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3rd Parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th Parameter	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th Parameter	1	1	↑		GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1')
MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')
ML	Scan Address Order (ML)	'1' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='1') '0'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='0')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order	'1' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='1') '0' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='0')
ST24	For Future Use	'0'
ST23	For Future Use	'0'
IFPF2 IFPF1 IFPF0	Interface Color Pixel Format Definition	"011" = 12-bit / pixel, "101" = 16-bit / pixel, "110" = 18-bit / pixel, others are no define
IDMON	Idle Mode On/Off	'1' = On, "0" = Off
PTLON	Partial Mode On/Off	'1' = On, "0" = Off
SLPOUT	Sleep In/Out	'1' = Out, "0" = In
NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
VSSON	Vertical Scrolling Status	'1' = Scroll on,"0" = Scroll off
ST14	Horizontal Scroll Status	'0'
INVON	Inversion Status	'1' = On, "0" = Off
ST12	All Pixels On (Not Used)	'0'
ST11	All Pixels Off (Not Used)	'0'
DISON	Display On/Off	'1' = On, "0" = Off
TEON	Tearing effect line on/off	'1' = On, "0" = Off
GCSEL2 GCSEL1 GCSEL0	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" to "111" = Not defined
TELOM	Tearing effect line mode	'0' = mode1, '1' = mode2
HSON	Horizontal Sync. (HS, RGB I/F)	'1' = On, '0' = Off
VSON	Vertical Sync, (VS, RGB I/F)	'1' = On, '0' = Off
PCLKON	Pixel Clock (PCLK, RGB I/F)	'1' = On, '0' = Off
DEON	Data Enable (DE, RGB I/F)	'1' = On, '0' = Off
ST0	For Future Use	'0'

Note: ST0, ST5, ST9, ST11-ST15, ST19, ST23, ST24 are set to '0', when RGB I/F.

Default

Status	Default Value (ST31 to ST0)			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx0xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

10.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off
SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In
NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
DISON	Display On/Off	'1' = Display On, '0' = Display Off
D1	Not Used	'0'
D0	Not Used	'0'

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000(08h)
S/W Reset	0000_1000(08h)
H/W Reset	0000_1000(08h)

10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑		MY	MX	MV	ML	RGB	MH	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
MX	Row Address Order	'1' = Bottom to Top (When MADCTL B7='1') '0' = Top to Bottom (When MADCTL B7='0')
MY	Column Address Order	'1' = Right to Left (When MADCTL B6='1') '0' = Left to Right (When MADCTL B6='0')
MV	Row/Column Order (MV)	'1' = Row/column exchange (MV=1) '0' = Normal (MV=0)
ML	Vertical Refresh Order	'1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom
RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
MH	Horizontal order	'1' =LCD Refresh Right to Left '0' =LCD Refresh Left to Right
D1	Not Used	'0'
D0	Not Used	'0'

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change
H/W Reset	0000_0000 (00h)

10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command indicates the current status of the display as described in the table below:

IFPF[2:0]		MCU Interface Color Format
011	3	12-bit/pixel
101	5	16-bit/pixel
110	6	18-bit/pixel
111	7	No used

Others are no define and invalid

VIFPF[2:0]		RGB Interface Color Format
0101	5	16-bit/pixel (1-times data transfer)
0110	6	18-bit/pixel (1-times data transfer)
0111	7	No used
1110	14	18-bit/pixel (3-times data transfer)

Others are no define and invalid

Default

Status	Default Value	
	IFPF[2:0]	VIPF[3:0]
Power On Sequence	0110 (18 bits/pixel)	0110 (18 bits/pixel)
S/W Reset	No Change	No Change
H/W Reset	0110 (18 bits/pixel)	0110 (18 bits/pixel)

10.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (0Dh): Read Display Image Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
VSSON	Vertical Scrolling On/Off	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	Horizontal Scrolling On/Off	"0" (Not used)
INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"0" (Not used)
D3	All Pixels Off	"0" (Not used)
GCS2 GCS1 GCS0	Gamma Curve Selection	"000" = GC0, "001" = GC1, "010" = GC2, "011" = GC3, "100" to "111" = Not defined

Default

Status	Default Value(D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

10.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (0Eh): Read Display Signal Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing Effect Line On/Off	"1" = On, "0" = Off
TELOM	Tearing effect line mode	"1" = mode1, "0" = mode2
HSON	Horizontal Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
VSON	Vertical Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
PCKON	Pixel Clock (PCLK, RGB I/F) On/Off	"1" = On, "0" = Off
DEON	Data Enable (DE, RGB I/F) On/Off	"1" = On, "0" = Off
D1	Not Used	"1" = On, "0" = Off
D0	Not Used	"1" = On, "0" = Off

Default

Status	Default Value(D7~D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

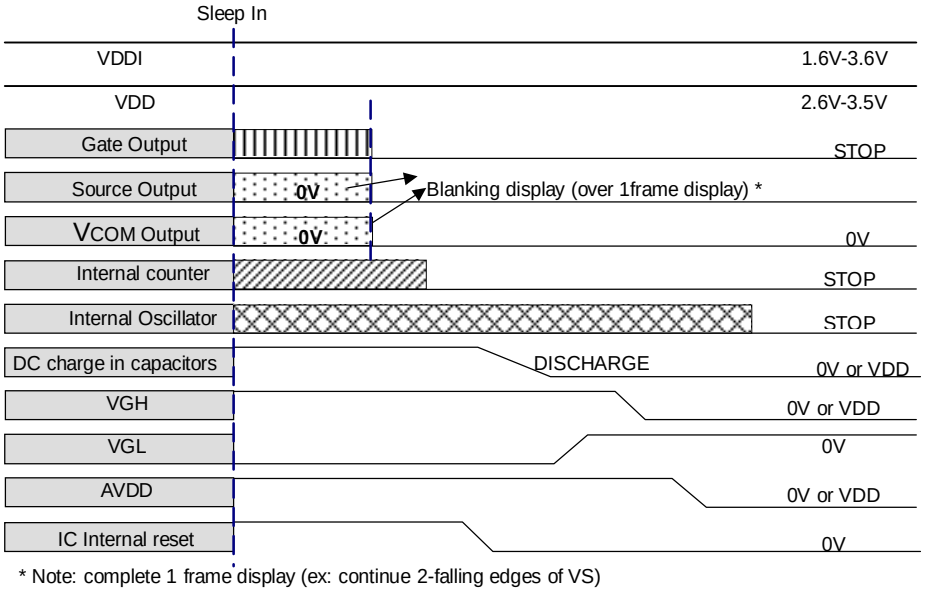
10.1.10 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
1st Parameter	No parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command causes the LCD module to enter the minimum power consumption mode.
-In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Restriction

-This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
-It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
-It will be necessary to wait *120msec* after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

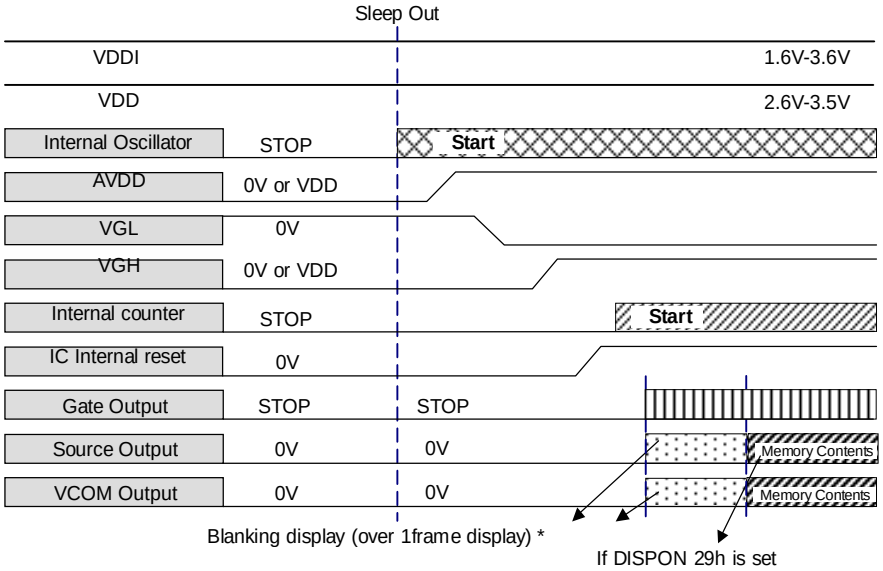
10.1.11 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command turns off sleep mode.
-In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Restriction

-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).
-It will be necessary to wait *5msec* before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
-DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode.
-DRIVER is doing self-diagnostic functions during this *5msec*. See also section 9.20.
-It will be necessary to wait *120msec* after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

10.1.12 PTLON (12h): Partial Display Mode On

12H	PTLON (12h): Partial Display Mode On												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h) -To leave Partial mode, the Normal Display Mode On command (13H) should be written.
Default	

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

10.1.13 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

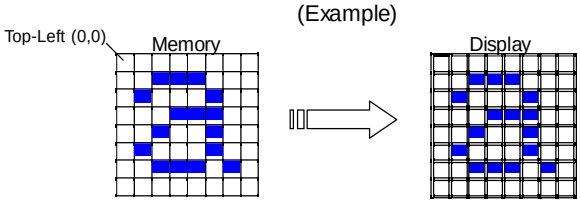
Description	-This command returns the display to normal mode. -Normal display mode on means Partial mode off, Scroll mode Off. -Exit from NORON by the Partial mode On command (12h)
Default	

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

10.1.14 INVOFF (20h): Display Inversion Off

20H	IVNOFF (Normal Display Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to recover from display inversion mode. (Example) 
Default	

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

10.1.15 INVON (21h): Display Inversion On

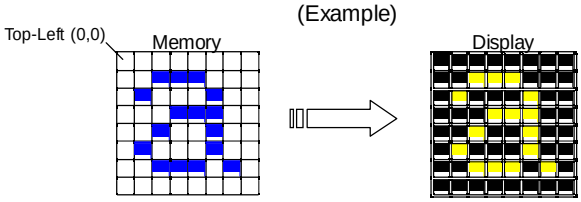
21H	IVNOFF (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to enter into display inversion mode
-To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)



Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

10.1.16 GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)
1st Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in section 9.17 The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC [7:0]	Parameter	Curve Selected
		GS=1
01h	GC0	Gamma Curve 1 (G2.2)
02h	GC1	Gamma Curve 2 (G1.8)
04h	GC2	Gamma Curve 3 (G2.5)
08h	GC3	Gamma Curve 4 (G1.0)

Note: All other values are undefined.

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

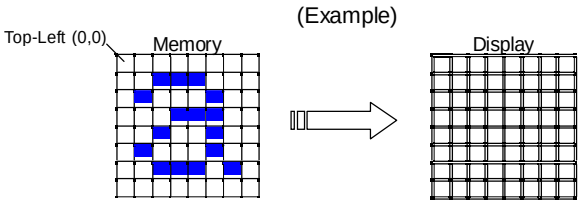
10.1.17 DISPOFF (28h): Display Off

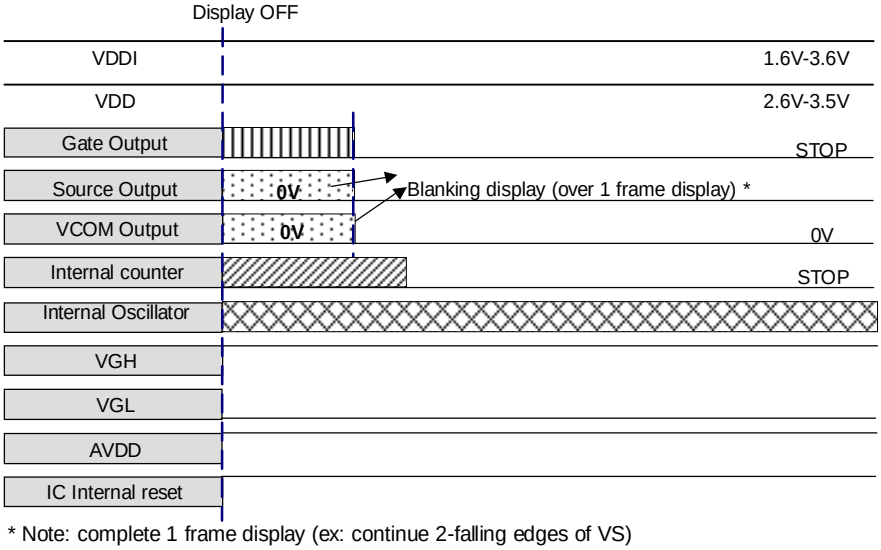
28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.
-Exit from this command by Display On (29h)





* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

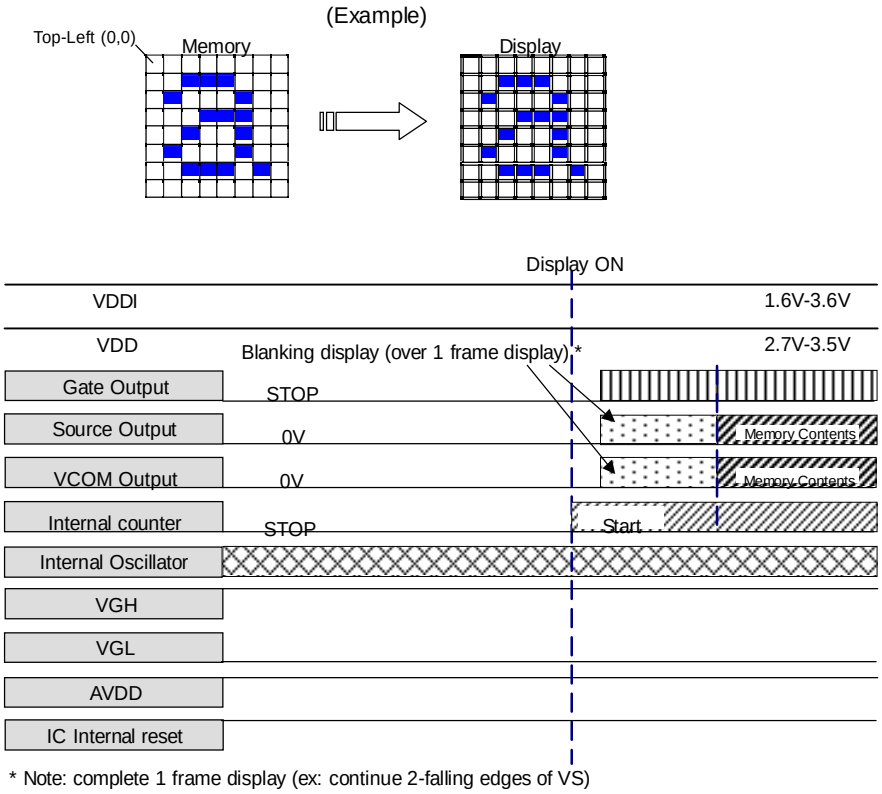
10.1.18 DISPON (29h): Display On

29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.



Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

10.1.19 CASET (2Ah): Column Address Set

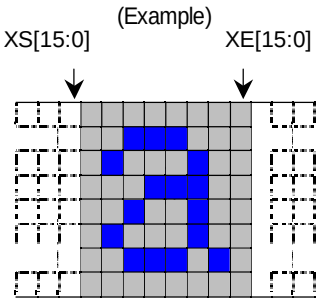
2AH	CASET(Colume Address Set)_												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(2Ah)
1st Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2nd Parameter	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3rd Parameter	1	↑	1		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4th Parameter	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.
-Each value represents one column line in the Frame Memory.

(Example)



estriction

XS [15:0] always must be equal to or less than XE [15:0]
When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.
(Parameter range: 0 ≦ XS [15:0] ≦ XE [15:0] ≦175 (00AFh)): MV="0"
(Parameter range: 0 ≦ XS [15:0] ≦ XE [15:0] ≦219 (00DBh)): MV="1"

Default

Status	Default Value		
	XS [15:0]	XE [15:0] (MV='**0** ')	XE [15:0] (MV='**1**')
Power On Sequence	0000h	00AFh (175)	
S/W Reset		00AFh (175)	00DBh (219)
H/W Reset		00AFh (175)	

10.1.20 RASET (2Bh): Row Address Set

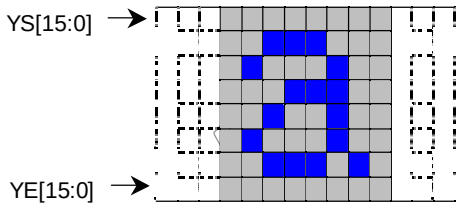
2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET (2Bh)	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.

Example



Restriction

YS [15:0] always must be equal to or less than YE [15:0]
When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.

(Parameter range: 0 ≦YS [15:0] ≦YE [15:0] ≦219 (00DBh)): MV="0"
(Parameter range: 0 ≦YS [15:0] ≦YE [15:0] ≦175 (009Fh)) : MV="1"

Default

Status	Default Value		
	YS [15:0]	YE [15:0] (MV='**0** ')	YE [15:0] (MV='**1**')
Power On Sequence	0000h	00DBh (219)	
S/W Reset	0000h	00DBh (219)	00AFh (175)
H/W Reset	0000h	00DBh (219)	

10.1.21 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
|	1	↑	1	|	|	|	|	|	|	|	|	|	|
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. (See section 9.12) -Sending any other command can stop Frame Write. In all color modes, there is no restriction on length of parameters. -1. 176x220 memory base (GM = '00') 176x220x18-bit memory can be written by this command Memory range: (0000h,0000h) -> (00AFh, 00DBh)
Default	Status: Power On Sequence — Default Value: Contents of memory is set randomly Status: S/W Reset — Default Value: Contents of memory is not cleared Status: H/W Reset — Default Value: Contents of memory is not cleared

10.1.22 RAMHD (2Eh): Memory Read

2EH	RAMHD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
|	1	1	↑	|	|	|	|	|	|	|	|	|	|
(N+1)th Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to transfer data from frame memory to MCU. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. (See section 9.12) -Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 9.10.2. -Frame Read can be cancelled by sending any other command. -See section 9.8 "Data color coding" for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.
Default	

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

10.1.25 PTLAR (30h): Partial Area

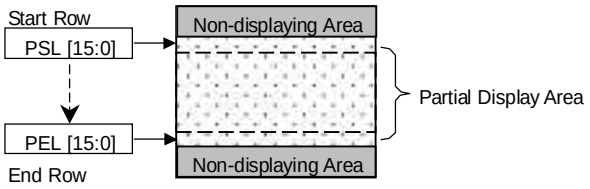
30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st Parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2nd Parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3rd Parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4th Parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

NOTE: "-" Don't care, can be set to VDDI or DGND level

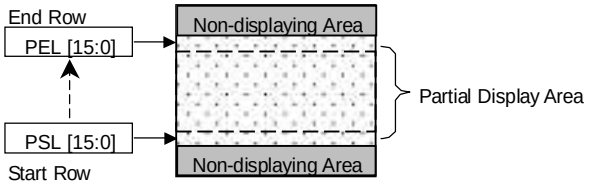
Description

-This command defines the partial mode's display area.
-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

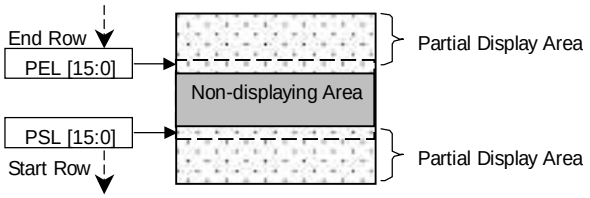
-If End Row **>** Start Row, when MADCTL ML='0'



-If End Row **>** Start Row, when MADCTL ML='1'



-If End Row **<** Start Row, when MADCTL ML='0'



-If End Row = Start Row then the Partial Area will be one row deep.

Default

Status	Default Value	
	PSL [15:0]	PEL [15:0]
Power On Sequence	0000h	00DBh
S/W Reset		
H/W Reset		

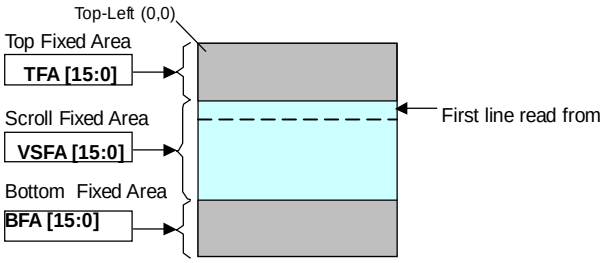
10.1.26 SCRLAR (33h): Scroll Area

33H	SCRLAR (Scrolll Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1st Parameter	1	↑	1	-	TFA15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	00h
2nd Parameter	1	↑	1	-	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	00h
3rd Parameter	1	↑	1	-	VSA15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	
4th Parameter	1	↑	1	-	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	
5th Parameter	1	↑	1	-	BFA15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	00h
6th Parameter	1	↑	1	-	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	00h

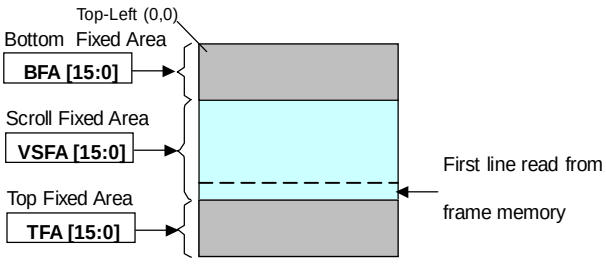
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command defines the Vertical Scrolling Area of the display.
When MADCTL ML=0
—The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
—The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
—The first line appears immediately after the bottom most line of the Top Fixed Area.
—The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
—TFA, VSA and BFA refer to the Frame Memory row address.



When MADCTL ML=1
—The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
—The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
—The first line appears immediately after the top most line of the Top Fixed Area.
—The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



See Section 9.10.1 for details of the Memory to Display Mapping.

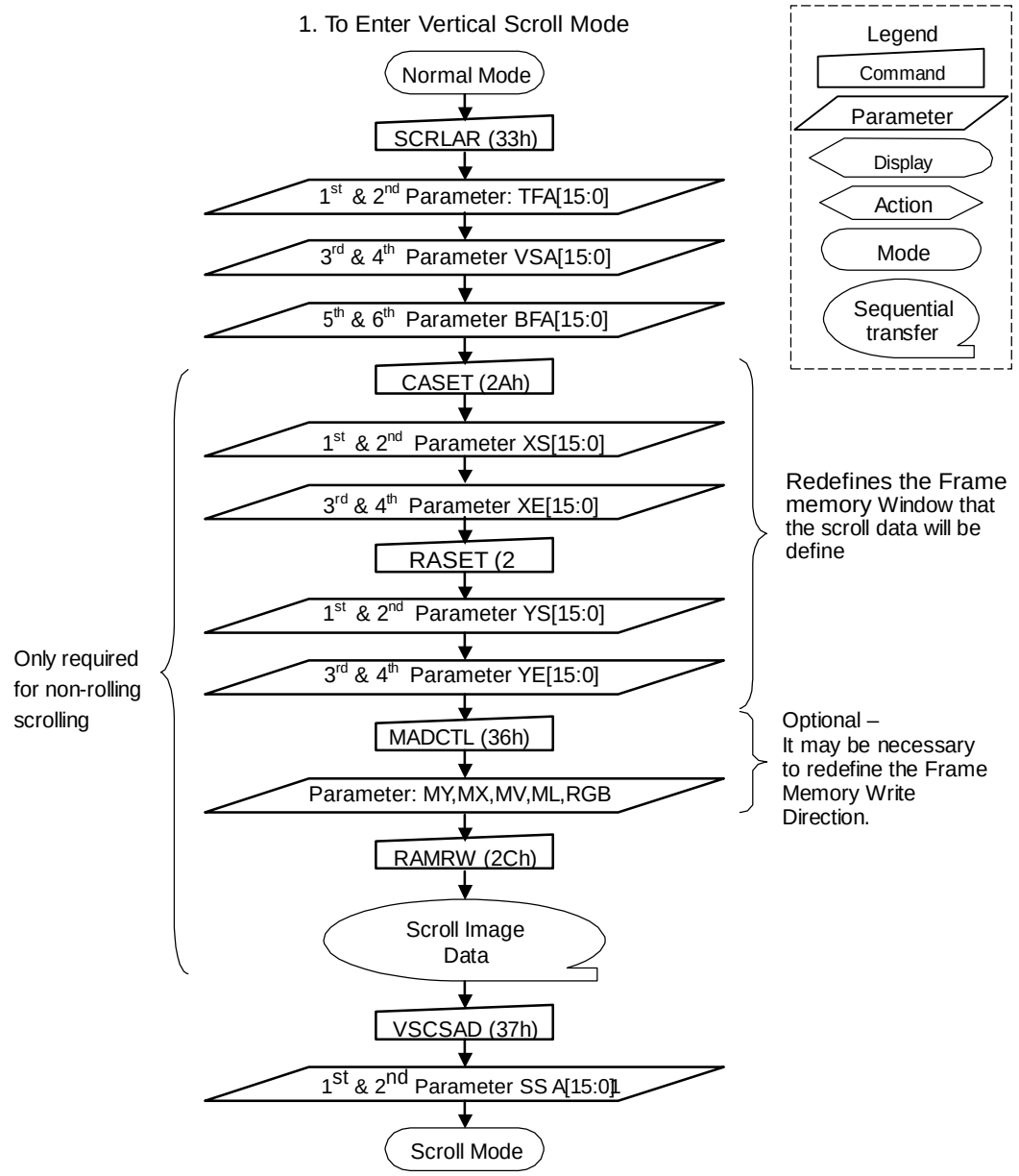
-The condition is 0≦(TFA+VSA+BFA) ≦220, otherwise Scrolling mode is undefined.

-In Vertical Scroll Mode, MADCTL parameter MV should be set to '0'-this only affects the Frame Memory Write.

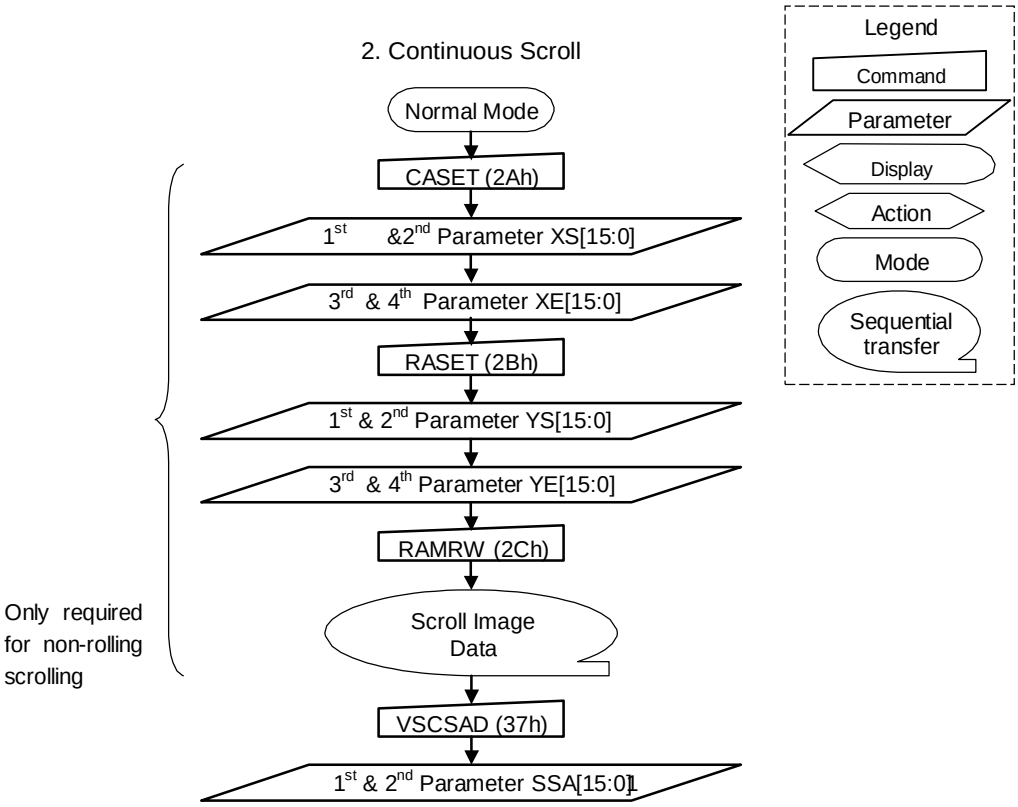
Default

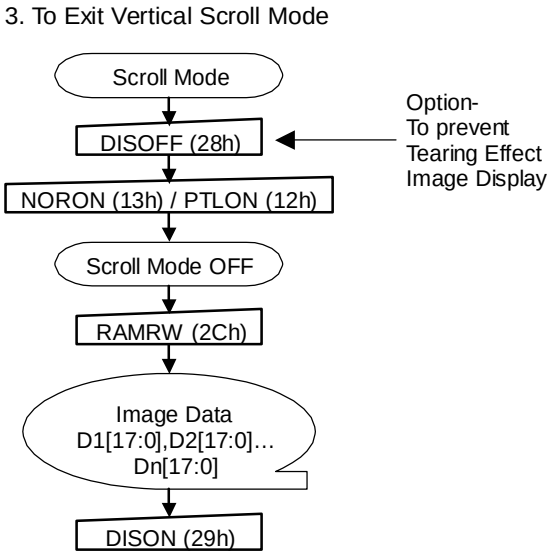
Status	Default Value		
	TFA [15:0]	VSA [15:0]	BFA [15:0]
Power On Sequence	0000h	00DBh	
S/W Reset			
H/W Reset			

Flow Chart



NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.





NOTE: Scroll Mode can be exit by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

10.1.27 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Default	

Status	Default Value	
	RCM1,RCM0 = "00","1x"	RCM1,RCM0 = "01"
Power On Sequence	OFF	ON
S/W Reset		
H/W Reset		

10.1.28 TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	TELOM	

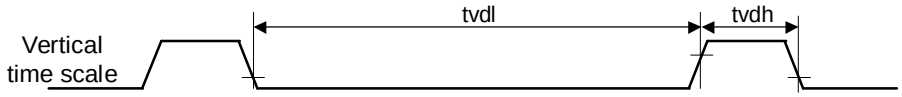
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.
-This output is not affected by changing MADCTL bit ML.
-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).

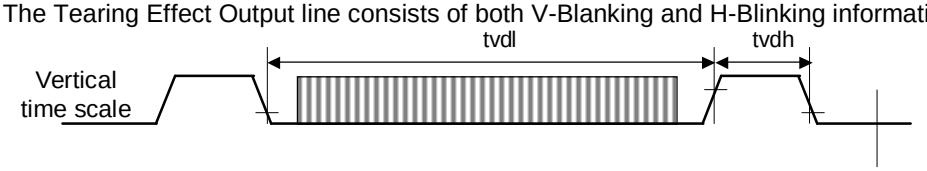
—When M='0':

The Tearing Effect Output line consists of V-Blanking information only.



—When M='1':

The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Default

Status	Default Value	
	RCM1,RCM0 = "00","1x"	RCM1,RCM0 = "01"
Power On Sequence	Tearing effect off & TELOM=0	Tearing effect on & TELOM=0
S/W Reset		
H/W Reset		

10.1.28 MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
1st Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0	00h

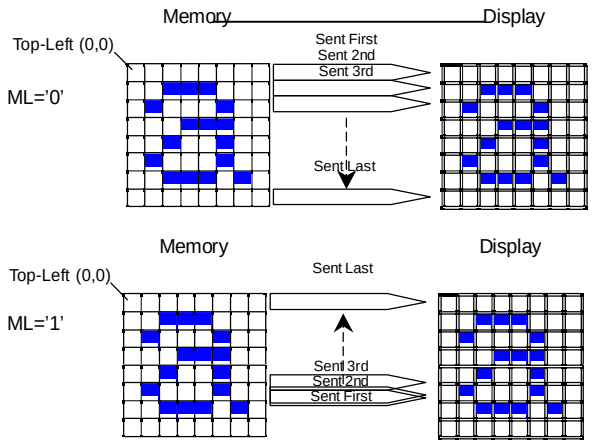
NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

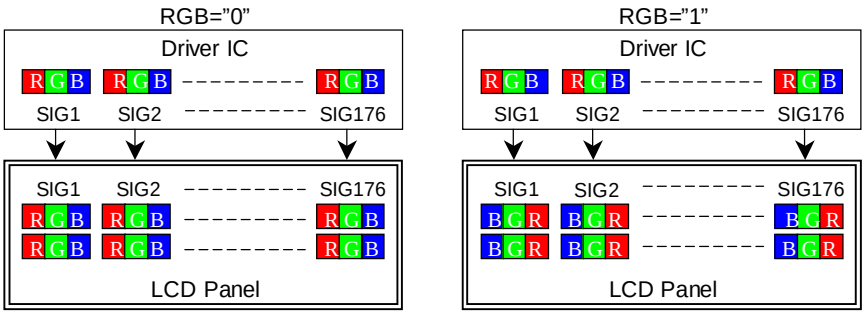
-This command defines read/ write scanning direction of frame memory.
-Bit Assignment

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction. (See Section 9.12)
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)
MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left

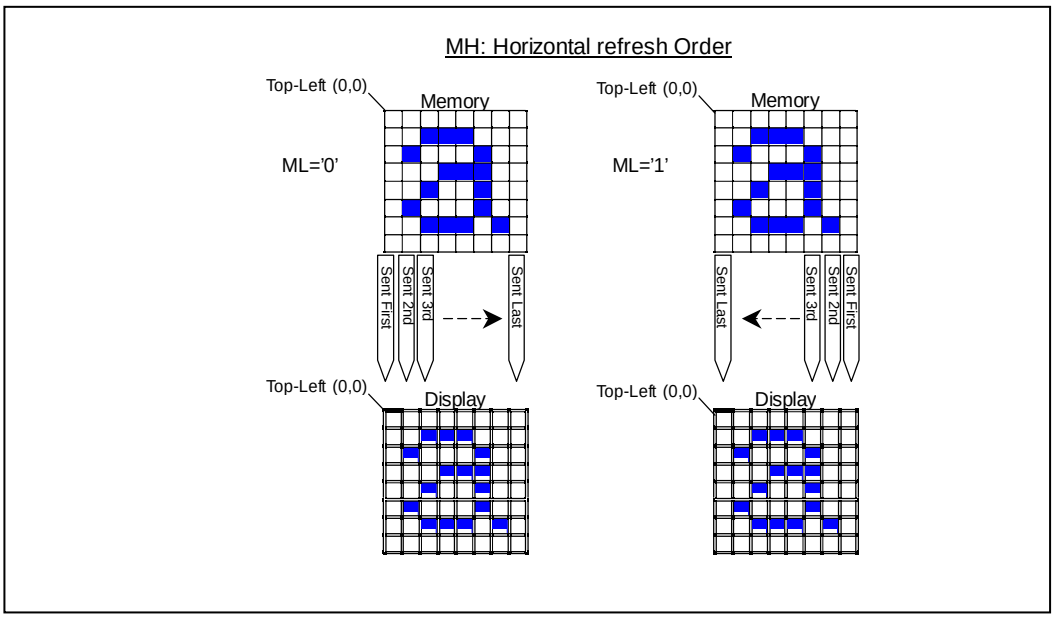
ML: Vertical Refresh Order



RGB: RGB-BGR Order



Description



Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0, MH=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0, MH=0

10.1.29 VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	SSA8	00h
2nd Parameter	1	↑	1		SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	00h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

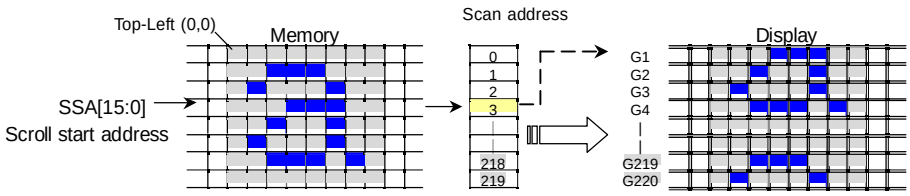
-This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
-This command Start the scrolling.
-Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTL ML= '0'

Example:

—When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=220 and Vertical Scrolling Pointer SSA= '3'.

(Example)

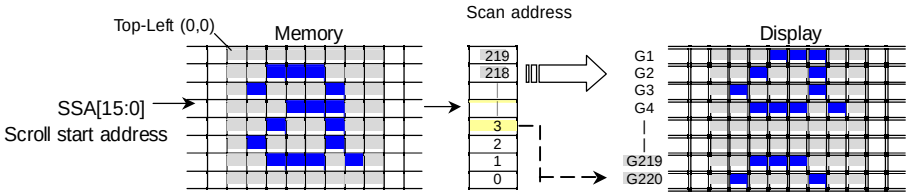


When MADCTL ML = '1'

Example:

—When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=220 and SSA= '3'

(Example)



NOTE: -When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
-SSA refers to the Frame Memory scan address.

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

10.1.30 IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description	-This command is used to recover from Idle mode on. -In the idle off mode, 1. LCD can display 4096, 65k or 262k colors. 2. Normal frame frequency is applied.
Default	

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

10.1.31 IDMON (39h): Idle Mode On

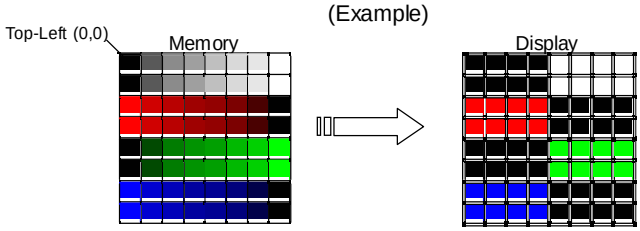
39H	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to enter into Idle mode on.
-There will be no abnormal visible effect on the display mode change transition.
-In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



Color	R_5 R_4 R_3 R_2 R_1 R_0	G_5 G_4 G_3 G_2 G_1 G_0	B_5 B_4 B_3 B_4 B_1 B_0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

10.1.32 COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (3Ah): Interface Pixel Format												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface and RGB interface. The formats are shown in the table:

IFPF[2:0]		MCU Interface Color Format
011	3	12-bit/pixel
101	5	16-bit/pixel
110	6	18-bit/pixel
111	7	No used

Others are no define and invalid

VIFPF[2:0]		RGB Interface Color Format
0101	5	16-bit/pixel (1-times data transfer)
0110	6	18-bit/pixel (1-times data transfer)
0111	7	No used
1110	14	18-bit/pixel (3-times data transfer)

Others are no define and invalid

Note1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

Note2: When RGB I/F the 12-bit/pixel don't care

Note 3: When VIPF[3:0]="1110",6-bit data width of 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Default

Status	Default Value	
	IFPF[2:0]	VIPF[3:0]
Power On Sequence	06H(18-bit/Pixel)	06H(18-bit/Pixel)
S/W Reset	No Change	No Change
H/W Reset	06H(18-bit/Pixel)	06H(18-bit/Pixel)

10.1.33 RDID1 (DAh): Read ID1 Value

DAH	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This read byte returns 8-bit LCD module's manufacturer ID

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

Default

Status	Default Value
Power On Sequence	29h
S/W Reset	29h
H/W Reset	29h

10.1.34 RDID2 (DBh): Read ID2 Value

DBH	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	'1'	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This read byte returns 8-bit LCD module/driver version ID
-The 1st parameter is dummy data
-The 2nd parameter (ID26 to ID20): LCD module/driver version ID
-Parameter Range: ID=80h to FFh

ID26 to ID20	Version	Changes
-		
-		
-		
-		
-		

NOTE: See command RDDID (04h), 3rd parameter.

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

10.1.35 RDID1 (DCh): Read ID3 Value

DAH	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID13	ID32	ID31	ID30	

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This read byte returns 8-bit LCD module/driver ID
-The 1st parameter is dummy data
-The 2nd parameter (ID17 to ID10): LCD module/driver ID.
NOTE: See command RDDID (04h), 4th parameter.

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

10.1.36 VSCTR1 (AEh): VSYNC Interface function control 1

DCH	RDID3 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSYNCOFF	0	↑	1	-	1	0	1	0	1	1	1	0	(AEh)
1st Parameter	1	↑	1	-	VSFP3	VSFP2	VSFP1	VSFP0	VSBP3	VSBP2	VSBP1	VSBP0	2Eh

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-Set the back porch and front porch on the VSYNC interface. The setting becomes effective as soon as the command is received.
-VSFP: Front porch set on VSYNC I/F
-VSBP: Back porch set on VSYNC I/F

VSBP[3:0] VSFP[3:0]		Front porch period(Line)	Back porch period(Line)
0000	0	Setting inhibited	Setting inhibited
0001	1	Setting inhibited	Setting inhibited
0010	2	2-lines	2-lines
0011	3	3-lines	3-lines
0100	4	4-lines	4-lines
0101	5	5-lines	5-lines
0110	6	6-lines	6-lines
0111	7	7-lines	7-lines
1000	8	8-lines	8-lines
1001	9	9-lines	9-lines
1010	10	10-lines	10-lines
1011	11	11-lines	11-lines
1100	12	12-lines	12-lines
1101	13	13-lines	13-lines
1110	14	14-lines	14-lines
1111	15	Setting inhibited	Setting inhibited

Default

Status	Default Value	
	VSFP[3:0]	VSBP[3:0]
Power On Sequence	02H	0EH
S/W Reset	No Change	No Change
H/W Reset	02H	0EH

10.2.1 RGBCTR (B0h): RGB signal control

B0H	RGBCTR (RGB signal control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBCTR	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1st Parameter	1	↑	1	-	0	0	SWX	ICM	DP	EP	HSP	VSP	00h

NOTE: "-" Don't care

Description

-Set the operation status on the RGB interface. The setting becomes effective as soon as the command is received.

-SWX: IDM,REV and SHUT H/W pin and S/W command setting control on RGB Mode 2

SWX	H/W pin and S/W command setting control on RGB Mode 2
0	-H/W pin active when Power on, H/W reset and S/W reset -H/W pin disable when S/w command setting have even been program
1	Only H/W pin function active

-ICM: GRAM Write/Read frequency and data input select on the RGB interface

ICM	Write/ Read frequency and input data select		
	Write cycle	Read cycle	Data input
0	PCLK	PCLK	D[17:0]
1	SCL	Internal oscillator	SDA
Symbol	Name	Clock polarity set for RGB Interface	
DP	PCLK polarity set	'1' = data fetched at the falling edge '0' = data fetched at the rising edge	
EP	Enable polarity set	'1' = Low enable for RGB interface '0' = High enable for RGB interface	
HSP	Hsync polarity set	'1' = High level sync clock '0' = Low level sync clock	
VSP	Vsync polarity set	'1' = High level sync clock '0' = Low level sync clock	

Default

Status	Default Value	
	ICM	DP/EP/HSP/VSP
Power On Sequence	00H	00/00/00/00 H
S/W Reset	00H	00/00/00/00 H
H/W Reset	00H	00/00/00/00 H

10.2.2 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	FRMCTR1 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D1 7-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st Parameter	1	↑	1	-	RTNA[7:0]								3Bh
2nd Parameter	1	↑	1	-				FPA[4:0]					04h
3rd Parameter	1	↑	1	-				BPA[4:0]					03h
Nth Parameter	1	↑	1	-	RTNA_VSYNC[7:0]								38h

NOTE: "-" Don't care

Description

-Set the frame frequency of the full colors normal mode,recommend to set under 110Hz.
-The frame frequency need to meet 60Hz±5% in this mode

$$\text{Frame rate(Hz)} = \frac{\text{OSC}}{(\text{RTNA}) * (220+\text{FPA}+\text{BPA})}$$

RTNA[7:0]		Frame Rate	RTNA[7:0]		Frame Rate
0100000	32	110	1010000	80	44
0100001	33	107	1010001	81	43
0100010	34	104	1010010	82	43
0100011	35	101	1010011	83	42
0100100	36	98	1010100	84	42
0100101	37	95	1010101	85	41
0100110	38	93	1010110	86	41
0100111	39	90	1010111	87	41
0101000	40	88	1011000	88	40
0101001	41	86	1011001	89	40
0101010	42	84	1011010	90	39
0101011	43	82	1011011	91	39
0101100	44	80	1011100	92	38
0101101	45	78	1011101	93	38
0101110	46	77	1011110	94	37
0101111	47	75	1011111	95	37
0110000	48	73	1100000	96	37
0110001	49	72	1100001	97	36
0110010	50	70	1100010	98	36
0110011	51	69	1100011	99	36
0110100	52	68	1100100	100	35
0110101	53	66	1100101	101	35
0110110	54	65	1100110	102	35
0110111	55	64	1100111	103	34
0111000	56	63	1101000	104	34
0111001	57	62	1101001	105	34
0111010	58	61	1101010	106	33
0111011	59	60	1101011	107	33
0111100	60	59	1101100	108	33
0111101	61	58	1101101	109	32
0111110	62	57	1101110	110	32
0111111	63	56	1101111	111	32
1000000	64	55	1110000	112	31
1000001	65	54	1110001	113	31
1000010	66	53	1110010	114	31
1000011	67	52	1110011	115	31
1000100	68	52	1110100	116	30
1000101	69	51	1110101	117	30
1000110	70	50	1110110	118	30
1000111	71	49	1110111	119	30
1001000	72	49	1111000	120	29
1001001	73	48	1111001	121	29
1001010	74	48	1111010	122	29
1001011	75	47	1111011	123	29
1001100	76	46	1111100	124	28

1001101	77	46	1111101	125	28
1001110	78	45	1111110	126	28
1001111	79	45	1111111	127	28

Note: OSC output fre. Is 800KHz, FPA=04H and BPA=03H

FPA[4:0]		Timing	BPA[4:0]		Timing
00000	0	0 line	00000	0	0 line
00001	1	1 line	00001	1	1 line
00010	2	2 lines	00010	2	2 lines
00011	3	3 lines	00011	3	3 lines
00100	4	4 lines	00100	4	4 lines
00101	5	5 lines	00101	5	5 lines
00110	6	6 lines	00110	6	6 lines
00111	7	7 lines	00111	7	7 lines
01000	8	8 lines	01000	8	8 lines
01001	9	9 lines	01001	9	9 lines
01010	10	10 lines	01010	10	10 lines
01011	11	11 lines	01011	11	11 lines
01100	12	12 lines	01100	12	12 lines
01101	13	13 lines	01101	13	13 lines
01110	14	14 lines	01110	14	14 lines
01111	15	15 lines	01111	15	15 lines
10000	16	16 lines	10000	16	16 lines
10001	17	17 lines	10001	17	17 lines
10010	18	18 lines	10010	18	18 lines
10011	19	19 lines	10011	19	19 lines
10100	20	20 lines	10100	20	20 lines
10101	21	21 lines	10101	21	21 lines
10110	22	22 lines	10110	22	22 lines
10111	23	23 lines	10111	23	23 lines
11000	24	24 lines	11000	24	24 lines
11001	25	25 lines	11001	25	25 lines
11010	26	26 lines	11010	26	26 lines
11011	27	27 lines	11011	27	27 lines
11100	28	28 lines	11100	28	28 lines
11101	29	29 lines	11101	29	29 lines
11110	30	30 lines	11110	30	30 lines
11111	31	31 lines	11111	31	31 lines

Default

Status	Default Value
Power On Sequence	3B/04/03/38 H
S/W Reset	-
H/W Reset	3B/04/03/38 H

10.2.3 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

B2H	FRMCTR2 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st Parameter	1	↑	1	-	RTNB[7:0]								3Bh
2nd Parameter	1	↑	1	-	-	-	-	FPB[4:0]					04h
3rd Parameter	1	↑	1	-	-	-	-	BPB[4:0]					03h

NOTE: "-" Don't care

Description

-Set the frame frequency of the full colors idle mode, ,recommend to set under 110Hz.
-The frame frequency need to meet 60Hz±5% in this mode

$$\text{Frame rate(Hz)} = \frac{\text{OSC}}{(\text{RTNB}) * (220+\text{FPB}+\text{BPB})}$$

RTNB[7:0]		Frame Rate	RTNB[7:0]		Frame Rate
0100000	32	110	1010000	80	44
0100001	33	107	1010001	81	43
0100010	34	104	1010010	82	43
0100011	35	101	1010011	83	42
0100100	36	98	1010100	84	42
0100101	37	95	1010101	85	41
0100110	38	93	1010110	86	41
0100111	39	90	1010111	87	41
0101000	40	88	1011000	88	40
0101001	41	86	1011001	89	40
0101010	42	84	1011010	90	39
0101011	43	82	1011011	91	39
0101100	44	80	1011100	92	38
0101101	45	78	1011101	93	38
0101110	46	77	1011110	94	37
0101111	47	75	1011111	95	37
0110000	48	73	1100000	96	37
0110001	49	72	1100001	97	36
0110010	50	70	1100010	98	36
0110011	51	69	1100011	99	36
0110100	52	68	1100100	100	35
0110101	53	66	1100101	101	35
0110110	54	65	1100110	102	35
0110111	55	64	1100111	103	34
0111000	56	63	1101000	104	34
0111001	57	62	1101001	105	34
0111010	58	61	1101010	106	33
0111011	59	60	1101011	107	33
0111100	60	59	1101100	108	33
0111101	61	58	1101101	109	32
0111110	62	57	1101110	110	32
0111111	63	56	1101111	111	32
1000000	64	55	1110000	112	31
1000001	65	54	1110001	113	31
1000010	66	53	1110010	114	31
1000011	67	52	1110011	115	31
1000100	68	52	1110100	116	30
1000101	69	51	1110101	117	30
1000110	70	50	1110110	118	30
1000111	71	49	1110111	119	30
1001000	72	49	1111000	120	29
1001001	73	48	1111001	121	29
1001010	74	48	1111010	122	29
1001011	75	47	1111011	123	29
1001100	76	46	1111100	124	28
1001101	77	46	1111101	125	28
1001110	78	45	1111110	126	28

1001111	79	45	1111111	127	28

Note: OSC output fre. Is 800KHz, FPB=04H and BPB=03H

FPB[4:0]		Timing	BPB[4:0]		Timing
00000	0	0 line	00000	0	0 line
00001	1	1 line	00001	1	1 line
00010	2	2 lines	00010	2	2 lines
00011	3	3 lines	00011	3	3 lines
00100	4	4 lines	00100	4	4 lines
00101	5	5 lines	00101	5	5 lines
00110	6	6 lines	00110	6	6 lines
00111	7	7 lines	00111	7	7 lines
01000	8	8 lines	01000	8	8 lines
01001	9	9 lines	01001	9	9 lines
01010	10	10 lines	01010	10	10 lines
01011	11	11 lines	01011	11	11 lines
01100	12	12 lines	01100	12	12 lines
01101	13	13 lines	01101	13	13 lines
01110	14	14 lines	01110	14	14 lines
01111	15	15 lines	01111	15	15 lines
10000	16	16 lines	10000	16	16 lines
10001	17	17 lines	10001	17	17 lines
10010	18	18 lines	10010	18	18 lines
10011	19	19 lines	10011	19	19 lines
10100	20	20 lines	10100	20	20 lines
10101	21	21 lines	10101	21	21 lines
10110	22	22 lines	10110	22	22 lines
10111	23	23 lines	10111	23	23 lines
11000	24	24 lines	11000	24	24 lines
11001	25	25 lines	11001	25	25 lines
11010	26	26 lines	11010	26	26 lines
11011	27	27 lines	11011	27	27 lines
11100	28	28 lines	11100	28	28 lines
11101	29	29 lines	11101	29	29 lines
11110	30	30 lines	11110	30	30 lines
11111	31	31 lines	11111	31	31 lines

Default

Status	Default Value
Power On Sequence	3B/04/03 H
S/W Reset	-
H/W Reset	3B/04/03 H

10.2.34FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3H	FRMCTR3 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st Parameter	1	↑	1	-	RTNC[7:0]								3Bh
2nd Parameter	1	↑	1	-				FPC[4:0]					04h
3rd Parameter	1	↑	1	-				BPC[4:0]					03h

NOTE: "-" Don't care

Description

-Set the frame frequency of the full colors partial mode,recommend to set under 110Hz.
-The frame frequency need to meet 60Hz±5% in this mode

$$\text{Frame rate(Hz)} = \frac{\text{OSC}}{(\text{RTNC}) * (220+\text{FPC}+\text{BPC})}$$

RTNC[7:0]		Frame Rate	RTNC[7:0]		Frame Rate
0100000	32	110	1010000	80	44
0100001	33	107	1010001	81	43
0100010	34	104	1010010	82	43
0100011	35	101	1010011	83	42
0100100	36	98	1010100	84	42
0100101	37	95	1010101	85	41
0100110	38	93	1010110	86	41
0100111	39	90	1010111	87	41
0101000	40	88	1011000	88	40
0101001	41	86	1011001	89	40
0101010	42	84	1011010	90	39
0101011	43	82	1011011	91	39
0101100	44	80	1011100	92	38
0101101	45	78	1011101	93	38
0101110	46	77	1011110	94	37
0101111	47	75	1011111	95	37
0110000	48	73	1100000	96	37
0110001	49	72	1100001	97	36
0110010	50	70	1100010	98	36
0110011	51	69	1100011	99	36
0110100	52	68	1100100	100	35
0110101	53	66	1100101	101	35
0110110	54	65	1100110	102	35
0110111	55	64	1100111	103	34
0111000	56	63	1101000	104	34
0111001	57	62	1101001	105	34
0111010	58	61	1101010	106	33
0111011	59	60	1101011	107	33
0111100	60	59	1101100	108	33
0111101	61	58	1101101	109	32
0111110	62	57	1101110	110	32
0111111	63	56	1101111	111	32
1000000	64	55	1110000	112	31
1000001	65	54	1110001	113	31
1000010	66	53	1110010	114	31
1000011	67	52	1110011	115	31
1000100	68	52	1110100	116	30
1000101	69	51	1110101	117	30
1000110	70	50	1110110	118	30
1000111	71	49	1110111	119	30
1001000	72	49	1111000	120	29
1001001	73	48	1111001	121	29
1001010	74	48	1111010	122	29
1001011	75	47	1111011	123	29
1001100	76	46	1111100	124	28
1001101	77	46	1111101	125	28
1001110	78	45	1111110	126	28
1001111	79	45	1111111	127	28

Note: OSC output fre. Is 800KHz, FPC=04H and BPC=03H

FPC[4:0]		Timing	BPC[4:0]		Timing
00000	0	0 line	00000	0	0 line
00001	1	1 line	00001	1	1 line
00010	2	2 lines	00010	2	2 lines
00011	3	3 lines	00011	3	3 lines
00100	4	4 lines	00100	4	4 lines
00101	5	5 lines	00101	5	5 lines
00110	6	6 lines	00110	6	6 lines
00111	7	7 lines	00111	7	7 lines
01000	8	8 lines	01000	8	8 lines
01001	9	9 lines	01001	9	9 lines
01010	10	10 lines	01010	10	10 lines
01011	11	11 lines	01011	11	11 lines
01100	12	12 lines	01100	12	12 lines
01101	13	13 lines	01101	13	13 lines
01110	14	14 lines	01110	14	14 lines
01111	15	15 lines	01111	15	15 lines
10000	16	16 lines	10000	16	16 lines
10001	17	17 lines	10001	17	17 lines
10010	18	18 lines	10010	18	18 lines
10011	19	19 lines	10011	19	19 lines
10100	20	20 lines	10100	20	20 lines
10101	21	21 lines	10101	21	21 lines
10110	22	22 lines	10110	22	22 lines
10111	23	23 lines	10111	23	23 lines
11000	24	24 lines	11000	24	24 lines
11001	25	25 lines	11001	25	25 lines
11010	26	26 lines	11010	26	26 lines
11011	27	27 lines	11011	27	27 lines
11100	28	28 lines	11100	28	28 lines
11101	29	29 lines	11101	29	29 lines
11110	30	30 lines	11110	30	30 lines
11111	31	31 lines	11111	31	31 lines

Default

Status	Default Value
Power On Sequence	3B/04/03 H
S/W Reset	-
H/W Reset	3B/04/03 H

10.2.5 INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	

NOTE: "-" Don't care

Description

-Display Inversion mode control

-NLA: Inversion setting in full colors normal mode (Normal mode on)

NLA	Inversion setting in full Colors normal mode
0	**Line Inversion**
1	Frame Inversion

-NLB: Inversion setting in Idle mode (Idle mode on)

NLB	Inversion setting in Idle mode
0	Line Inversion
1	**Frame Inversion**

-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLC	Inversion setting in full Colors partial mode
0	**Line Inversion**
1	Frame Inversion

Default

Status	Default Value			
	NLA	NLB	NLC	B4h
Power On Sequence	0d	1d	0d	02h
S/W Reset	No Change	No Change	No Change	No Change
H/W Reset	0d	1d	0d	02h

10.2.6 RGBBPCTR (B5h): RGB Interface Blanking Porch setting

B5H	RGBPSET (RGB Interface Blanking Porch setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBBPCTR	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
1st Parameter	1	↑	1	-	VFPR[7:0]								-
2nd Parameter	1	↑	1	-	VBPR[7:0]								-
3rd Parameter	1	↑	1	-			HFPR[5:0]						-
4th Parameter	1	↑	1	-			HBPR[5:0]						-

NOTE: "-" Don't care

Description

-Set the blanking porch in the RGB interface

-The detail settings are designed by driver maker

Default

Status	Default Value			
	VFPR[7:0]	VBPR[7:0]	HFPR[5:0]	HBPR[5:0]
Power On Sequence	01H	03H	0AH	0AH
S/W Reset	01H	03H	0AH	0AH
H/W Reset	01H	03H	0AH	0AH

10.2.7 DISSET5 (B6h): Display Function set 5

B6H	DISSET (Display Function set 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET5	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)
1st Parameter	1	↑	1	-	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ0	15h
2nd Parameter	1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0	00h

NOTE: "-" Don't care

Description

-1st parameter: Set output waveform relation.

-NO[1:0]: Set the amount of non-overlap of the gate output

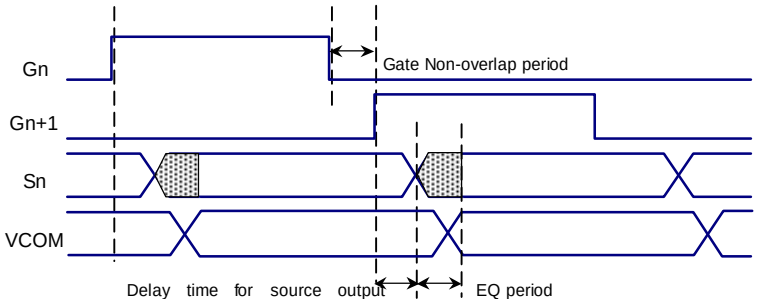
NO[1:0]		Amount of non-overlap of the gate output	
		Refer the Internal oscillator	Refer the PCLK
00	0	No	4 clock cycle
01	1	1 clock cycle	16 clock cycle
10	2	4 clock cycle	24 clock cycle
11	3	6 clock cycle	32 clock cycle

-SDT[1:0]: Set delay amount from gate signal falling edge of the source output.

SDT[1:0]		Amount of non-overlap of the gate output	
		Refer the Internal oscillator	Refer the PCLK
00	0	No	4 clock cycle
01	1	1 clock cycle	8 clock cycle
10	2	2 clock cycle	12clock cycle
11	3	3 clock cycle	16 clock cycle

-EQ[1:0]: Set the Equalizing period

EQ[1:0]		Amount of non-overlap of the gate output	
		Refer the Internal oscillator	Refer the PCLK
00	0	No EQ	No EQ
01	1	2 clock cycle	4 clock cycle
10	2	4 clock cycle	16 clock cycle
11	3	6 clock cycle	24 clock cycle



-2nd parameter: Set the output waveform in non-display area.

-PTG[1:0]: Determine gate output in a non-display area in the partial mode

PTG[1:0]		Gate output in a non-display area
00	0	Normal scan
01	1	Fix on VGL
10	2	Fix on VGL
11	3	Fix on VGL

-PT[1:0]: Determine Source /VCOM output in a non-display area in the partial mode

PT[1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive	Negative	Positive	Negative
00	0	V63	V0	VCOML	VCOMH
01	1	V0	V63	VCOML	VCOMH
10	2	AGND	AGND	AGND	AGND
11	3	Hi-z	Hi-z	AGND	AGND

Default	Status	Default Value				
		NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]
	Power On Sequence	01H	01H	01H	01H	10H
	S/W Reset	01H	01H	01H	01H	10H
	H/W Reset	01H	01H	01H	01H	10H

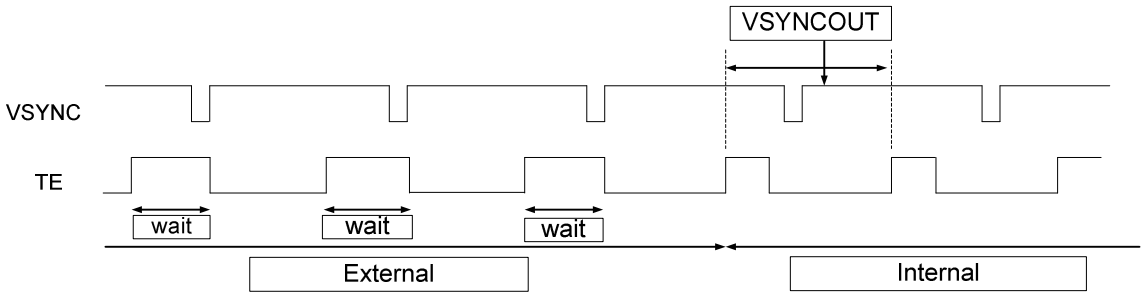
10.2.8 SRGBOFF (BCh): VSYNC Interface OFF

DCH	RDID3 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSYNCOFF	0	↑	1	-	1	0	1	1	1	1	0	0	(BCh)
1st Parameter	No Parameter												

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

This command comes off external VSYNC a display synchronous.



Operation shifts to an internal synchronous mode by the VSYNCOUT command while external VSYNC is synchronizing. VSYNCOUT command is recognized frame synchronously. The shift operation becomes the same for the VSYNCOUT command issued within the range of the inside of the figure.

Restriction

-If this register not using the register need be reserved.

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	
H/W Reset	

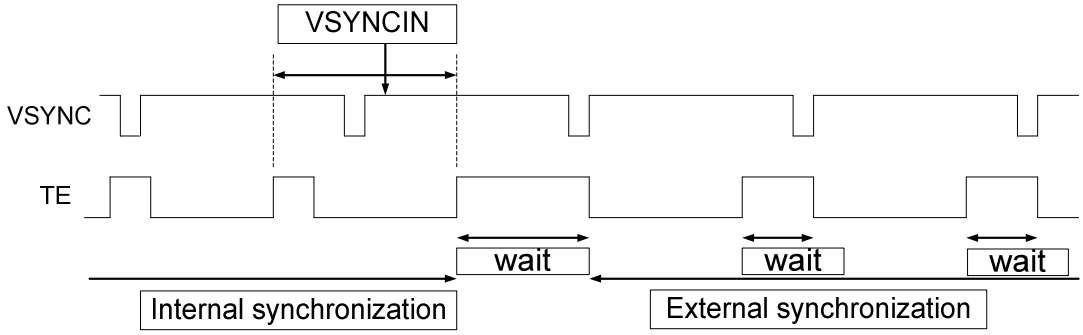
10.2.9 SRGBON (BDh): VSYNC Interface ON

DCH	RDID3 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSYNCON	0	↑	1	-	1	0	1	1	1	1	0	1	(BDh)
1st Parameter	No Parameter												

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-The frame to which the command is input finishes sending data by an internal vertical synchronizing signal. Afterward, an external vertical synchronizing signal is waiting for at the rest period. The operation after that becomes external synchronous. Operation enters the rest period when the transmission of data ends for one frame while the external is synchronizing.



wait: Synchronous waiting period.
Operation is external VSYNC perceives "L" level of the VSYNC signal and internal operate and after synchronization t, scans the display for one frame. External VSYNC signal through TE pin.

Operation enters the synchronous waiting period again when the display sacanning ends.

Restriction

-If this register not using the register need be reserved.

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	
H/W Reset	

10.2.10 PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st Parameter	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	

NOTE: "-" Don't care

Description

-Set the GVDD and VCI1 voltage

VRH[4:0]		GVDD
00000	0	5.00
00001	1	4.75
00010	2	4.70
00011	3	4.65
00100	4	4.60
00101	5	**4.55**
00110	6	4.50
00111	7	4.45
01000	8	4.40
01001	9	4.35
01010	10	4.30
01011	11	4.25
01100	12	4.20
01101	13	4.15
01110	14	4.10
01111	15	4.05
10000	16	4.00
10001	17	3.95
10010	18	3.90
10011	19	3.85
10100	20	3.80
10101	21	3.75
10110	22	3.70
10111	23	3.65
11000	24	3.60
11001	25	3.55
11010	26	3.50
11011	27	3.45
11100	28	3.40
11101	29	3.35
11110	30	3.25
11111	31	3.00

VC[2:0]		VCI1
000	0	2.75
001	1	2.70
010	2	2.65
011	3	2.60
100	4	2.55
101	5	2.50
110	6	reserved
111	7	reserved

Default

Status	Default Value	
	TM LC type	
	VRH[4:0]	VC[2:0]
Power On Sequence	05H	01H
S/W Reset	05H	01H
H/W Reset	05H	01H

10.2.11 PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st Parameter	1	↑	1		VGH3	VGH2	VGH1	VGH0	VGL3	VGL2	VGL1	VGL0	BBh

NOTE: "-" Don't care

Description

-Set the VGH and VGL supply power level

VGH[3:0]/VGL[3:0]		VGH	VGL
0000	0	10	-5.5
0001	1	10.5	-6
0010	2	11	-7.5
0011	3	11.5	-8
0100	4	12	-8.5
0101	5	12.5	-9
0110	6	13	-9.5
0111	7	13.5	-10
1000	8	14	-10.5
1001	9	14.5	-11
1010	10	15	-11.5
1011	11	15.5	-12
1100	12	16	-12.5
1101	13	16.5	-13
1110	14	X	-13.5
1111	15	X	X

Unit(V)

Default

Status	Default Value	
	VGH[3:0]	VGL[3:0]
Power On Sequence	-	-
S/W Reset	0Bh	0Bh
H/W Reset	0Bh	0Bh

10.2.12 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st Parameter	1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0	04h

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in normal mode/full colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APA[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

Default

Status	Default Value
	APA[2:0]
Power On Sequence	-
S/W Reset	04h
H/W Reset	04h

10.2.13 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st Parameter	1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0	

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in Idle mode/8 colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APB[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

Default

Status	Default Value
	APB[2:0]
Power On Sequence	-
S/W Reset	04h
H/W Reset	04h

10.2.14 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0	04h

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in Partial mode/ full-colors.
-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APC[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

Default

Status	Default Value
	APC[2:0]
Power On Sequence	-
S/W Reset	04h
H/W Reset	04h

10.2.15 VMCTR1 (C5h): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st Parameter	1	↑	1	-	0	VMH6	VMH5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	3Ch
2nd Parameter	1	↑	1	-	0	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	3Ch

NOTE: "-" Don't care

Description

-Set VCOMH Voltage

VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH
0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525
0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550
0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575
0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600
0000100	4	2.600	0011111	31	3.275	0111010	58	3.950	1010101	85	4.625
0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650
0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675
0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700
0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725
0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750
0001010	10	2.750	0100101	37	3.425	1000000	64	4.100	1011011	91	4.775
0001011	11	2.775	0100110	38	3.450	1000001	65	4.125	1011100	92	4.800
0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825
0001101	13	2.825	0101000	40	3.500	1000011	67	4.175	1011110	94	4.850
0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875
0001111	15	2.875	0101010	42	3.550	1000101	69	4.225	1100000	96	4.900
0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925
0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950
0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975
0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000
0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101	Not Permitted
0010101	21	3.025	0110000	48	3.700	1001011	75	4.375		|	
0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	1111111	127	
0010111	23	3.075	0110010	50	3.750	1001101	77	4.425			
0011000	24	3.100	0110011	51	3.775	1001110	78	4.450			
0011001	25	3.125	0110100	52	3.800	1001111	79	4.475			
0011010	26	3.150	0110101	53	3.825	1010000	80	4.500			

-Set VCOML Voltage

VML[6:0]		VCOML	VML[6:0]		VCOML	VML[6:0]		VCOML	VML[6:0]		VCOML
0000000	0	-2.500	0011011	27	-1.825	0110110	54	-1.150	1010001	81	-0.475
0000001	1	-2.475	0011100	28	-1.800	0110111	55	-1.125	1010010	82	-0.450
0000010	2	-2.450	0011101	29	-1.775	0111000	56	-1.100	1010011	83	-0.425
0000011	3	-2.425	0011110	30	-1.750	0111001	57	-1.075	1010100	84	-0.400
0000100	4	-2.400	0011111	31	-1.725	0111010	58	-1.050	1010101	85	-0.375
0000101	5	-2.375	0100000	32	-1.700	0111011	59	-1.025	1010110	86	-0.350
0000110	6	-2.350	0100001	33	-1.675	0111100	60	-1.000	1010111	87	-0.325
0000111	7	-2.325	0100010	34	-1.650	0111101	61	-0.975	1011000	88	-0.300
0001000	8	-2.300	0100011	35	-1.625	0111110	62	-0.950	1011001	89	-0.275
0001001	9	-2.275	0100100	36	-1.600	0111111	63	-0.925	1011010	90	-0.250
0001010	10	-2.250	0100101	37	-1.575	1000000	64	-0.900	1011011	91	-0.225
0001011	11	-2.225	0100110	38	-1.550	1000001	65	-0.875	1011100	92	-0.200
0001100	12	-2.200	0100111	39	-1.525	1000010	66	-0.850	1011101	93	-0.175
0001101	13	-2.175	0101000	40	-1.500	1000011	67	-0.825	1011110	94	-0.150
0001110	14	-2.150	0101001	41	-1.475	1000100	68	-0.800	1011111	95	-0.125
0001111	15	-2.125	0101010	42	-1.450	1000101	69	-0.775	1100000	96	-0.100
0010000	16	-2.100	0101011	43	-1.425	1000110	70	-0.750	1100001	97	-0.075
0010001	17	-2.075	0101100	44	-1.400	1000111	71	-0.725	1100010	98	-0.050
0010010	18	-2.050	0101101	45	-1.375	1001000	72	-0.700	1100011	99	-0.025
0010011	19	-2.025	0101110	46	-1.350	1001001	73	-0.675	1100100	100	0.000
0010100	20	-2.000	0101111	47	-1.325	1001010	74	-0.650	1100101	101	Not Permitted
0010101	21	-1.975	0110000	48	-1.300	1001011	75	-0.625		|	
0010110	22	-1.950	0110001	49	-1.275	1001100	76	-0.600	1111111	127	
0010111	23	-1.925	0110010	50	-1.250	1001101	77	-0.575			
0011000	24	-1.900	0110011	51	-1.225	1001110	78	-0.550			
0011001	25	-1.875	0110100	52	-1.200	1001111	79	-0.525			
0011010	26	-1.850	0110101	53	-1.175	1010000	80	-0.500			

Default	Status	Default Value
		LCM = “01” TM LC type
		VMH[6:0] / VML[6:0]
	Power On Sequence	-
	S/W Reset	3Ch / 3C h
	H/W Reset	3Ch / 3Ch

10.2.16 VMOFCTR (C7h): VCOM Offset Control

C7H	VMOFCTR (VCOM Offset Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMOFCTR	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)
1st Parameter	1	↑	1	-	0	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	3Ch

NOTE: “-“ Don’t care, can be set to VDDI or DGND level

Description

-Set VCOM Voltage level for reduce the flicker issue

VMF[6:0]	VCOMH Output Level	VCOML Output Level
4	“VMH”-64d	“VML”-60d
5	“VMH”-63d	“VML”-59d
6	“VMH”-62d	“VML”-58d
|	|	|
58	“VMH”-2d	“VML”-2d
59	“VMH”-1d	“VML”-1d
60	“VMH”	“VML”
61	“VMH”+1d	“VML”+1d
62	“VMH”+2d	“VML”+2d
|	|	|
126	“VMH”+62d	“VML”+62d
127	“VMH”+63d	“VML”+63d

-IF “VMH”-xd or “VML”-xd is less than 0d, it becomes 0d.
-IF”VMH”+xd or “VML”+xd is large than 100d, it becomes 100d.
-VMF[6:0] are stored in NV memory to contrast.

-The nVM need be used in 1st parameter of VMOFCTR (C7h)

Default

Status	Default Value VMF[5:0]
Power Mode On Sequence	3Ch
S/W Reset	3Ch
H/W Reset	3Ch

10.2.17 STEP CTR (C9h): step1/2/4 booster frequency control

BEH	RDVMOF (Read the VCOM Offset Value NV memory)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDVMOF	0	↑	1	-	1	1	0	0	1	0	0	1	(C9h)
1st Parameter	1	↑	1	-	DUAL_EN	STEP_DIV_EN	1	0	0	CP1_FREQ_SEL[2:0]			A4h
2nd Parameter	1	↑	1	-	NW_MODE	0	0	0	0	CP2_FREQ_SEL[2:0]			04h
2nd Parameter	1	↑	1	-	0	0	0	0	0	CP4_FREQ_SEL[2:0]			04h

NOTE: "-" Don't care

Description

DUAL_EN：STEP1/2/4 booster mode select, default：1(Dual mode)

STEP_DIV_EN：STEP1/2/3 CLK select OSC frequency divid 4 enable,0(default),1：divid 4

NW_MODE：select panel type,0=Normally White,1=Normally Black

STEP_DIV_EN	CP1_FREQ_SEL[2:0]		Step-up cycle in Booster circuit1	CP2_FREQ_SEL[2:0]		Step-up cycle in Booster circuit 2
0/1	000	0	OSC/1024, OSC/4096	000	0	OSC/1024, OSC/4096
0/1	001	1	OSC/512, OSC/2048	001	1	OSC/512, OSC/2048
0/1	010	2	OSC/256, OSC/1024	010	2	OSC/256, OSC/1024
0/1	011	3	OSC/128, OSC/512	011	3	OSC/128, OSC/512
0/1	100	4	OSC/64, OSC/256	100	4	OSC/64, OSC/256
0/1	101	5	OSC/32, OSC/128	101	5	OSC/32, OSC/128
0/1	110	6	OSC/16, OSC/64	110	6	OSC/16, OSC/64
0/1	111	7	OSC/8, OSC/32	111	7	OSC/8, OSC/32

STEP_DIV_EN	CP4_FREQ_SEL[2:0]		Step-up cycle in Booster circuit4
0/1	000	0	OSC/1024, OSC/4096
0/1	001	1	OSC/512, OSC/2048
0/1	010	2	OSC/256, OSC/1024
0/1	011	3	OSC/128, OSC/512
0/1	100	4	OSC/64, OSC/256
0/1	101	5	OSC/32, OSC/128
0/1	110	6	OSC/16, OSC/64
0/1	111	7	OSC/8, OSC/32

Default

Status	Default Value
Power On Sequence	-
S/W Reset	A4h/04h/04h
H/W Reset	A4h/04h/04h

10.2.18 8-color (F8h): 8 color detect function

F8H	VMOFCTR (VCOM Offset Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
8-color detect	0	↑	1	-	1	1	1	1	1	0	0	0	(F8h)
1st Parameter	1	↑	1	-	0	0	0	0	0	8-color	0	0	04h

NOTE: "-" Don't care, can be set to VDDI or DGND level

Description

-This command is used to turn on/off 8-color detect function

1：enable 8-color detect function

0：disable 8-color detect function

Default

Status	Default Value
Power On Sequence	04h
S/W Reset	04h
H/W Reset	04h

10.2.19 PWCTR6 (FCh): Power Control 6

FCH	RDVMOF (Read the VCOM Offset Value NV memory)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR6	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)
1st Parameter	1	↑	1	-	0	0	1	1	1	SAPA[2:0]			3Ch
2nd Parameter	1	↑	1	-	0	1	1	1	1	SAPB[2:0]			7Ch
2nd Parameter	1	↑	1	-	0	0	0	0	0	SAPC[2:0]			04h

NOTE: "-" Don't care

Description

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the gate driver.

-SAPA[2:0]：Set the amount of current in Operational amplifier in Normal mode.

SAPA[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	4	Medium High
101	5	Large Low
110	6	Large
111	7	Large High

-SAPB[2:0]：Set the amount of current in Operational amplifier in Idle mode.

SAPA[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	4	Medium High
101	5	Large Low
110	6	Large
111	7	Large High

-SAPC[2:0]：Set the amount of current in Operational amplifier in Partial/Full color mode.

SAPC[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	4	Medium High
101	5	Large Low
110	6	Large
111	7	Large High

Default

Status	Default Value
	SAPA[2:0]/ SAPB[2:0]/SAPC[2:0]
Power On Sequence	-
S/W Reset	3C/7C/04h
H/W Reset	3C/7C/04h

10.2.20 WRID2 (D1h): Write ID2 Value

D1H	WRID2 (Write ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
1st Parameter	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description	-Write 7-bit data of LCD module version to save it to NV memory. -The 1st parameter ID2[6:0] is LCD Module version ID.
Default	

Status	Default Value
Power On Sequence	Not fixed
S/W Reset	Not fixed
H/W Reset	Not fixed

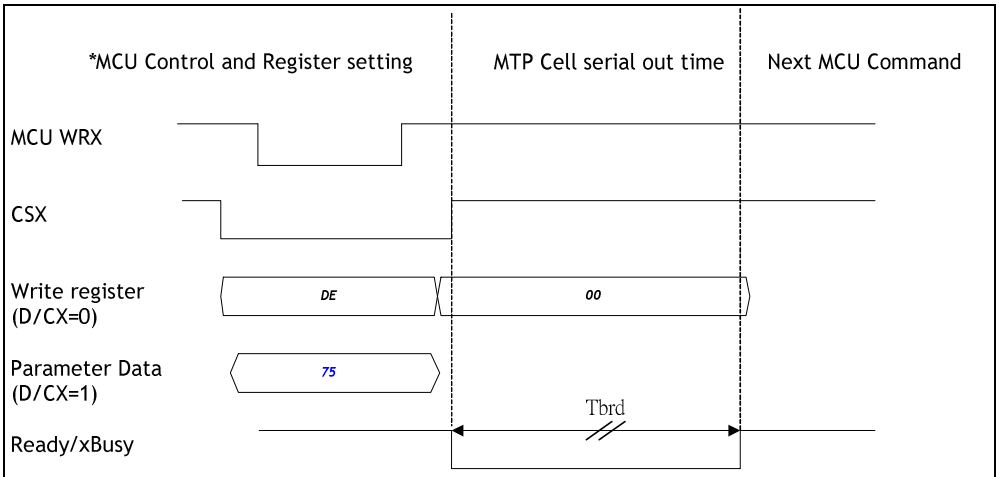
10.2.21 NVFCTR2 (DEh): NV Memory Function Controller 2

DEH	NVFCTR1 (NV Memory Function Controller 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR1	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)
1st Parameter	1	↑	1		0	1	0	1	0	1	0	1	75

NOTE: "-" Don't care

Description

1. MTP burst read



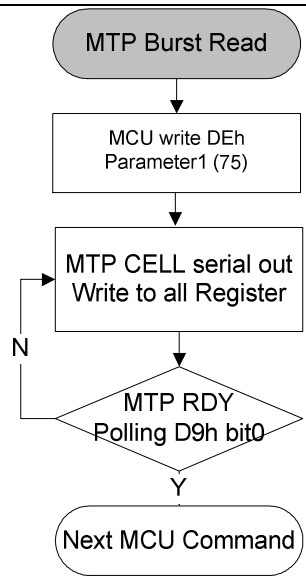
* Please refer to 8080-series/6800-series MCU Interface timing

		MIN	MAX	Unit	
Tbrd	Burst read waiting time	58	464	us	

Fig. MTP Burst read timing

Default

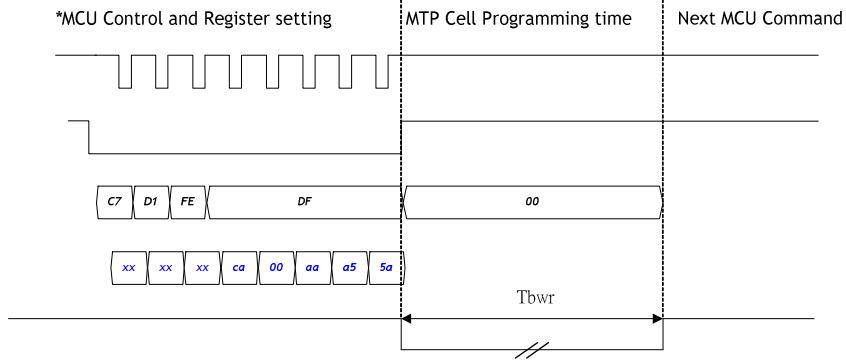
Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart	 Fig. MTP burst read flow

10.2.22 NVFCTR3 (DFh): NV Memory Function Controller 3

DFH	NVFCTR1 (NV Memory Function Controller 3												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR1	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
1st Parameter	1	↑	1	-	1	1	0	0	1	0	1	0	CA
2ndParameter	1	↑	1	-	0	0	0	0	0	0	0	0	00
3rd Parameter	1	↑	1	-	1	0	1	0	1	0	1	0	AA
4rd Parameter	1	↑	1	-	1	0	1	0	0	1	0	1	A5
5rd Parameter	1	↑	1	-	0	1	0	1	1	0	1	0	5A

NOTE: "-" Don't care

Description	MTP Write Command
Description	1. MTP burst write  * Please refer to 8080-series/6800-series MCU Interface timing Fig. MTP Burst write timing

		MIN	MAX	Unit	
Tbwr	Burst write programming time	71	568	ms	

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart

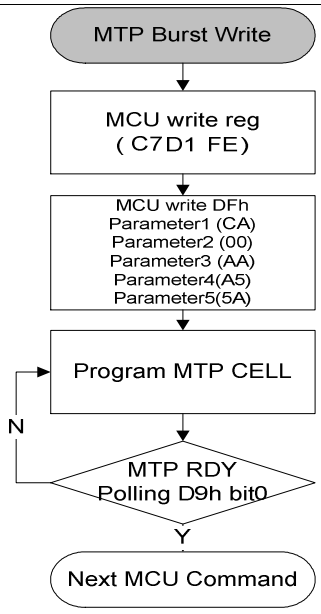


Fig. MTP burst write flow

10.2.23 GMCTRP1 (E0h): Gamma ('+'polarity) Correction Characteristics Setting

E0H	GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st Parameter	1	↑	1	-	-	-	VRF0P[5]	VRF0P[4]	VF0P[3]	VRF0P[2]	VRF0P[1]	VRF0P[0]	
2nd Parameter	1	↑	1	-	-	-	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]	
3rd Parameter	1	↑	1	-	-	-	PK0P[5]	PK0P[4]	PK0P[3]	PK0P[2]	PK0P[1]	PK0P[0]	
4th Parameter	1	↑	1	-	-	-	PK1P[5]	PK1P[4]	PK1P[3]	PK1P[2]	PK1P[1]	PK1P[0]	
5thParameter	1	↑	1	-	-	-	PK2P[5]	PK2P[4]	PK2P[3]	PK2P[2]	PK2P[1]	PK2P[0]	
6th Parameter	1	↑	1	-	-	-	PK3P[5]	PK3P[4]	PK3P[3]	PK3P[2]	PK3P[1]	PK3P[0]	
7th Parameter	1	↑	1	-	-	-	PK4P[5]	PK4P[4]	PK4P[3]	PK4P[2]	PK4P[1]	PK4P[0]	
8th Parameter	1	↑	1	-	-	-	PK5P[5]	PK5P[4]	PK5P[3]	PK5P[2]	PK5P[1]	PK5P[0]	
9th Parameter	1	↑	1	-	-	-	PK6P[5]	PK6P[4]	PK6P[3]	PK6P[2]	PK6P[1]	PK6P[0]	
10th Parameter	1	↑	1	-	-	-	PK7P[5]	PK7P[4]	PK7P[3]	PK7P[2]	PK7P[1]	PK7P[0]	
11th Parameter	1	↑	1	-	-	-	PK8P[5]	PK8P[4]	PK8P[3]	PK8P[2]	PK8P[1]	PK8P[0]	
12th Parameter	1	↑	1	-	-	-	PK9P[5]	PK9P[4]	PK9P[3]	PK9P[2]	PK9P[1]	PK9P[0]	
13th Parameter	1	↑	1	-	-	-	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]	
14th Parameter	1	↑	1	-	-	-	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]	
15th Parameter	1	↑	1	-	-	-	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]	
16th Parameter	1	↑	1	-	-	-	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]	

NOTE: "-" Don't care

	Register Group	Negative Polarity	Set-up Contents
Description	High level adjustment	VRF0P[5:0]	Variable resistor VRHP
	Mid level adjustment	SELV0P[5:0]	The voltage of grayscale number 0 is selected by the 64 to 1 selector
		SELV1P[5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
		PK0P[5:0]	The voltage of grayscale number 3 is selected by the 64 to 1 selector
		PK1P[5:0]	The voltage of grayscale number 6 is selected by the 64 to 1 selector
		PK2P[5:0]	The voltage of grayscale number 11 is selected by the 64 to 1 selector
		PK3P[5:0]	The voltage of grayscale number 19 is selected by the 64 to 1 selector
		PK4P[5:0]	The voltage of grayscale number 27 is selected by the 64 to 1 selector
		PK5P[5:0]	The voltage of grayscale number 36 is selected by the 64 to 1 selector
		PK6P[5:0]	The voltage of grayscale number 44 is selected by the 64 to 1 selector
		PK7P[5:0]	The voltage of grayscale number 52 is selected by the 64 to 1 selector
		PK8P[5:0]	The voltage of grayscale number 57 is selected by the 64 to 1 selector
		PK9P[5:0]	The voltage of grayscale number 60 is selected by the 64 to 1 selector
		SELV62P[5:0]	The voltage of grayscale number 62 is selected by the 64 to 1 selector
		SELV63P[5:0]	The voltage of grayscale number 63 is selected by the 64 to 1 selector
	Low level adjustment	VOS0P[5:0]	Variable resistor VRLP

10.2.24 GMCTRN1 (E1h): Gamma '-'polarity Correction Characteristics Setting

E0H	GMCTRP0 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRN1	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1st Parameter	1	↑	1	-	-	-	VRF0N[5]	VRF0N[4]	VF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]	
2nd Parameter	1	↑	1	-	-	-	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]	
3rd Parameter	1	↑	1	-	-	-	PK0N[5]	PK0N[4]	PK0N[3]	PK0N[2]	PK0N[1]	PK0N[0]	
4th Parameter	1	↑	1	-	-	-	PK1N[5]	PK1N[4]	PK1N[3]	PK1N[2]	PK1N[1]	PK1N[0]	
5thParameter	1	↑	1	-	-	-	PK2N[5]	PK2N[4]	PK2N[3]	PK2N[2]	PK2N[1]	PK2N[0]	
6th Parameter	1	↑	1	-	-	-	PK3N[5]	PK3N[4]	PK3N[3]	PK3N[2]	PK3N[1]	PK3N[0]	
7th Parameter	1	↑	1	-	-	-	PK4N[5]	PK4N[4]	PK4N[3]	PK4N[2]	PK4N[1]	PK4N[0]	
8th Parameter	1	↑	1	-	-	-	PK5N[5]	PK5N[4]	PK5N[3]	PK5N[2]	PK5N[1]	PK5N[0]	
9th Parameter	1	↑	1	-	-	-	PK6N[5]	PK6N[4]	PK6N[3]	PK6N[2]	PK6N[1]	PK6N[0]	
10th Parameter	1	↑	1	-	-	-	PK7N[5]	PK7N[4]	PK7N[3]	PK7N[2]	PK7N[1]	PK7N[0]	
11th Parameter	1	↑	1	-	-	-	PK8N[5]	PK8N[4]	PK8N[3]	PK8N[2]	PK8N[1]	PK8N[0]	
12th Parameter	1	↑	1	-	-	-	PK9[5]	PK9N[4]	PK9N[3]	PK9N[2]	PK9N[1]	PK9N[0]	
13th Parameter	1	↑	1	-	-	-	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]	
14th Parameter	1	↑	1	-	-	-	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]	
15th Parameter	1	↑	1	-	-	-	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]	
16th Parameter	1	↑	1	-	-	-	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]	

NOTE: "-" Don't care

Description

Register Group	Negative Polarity	Set-up Contents
High level adjustment	VRF0N[5:0]	Variable resistor VRHN
Mid level adjustment	SELV0N[5:0]	The voltage of grayscale number 0 is selected by the 64 to 1 selector
	SELV1N[5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
	PK0N[5:0]	The voltage of grayscale number 3 is selected by the 64 to 1 selector
	PK1N[5:0]	The voltage of grayscale number 6 is selected by the 64 to 1 selector
	PK2N[5:0]	The voltage of grayscale number 11 is selected by the 64 to 1 selector
	PK3N[5:0]	The voltage of grayscale number 19 is selected by the 64 to 1 selector
	PK4N[5:0]	The voltage of grayscale number 27 is selected by the 64 to 1 selector
	PK5N[5:0]	The voltage of grayscale number 36 is selected by the 64 to 1 selector
	PK6N[5:0]	The voltage of grayscale number 44 is selected by the 64 to 1 selector
	PK7N[5:0]	The voltage of grayscale number 52 is selected by the 64 to 1 selector
	PK8N[5:0]	The voltage of grayscale number 57 is selected by the 64 to 1 selector
	PK9N[5:0]	The voltage of grayscale number 60 is selected by the 64 to 1 selector
	SELV62N[5:0]	The voltage of grayscale number 62 is selected by the 64 to 1 selector
	SELV63N[5:0]	The voltage of grayscale number 63 is selected by the 64 to 1 selector
Low level adjustment	VOS0N[5:0]	Variable resistor VRLN

11. Power structure

11.1. Driver IC Operating voltages Specification

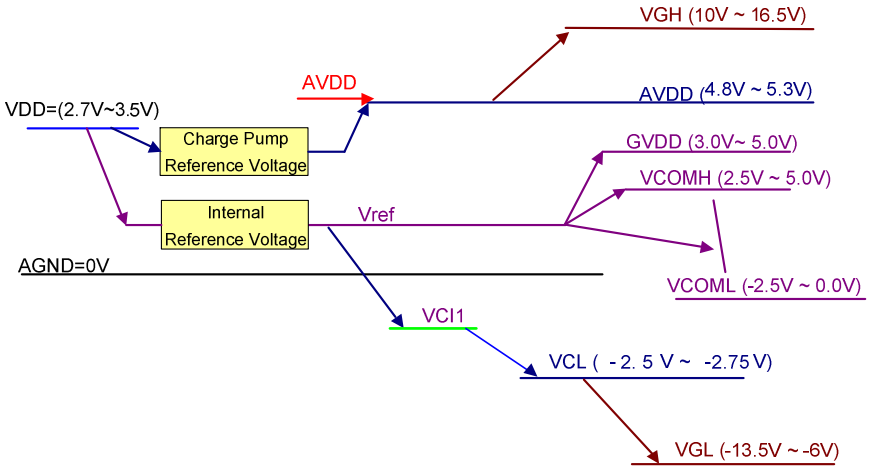


Fig. 11.1.1 Power Booster Level

Remark
1. AVDD supply to all power source (exclude VGH, VGL)
2. Source output range: 0.1V ~ AVDD-0.1V
3. Linear Range: 0.2V ~ AVDD-0.2V (For all output voltage, but exclude VGH, VGL)
4. Above operating voltages is min range.

11.2 Power Step1/2/4 Circuit

11.2.1 VCI1 generate frome Vref

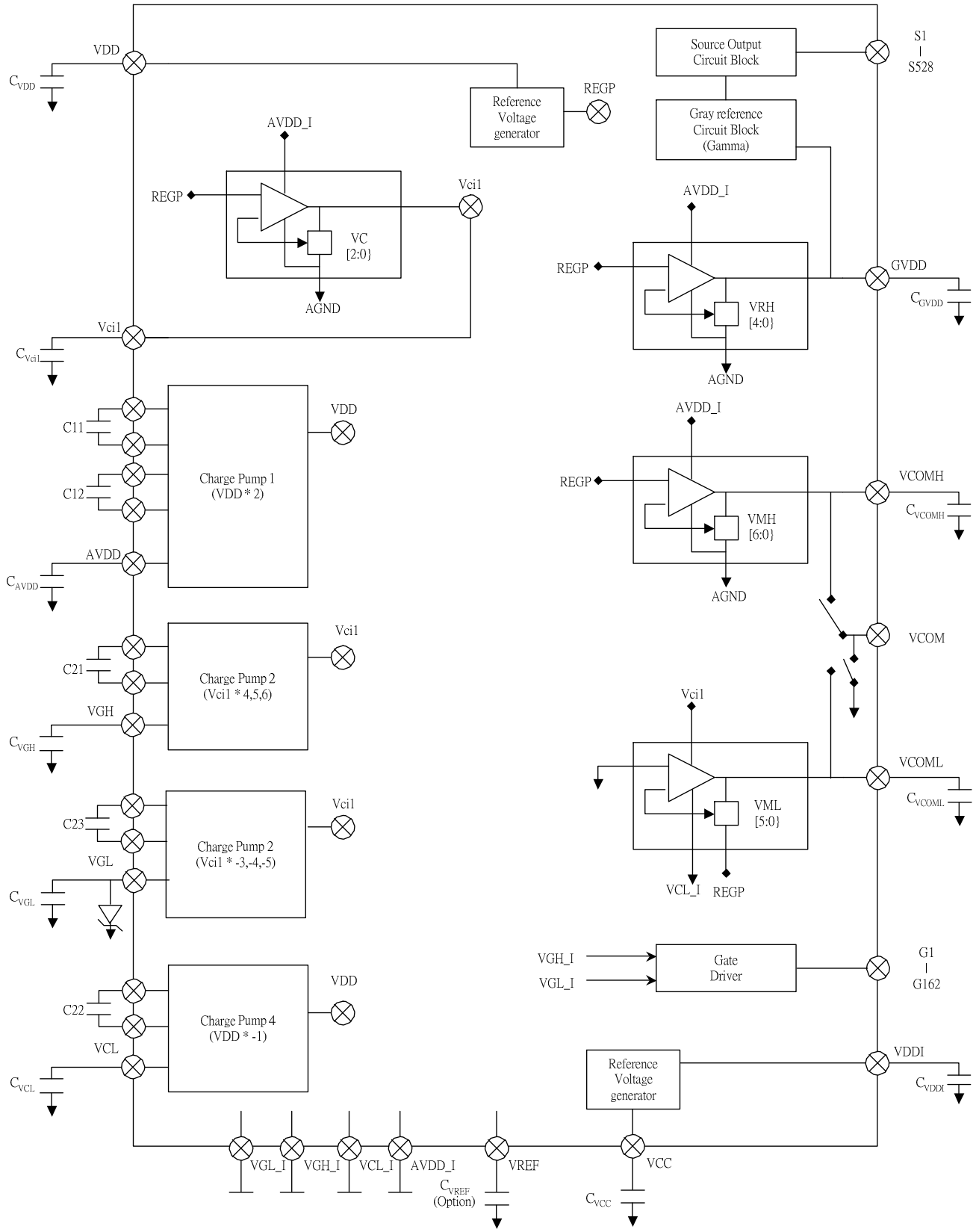


Fig. 11.2.1 Power Booster Structure (1)

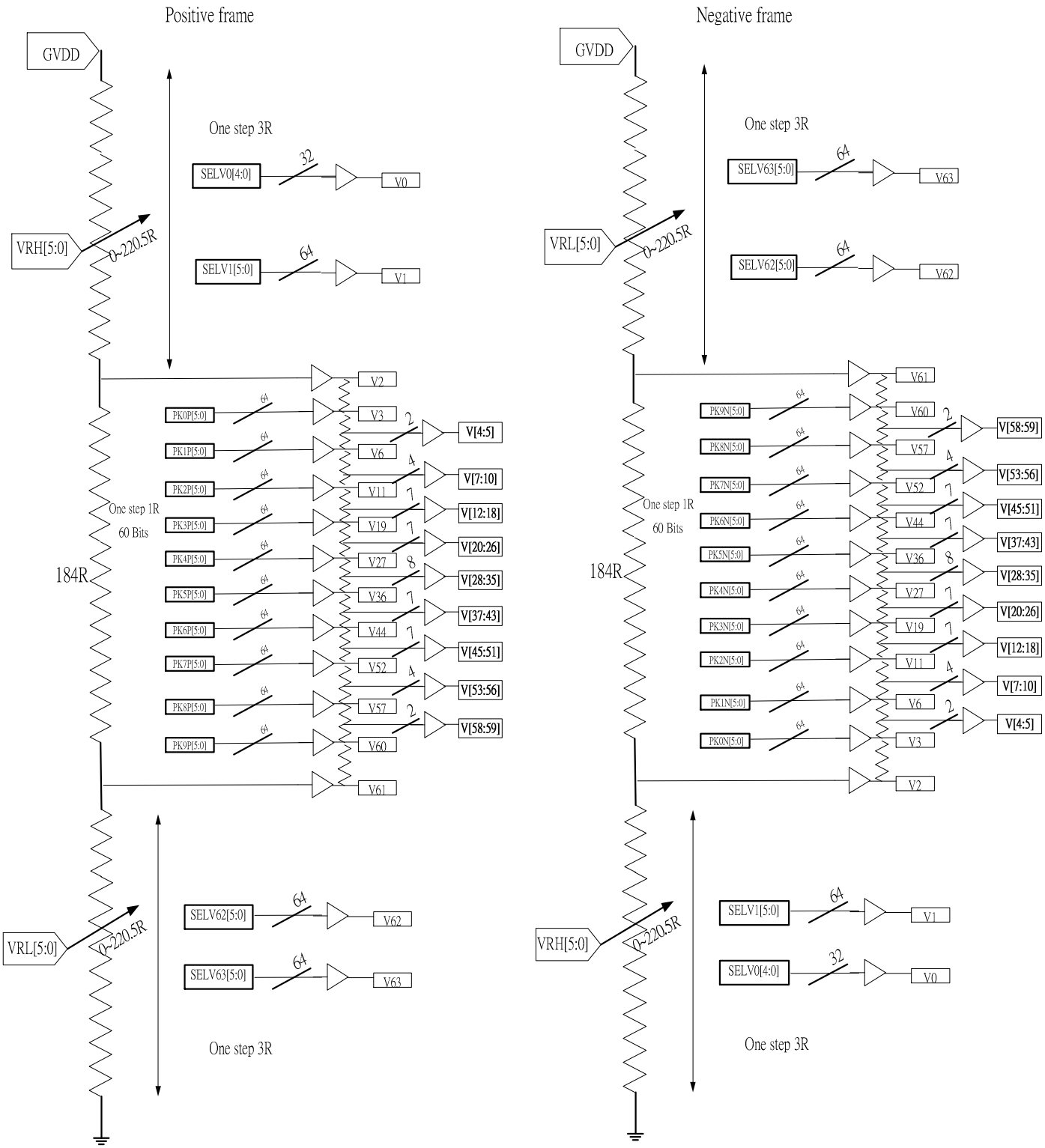
11.2.2 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Rated (Min) Voltage	Typical capacitance value
VDDI	VDDI (Logic Power)	10.0V	1.0 uF
VDD	VDD (Analog Power)	10.0V	1.0 uF
VCC	Connect to Capacitor (Max 3V): VCC -------||-------- GND	10.0V	1.0 uF
AGND	Analog ground (Connect to GND)		
DGND	Digital ground (Connect to GND)		
C23P, C23N	Connect to Capacitor: C23P -------||--------C23N	25.0V	1.0 uF
C22P, C22N	Connect to Capacitor: C22P -------||--------C22N	25.0V	1.0 uF
C21P, C22N	Connect to Capacitor: C21P -------||--- -----C21N	10.0V	1.0 uF
C12P, C12N	Connect to Capacitor: C12P -------||--------C12N	10.0V	1.0 uF
C11P, C11N	Connect to Capacitor: C11P -------||--------C11N	10.0V	1.0 uF
AVDD	Connect to Capacitor: AVDD -------||-------- GND	10.0V	1.0 uF
VCI1	Connect to Capacitor: AVDD -------||-------- GND	10.0V	1.0 uF
VGH	Connect to Capacitor: VGH -------||-------- GND	25.0V	1.0 uF
VGL	Connect to Capacitor: VGL -------||-------- GND	25.0V	1.0 uF
VCL	Connect to Capacitor: VCL -------||-------- GND	10.0V	1.0 uF
VREF	Connect to Capacitor: VREF -------||-------- GND(Optional)	10.0V	1.0 uF
GVDD	Connect to Capacitor: GVDD -------||-------- GND(Optional)	10.0V	1.0 uF
VCOMH	Connect to Capacitor: VCOMH-------||--------- GND	10.0V	1.0 uF
VCOML	Connect to Capacitor: VCOML -------||-------- GND	10.0V	1.0 uF
VGL	Connect to Schottky diode: VGL ----▶|-------- GND	30V	Schottky diode

12. Gamma structure

12.1 STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of grayscale amplifier is shown as below. 16 voltage levels (VIN0-VIN15) between GVDD and VGS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63 and outputs one of 64 levels.



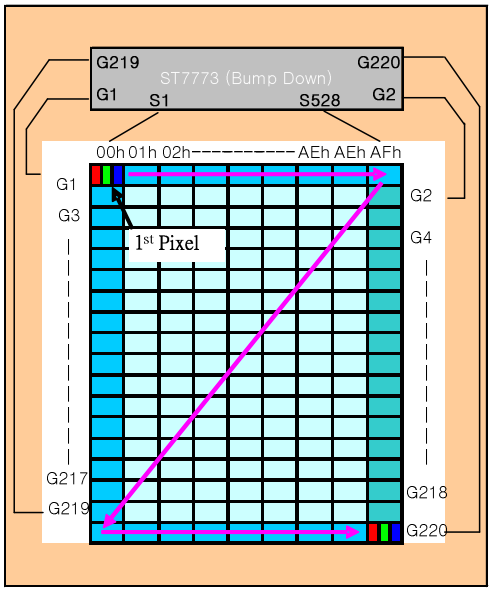
12.2 ST7773 Gamma Voltage Formula (Positive/ Negative Polarity)

Grayscale	Voltage Formula(Positive)	Voltage Formula(Negative)
0	VINP0	VINN0
1	VINP1	VINN1
2	VINP2	VINN2
3	VINP3	VINN3
4	V3-(V3-V6)*(11/30)	V3-(V3-V6)*(11/30)
5	V3-(V3-V6)*(21/30)	V3-(V3-V6)*(21/30)
6	VINP4	VINN4
7	V6-(V6-V11)*(7/30)	V6-(V6-V11)*(7/30)
8	V6-(V6-V11)*(14/30)	V6-(V6-V11)*(14/30)
9	V6-(V6-V11)*(20/30)	V6-(V6-V11)*(20/30)
10	V6-(V6-V11)*(25/30)	V6-(V6-V11)*(25/30)
11	VINP5	VINN5
12	V11-(V11-V19)*(4/32)	V11-(V11-V19)*(4/32)
13	V11-(V11-V19)*(8/32)	V11-(V11-V19)*(8/32)
14	V11-(V11-V19)*(12/32)	V11-(V11-V19)*(12/32)
15	V11-(V11-V19)*(16/32)	V11-(V11-V19)*(16/32)
16	V11-(V11-V19)*(20/32)	V11-(V11-V19)*(20/32)
17	V11-(V11-V19)*(24/32)	V11-(V11-V19)*(24/32)
18	V11-(V11-V19)*(28/32)	V11-(V11-V19)*(28/32)
19	VINP6	VINN6
20	V19-(V19-V27)*(4/32)	V19-(V19-V27)*(4/32)
21	V19-(V19-V27)*(8/32)	V19-(V19-V27)*(8/32)
22	V19-(V19-V27)* (12/32)	V19-(V19-V27)* (12/32)
23	V19-(V19-V27)* (1632/)	V19-(V19-V27)* (1632/)
24	V19-(V19-V27)* (20/32)	V19-(V19-V27)* (20/32)
25	V19-(V19-V27)* (24/32)	V19-(V19-V27)* (24/32)
26	V19-(V19-V27)* (28/32)	V19-(V19-V27)* (28/32)
27	VINP7	VINN7
28	V27-(V27-V36)* (4/36)	V27-(V27-V36)* (4/36)
29	V27-(V27-V36)* (8/36)	V27-(V27-V36)* (8/36)
30	V27-(V27-V36)* (12/36)	V27-(V27-V36)* (12/36)
31	V27-(V27-V36)* (16/36)	V27-(V27-V36)* (16/36)
32	V27-(V27-V36)* (20/36)	V27-(V27-V36)* (20/36)
33	V27-(V27-V36)* (24/36)	V27-(V27-V36)* (24/36)
34	V27-(V27-V36)* (28/36)	V27-(V27-V36)* (28/36)
35	V27-(V27-V36)* (32/36)	V27-(V27-V36)* (32/36)
36	VINP8	VINN8
37	V36-(V36-V44)*(4/32)	V36-(V36-V44)*(4/32)
38	V36-(V36-V44)*(8/32)	V36-(V36-V44)*(8/32)
39	V36-(V36-V44)*(12/32)	V36-(V36-V44)*(12/32)
40	V36-(V36-V44)*(16/32)	V36-(V36-V44)*(16/32)
41	V36-(V36-V44)*(20/32)	V36-(V36-V44)*(20/32)
42	V36-(V36-V44)*(24/32)	V36-(V36-V44)*(24/32)
43	V36-(V36-V44)*(28/32)	V36-(V36-V44)*(28/32)
44	VINP9	VINN9
45	V44-(V44-V52)*(4/32)	V44-(V44-V52)*(4/32)
46	V44-(V44-V52)*(8/32)	V44-(V44-V52)*(8/32)
47	V44-(V44-V52)*(12/32)	V44-(V44-V52)*(12/32)
48	V44-(V44-V52)*(16/32)	V44-(V44-V52)*(16/32)
49	V44-(V44-V52)*(20/32)	V44-(V44-V52)*(20/32)
50	V44-(V44-V52)*(24/32)	V44-(V44-V52)*(24/32)
51	V44-(V44-V52)*(28/32)	V44-(V44-V52)*(28/32)
52	VINP10	VINN10
53	V52-(V52-V57)*(5/30)	V52-(V52-V57)*(5/30)
54	V52-(V52-V57)*(11/30)	V52-(V52-V57)*(11/30)

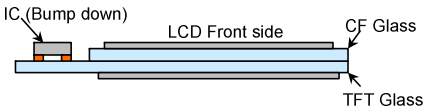
55	V52-(V52-V57)*(17/30)	V52-(V52-V57)*(17/30)
56	V52-(V52-V57)*(23/30)	V52-(V52-V57)*(23/30)
57	VINP11	VINN11
58	V57-(V57-V60)*(8/30)	V57-(V57-V60)*(8/30)
59	V57-(V57-V60)*(18/30)	V57-(V57-V60)*(18/30)
60	VINP12	VINN12
61	VINP13	VINN13
62	VINP14	VINN14
63	VINP15	VINN15

13. Example Connection with Panel direction and Different Resolution

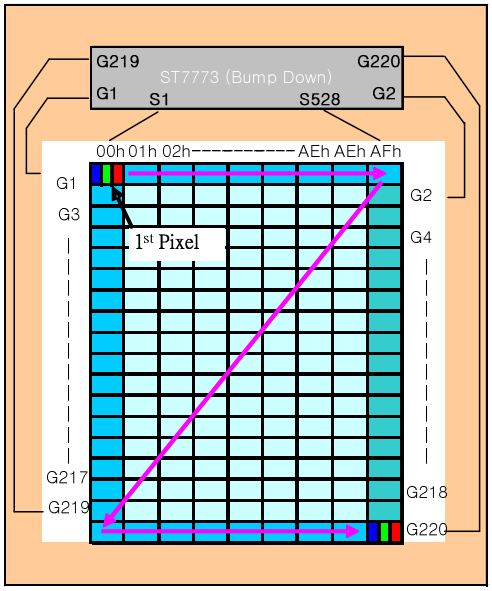
Case 1: (This is default case)
- 1st Pixel is at *Left Top* of the panel
- RGB filter order = RGB



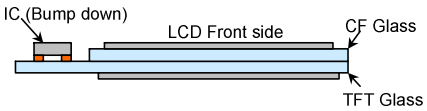
- Direction default setting (H/W)
  SMX = '0'
  SMY = '0'
  SRGB = '0'
  S1 = Filter R
  S2 = Filter G
  S3 = Filter B
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV



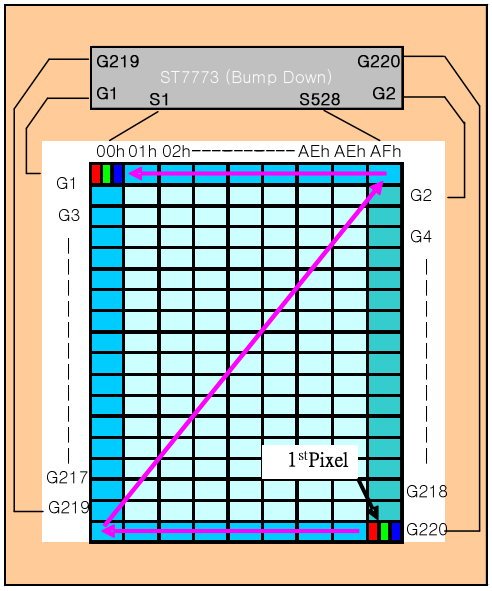
Case 2:
- 1st Pixel is at *Left Top* of the panel
- RGB filter order = BGR



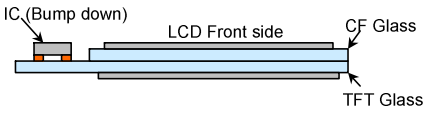
- Direction default setting (H/W)
  SMX = '0'
  SMY = '0'
  SRGB = '1'
  S1 = Filter B
  S2 = Filter G
  S3 = Filter R
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV



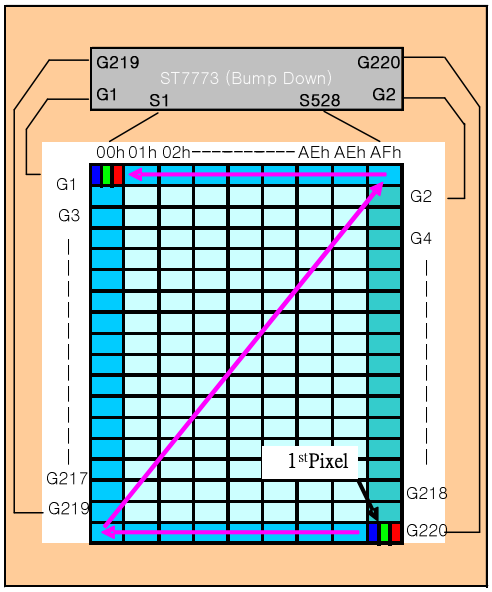
Case 3:
- 1st Pixel is at *Righ Bottom* of the panel
- RGB filter order = RGB



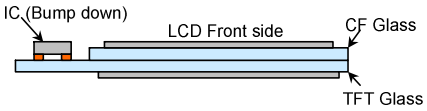
- Direction default setting (H/W)
  SMX = '1'
  SMY = '1'
  SRGB = '0'
  S1 = Filter R
  S2 = Filter G
  S3 = Filter B
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV



Case 4:
- 1st Pixel is at *Righ Bottom* of the panel
- RGB filter order = BGR



- Direction default setting (H/W)
  SMX = '1'
  SMY = '1'
  SRGB = '1'
  S1 = Filter B
  S2 = Filter G
  S3 = Filter R
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV



13.3 MicroProcessor Interface applications

13.3.1 8080-Seriers MCU + SPI Interface (RCM = ‘0x’, P68=’0’, IM2=’1’, VSYNCOFF(ACh))

13.3.1.1 8080-Series MCU Interface for 8-bit data bus (IM1, IM0=”00”)

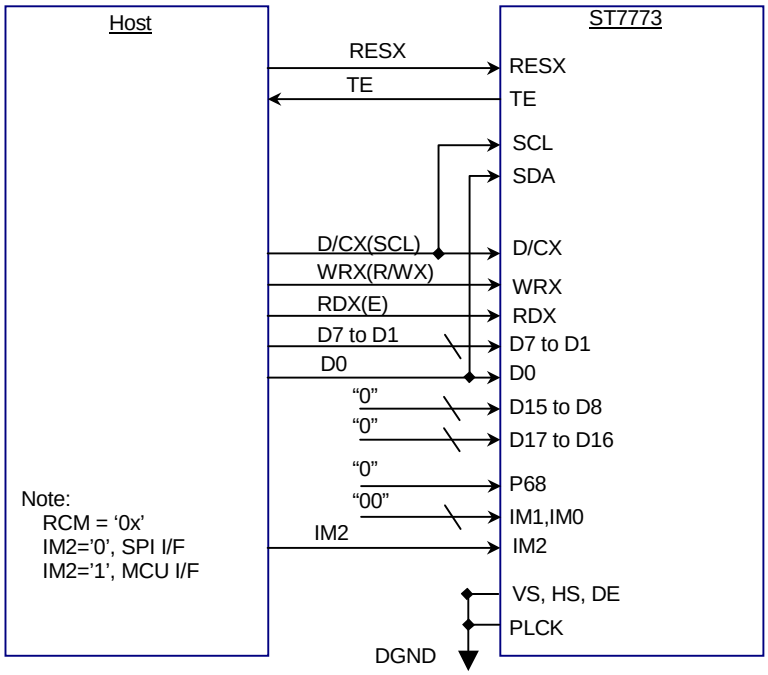


Fig. 13.3.1.1 8080-Series MCU Interface for 8-bit data bus

13.3.1.2 8080-Series MCU Interface for 16-bit data bus (IM1, IM0=”01”)

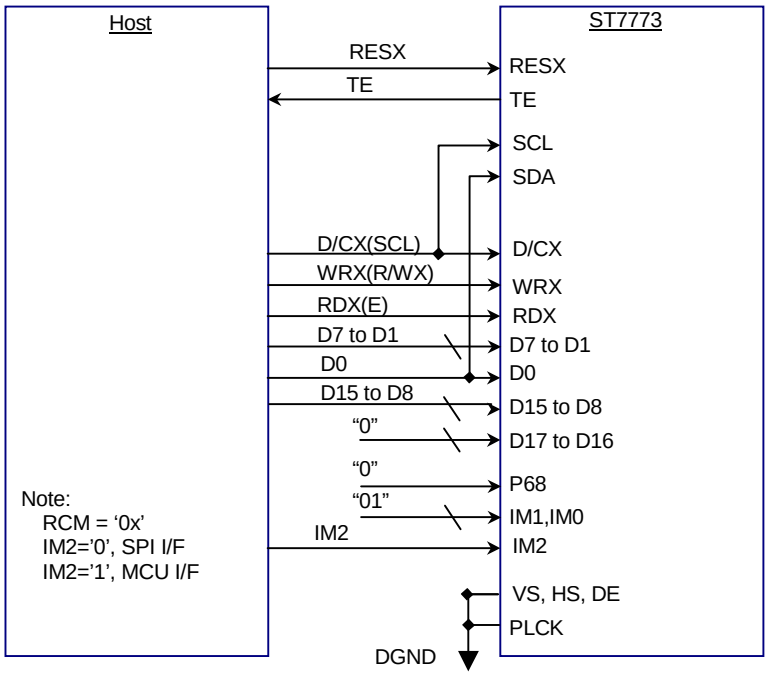


Fig. 13.3.1.2 8080-Series MCU Interface for 16-bit data bus

13.3.1.3 8080-Series MCU Interface for 9-bit data bus (IM1, IM0=”10”)

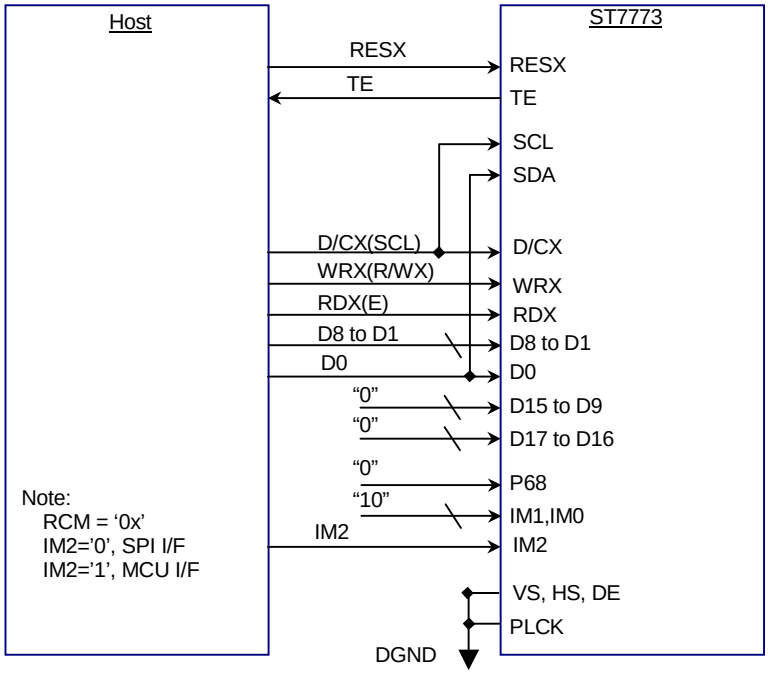


Fig. 13.3.1.3 8080-Series MCU Interface for 9-bit data bus

12.3.1.4 8080-Series MCU Interface for 18-bit data bus (IM1, IM0=”11”)

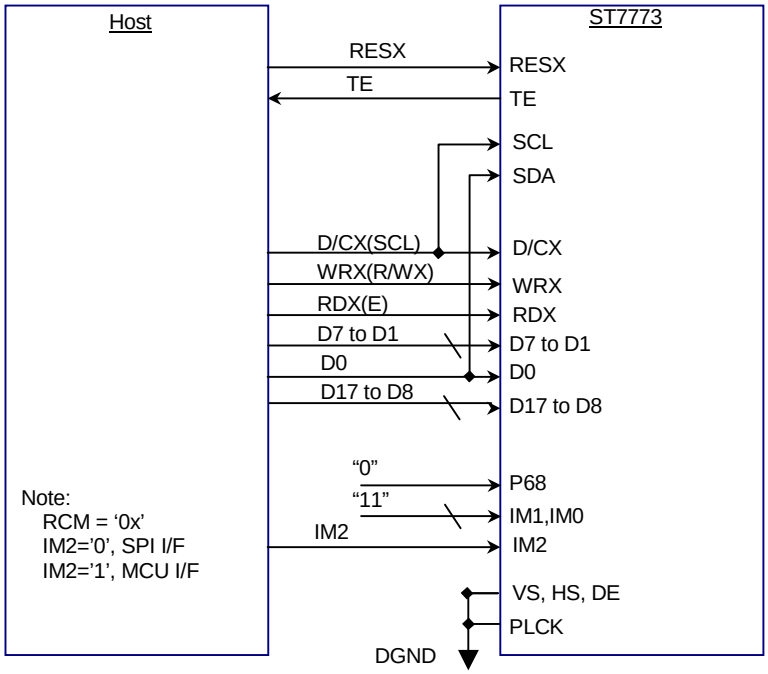


Fig. 13.3.1.4 8080-Series MCU Interface for 18-bit data bus

13.3.2 6800-Seriers MCU + SPI Interface (RCM = ‘0x’, P68=’1’, IM2=’1’, VSYNCOFF(ACh))

13.3.2.1 6800-Series MCU Interface for 8-bit data bus (IM1, IM0=”00”)

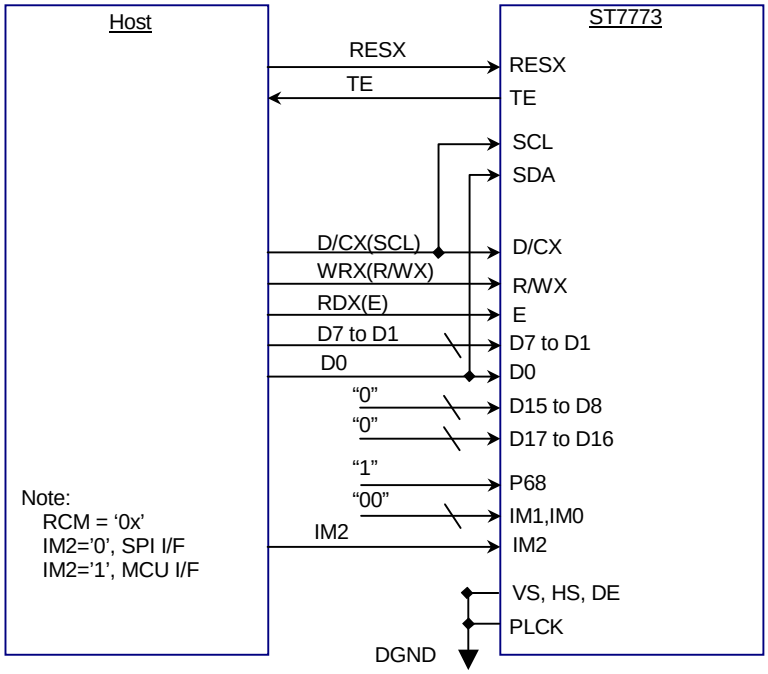


Fig. 13.3.2.1 6800-Series MCU Interface for 8-bit data bus

13.3.2.2 6800-Series MCU Interface for 16-bit data bus (IM1, IM0=”01”)

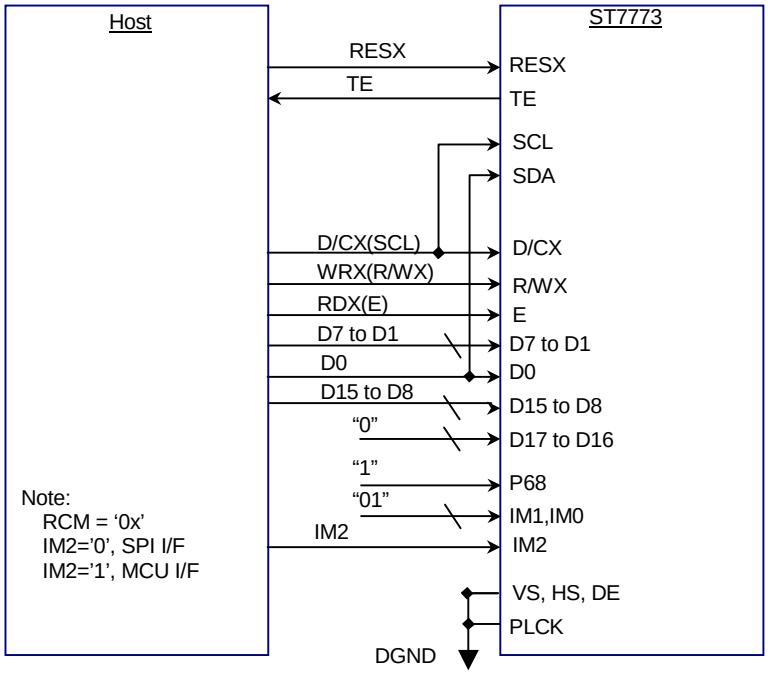


Fig. 13.3.2.2 6800-Series MCU Interface for 16-bit data bus

13.3.2.3 6800-Series MCU Interface for 9-bit data bus (IM1, IM0=”10”)

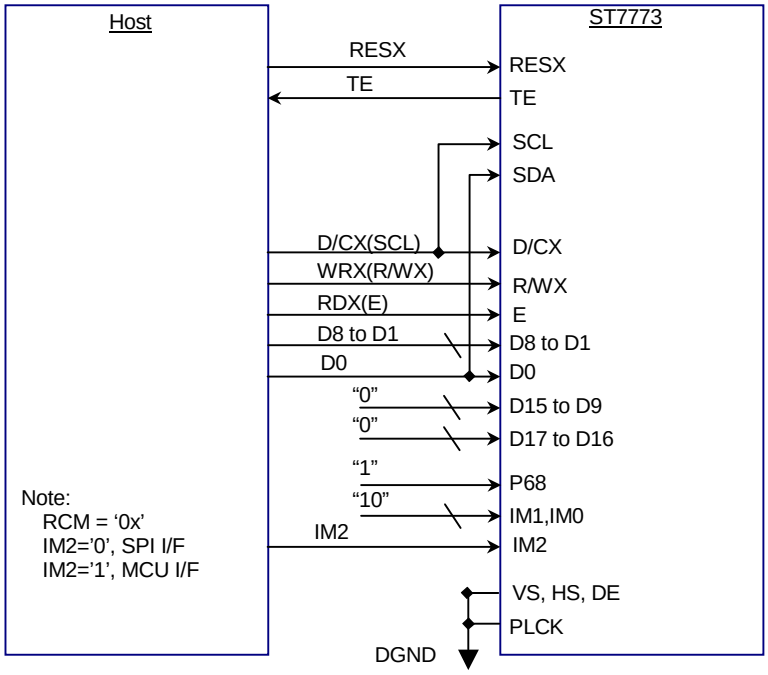


Fig. 13.3.2.3 6800-Series MCU Interface for 9-bit data bus

13.3.2.4 6800-Series MCU Interface for 18-bit data bus (IM1, IM0=”11”)

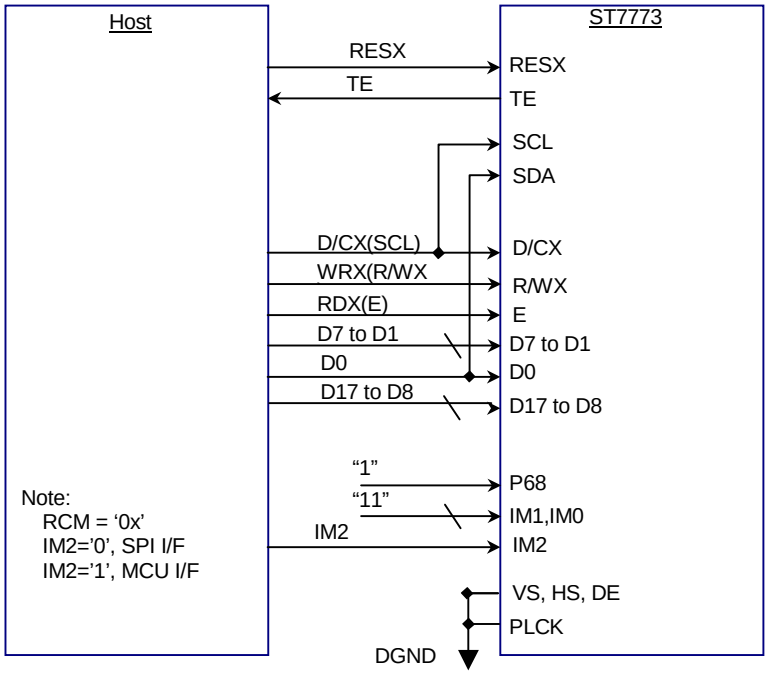


Fig. 13.3.2.4 6800-Series MCU Interface for 18-bit data bus

13.3.3SPI Interface (RCM = ‘0x’, P68=’0’, IM2=’0’, VSYNCOFF(ACh))

13.3.4 RGB Interface (RCM = ‘1’)

13.3.4.1 RGBInterface for 6-bit Data Width

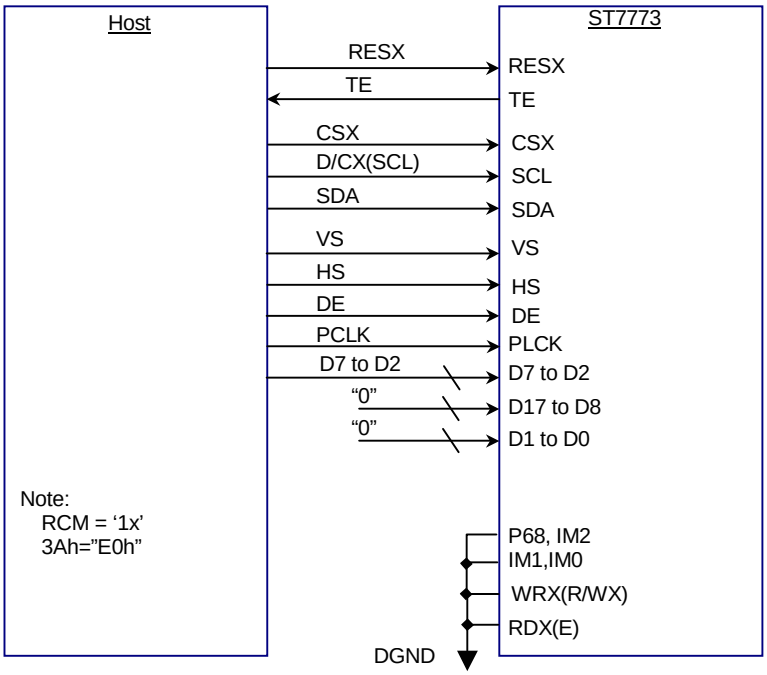


Fig. 13.3.3.1 RGB Interface for 8-bit data width

13.3.4.2 RGBInterface for 16-bit Data Width

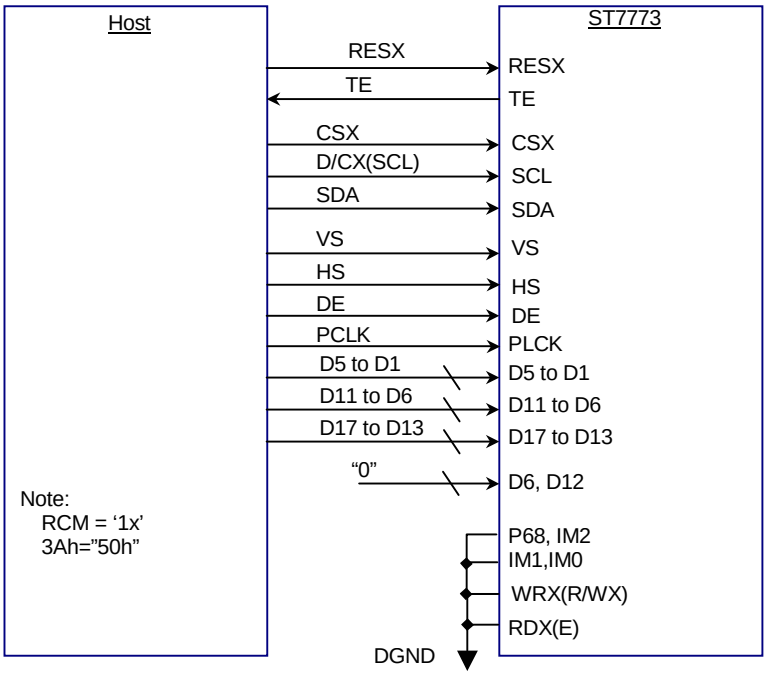


Fig. 13.3.3.2 RGB Interface for 16-bit data width

13.3.4.3 RGBInterface for 18-bit Data Width

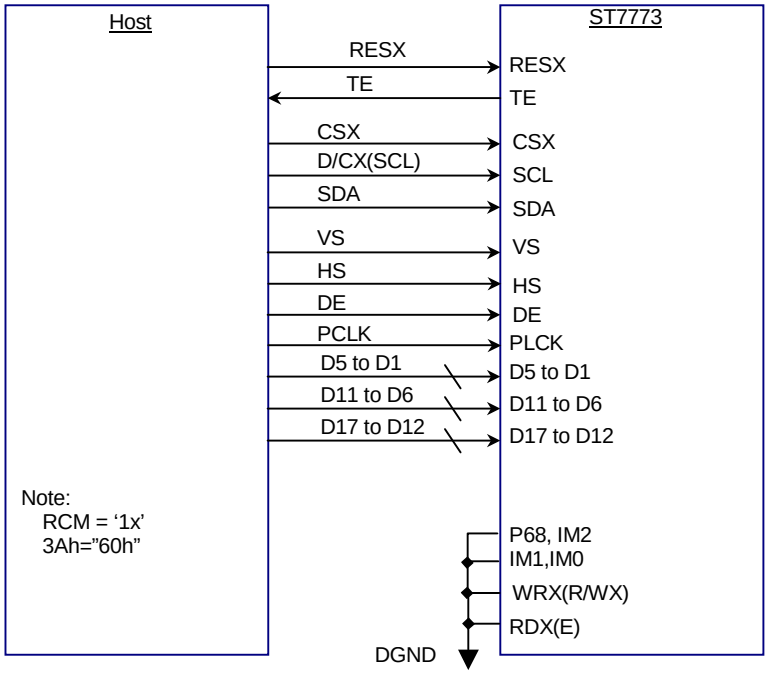
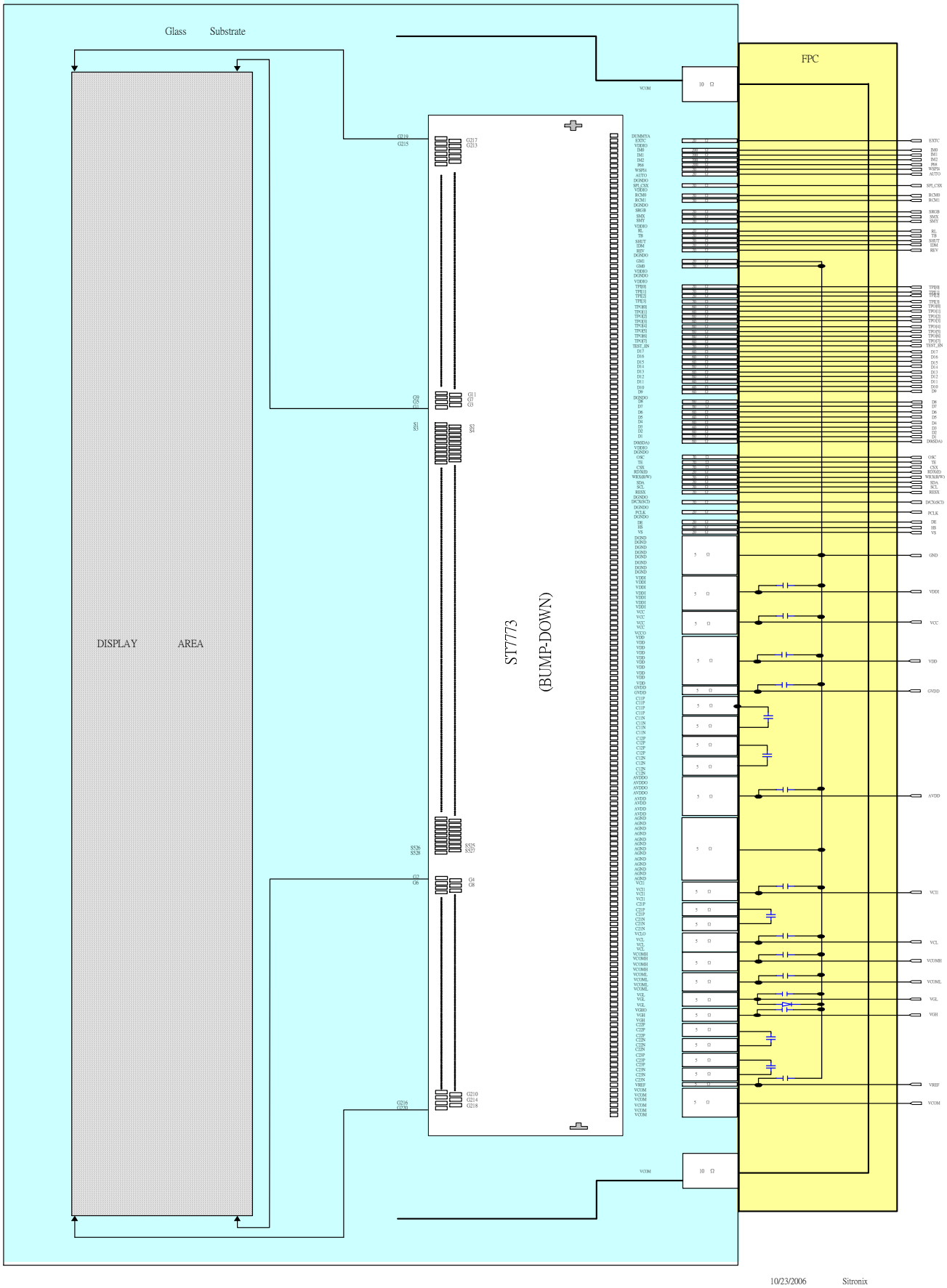


Fig. 13.3.3.3 RGB Interface for 18-bit data width

14. Recommended resistance and connection example



ST7773 Serial Specification Revision History		
Version	**Date**	**Description**
0.1A	2006/11/05	Preliminary 0.1A
0.2A	2007/04/13	Modified the description of some commands.
0.3A	2007/04/10	Modified the description of some commands.
0.4A	2007/07/03	Modify VDD range: 2.7~3.5V Cancel command 0x2D. Modify command 0xC0.(10.2.10,p146) Add command 0xF8,0xFC.(10.2.18,p153,10.2.19,p153) Add gamma structure & gamma voltage formula(13,p162)

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