



# Sitronix

## ST7567

### 65 x 132 Dot Matrix LCD Controller/Driver

## 1. INTRODUCTION

ST7567 is a single-chip dot matrix LCD driver which incorporates LCD controller and common/segment drivers. ST7567 can be connected directly to a microprocessor with 8-bit parallel interface or 4-line serial interface (SPI-4). Display data sent from MPU is stored in the internal Display Data RAM (DDRAM) of 65x132 bits. The display data bits which are stored in DDRAM are directly related to the pixels of LCD panel. ST7567 contains 132 segment-outputs, 64 common-outputs and 1 icon-common-output. With built-in oscillation circuit and low power consumption power circuit, ST7567 generates LCD driving signal without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

## 2. FEATURES

### Single-chip LCD Controller & Driver

#### On-chip Display Data RAM (DDRAM)

- Capacity: 65x132=8580 bits
- Directly display RAM pattern from DDRAM

#### Selectable Display Duty (by SEL2 & SEL1)

- 1/65 duty : 65 common x 132 segment
- 1/55 duty : 55 common x 132 segment
- 1/49 duty : 49 common x 132 segment
- 1/33 duty : 33 common x 132 segment

#### Microprocessor Interface

- Bidirectional 8-bit parallel interface supports: 8080-series and 6800-series MPU
- Serial interface (SPI-4) is also supported (write only)

#### Abundant Functions

- Display ON/OFF, Normal/Reverse Display Mode, Set Display Start Line, Read IC Status, Set all Display Points ON, Set LCD Bias, Electronic Volume Control, Read-modify-Write, Select Segment Driver Direction,

Power Saving Mode, Select Common Driver Direction, Select Voltage Regulator Resistor Ratio (for V0).

#### External Hardware Reset Pin (RSTB)

#### Built-in Oscillation Circuit

- No external component required

#### Low Power Consumption Analog Circuit

- Voltage Booster (4X, 5X & 6X)
- High-accuracy Voltage Regulator for LCD Vop: (Thermal Gradient: -0.11%/°C)
- Voltage Follower for LCD Bias Voltage

#### Wide Operation Voltage Range

- VDD1-VSS1=1.8V~3.3V
- VDD2-VSS2=2.4V~3.3V
- Recommend Vop Range: 4V~9.5V

#### Temperature Range: -30~85°C

#### Package Type: COG

ST7567

6800 , 8080 , 4-Line



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3-1. ST7567 COG OUTLINE

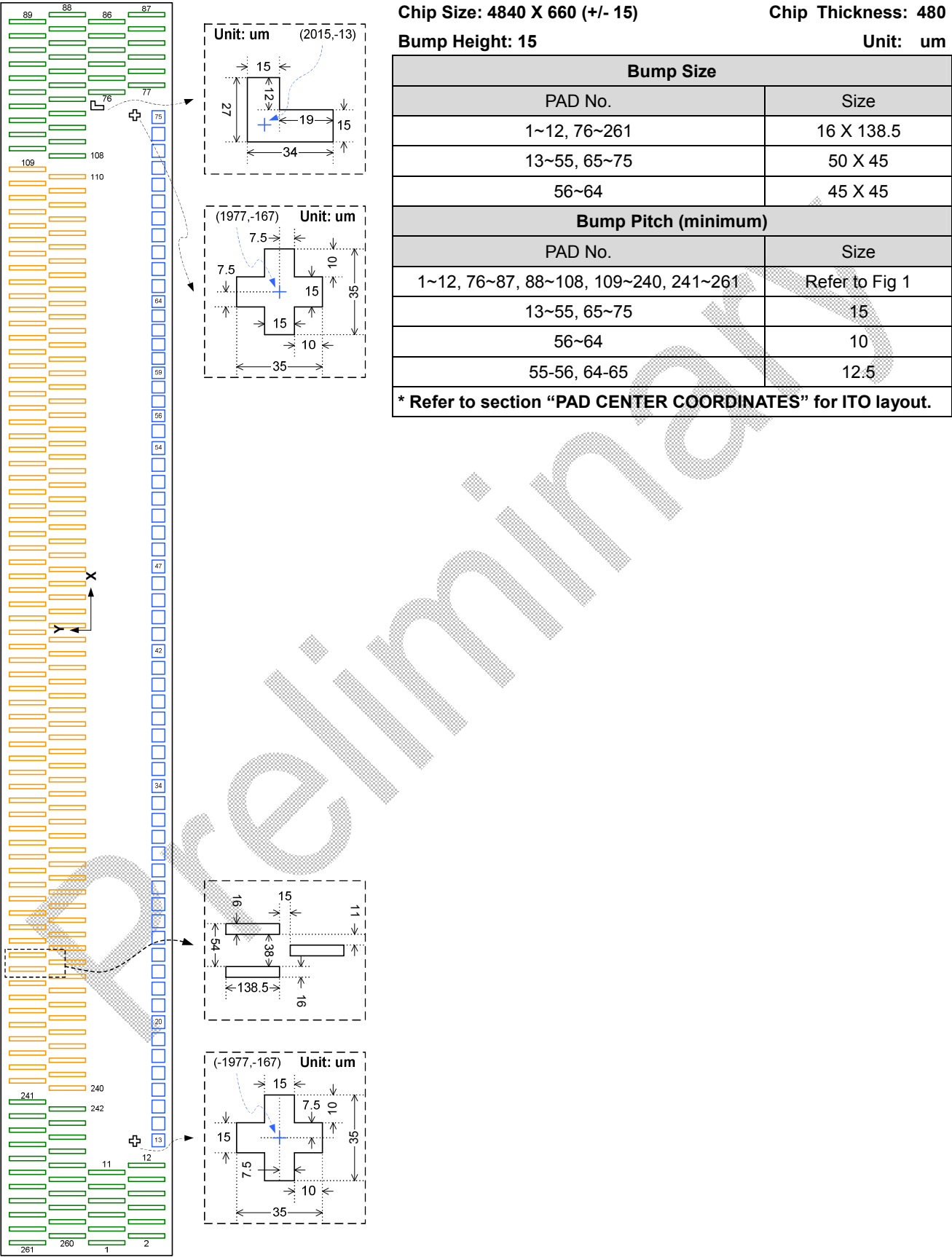


Fig 1. Chip Outline

3-2. PAD CENTER COORDINATES

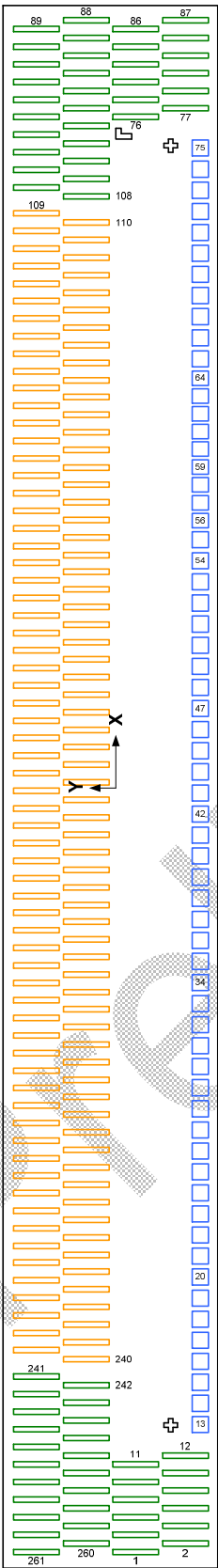


Fig 2. PAD Location

65 Duty

| PAD NO. | PIN Name | X        | Y       |
|---------|----------|----------|---------|
| 1       | COM[53]  | -2363.00 | -74.25  |
| 2       | COM[54]  | -2336.00 | -227.75 |
| 3       | COM[55]  | -2309.00 | -74.25  |
| 4       | COM[56]  | -2282.00 | -227.75 |
| 5       | COM[57]  | -2255.00 | -74.25  |
| 6       | COM[58]  | -2228.00 | -227.75 |
| 7       | COM[59]  | -2201.00 | -74.25  |
| 8       | COM[60]  | -2174.00 | -227.75 |
| 9       | COM[61]  | -2147.00 | -74.25  |
| 10      | COM[62]  | -2120.00 | -227.75 |
| 11      | COM[63]  | -2093.00 | -74.25  |
| 12      | COMS1    | -2066.00 | -227.75 |
| 13      | CL       | -1970.00 | -274.50 |
| 14      | CSB      | -1905.00 | -274.50 |
| 15      | RSTB     | -1840.00 | -274.50 |
| 16      | A0       | -1775.00 | -274.50 |
| 17      | RWR      | -1710.00 | -274.50 |
| 18      | ERD      | -1645.00 | -274.50 |
| 19      | VDDH     | -1580.00 | -274.50 |
| 20      | D0       | -1515.00 | -274.50 |
| 21      | D1       | -1450.00 | -274.50 |
| 22      | D2       | -1385.00 | -274.50 |
| 23      | D3       | -1320.00 | -274.50 |
| 24      | D4       | -1255.00 | -274.50 |
| 25      | D5       | -1190.00 | -274.50 |
| 26      | D6       | -1125.00 | -274.50 |
| 27      | D7       | -1060.00 | -274.50 |
| 28      | VDD1     | -995.00  | -274.50 |
| 29      | VDD1     | -930.00  | -274.50 |
| 30      | VDD2     | -865.00  | -274.50 |
| 31      | VDD2     | -800.00  | -274.50 |
| 32      | VDD2     | -735.00  | -274.50 |
| 33      | VDD3     | -670.00  | -274.50 |
| 34      | VSS1     | -605.00  | -274.50 |
| 35      | VSS1     | -540.00  | -274.50 |
| 36      | VSS3     | -475.00  | -274.50 |
| 37      | VSS2     | -410.00  | -274.50 |
| 38      | VSS2     | -345.00  | -274.50 |
| 39      | VSS2     | -280.00  | -274.50 |
| 40      | V0in     | -215.00  | -274.50 |

| PAD NO. | PIN Name | X       | Y       |
|---------|----------|---------|---------|
| 41      | V0in     | -150.00 | -274.50 |
| 42      | V0s      | -85.00  | -274.50 |
| 43      | V0out    | -20.00  | -274.50 |
| 44      | V0out    | 45.00   | -274.50 |
| 45      | XV0out   | 110.00  | -274.50 |
| 46      | XV0out   | 175.00  | -274.50 |
| 47      | XV0s     | 240.00  | -274.50 |
| 48      | XV0in    | 305.00  | -274.50 |
| 49      | XV0in    | 370.00  | -274.50 |
| 50      | VMO      | 435.00  | -274.50 |
| 51      | VMO      | 500.00  | -274.50 |
| 52      | VGin     | 565.00  | -274.50 |
| 53      | VGin     | 630.00  | -274.50 |
| 54      | VGs      | 695.00  | -274.50 |
| 55      | VGout    | 760.00  | -274.50 |
| 56      | T[6]     | 820.00  | -274.50 |
| 57      | T[7]     | 875.00  | -274.50 |
| 58      | T[8]     | 930.00  | -274.50 |
| 59      | TFCOM    | 985.00  | -274.50 |
| 60      | T[1]     | 1040.00 | -274.50 |
| 61      | T[2]     | 1095.00 | -274.50 |
| 62      | T[3]     | 1150.00 | -274.50 |
| 63      | T[4]     | 1205.00 | -274.50 |
| 64      | T[5]     | 1260.00 | -274.50 |
| 65      | Vref     | 1320.00 | -274.50 |
| 66      | VSSL     | 1385.00 | -274.50 |
| 67      | VDDH     | 1450.00 | -274.50 |
| 68      | C86      | 1515.00 | -274.50 |
| 69      | PSB      | 1580.00 | -274.50 |
| 70      | SEL1     | 1645.00 | -274.50 |
| 71      | VSSL     | 1710.00 | -274.50 |
| 72      | SEL2     | 1775.00 | -274.50 |
| 73      | VDD1     | 1840.00 | -274.50 |
| 74      | VDD2     | 1905.00 | -274.50 |
| 75      | VDD3     | 1970.00 | -274.50 |
| 76      | COM[31]  | 2066.00 | -74.25  |
| 77      | COM[30]  | 2093.00 | -227.75 |
| 78      | COM[29]  | 2120.00 | -74.25  |
| 79      | COM[28]  | 2147.00 | -227.75 |
| 80      | COM[27]  | 2174.00 | -74.25  |

| PAD NO. | PIN Name | X       | Y       |
|---------|----------|---------|---------|
| 81      | COM[26]  | 2201.00 | -227.75 |
| 82      | COM[25]  | 2228.00 | -74.25  |
| 83      | COM[24]  | 2255.00 | -227.75 |
| 84      | COM[23]  | 2282.00 | -74.25  |
| 85      | COM[22]  | 2309.00 | -227.75 |
| 86      | COM[21]  | 2336.00 | -74.25  |
| 87      | COM[20]  | 2363.00 | -227.75 |
| 88      | COM[19]  | 2363.00 | 74.25   |
| 89      | COM[18]  | 2336.00 | 227.75  |
| 90      | COM[17]  | 2309.00 | 74.25   |
| 91      | COM[16]  | 2282.00 | 227.75  |
| 92      | COM[15]  | 2255.00 | 74.25   |
| 93      | COM[14]  | 2228.00 | 227.75  |
| 94      | COM[13]  | 2201.00 | 74.25   |
| 95      | COM[12]  | 2174.00 | 227.75  |
| 96      | COM[11]  | 2147.00 | 74.25   |
| 97      | COM[10]  | 2120.00 | 227.75  |
| 98      | COM[9]   | 2093.00 | 74.25   |
| 99      | COM[8]   | 2066.00 | 227.75  |
| 100     | COM[7]   | 2039.00 | 74.25   |
| 101     | COM[6]   | 2012.00 | 227.75  |
| 102     | COM[5]   | 1985.00 | 74.25   |
| 103     | COM[4]   | 1958.00 | 227.75  |
| 104     | COM[3]   | 1931.00 | 74.25   |
| 105     | COM[2]   | 1904.00 | 227.75  |
| 106     | COM[1]   | 1877.00 | 74.25   |
| 107     | COM[0]   | 1850.00 | 227.75  |
| 108     | COMS2    | 1823.00 | 74.25   |
| 109     | SEG[0]   | 1768.50 | 227.75  |
| 110     | SEG[1]   | 1741.50 | 74.25   |
| 111     | SEG[2]   | 1714.50 | 227.75  |
| 112     | SEG[3]   | 1687.50 | 74.25   |
| 113     | SEG[4]   | 1660.50 | 227.75  |
| 114     | SEG[5]   | 1633.50 | 74.25   |
| 115     | SEG[6]   | 1606.50 | 227.75  |
| 116     | SEG[7]   | 1579.50 | 74.25   |
| 117     | SEG[8]   | 1552.50 | 227.75  |
| 118     | SEG[9]   | 1525.50 | 74.25   |
| 119     | SEG[10]  | 1498.50 | 227.75  |
| 120     | SEG[11]  | 1471.50 | 74.25   |

| PAD NO. | PIN Name | X       | Y      |
|---------|----------|---------|--------|
| 121     | SEG[12]  | 1444.50 | 227.75 |
| 122     | SEG[13]  | 1417.50 | 74.25  |
| 123     | SEG[14]  | 1390.50 | 227.75 |
| 124     | SEG[15]  | 1363.50 | 74.25  |
| 125     | SEG[16]  | 1336.50 | 227.75 |
| 126     | SEG[17]  | 1309.50 | 74.25  |
| 127     | SEG[18]  | 1282.50 | 227.75 |
| 128     | SEG[19]  | 1255.50 | 74.25  |
| 129     | SEG[20]  | 1228.50 | 227.75 |
| 130     | SEG[21]  | 1201.50 | 74.25  |
| 131     | SEG[22]  | 1174.50 | 227.75 |
| 132     | SEG[23]  | 1147.50 | 74.25  |
| 133     | SEG[24]  | 1120.50 | 227.75 |
| 134     | SEG[25]  | 1093.50 | 74.25  |
| 135     | SEG[26]  | 1066.50 | 227.75 |
| 136     | SEG[27]  | 1039.50 | 74.25  |
| 137     | SEG[28]  | 1012.50 | 227.75 |
| 138     | SEG[29]  | 985.50  | 74.25  |
| 139     | SEG[30]  | 958.50  | 227.75 |
| 140     | SEG[31]  | 931.50  | 74.25  |
| 141     | SEG[32]  | 904.50  | 227.75 |
| 142     | SEG[33]  | 877.50  | 74.25  |
| 143     | SEG[34]  | 850.50  | 227.75 |
| 144     | SEG[35]  | 823.50  | 74.25  |
| 145     | SEG[36]  | 796.50  | 227.75 |
| 146     | SEG[37]  | 769.50  | 74.25  |
| 147     | SEG[38]  | 742.50  | 227.75 |
| 148     | SEG[39]  | 715.50  | 74.25  |
| 149     | SEG[40]  | 688.50  | 227.75 |
| 150     | SEG[41]  | 661.50  | 74.25  |
| 151     | SEG[42]  | 634.50  | 227.75 |
| 152     | SEG[43]  | 607.50  | 74.25  |
| 153     | SEG[44]  | 580.50  | 227.75 |
| 154     | SEG[45]  | 553.50  | 74.25  |
| 155     | SEG[46]  | 526.50  | 227.75 |
| 156     | SEG[47]  | 499.50  | 74.25  |
| 157     | SEG[48]  | 472.50  | 227.75 |
| 158     | SEG[49]  | 445.50  | 74.25  |
| 159     | SEG[50]  | 418.50  | 227.75 |
| 160     | SEG[51]  | 391.50  | 74.25  |

| PAD NO. | PIN Name | X       | Y      |
|---------|----------|---------|--------|
| 161     | SEG[52]  | 364.50  | 227.75 |
| 162     | SEG[53]  | 337.50  | 74.25  |
| 163     | SEG[54]  | 310.50  | 227.75 |
| 164     | SEG[55]  | 283.50  | 74.25  |
| 165     | SEG[56]  | 256.50  | 227.75 |
| 166     | SEG[57]  | 229.50  | 74.25  |
| 167     | SEG[58]  | 202.50  | 227.75 |
| 168     | SEG[59]  | 175.50  | 74.25  |
| 169     | SEG[60]  | 148.50  | 227.75 |
| 170     | SEG[61]  | 121.50  | 74.25  |
| 171     | SEG[62]  | 94.50   | 227.75 |
| 172     | SEG[63]  | 67.50   | 74.25  |
| 173     | SEG[64]  | 40.50   | 227.75 |
| 174     | SEG[65]  | 13.50   | 74.25  |
| 175     | SEG[66]  | -13.50  | 227.75 |
| 176     | SEG[67]  | -40.50  | 74.25  |
| 177     | SEG[68]  | -67.50  | 227.75 |
| 178     | SEG[69]  | -94.50  | 74.25  |
| 179     | SEG[70]  | -121.50 | 227.75 |
| 180     | SEG[71]  | -148.50 | 74.25  |
| 181     | SEG[72]  | -175.50 | 227.75 |
| 182     | SEG[73]  | -202.50 | 74.25  |
| 183     | SEG[74]  | -229.50 | 227.75 |
| 184     | SEG[75]  | -256.50 | 74.25  |
| 185     | SEG[76]  | -283.50 | 227.75 |
| 186     | SEG[77]  | -310.50 | 74.25  |
| 187     | SEG[78]  | -337.50 | 227.75 |
| 188     | SEG[79]  | -364.50 | 74.25  |
| 189     | SEG[80]  | -391.50 | 227.75 |
| 190     | SEG[81]  | -418.50 | 74.25  |
| 191     | SEG[82]  | -445.50 | 227.75 |
| 192     | SEG[83]  | -472.50 | 74.25  |
| 193     | SEG[84]  | -499.50 | 227.75 |
| 194     | SEG[85]  | -526.50 | 74.25  |
| 195     | SEG[86]  | -553.50 | 227.75 |
| 196     | SEG[87]  | -580.50 | 74.25  |
| 197     | SEG[88]  | -607.50 | 227.75 |
| 198     | SEG[89]  | -634.50 | 74.25  |
| 199     | SEG[90]  | -661.50 | 227.75 |
| 200     | SEG[91]  | -688.50 | 74.25  |

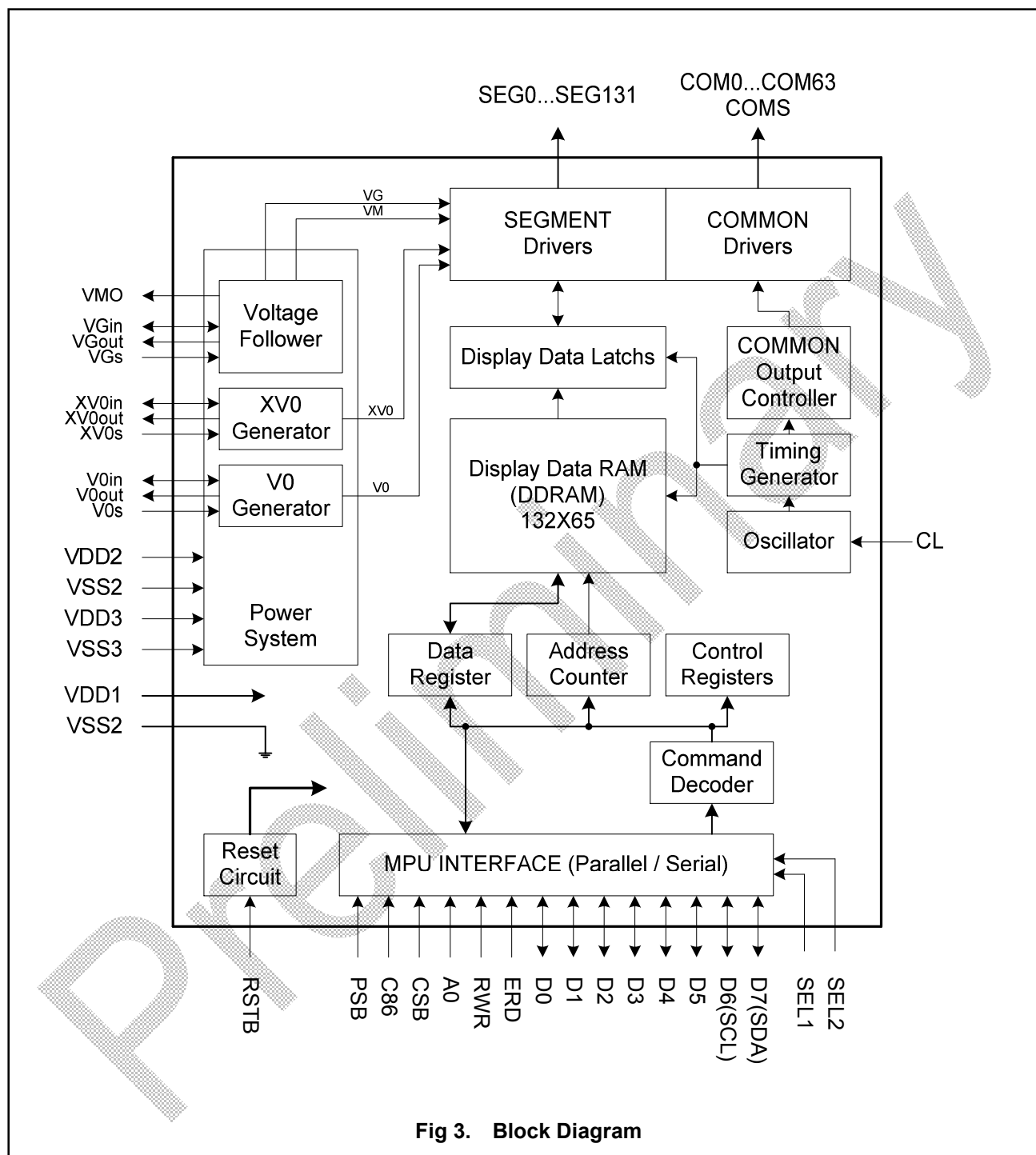
| PAD NO. | PIN Name | X        | Y      |
|---------|----------|----------|--------|
| 201     | SEG[92]  | -715.50  | 227.75 |
| 202     | SEG[93]  | -742.50  | 74.25  |
| 203     | SEG[94]  | -769.50  | 227.75 |
| 204     | SEG[95]  | -796.50  | 74.25  |
| 205     | SEG[96]  | -823.50  | 227.75 |
| 206     | SEG[97]  | -850.50  | 74.25  |
| 207     | SEG[98]  | -877.50  | 227.75 |
| 208     | SEG[99]  | -904.50  | 74.25  |
| 209     | SEG[100] | -931.50  | 227.75 |
| 210     | SEG[101] | -958.50  | 74.25  |
| 211     | SEG[102] | -985.50  | 227.75 |
| 212     | SEG[103] | -1012.50 | 74.25  |
| 213     | SEG[104] | -1039.50 | 227.75 |
| 214     | SEG[105] | -1066.50 | 74.25  |
| 215     | SEG[106] | -1093.50 | 227.75 |
| 216     | SEG[107] | -1120.50 | 74.25  |
| 217     | SEG[108] | -1147.50 | 227.75 |
| 218     | SEG[109] | -1174.50 | 74.25  |
| 219     | SEG[110] | -1201.50 | 227.75 |
| 220     | SEG[111] | -1228.50 | 74.25  |
| 221     | SEG[112] | -1255.50 | 227.75 |
| 222     | SEG[113] | -1282.50 | 74.25  |
| 223     | SEG[114] | -1309.50 | 227.75 |
| 224     | SEG[115] | -1336.50 | 74.25  |
| 225     | SEG[116] | -1363.50 | 227.75 |
| 226     | SEG[117] | -1390.50 | 74.25  |
| 227     | SEG[118] | -1417.50 | 227.75 |
| 228     | SEG[119] | -1444.50 | 74.25  |
| 229     | SEG[120] | -1471.50 | 227.75 |
| 230     | SEG[121] | -1498.50 | 74.25  |
| 231     | SEG[122] | -1525.50 | 227.75 |
| 232     | SEG[123] | -1552.50 | 74.25  |
| 233     | SEG[124] | -1579.50 | 227.75 |
| 234     | SEG[125] | -1606.50 | 74.25  |
| 235     | SEG[126] | -1633.50 | 227.75 |
| 236     | SEG[127] | -1660.50 | 74.25  |
| 237     | SEG[128] | -1687.50 | 227.75 |
| 238     | SEG[129] | -1714.50 | 74.25  |
| 239     | SEG[130] | -1741.50 | 227.75 |
| 240     | SEG[131] | -1768.50 | 74.25  |

| PAD NO. | PIN Name | X        | Y      |
|---------|----------|----------|--------|
| 241     | COM[32]  | -1823.00 | 227.75 |
| 242     | COM[33]  | -1850.00 | 74.25  |
| 243     | COM[34]  | -1877.00 | 227.75 |
| 244     | COM[35]  | -1904.00 | 74.25  |
| 245     | COM[36]  | -1931.00 | 227.75 |
| 246     | COM[37]  | -1958.00 | 74.25  |
| 247     | COM[38]  | -1985.00 | 227.75 |
| 248     | COM[39]  | -2012.00 | 74.25  |
| 249     | COM[40]  | -2039.00 | 227.75 |
| 250     | COM[41]  | -2066.00 | 74.25  |
| 251     | COM[42]  | -2093.00 | 227.75 |
| 252     | COM[43]  | -2120.00 | 74.25  |
| 253     | COM[44]  | -2147.00 | 227.75 |
| 254     | COM[45]  | -2174.00 | 74.25  |
| 255     | COM[46]  | -2201.00 | 227.75 |
| 256     | COM[47]  | -2228.00 | 74.25  |
| 257     | COM[48]  | -2255.00 | 227.75 |
| 258     | COM[49]  | -2282.00 | 74.25  |
| 259     | COM[50]  | -2309.00 | 227.75 |
| 260     | COM[51]  | -2336.00 | 74.25  |
| 261     | COM[52]  | -2363.00 | 227.75 |

Note:

1. Unit:  $\mu\text{m}$
2. This is the default PAD Center Coordinate Table with 1/65 Duty. Other duty output mapping can be found in Section 6. FUNCTION DESCRIPTION and Fig 9.
3. Tolerance:  $\pm 0.05 \mu\text{m}$ .

## 4. BLOCK DIAGRAM



## 5. PIN DESCRIPTION

### LCD Driver Output Pins

| Pin Name                | Type  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | No. of Pins     |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
|-------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------|-------------------------------|--|----------------|-----------------|---|---|-----|-----|---|---|-----|----|---|---|-----|----|---|---|----|-----|-------------------------|--|-----|-----|-----|
| SEG0 to SEG131          | O     | <p>LCD segment driver outputs.</p> <p>The display data and the frame control the output voltage.</p> <table border="1"> <thead> <tr> <th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment Driver Output Voltage</th></tr> <tr> <th>Normal Display</th><th>Inverse Display</th></tr> </thead> <tbody> <tr> <td>H</td><td>+</td><td>VG</td><td>VSS</td></tr> <tr> <td>H</td><td>-</td><td>VSS</td><td>VG</td></tr> <tr> <td>L</td><td>+</td><td>VSS</td><td>VG</td></tr> <tr> <td>L</td><td>-</td><td>VG</td><td>VSS</td></tr> <tr> <td colspan="2">Display OFF, Power Save</td><td>VSS</td><td>VSS</td></tr> </tbody> </table>           | Display data    | Frame | Segment Driver Output Voltage |  | Normal Display | Inverse Display | H | + | VG  | VSS | H | - | VSS | VG | L | + | VSS | VG | L | - | VG | VSS | Display OFF, Power Save |  | VSS | VSS | 132 |
| Display data            | Frame | Segment Driver Output Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
|                         |       | Normal Display                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Inverse Display |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| H                       | +     | VG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | VSS             |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| H                       | -     | VSS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | VG              |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| L                       | +     | VSS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | VG              |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| L                       | -     | VG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | VSS             |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| Display OFF, Power Save |       | VSS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | VSS             |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| COM0 to COM63           | O     | <p>LCD common driver outputs.</p> <p>The internal scanning signal and the frame control the output voltage.</p> <table border="1"> <thead> <tr> <th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common Driver Output Voltage</th></tr> <tr> <th>Normal Display</th><th>Inverse Display</th></tr> </thead> <tbody> <tr> <td>H</td><td>+</td><td colspan="2">XV0</td></tr> <tr> <td>H</td><td>-</td><td colspan="2">V0</td></tr> <tr> <td>L</td><td>+</td><td colspan="2">VM</td></tr> <tr> <td>L</td><td>-</td><td colspan="2">VM</td></tr> <tr> <td colspan="2">Display OFF, Power Save</td><td colspan="2">VSS</td></tr> </tbody> </table> | Scan signal     | Frame | Common Driver Output Voltage  |  | Normal Display | Inverse Display | H | + | XV0 |     | H | - | V0  |    | L | + | VM  |    | L | - | VM |     | Display OFF, Power Save |  | VSS |     | 64  |
| Scan signal             | Frame | Common Driver Output Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
|                         |       | Normal Display                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Inverse Display |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| H                       | +     | XV0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| H                       | -     | V0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| L                       | +     | VM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| L                       | -     | VM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| Display OFF, Power Save |       | VSS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| COMS1, COMS2<br>(COMS)  | O     | <p>LCD common driver outputs for icons.</p> <p>The output signals of these two pins are the same.</p> <p>When icon feature is not used, these pins should be left open.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 2               |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |

### Microprocessor Interface Pins

| Pin Name | Type        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | No. of Pins                                                                                    |          |     |             |   |             |     |                                                                    |   |             |     |                                                                                                |   |
|----------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|----------|-----|-------------|---|-------------|-----|--------------------------------------------------------------------|---|-------------|-----|------------------------------------------------------------------------------------------------|---|
| RSTB     | I           | Hardware reset input pin. When RSTB is "L", internal initialization is executed and the internal registers will be initialized.                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1                                                                                              |          |     |             |   |             |     |                                                                    |   |             |     |                                                                                                |   |
| CSB      | I           | Chip select input pin. Interface access is enabled when CSB is "L".<br>When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.                                                                                                                                                                                                                                                                                                                                                                                                                                         | 1                                                                                              |          |     |             |   |             |     |                                                                    |   |             |     |                                                                                                |   |
| A0       | I           | It determines whether the access is related to data or command.<br>A0="H" : Indicates that signals on D[7:0] are display data.<br>A0="L" : Indicates that signals on D[7:0] are command.                                                                                                                                                                                                                                                                                                                                                                                         | 1                                                                                              |          |     |             |   |             |     |                                                                    |   |             |     |                                                                                                |   |
| RWR      | I           | <p>Read/Write execution control pin. When PSB is "H",</p> <table border="1"> <thead> <tr> <th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr> </thead> <tbody> <tr> <td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.<br/>R/W="H": read.<br/>R/W="L": write.</td></tr> <tr> <td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.<br/>Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr> </tbody> </table> <p>RWR is not used in serial interface and should fix to "H" by VDD1 or VDDH.</p> | C86                                                                                            | MPU Type | RWR | Description | H | 6800 series | R/W | Read/Write control input pin.<br>R/W="H": read.<br>R/W="L": write. | L | 8080 series | /WR | Write enable input pin.<br>Signals on D[7:0] will be latched at the rising edge of /WR signal. | 1 |
| C86      | MPU Type    | RWR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Description                                                                                    |          |     |             |   |             |     |                                                                    |   |             |     |                                                                                                |   |
| H        | 6800 series | R/W                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Read/Write control input pin.<br>R/W="H": read.<br>R/W="L": write.                             |          |     |             |   |             |     |                                                                    |   |             |     |                                                                                                |   |
| L        | 8080 series | /WR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Write enable input pin.<br>Signals on D[7:0] will be latched at the rising edge of /WR signal. |          |     |             |   |             |     |                                                                    |   |             |     |                                                                                                |   |



| Pin Name | Type                                                                       | Description                                                                                                                                                                                                                                      |             |     |                                                                                                                                                                | No. of Pins |
|----------|----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| ERD      | I                                                                          | Read/Write execution control pin. When PSB is “H”,                                                                                                                                                                                               |             |     |                                                                                                                                                                | 1           |
|          |                                                                            | C86                                                                                                                                                                                                                                              | MPU Type    | ERD | Description                                                                                                                                                    |             |
|          |                                                                            | H                                                                                                                                                                                                                                                | 6800 series | E   | Read/Write control input pin.<br>R/W=“H”: When E is “H”, D[7:0] are in output mode.<br>R/W=“L”: Signals on D[7:0] are latched at the falling edge of E signal. |             |
|          |                                                                            | L                                                                                                                                                                                                                                                | 8080 series | /RD | Read enable input pin.<br>When /RD is “L”, D[7:0] are in output mode.                                                                                          |             |
|          | ERD is not used in serial interface and should fix to “H” by VDD1 or VDDH. |                                                                                                                                                                                                                                                  |             |     |                                                                                                                                                                |             |
| D[7:0]   | I/O                                                                        | <b>When using 8-bit parallel interface: (6800 or 8080 mode)</b><br>8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.<br>When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.                          |             |     |                                                                                                                                                                | 8           |
|          | I                                                                          | <b>When using serial interface: 4-LINE</b><br>D7=SDA : Serial data input.<br>D6=SCL : Serial clock input.<br>D[5:0] are not used and should connect to “H” by VDD1 or VDDH.<br>When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance. |             |     |                                                                                                                                                                |             |

## Note:

- After VDD1 is turned ON, any MPU interface pins cannot be left floating.

## Configuration Pins

| Pin Name                                                                                                                          | Type | Description                                                                                                                                                                                                                                                                                                                                      | No. of Pins |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|-----------------------------------------------------------------------------------------------------------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|------------------------------------|--------------------|------|-----|------------------------------------|------|------------|------------------------------------|-----|------|-----------------------------|-----|-----|------|------------|-----|-----|------|------------|
| VDDH                                                                                                                              | I    | Logic “1” level for option pins which should connect to “H”.                                                                                                                                                                                                                                                                                     | 2           |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
| VSSL                                                                                                                              | I    | Logical “0” level for option pins which should connect to “L”.                                                                                                                                                                                                                                                                                   | 2           |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
| PSB                                                                                                                               | I    | PSB selects the interface type: Serial or Parallel.                                                                                                                                                                                                                                                                                              | 1           |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
| C86                                                                                                                               | I    | C86 selects the microprocessor type in parallel interface mode.                                                                                                                                                                                                                                                                                  | 1           |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      | <table><tr><th>PSB</th><th>C86</th><th>Selected Interface</th></tr><tr><td>“H”</td><td>“H”</td><td>Parallel 6800 Series MPU Interface</td></tr><tr><td>“H”</td><td>“L”</td><td>Parallel 8080 Series MPU Interface</td></tr><tr><td>“L”</td><td>“X”</td><td>Serial 4-Line SPI Interface</td></tr></table>                                         |             | PSB  | C86                                | Selected Interface | “H”  | “H” | Parallel 6800 Series MPU Interface | “H”  | “L”        | Parallel 8080 Series MPU Interface | “L” | “X”  | Serial 4-Line SPI Interface |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      | PSB                                                                                                                                                                                                                                                                                                                                              |             | C86  | Selected Interface                 |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      | “H”                                                                                                                                                                                                                                                                                                                                              |             | “H”  | Parallel 6800 Series MPU Interface |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      | “H”                                                                                                                                                                                                                                                                                                                                              |             | “L”  | Parallel 8080 Series MPU Interface |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
| “L”                                                                                                                               | “X”  | Serial 4-Line SPI Interface                                                                                                                                                                                                                                                                                                                      |             |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
| Please refer to “APPLICATION NOTES” and “Microprocessor Interface” (Section 6) for detailed connection of the selected interface. |      |                                                                                                                                                                                                                                                                                                                                                  |             |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      |                                                                                                                                                                                                                                                                                                                                                  |             |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      |                                                                                                                                                                                                                                                                                                                                                  |             |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
| SEL[2:1]                                                                                                                          | I    | These pins select the display duty and bias of ST7567.                                                                                                                                                                                                                                                                                           | 2           |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      | <table><tr><th>SEL2</th><th>SEL1</th><th>Duty</th><th>Bias</th></tr><tr><td>“L”</td><td>“L”</td><td>1/65</td><td>1/9 or 1/7</td></tr><tr><td>“L”</td><td>“H”</td><td>1/49</td><td>1/8 or 1/6</td></tr><tr><td>“H”</td><td>“L”</td><td>1/33</td><td>1/6 or 1/5</td></tr><tr><td>“H”</td><td>“H”</td><td>1/55</td><td>1/8 or 1/6</td></tr></table> |             | SEL2 | SEL1                               | Duty               | Bias | “L” | “L”                                | 1/65 | 1/9 or 1/7 | “L”                                | “H” | 1/49 | 1/8 or 1/6                  | “H” | “L” | 1/33 | 1/6 or 1/5 | “H” | “H” | 1/55 | 1/8 or 1/6 |
|                                                                                                                                   |      | SEL2                                                                                                                                                                                                                                                                                                                                             |             | SEL1 | Duty                               | Bias               |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      | “L”                                                                                                                                                                                                                                                                                                                                              |             | “L”  | 1/65                               | 1/9 or 1/7         |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      | “L”                                                                                                                                                                                                                                                                                                                                              |             | “H”  | 1/49                               | 1/8 or 1/6         |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      | “H”                                                                                                                                                                                                                                                                                                                                              |             | “L”  | 1/33                               | 1/6 or 1/5         |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
| “H”                                                                                                                               | “H”  | 1/55                                                                                                                                                                                                                                                                                                                                             | 1/8 or 1/6  |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      |                                                                                                                                                                                                                                                                                                                                                  |             |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      |                                                                                                                                                                                                                                                                                                                                                  |             |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      |                                                                                                                                                                                                                                                                                                                                                  |             |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |
|                                                                                                                                   |      |                                                                                                                                                                                                                                                                                                                                                  |             |      |                                    |                    |      |     |                                    |      |            |                                    |     |      |                             |     |     |      |            |     |     |      |            |

## Power System Pins

| Pin Name                | Type  | Description                                                                                                                                                                                                                                                                                                                                                                                 | No. of Pins |
|-------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| VDD1                    | Power | Digital power. If VDD1=VDD2, connect to VDD2 externally.                                                                                                                                                                                                                                                                                                                                    | 3           |
| VDD2                    | Power | Analog power. If VDD1=VDD2, connect to VDD1 externally.                                                                                                                                                                                                                                                                                                                                     | 4           |
| VDD3                    | Power | Power for reference voltage circuit.                                                                                                                                                                                                                                                                                                                                                        | 2           |
| VSS1                    | Power | Digital ground. Connect to VSS2 externally.                                                                                                                                                                                                                                                                                                                                                 | 2           |
| VSS2                    | Power | Analog ground. Connect to VSS1 externally.                                                                                                                                                                                                                                                                                                                                                  | 3           |
| VSS3                    | Power | Ground for reference voltage circuit.                                                                                                                                                                                                                                                                                                                                                       | 1           |
| V0out<br>V0in<br>V0s    | Power | V0 is the LCD driving voltage for common circuits at negative frame.<br>V0out is the output of V0 regulator. V0s is the feedback of V0 regulator.<br>V0in is the V0 input of common circuits.<br>Be sure that: $V0 \geq VG > VM > VSS \geq XV0$ (under operation).<br>V0out, V0in & V0s should be separated in ITO layout.<br>V0out, V0in & V0s should be connected together in FPC layout. | 2<br>2<br>1 |
| XV0out<br>XV0in<br>XV0s | Power | XV0 is the LCD driving voltage for common circuits at positive frame.<br>XV0out is the output of XV0 regulator. XV0s is the feedback of XV0 regulator.<br>XV0in is the V0 input of common circuits.<br>XV0out, XV0in & XV0s should be separated in ITO layout.<br>XV0out, XV0in & XV0s should be connected together in FPC layout.                                                          | 2<br>2<br>1 |
| VGout<br>VGin<br>VGs    | Power | VG is the LCD driving voltage for segment circuits.<br>VGout is the output of VG regulator. VGs is the feedback of VG regulator.<br>VGin is the VG input of segment circuits.<br>VGout, VGin & VGs should be separated in ITO layout.<br>VGout, VGin & VGs should be connected together in FPC layout.<br>$1.24 \leq VG < VDD2$ .                                                           | 1<br>2<br>1 |
| VMO                     | Power | VM is the LCD driving voltage for common circuits.<br>$0.62V \leq VM < VDD2$ .                                                                                                                                                                                                                                                                                                              | 2           |

## Test Pins

| Pin Name | Type | Description                                                                                 | No. of Pins |
|----------|------|---------------------------------------------------------------------------------------------|-------------|
| Vref     | T    | Test pin for power system.<br>This pin must be left open (without any kinds of connection). | 1           |
| T1~T8    | T    | Do NOT use. Reserved for testing.<br>Must be floating.                                      | 8           |
| TFCOM    | T    | Do NOT use. Reserved for testing.<br>Must be floating.                                      | 1           |
| CL       | T    | Do NOT use. Reserved for testing.<br>Must be floating.                                      | 1           |

## Recommend ITO Resistance

| Pin Name                                                             | ITO Resistance |
|----------------------------------------------------------------------|----------------|
| VMO, Vref, T[1:8], TFCOM, CL                                         | Floating       |
| VDD1, VDD2, VDD3, VSS1, VSS2, VSS3                                   | < 100Ω         |
| V0(V0in, V0out, V0s), VG(VGin, VGout, VGs), XV0(XV0in, XV0out, XV0s) | < 300Ω         |
| A0, RWR, ERD, CSB, D[7:0]                                            | < 1KΩ          |
| PSB, C86, SEL[2:1]                                                   | < 5KΩ          |
| RSTB <sup>*1</sup>                                                   | < 10KΩ         |

Note:

1. To prevent the ESD pulse resetting the internal register, applications should increase the resistance of RSTB signal (add a series resistor or increase ITO resistance). The value is different from modules.
2. The option setting to be "H" should connect to VDD1 or VDDH.
3. The option setting to be "L" should connect to VSS1 or VSSL.

## 6. FUNCTION DESCRIPTION

### Microprocessor Interface

#### Chip Select Input

CSB pin is used for chip selection. When CSB is "L", the microprocessor interface is enabled and ST7567 can interface with an MPU. When CSB is "H", the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 4-Line serial interface, the internal shift register and serial counter are reset when CSB is "H".

#### Interface Selection

The interface selection is controlled by C86 and PSB pins. The selection for parallel or serial interface is shown in Table 1.

**Table 1. Parallel/Serial Interface Mode**

| PSB | C86 | CSB | A0 | ERD | RWR | D[7:0]                     | MPU Interface                  |
|-----|-----|-----|----|-----|-----|----------------------------|--------------------------------|
| "H" | "H" | CSB | A0 | E   | R/W | D[7:0]                     | 6800-series parallel interface |
| "H" | "L" |     |    | /RD | /WR |                            | 8080-series parallel interface |
| "L" | "X" |     |    | --- | --- | Refer to serial interface. | 4-Line SPI interface           |

\* The un-used pins are marked as "---" and should be fixed to "H" by VDD1 or VDDH.

#### Parallel Interface

When PSB="H", the 8-bit bi-directional parallel interface is enabled and the type of MPU is selected by "C86" pin as shown in Table 2. The data transfer type is determined by signals on A0, ERD and RWR as shown in Table 3.

**Table 2. Microprocessor Selection for Parallel Interface**

| PSB | C86 | CSB | A0 | ERD | RWR | D[7:0] | MPU Interface                  |
|-----|-----|-----|----|-----|-----|--------|--------------------------------|
| "H" | "H" | CSB | A0 | E   | R/W | D[7:0] | 6800-series parallel interface |
| "H" | "L" |     |    | /RD | /WR |        | 8080-series parallel interface |

**Table 3. Parallel Data Transfer Type**

| Common Pins |     | 6800-Series |           | 8080-Series |           | Description                               |
|-------------|-----|-------------|-----------|-------------|-----------|-------------------------------------------|
| CSB         | A0  | E (ERD)     | R/W (RWR) | /RD (ERD)   | /WR (RWR) |                                           |
| "L"         | "H" | "H"         | "H"       | "L"         | "H"       | Display data read out                     |
|             | "H" | "H"         | "L"       | "H"         | "L"       | Display data write                        |
|             | "L" | "H"         | "H"       | "L"         | "H"       | Internal status read                      |
|             | "L" | "H"         | "L"       | "H"         | "L"       | Writes to internal register (instruction) |

#### Setting Serial Interface

| Serial Mode          | PSB | C86 | CSB | A0 | ERD | RWR | D[7:0]                                  |
|----------------------|-----|-----|-----|----|-----|-----|-----------------------------------------|
| 4-Line SPI interface | "L" | X   | CSB | A0 | --- | --- | SDA, SCLK, ---, ---, ---, ---, ---, --- |

\* The un-used pins are marked as "---" and should be fixed to "H" by VDD1 or VDDH.

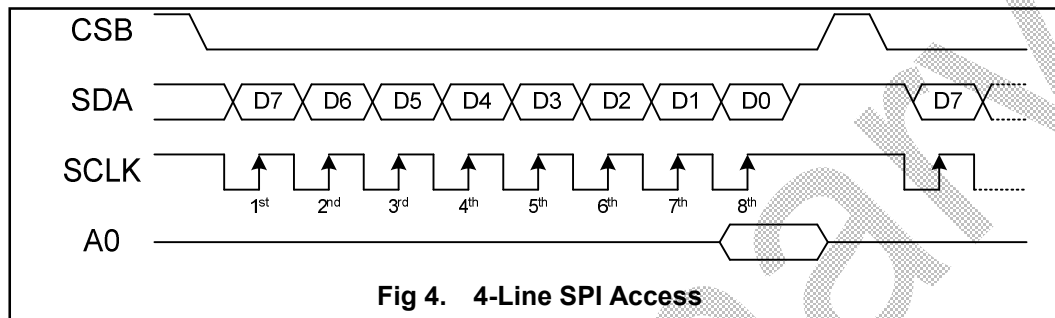
\* C86 is marked as "X" and can be fixed to "H" or "L".

Note:

1. The option setting to be "H" should connect to VDD1 or VDDH.
2. The option setting to be "L" should connect to VSS1 or VSSL.

**4-line SPI interface (PSB="L", CSB="H" or "L")**

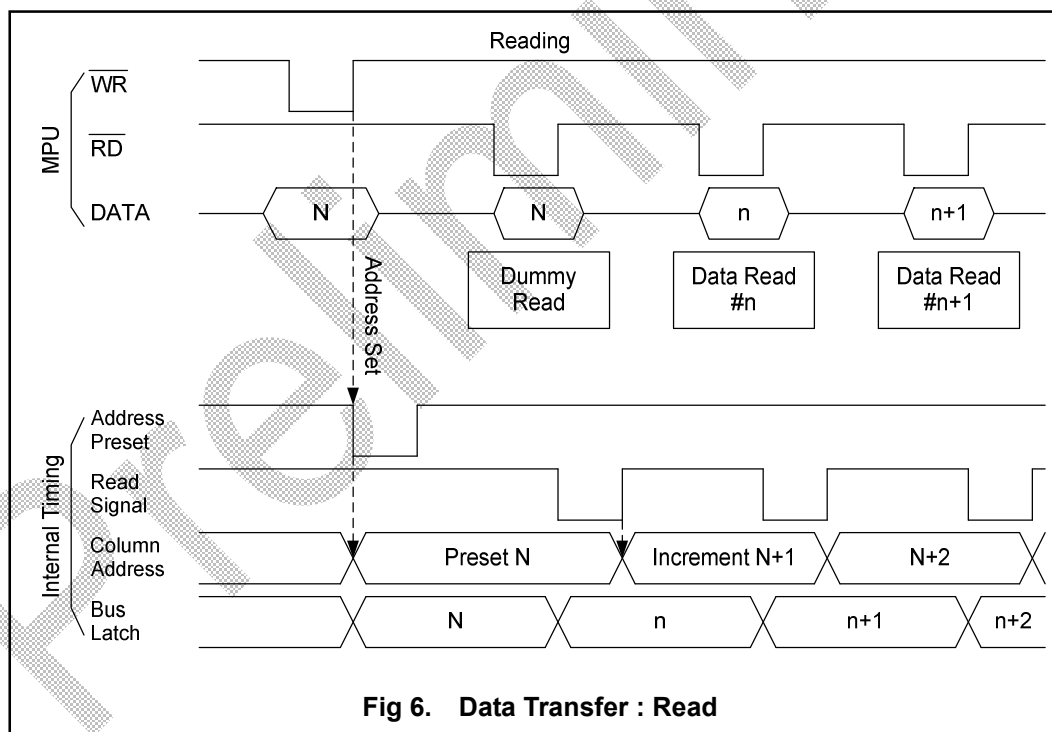
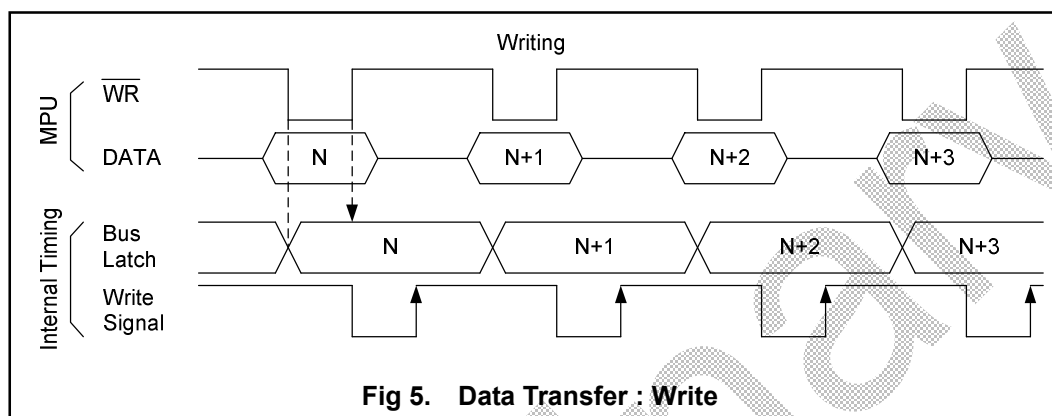
When ST7567 is active (CSB="L"), serial data (SDA) and serial clock (SCLK) inputs are enabled. When ST7567 is not active (CSB="H"), the internal 8-bit shift register and 3-bit counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCLK. After the 8<sup>th</sup> serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8<sup>th</sup> clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is "H" and will be instruction when A0 is "L". The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCLK signal quality is very important and external noise may cause unexpected data/instruction latch.

**Note:**

- Some MPU will set the interface to be Hi-Z (high impedance) mode when power saving mode or after hardware reset. This is not allowed when the VDD1 of ST7567 is turned ON. Because the floating input (especially for those control pins such as CSB, RSTB, RWR or ERD...) may cause abnormal latch and cause abnormal display.

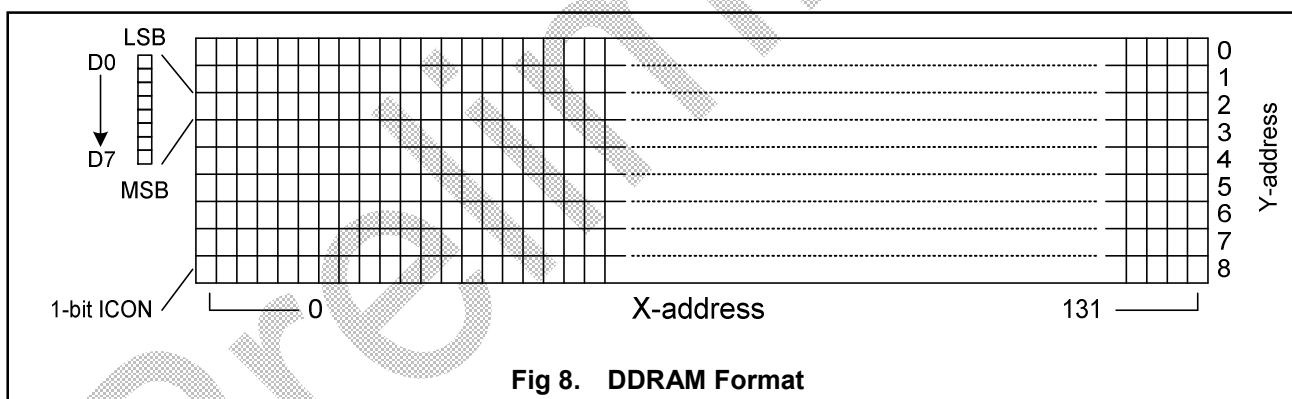
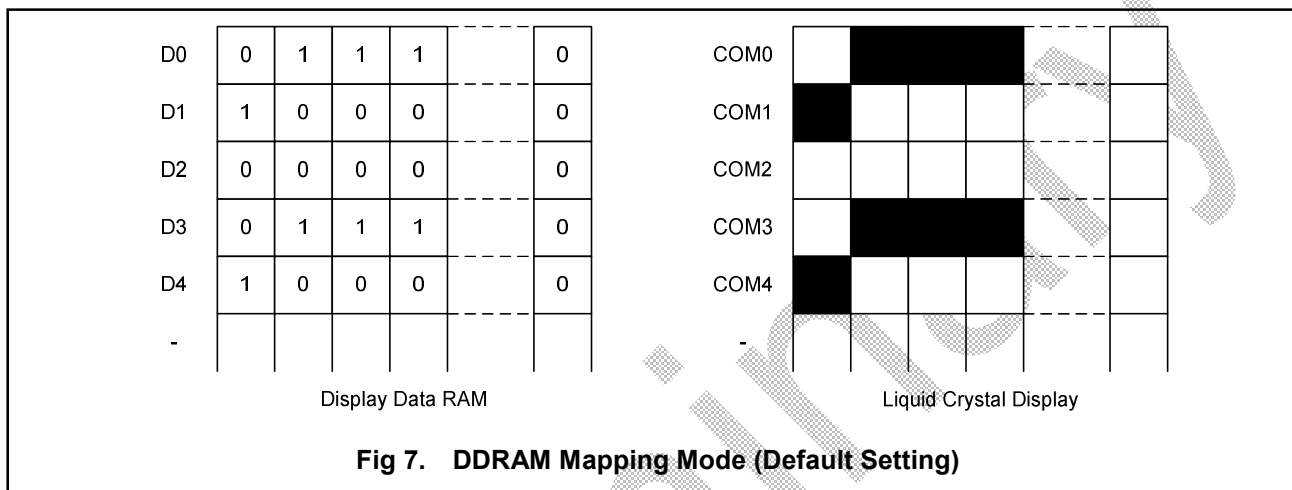
## Data Transfer

ST7567 uses bus latch and internal data bus for interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM as shown in Fig 5. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle as shown in Fig 6. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.



## Display Data RAM (DDRAM)

ST7567 is built-in a RAM with 65X132 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Fig 7 for detailed illustration). The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0). Refer to Fig 8 for detailed illustration. The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.



## Addressing

Data is downloaded into the Display Data RAM matrix in ST7567 as byte-format. The Display Data RAM has a matrix of 65 by 132 bits. The address ranges are: X=0~131 (column address), Y=0~8 (page address). Addresses outside these ranges are not allowed.

### Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the "Page Address Set" instruction only. The Page Address must be set before accessing DDRAM content. Page Address "8" is a special RAM area for the icons with only one valid bit: D0.

### Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. The column address is increased (+1) after each display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address "83h") because the Column Address and Page Address circuits are independent. For example, both Page Address and Column Address should be assigned for changing the DDRAM pointer from (Page-0, Column-83h) to (Page-1, Column-0).

Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG). It is necessary to rewrite the display data into DDRAM after changing MX setting.



The relation between DDRAM and outputs with different MX or MY setting is shown below.

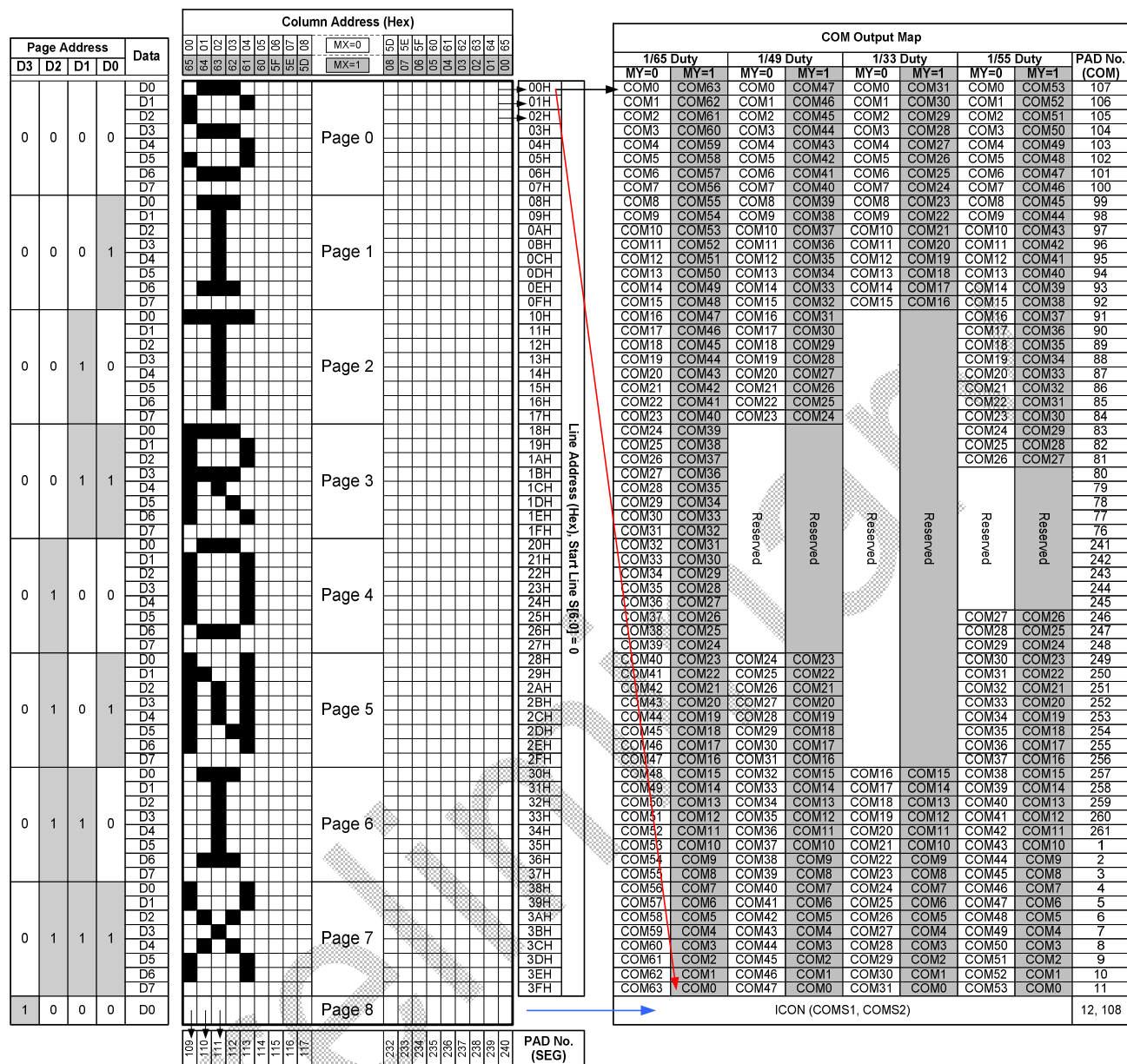


Fig 9. DDRAM and Output Map (COM/SEG)

## Line Address Circuit

The Line Address Circuit incorporates a counter and a Line Address register which is changed only by the “Display Start Line Set” instruction. This circuit assigns DDRAM a Line Address corresponding to the first display line (COM0). Therefore, by setting Line Address repeatedly, ST7567 can realize the screen scrolling without changing the contents of DDRAM as shown in Fig 10. The last common is always the COMS (common output for the icons). That means the icons will never scroll with the general display data.

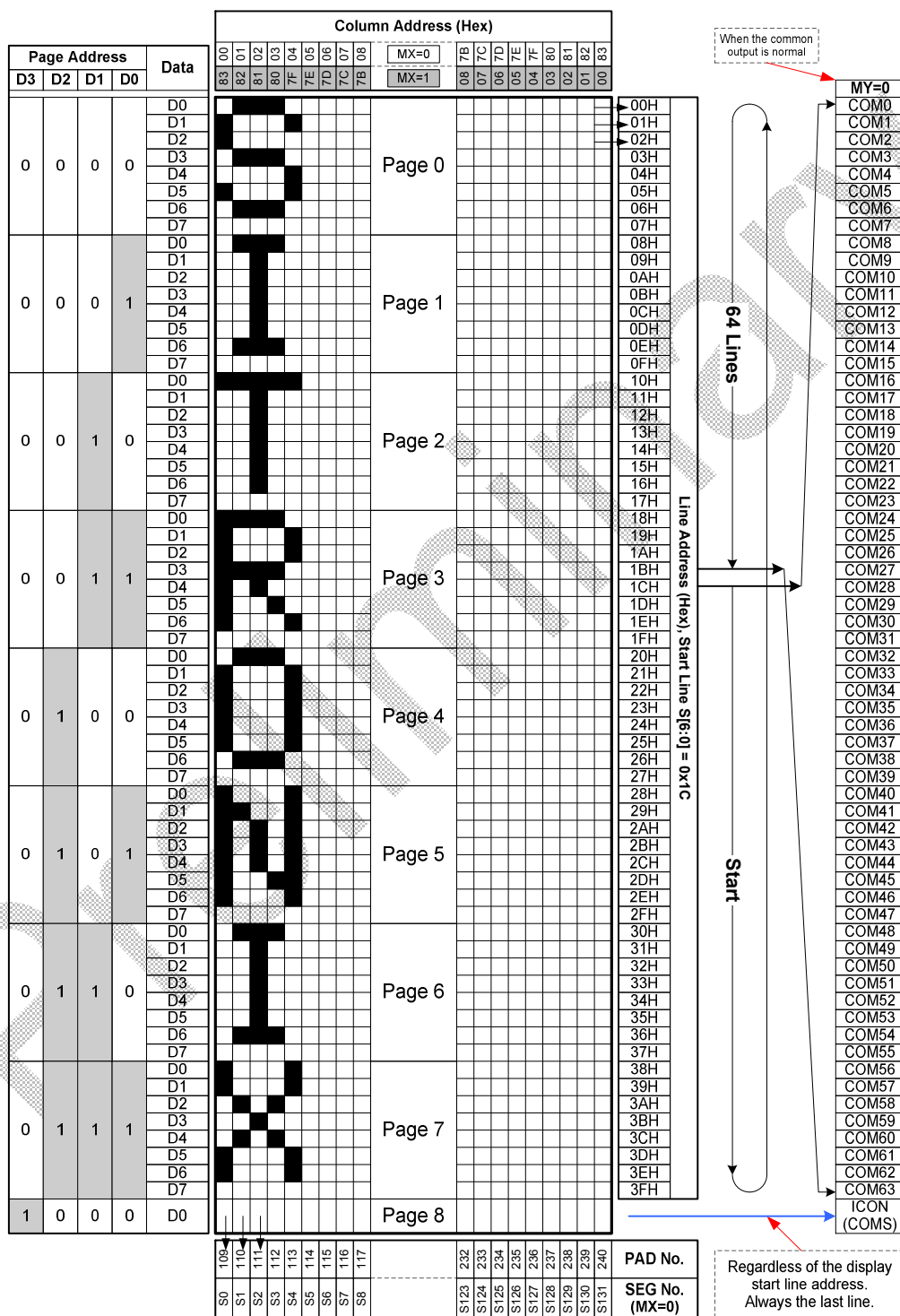


Fig 10. Start Line Function

## Display Data Latch Circuit

The display data latch circuit latches temporarily display data of each segment output which will be output at the next clock. The special functions such as reverse display, display OFF and display all points ON only change the data in the latch and the content in the Display Data RAM is not changed.

## Oscillation Circuit

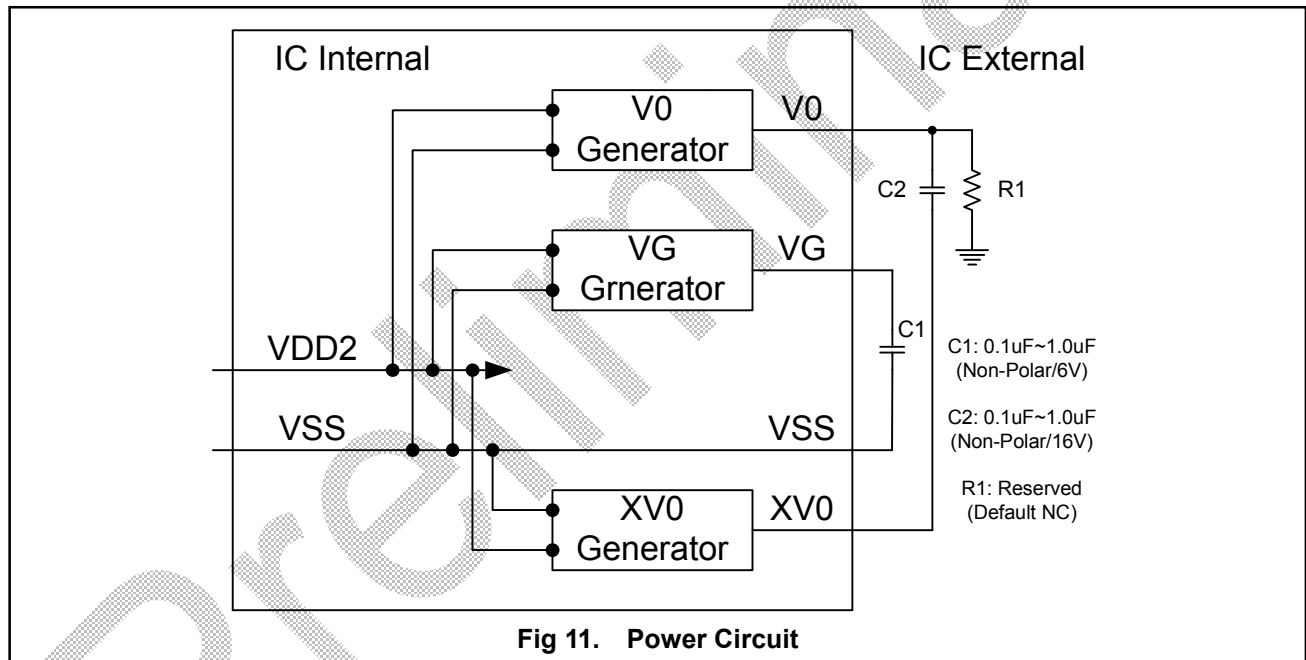
The built-in oscillation circuit generates the system clock for the liquid crystal driving circuit. The oscillation circuit is enabled after initializing ST7567. The clock will not be output to reduce the power consumption.

## Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external components. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST7567 OFF, a Power OFF procedure is needed (please refer to the OPERATION FLOW section).

## External Components of Power Circuit

The recommended external power components need only 2 capacitors. The detailed values of these two capacitors are determined by the panel size and loading.



## Regulator Circuit

The built-in high accuracy regulation circuit has 8 regulation ratios and each one has 64 EV-levels for voltage adjustment. Without additional external component, the output voltage can be changed by instructions such as "Regulation Ratio" and "Set EV". The temperature compensation coefficient of the built-in regulator is  $-0.11\%/^{\circ}\text{C}$ . The detailed setting method can be found in the INSTRUCTION DESCRIPTION section.

## 7. RESET CIRCUIT

Setting RSTB to “L” can initialize internal function. While RSTB is “L”, no instruction except read status can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating. Please note the hardware reset is not same as the software reset. When RSTB becomes “L”, the hardware reset procedure will start. When RESET instruction is executed, the software reset procedure will start. The procedure is listed below:

| Procedure                                                           | Hardware Reset | Software Reset |
|---------------------------------------------------------------------|----------------|----------------|
| Display OFF: D=0, all SEGs/COMs output at VSS                       | V              | X              |
| Normal Display: INV=0, AP=0                                         | V              | X              |
| SEG Normal Direction: MX=0                                          | V              | X              |
| Clear Serial Counter and Shift Register (if using Serial Interface) | V              | X              |
| Bias Selection: BS=0                                                | V              | X              |
| Booster Level BL[1:0]=0                                             | V              | X              |
| Exit Power Saving Mode                                              | V              | X              |
| Power Control OFF: VB=0, VR=0, VF=0                                 | V              | X              |
| Exit Read-modify-Write mode                                         | V              | V              |
| Start Line S[5:0]=0                                                 | V              | V              |
| Column Address X[7:0]=0                                             | V              | V              |
| Page Address Y[3:0]=0                                               | V              | V              |
| COM Normal Direction: MY=0                                          | V              | V              |
| V0 Regulation Ratio RR[2:0]=(1,0,0)                                 | V              | V              |
| EV[5:0]=(1,0,0,0,0,0)                                               | V              | V              |
| Exit Test Mode                                                      | V              | V              |

After power-on, RAM data are undefined and the display status is “Display OFF”. It's better to initialize whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

## 8. INSTRUCTION TABLE

| INSTRUCTION               | A0 | R/W<br>(RWR) | COMMAND BYTE     |    |     |     |     |     |     |     | DESCRIPTION                                                                      |
|---------------------------|----|--------------|------------------|----|-----|-----|-----|-----|-----|-----|----------------------------------------------------------------------------------|
|                           |    |              | D7               | D6 | D5  | D4  | D3  | D2  | D1  | D0  |                                                                                  |
| (1) Display ON/OFF        | 0  | 0            | 1                | 0  | 1   | 0   | 1   | 1   | 1   | D   | D=1, display ON<br>D=0, display OFF                                              |
| (2) Set Start Line        | 0  | 0            | 0                | 1  | S5  | S4  | S3  | S2  | S1  | S0  | Set display start line                                                           |
| (3) Set Page Address      | 0  | 0            | 1                | 0  | 1   | 1   | Y3  | Y2  | Y1  | Y0  | Set page address                                                                 |
| (4)<br>Set Column Address | 0  | 0            | 0                | 0  | 0   | 1   | X7  | X6  | X5  | X4  | Set column address (MSB)                                                         |
|                           | 0  | 0            | 0                | 0  | 0   | 0   | X3  | X2  | X1  | X0  | Set column address (LSB)                                                         |
| (5) Read Status           | 0  | 1            | 0                | MX | D   | RST | 0   | 0   | 0   | 0   | Read IC Status                                                                   |
| (6) Write Data            | 1  | 0            | D7               | D6 | D5  | D4  | D3  | D2  | D1  | D0  | Write display data to RAM                                                        |
| (7) Read Data             | 1  | 1            | D7               | D6 | D5  | D4  | D3  | D2  | D1  | D0  | Read display data from RAM                                                       |
| (8) SEG Direction         | 0  | 0            | 1                | 0  | 1   | 0   | 0   | 0   | 0   | MX  | Set scan direction of SEG<br>MX=1, reverse direction<br>MX=0, normal direction   |
| (9) Inverse Display       | 0  | 0            | 1                | 0  | 1   | 0   | 0   | 1   | 1   | INV | INV =1, inverse display<br>INV =0, normal display                                |
| (10) All Pixel ON         | 0  | 0            | 1                | 0  | 1   | 0   | 0   | 1   | 0   | AP  | AP=1, set all pixel ON<br>AP=0, normal display                                   |
| (11) Bias Select          | 0  | 0            | 1                | 0  | 1   | 0   | 0   | 0   | 1   | BS  | Select bias setting<br>0=1/9, 1=1/7 (at 1/65 duty)                               |
| (12)<br>Read-modify-Write | 0  | 0            | 1                | 1  | 1   | 0   | 0   | 0   | 0   | 0   | Column address increment:<br>Read:+0 , Write:+1                                  |
| (13) END                  | 0  | 0            | 1                | 1  | 1   | 0   | 1   | 1   | 1   | 0   | Exit Read-modify-Write mode                                                      |
| (14) RESET                | 0  | 0            | 1                | 1  | 1   | 0   | 0   | 0   | 1   | 0   | Software reset                                                                   |
| (15) COM Direction        | 0  | 0            | 1                | 1  | 0   | 0   | MY  | -   | -   | -   | Set output direction of COM<br>MY=1, reverse direction<br>MY=0, normal direction |
| (16) Power Control        | 0  | 0            | 0                | 0  | 1   | 0   | 1   | VB  | VR  | VF  | Control built-in power circuit<br>ON/OFF                                         |
| (17) Regulation Ratio     | 0  | 0            | 0                | 0  | 1   | 0   | 0   | RR2 | RR1 | RR0 | Select regulation resistor ratio                                                 |
| (18) Set EV               | 0  | 0            | 1                | 0  | 0   | 0   | 0   | 0   | 0   | 1   | Double command!! Set<br>electronic volume (EV) level                             |
|                           | 0  | 0            | 0                | 0  | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |                                                                                  |
| (19) Set Booster          | 0  | 0            | 1                | 1  | 1   | 1   | 1   | 0   | 0   | 0   | Double command!!<br>Set booster level:<br>00=4X, 01=5X, 10=6X                    |
|                           | 0  | 0            | 0                | 0  | 0   | 0   | 0   | 0   | BL1 | BL0 |                                                                                  |
| (20) Power Save           | 0  | 0            | Compound Command |    |     |     |     |     |     |     | Display OFF + All Pixel ON                                                       |
| (21) NOP                  | 0  | 0            | 1                | 1  | 1   | 0   | 0   | 0   | 1   | 1   | No operation                                                                     |
| (22) Test                 | 0  | 0            | 1                | 1  | 1   | 1   | 1   | 1   | 1   | -   | Do NOT use.<br>Reserved for testing.                                             |

Note: Symbol “-” means this bit can be “H” or “L”.

## 9. INSTRUCTION DESCRIPTION

### Display ON/OFF

The D flag selects the display mode.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 0  | 1  | 1  | 1  | D  |

D=1: Normal Display Mode.

D=0: Display OFF. All SEGs/COMs output with VSS.

### Set Start Line

This instruction sets the line address of the Display Data RAM to determine the initial display line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 1  | S5 | S4 | S3 | S2 | S1 | S0 |

| S5 | S4 | S3 | S2 | S1 | S0 | Line address |
|----|----|----|----|----|----|--------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0            |
| 0  | 0  | 0  | 0  | 0  | 1  | 1            |
| 0  | 0  | 0  | 0  | 1  | 0  | 2            |
| 0  | 0  | 0  | 0  | 1  | 1  | 3            |
| :  | :  | :  | :  | :  | :  | :            |
| 1  | 1  | 1  | 1  | 0  | 1  | 61           |
| 1  | 1  | 1  | 1  | 1  | 0  | 62           |
| 1  | 1  | 1  | 1  | 1  | 1  | 63           |

### Set Page Address

Y [3:0] defines the Y address vector address of the display RAM.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 1  | Y3 | Y2 | Y1 | Y0 |

| Y3 | Y2 | Y1 | Y0 | Page Address      | Valid Bit |
|----|----|----|----|-------------------|-----------|
| 0  | 0  | 0  | 0  | Page0             | D0~ D7    |
| 0  | 0  | 0  | 1  | Page1             | D0~ D7    |
| 0  | 0  | 1  | 0  | Page2             | D0~ D7    |
| :  | :  | :  | :  | :                 | :         |
| 0  | 1  | 1  | 0  | Page6             | D0~ D7    |
| 0  | 1  | 1  | 1  | Page7             | D0~ D7    |
| 1  | 0  | 0  | 0  | Page8 (icon page) | D0        |

## Set Column Address of RAM

The range of column address is 0...131. The parameter is separated into 2 instructions. The column address is increased (+1) after each byte of display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address "83h").

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 0  | 0  | 1  | X7 | X6 | X5 | X4 |

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 0  | 0  | 0  | X3 | X2 | X1 | X0 |

| X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | Column address |
|----|----|----|----|----|----|----|----|----------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1              |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 2              |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 3              |
| :  | :  | :  | :  | :  | :  | :  | :  | :              |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 129            |
| 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 120            |
| 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 131            |

## Read Status

Read the internal status of ST7567. The read function is not available in serial interface mode.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4  | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|-----|----|----|----|----|
| 0  | 1        | 0  | MX | D  | RST | 0  | 0  | 0  | 0  |

| Flag | Description                                                                     |
|------|---------------------------------------------------------------------------------|
| MX   | MX=0: Normal direction (SEG0->SEG131)<br>MX=1: Reverse direction (SEG131->SEG0) |
| D    | D=0: Display ON<br>D=1: Display OFF                                             |
| RST  | RST=1: During reset (hardware or software reset)<br>RST=0: Normal operation     |

## Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

| A0 | R/W(RWR) | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|------------|----|----|----|----|----|----|----|
| 1  | 0        | Write Data |    |    |    |    |    |    |    |

## Read Data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor. The read function is not available in serial interface mode.

| A0 | R/W(RWR) | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|-----------|----|----|----|----|----|----|----|
| 1  | 1        | Read Data |    |    |    |    |    |    |    |

## SEG Direction

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 0  | 0  | 0  | 0  | MX |

| Flag | Description                                                                     |
|------|---------------------------------------------------------------------------------|
| MX   | MX=0: Normal direction (SEG0->SEG131)<br>MX=1: Reverse direction (SEG131->SEG0) |

## Inverse Display

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (white -> Black, Black -> White) while the display data in the Display Data RAM is never changed.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0  |
|----|----------|----|----|----|----|----|----|----|-----|
| 0  | 0        | 1  | 0  | 1  | 0  | 0  | 1  | 1  | INV |

| Flag | Description                                     |
|------|-------------------------------------------------|
| INV  | INV=0: Normal display<br>INV=1: Inverse display |

## All Pixel ON

This instruction will let all segments output the selected voltage and make all pixels turned ON.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 0  | 0  | 1  | 0  | AP |

| Flag | Description                                 |
|------|---------------------------------------------|
| AP   | AP=0: Normal display<br>AP=1: All pixels ON |

## Bias Select

Select LCD bias ratio of the voltage required for driving the LCD.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 0  | 0  | 0  | 1  | BS |

| Duty | Bias |      |
|------|------|------|
|      | BS=0 | BS=1 |
| 1/65 | 1/9  | 1/7  |
| 1/49 | 1/8  | 1/6  |
| 1/33 | 1/6  | 1/5  |
| 1/55 | 1/8  | 1/6  |

Reference LCD Bias Voltage (1/65 Duty with 1/9 Bias)

| Symbol | Bias Voltage |
|--------|--------------|
| V0     | V0           |
| VG     | 2/9 x V0     |
| VM     | 1/9 x V0     |
| VSS    | VSS          |

Please Note:

\* VG range:  $1.24V \leq VG < VDD2$ .

\* VM range:  $0.62V \leq VM < VDD2$ .

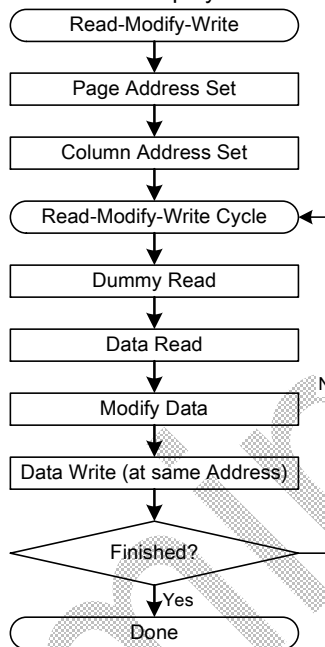


## Read-modify-Write

This command is used paired with the “END” instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address ( $X[7:0]+1$ ). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  |

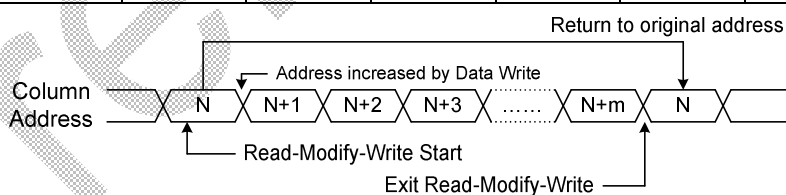
\* In Read-modify-Write mode, other instructions aside from display data read/write commands can also be used.



## END

When the END command is input, the Read-modify-Write mode is released and the column address returns to the address it was when the Read-modify-Write instruction was entered.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  |



## RESET

This instruction resets Start Line (S[5:0]), Column Address (X[7:0]), Page Address (Y[3:0]) and COM Direction (MY) to their default setting. Please note this instruction is not complete same as hardware reset (RSTB=L) and cannot initialize the built-in power circuit which is initialized by the RSTB pin. The detailed information is in “Section 7. RESET CIRCUIT”.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 0  |

## COM Direction

This instruction controls the common output status which changes the vertical display direction. The detailed information can be found in Fig 9.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 0  | 0  | MY | -  | -  | -  |

| Flag | Description                                                                   |
|------|-------------------------------------------------------------------------------|
| MY   | MY=0: Normal direction (COM0->COM63)<br>MY=1: Reverse direction (COM63->COM0) |

## Power Control

This instruction controls the built-in power circuits. Typically, these 3 flags are turned ON at the same time.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 0  | 1  | 0  | 1  | VB | VR | VF |

| Flag | Description                                                 |
|------|-------------------------------------------------------------|
| VB   | VB=0: Built-in Booster OFF<br>VB=1: Built-in Booster ON     |
| VR   | VR=0: Built-in Regulator OFF<br>VR=1: Built-in Regulator ON |
| VF   | VF=0: Built-in Follower OFF<br>VF=1: Built-in Follower ON   |

## Regulation Ratio

This instruction controls the regulation ratio of the built-in regulator.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2  | D1  | D0  |
|----|----------|----|----|----|----|----|-----|-----|-----|
| 0  | 0        | 0  | 0  | 1  | 0  | 0  | RR2 | RR1 | RR0 |

| RR2 | RR1 | RR0 | Regulation Ratio (RR) |
|-----|-----|-----|-----------------------|
| 0   | 0   | 0   | 3.0                   |
| 0   | 0   | 1   | 3.5                   |
| 0   | 1   | 0   | 4.0                   |
| 0   | 1   | 1   | 4.5                   |
| 1   | 0   | 0   | 5.0                   |
| 1   | 0   | 1   | 5.5                   |
| 1   | 1   | 0   | 6.0                   |
| 1   | 1   | 1   | 6.5                   |

The operation voltage (V0) calculation formula is shown below: (RR comes from Regulation Ratio, EV comes from EV[5:0])

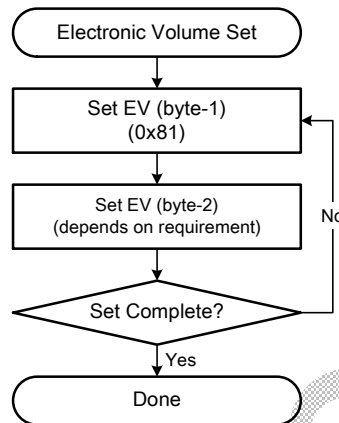
$$V0 = RR \times [1 - (63 - EV) / 162] \times 2.1, \text{ or } V0 = RR \times [(99 + EV) / 162] \times 2.1$$

| SYMBOL | REGISTER | VALUE                             |
|--------|----------|-----------------------------------|
| RR     | RR[2:0]  | 3, 3.5, 4, 4.5, 5, 5.5, 6 and 6.5 |
| EV     | EV[5:0]  | 0~63                              |

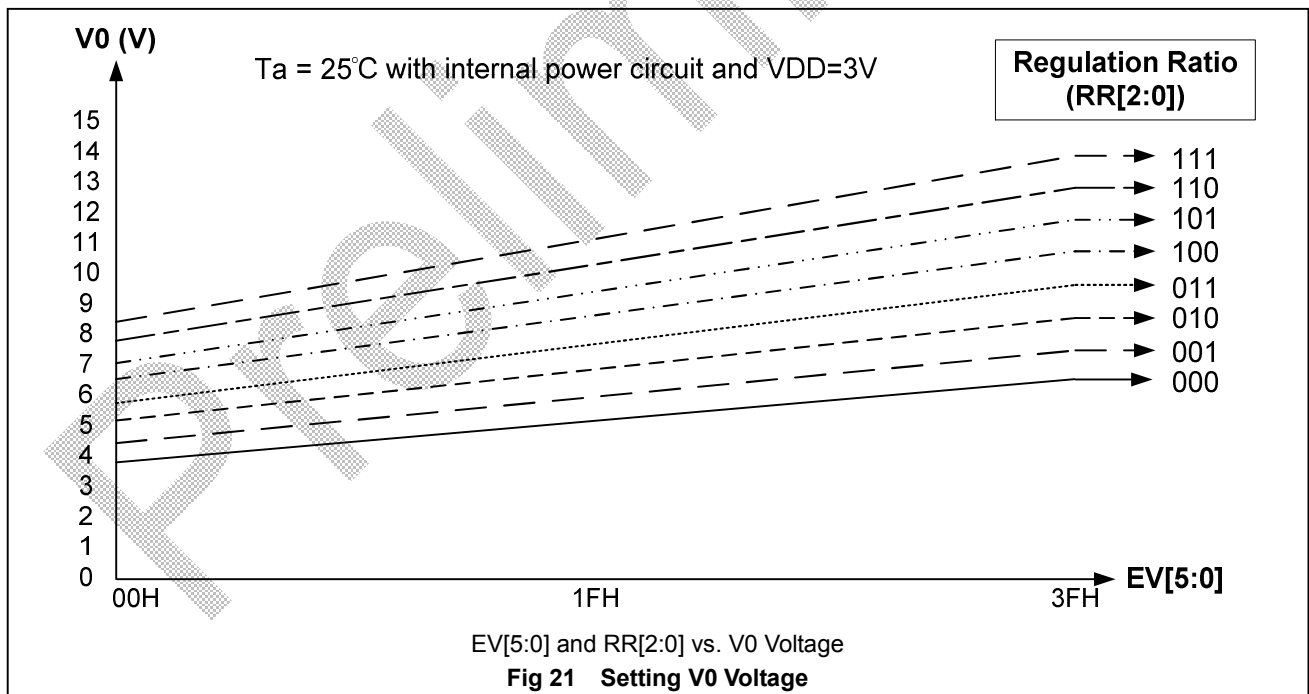
## Set EV

This is double byte instruction. The first byte set ST7567 into EV adjust mode and the following instruction will change the EV setting. That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the LCD.

| A0 | R/W(RWR) | D7 | D6 | D5  | D4  | D3  | D2  | D1  | D0  |
|----|----------|----|----|-----|-----|-----|-----|-----|-----|
| 0  | 0        | 1  | 0  | 0   | 0   | 0   | 0   | 0   | 1   |
| 0  | 0        | 0  | 0  | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |



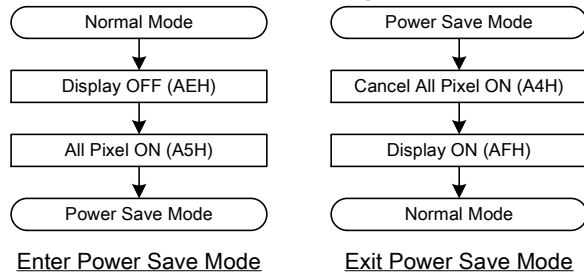
The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of LCD module. There are 8 V0 voltage curve can be selected. It is recommended the EV should be close to the center (1FH) for easy contrast adjustment. Please refer to the "Selection of Application Voltage" section for detailed information.



## Power Save (Compound Instruction)

This is compound instruction. The 1<sup>st</sup> instruction is Display OFF (D=0) and the 2<sup>nd</sup> instruction is All Pixel ON (AP=1). The Power Save mode starts the following procedure: (the display data and register settings are still kept except D-Flag and AP-Flag)

1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at VSS.

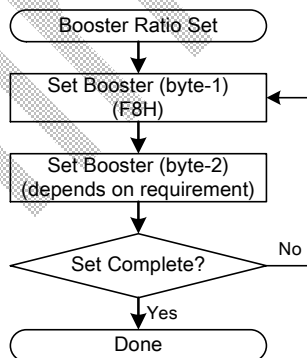


After exiting Power Save mode, the settings will return to be as they were before.

## Set Booster

This is double byte instruction. The first byte set ST7567 into booster configuration mode and the following instruction will change the booster setting. That means these 2 bytes must be used together. They control the built-in booster circuit to provide the power source of the built-in regulator. ST7567 booster is built-in booster capacitors. The only external component is a keep capacitor between V0 and XV0. Booster level can be changed with instruction only without changing hardware connection.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1  | D0  |
|----|----------|----|----|----|----|----|----|-----|-----|
| 0  | 0        | 1  | 1  | 1  | 1  | 1  | 0  | 0   | 0   |
| 0  | 0        | 0  | 0  | 0  | 0  | 0  | 0  | BL1 | BL0 |



## NOP

"No Operation" instruction. ST7567 will do nothing when receiving this instruction.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 1  |

## Test

The test mode is reserved for IC testing. Please don't use this instruction. If the test mode is enabled accidentally, it can be cleared by: issuing an "L" pulse on RSTB pin, issuing RESET instruction or issuing NOP instruction.

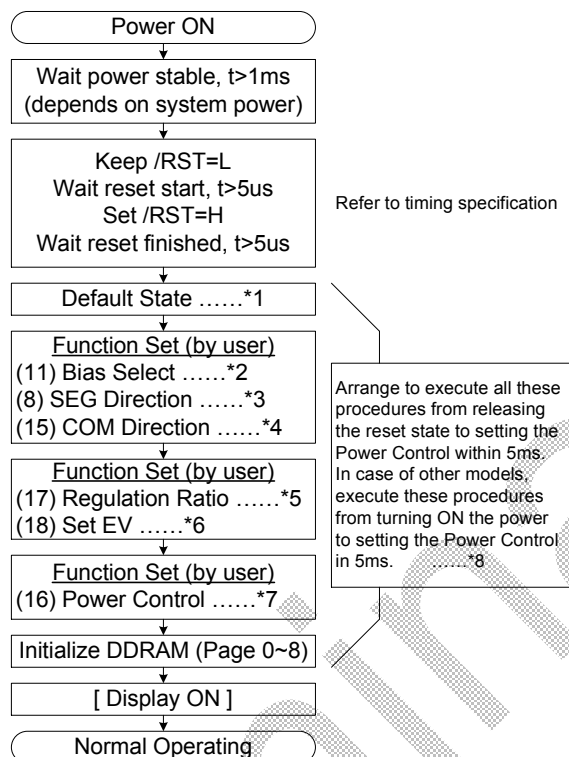
| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 1  | 1  | 1  | 1  | -  |

Note: "-" means "1" or "0".

## 10. OPERATION FLOW

This section introduces some reference operation flows.

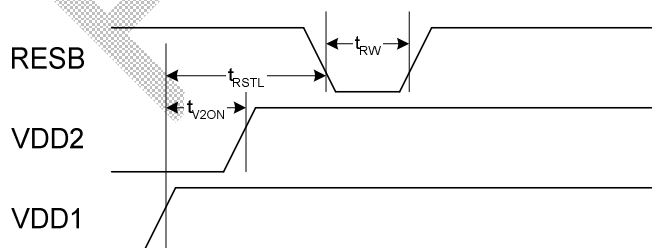
### Power ON and initialization



Note: The detailed description can be found in the respective sections listed below.

- Section 7. RESET CIRCUIT;
- Section 9. INSTRUCTION DESCRIPTION, Bias Select;
- Section 9. INSTRUCTION DESCRIPTION, SEG Direction;
- Section 9. INSTRUCTION DESCRIPTION, COM Direction;
- Section 9. INSTRUCTION DESCRIPTION, Regulation Ratio; APPLICATION NOTE, Selection of Application Voltage;
- Section 9. INSTRUCTION DESCRIPTION, Set EV; APPLICATION NOTE, Selection of Application Voltage;
- Section 9. INSTRUCTION DESCRIPTION, Power Control;
- The 5ms requirement depends on the characteristics of LCD panel and the external component of the power circuit. It is recommended to check with the real products with external component.

### Power Sequence



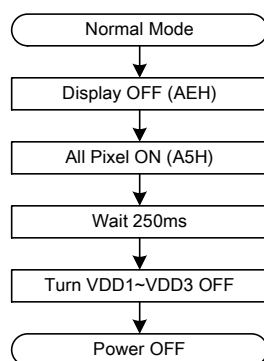
- $t_{V2ON}$ : VDD2 power ON delay.  
 $\Rightarrow 0 \leq t_{V2ON}^{*1}$ .
- $t_{RSTL}$ : Reset high period after VDD1 is stable.  
 $\Rightarrow 0 \leq t_{RSTL} \leq 30 \text{ ms}^{*1}$ .
- $t_{RW}$ : Reset low pulse width.  
Please refer to reset timing specification.

Note:

- IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON. The specification listed here is to prevent abnormal display on LCD module.

## Power OFF Flow and Sequence

ST7567 will go into power save mode by issuing the Power Save instruction (Display OFF + All Pixel ON). The LCD driving outputs are fixed to VSS, built-in power circuits are turned OFF and a discharge process starts.



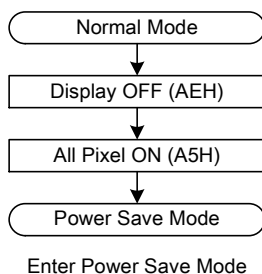
Power OFF Flow

### Instruction Flow

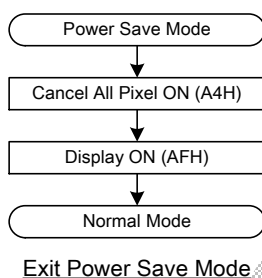
After the built-in power circuits are turned OFF and completely discharged, the power (VDD1 and VDD2) can be removed.

## Power-Save Flow and Sequence

### ENTERING THE POWER SAVE MODE

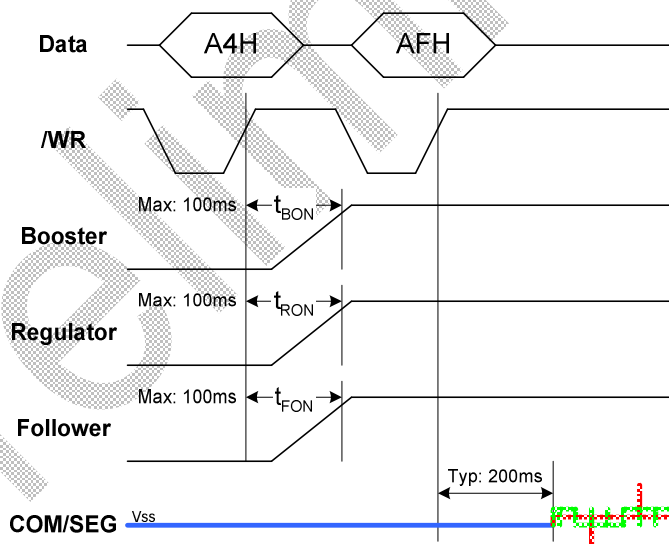


### EXITING THE POWER SAVE MODE



### INTERNAL SEQUENCE of EXIT POWER SAVE MODE

After receiving "PD=0", the internal circuits (Power) will starts the following procedure.



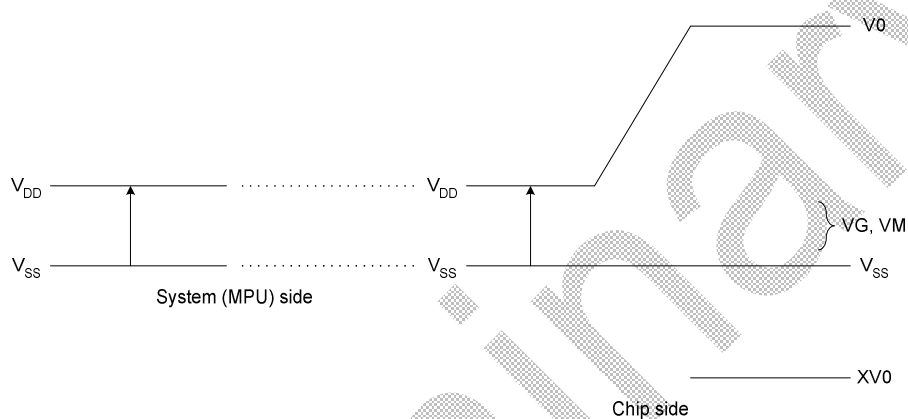
Note:

1. The power stable time is determined by LCD panel loading.
2. The power stable time in this figure is base on: LCD Panel Size = 1.4" with  $C1=1\mu F$ ,  $C2=1\mu F$ .

## 11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

| Parameter                    | Symbol | Conditions  | Unit |
|------------------------------|--------|-------------|------|
| Digital Power Supply Voltage | VDD1   | -0.3 ~ 3.6  | V    |
| Analog Power supply voltage  | VDD2   | -0.3 ~ 3.6  | V    |
| LCD Power supply voltage     | V0-XV0 | -0.3 ~ 16   | V    |
| LCD Power driving voltage    | VG, VM | -0.3 ~ VDD2 | V    |
| Operating temperature        | TOPR   | -30 to +85  | °C   |
| Storage temperature          | TSTR   | -65 to +150 | °C   |



### Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation:  

$$V0 \geq VDD2 > VG > VM > VSS \geq XV0$$



## 12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

## 13. DC CHARACTERISTICS

VDD1=1.8V to 3.3V, VSS=0V; Tamb = -30°C to +85°C; unless otherwise specified.

| Item                                | Symbol           | Condition                         | Rating          |      |      | Unit | Applicable Pin |
|-------------------------------------|------------------|-----------------------------------|-----------------|------|------|------|----------------|
|                                     |                  |                                   | Min.            | Typ. | Max. |      |                |
| Operating Voltage (1)               | VDD1             |                                   | 1.8             | —    | 3.3  | V    | VDD1           |
| Operating Voltage (2)               | VDD2             |                                   | 2.4             | —    | 3.3  | V    | VDD2           |
| Input High-level Voltage            | V <sub>IHC</sub> |                                   |                 |      |      | V    | MPU Interface  |
| Input Low-level Voltage             | V <sub>ILC</sub> |                                   |                 |      |      | V    | MPU Interface  |
| Output High-level Voltage           | V <sub>OHC</sub> | I <sub>OUT</sub> =1mA, VDD1=1.8V  |                 |      |      | V    | D[7:0]         |
| Output Low-level Voltage            | V <sub>OLC</sub> | I <sub>OUT</sub> =-1mA, VDD1=1.8V |                 |      |      | V    | D[7:0]         |
| Input Leakage Current               | I <sub>LI</sub>  |                                   |                 |      |      | μA   | MPU Interface  |
| Output Leakage Current              | I <sub>LO</sub>  |                                   |                 |      |      | μA   | MPU Interface  |
| Liquid Crystal Driver ON Resistance | R <sub>ON</sub>  | Ta=25°C                           | Vop=9V, ΔV=0.9V |      |      | KΩ   | COMx           |
|                                     |                  |                                   | VG=2V, ΔV=0.2V  |      |      | KΩ   | SEGx           |
| Frame Frequency                     | FR               | FR default (1,0,0)<br>Ta = 25°C   |                 |      |      | Hz   |                |

Note:

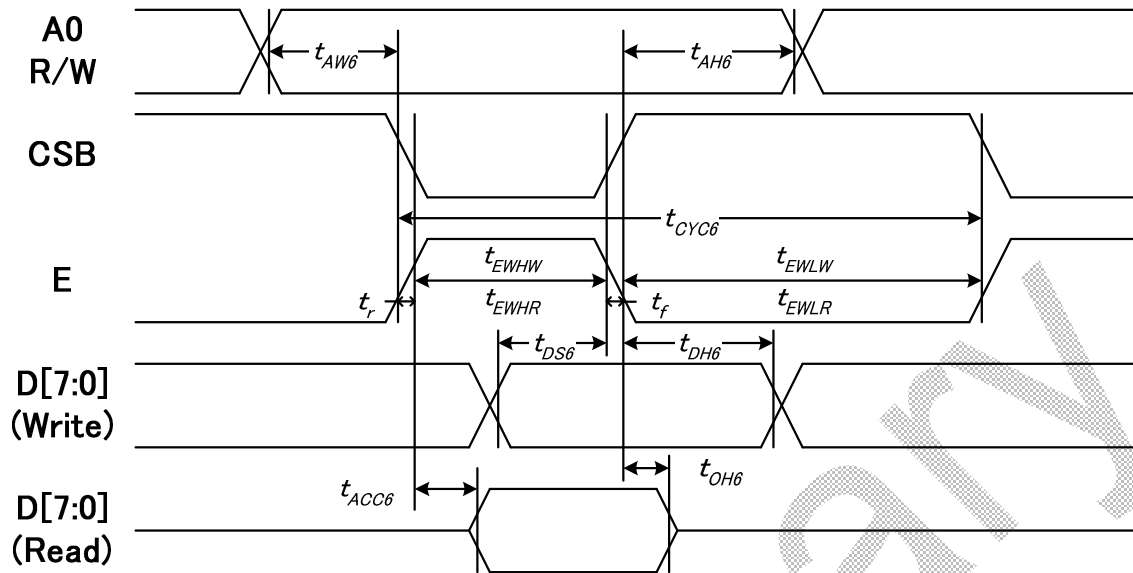
1. Recommend application Vop range : 4V ~ 9.5V.
2. LCD module size : 1.8" (max).

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

| Test Pattern                   | Symbol | Condition                                                                        | Rating |      |      | Unit | Note |
|--------------------------------|--------|----------------------------------------------------------------------------------|--------|------|------|------|------|
|                                |        |                                                                                  | Min.   | Typ. | Max. |      |      |
| Display Pattern: SNOW (Static) | ISS    | VDD1=VDD2=3.0V,<br>Booster X5<br>V <sub>OP</sub> = 9.0 V, Blk = 1/9<br>Ta = 25°C |        |      |      | μA   |      |
| Power Down                     | ISS    | VDD1=VDD2=3.0V,<br>Ta=25°C                                                       |        |      |      | μA   |      |

## 14. TIMING CHARACTERISTICS

### System Bus Timing for 6800 Series MPU



(VDD = 3.3V , Ta = -30~85°C)

| Item                          | Signal | Symbol | Condition  | Min. | Max. | Unit |
|-------------------------------|--------|--------|------------|------|------|------|
| Address setup time            | A0     | tAW6   |            |      |      | ns   |
| Address hold time             |        | tAH6   |            |      |      |      |
| System cycle time             | E      | tCYC6  |            |      |      |      |
| Enable L pulse width (WRITE)  |        | tEHLW  |            |      |      |      |
| Enable H pulse width (WRITE)  |        | tEHWLW |            |      |      |      |
| Enable L pulse width (READ)   |        | tEHLR  |            |      |      |      |
| Enable H pulse width (READ)   |        | tEHWLR |            |      |      |      |
| Write data setup time         | D[7:0] | tDS6   |            |      |      |      |
| Write data hold time          |        | tDH6   |            |      |      |      |
| Read data access time         |        | tACC6  | CL = 16 pF |      |      |      |
| Read data output disable time |        | tOH6   | CL = 16 pF |      |      |      |

(VDD = 2.8V , Ta = -30~85°C)

| Item                          | Signal | Symbol | Condition  | Min. | Max. | Unit |
|-------------------------------|--------|--------|------------|------|------|------|
| Address setup time            | A0     | tAW6   |            |      |      | ns   |
| Address hold time             |        | tAH6   |            |      |      |      |
| System cycle time             | E      | tCYC6  |            |      |      |      |
| Enable L pulse width (WRITE)  |        | tEHLW  |            |      |      |      |
| Enable H pulse width (WRITE)  |        | tEHWLW |            |      |      |      |
| Enable L pulse width (READ)   |        | tEHLR  |            |      |      |      |
| Enable H pulse width (READ)   |        | tEHWLR |            |      |      |      |
| Write data setup time         | D[7:0] | tDS6   |            |      |      |      |
| Write data hold time          |        | tDH6   |            |      |      |      |
| Read data access time         |        | tACC6  | CL = 16 pF |      |      |      |
| Read data output disable time |        | tOH6   | CL = 16 pF |      |      |      |

(VDD = 1.8V , Ta = -30~85°C)

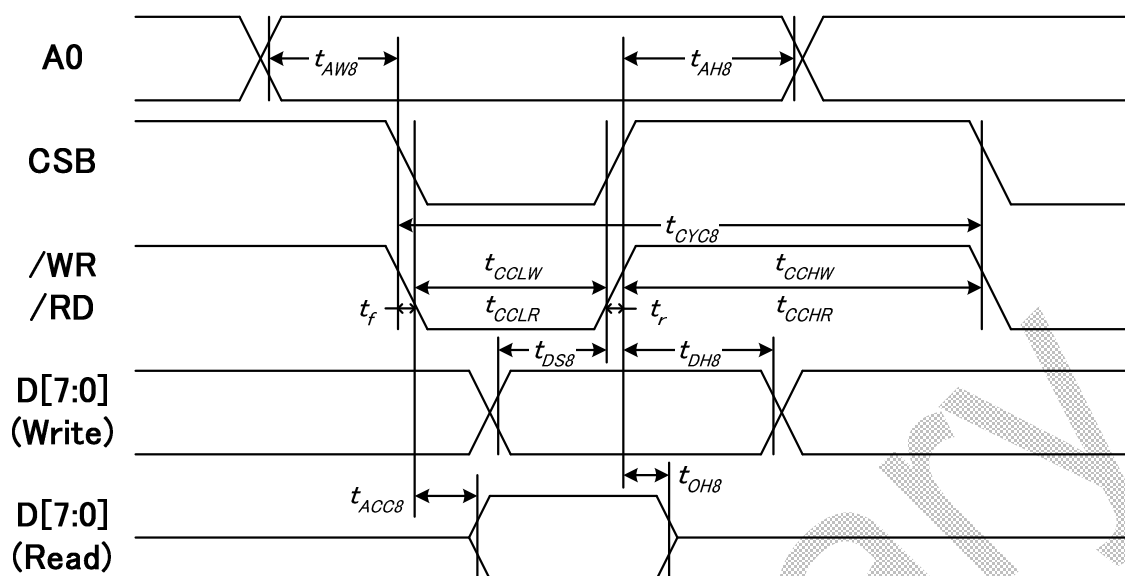
| Item                          | Signal | Symbol | Condition  | Min. | Max. | Unit |
|-------------------------------|--------|--------|------------|------|------|------|
| Address setup time            | A0     | tAW6   |            |      |      | ns   |
| Address hold time             |        | tAH6   |            |      |      |      |
| System cycle time             | E      | tCYC6  |            |      |      |      |
| Enable L pulse width (WRITE)  |        | tEWLW  |            |      |      |      |
| Enable H pulse width (WRITE)  |        | tEWHW  |            |      |      |      |
| Enable L pulse width (READ)   |        | tEWLR  |            |      |      |      |
| Enable H pulse width (READ)   |        | tEWHR  |            |      |      |      |
| Write data setup time         | D[7:0] | tDS6   |            |      |      |      |
| Write data hold time          |        | tDH6   |            |      |      |      |
| Read data access time         |        | tACC6  | CL = 16 pF |      |      |      |
| Read data output disable time |        | tOH6   | CL = 16 pF |      |      |      |

\*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 - tEWLW - tEWHW) for (tr + tf) ≤ (tCYC6 - tEWLR - tEWHR) are specified.

\*2 All timing is specified using 20% and 80% of VDD1 as the reference.

\*3 tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.

## System Bus Timing for 8080 Series MPU



(VDD = 3.3V , Ta = -30~85°C)

| Item                         | Signal | Symbol | Condition  | Min. | Max. | Unit |
|------------------------------|--------|--------|------------|------|------|------|
| Address setup time           | A0     | tAW8   |            |      |      | ns   |
| Address hold time            |        | tAH8   |            |      |      |      |
| System cycle time            | /WR    | tCYC8  |            |      |      |      |
| Enable L pulse width (WRITE) |        | tCCLW  |            |      |      |      |
| Enable H pulse width (WRITE) |        | tCCHW  |            |      |      |      |
| Enable L pulse width (READ)  |        | tCCLR  |            |      |      |      |
| Enable H pulse width (READ)  | RD     | tCCHR  |            |      |      |      |
| WRITE Data setup time        |        | tDS8   |            |      |      |      |
| WRITE Data hold time         |        | tDH8   |            |      |      |      |
| READ access time             |        | tACC8  | CL = 16 pF |      |      |      |
| READ Output disable time     | D[7:0] | tOH8   | CL = 16 pF |      |      |      |

(VDD = 2.8V , Ta = -30~85°C)

| Item                         | Signal | Symbol | Condition  | Min. | Max. | Unit |
|------------------------------|--------|--------|------------|------|------|------|
| Address setup time           | A0     | tAW8   |            |      |      | ns   |
| Address hold time            |        | tAH8   |            |      |      |      |
| System cycle time            | /WR    | tCYC8  |            |      |      |      |
| Enable L pulse width (WRITE) |        | tCCLW  |            |      |      |      |
| Enable H pulse width (WRITE) |        | tCCHW  |            |      |      |      |
| Enable L pulse width (READ)  |        | tCCLR  |            |      |      |      |
| Enable H pulse width (READ)  | RD     | tCCHR  |            |      |      |      |
| WRITE Data setup time        |        | tDS8   |            |      |      |      |
| WRITE Data hold time         |        | tDH8   |            |      |      |      |
| READ access time             |        | tACC8  | CL = 16 pF |      |      |      |
| READ Output disable time     | D[7:0] | tOH8   | CL = 16 pF |      |      |      |

(VDD = 1.8V , Ta = -30~85°C)

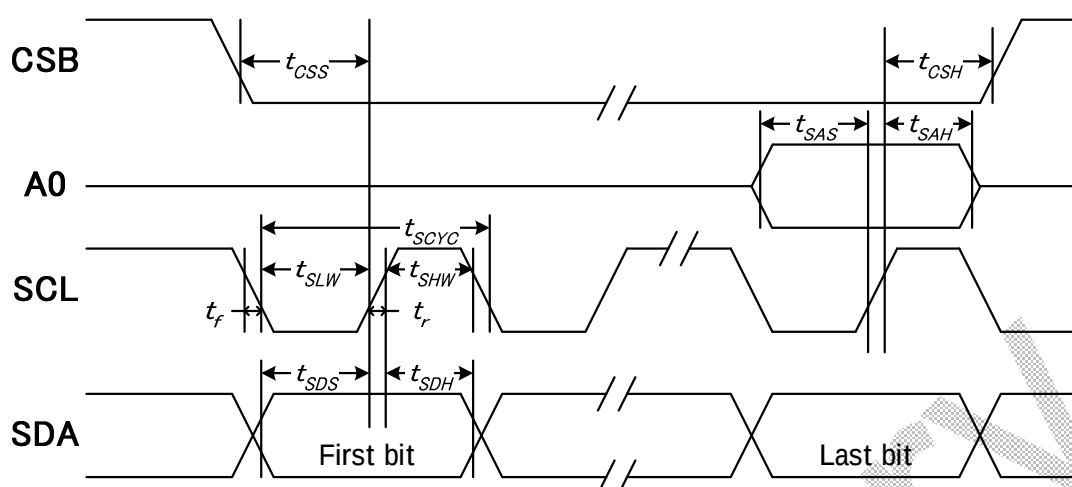
| Item                         | Signal | Symbol | Condition  | Min. | Max. | Unit |
|------------------------------|--------|--------|------------|------|------|------|
| Address setup time           | A0     | tAW8   |            |      |      | ns   |
| Address hold time            |        | tAH8   |            |      |      |      |
| System cycle time            | /WR    | tCYC8  |            |      |      |      |
| Enable L pulse width (WRITE) |        | tCCLW  |            |      |      |      |
| Enable H pulse width (WRITE) |        | tCCLH  |            |      |      |      |
| Enable L pulse width (READ)  | RD     | tCCLW  |            |      |      |      |
| Enable H pulse width (READ)  |        | tCCLH  |            |      |      |      |
| WRITE Data setup time        | D[7:0] | tDS8   |            |      |      |      |
| WRITE Data hold time         |        | tDH8   |            |      |      |      |
| READ access time             |        | tACC8  | CL = 16 pF |      |      |      |
| READ Output disable time     |        | tOH8   | CL = 16 pF |      |      |      |

\*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 - tCCLW - tCCHW) for (tr + tf) ≤ (tCYC8 - tCCLR - tCCHR) are specified.

\*2 All timing is specified using 20% and 80% of VDD1 as the reference.

\*3 tCCLW and tCCLR are specified as the overlap between CSB being "L" and WR and RD being at the "L" level.

## System Bus Timing for 4-Line Serial Interface



(VDD = 3.3V, Ta = -30~85°C)

| Item                 | Signal | Symbol | Condition | Min. | Max. | Unit |
|----------------------|--------|--------|-----------|------|------|------|
| Serial clock period  | SCLK   | tSCYC  |           |      |      | ns   |
| SCLK "H" pulse width |        | tSHW   |           |      |      |      |
| SCLK "L" pulse width |        | tSLW   |           |      |      |      |
| Address setup time   | A0     | tSA    |           |      |      |      |
| Address hold time    |        | tSAH   |           |      |      |      |
| Data setup time      | SDA    | tSDS   |           |      |      |      |
| Data hold time       |        | tSDH   |           |      |      |      |
| CSB-SCLK time        | CSB    | tCSS   |           |      |      |      |
| CSB-SCLK time        |        | tCSH   |           |      |      |      |

(VDD = 2.8V, Ta = -30~85°C)

| Item                 | Signal | Symbol | Condition | Min. | Max. | Unit |
|----------------------|--------|--------|-----------|------|------|------|
| Serial clock period  | SCLK   | tSCYC  |           |      |      | ns   |
| SCLK "H" pulse width |        | tSHW   |           |      |      |      |
| SCLK "L" pulse width |        | tSLW   |           |      |      |      |
| Address setup time   | A0     | tSA    |           |      |      |      |
| Address hold time    |        | tSAH   |           |      |      |      |
| Data setup time      | SDA    | tSDS   |           |      |      |      |
| Data hold time       |        | tSDH   |           |      |      |      |
| CSB-SCLK time        | CSB    | tCS    |           |      |      |      |
| CSB-SCLK time        |        | tCSH   |           |      |      |      |

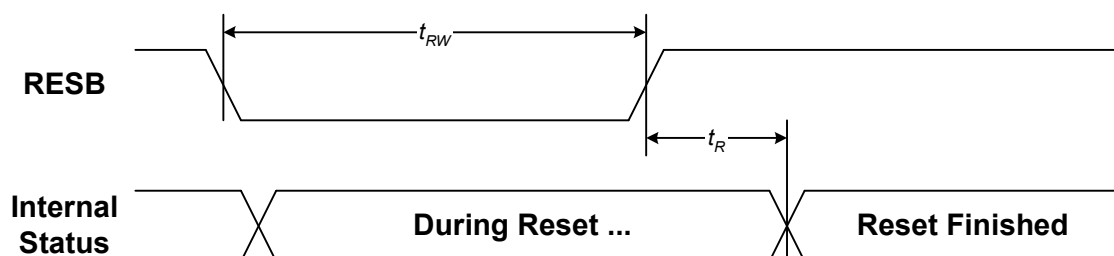
(VDD = 1.8V , Ta = -30~85°C)

| Item                 | Signal | Symbol | Condition | Min. | Max. | Unit |
|----------------------|--------|--------|-----------|------|------|------|
| Serial clock period  | SCLK   | tSCYC  |           |      |      | ns   |
| SCLK "H" pulse width |        | tSHW   |           |      |      |      |
| SCLK "L" pulse width |        | tSLW   |           |      |      |      |
| Address setup time   | A0     | tSA    |           |      |      |      |
| Address hold time    |        | tSH    |           |      |      |      |
| Data setup time      | SDA    | tSDS   |           |      |      |      |
| Data hold time       |        | tSDH   |           |      |      |      |
| CSB-SCLK time        | CSB    | tCSS   |           |      |      |      |
| CSB-SCLK time        |        | tCS    |           |      |      |      |

\*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

\*2 All timing is specified using 20% and 80% of VDD1 as the standard.

## Hardware Reset Timing



(VDD = 3.3V , Ta = -30~85°C)

| Item                  | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|--------|-----------|------|------|------|
| Reset time            | tR     |           |      |      | us   |
| Reset "L" pulse width | tRW    |           |      |      |      |

(VDD = 2.8V , Ta = -30~85°C)

| Item                  | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|--------|-----------|------|------|------|
| Reset time            | tR     |           |      |      | us   |
| Reset "L" pulse width | tRW    |           |      |      |      |

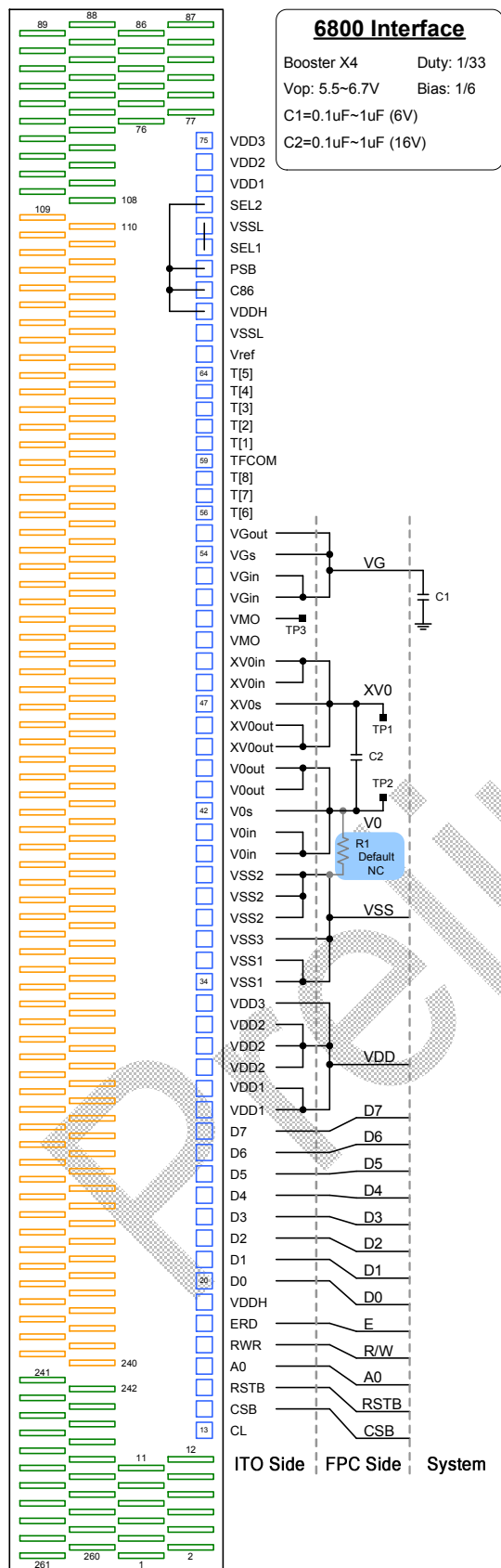
(VDD = 1.8V , Ta = -30~85°C)

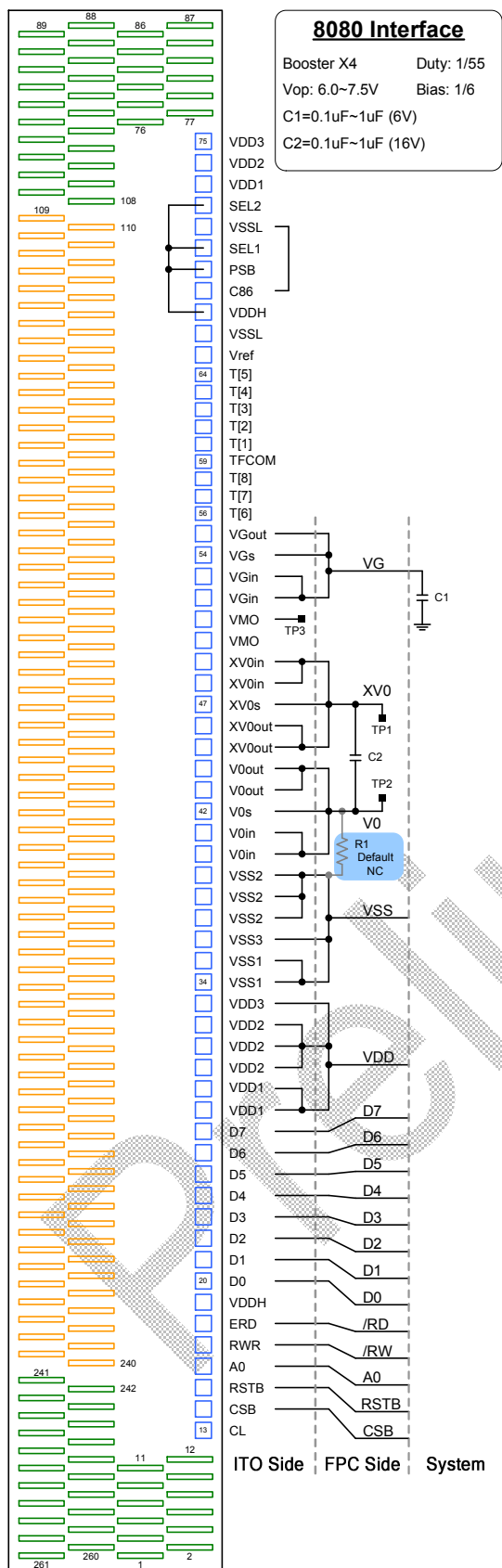
| Item                  | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|--------|-----------|------|------|------|
| Reset time            | tR     |           |      |      | us   |
| Reset "L" pulse width | tRW    |           |      |      |      |

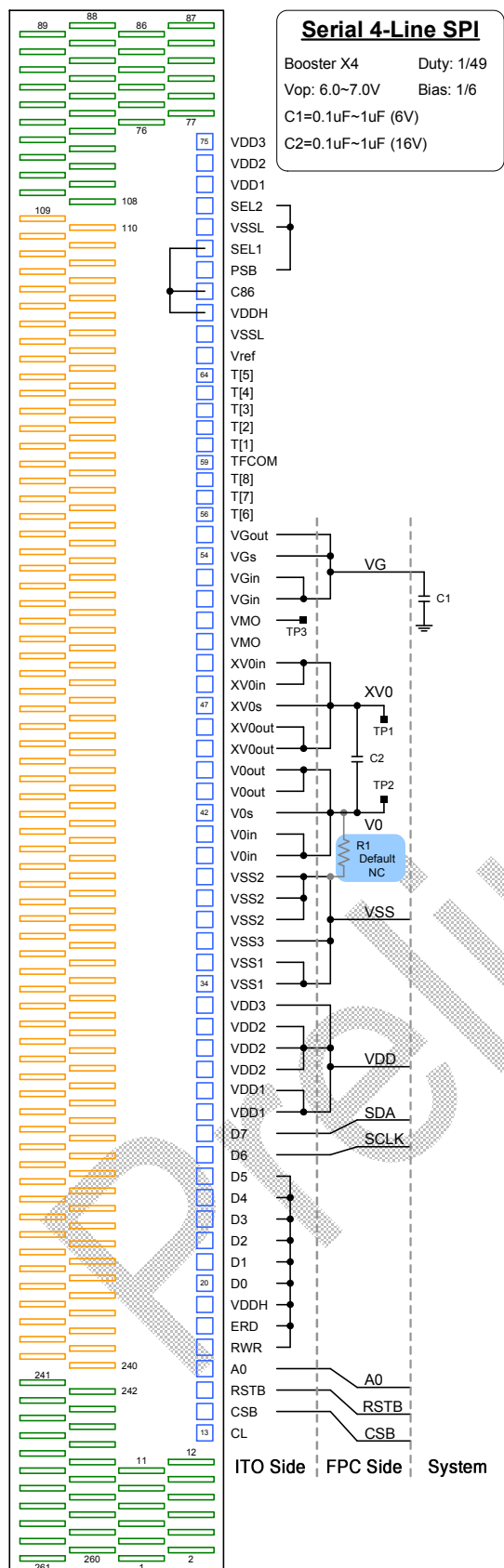


## APPLICATION NOTE

### Application Circuits







## Selection of Application Voltage

### Power Range Summary

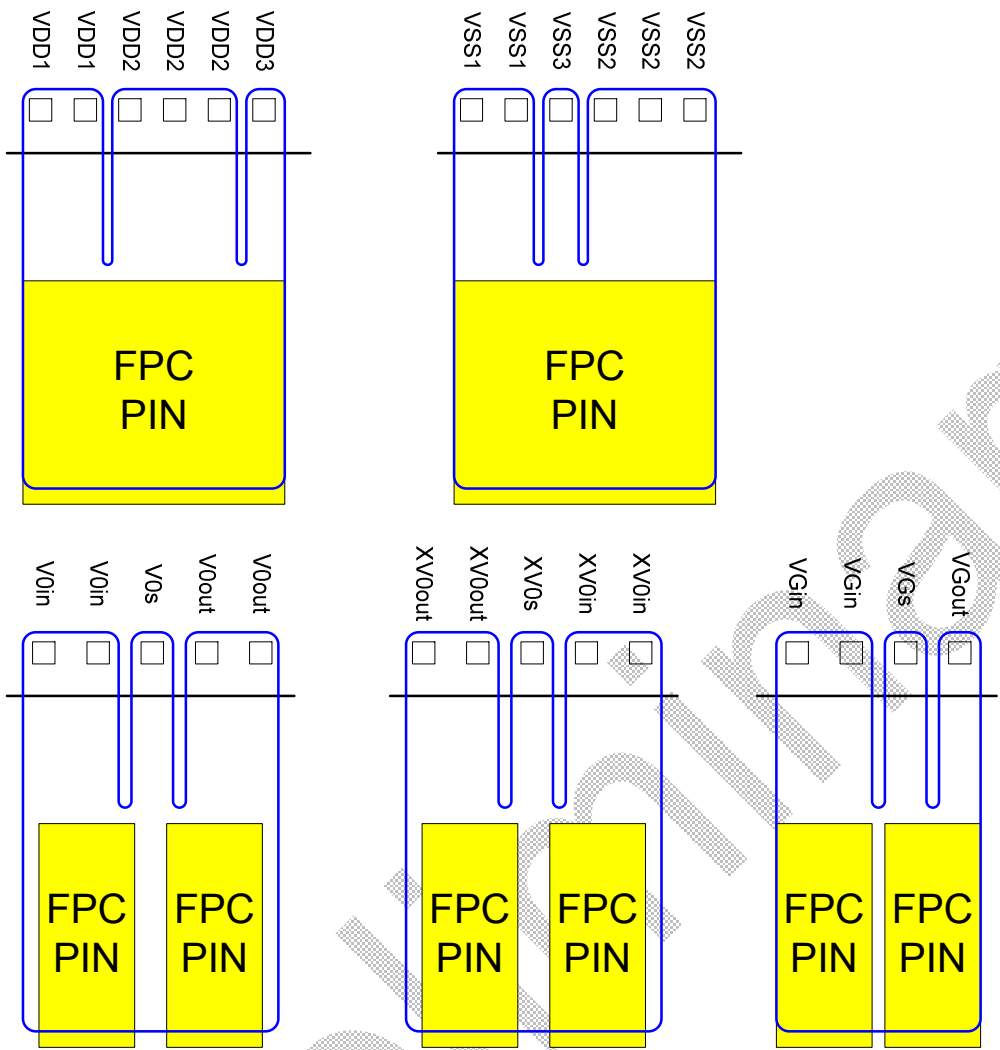
- Positive Booster:  $(VDD2 \times PCn \times BE) \geq V0$  or  $(VDD2 \times PCn \times BE) \geq Vop$ ;
- Negative Booster:  $[-VDD2 \times (PCn - 1) \times BE] \leq XV0$  or  $[VDD2 \times (PCn - 1) \times BE] \geq (Vop - VG)$ ,  
where  $VG = Vop \times 2 / N$ ;
- Vop requirement:  $[VDD2 \times (PCn - 1) \times BE] \geq [Vop \times (N - 2) / N]$  or  $[Vop \leq VDD2 \times (PCn - 1) \times BE \times N / (N - 2)]$ .
- PCn is the booster stage and BE is the booster efficiency. Referential values are listed below: (assume VDD2=2.4V)  
Module Size  $\leq 1.4"$ : BE=80% (min);  
Module Size =  $1.4" \sim 1.8"$ : BE=76% (min).  
Actual BE should be determined by module loading and ITO resistance value.
- $1.24 \leq VG < VDD2$ . Recommend VG is: VDD2-VG around 0.5~0.8V.
- $VM=VG/2$  and  $0.62V \leq VM < VDD2$ .
- The worse condition should be considered:  
Low temperature effect and display on with snow pattern on panel (max: 1.8").

### Referential LCD Module Setting

VDD1=1.8V ~ 3.3V, VDD2=2.4V ~ 3.3V, Panel Size= ~85°C

| Duty | Booster | Bias |
|------|---------|------|
|      |         |      |
|      |         |      |
|      |         |      |

Note: It is recommended to reserve a range for adjustment and temperature effect.



**REVERSION HISTORY**

| Version | Date       | Description                                                                                                                                                                                                                                                  |
|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0.0     |            |                                                                                                                                                                                                                                                              |
| 0.0a    | 2007/06/2  | <ul style="list-style-type: none"><li>● Rearrange section.</li><li>● Rewrite description.</li><li>● Add Application Circuit.</li></ul>                                                                                                                       |
| 0.1     | 2007/06/19 | <ul style="list-style-type: none"><li>● Add pad location.</li><li>● Redraw application circuit (remove VMO capacitor).</li><li>● Reserve R1 for abnormal power off procedure.</li><li>● Rewrite description.</li><li>● Add more application notes.</li></ul> |

With collaboration of <https://www.displayfuture.com>