

# **SSD1673**

## ***Product Preview***

### **Active Matrix EPD 150 x 250 Display Driver with Controller**

This document contains information on a product under development. Solomon Systech reserves the right to change or discontinue this product without notice.

### Appendix: IC Revision history of SSD1673 Specification

| Revision | Change Items                                                                                                             | Effective Date |
|----------|--------------------------------------------------------------------------------------------------------------------------|----------------|
| 0.10     | Initial Release                                                                                                          | 09-Apr-14      |
| 0.11     | - Updated Section 7 Command Table<br>- Added VCOM OTP Program and WS OTP Program in Section 9 Typical Operating Sequence | 07-Jul-14      |
| 0.12     | - Updated Section 11 DC CHARACTERISTICS<br>- Added Section 14.1 DIE TRAY DIMENSIONS                                      | 20-Aug-14      |
| 0.20     | - Revised the LUT format and corresponding OTP content mapping.                                                          | 20-Nov-14      |
| 0.21     | - Added Panel Break Detection                                                                                            | 24-Nov-14      |

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## 1 GENERAL DESCRIPTION

The SSD1673 is a CMOS active matrix bistable display driver with controller. It consists of 150 source outputs, 250 gate outputs, 1 VCOM and 1 VBD for border that can support a maximum display resolution 150x250.

The SSD1673 embeds booster, regulators and oscillator. Data/Commands are sent from general MCU through the hardware selectable Serial Peripheral Interface.

## 2 FEATURES

- Design for dot matrix type active matrix EPD display, support mono color for black/white
- Resolution: 150 source outputs; 250 gate outputs; 1 VCOM; 1VBD for border
- Power supply
  - VCI: 2.4 to 3.7V
  - VDDIO: Connect to VCI
  - VDD: 1.8V, regulate from VCI supply
- Gate driving output voltage:
  - 2 levels output (VGH, VGL)
  - Max 42Vp-p
  - VGH: 22V
  - VGL: -20V
- Source / VBD driving output voltage:
  - 3 levels output (VSH, VSS, VSL)
  - VSH: 15V
  - VSL: -15V
- Low current deep sleep mode
- Support mono color for black/white
- On chip display RAM with double display buffer
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- Serial peripheral interface available
- Available in COG package

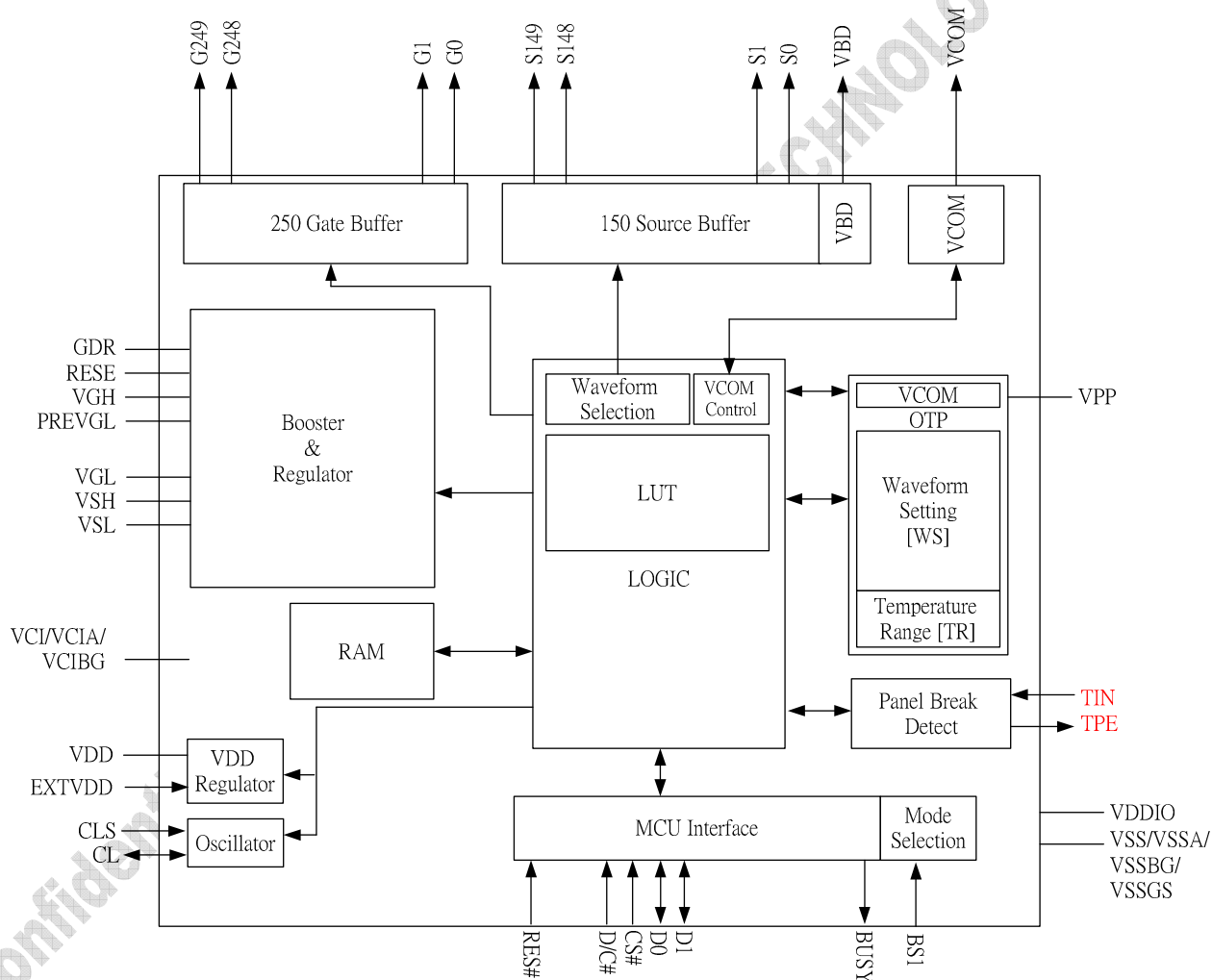
### 3 ORDERING INFORMATION

Table 3-1 : Ordering Information

| Ordering Part Number | Package Form  | Reference | Remark               |
|----------------------|---------------|-----------|----------------------|
| SSD1673Z             | Gold Bump Die |           | 300um die thickness. |

### 4 BLOCK DIAGRAM

Figure 4-1 : SSD1673 Block Diagram



## 5 PIN DESCRIPTION

**Key:** I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin  
NC = Not Connected, Pull L =connect to V<sub>SS</sub>, Pull H = connect to V<sub>DDIO</sub>

| Pin name           | Type | Connect to   | Function                       | Description                                                                                                                                          | When not in use |
|--------------------|------|--------------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| <b>Input power</b> |      |              |                                |                                                                                                                                                      |                 |
| VCI                | P    | Power Supply | Power Supply                   | Power Supply for the chip.                                                                                                                           | -               |
| VCIA               | P    | Power Supply | Power Supply                   | Power input for the chip, Connected with VCI.                                                                                                        | -               |
| VCIBG              | P    | Power Supply | Power Supply                   | Power input for the chip (Reference), Connected with VCI.                                                                                            | -               |
| VDDIO              | P    | Power Supply | Power for interface logic pins | Power Supply for the Interface, it should be connected with VCI.                                                                                     | -               |
| VDD                | P    | Capacitor    | Regulator output               | Core logic power pin.<br>VDD can be regulated internally from VCI.<br>- A capacitor should be connected between VDD and VSS under all circumstances. | -               |
| EXTVDD             | I    | VDDIO        | Regulator bypass               | This pin is VDD regulator bypass pin.<br>- EXTVDD should be connected to VSS.                                                                        | -               |
| VSS                | P    | VSS          | GND                            | Ground (Digital).                                                                                                                                    | -               |
| VSSA               | P    | VSS          | GND                            | Ground (Analog).<br>It should be connected with VSS.                                                                                                 | -               |
| VSSBG              | P    | VSS          | GND                            | Ground (Reference).<br>Connected with VSS.                                                                                                           | -               |
| VSSGS              | P    | VSS          | GND                            | Ground (Output).<br>Connected with VSS.                                                                                                              | -               |
| VPP                | P    | Power Supply | OTP power                      | Power Supply for OTP Programming.                                                                                                                    | Open            |

| Digital I/O |                                                           |                                 |                              |                                                                                                                                                                                                                                                                                                                                         |              |               |   |                                           |   |                                                           |   |
|-------------|-----------------------------------------------------------|---------------------------------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|---|-------------------------------------------|---|-----------------------------------------------------------|---|
| D [1:0]     | I/O                                                       | MPU                             | Data Bus                     | SPI mode:<br>D0: SCLK<br>D1: SDIN                                                                                                                                                                                                                                                                                                       | -            |               |   |                                           |   |                                                           |   |
| CS#         | I                                                         | MPU                             | Logic Control                | This pin is the chip select input connecting to the MCU.                                                                                                                                                                                                                                                                                | VDDIO or VSS |               |   |                                           |   |                                                           |   |
| D/C#        | I                                                         | MPU                             |                              | This pin is Data/Command control pin connecting to the MCU.                                                                                                                                                                                                                                                                             | VDDIO or VSS |               |   |                                           |   |                                                           |   |
| RES#        | I                                                         | MPU                             | System Reset                 | This pin is reset signal input.<br>Active Low.                                                                                                                                                                                                                                                                                          | -            |               |   |                                           |   |                                                           |   |
| BUSY        | O                                                         | MPU                             | Device Busy Signal           | This pin is Busy state output pin.<br>When Busy is High, the operation of the chip should not be interrupted, and command should not be sent.                                                                                                                                                                                           | Open         |               |   |                                           |   |                                                           |   |
| CLS         | I                                                         | VDDIO/<br>VSS                   | Clock Mode Selection         | CLS pin should be connected to VDDIO.                                                                                                                                                                                                                                                                                                   | -            |               |   |                                           |   |                                                           |   |
| BS1         | I                                                         | VDDIO/<br>VSS                   | MCU Interface Mode Selection | These pins are for selecting different bus interface.<br><br><div><b>Table 5-1 : MCU interface selection</b><table><tr><td>BS1</td><td>MPU Interface</td></tr><tr><td>L</td><td>4-lines serial peripheral interface (SPI)</td></tr><tr><td>H</td><td>3-lines serial peripheral interface (SPI)<br/>– 9 bits SPI</td></tr></table></div> | BS1          | MPU Interface | L | 4-lines serial peripheral interface (SPI) | H | 3-lines serial peripheral interface (SPI)<br>– 9 bits SPI | - |
| BS1         | MPU Interface                                             |                                 |                              |                                                                                                                                                                                                                                                                                                                                         |              |               |   |                                           |   |                                                           |   |
| L           | 4-lines serial peripheral interface (SPI)                 |                                 |                              |                                                                                                                                                                                                                                                                                                                                         |              |               |   |                                           |   |                                                           |   |
| H           | 3-lines serial peripheral interface (SPI)<br>– 9 bits SPI |                                 |                              |                                                                                                                                                                                                                                                                                                                                         |              |               |   |                                           |   |                                                           |   |
| Analog Pin  |                                                           |                                 |                              |                                                                                                                                                                                                                                                                                                                                         |              |               |   |                                           |   |                                                           |   |
| GDR         | O                                                         | POWER MOSFET Driver Control     | VGH & PREVGL Generation      | This pin is the N-Channel MOSFET Gate Drive Control.                                                                                                                                                                                                                                                                                    | -            |               |   |                                           |   |                                                           |   |
| RESE        | I                                                         | Booster Control Input           |                              | This pin is the Current Sense Input for the Control Loop.                                                                                                                                                                                                                                                                               | -            |               |   |                                           |   |                                                           |   |
| VGH         | C                                                         | Stabilizing capacitor           |                              | This pin is the Positive Gate driving voltage and the Power Supply pin for VSH.<br>A stabilizing capacitor should be connected between VGH and VSS.                                                                                                                                                                                     | -            |               |   |                                           |   |                                                           |   |
| PREVGL      | C                                                         | Stabilizing capacitor           |                              | This pin is the Power Supply pin for VGL and VSL.<br>A stabilizing capacitor should be connected between PREVGL and VSS.                                                                                                                                                                                                                | -            |               |   |                                           |   |                                                           |   |
| VGL         | C                                                         | Stabilizing capacitor           | VGL Generation               | This pin is the Negative Gate driving voltage.<br>A stabilizing capacitor should be connected between VGL and VSS.                                                                                                                                                                                                                      | -            |               |   |                                           |   |                                                           |   |
| VSH         | C                                                         | Stabilizing capacitor           | VSH, VSL Generation          | This pin is the Positive Source driving voltage.<br>A stabilizing capacitor should be connected between VSH and VSS.                                                                                                                                                                                                                    | -            |               |   |                                           |   |                                                           |   |
| VSL         | C                                                         | Stabilizing capacitor           |                              | This pin is the Negative Source driving voltage and the Power Supply pin for VCOM.<br>A stabilizing capacitor should be connected between VSL and VSS.                                                                                                                                                                                  | -            |               |   |                                           |   |                                                           |   |
| VCOM        | C                                                         | Panel/<br>Stabilizing capacitor | VCOM                         | This pin is the VCOM driving voltage<br>A stabilizing capacitor should be connected between VCOM and VSS.                                                                                                                                                                                                                               | -            |               |   |                                           |   |                                                           |   |



| Panel Driving                  |    |       |                       |                                                                                                                |       |
|--------------------------------|----|-------|-----------------------|----------------------------------------------------------------------------------------------------------------|-------|
| S [149:0]                      | O  | Panel | Source driving signal | Source output pin.                                                                                             | Open  |
| G [249:0]                      | O  | Panel | Gate driving signal   | Gate output pin.                                                                                               | Open  |
| VBD                            | O  | Panel | Border driving signal | Border output pin.                                                                                             | Open  |
| Panel Break Detection          |    |       |                       |                                                                                                                |       |
| TIN                            | I  | Panel | Panel Break Detection | TIN is the sensing pin for panel break detection. Connect to TPE through ITO.                                  | -     |
| TPE                            | O  | Panel |                       | TPE is the output pin for panel break detection. Connect to TIN through ITO.                                   | -     |
| Others                         |    |       |                       |                                                                                                                |       |
| NC                             | NC | NC    | Not Connected         | Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD, TPF, TOUT1, TIN1 and TIN2. | Open  |
| TPA, TPB, TPC, TPD, TPF, TOUT1 | NC | NC    | Reserved for Testing  | Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD, TPF, TOUT1, TIN1 and TIN2. | Open  |
| TIN1                           | I  | VDDIO | Reserved for Testing  | Connect to VDDIO.                                                                                              | VDDIO |
| TIN2                           | I  | VSS   | Reserved for Testing  | Connect to VSS.                                                                                                | VSS   |

## 6 FUNCTIONAL BLOCK DESCRIPTION

The device can drive an active matrix TFT EPD panel. It composes of 150 source outputs, 250 gate outputs, 1 VBD and 1 VCOM. It contains flexible built-in waveforms to drive the EPD panel.

### 6.1 MCU Interface

#### 6.1.1 MCU Interface selection

The SSD1673 can 3-wire/4-wire serial peripheral Interface. In the SSD1673, the MCU interface is pin selectable by BS1 pins shown in Table 6-2. .

**Table 6-1 : MCU interface selection by BS0 and BS1**

|     |                                                           |
|-----|-----------------------------------------------------------|
| BS1 | MPU Interface                                             |
| L   | 4-lines serial peripheral interface (SPI)                 |
| H   | 3-lines serial peripheral interface (SPI)<br>– 9 bits SPI |

The MCU interface consists of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6-2.

**Table 6-2 : MCU interface assignment under different bus interface mode**

| Pin Name      | Data/Command Interface |      | Control Signal |      |      |
|---------------|------------------------|------|----------------|------|------|
| Bus Interface | D1                     | D0   | CS#            | D/C# | RES# |
| SPI4          | SDin                   | SCLK | CS#            | D/C# | RES# |
| SPI3          | SDin                   | SCLK | CS#            | L    | RES# |

#### Note

- (1) L is connected to  $V_{SS}$
- (2) H is connected to  $V_{DDIO}$

### 6.1.2 MCU Serial Peripheral Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

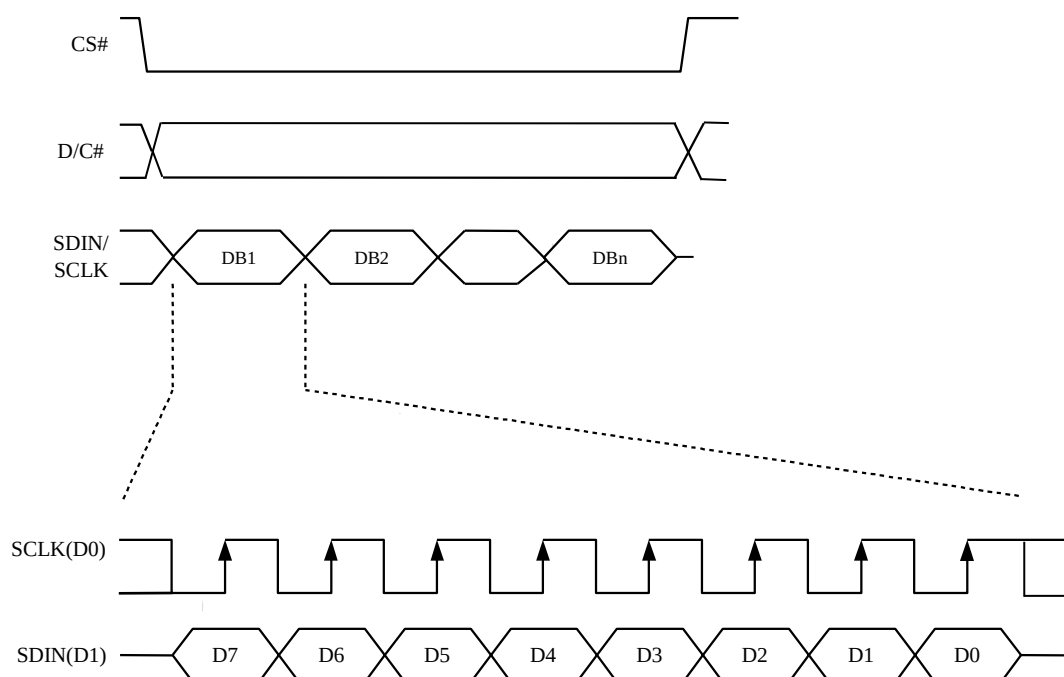
**Table 6-3 : Control pins of 4-wire Serial Peripheral interface**

| Function      | CS# | D/C# | SCLK |
|---------------|-----|------|------|
| Write command | L   | L    | ↑    |
| Write data    | L   | H    | ↑    |

**Note:** ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

**Figure 6-1 : Write procedure in 4-wire Serial Peripheral Interface mode**



### 6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

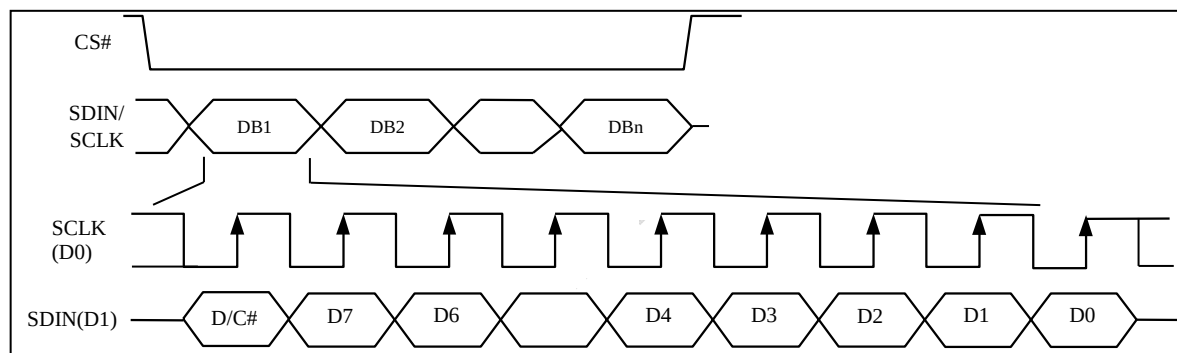
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 6-4 : Control pins of 3-wire Serial Peripheral interface

| Function      | E(RD#)  | R/W#(WR#) | CS# | D/C#    | SCLK |
|---------------|---------|-----------|-----|---------|------|
| Write command | Tie LOW | Tie LOW   | L   | Tie LOW | ↑    |
| Write data    | Tie LOW | Tie LOW   | L   | Tie LOW | ↑    |

**Note:** ↑ stands for rising edge of signal

Figure 6-2 : Write procedure in 3-wire Serial Peripheral Interface mode



## 6.2 RAM

The On chip display RAM is holding the image data. 1 set of RAM is built for historical data and the other set is built for the current image data. The size of each RAM is 150x250 bits.

Table 6-5 shows the RAM map under the following condition:

- Command "Data Entry Mode" R11h is set to:

|                                       |             |
|---------------------------------------|-------------|
| Address Counter update in X direction | AM=0        |
| X: Increment                          | ID[1:0] =11 |
| Y: Increment                          |             |

- Command "Driver Output Control" R01h is set to

|                                   |           |
|-----------------------------------|-----------|
| 250 Mux                           | MUX = F9h |
| Select G0 as 1 <sup>st</sup> gate | GD = 0    |
| Left and Right gate Interlaced    | SM = 0    |
| Scan From G0 to G249              | TB = 0    |

- Command "Gate Start Position" R0Fh is set to:

|                                     |       |
|-------------------------------------|-------|
| Set the Start Position of Gate = G0 | SCN=0 |
|-------------------------------------|-------|

- Data byte sequence: DB0, DB1, DB2 ... DB4749

**Table 6-5 : RAM address map**

|      |     | S0            | S1            | S2            | S3            | S4            | S5            | S6            | S7            | ... | ... | S144          | S145          | S146          | S147          | S148          | S149          | XX            | XX            |
|------|-----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|-----|-----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
|      |     | 00h           |               |               |               |               |               |               |               | ... |     | 12h           |               |               |               |               |               |               |               |
| G0   | 00h | DB0<br>[7]    | DB0<br>[6]    | DB0<br>[5]    | DB0<br>[4]    | DB0<br>[3]    | DB0<br>[2]    | DB0<br>[1]    | DB0<br>[0]    | ... | ... | DB18<br>[7]   | DB18<br>[6]   | DB18<br>[5]   | DB18<br>[4]   | DB18<br>[3]   | DB18<br>[2]   | DB18<br>[1]   | DB18<br>[0]   |
| G1   | 01h | DB19<br>[7]   | DB19<br>[6]   | DB19<br>[5]   | DB19<br>[4]   | DB19<br>[3]   | DB19<br>[2]   | DB19<br>[1]   | DB19<br>[0]   | ... | ... | DB36<br>[7]   | DB36<br>[6]   | DB36<br>[5]   | DB36<br>[4]   | DB36<br>[3]   | DB36<br>[2]   | DB36<br>[1]   | DB36<br>[0]   |
| ...  | ... | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ... | ... | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ...           |
| ...  | ... | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ... | ... | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ...           |
| ...  | ... | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ... | ... | ...           | ...           | ...           | ...           | ...           | ...           | ...           | ...           |
| G248 | F8h | DB4698<br>[7] | DB4698<br>[6] | DB4698<br>[5] | DB4698<br>[4] | DB4698<br>[3] | DB4698<br>[2] | DB4698<br>[1] | DB4698<br>[0] | ... | ... | DB4716<br>[7] | DB4716<br>[6] | DB4716<br>[5] | DB4716<br>[4] | DB4716<br>[3] | DB4716<br>[2] | DB4716<br>[1] | DB4716<br>[0] |
| G249 | F9h | DB4717<br>[7] | DB4717<br>[6] | DB4717<br>[5] | DB4717<br>[4] | DB4717<br>[3] | DB4717<br>[2] | DB4717<br>[1] | DB4717<br>[0] | ... | ... | DB4749<br>[7] | DB4749<br>[6] | DB4749<br>[5] | DB4749<br>[4] | DB4749<br>[3] | DB4749<br>[2] | DB4749<br>[1] | DB4749<br>[0] |

Source  
X-  
ADDR

GATE  
Y-ADDR

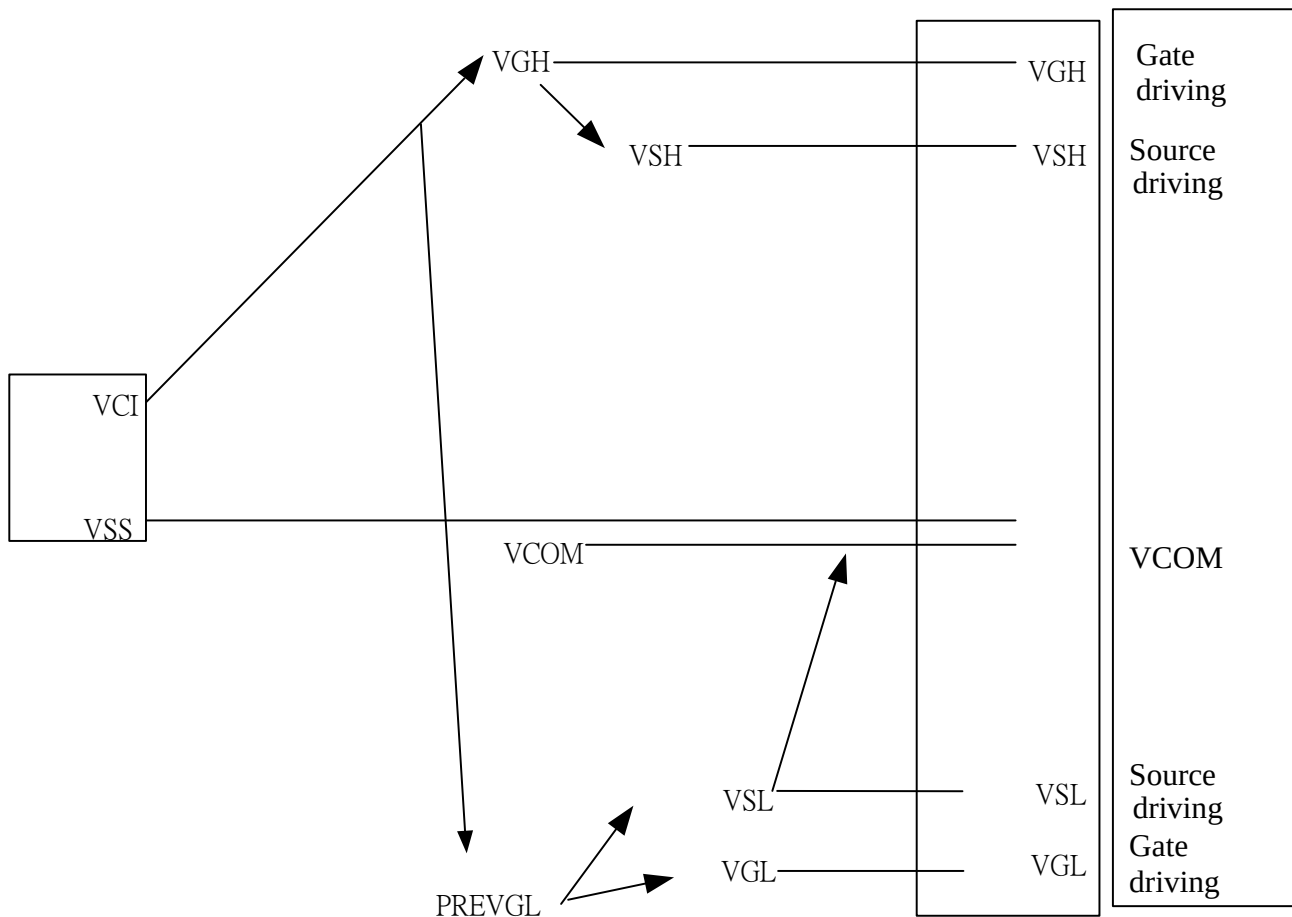
## 6.3 Oscillator

The on-chip oscillator is included for the use on waveform timing and Booster operations. In order to enable the internal oscillator, the CLS pin must be connected to VDDIO.

#### 6.4 Booster & Regulator

A voltage generation system is included in the SSD1673. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH, VSL and VCOM. Figure 6-3 shows the relation of the voltages. External application circuit is needed to make the on-chip booster & regulator circuit work properly.

Figure 6-3 : Input and output voltage relation chart

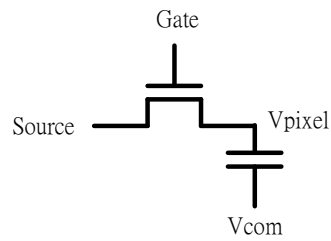


- Max voltage difference between VGH and VGL is 42V.

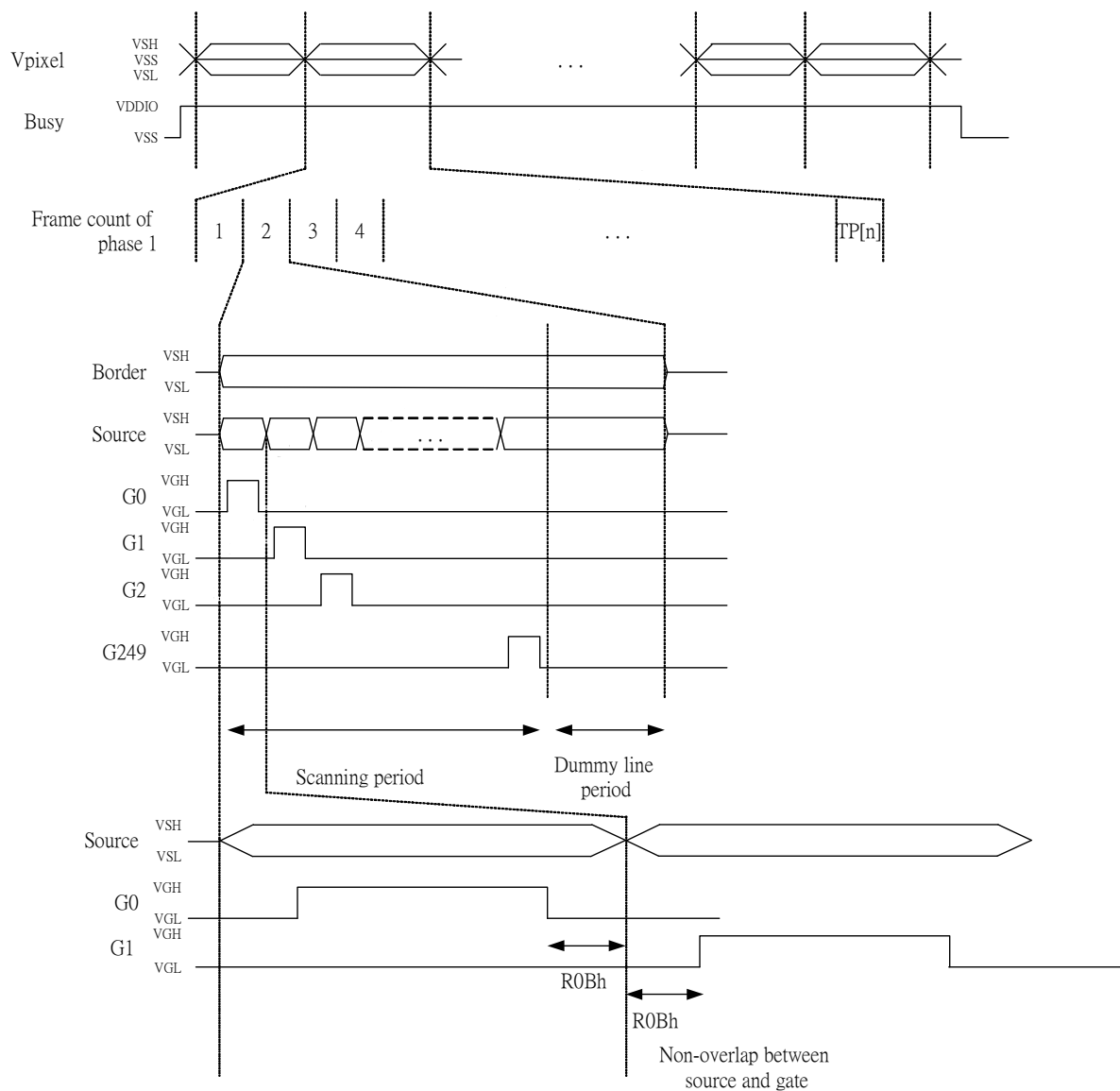
## 6.5 Panel Driving Waveform

The Vpixel is defined as Figure 6-4, and its relations with GATE, SOURCE are shown Figure 6-5.

**Figure 6-4 : Vpixel Definition**



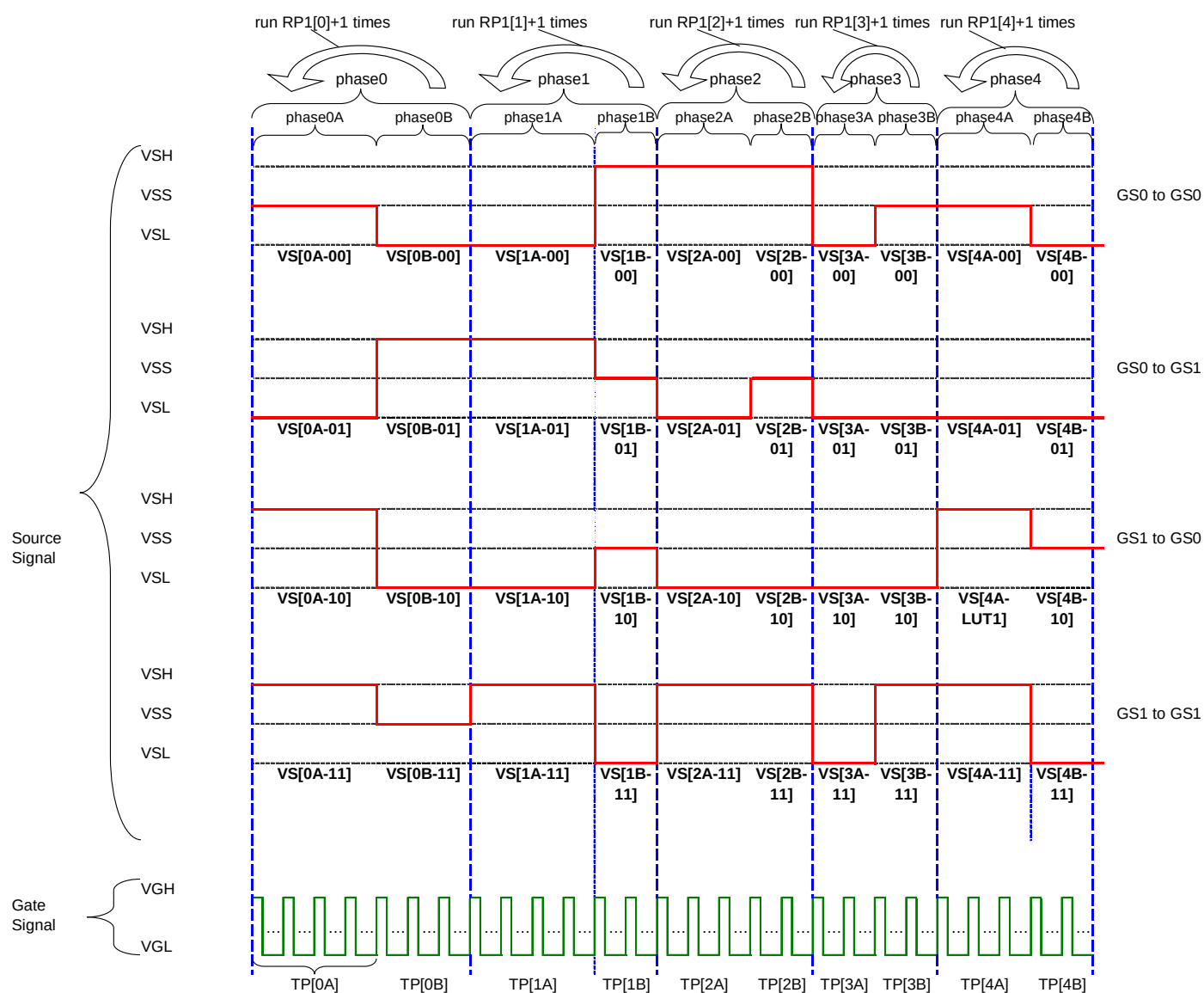
**Figure 6-5 : The Relation of Vpixel Waveform with Gate and Source**



## 6.6 Gate and Programmable Source waveform

Programmable Source waveform of different phase length would be made according to the format of Figure 6-6.

Figure 6-6 : Programmable Source and Gate waveform illustration



- There are totally 10 phases for programmable Source waveform of different phase length.
- The phase period defined as  $TP[n] * T_{FRAME}$ , where  $TP[n]$  range from 0 to 31.
- $TP[n] = 0$  indicates phase skipped
- Source Voltage Level:  $VS[n-XY]$  is constant in each phase
- The repeat counter defined as  $RP[n]$ , which represents repeating  $TP[nA]$  and  $TP[nB]$ 
  - $RP[n] = 0$  indicates run time =1, where  $RP[n]$  range from 0 to 63.
- $VS[n-XY]$  indicates the voltage in phase n for transition from GS X to GS Y
  - 00 – VSS
  - 01 – VSH
  - 10 – VSL
- $VS[n-XY]$  and  $TP[n]$  are stored in waveform lookup table register [LUT].



## 6.7 Waveform Look Up Table (LUT)

LUT contains 256 bits, which defines the display driving waveform settings. They are arranged in format shown in Figure 6-7.

Figure 6-7 : VS[n-XY] and TP[n] mapping in LUT

| in<br>Decimal | D7                    | D6         | D5         | D4                       | D3         | D2 | D1         | D0 |
|---------------|-----------------------|------------|------------|--------------------------|------------|----|------------|----|
| 0             | VS[0A-11]             |            | VS[0A-10]  |                          | VS[0A-01]  |    | VS[0A-00]  |    |
| 1             | VS[0B-11]             |            | VS[0B -10] |                          | VS[0B -01] |    | VS[0B-00]  |    |
| 2             | VS[1A-11]             |            | VS[1A -10] |                          | VS[1A -01] |    | VS[1A -00] |    |
| ...           | ...                   |            | ...        |                          | ...        |    | ...        |    |
| 7             | VS[3A-11]             |            | VS[3A -10] |                          | VS[3A -01] |    | VS[3A -00] |    |
| 8             | VS[4A -11]            |            | VS[4A -10] |                          | VS[4A -01] |    | VS[4A -00] |    |
| 9             | VS[4B -11]            |            | VS[4B -10] |                          | VS[4B -01] |    | VS[4B -00] |    |
| 10            | 0x00                  |            |            |                          |            |    |            |    |
| 11            | 0x00                  |            |            |                          |            |    |            |    |
| 12            | 0x00                  |            |            |                          |            |    |            |    |
| 13            | 0x00                  |            |            |                          |            |    |            |    |
| 14            | 0x00                  |            |            |                          |            |    |            |    |
| 15            | 0x00                  |            |            |                          |            |    |            |    |
| 16            | RP[0] [2:0] Low bits  |            |            | TP[0A]                   |            |    |            |    |
| 17            | RP[0] [5:3] High bits |            |            | TP[0B]                   |            |    |            |    |
| 18            | RP[1] [2:0] Low bits  |            |            | TP[1A]                   |            |    |            |    |
| 19            | RP[1] [5:3] High bits |            |            | TP[1B]                   |            |    |            |    |
| 20            | RP[2] [2:0] Low bits  |            |            | TP[2A]                   |            |    |            |    |
| 21            | RP[2] [5:3] High bits |            |            | TP[2B]                   |            |    |            |    |
| 22            | RP[3] [2:0] Low bits  |            |            | TP[3A]                   |            |    |            |    |
| 23            | RP[3] [5:3] High bits |            |            | TP[3B]                   |            |    |            |    |
| 24            | RP[4] [2:0] Low bits  |            |            | TP[4A]                   |            |    |            |    |
| 25            | RP[4] [5:3] High bits |            |            | TP[4B]                   |            |    |            |    |
| 26            | 0x00                  |            |            |                          |            |    |            |    |
| 27            | 0x00                  |            |            |                          |            |    |            |    |
| 28            | 0x00                  |            |            |                          |            |    |            |    |
| 29            |                       | R3A_A[6:0] |            |                          |            |    |            |    |
| 30            |                       |            |            | R04_A[4:0] - VSH Setting |            |    |            |    |
| 31            | DUMMY                 |            |            |                          | R3B_A[3:0] |    |            |    |

## 6.8 OTP

The OTP is the non-volatile memory and is used to store the information of OTP Selection Option, VCOM value, 7 sets of WAVEFORM SETTING (WS) [256bits x 7] and 6 sets of TEMPERATURE RANGE (TR) [24bits x 6].

The OTP is the non-volatile memory and stored the information of:

- OTP Selection Option
- VCOM value
- Source value
- 7 set of WAVEFORM SETTING (WS) [256bits x 7]
- 6set of TEMPERATURE RANGE (TR) [24bits x 6]

For Programming the WS and TR, Write RAM is required, and the configurations should be

|                                      |                     |                                                                                                                       |
|--------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------|
| Command: Data Entry mode             | C11,<br>D03         | Set Address automatic increment setting =<br>X increment and Y increment<br>Set Address counter update in X direction |
| Command: X RAM address<br>start /end | C44,<br>D00,<br>D12 | Set RAM Address for S0 to S149                                                                                        |
| Command: Y RAM address<br>start /end | C45,<br>D00,<br>DF9 | Set RAM Address for G0 to G249                                                                                        |
| Command: RAM X address<br>counter    | C4E,<br>D00         | Set RAM X AC as 0                                                                                                     |
| Command: RAM Y address<br>counter    | C4F,<br>D00         | Set RAM Y AC as 0                                                                                                     |

The mapping table of OTP is shown in below figure,

**Figure 6-8 : OTP Content and Address Mapping**

| Default | SPARE   | WRITE RAM |    | D7                   | D6 | D5        | D4 | D3                       | D2 | D1        | D0 |
|---------|---------|-----------|----|----------------------|----|-----------|----|--------------------------|----|-----------|----|
| OTP     | OTP     | ADDRESS   |    |                      |    |           |    |                          |    |           |    |
| ADDRESS | ADDRESS | X         | Y  |                      |    |           |    |                          |    |           |    |
| 0       | 256     | 0         | 0  | VS[0A-11]            |    | VS[0A-10] |    | VS[0A-01]                |    | VS[0A-00] |    |
| 1       | 257     | 1         | 0  | VS[0B-11]            |    | VS[0B-10] |    | VS[0B-01]                |    | VS[0B-00] |    |
| 2       | 258     | 0         | 0  | VS[1A-11]            |    | VS[1A-10] |    | VS[1A-01]                |    | VS[1A-00] |    |
| 3       | 259     | 3         | 0  | VS[1B-11]            |    | VS[1B-10] |    | VS[1B-01]                |    | VS[1B-00] |    |
| 4       | 260     | 4         | 0  | VS[2A-11]            |    | VS[2A-10] |    | VS[2A-01]                |    | VS[2A-00] |    |
| 5       | 261     | 5         | 0  | VS[2B-11]            |    | VS[2B-10] |    | VS[2B-01]                |    | VS[2B-00] |    |
| 6       | 262     | 6         | 0  | VS[3A-11]            |    | VS[3A-10] |    | VS[3A-01]                |    | VS[3A-00] |    |
| 7       | 263     | 7         | 0  | VS[3B-11]            |    | VS[3B-10] |    | VS[3B-01]                |    | VS[3B-00] |    |
| 8       | 264     | 8         | 0  | VS[4A-11]            |    | VS[4A-10] |    | VS[4A-01]                |    | VS[4A-00] |    |
| 9       | 265     | 9         | 0  | VS[4B-11]            |    | VS[4B-10] |    | VS[4B-01]                |    | VS[4B-00] |    |
| 10      | 266     | 10        | 0  | 0x00                 |    |           |    |                          |    |           |    |
| 11      | 267     | 11        | 0  | 0x00                 |    |           |    |                          |    |           |    |
| 12      | 268     | 12        | 0  | 0x00                 |    |           |    |                          |    |           |    |
| 13      | 269     | 13        | 0  | 0x00                 |    |           |    |                          |    |           |    |
| 14      | 270     | 14        | 0  | 0x00                 |    |           |    |                          |    |           |    |
| 15      | 271     | 15        | 0  | 0x00                 |    |           |    |                          |    |           |    |
| 16      | 272     | 16        | 0  | RP[0][2:0] Low bits  |    |           |    | TP[0A]                   |    |           |    |
| 17      | 273     | 17        | 0  | RP[0][5:3] High bits |    |           |    | TP[0B]                   |    |           |    |
| 18      | 274     | 18        | 0  | RP_TP[1]             |    |           |    |                          |    |           |    |
| 19      | 275     | 0         | 1  |                      |    |           |    |                          |    |           |    |
| 20      | 276     | 1         | 1  |                      |    |           |    |                          |    |           |    |
| 21      | 277     | 2         | 1  |                      |    |           |    |                          |    |           |    |
| 22      | 278     | 3         | 1  |                      |    |           |    |                          |    |           |    |
| 23      | 279     | 4         | 1  | RP_TP[3]             |    |           |    |                          |    |           |    |
| 24      | 280     | 5         | 1  |                      |    |           |    |                          |    |           |    |
| 25      | 281     | 6         | 1  |                      |    |           |    |                          |    |           |    |
| 26      | 282     | 7         | 1  |                      |    |           |    |                          |    |           |    |
| 27      | 283     | 8         | 1  |                      |    |           |    |                          |    |           |    |
| 28      | 284     | 9         | 1  | 0x00                 |    |           |    |                          |    |           |    |
| 29      | 285     | 10        | 1  | 0x00                 |    |           |    |                          |    |           |    |
| 30      | 286     | 11        | 1  | 0x00                 |    |           |    |                          |    |           |    |
| 31      | 287     | 12        | 1  | DUMMY                |    |           |    | R3A_A[6:0]               |    |           |    |
| 32      | 288     | 13        | 1  |                      |    |           |    | R04_A[4:0] - VSH Setting |    |           |    |
|         |         |           |    |                      |    |           |    | R3B_A[3:0]               |    |           |    |
|         |         |           |    | WS[1]                |    |           |    |                          |    |           |    |
| 63      | 319     | 6         | 3  |                      |    |           |    |                          |    |           |    |
|         |         |           |    | ...                  |    |           |    |                          |    |           |    |
| 192     | 448     | 2         | 10 | WS[6]                |    |           |    |                          |    |           |    |
|         |         |           |    |                      |    |           |    |                          |    |           |    |
| 223     | 479     | 14        | 11 |                      |    |           |    |                          |    |           |    |
| 224     | 480     | 15        | 11 | TEMP[1L][11:0]       |    |           |    |                          |    |           |    |
| 225     | 481     | 16        | 11 |                      |    |           |    |                          |    |           |    |
| 226     | 482     | 17        | 11 | TEMP[1-H][11:0]      |    |           |    |                          |    |           |    |
| 227     | 483     | 18        | 11 | TEMP[2L][11:0]       |    |           |    |                          |    |           |    |
| 228     | 484     | 0         | 12 |                      |    |           |    |                          |    |           |    |
| 229     | 485     | 1         | 12 | TEMP[2-H][11:0]      |    |           |    |                          |    |           |    |
|         |         |           |    | ...                  |    |           |    |                          |    |           |    |
| 236     | 492     | 8         | 12 | TEMP[5L][11:0]       |    |           |    |                          |    |           |    |
| 237     | 493     | 9         | 12 |                      |    |           |    |                          |    |           |    |
| 238     | 494     | 10        | 12 | TEMP[5-H][11:0]      |    |           |    |                          |    |           |    |
| 239     | 495     | 11        | 12 | TEMP[6L][11:0]       |    |           |    |                          |    |           |    |
| 240     | 496     | 12        | 12 |                      |    |           |    |                          |    |           |    |
| 241     | 497     | 13        | 12 | TEMP[6-H][11:0]      |    |           |    |                          |    |           |    |
| 242     | 498     | 14        | 12 | DUMMY                |    |           |    |                          |    |           |    |
| 243     | 499     | 15        | 12 | DUMMY                |    |           |    |                          |    |           |    |
| 244     | 500     | 16        | 12 | DUMMY                |    |           |    |                          |    |           |    |
| 245     | 501     | 17        | 12 | DUMMY                |    |           |    |                          |    |           |    |

Remark:

- WS [m] means the waveform setting of temperature set m, the configuration are same as the definition in LUT. The corresponding low temperature range of WS[m] defined as TEMP [m-L] and high range defined as TEMP [m-H]
- Load WS [m] from OTP for LUT if Temp [m-L] < Temperature Register <= Temp [m-H]

## 6.9 Temperature Searching Mechanism

Legend:

|                      |                                                                                  |
|----------------------|----------------------------------------------------------------------------------|
| WS#                  | Waveform Setting no. #                                                           |
| TR#                  | Temperature Range no. #                                                          |
| LUT                  | 720 bit register storing the waveform setting (volatile)                         |
| Temperature register | 12bit Register storing (volatile)                                                |
| OTP                  | A non-volatile storing 7 sets of waveform setting and 6 set of temperature range |
| WS_sel_address       | an address pointer indicating the selected WS#                                   |

Figure 6-9 : Waveform Setting and Temperature Range # mapping

| OTP (non-volatile) |     |
|--------------------|-----|
| WS0                |     |
| WS1                | TR1 |
| WS2                | TR2 |
| WS3                | TR3 |
| WS4                | TR4 |
| WS5                | TR5 |
| WS6                | TR6 |

| IC implementation requirement |                                                                                                                                                                                                |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                             | Default selection is <b>WS0</b> .                                                                                                                                                              |
| 2                             | Compare temperature register from <b>TR1 to TR6</b> , in sequence. <b>The last match will be recorded.</b><br>i.e. If the temperature register fall in both TR3 and TR5. WS5 will be selected. |
| 3                             | If none of the range TR1 to TR6 is match, WS0 will be selected.                                                                                                                                |
| User application              |                                                                                                                                                                                                |
| 1                             | The default waveform should be programmed as WS0.                                                                                                                                              |
| 2                             | There is no restriction on the sequence of TR1, TR2.... TR6.                                                                                                                                   |

## 6.10 Temperature Register Mapping

1. If the Temperature value MSByte bit D11 = 0, then

The temperature is positive and value (DegC) = + (Temperature value) / 16

2. If the Temperature value MSByte bit D11 = 1, then

The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

| 12-bit binary<br>(2's complement) | Hexadecimal<br>Value | Decimal<br>Value | Value<br>[DegC] |
|-----------------------------------|----------------------|------------------|-----------------|
| 0111 1111 0000                    | 7F0                  | 2032             | 127             |
| 0111 1110 1110                    | 7EE                  | 2030             | 126.875         |
| 0111 1110 0010                    | 7E2                  | 2018             | 126.125         |
| 0111 1101 0000                    | 7D0                  | 2000             | 125             |
| 0001 1001 0000                    | 190                  | 400              | 25              |
| 0000 0000 0010                    | 002                  | 2                | 0.125           |
| 0000 0000 0000                    | 000                  | 0                | 0               |
| 1111 1111 1110                    | FFE                  | -2               | -0.125          |
| 1110 0111 0000                    | E70                  | -400             | -25             |
| 1100 1001 0010                    | C92                  | -878             | -54.875         |
| 1100 1001 0000                    | C90                  | -880             | -55             |

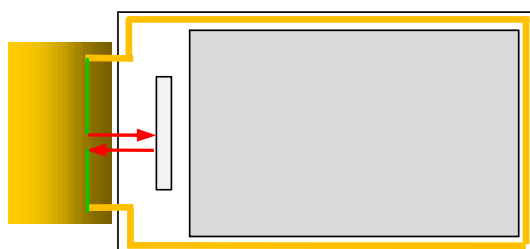
## 6.11 Panel Break Detection

The panel break detection function is used to detect the breakage at panel edge.

Two I/O pins TIN and TPE are used for this function. TIN pin is the sensing pin and TPE pin is the output pin for the panel break detection function. In order to use the panel break detection function, there must have an ITO trace routed around the panel edge. For this ITO trace, one point is connecting to pin TIN and another point is connecting to pin TPE through the FPC. Figure 6-10 shows the ITO routing on panel using the panel break detection function.

In the SSD1673, there is a command to execute the panel break detection function. When the panel break detection command is issued, the panel break detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of panel break.

Figure 6-10 : Panel ITO routing example for panel break detection



## 7 COMMAND TABLE

Table 7-1: Command Table

| Command Table |   |    |                |                |                |                |                |                |                |                | Command                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------|---|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0             | 0 | 01 | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 1              | Driver Output control          | Gate setting<br>A[7:0]: MUX Gate lines setting as (A[7:0] + 1)<br>POR = F9h + 1 MUX<br><br>B[2:0]: Gate scanning sequence and direction<br><br>B[2]: GD<br>Selects the 1st output Gate<br>GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ...<br>GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3,<br><br>B[1]: SM<br>Change scanning order of gate driver.<br>SM=0 [POR], G0, G1, G2, G3...G249 (left and right gate interlaced)<br>SM=1, G0, G2, G4 ...G248, G1, G3, ...G249<br><br>B[0]: TB<br>TB = 0 [POR], scan from G0 to G249<br>TB = 1, scan from G249 to G0. |
| 0             | 1 |    | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 0             | 1 |    | 0              | 0              | 0              | 0              | 0              | B <sub>2</sub> | B <sub>1</sub> | B <sub>0</sub> |                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 0             | 0 | 03 | 0              | 0              | 0              | 0              | 0              | 0              | 1              | 1              | Gate Driving voltage Control   | Set Gate related driving voltage<br><br>A[4:0] = 10h [POR], VGH at 22V<br>B[3:0] = 0Ah [POR], VGL at -20V                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 0             | 1 |    | 0              | 0              | 0              | A              | A              | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 0             | 1 |    | 0              | 0              | 0              | 0              | B              | B <sub>2</sub> | B <sub>1</sub> | B <sub>0</sub> |                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 0             | 0 | 04 | 0              | 0              | 0              | 0              | 0              | 1              | 0              | 0              | Source Driving voltage Control | Set Source output voltage magnitude<br><br>A[4:0] = 19h [POR], VSH/VSL at +/-15V                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0             | 1 |    | 0              | 0              | 0              | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

| Command Table |                       |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
|---------------|-----------------------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|---|-------------------|---|-----------------------|
| R/W#          | D/C#                  | Hex | D7             | D6             | D5             | D4             | D3             | D2             | D1             | D0             | Command                                                    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |        |             |   |                   |   |                       |
| 0             | 0                     | 10  | 0              | 0              | 0              | 1              | 0              | 0              | 0              | 0              | Deep Sleep mode                                            | Deep Sleep mode Control                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |        |             |   |                   |   |                       |
| 0             | 1                     |     | 0              | 0              | 0              | 0              | 0              | 0              | 0              | A <sub>0</sub> |                                                            | <table><tr><td>A[0] :</td><td>Description</td></tr><tr><td>0</td><td>Normal Mode [POR]</td></tr><tr><td>1</td><td>Enter Deep Sleep Mode</td></tr></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | A[0] : | Description | 0 | Normal Mode [POR] | 1 | Enter Deep Sleep Mode |
| A[0] :        | Description           |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
| 0             | Normal Mode [POR]     |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
| 1             | Enter Deep Sleep Mode |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
|               |                       |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
|               |                       |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
| 0             | 0                     | 11  | 0              | 0              | 0              | 1              | 0              | 0              | 0              | 1              | Data Entry mode setting                                    | Define data entry sequence                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |        |             |   |                   |   |                       |
| 0             | 1                     |     | 0              | 0              | 0              | 0              | 0              | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                                            | A [1:0] = ID[1:0]<br>Address automatic increment / decrement setting<br>The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.<br><br>00 –Y decrement, X decrement,<br>01 –Y decrement, X increment,<br>10 –Y increment, X decrement,<br>11 –Y increment, X increment [POR]<br><br>A[2] = AM<br>Set the direction in which the address counter is updated automatically after data are written to the RAM.<br><br>AM= 0, the address counter is updated in the X direction. [POR]<br>AM = 1, the address counter is updated in the Y direction. |        |             |   |                   |   |                       |
|               |                       |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
|               |                       |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
| 0             | 0                     | 12  | 0              | 0              | 0              | 1              | 0              | 0              | 1              | 0              | SWRESET                                                    | It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode<br>Note: RAM are unaffected by this command.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |        |             |   |                   |   |                       |
|               |                       |     |                |                |                |                |                |                |                |                |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |
| 0             | 0                     | 1A  | 0              | 0              | 0              | 1              | 1              | 0              | 1              | 0              | Temperature Sensor Control (Write to temperature register) | Write to temperature register.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |        |             |   |                   |   |                       |
| 0             | 1                     |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                                            | A[7:0] – MSByte 01111111[POR]<br>B[7:0] – LSByte 11110000[POR]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |        |             |   |                   |   |                       |
| 0             | 1                     |     | B <sub>7</sub> | B <sub>6</sub> | B <sub>5</sub> | B <sub>4</sub> | 0              | 0              | 0              | 0              |                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |             |   |                   |   |                       |

| Command Table |      |     |                |                |                |                |                |                |                |                |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
|---------------|------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|-----|----|-----|-----|----------|-----|-----|----|-----|-----|----|-----|-----|
| R/W#          | D/C# | Hex | D7             | D6             | D5             | D4             | D3             | D2             | D1             | D0             | Command                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 0    | 20  | 0              | 0              | 1              | 0              | 0              | 0              | 0              | 0              | Master Activation      | Activate Display Update Sequence<br><br>The Display Update Sequence Option is located at R22h<br><br>User should not interrupt this operation to avoid corruption of panel images.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 0    | 21  | 0              | 0              | 1              | 0              | 0              | 0              | 0              | 1              | Display Update Control | Option for Display Update                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 1    |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | 1                      | Bypass Option used for Pattern Display, which is used for display the RAM content into the Display<br><br>OLD RAM Bypass option<br>A [7]<br>A[7] = 1: Enable bypass<br>A[7] = 0: Disable bypass [POR]<br><br>NEW RAM Bypass option<br><br>A[6] = 1: Enable bypass<br>A[6] = 0: Disable bypass [POR]<br><br>A[5] value will be used as Old RAM for bypass.<br>A[5] = 0 [POR]<br><br>A[4] value will be used as New RAM for bypass.<br>A[4] = 0 [POR]<br><br>A[3]: the inverse option for OLD RAM<br>A[3] = 1: Enable inverse<br>A[3] = 0: Disable inverse [POR]<br><br>A[2]: the inverse option for NEW RAM<br>A[2] = 1: Enable inverse<br>A[2] = 0: Disable inverse [POR]<br><br>A[1:0] Initial Update Option - Source Control<br><table><tr><td>A[1:0]</td><td>GSC</td><td>GSD</td></tr><tr><td>00</td><td>GS0</td><td>GS0</td></tr><tr><td>01 [POR]</td><td>GS0</td><td>GS1</td></tr><tr><td>10</td><td>GS1</td><td>GS0</td></tr><tr><td>11</td><td>GS1</td><td>GS1</td></tr></table> | A[1:0] | GSC | GSD | 00 | GS0 | GS0 | 01 [POR] | GS0 | GS1 | 10 | GS1 | GS0 | 11 | GS1 | GS1 |
| A[1:0]        | GSC  | GSD |                |                |                |                |                |                |                |                |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 00            | GS0  | GS0 |                |                |                |                |                |                |                |                |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 01 [POR]      | GS0  | GS1 |                |                |                |                |                |                |                |                |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 10            | GS1  | GS0 |                |                |                |                |                |                |                |                |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 11            | GS1  | GS1 |                |                |                |                |                |                |                |                |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |



| Command Table |      |     |                |                |                |                |                |                |                |                |                          |                                                                                                                                                                                  |                                                                                                                                     |
|---------------|------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| R/W#          | D/C# | Hex | D7             | D6             | D5             | D4             | D3             | D2             | D1             | D0             | Command                  | Description                                                                                                                                                                      |                                                                                                                                     |
| 0             | 0    | 22  | 0              | 0              | 1              | 0              | 0              | 0              | 1              | 0              | Display Update Control 2 | Display Update Sequence Option:<br>Enable the stage for Master Activation                                                                                                        |                                                                                                                                     |
| 0             | 1    |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                          |                                                                                                                                                                                  | Parameter<br>(in Hex)                                                                                                               |
|               |      |     |                |                |                |                |                |                |                |                |                          | Enable Clock Signal,<br>Then Enable CP<br>Then Load Temperature value<br>Then Load LUT<br>Then INITIAL DISPLAY<br>Then PATTERN DISPLAY<br>Then Disable CP<br>Then Disable OSC    | FF<br>[POR]                                                                                                                         |
|               |      |     |                |                |                |                |                |                |                |                |                          | Enable Clock Signal,<br>Then Enable CP<br>Then Load Temperature value<br>Then Load LUT<br>Then PATTERN DISPLAY<br>Then Disable CP<br>Then Disable OSC                            | F7                                                                                                                                  |
|               |      |     |                |                |                |                |                |                |                |                |                          | To Enable Clock Signal<br>(CLKEN=1)                                                                                                                                              | 80                                                                                                                                  |
|               |      |     |                |                |                |                |                |                |                |                |                          | To Enable Clock Signal,<br>then Enable CP<br>(CLKEN=1, CPEN=1)                                                                                                                   | C0                                                                                                                                  |
|               |      |     |                |                |                |                |                |                |                |                |                          | To INITIAL DISPLAY + PATTEN<br>DISPLAY                                                                                                                                           | 0C                                                                                                                                  |
|               |      |     |                |                |                |                |                |                |                |                |                          | To INITIAL DISPLAY                                                                                                                                                               | 08                                                                                                                                  |
|               |      |     |                |                |                |                |                |                |                |                |                          | To DISPLAY PATTEN                                                                                                                                                                | 04                                                                                                                                  |
|               |      |     |                |                |                |                |                |                |                |                |                          | To Disable CP,<br>then Disable Clock Signal<br>(CLKEN=1, CPEN=1)                                                                                                                 | 03                                                                                                                                  |
|               |      |     |                |                |                |                |                |                |                |                |                          | To Disable Clock Signal<br>(CLKEN=1)                                                                                                                                             | 01                                                                                                                                  |
|               |      |     |                |                |                |                |                |                |                |                |                          | Remark:<br>CLKEN=1:<br>If CLS=VDDIO then Enable OSC<br>If CLS=VSS then Enable External Clock<br>CLKEN=0:<br>If CLS=VDDIO then Disable OSC<br>AND<br>INTERNAL CLOCK Signal = VSS, |                                                                                                                                     |
|               |      |     |                |                |                |                |                |                |                |                |                          |                                                                                                                                                                                  |                                                                                                                                     |
| 0             | 0    | 23  | 0              | 0              | 1              | 0              | 0              | 0              | 1              | 1              |                          | Panel Break Detection                                                                                                                                                            | After this command, panel break detection starts. During detection, BUSY pad will output high.<br><br>The command required CLKEN=1. |
|               |      |     |                |                |                |                |                |                |                |                |                          |                                                                                                                                                                                  |                                                                                                                                     |
| 0             | 0    | 24  | 0              | 0              | 1              | 0              | 0              | 1              | 0              | 0              | Write RAM                | After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.                                       |                                                                                                                                     |
|               |      |     |                |                |                |                |                |                |                |                |                          |                                                                                                                                                                                  |                                                                                                                                     |

| Command Table |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
|---------------|----------------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------|------|-------------|--------|--------------|------|-----------|
| R/W#          | D/C#           | Hex | D7             | D6             | D5             | D4             | D3             | D2             | D1             | D0             | Command               | Description                                                                                                                                                                                                                                                                                           |        |                |      |             |        |              |      |           |
| 0             | 0              | 28  | 0              | 0              | 1              | 0              | 1              | 0              | 0              | 0              | VCOM Sense            | Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value.<br>The sensed VCOM voltage is stored in register<br>The command required CLKEN=1.                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 0              | 29  | 0              | 0              | 1              | 0              | 1              | 0              | 0              | 1              | VCOM Sense Duration   | Stabling time between entering VCOM sensing mode and reading acquired.<br>VCOM sense duration = Setting + 1 Seconds<br><br>A[3:0] = 09h [POR], duration = 10s                                                                                                                                         |        |                |      |             |        |              |      |           |
| 0             | 1              |     | 0              | 0              | 0              | 0              | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 0              | 2C  | 0              | 0              | 1              | 0              | 1              | 0              | 1              | 1              | Write VCOM register   | Write VCOM register from MCU interface                                                                                                                                                                                                                                                                |        |                |      |             |        |              |      |           |
| 0             | 1              |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 0              | 2F  | 0              | 0              | 1              | 0              | 1              | 0              | 0              | 1              | Status Bit Read       | A[3]: Panel-Break flag (POR=0)<br>0: Normal<br>1: Broken<br><br>A[1:0]: Chip ID (POR=01)                                                                                                                                                                                                              |        |                |      |             |        |              |      |           |
| 1             | 1              |     | 0              | 0              | 0              | 0              | A <sub>3</sub> | 0              | A <sub>1</sub> | A <sub>0</sub> |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 0              | 30  | 0              | 0              | 1              | 1              | 0              | 0              | 0              | 0              | Program WS OTP        | Program OTP of Waveform Setting<br>The contents should be written into RAM before sending this command.                                                                                                                                                                                               |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 0              | 32  | 0              | 0              | 1              | 1              | 0              | 0              | 1              | 0              | Write LUT register    | Write LUT register from MCU interface [30 bytes]<br>(excluding the VSH/VSL and Dummy bit)                                                                                                                                                                                                             |        |                |      |             |        |              |      |           |
| 0             | 1              |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 1              |     | B <sub>7</sub> | B <sub>6</sub> | B <sub>5</sub> | B <sub>4</sub> | B <sub>3</sub> | B <sub>2</sub> | B <sub>1</sub> | B <sub>0</sub> |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 1              |     | :              | :              | :              | :              | :              | :              | :              | :              |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 1              |     | .              | ..             | .              | .              | .              | .              | .              | .              |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 0              | 36  | 0              | 0              | 1              | 1              | 0              | 1              | 1              | 0              | Program OTP selection | Program OTP Selection according to the OTP Selection Control [R37h]                                                                                                                                                                                                                                   |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 0              | 37  | 0              | 0              | 1              | 1              | 0              | 1              | 1              | 1              | OTP selection Control | Write the OTP Selection:<br><table><tr><td>A[7]=1</td><td>spare VCOM OTP</td></tr><tr><td>A[6]</td><td>VCOM_Status</td></tr><tr><td>A[5]=1</td><td>spare WS OTP</td></tr><tr><td>A[4]</td><td>WS_Status</td></tr></table><br>A[3:0] are reserved OTP bit. User can treat the bits as Version Control. | A[7]=1 | spare VCOM OTP | A[6] | VCOM_Status | A[5]=1 | spare WS OTP | A[4] | WS_Status |
| A[7]=1        | spare VCOM OTP |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| A[6]          | VCOM_Status    |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| A[5]=1        | spare WS OTP   |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| A[4]          | WS_Status      |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
| 0             | 1              |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |
|               |                |     |                |                |                |                |                |                |                |                |                       |                                                                                                                                                                                                                                                                                                       |        |                |      |             |        |              |      |           |

| Command Table |            |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
|---------------|------------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------|------|----------|----|-----|----|-----|---------|-----|--------|-----|-----|----|-----|-----|----------|-----|-----|----|-----|-----|----|-----|-----|
| R/W#          | D/C#       | Hex | D7             | D6             | D5             | D4             | D3             | D2             | D1             | D0             | Command                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 0          | 3A  | 0              | 0              | 1              | 1              | 1              | 0              | 1              | 0              | Set dummy line period   | Set number of dummy line period                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 1          |     | 0              | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                         | A[6:0]: Number of dummy line period in term of TGate<br>A[6:0] = 06h [POR]<br><br>Available setting 0 to 127.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
|               |            |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 0          | 3B  | 0              | 0              | 1              | 1              | 1              | 0              | 1              | 1              | Set Gate line width     | Set Gate line width (TGate)<br>A[3:0] Line width in us                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 1          |     | 0              | 0              | 0              | 0              | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                         | <table><tr><td>A[3:0]</td><td>TGate / us</td></tr><tr><td>1011</td><td>78 [POR]</td></tr></table><br>Remark: Default value will give 50Hz Frame frequency under 6 dummy line pulse setting.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | A[3:0] | TGate / us | 1011 | 78 [POR] |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| A[3:0]        | TGate / us |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 1011          | 78 [POR]   |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
|               |            |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 0          | 3C  | 0              | 0              | 1              | 1              | 1              | 1              | 0              | 0              | Border Waveform Control | Select border waveform for VBD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 0             | 1          |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | 0              | 0              | A <sub>1</sub> | A <sub>0</sub> |                         | A [7] Follow Source at Initial Update Display<br>A [7]=0: [POR]<br>A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE.<br><br>A [6] Select GS Transition/ Fix Level for VBD<br>A [6]=0: Select GS Transition A[3:0] for VBD<br>A [6]=1: Select FIX level Setting A[5:4] [POR]<br><br>A [5:4] Fix Level Setting for VBD<br><table><tr><td>A[5:4]</td><td>VBD level</td></tr><tr><td>00</td><td>VSS</td></tr><tr><td>01</td><td>VSH</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11[POR]</td><td>HiZ</td></tr></table><br>A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0])<br><table><tr><td>A[1:0]</td><td>GSA</td><td>GSB</td></tr><tr><td>00</td><td>GS0</td><td>GS0</td></tr><tr><td>01 [POR]</td><td>GS0</td><td>GS1</td></tr><tr><td>10</td><td>GS1</td><td>GS0</td></tr><tr><td>11</td><td>GS1</td><td>GS1</td></tr></table> | A[5:4] | VBD level  | 00   | VSS      | 01 | VSH | 10 | VSL | 11[POR] | HiZ | A[1:0] | GSA | GSB | 00 | GS0 | GS0 | 01 [POR] | GS0 | GS1 | 10 | GS1 | GS0 | 11 | GS1 | GS1 |
| A[5:4]        | VBD level  |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 00            | VSS        |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 01            | VSH        |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 10            | VSL        |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 11[POR]       | HiZ        |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| A[1:0]        | GSA        | GSB |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 00            | GS0        | GS0 |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 01 [POR]      | GS0        | GS1 |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 10            | GS1        | GS0 |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
| 11            | GS1        | GS1 |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |
|               |            |     |                |                |                |                |                |                |                |                |                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |      |          |    |     |    |     |         |     |        |     |     |    |     |     |          |     |     |    |     |     |    |     |     |

| Command Table |      |     |                |                |                |                |                |                |                |                |                                             |                                                                                                                                                                 |
|---------------|------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R/W#          | D/C# | Hex | D7             | D6             | D5             | D4             | D3             | D2             | D1             | D0             | Command                                     | Description                                                                                                                                                     |
| 0             | 0    | 44  | 0              | 1              | 0              | 0              | 0              | 1              | 0              | 0              | Set RAM X - address<br>Start / End position | Specify the start/end positions of the<br>window address in the X direction by an<br>address unit<br><br>A[4:0]: X-Start, POR = 00h<br>B[4:0]: X-End, POR = 12h |
| 0             | 1    |     | 0              | 0              | 0              | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                             |                                                                                                                                                                 |
| 0             | 1    |     | 0              | 0              | 0              | B <sub>4</sub> | B <sub>3</sub> | B <sub>2</sub> | B <sub>1</sub> | B <sub>0</sub> |                                             |                                                                                                                                                                 |
|               |      |     |                |                |                |                |                |                |                |                |                                             |                                                                                                                                                                 |
| 0             | 0    | 45  | 0              | 1              | 0              | 0              | 0              | 1              | 0              | 1              | Set Ram Y- address<br>Start / End position  | Specify the start/end positions of the<br>window address in the Y direction by an<br>address unit<br>A[7:0]: Y-Start, POR = 00h<br>B[7:0]: Y-End, POR = F9h     |
| 0             | 1    |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                             |                                                                                                                                                                 |
| 0             | 1    |     | B <sub>7</sub> | B <sub>6</sub> | B <sub>5</sub> | B <sub>4</sub> | B <sub>3</sub> | B <sub>2</sub> | B <sub>1</sub> | B <sub>0</sub> |                                             |                                                                                                                                                                 |
|               |      |     |                |                |                |                |                |                |                |                |                                             |                                                                                                                                                                 |
| 0             | 0    | 4E  | 0              | 1              | 0              | 0              | 1              | 1              | 1              | 0              | Set RAM X address<br>counter                | Make initial settings for the RAM X<br>address in the address counter (AC)<br>A[4:0]: POR is 00h                                                                |
| 0             | 1    |     | 0              | 0              | 0              | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                             |                                                                                                                                                                 |
|               |      |     |                |                |                |                |                |                |                |                |                                             |                                                                                                                                                                 |
| 0             | 0    | 4F  | 0              | 1              | 0              | 0              | 1              | 1              | 1              | 1              | Set RAM Y address<br>counter                | Make initial settings for the RAM Y<br>address in the address counter (AC)<br>A[7:0]: POR is 00h                                                                |
| 0             | 1    |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |                                             |                                                                                                                                                                 |

## 8 COMMAND DESCRIPTION

### 8.1 Driver Output Control (01h)

This double byte command has multiple configurations and each bit setting is described as follows:

| R/W | DC | IB7    | IB6    | IB5    | IB4    | IB3    | IB2    | IB1    | IB0    |
|-----|----|--------|--------|--------|--------|--------|--------|--------|--------|
| W   | 1  | MUX[7] | MUX[6] | MUX[5] | MUX[4] | MUX[3] | MUX[2] | MUX[1] | MUX[0] |
| POR |    | 1      | 1      | 1      | 1      | 1      | 0      | 0      | 1      |
| W   | 1  |        |        |        |        |        | GD     | SM     | TB     |
| POR |    |        |        |        |        |        | 0      | 0      | 0      |

#### MUX[7:0]:

Specify number of lines for the driver: MUX[7:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 250MU

#### GD:

Selects the 1st output Gate

This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

#### SM:

Change scanning order of gate driver.

When SM is set to 0, left and right interlaced is performed.

When SM is set to 1, no splitting odd / even of the GATE signal is performed,

Output pin assignment sequence is shown as below (for 250 MUX ratio):

|        | SM=0   | SM=0   | SM=1   | SM=1   |
|--------|--------|--------|--------|--------|
| Driver | GD=0   | GD=1   | GD=0   | GD=1   |
| G0     | ROW0   | ROW1   | ROW0   | ROW125 |
| G1     | ROW1   | ROW0   | ROW125 | ROW0   |
| G2     | ROW2   | ROW3   | ROW1   | ROW126 |
| G3     | ROW3   | ROW2   | ROW126 | ROW1   |
| :      | :      | :      | :      | :      |
| G123   | ROW123 | ROW122 | ROW186 | ROW61  |
| G124   | ROW124 | ROW125 | ROW62  | ROW187 |
| G125   | ROW125 | ROW124 | ROW187 | ROW62  |
| G126   | ROW126 | ROW127 | ROW63  | ROW188 |
| :      | :      | :      | :      | :      |
| G246   | ROW246 | ROW247 | ROW123 | ROW248 |
| G247   | ROW247 | ROW246 | ROW248 | ROW123 |
| G248   | ROW248 | ROW249 | ROW124 | ROW249 |
| G249   | ROW249 | ROW248 | ROW249 | ROW124 |

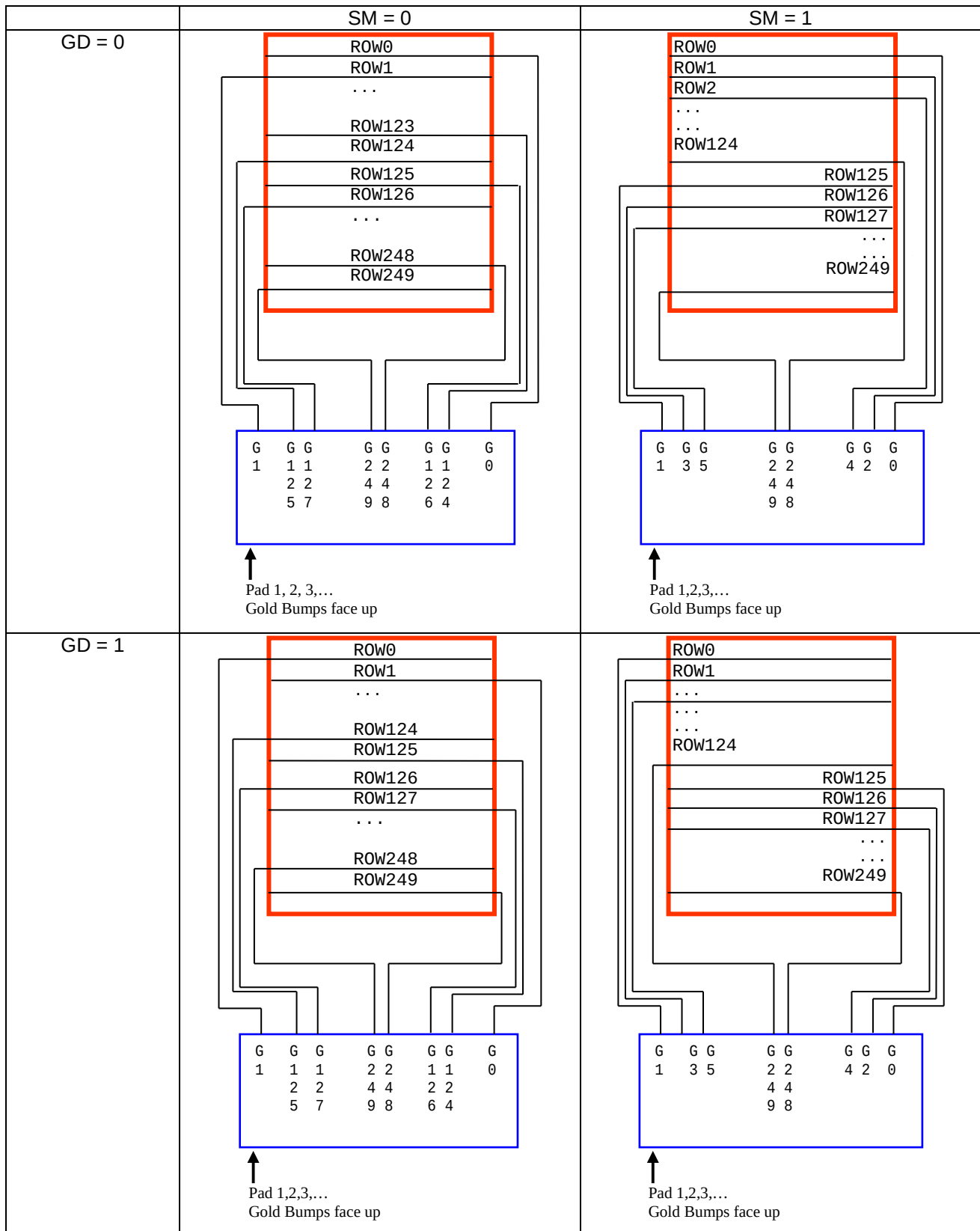
See "Scan Mode Setting" on next page.

#### TB:

Change scanning direction of gate driver.

This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

Figure 8-1: Output pin assignment on different Scan Mode Setting





## 8.2 Gate Scan Start Position (0Fh)

| R/W | DC | IB7  | IB6  | IB5  | IB4  | IB3  | IB2  | IB1  | IB0  |
|-----|----|------|------|------|------|------|------|------|------|
| W   | 1  | SCN7 | SCN6 | SCN5 | SCN4 | SCN3 | SCN2 | SCN1 | SCN0 |
| POR |    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 249. Figure 8-2 shows an example using this command of this command when MUX ratio= 250 and MUX ratio= 125 “ROW” means the graphic display data RAM row.

**Figure 8-2: Example of Set Display Start Line with no Remapping**

| GATE Pin        | MUX ratio (01h) = F9h               | MUX ratio (01h) = 7Ch               | MUX ratio (01h) = 7Ch               |
|-----------------|-------------------------------------|-------------------------------------|-------------------------------------|
|                 | Gate Start Position (0Fh)<br>= 000h | Gate Start Position (0Fh)<br>= 000h | Gate Start Position (0Fh)<br>= 046h |
| G0              | ROW0                                | ROW0                                | -                                   |
| G1              | ROW1                                | ROW1                                | -                                   |
| G2              | ROW2                                | ROW2                                | -                                   |
| G3              | ROW3                                | ROW3                                | -                                   |
| :               | :                                   | :                                   | :                                   |
| :               | :                                   | :                                   | :                                   |
| G68             | :                                   | :                                   | -                                   |
| G69             | :                                   | :                                   | -                                   |
| G70             | :                                   | :                                   | ROW70                               |
| G71             | :                                   | :                                   | ROW71                               |
| :               | :                                   | :                                   | :                                   |
| :               | :                                   | :                                   | :                                   |
| G123            | ROW123                              | ROW123                              | :                                   |
| G124            | ROW124                              | ROW124                              | :                                   |
| G125            | ROW125                              | -                                   | :                                   |
| G126            | ROW126                              | -                                   | :                                   |
| :               | :                                   | :                                   | :                                   |
| :               | :                                   | :                                   | :                                   |
| G219            | :                                   | :                                   | ROW219                              |
| G220            | :                                   | :                                   | ROW220                              |
| G221            | :                                   | :                                   | -                                   |
| G222            | :                                   | :                                   | -                                   |
| :               | :                                   | :                                   | :                                   |
| :               | :                                   | :                                   | :                                   |
| G246            | ROW246                              | -                                   | -                                   |
| G247            | ROW247                              | -                                   | -                                   |
| G248            | ROW248                              | -                                   | -                                   |
| G249            | ROW249                              | -                                   | -                                   |
| Display Example |                                     |                                     |                                     |



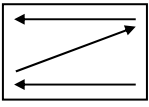
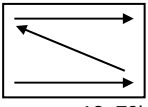
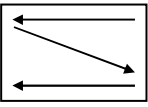
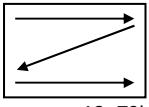
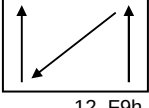
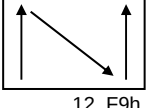
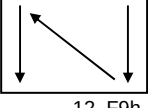
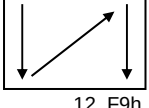
### 8.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

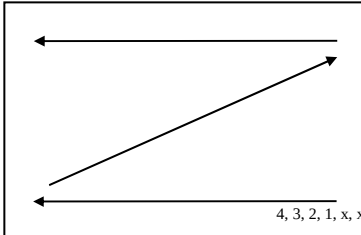
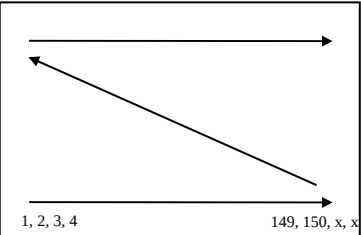
| R/W | DC | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| W   | 1  |     |     |     |     |     | AM  | ID1 | ID0 |
| POR |    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**ID[1:0]:** The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = "01". The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = "00". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

**AM:** Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = "0", the address counter is updated in the X direction. When AM = "1", the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

|                  | ID [1:0]="00"<br>X: decrement<br>Y: decrement                                                            | ID [1:0]="01"<br>X: increment<br>Y: decrement                                                            | ID [1:0]="10"<br>X: decrement<br>Y: increment                                                            | ID [1:0]="11"<br>X: increment<br>Y: increment                                                              |
|------------------|----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| AM="0"<br>X-mode | 00,00h<br><br>12, F9h   | 00,00h<br><br>12, F9h   | 00,00h<br><br>12, F9h   | 00,00h<br><br>12, F9h   |
| AM="1"<br>Y-mode | 00,00h<br><br>12, F9h | 00,00h<br><br>12, F9h | 00,00h<br><br>12, F9h | 00,00h<br><br>12, F9h |

The pixel sequence is defined by the ID [0],

|                  | ID[1:0]="00"<br>X: decrement<br>Y: decrement                                                             | ID[1:0]="01"<br>X: increment<br>Y: decrement                                                              |
|------------------|----------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|
| AM="0"<br>X-mode | 00,00h<br><br>12, F9h | 00,00h<br><br>12, F9h |

## 8.4 Set RAM X - Address Start / End Position (44h)

| R/W | DC | IB7 | IB6 | IB5 | IB4  | IB3  | IB2  | IB1  | IB0  |
|-----|----|-----|-----|-----|------|------|------|------|------|
| W   | 1  |     |     |     | XSA4 | XSA3 | XSA2 | XSA1 | XSA0 |
| POR |    | 0   | 0   | 0   | 0    | 0    | 0    | 0    | 0    |
| W   | 1  |     |     |     | XEA4 | XEA3 | XEA2 | XEA1 | XEA0 |
| POR |    | 0   | 0   | 0   | 1    | 0    | 0    | 1    | 0    |

**XSA[4:0]/XEA[4:0]:** Specify the start/end positions of the window address in the X direction by 8 times address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write.

It allows on  $XEA [4:0] \leq XSA [4:0]$ . The settings follow the condition on  $00h \leq XSA [4:0]$ ,  $XEA [4:0] \leq 12h$ . The windows is followed by the control setting of Data Entry Setting (R11h)

## 8.5 Set RAM Y - Address Start / End Position (45h)

| R/W | DC | IB7  | IB6  | IB5  | IB4  | IB3  | IB2  | IB1  | IB0  |
|-----|----|------|------|------|------|------|------|------|------|
| W   | 1  | YSA7 | YSA6 | YSA5 | YSA4 | YSA3 | YSA2 | YSA1 | YSA0 |
| POR |    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| W   | 1  | YEA7 | YEA6 | YEA5 | YEA4 | YEA3 | YEA2 | YEA1 | YEA0 |
| POR |    | 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1    |

**YSA[7:0]/YEA[7:0]:** Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [7:0] and YEA [7:0]. These addresses must be set before the RAM write.

It allows  $YEA [7:0] \leq YSA [7:0]$ . The settings follow the condition on  $00h \leq YSA [7:0]$ ,  $YEA [7:0] \leq F9h$ . The windows is followed by the control setting of Data Entry Setting (R11h)

## 8.6 Set RAM Address Counter (4Eh-4Fh)

| Reg# | R/W | DC | IB7  | IB6  | IB5  | IB4  | IB3  | IB2  | IB1  | IB0  |
|------|-----|----|------|------|------|------|------|------|------|------|
| 4Eh  | W   | 1  |      |      |      | XAD4 | XAD3 | XAD2 | XAD1 | XAD0 |
|      | POR |    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| 4Fh  | W   | 1  | YAD7 | YAD6 | YAD5 | YAD4 | YAD3 | YAD2 | YAD1 | YAD0 |
|      | POR |    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**XAD[4:0]:** Make initial settings for the RAM X address in the address counter (AC).

**YAD[7:0]:** Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]}; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

## 9 Typical Operating Sequence

### 9.1 Normal Display

| Sequence | Action by | Command | Action Description                                                                                                                                        | Remark |
|----------|-----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
| 1        | User      | -       | Power on (VCI supply);                                                                                                                                    |        |
| 2        | User      | -       | HW Reset                                                                                                                                                  |        |
|          | IC        |         | After HW reset, the IC will have<br>Registers load with POR value<br>Ready for command input<br>VCOM register loaded with OTP value<br>IC enter idle mode |        |
| 3        |           | -       | Send initial code to driver including setting of                                                                                                          |        |
|          | User      | C 01    | Command: Panel configuration (MUX, Source gate scanning direction)                                                                                        |        |
|          | User      | C 3A    | Command: Set dummy line pulse period                                                                                                                      |        |
|          | User      | C 3B    | Command: Set Gate line width                                                                                                                              |        |
|          | User      | C 3C    | Command: Select Border waveform                                                                                                                           |        |
| 4        |           | -       | Data operations                                                                                                                                           |        |
|          | User      | C 11    | Command: Data Entry mode                                                                                                                                  |        |
|          | User      | C 44    | Command: X RAM address start /end                                                                                                                         |        |
|          | User      | C 45    | Command: Y RAM address start /end                                                                                                                         |        |
|          | User      | C 4E    | Command: RAM X address counter                                                                                                                            |        |
|          | User      | C 4F    | Command: RAM Y address counter                                                                                                                            |        |
|          | User      | C 24    | Command: write display data to RAM                                                                                                                        |        |
|          |           |         | Ram Content for Display                                                                                                                                   |        |
| 5        | User      | C 22    | Command: Display Update Control 2                                                                                                                         |        |
|          | User      | C 20    | Command: Master Activation                                                                                                                                |        |
|          | IC        | -       | Booster and regulators turn on                                                                                                                            |        |
|          | IC        | -       | Load LUT register with corresponding waveform setting stored in OTP)                                                                                      |        |
|          | IC        | -       | Send output waveform according initial update option                                                                                                      |        |
|          | IC        | -       | Send output waveform according to data                                                                                                                    |        |
|          | IC        | -       | Booster and Regulators turn off                                                                                                                           |        |
|          | IC        | -       | Back to idle mode                                                                                                                                         |        |
| 6        | User      | -       | IC power off;                                                                                                                                             |        |

## 9.2 VCOM OTP Program

| Sequence | Action by | Command              | Action Description                                                                           | Remark                                                   |
|----------|-----------|----------------------|----------------------------------------------------------------------------------------------|----------------------------------------------------------|
| 1        | User      | -                    | Power on (VCI and VPP supply)                                                                |                                                          |
| 2        | User      | -                    | HW Reset                                                                                     |                                                          |
| 3        | User      | C 22<br>D 80<br>C 20 | Command: CLKEN=1                                                                             |                                                          |
|          | User      | -                    | Wait until BUSY = L                                                                          |                                                          |
| 4        | User      | C 37                 | Proceed OTP sequence.<br>Command: Indicate which OTP location to be use (default or spare)   | OTP selection register                                   |
| 5        | User      | C 36                 | Program OTP selection register                                                               |                                                          |
|          | User      | -                    | Wait until BUSY = L                                                                          |                                                          |
|          | User      | -                    | Power OFF (VPP supply)                                                                       |                                                          |
| 6        |           | -                    | Send initial code to driver including setting of (or leave as POR)                           | VCOM sensing should have same setting during application |
|          | User      | C 22<br>D 40         | Command: Booster on and High voltage ready                                                   |                                                          |
|          | User      | C 01                 | Command: Panel configuration (MUX, Source gate scanning direction)                           |                                                          |
|          | User      | C 03                 | Command: VGH, VGL voltage                                                                    |                                                          |
|          | User      | C 04                 | Command: VSH / VSL voltage                                                                   |                                                          |
|          | User      | C 3A                 | Command: Set dummy line pulse period                                                         |                                                          |
|          | User      | C 3B                 | Command: Set Set 1 Gate line duration as default                                             |                                                          |
|          | User      | C 32                 | VCOM sense required full set of LUT for operation, USER required writing LUT in register 32h |                                                          |
|          |           | -                    | LUT parameter                                                                                |                                                          |
|          | User      | C 20                 | Perform the turn off analog operation (assigned by R22h) [Enable Analog blocks ]             |                                                          |
|          | User      | -                    | Wait until BUSY = L                                                                          |                                                          |
| 7        | User      | C 29                 | Command: Set Set the VCOM Sensing time                                                       |                                                          |
| 8        | User      | C 28                 | Command: Enter VCOM sensing mode                                                             |                                                          |
|          | IC        | -                    | VCOM pin in sensing mode                                                                     |                                                          |
|          | IC        | -                    | All Source cell have VSS output                                                              |                                                          |
|          |           |                      | All Gate scanning continuously                                                               |                                                          |
|          | IC        | -                    | Wait for 10s                                                                                 | According to R29h                                        |
|          | IC        | -                    | Detect VCOM voltage and store in register                                                    |                                                          |
|          | IC        | -                    | All Gate Stop Scanning.                                                                      |                                                          |
| 9        | User      | -                    | Wait until BUSY = L                                                                          |                                                          |
|          | User      | C 22<br>D 02<br>C 20 | Command: Booster and High voltage disable                                                    |                                                          |
|          | User      | -                    | Wait until BUSY = L                                                                          |                                                          |
| 10       | User      | -                    | Power On (VPP supply)                                                                        |                                                          |
|          | User      | C 2A                 | Command: VCOM OTP program                                                                    |                                                          |
| 11       | User      | -                    | Wait until BUSY = L                                                                          |                                                          |
|          | User      | C 22<br>D 01<br>C 20 | Command: CLKEN=0                                                                             |                                                          |
|          | User      | -                    | Wait until BUSY = L                                                                          |                                                          |
| 12       | User      | -                    | IC power off (VCI and VPP Supply)                                                            |                                                          |

### 9.3 WS OTP Program

| Sequence | Action by | Command                      | Action Description                                                                            | Remark                    |
|----------|-----------|------------------------------|-----------------------------------------------------------------------------------------------|---------------------------|
| 1        | User      | -                            | Power on (VCI supply)                                                                         |                           |
| 2        | User      | -                            | Power on (VPP supply)                                                                         |                           |
| 3        | User      | -                            | HW Reset                                                                                      |                           |
| 4        | User      | C 22<br>D 80<br>C 20         | Command: CLKEN=1                                                                              |                           |
|          | User      | -                            | Wait BUSY = L                                                                                 |                           |
| 4        | User      | C 37                         | Proceed OTP sequence.<br>Command: Indicate which OTP location to be use<br>(default or spare) | OTP selection<br>register |
| 5        | User      | C 36                         | Program OTP selection register                                                                |                           |
|          | User      | -                            | Wait BUSY = L                                                                                 |                           |
| 6        | User      | C 24                         | Write corresponding data into RAM                                                             |                           |
|          |           |                              | Following specific format                                                                     |                           |
|          |           |                              | Write into RAM                                                                                |                           |
|          |           |                              | Full LUT                                                                                      |                           |
| 7        | User      | C 4E<br>D 00<br>C 4F<br>D 00 | Command: Initial Ram address counter                                                          |                           |
| 8        | User      | C 30                         | Waveform Setting OTP programming                                                              |                           |
|          | User      | -                            | Wait BUSY = L                                                                                 |                           |
| 9        | User      | C 22<br>D 01<br>C 20         | Command: CLKEN=0                                                                              |                           |
|          | User      | -                            | Wait BUSY = L                                                                                 |                           |
| 10       | User      | -                            | Power off VPP and VCI                                                                         |                           |

## 10 ABSOLUTE MAXIMUM RATING

Table 10-1: Maximum Ratings

| Symbol           | Parameter                   | Rating                         | Unit |
|------------------|-----------------------------|--------------------------------|------|
| V <sub>CI</sub>  | Logic supply voltage        | -0.5 to +4.0                   | V    |
| V <sub>IN</sub>  | Logic Input voltage         | -0.5 to V <sub>DDIO</sub> +0.5 | V    |
| V <sub>OUT</sub> | Logic Output voltage        | -0.5 to V <sub>DDIO</sub> +0.5 | V    |
| T <sub>OPR</sub> | Operation temperature range | -40 to +85                     | °C   |
| T <sub>STG</sub> | Storage temperature range   | -65 to +150                    | °C   |

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V<sub>CI</sub> be constrained to the range V<sub>SS</sub> < V<sub>CI</sub>. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DDIO</sub>). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

## 11 DC CHARACTERISTICS

The following specifications apply for:  $V_{SS}=0V$ ,  $V_{CI}=3.0V$ ,  $V_{DD}=1.8V$ ,  $T_{OPR}=25^{\circ}C$ .

**Table 11-1: DC Characteristics**

| Symbol          | Parameter                        | Test Condition                                                                                                                  | Applicable pin | Min.          | Typ. | Max.          | Unit    |
|-----------------|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------|----------------|---------------|------|---------------|---------|
| $V_{SS}$        | Ground                           |                                                                                                                                 |                |               | 0    |               | V       |
| $V_{CI}$        | VCI operation voltage            |                                                                                                                                 | VCI            | 2.4           | 3.0  | 3.7           | V       |
| $V_{DD}$        | VDD operation voltage            |                                                                                                                                 | VDD            | 1.7           | 1.8  | 1.9           | V       |
| $V_{COM}$       | VCOM output voltage              |                                                                                                                                 | VCOM           | -4.0          |      | -0.2          | V       |
|                 |                                  |                                                                                                                                 |                |               |      |               |         |
| $V_{GATE}$      | Gate output voltage              |                                                                                                                                 | G0-249         | -20           |      | +22           | V       |
| $V_{GATE(p-p)}$ | Gate output peak to peak voltage |                                                                                                                                 | G0-249         |               |      | 42            | V       |
| $V_{SH}$        | Positive Source output voltage   |                                                                                                                                 | S0-149         |               | 15   |               | V       |
| $V_{SL}$        | Negative Source output voltage   |                                                                                                                                 | S0-149         |               | -VSH |               | V       |
| $V_{IH}$        | High level input voltage         | $V_{CI} = V_{DDIO}$                                                                                                             |                | $0.8V_{DDIO}$ |      |               | V       |
| $V_{IL}$        | Low level input voltage          | $V_{CI} = V_{DDIO}$                                                                                                             |                |               |      | $0.2V_{DDIO}$ | V       |
| $V_{OH}$        | High level output voltage        | $V_{CI} = V_{DDIO}$<br>$I_{OH} = -100\mu A$                                                                                     |                | $0.9V_{DDIO}$ |      |               | V       |
| $V_{OL}$        | Low level output voltage         | $V_{CI} = V_{DDIO}$<br>$I_{OL} = 100\mu A$                                                                                      |                |               |      | $0.1V_{DDIO}$ | V       |
| $V_{PP}$        | OTP Program voltage              |                                                                                                                                 | VPP            |               | 7.5  |               | V       |
| Dislp_VCI       | Deep sleep mode current          | - DC/DC off<br>- No clock,<br>- No output load<br>- No MCU interface access<br>- RAM data retain only and cannot access the RAM | VCI            |               | 2    | 5             | $\mu A$ |
| Islp_VCI        | Sleep mode current               | - DC/DC off<br>- No clock<br>- No output load<br>- MCU interface access<br>- RAM data access                                    | VCI            |               | 35   | 50            | $\mu A$ |

| Symbol           | Parameter         | Test Condition                                                                                                                                                                                             | Applicable pin | Min.  | Typ. | Max.  | Unit |
|------------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-------|------|-------|------|
| Iopr_VCI         | Operating current | - DC/DC on<br>- VGH=22V<br>- VGL=-20V<br>- VSH=15V<br>- VSL=-15V<br>- VCOM = -2V<br>- No waveform transitions.<br>- No loading.<br>- No RAM read/write<br>- No OTP read /write<br>- Osc on<br>- Bandgap on | VCI            |       | 2000 |       | uA   |
| V <sub>GH</sub>  | Operating Mode    | VCI=3.0V                                                                                                                                                                                                   | VGH            | 21    | 22   | 23    | V    |
| V <sub>SH</sub>  | Output Voltage    | DC/DC on                                                                                                                                                                                                   | VSH            | 14.5  | 15   | 15.5  | V    |
| V <sub>COM</sub> |                   | VGH=22V                                                                                                                                                                                                    | VCOM           | -2.5  | -2   | -1.5  | V    |
| V <sub>SL</sub>  |                   | VGL=-20V                                                                                                                                                                                                   | VSL            | -15.5 | -15  | -14.5 | V    |
| V <sub>GL</sub>  |                   | VSH=15V<br>VSL=-15V<br>VCOM = -2V<br>No waveform transitions.<br>No loading.<br>Osc on<br>Bandgap on                                                                                                       | VGL            | -21   | -20  | -19   | V    |

**Table 11-2: Regulators Characteristics**

| Symbol | Parameter    | Test Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|--------|--------------|----------------|----------------|------|------|------|------|
| IVGH   | VGH current  | VGH = 22V      | VGH            |      |      | 400  | uA   |
| IVGL   | VGL current  | VGL = -20V     | VGL            |      |      | 600  | uA   |
| IVSH   | VSH current  | VSH = +15V     | VSH            |      |      | 4000 | uA   |
| IVSL   | VSL current  | VSL = -15V     | VSL            |      |      | 4000 | uA   |
| IVCOM  | VCOM current | VCOM = -2V     | VCOM           |      |      | 100  | uA   |



## 12 AC CHARACTERISTICS

### 12.1 Oscillator frequency

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T<sub>OPR</sub>=25°C.

**Table 12-1: Oscillator Frequency**

| Symbol | Parameter                     | Test Condition  | Applicable pin | Min. | Typ. | Max. | Unit |
|--------|-------------------------------|-----------------|----------------|------|------|------|------|
| Fosc   | Internal Oscillator frequency | VCI=2.4 to 3.7V | CL             | 0.95 | 1    | 1.05 | MHz  |

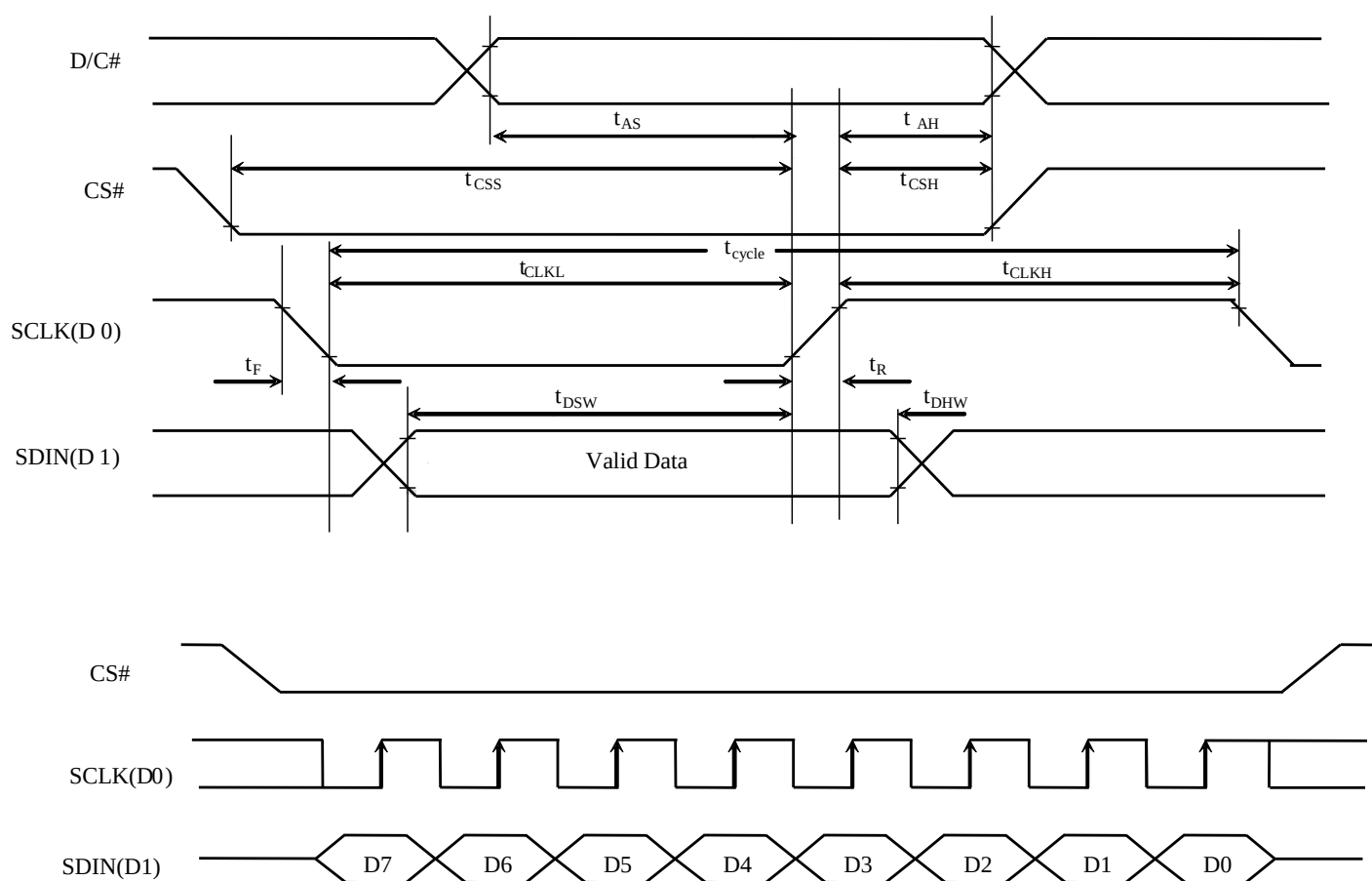
## 12.2 Interface Timing

**Table 12-2 : Serial Peripheral Interface Timing Characteristics**

( $V_{DDIO} - V_{SS} = 2.4V$  to  $3.7V$ ,  $T_{OPR} = 25^{\circ}C$ ,  $C_L = 20pF$ )

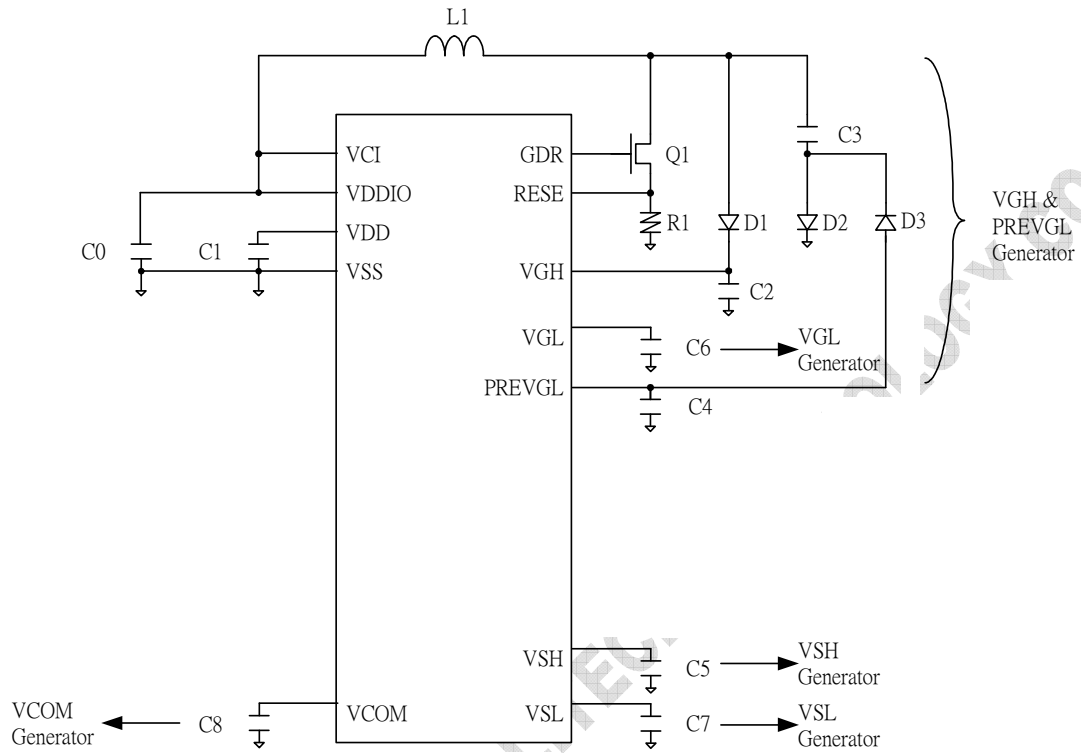
| Symbol      | Parameter              | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| $t_{cycle}$ | Clock Cycle Time       | 250 | -   | -   | ns   |
| $t_{AS}$    | Address Setup Time     | 150 | -   | -   | ns   |
| $t_{AH}$    | Address Hold Time      | 150 | -   | -   | ns   |
| $t_{CSS}$   | Chip Select Setup Time | 120 | -   | -   | ns   |
| $t_{CSH}$   | Chip Select Hold Time  | 60  | -   | -   | ns   |
| $t_{DSW}$   | Write Data Setup Time  | 50  | -   | -   | ns   |
| $t_{DHW}$   | Write Data Hold Time   | 15  | -   | -   | ns   |
| $t_{CLKL}$  | Clock Low Time         | 100 | -   | -   | ns   |
| $t_{CLKH}$  | Clock High Time        | 100 | -   | -   | ns   |
| $t_R$       | Rise Time [20% ~ 80%]  | -   | -   | 15  | ns   |
| $t_F$       | Fall Time [20% ~ 80%]  | -   | -   | 15  | ns   |

**Figure 12-1 : Serial peripheral interface characteristics**



## 13 APPLICATION CIRCUIT

Figure 13-1 : Booster Connection Diagram



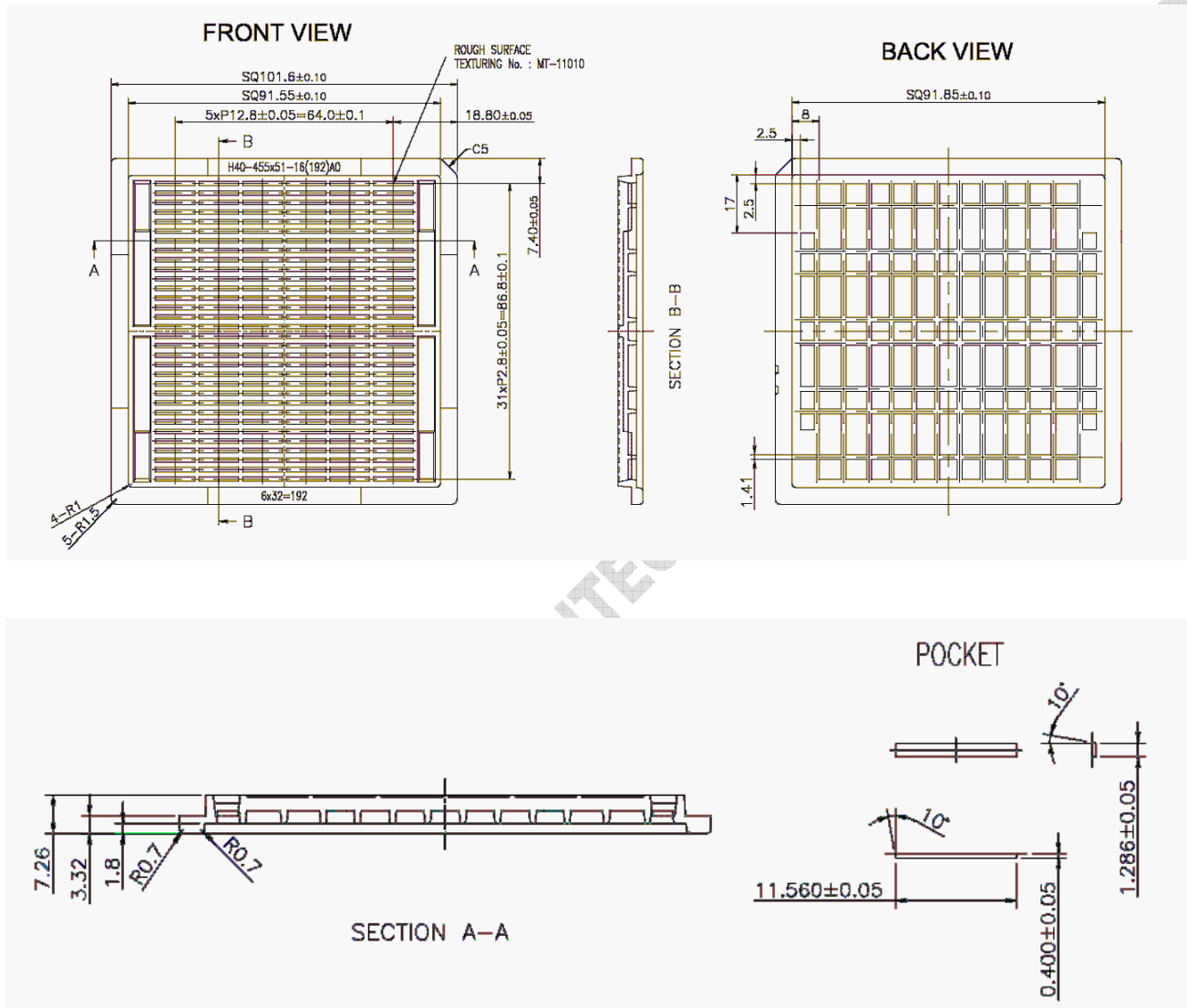
**Table 13-1 : Reference Component Value**

| Part Name | Value                    | Max Volt.<br>Rating<br>[In V] | Pins Connected  | MAX COG ITO<br>resistance [in Ohm] |
|-----------|--------------------------|-------------------------------|-----------------|------------------------------------|
| C0        | 1uF                      | 6                             | VCI, VDDIO, VSS | 5                                  |
| C1        | 1uF                      | 6                             | VDD, VSS        | 30                                 |
| C2        | 1uF                      | 50                            | VGH             | 5                                  |
| C3        | 1uF                      | 50                            | L1 and D2/D3    | NA                                 |
| C4        | 1uF                      | 50                            | PREVGL          | 5                                  |
| C5        | 1uF                      | 25                            | VSH             | 5                                  |
| C6        | 1uF                      | 25                            | VGL             | 10                                 |
| C7        | 1uF                      | 25                            | VSL             | 5                                  |
| C8        | 1uF                      | 6                             | VCOM            | 5                                  |
| L1        | 47uH                     |                               |                 |                                    |
| Q1        | NMOS [Vishay: Si1304BDL] |                               | GDR, RESE       | 5                                  |
| D1        | Diode [OnSemi: MBR0530]  |                               | PREVGH          | NA                                 |
| D2        | Diode [OnSemi: MBR0530]  |                               |                 | NA                                 |
| D3        | Diode [OnSemi: MBR0530]  |                               | PREVGL, VSS     | NA                                 |
| R1        | 2.2 Ohm                  |                               | RESE            | 5                                  |

## 14 PACKAGE INFORMATION

### 14.1 DIE TRAY DIMENSIONS

Figure 14-1 : SSD1673Z die tray information



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