Rev.0.01

Reference Specification

S6D04K1

-X02

MOBILE DISPLAY DRIVER IC

Preliminary

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REVISION HISTORY

Rev.#	Date	History	Author
0.00	Aug `09	1. Initial Release	Aliex
0.01	Jan 5 10	1. Update PAD coordinate P385~P396 2. Update Application circuit P378 3. Update Bump Dimention P27 4. Update DISPLAY DATA RAM P167~P177 5. Update COMMAND P197~P376	Aliex/Leo

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Preface

About This Reference Specification

This document is to provide a complete reference specification of S6D04K1 IC design. It also provides useful information to those who works on a panel module or a set

IMPORTANT NOTICE

Precautions against Light

The conductivity of a semiconductor is strongly influenced by electro-magnetic radiation such as visible light, infrared light, ultraviolet light, or gamma radiation. When light is absorbed, electron-hole pairs are generated raising the conductivity of the material, eventually altering the electrical characteristics of the IC. Therefore, if the packages that expose IC's to external light sources, such as COB, COG, TCP, and COF, are used, effective means to shield the IC from the light coming in all directions – top, bottom, and the sides – must be devised. Full observation of the following precautions is strongly recommended.

1. Make sure that the IC and substrate (board or glass) are protected from a stray light.
2. Always test and inspect products under the environment with no light penetration.

CHAPTER 1

OVERVIEW

1.1 Introduction
1.2 Product Options
1.3 Features
1.4 Block Diagram
1.5 Pad Information
1.6 Description of Signal Pads

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1. OVERVIEW

1.1. INTRODUCTION

S6D04K1 is a single-chip display driver IC for a TFT-LCD panel. S6D04K1 has source drivers with built-in memory, gate drivers and power sources. S6D04K1 can support a TFT-LCD panel up to a resolution of 320-RGB x 240-dot graphics with 262k colors.

1.2. PRODUCT OPTIONS

S6D04K1 may offer more than one option in order to meet customer-specific functions from the customers. Table 1 describes its functions.

Table 1. List of S6D04K1 Options.

Options	Remarks
-x02	Reference Design of S6D04K1-X01

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1.3. FEATURES

S6D04K1 offers the following key features:

- Single chip TFT-LCD controller and driver with Display RAM.
- Display resolution: 320*RGB(H) *240(V)
- Display data RAM (frame memory) 320 x 240 x 18-bit = 1,382,400 bits
- Output:
  - Source output
  - Common electrode output
  - Gate output
- Display mode (Color mode)
  - Full color mode (Idle mode off): 262k-color
  - 65k-color
  - Reduce color mode (Idle mode on): 8-color
- MPU Interface:
  - 3-wire 9bit data serial interface
  - 4-wire 8bit data serial interface
  - 8 / 9 / 16 / 18bit parallel interface with 80-series MPU
  - 8 / 9 / 16 / 18bit parallel interface with 68-series MPU
  - 6 / 18bit RGB interface
- VSYNC Interface with 80-series MPU
- Display features
  - CABC (MIE2.5G) for saving current consumption
  - Partial display mode
  - Line inversion for low cross talk
- Display/Control Interface
  - DDIMobile Display Digital Interface
- MIPI DCS support
- MIE (Mobile Image Enhancement) function
  - Adaptive luminance/contrast enhancement function
  - Reduce the power consumption of backlight
- On chip
  - DC/DC converter
  - Adjusted VCOM generation
  - Oscillator for display clock generation

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- Timing generation

- Non-Volatile Memory (NVM)
  - 20 bits for VCOM offset and VCOMH/L adjustment
  - 408 bits for Gamma2.2 table.

- Driving Algorithm
  - Line inversion, frame inversion
- Supply voltage range
  - Analog supply voltage range for VCI to VSSA: 2.4V ~ 3.3V
  - I/O supply voltage range for VDD3 to VSS: 1.65V ~ 3.3V
- Output voltage levels
  - Source output voltage range for GVDD to VSSA: 3.26V to 5.0V
  - Power supply for driver circuit range for AVDD to VSSA: 4.2V to 6.0V
  - Max 6.0V Common electrode output voltage range for VCOM
  - Positive Gate output voltage range for VGH to VSSA: 8.4V to 16.5V (Note 3)
  - Negative Gate output voltage range for VGL to VSSA: -15V to –6.3V (Note 3)
- Lower power consumption, suitable for battery operated systems
- Optimized layout for COG assembly
- Operate temperature range: -40℃ to +85℃

Note.

1. Blank display means: Normal White Display = White, Normal Black Display = Black.
2. AVDD Min: When VCI1 = 2.1V, AVDD Max: When VCI1=3.0V
3. |VGH| & |VGL| Min: When VCI1 = 2.1V, |VGL| Max: When VCI1=3.0V, |VGH - VGL| Max: 30.0V
4. |VGH| Max should be lower than or equal to 16.5V in normal operating condition,
5. NVM and EEPROM mean MTP (Multi Time Programmable) in this specification.

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1.4. BLOCK DIAGRAM

1.4.1. MODULE LEVEL

Figure 1 shows the block diagram of a mobile display panel module and related interface signals required by set makers and module makers. Level I interface signals are usually required by a set maker who would then request the display module such a function, and Level II interface signals are required by a display module maker for its own purpose.

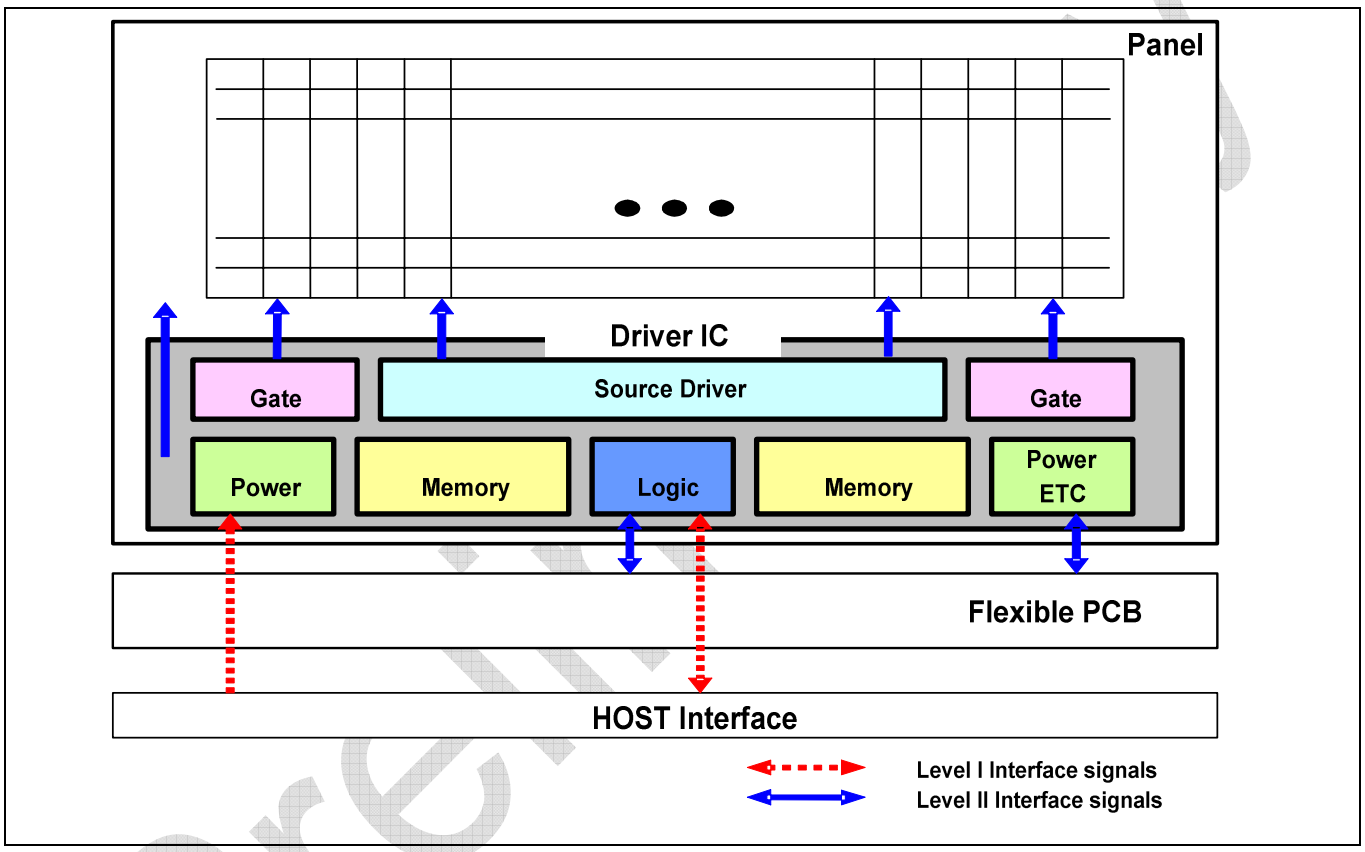

Figure1. Interface Signal Flow of a Mobile Display Panel Module.

There are also Level III signals which is for the internal use only for the driver IC itself. These signals may not necessarily be released to the customer since it is designed for a specific manufacturing purpose and are supposed to be hidden to customers.

This reference specification only provide a guideline to Level I and II interface signals since some of specifications related to Level I and II need a margin on IC side and would not be necessarily the same as the one in Level I and II specification even though both uses the same interface signals. This is mainly due to the parasitic and design requirements within the flexible PCB used by a display module maker. IC specification will offer related information among Level I/II on how each interface signals interact each other.

1.4.2. FUNCTIONAL BLOCK DIAGRAM OF THE IC

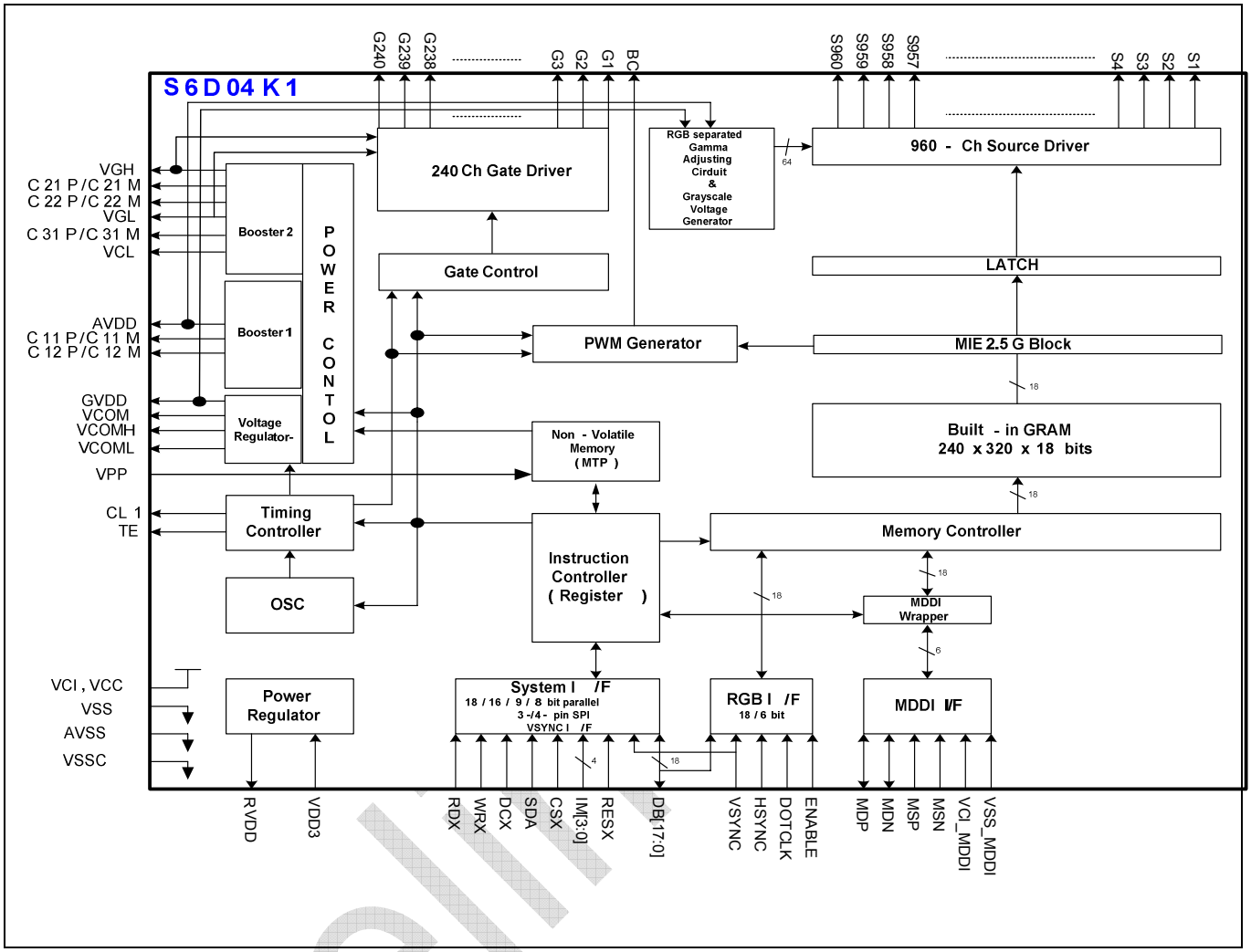

Figure2. S6D04K1 Block Diagram

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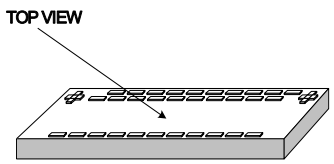
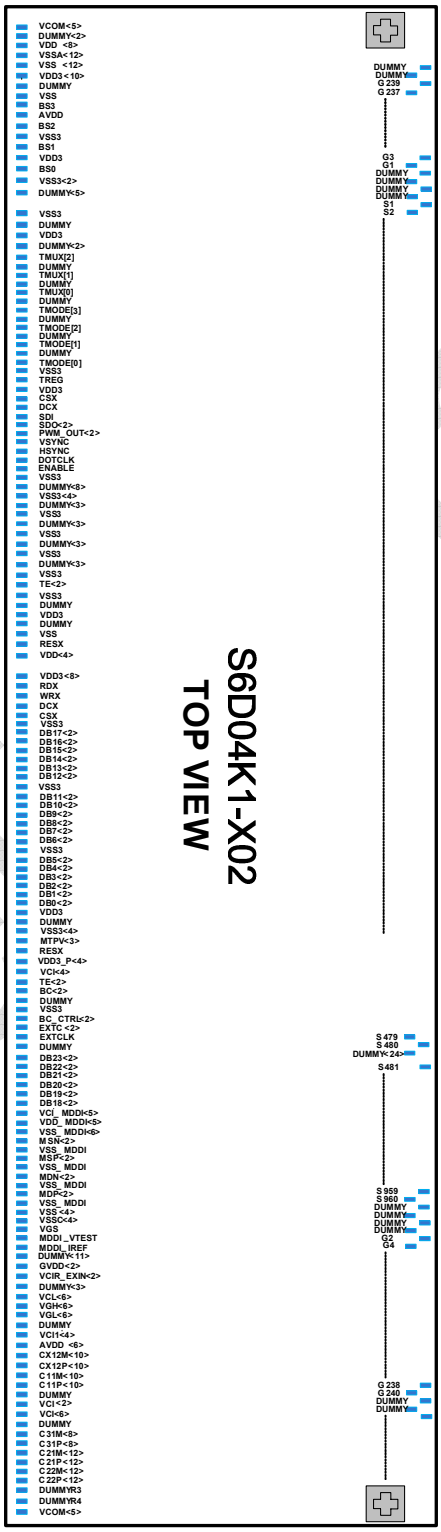
1.5. PAD INFORMATION

1.5.1. CONFIGURATION OF SIGNAL PADS





Preliminary

Figure3. S6D04K1 PAD Configuration

Note.

Pattern Surface

1.5.2. BUMP INFORMATION

Table 2. Bump Information

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	-	18620	700	μm
Pad Pitch	Input Side	40		
	Output Side	14/16		
Bumped Pad Top Size	Input Side	40±2	56±2	
	Output Side	14±2	104±2	
Bumped Pad Height	Height In Wafer	15±3		
	Tolerance In Chip	Under 2		
	Dimple Height	Under 2		
Chip Thickness	-	300±10		

Note.

1. Scribe lane 80um included in this die size
2. Wafer thickness can be varied with the customer's needs.

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1.5.3. BUMP DIMENSION

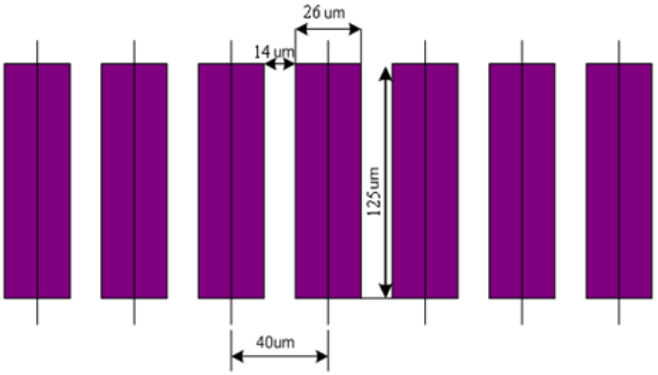
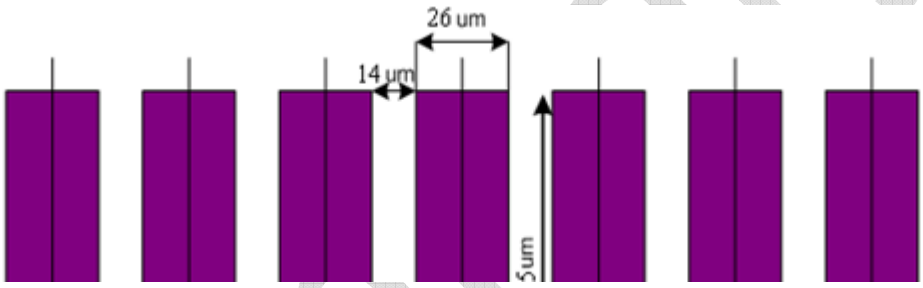
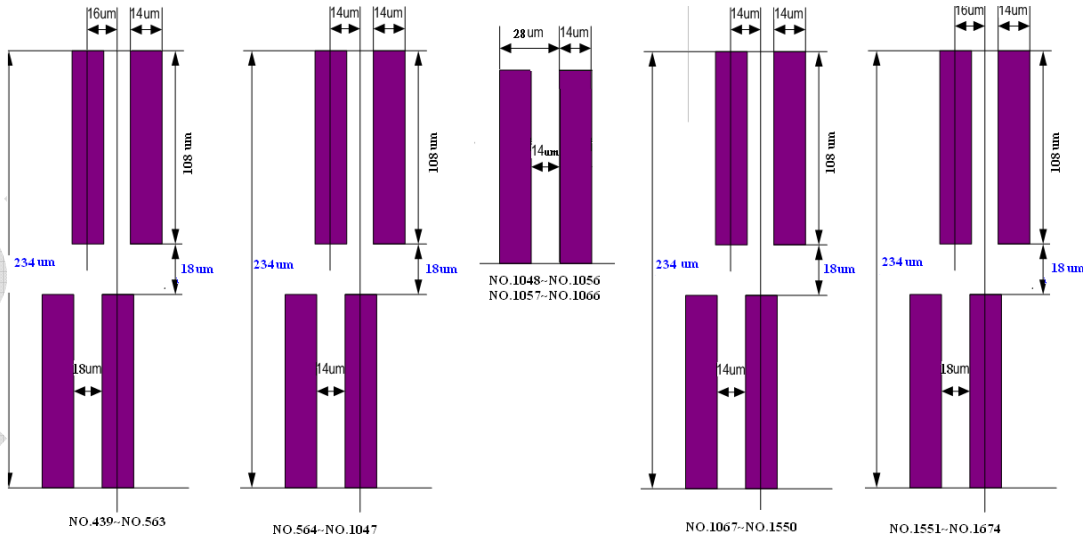
Input PAD	Bump Arrangement
No. 1 – No. 438	 NO.1~NO.219 NO.220~NO.438  NO.6~NO.10, NO.100~NO.102, NO.115~NO.118, NO.226~NO.228, NO.239~NO.240, NO.244~NO.246, NO.299~NO.30
No. 437 – No. 1672	

Figure4. Bump Dimension

1.5.4. ALIGN KEY

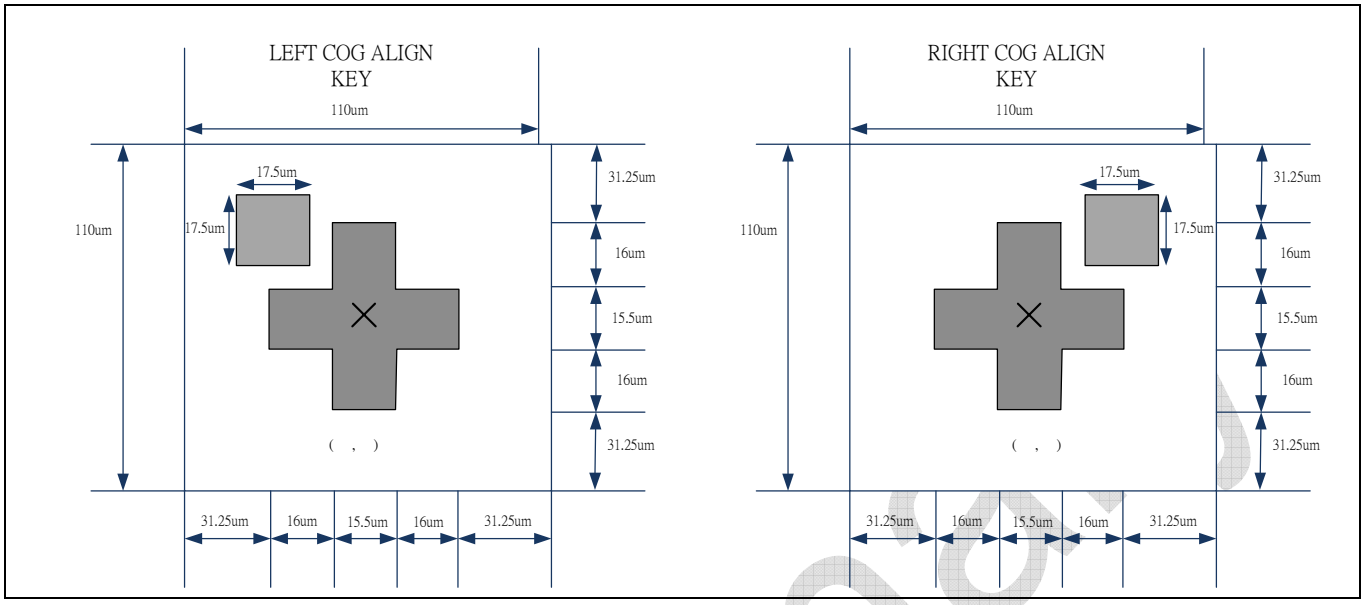


Figure5. COG Align Key Configuration and Coordinate

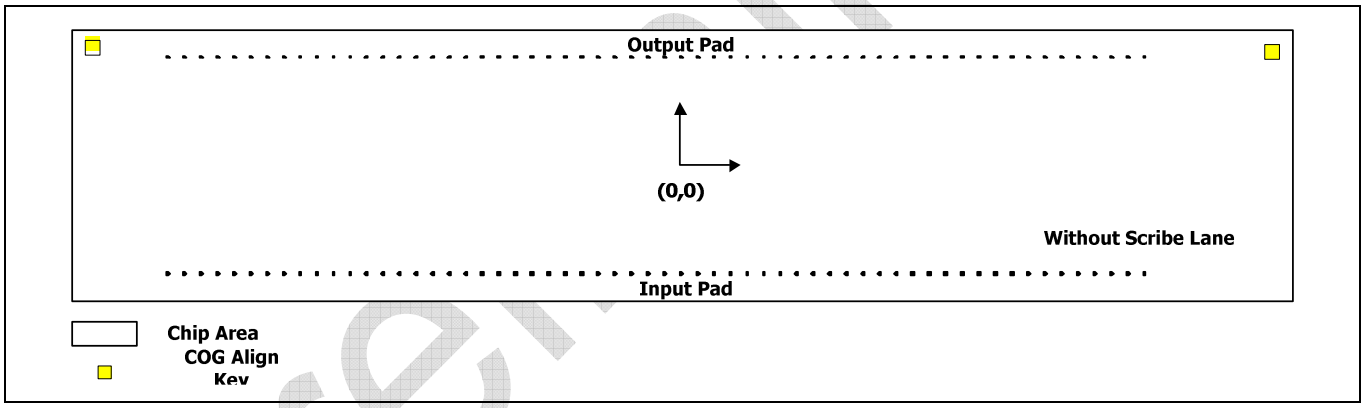


Figure6. COG Align Key Arrangement Layout

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1.6. DESCRIPTION OF SIGNAL PADS

1.6.1. POWER SUPPLY PINS

Table 3. Power Supply Pins

Symbol	Name	Description
VDD3	I/O voltage	Low voltage power supply for interface logic circuits (1.65 ~3.3 V)
VDD3	LED driver Power	Power supply for LED driver interface. (1.65 ~3.3 V) If LED driver is not used, fix this pin at VSS.
VCC	Analog Power	High voltage power supply for analog circuit blocks (2.4~3.3 V)
VDD	Regulated Voltage	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad
VSS3	I/O Ground	System ground level for I/O circuits.
VSS	Logic Ground	System ground level for logic blocks
VSSA	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.
VSSA	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise

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1.6.2. INTERFACE LOGIC PINS

Table 4. Interface Logic Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>Selects the MPU interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface mode</th><th>Data pad</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>68 MCU 8-bit Parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>68 MCU 9-bit Parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>68 MCU 16-bit Parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>68 MCU 18-bit Parallel I/F</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>80 MCU 8-bit Parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>80 MCU 9-bit Parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>80 MCU 16-bit Parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>80 MCU 18-bit Parallel I/F</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>MDDI + spi 3-wire 9-bit interface</td><td>MDDI_DATAP/N, SDI, SDO</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3-wire 9-bit data Serial interface I</td><td>SDA : In/Out</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data Serial interface II</td><td>SDI : In / SDO : Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data Serial interface I</td><td>SDA : In/Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data Serial interface II</td><td>SDI : In / SDO : Out</td></tr>
</table>
MPU Parallel interface bus and serial interface select
* : Fix this pin at VDD3 or VSS.</td></tr>
<tr><td>RESX (NRESET)</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.</td></tr>
<tr><td>EXTC</td><td>I</td><td>Select to access Level2 command (“Low” : Leve1 only, “High” : Level1 and Level2”)</td></tr>
<tr><td>CSX (NCS)</td><td>I</td><td>Chip select input pin (“Low” enable).
This pin can be permanently fixed “Low” in MPU interface mode only.
* note1,2,3</td></tr>
</table>

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Symbol	I/O	Description
DCX (DNC_SCL)	I	This pin is used to select “Data or Command” in the parallel interface or 4-wire 8-bit serial data interface. When DCX = ’1’, data is selected. When DCX = ’0’, command is selected. This pin is used serial interface clock in 3-wire 9-bit/4-wire 8-bit serial data interface. If not used, this pin should be connected to VDD3 or VSS.
RDX (E) (NRD_E)	I	This pin is used to “Read Clock” in 80-series parallel interface. This pin is used to “Read / Write Clock” in 68-series parallel interface. If not used, this pin should be connected to VDD3.
WRX (RWX) (NWR_RNW)	I	This pin is used to “Write Clock” in 80-series parallel interface. This pin is used to select “Read / Write Operation” in 68-series parallel interface. This pin is used as DCX when 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDD3 or VSS.
DB[17:0]	I/O	When RGB I/F, DB[17:0] are used to RGB interface data bus. When MPU I/F, DB[17:0] are used to MPU parallel interface data bus. If not used, this pin should be connected to VSS.
SDO / SDA	I/O	When IM[3:0] =1001, 1101 or 1111 SDO/SDA pin is used as SDO Output. During this setting, use SDI as input signal for SPI interface. When IM[3:0] =1100 or 1110 SDO/SDA pin is used as bi-directional SDA signal. The input data is sampled at the rising edge of SCL signal. The output data is driven out from the falling edge of SCL signal. If not used, fix this pin at VDD3 or VSS.
SDI	I	Serial input signal. The input data is sampled at the rising edge of SCL signal. If not used, fix this pin at VDD3 or VSS.
TE	O	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	Pixel clock signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
VSYNC	I	Vertical sync. Signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.

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Symbol	I/O	Description
HSYNC	I	Horizontal sync. Signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
ENABLE	I	Data enable signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.

Note.

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.
2. When CSX='1', there is no influence to the parallel and serial interface.

Table 5. Pads for MDDI

Name	I/O	Description
MDP/MDN	I/O	DIFFERENTIAL DATA INPUT/OUTPUT PADS FOR MDDI INTERFACE. IF THE FORWARD LINK ACTIVATES, MDP/MDN RECEIVES DATA FROM THE HOST. IF THE REVERSE LINK ACTIVATES, MDP/MDN TRANSMITS DATA TO THE HOST. IF MDDI IS NOT USED, THIS PAD SHOULD BE FLOATING.
MSP/MSN	I/O	Differential Strobe input pads for MDDI interface. These pads always receive strobe data regardless of the link direction. Also these pads are output pads for MDDI failsafe function. IF MDDI IS NOT USED, THIS PAD SHOULD BE FLOATING.
MDDI_VTEST	I	Test pin for measuring MDDI bias current and forcing external voltage. IF NOT USED, THIS PIN SHOULD BE FLOATING.
MDDI_IREF	I	TEST PIN FOR MEASURING MDDI BIAS CURRENT. IF NOT USED, THIS PIN SHOULD BE FLOATING.

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1.6.3. DRIVER INPUT / OUTPUT PINS

Table 6. Driver Input / Output Pins

Symbol	I/O	Description
S1 ~ S960		Source driver output pads.
G1 ~ G240		Gate driver output pads
VCI1		An internal reference voltage generated between VCI and VSSA. Reference input voltage for 1st and 3rd step up circuit.
AVDD		Output voltage of 1st step up circuit (2 x VCI1). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.
VGH		Positive power output of the 2nd step up circuit. Connect a capacitor for stabilization. Gate “ON” level voltage.
VGL		Negative power output of the 2nd step up circuit. Connect a capacitor for stabilization. To protect IC against Latch up, connect the cathode of the schottky diode to the VSS pad. And the anode of the schottky diode to the VGL pad. Refer to application circuit.
VCL		Power supply for generating VCOM low level. 3rd step up circuit output voltage. Connect a capacitor for stabilization.
C11P/C11M C12P/C12M	~	Connect the charge-pumping capacitor for generating AVDD level.
C21P/C21M C22P/C22M	~	Connect the charge-pumping capacitor for generating VGH, VGL level.
C31P/C31M	~	Connect the charge-pumping capacitor for generating VCL level.
GVDD		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VGS		Low reference voltage for grayscale voltage generator. Connect an external resistor or to system ground.
VCOM		Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.
PWM_OUT		Output pin for PWM(Pulse Width Modulation) signal of LED driving. If not used, open this pad.
BC_CTRL		Output pin for enabling LED driving. If not used, open this pad.

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TEST PINS

Table 7. Test Pins

Symbol	I/O	Description
DUMMYR1 DUMMYR2		Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at VSS level. When measuring an ohmic resistance of the contact, do not apply any power.
TMODE[3:0]	~ -	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
TMUX[2:0]	~ -	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
MDDI_VTEST	~ -	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
VCIR_EXIN	-	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
DUMMY	-	Dummy pin. Leave these pads open.
TREG	I	Input pads used only for test purpose at IC-side During normal operation, connect this PAD to VDD3
OSC	-	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.

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CHAPTER 2

ELECTRICAL SPECIFICATION

2.1 Absolute Maximum Ratings
2.2 DC Electrical Characteristics
2.3 AC Characteristics

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2. ELECTRICAL SPECIFICATIONS

2.1. ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage for logic block	VDD~VSS	-0.3 to 3.3	V
Supply voltage for I/O block	VDD3~VSS	-0.3 to +5.0	V
Supply voltage for step-up circuit	VCC ~VSS	-0.3 to +5.0	V
LCD Supply Voltage range	AVDD ~VSS	-0.3 to +6.5	V
	VGH ~VSS	-0.3 to +22.0	V
	VSS ~VGL	-0.3 to +22.0	V
	VSS ~VCL	-0.3 to +5.0	V
	| VGH – VGL |	-0.3 to +33	V
Input Voltage range	Vin	-0.3 to VDD3+0.5	V
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +110	°C

Note.

1. The absolute maximum rating is the limit value. When the IC is exposed to the operating environment beyond this range, the IC does not assure normal operations and may be damaged permanently, not be able to be recovered.
2. The operating temperature is the range of device-operating temperature. They do not guarantee chip performance.

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CAUTION

Stresses above these absolute maximum ratings may cause permanent damage. These are stress ratings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability.

2.2. DC ELECTRICAL CHARACTERISTICS

Table 9. DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Pin
Power voltage(1)	VDD3		1.65	1.8	3.3	V	VDD3
Power voltage(2)	VCC		2.4	~	3.3	V	VCC
LCD driving voltage	AVDD		4.2		6.0	V	AVDD
	VGH		8.4		16.5	V	VGH
	VGL		-15		-6.3	V	VGL
	VGH-VGL				30.0	V	VGH, VGL
	VCL		-3		-2.1	V	VCL
	VCI-VCL				6.0	V	VCI, VCL
	GVDD		3.26		5.0	V	GVDD
High Level Input Voltage	VIH		0.7VDD3		VDD3	V	All input pins
Low Level Input Voltage	VIL		0.0		0.3VDD3	V	All input pins
High Level Output Voltage	VOH	IOH ~ 0.5mA	0.8VDD3		VDD3	V	DB[23:0], TE
Low Level Output Voltage	VOL	IOH ~ 0.5mA	0.0		0.2VDD3	V	DB[23:0], TE
Input Current	ILI1	GND ≤ VIN ≤ VDD3	-1.0		1.0	uA	CSX,RDX,WRX, DB[23:0],& RESX
Output voltage deviation (Mean value)	ΔVo	GVDD-0.8 ≤ Vso	~	~	±55	mV	S[1:960]
		VSS+0.8 < Vso < GVDD-0.8	~	~	±25		
		Vso ≤ VSS + 0.8	~	~	±55		
Sleep In Current	IDD_{SI}_VDD3	VIN=VDD3,VCI,GND Ta=25℃	~	~	25	uA	VSS
	IDD_{SI}_VCI		~	~	5	uA	VSS
Operating Current 1	IDD_{OP1}_VDD3	10MHz Memory Access. (VCI=2.8v,VDD3=1.8v Load=100pf. Ta=25℃)	~		*1.8	mA	
	IDD_{OP1}_VCI	10MHz Memory Access	~		8.8	mA	

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Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Pin
		(VCI=2.8v,VDD3=1.8v Load=100pf. Ta=25℃)					
Operating Current 2	IDD_{OP2}_ VDD3	Memory Not Access (VCI=2.8v,VDD3=1.8v Load=100pf. Ta=25℃)	~		*500	uA	
	IDD_{OP2}_VCI	Memory Not Access (VCI=2.8v,VDD3=1.8v Load=100pf. Ta=25℃)	~		8.8	mA	
Internal Oscillator frequency	Fosc1	Frame freq. = 60 Hz Display line = 240 Ta = 25℃	8.1	9	9.9	MHz	
Step-up output efficiency	AVDD	ILOAD = 4 mA	90	95	~	%	
	VGH	ILOAD = 0.1 mA	90	95	~	%	
	VGL	ILOAD = 0.1 mA	90	95	~	%	
	VCL	ILOAD = 0.3 mA	90	95	~	%	
LCD Gate driver output On resistance	Ronvgh	VGH = 8.4V VGL = 6.3V	~	~	7	kΩ	
	Ronvgl		~	~	7	kΩ	
LCD source driver output On resistance	Ronp	AVDD = 4.5V VSSA = 0V	~	~	30	kΩ	
	Ronn		~	~	30	kΩ	
LCD Binary driver Output On resistance	Ronpb	GVDD = 4.5V VSSA = 0V	~	~	300	kΩ	
	Ronnb		~	~	300	kΩ	

Note.

Ta = -40℃ to +85℃ (to +85℃ no damage)

..: Don't applied to MIE function

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2.3. AC CHARACTERISTEICS

2.3.1. 80-SERIES 8/ 9/ 16/ 18 BIT PARALLEL INTERFACE

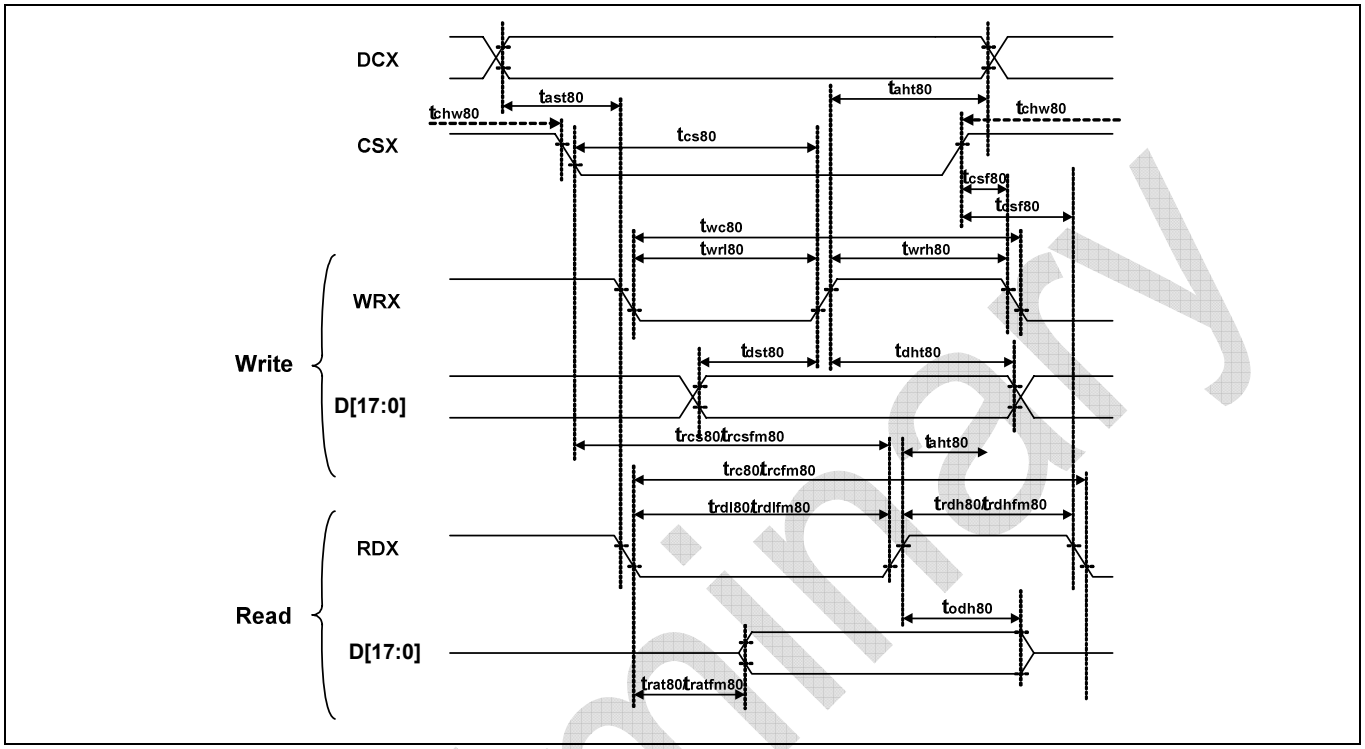

Figure7. 80-Series Parallel Interface

Table 10. AC Characteristics of 80-Series Parallel Interface

Signal	Parameter	Symbol	Min	Max	Unit	Description
DCX	DCX setup time	tast80	0	~	ns	
	DCX hold time	taht80	10	~	ns	
CSX	CSX “H” pulse width	tchw80	0	~	ns	
	Chip select setup time(write)	tcs80	15	~	ns	
	Chip select setup time (Read ID)	trcs80	45	~	ns	
	Chip select setup time (Read FM)	trcsfm80	355	~	ns	
	Chip select wait time(write/read)	tcsf80	10	~	ns	
WRX	Write cycle	twc80	66	~	ns	
	Control pulse H duration	twrh80	15	~	ns	
	Control pulse L duration	twrl80	15	~	ns	
RDX(ID)	Read cycle	trc80	160	~	ns	When read ID data
	Control pulse H duration	trdh80	90	~	ns	
	Control pulse L duration	trdl80	45	~	ns	

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Signal	Parameter	Symbol	Min	Max	Unit	Description
RDX(FM)	Read cycle	trcfm80	450	~	ns	When read from frame memory
	Control pulse H duration	trdhfm80	90	~	ns	
	Control pulse L duration	trdlfm80	355	~	ns	
D[17:0]	Write data setup time	tdst80	10	~	ns	For maximum CL = 30 pF For minimum CL = 8 pF
	Write data hold time	tdht80	10	~	ns	
	Read access time	trat80	~	40	ns	
	Read access time (FM)	tratfm80	~	340	ns	
	Read output disable time	todh80	20	80	ns	

Note.

Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V, VSS=0V

Preliminary

2.3.2. 68-SERIES 8/ 9/ 16/ 18 BIT PARALLEL INTERFACE

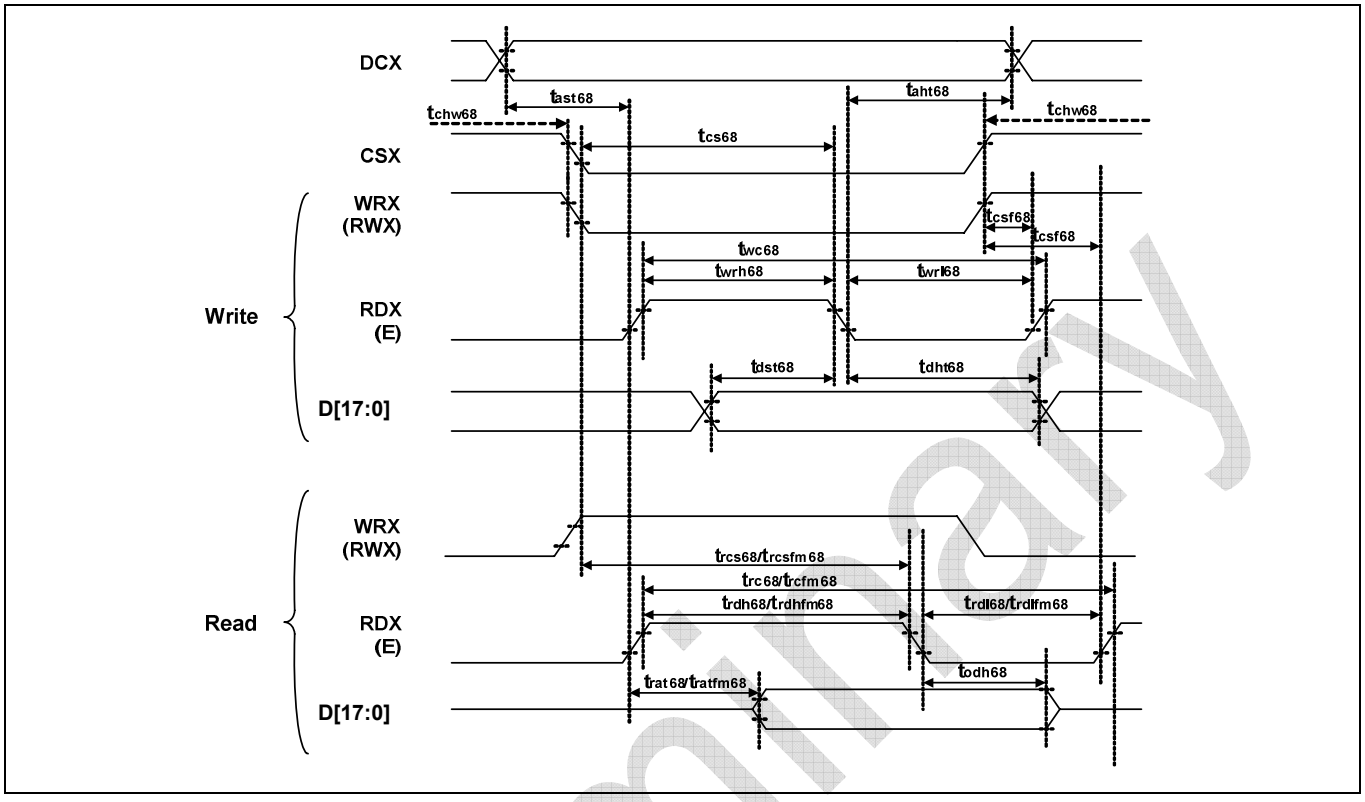

Figure8. 68-Series Parallel Interface

Table 11. AC Characteristics of 68-Series Parallel Interface

Signal	Parameter	Symbol	Min	Max	Unit	Description
DCX	DCX setup time	tast68	0	~	ns	
	DCX hold time	taht68	10	~	ns	
CSX	CSX “H” pulse width	tchw68	0	~	ns	
	Chip select setup time(write)	tcs68	15	~	ns	
	Chip select setup time (Read ID)	trcs68	45	~	ns	
	Chip select setup time (Read FM)	trcsfm68	355	~	ns	
	Chip select wait time(write/read)	tcsf68	10	~	ns	
WRX	Write cycle	twc68	66	~	ns	
	Control pulse H duration	twrh68	15	~	ns	
	Control pulse L duration	twrl68	15	~	ns	
RDX(ID)	Read cycle	trc68	160	~	ns	When read ID data
	Control pulse H duration	trdh68	90	~	ns	
	Control pulse L duration	trdl68	45	~	ns	
RDX(FM)	Read cycle	trcfm68	450	~	ns	When read

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Signal	Parameter	Symbol	Min	Max	Unit	Description
	Control pulse H duration	trdhfm68	90	~	ns	from frame memory
	Control pulse L duration	trdlfm68	355	~	ns	
DB[17:0]	Write data setup time	tdst68	10	~	ns	For maximum CL = 30 pF For minimum CL = 8 pF
	Write data hold time	tdht68	10	~	ns	
	Read access time	trat68	~	40	ns	
	Read access time (FM)	tratfm68	~	340	ns	
	Read output disable time	todh68	20	80	ns	

Note.

Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V, VSS=0V

Preliminary

2.3.3. 3-WIRE 9-BIT SERIAL INTERFACE

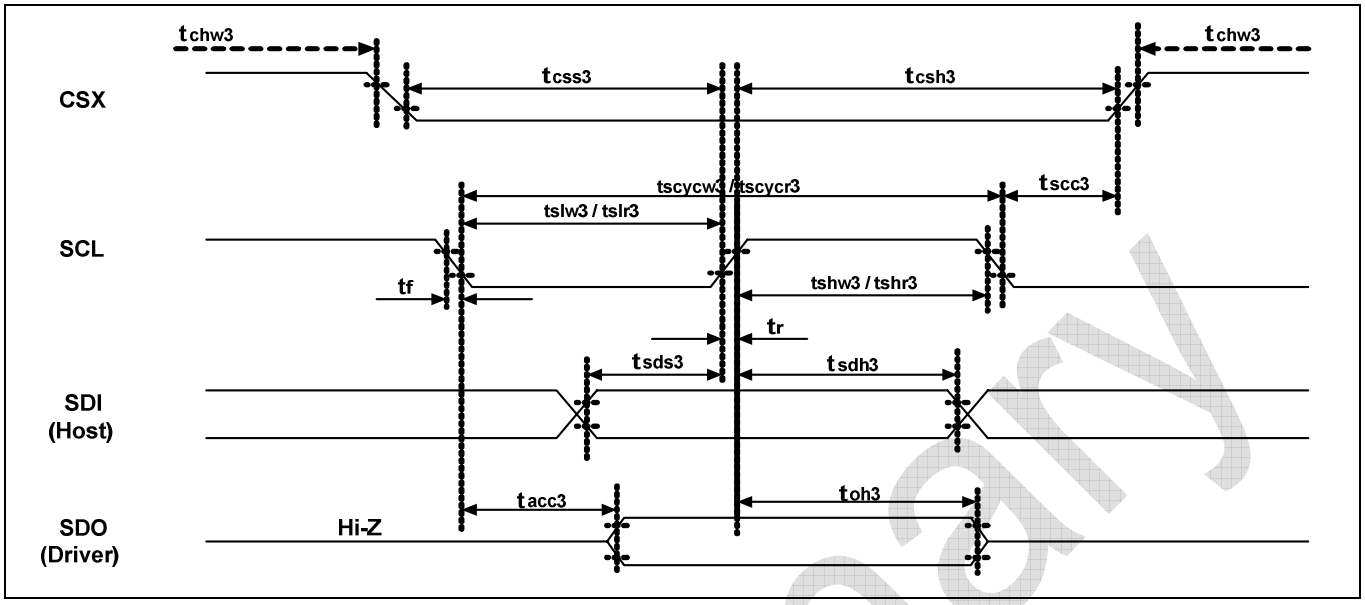

Figure9. 3-Wire 9-Bit Serial Interface

Table 12. AC Characteristics of 3-Wire 9-Bit Serial Interface

Parameter	Symbol	Conditions	Min	Max	Unit
Serial Clock Cycle(Write)	tscycw3	SCL	100	~	ns
SCL "H" pulse width(Write)	tshw3	SCL	35	~	ns
SCL "L" pulse width(Write)	tslw3	SCL	35	~	ns
Data setup time(Write)	tsds3	SDA	30	~	ns
Data hold time(Write)	tsdh3	SDA	30	~	ns
Serial Clock Cycle(Read)	tscycr3	SCL	150	~	ns
SCL "H" pulse width(Read)	tshr3	SCL	60	~	ns
SCL "L" pulse width(Read)	tslr3	SCL	60	~	ns
Access time	tacc3	SDO (Note2)	10	50	ns
Output disable time	toh3	SDO (Note2)	15	50	ns
CSX "H" pulse width	tchw3	CSX	40	~	ns
CSX-SCL time	tcss3	CSX(Write)	60	~	ns
	tcsh3	CSX(Write)	65	~	ns

Note.

1. Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V, VSS=0V
2. For maximum CL = 30 pF, for minimum CL = 8 pF

Preliminary

2.3.4. 4-WIRE 8-BIT SERIAL INTERFACE

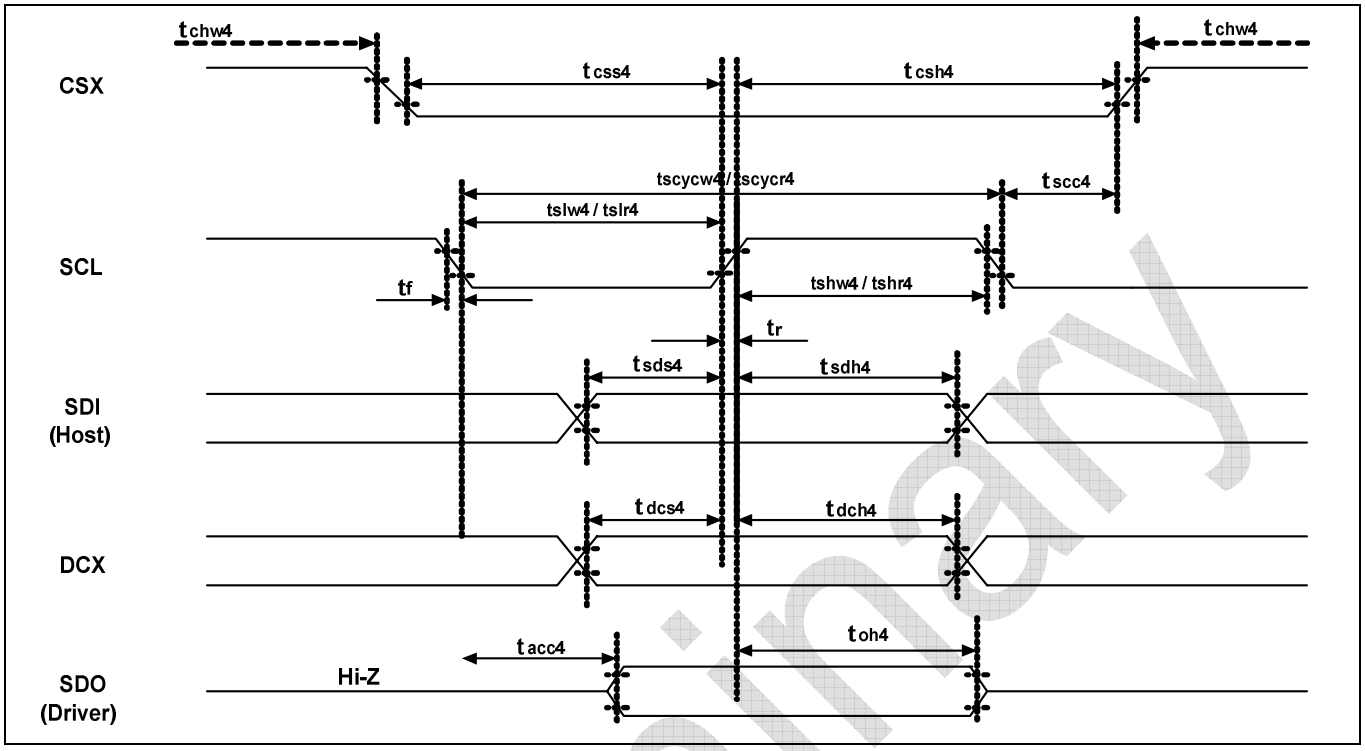

Figure10. 4-Wire 8-Bit Serial Interface

Table 13. AC Characteristics of 4-Wire 8-Bit Serial Interface

Parameter	Symbol	Conditions	Min	Max	Unit
Serial Clock Cycle(Write)	tscycw4	SCL	100	~	ns
SCL ”H” pulse width(Write)	tshw4	SCL	35	~	ns
SCL ”L” pulse width(Write)	tslw4	SCL	35	~	ns
Data setup time(Write)	tsds4	SDA	30	~	ns
Data hold time(Write)	tsdh4	SDA	30	~	ns
DCX setup time	tdcs4	DCX	30	~	ns
DCX hold time	tdch4	DCX	30	~	ns
Serial Clock Cycle(Read)	tscycr4	SCL	150	~	ns
SCL ”H” pulse width(Read)	tshr4	SCL	60	~	ns
SCL ”L” pulse width(Read)	tslr4	SCL	60	~	ns
Access time	tacc4	SDO (Note2)	10	50	ns
Output disable time	toh4	SDO (Note2)	15	50	ns
CSX “H” pulse width	tchw4	CSX	40	~	ns
CSX-SCL time(Write)	tcss4	CSX	60	~	ns
	tcsh4	CSX	65	~	ns

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Note.

1. Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V, VSS=0V
2. Note2. For maximum CL = 30 pF, for minimum CL = 8 pF

Preliminary

2.3.5. RGB INTERFACE CHARACTERISTICS

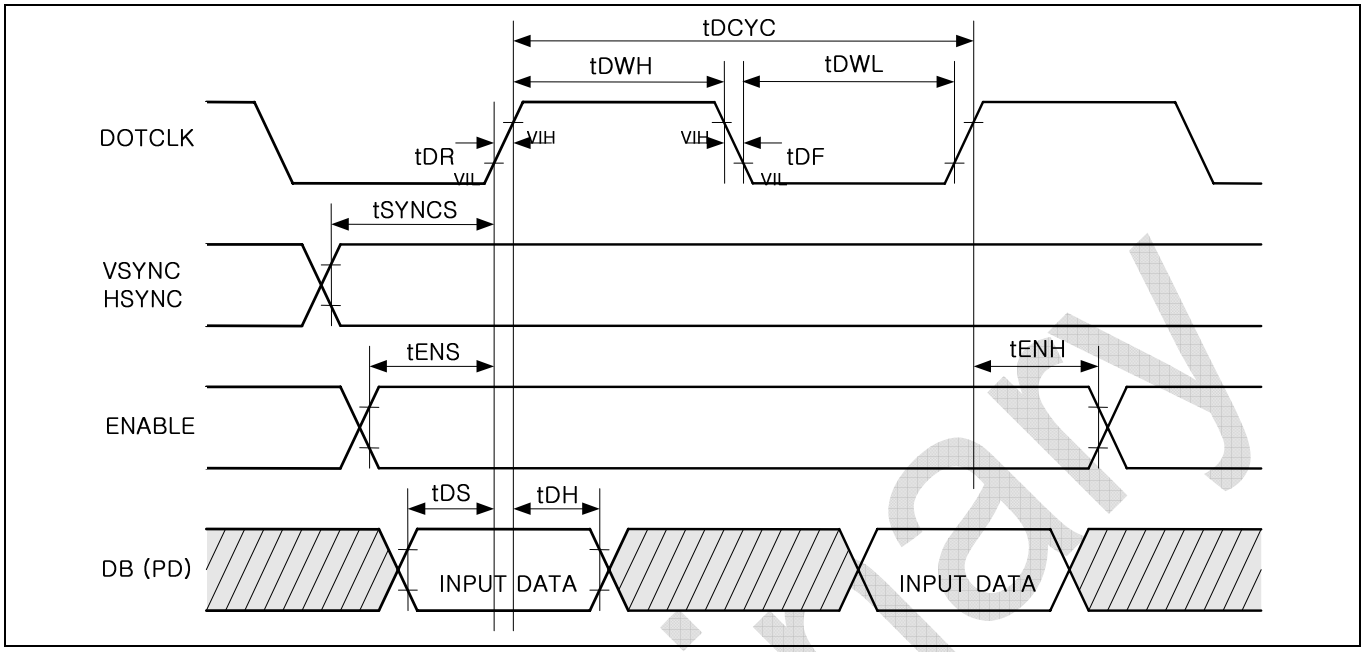

Figure11. RGB Interface

Table 14. RGB Interface AC Characteristics

(Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V)

Parameter	Description	Min	Max	Unit
tDCYC	DOTCLK period	100	~	ns
tDWL	DOTCLK pulse width low	50	~	ns
tDWH	DOTCLK pulse width high	50	~	ns
tDR / tDF	DOTCLK rising / falling time	~	20	ns
tSYNCS	VSYNC, HSYNC setup	30	~	ns
tENS	ENABLE setup	50	~	ns
tENH	ENABLE hold	50	~	ns
tDS	Input Data setup	50	~	ns
tDH	Input Data hold	50	~	ns

Note.

1. VSYNC Low Pulse Width ≥1H
2. HSYNC Low Pulse Width ≥ 1 DOTCLK

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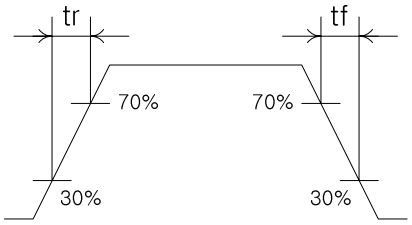

Figure12. Rising and Falling

Note.

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

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2.3.6. TACC, TODH MEASUREMENT CONDITION

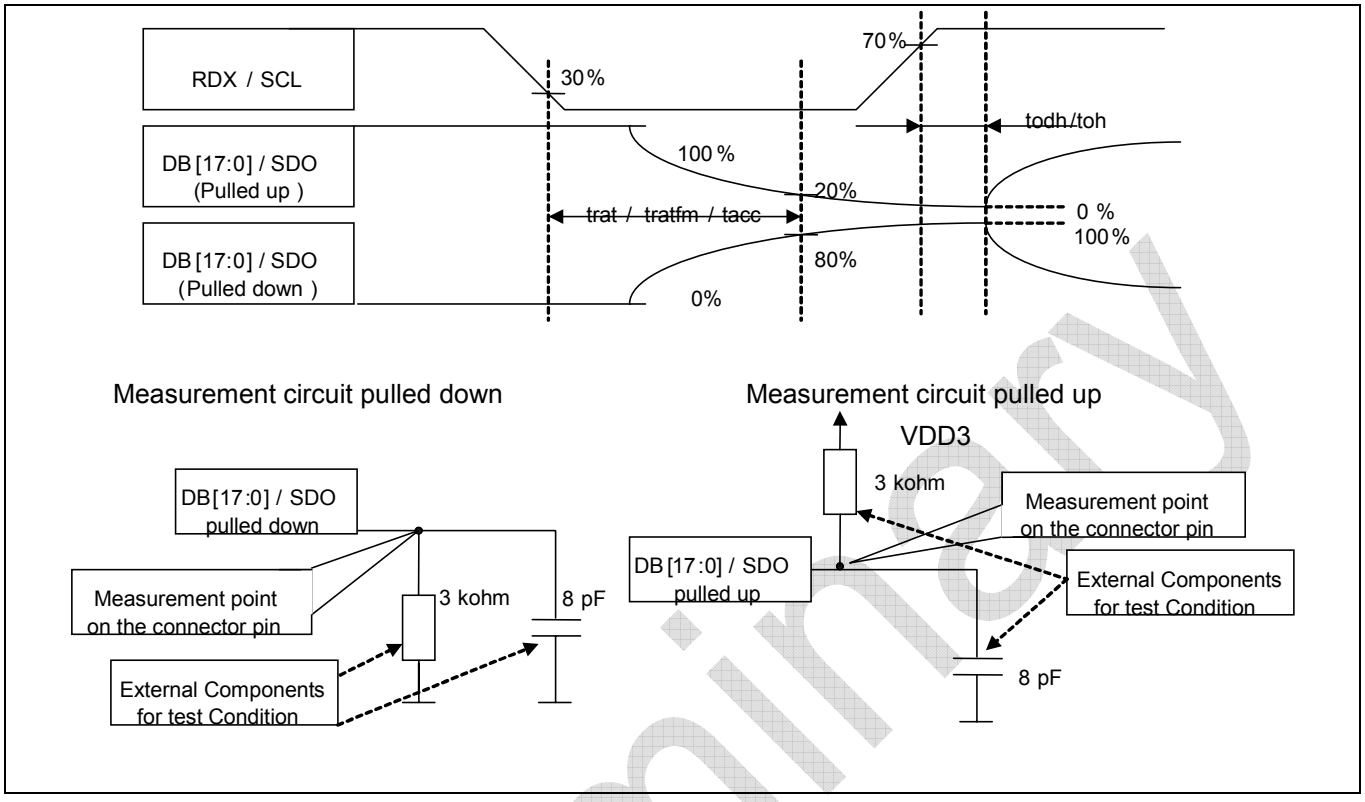

Figure13. Minimum Measurement Condition

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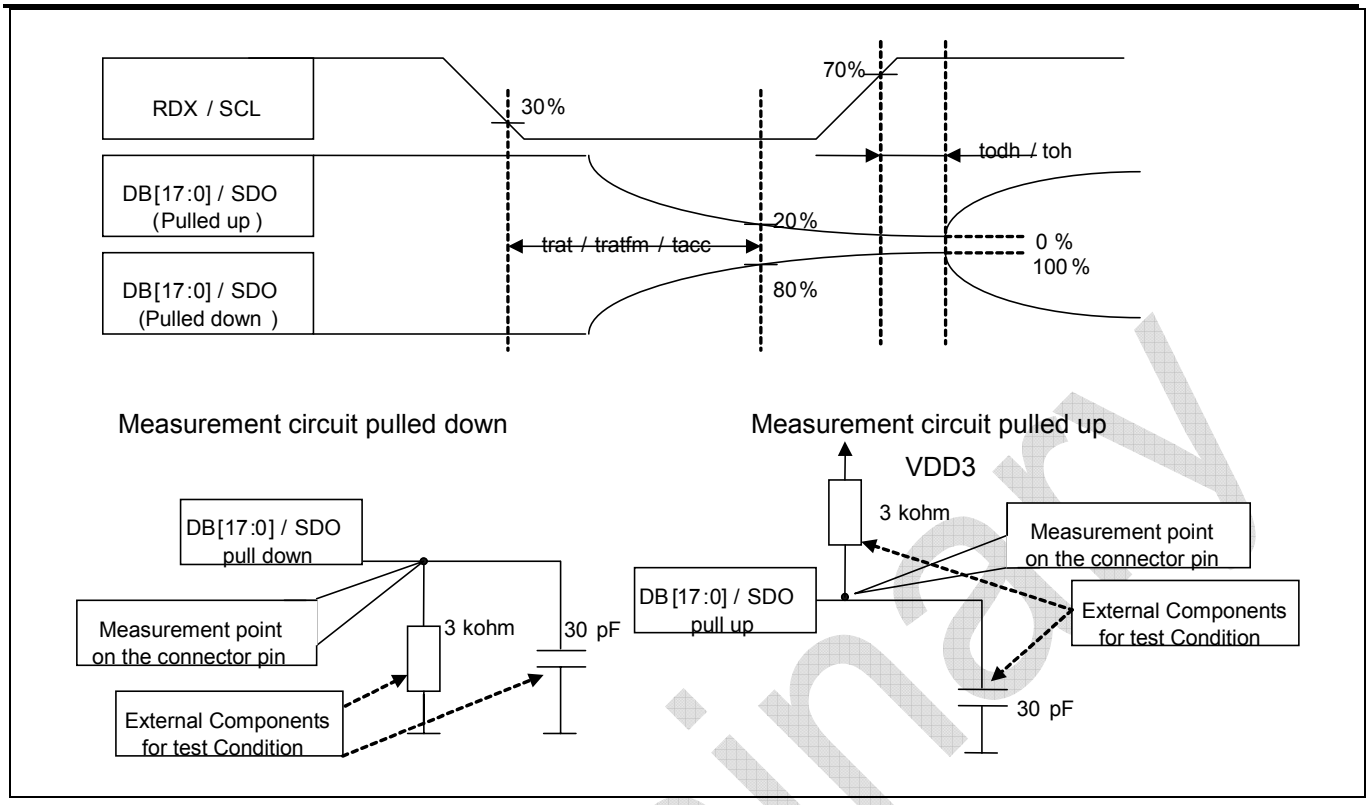

Figure14. Maximum Measurement Condition

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2.3.7. RESET TIMING

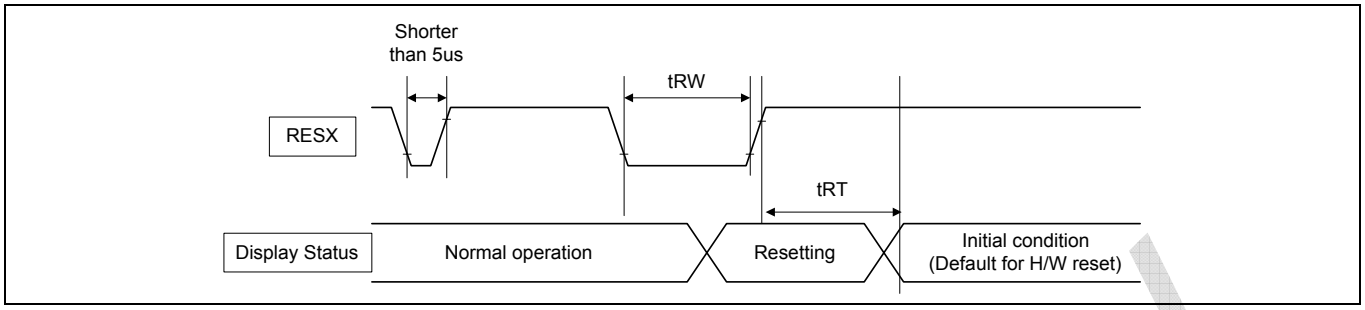

Figure15. Reset Timing

Table 15. Reset Input Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10	~	us
	tRT	Reset cancel	~	5 (note 5)	ms
			~	120 (note 6, 7)	ms

Note.

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

Table 16. Reset Operation According to Resx Pulse Width

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.

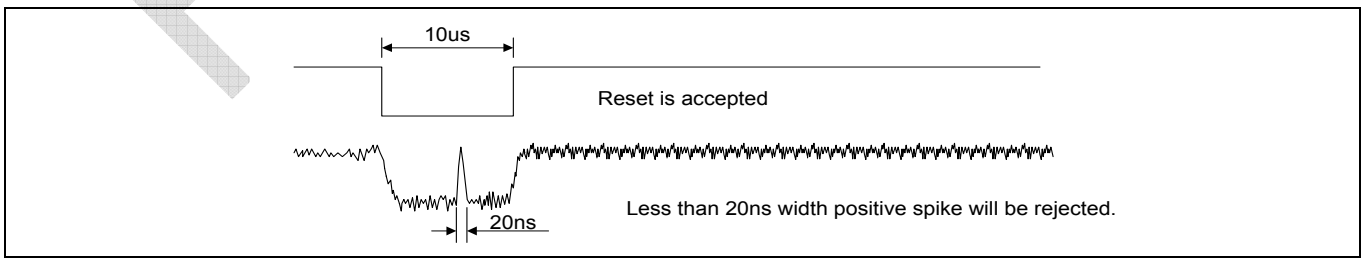

Figure16. Spike Rejection

4. Spike Rejection also applies during a valid reset pulse as shown below:

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5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also, Sleep Out command cannot be sent for 120msec.

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2.4. MDDI CHARACTERISTEICS

2.4.1. DC CHARACTERISTICS

Data/Strobe Rx DC characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal shall be interpreted as a logic-one level.			50	mV	
V_{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as logic-zero level.	-50			mV	
V_{IT+}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal shall be interpreted as a logic-one level.		125	175	mV	
V_{IT-}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Below this differential voltage the input signal shall be interpreted as logic-zero level.	75	125		mV	
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0		1.65	V	
R_{term}	Parallel termination resistance value	98	100	102	Ω	

Driver electrical DC characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
$I_{diffabs}$	Absolute driver differential output current range (Current through the termination resistor)	2.5		4.5	mA	Rterm= 100 Ω
$V_{out-rng-int}$	Single-ended driver output voltage range with respect to ground, internal mode	0.35		1.60	V	Under all conditions, including double-drive

Note: Please refer to VESA specification Ver 1.0

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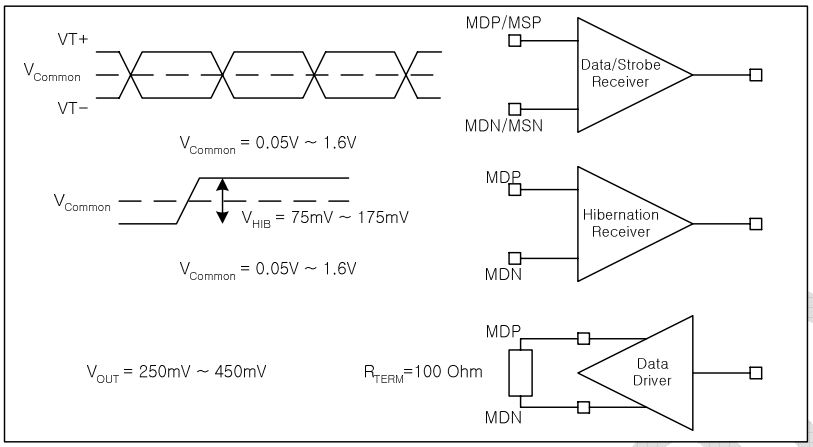
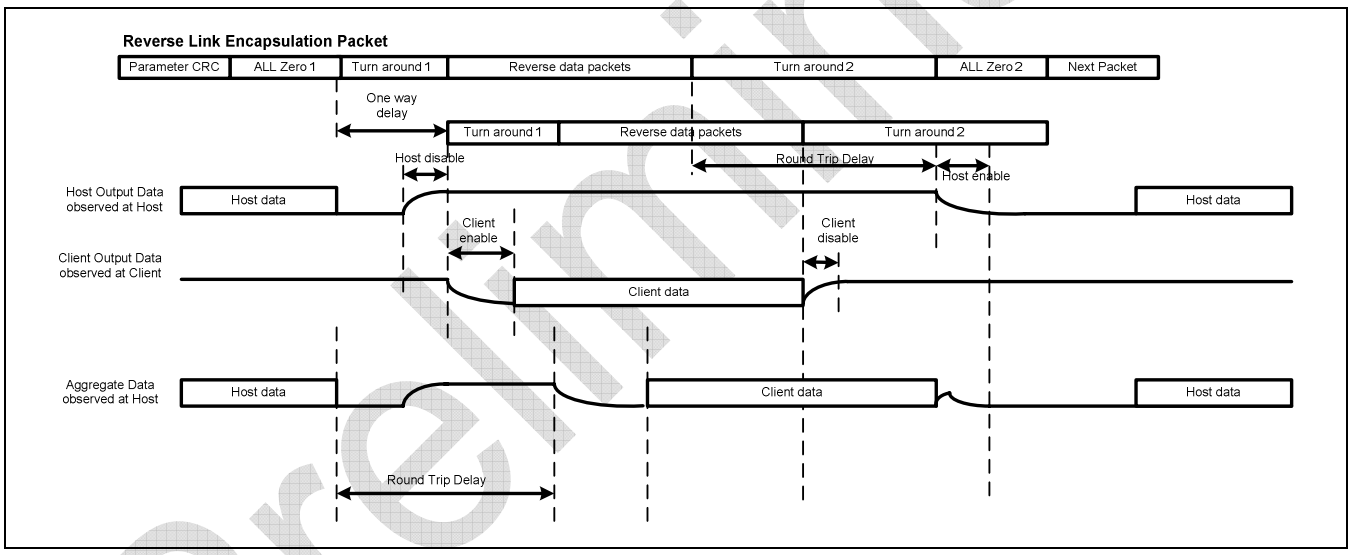


MDDI receiver, driver electrical diagram



Host enable/disable time and client enable/disable time diagram

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2.4.2. AC CHARACTERISTICS

Receiver AC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit
$T_{host\text{-}enable}$	Host output enable time	0		$24*t_{BIT}$	ns
$T_{host\text{-}disable}$	Host output disable time, entire length of the Turn-Around 1 field	0		$24*t_{BIT}$	ns
$T_{client\text{-}enable}$	Client output enable time, entire length of the Turn-Around 1 field	0		$24*t_{BIT}$	Ns
$T_{client\text{-}disable}$	Client output disable time, measured from the end of the last bit of the Turn-Around 2 field	0		$24*t_{BIT}$	ns

Note, tBIT= 1 / Link_Data_Rate, where Link_Data_Rate is the bit rate of a single data pair.

(For example, if the average forward link bit rate is 150Mbps, then tBIT= 1 / 150Mbps = 6.6ns)

These specifications are from VESA specification Ver 1.0.

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CHAPTER 3

INTERFACE

3.1 MPU Interface
3.2 Interface Description
3.3 Display Data Format
3.4 RGB Interface
3.5 VSYNC Interface
3.6 MDDI Interface

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3. INTERFACE

3.1. MPU INTERFACE

3.1.1. INTERFACE TYPE SELECTION

Selection of given interfaces are set by IM[3], IM[2], IM[1], and IM[0] pins as shown below.

Table 17. Interface Type Selection

IM[3]	IM[2]	IM[1]	IM[0]	Interface	Description
0	0	0	0	68 MCU 8-bit Parallel I/F	8bit read display data and 8bit read parameter
0	0	0	1	68 MCU 9-bit Parallel I/F	9bit read display data and 8bit read parameter
0	0	1	0	68 MCU 16-bit Parallel I/F	16bit read display data and 8bit read parameter
0	0	1	1	68 MCU 18-bit Parallel I/F	18bit read display data and 8bit read parameter
0	1	0	0	80 MCU 8-bit Parallel I/F	8bit read display data and 8bit read parameter
0	1	0	1	80 MCU 9-bit Parallel I/F	9bit read display data and 8bit read parameter
0	1	1	0	80 MCU 16-bit Parallel I/F	16bit read display data and 8bit read parameter
0	1	1	1	80 MCU 18-bit Parallel I/F	18bit read display data and 8bit read parameter
1	0	0	1	MDDI + spi 3-wire 9-bit interface	MDDI interface with Serial interface (Only for hibernation mode)
1	1	0	0	3-wire 9-bit data Serial interface I	8bit command and 8 / 24 / 32bit parameter
1	1	0	1	3-wire 9-bit data Serial interface II	8bit command and 8 / 24 / 32bit parameter
1	1	1	0	4-wire 8-bit data Serial interface I	8bit command and 8 / 24 / 32bit parameter
1	1	1	1	4-wire 8-bit data Serial interface II	8bit command and 8 / 24 / 32bit parameter

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3.1.2. PIN DESCRIPTION

MPU interface is changed according to the bus width used. The pin assignment is listed in the table below.

3.1.2.1. 3-Wire 9-bit serial interface

Pin Name	Description
CSX (NCS)	Chip select signal
SCL (DNC_SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of DCX (SCL) signal.
SDA (SDI)	Serial input/output data
DB[17:0]	Display Data of RGB Interface

3.1.2.2. 4-Wire 8-bit serial interface

Pin Name	Description
CSX (NCS)	Chip select signal
DCX (NWR_RNW)	Data is regard as a command when DCX is low. Data is regard as a parameter or a display data when DCX is high.
SCL (DNC_SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of WRX signal.
SDA (SDI)	Serial input/output data
DB[17:0]	Display Data of RGB Interface

3.1.2.3. 3-Wire 9-bit serial interface

Pin Name	Description
CSX (NCS)	Chip select signal
SCL (DNC_SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of DCX (SCL) signal.
SDI	Serial input data
SDO	Serial output data
DB[17:0]	Display Data of RGB Interface

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3.1.2.4. 4-Wire 8-bit serial interface

Pin Name	Description
CSX (NCS)	Chip select signal
DCX (NWR_RNW)	Data is regard as a command when DCX is low. Data is regard as a parameter or a display data when DCX is high.
SCL (DNC_SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of WRX signal.
SDI	Serial input data
SDO	Serial output data
DB[17:0]	Display Data of RGB Interface

3.1.2.5. 80-Series parallel interface

Pin Name	Description
CSX (NCS)	Chip select signal
DCX (DCX_SCL)	Data bus is regard as a command when DCX is low. Data bus is regard as a parameter or a display data when DCX is high.
RDX/E (NRD_E)	Clock for read operation. When RDX is low, the data bus held on output state.
WRX (NWR_RNW)	Clock for write operation. The data is latched on the rising edge of WRX.
DB[17:0]	Data bus Interface / DB Pins 8-bit Parallel Interface / DB17-DB8 : unused, DB7-DB0 : 8-bit data 16-bit Parallel Interface / DB17-DB16 : unused, DB15-DB0 : 16-bit data 9-bit Parallel Interface / DB17-DB9 : unused, DB8-DB0 : 9-bit data 18-bit Parallel Interface / DB17-DB0 : 18-bit data If not used, fix this pin to VSS.

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3.1.2.6. 68-Series parallel interface

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>CSX (NCS)</td><td>Chip select signal</td></tr>
<tr><td>DCX (DCX_SCL)</td><td>Data bus is regard as a command when DCX is low.
Data bus is regard as a parameter or a display data when DCX is high.</td></tr>
<tr><td>RDX/E (NRD_E)</td><td>Clock for read / write operation</td></tr>
<tr><td>WRX (NWR_RNW)</td><td>Read / write selection signal (Read: High / Write: Low)</td></tr>
<tr><td>DB[17:0]</td><td>Data bus
<table>
<tr><th>Interface</th><th>DB Pins</th></tr>
<tr><td>8-bit Parallel Interface</td><td>DB17-DB8: unused, DB7-DB0 : 8-bit data</td></tr>
<tr><td>16-bit Parallel Interface</td><td>DB17-DB16: unused, DB15-DB0 : 16-bit data</td></tr>
<tr><td>9-bit Parallel Interface</td><td>DB17-DB9: unused, DB8-DB0 : 9-bit data</td></tr>
<tr><td>18-bit Parallel Interface</td><td>DB17-DB0: 18-bit data</td></tr>
</table>
If not used, fix this pin to VSS.</td></tr>
</table>

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3.1.3. INPUT / OUTPUT PIN ASSIGNMENT

The block diagrams for MPU interface are illustrated below.

3.1.3.1. 3-Wire 9-bit serial interface I

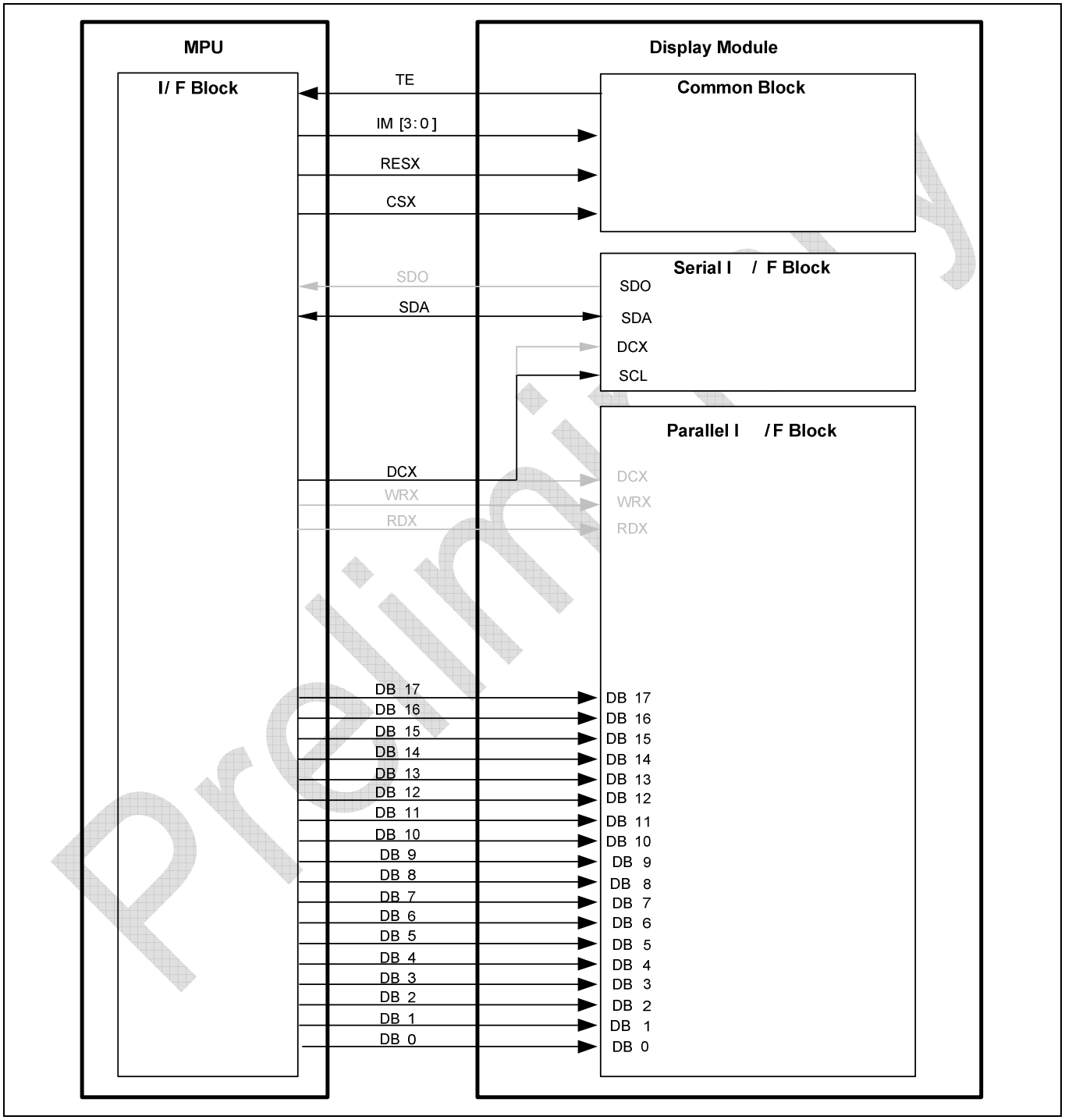

Figure17. 3-Wire 9-Bit Serial Interface I(RGB 18-Bit I/F)

3.1.3.2. 4-Wire 8-bit serial interface I

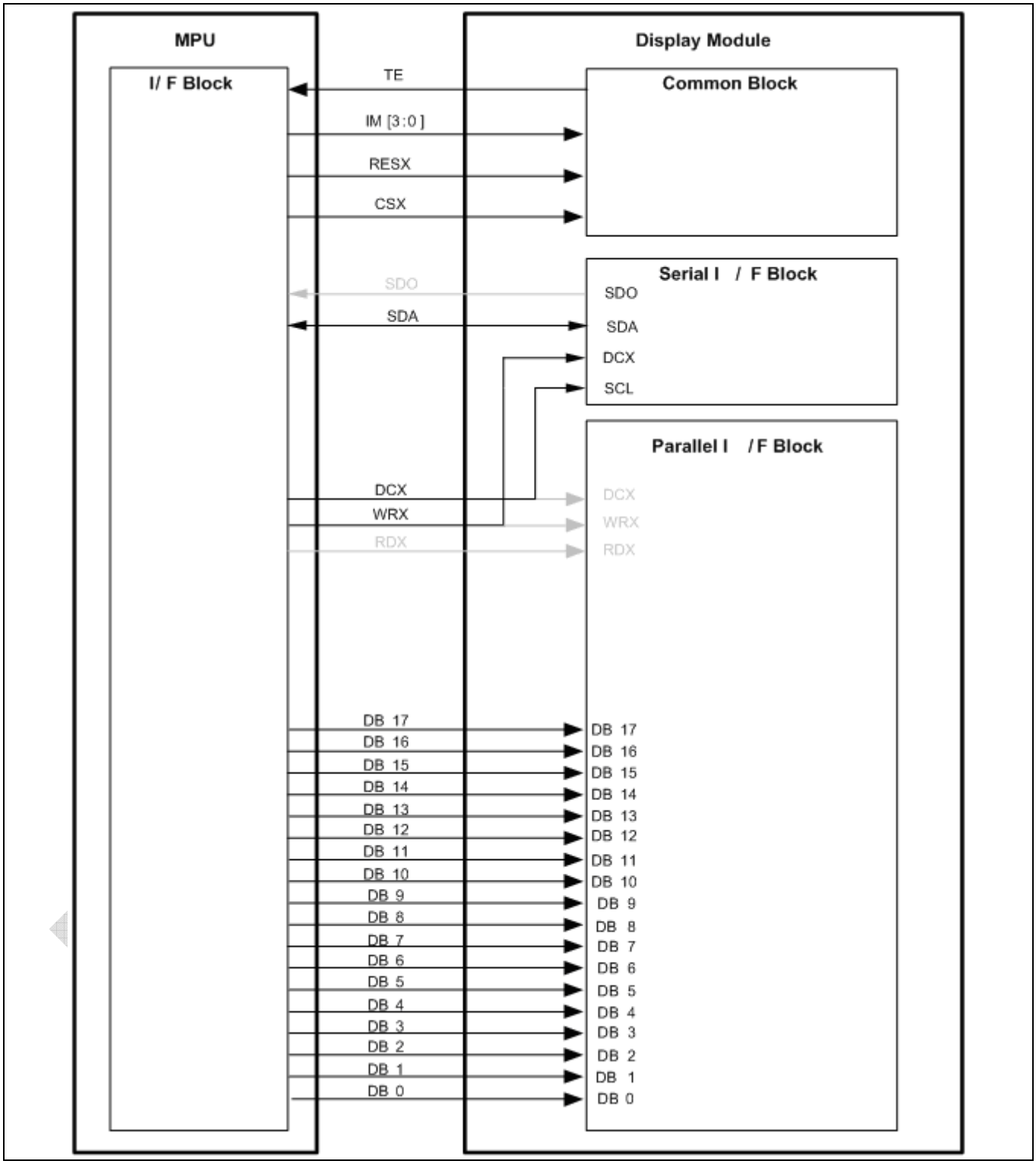

Figure18. 4-Wire 8-Bit Serial Interface I (RGB 18-Bit I/F)

3.1.3.3. 3-Wire 9-bit serial interface II

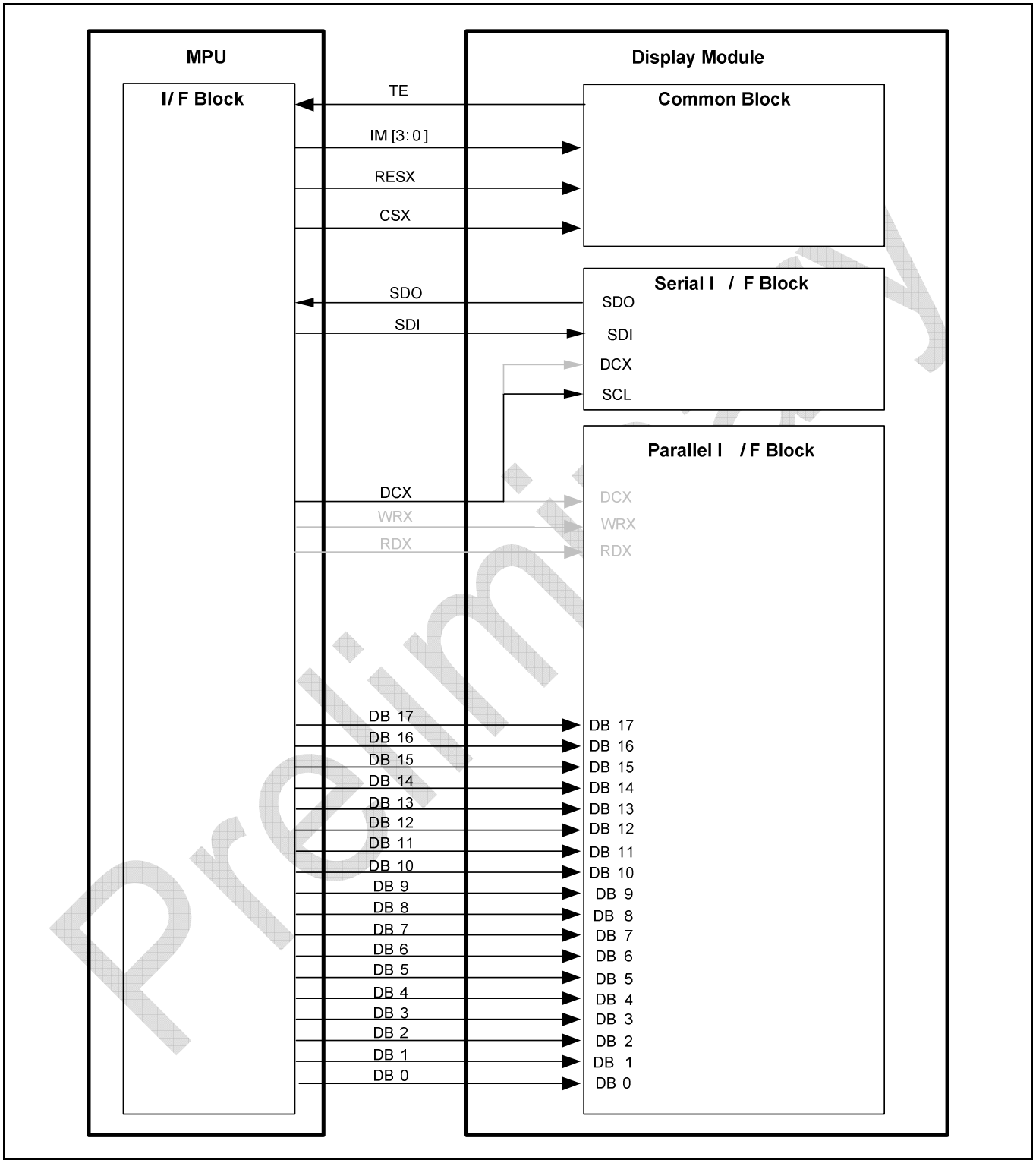

Figure19. 3-Wire 9-Bit Serial Interface II (RGB 18-Bit I/F)

3.1.3.4. 4-Wire 8-bit serial interface II

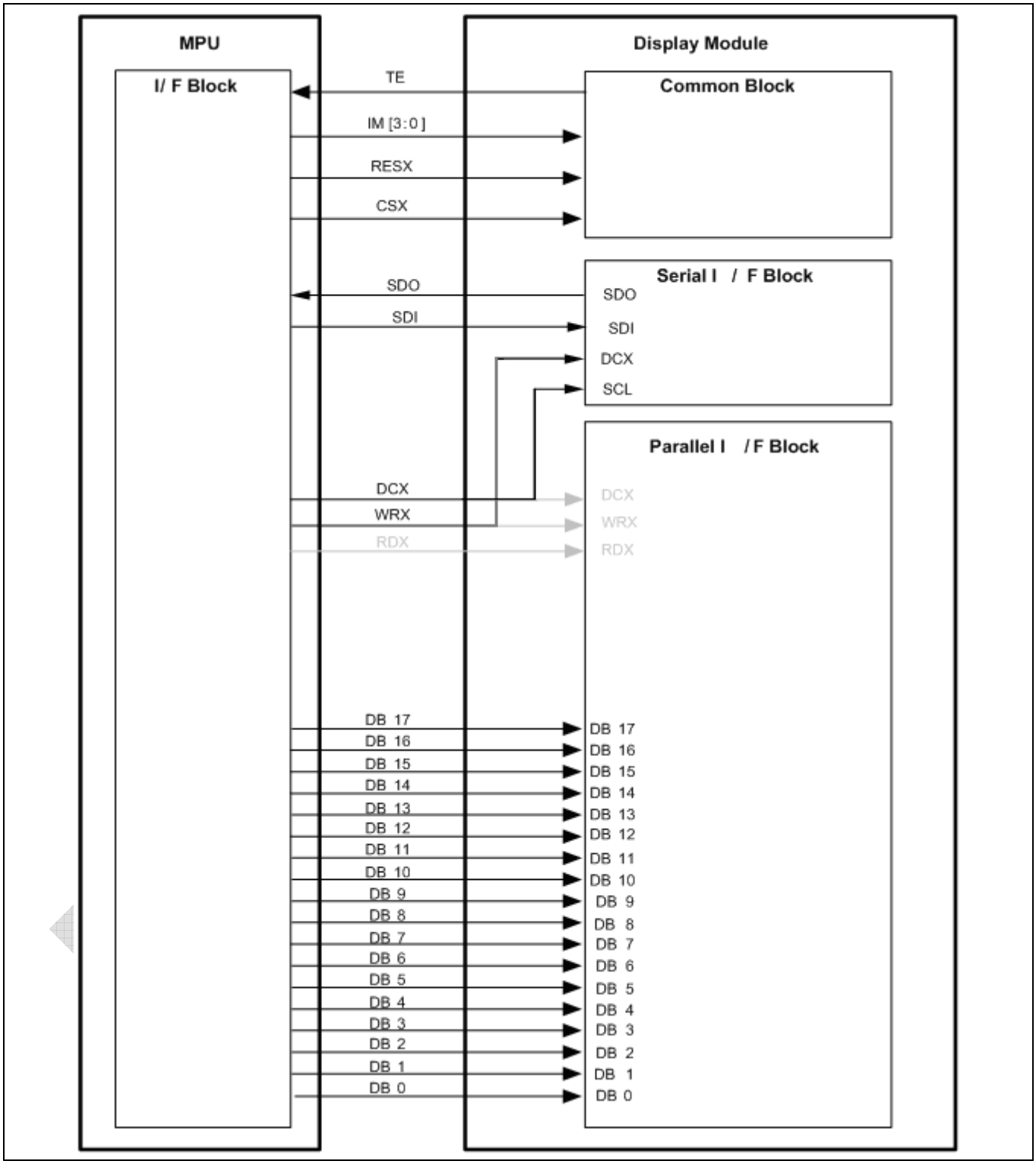

Figure20. 4-Wire 8-Bit Serial Interface II (RGB 18-Bit I/F)

3.1.3.5. 80-Series parallel interface

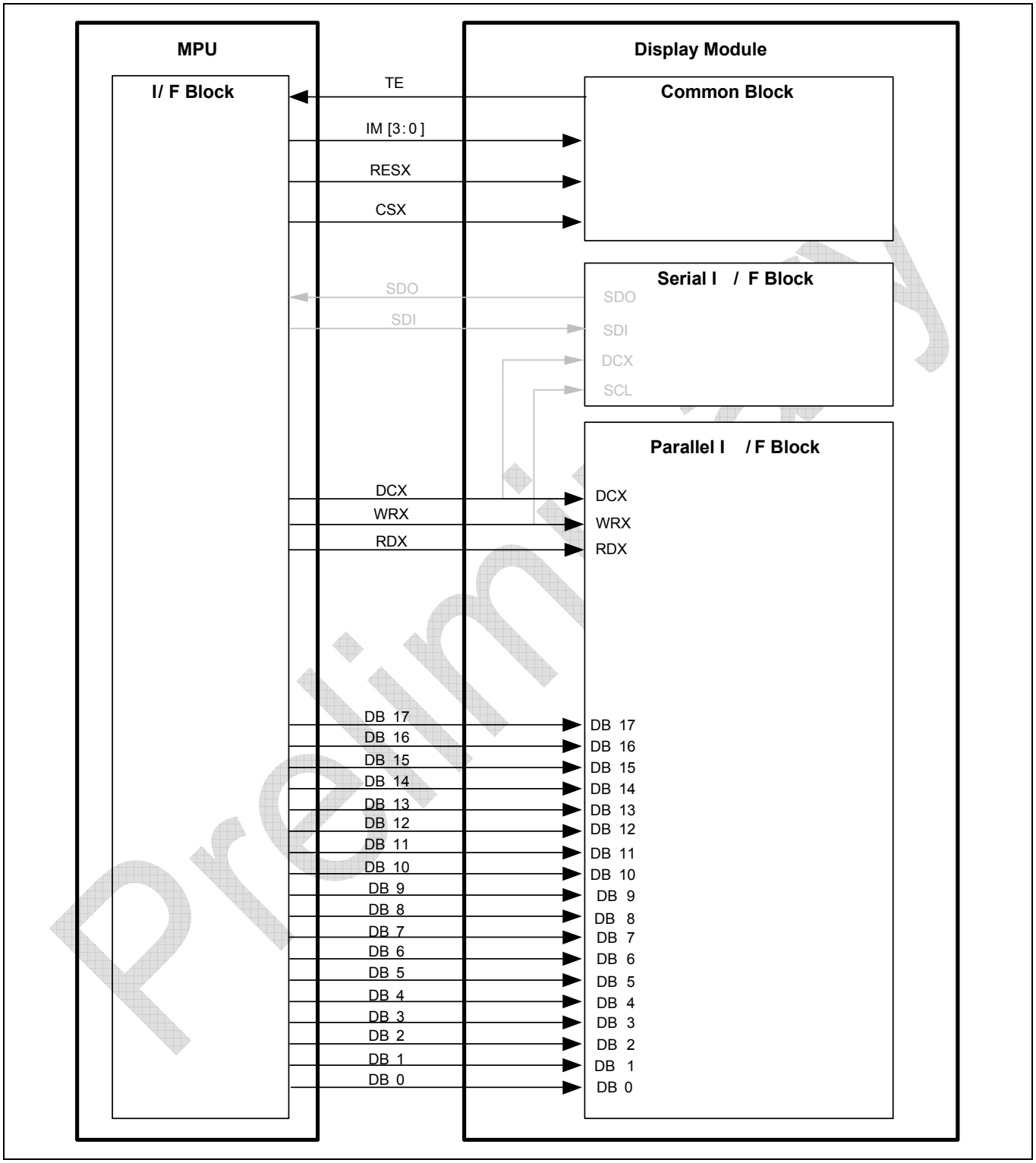

Figure21. 80-Series Parallel Interface

3.1.3.6. 68-Series parallel interface

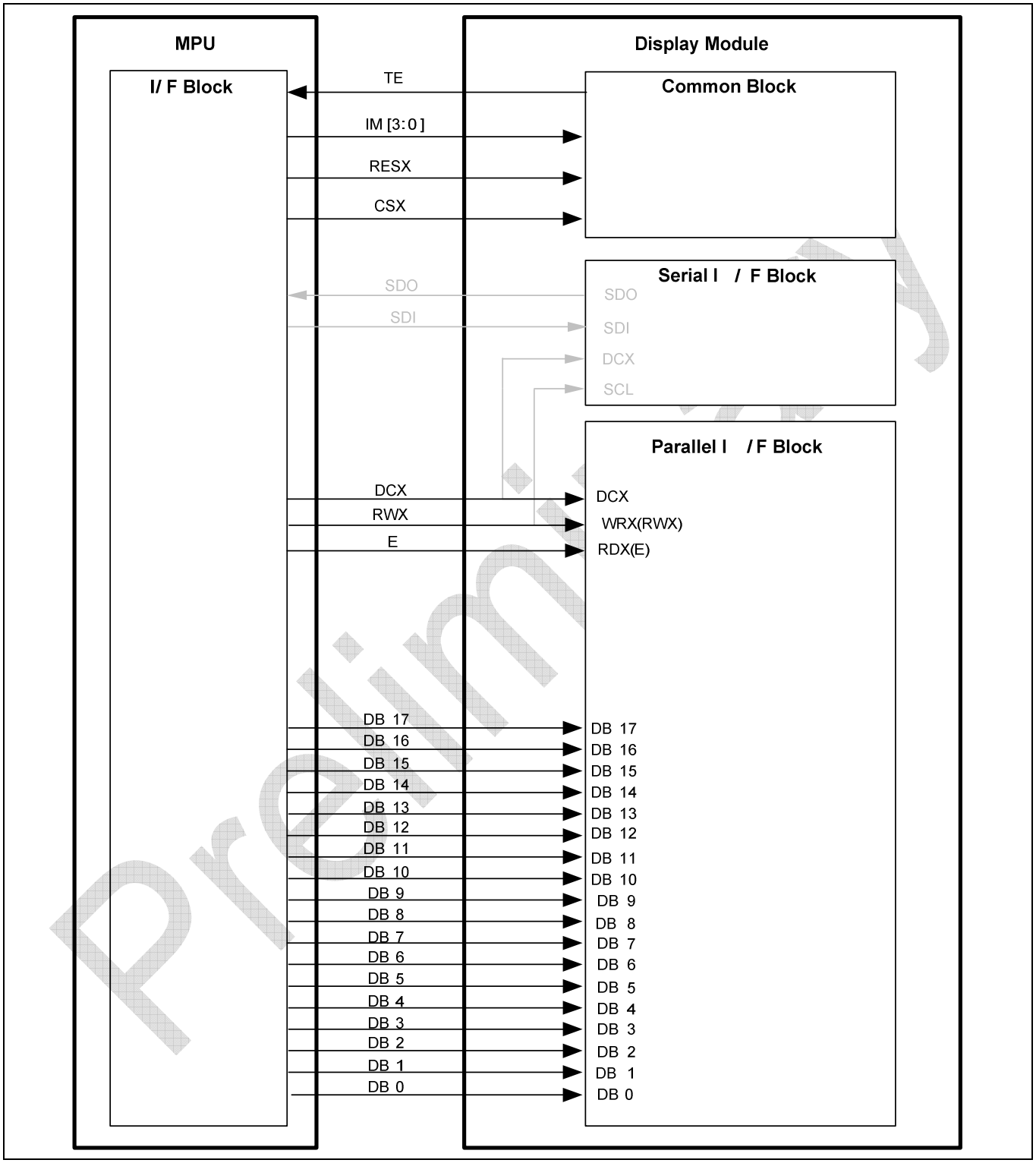

Figure22. 68-Series Parallel Interface

3.1.4. 3-WIRE 9-BIT SERIAL INTERFACE

This serial interface is 3-wire 9-bit bi-directional interface for communication between the micro controller and the LCD driver IC. CSX, SCL (DCX), SDA and SDO are used for interface with MPU only, so it can be stopped when no communication is necessary.

3.1.4.1. 3-Wire 9-bit data serial interface write mode

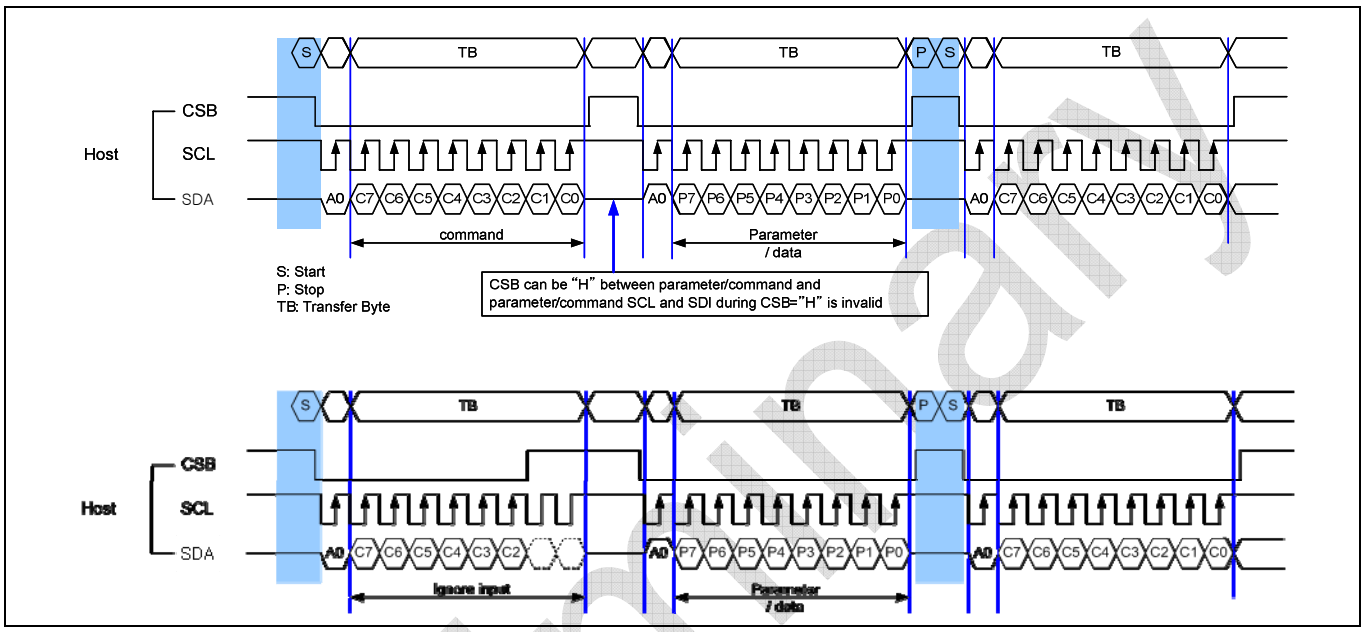

Figure23. 3-Wire 9-Bit Serial Interface I Bus Protocol, Write to Register or Display RAM

3.1.4.2. 3-Wire 9-bit data serial interface read 1-byte mode

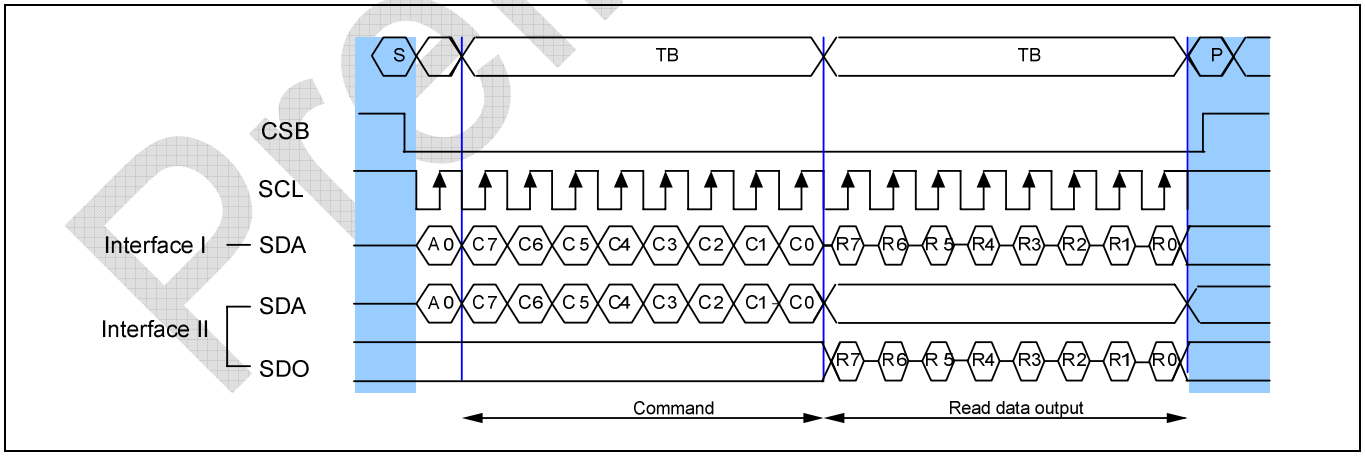

Figure24. 3-Wire 9-Bit Serial Interface I/II Bus Protocol, Read 1-Byte From Register

Preliminary

3.1.4.3. 3-Wire 9-bit data serial interface read multi-byte mode

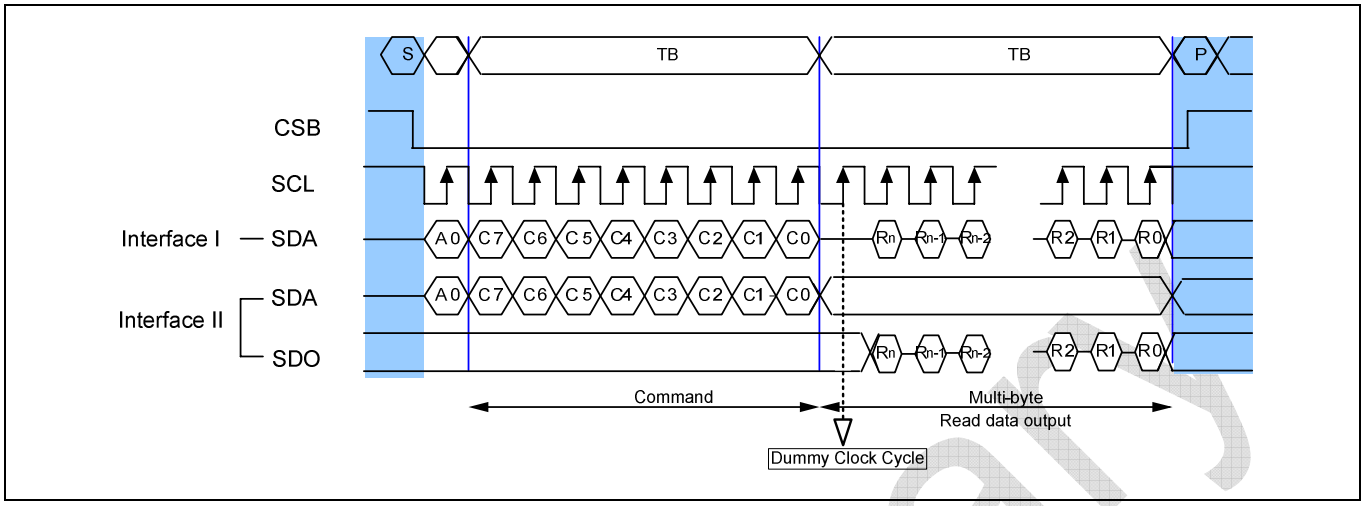

Figure25. 3-Wire 9-Bit Serial Interface I/II Bus Protocol, Read Multi-Byte From Register

Preliminary

3.1.5. 4-WIRE 8-BIT SERIAL INTERFACE

This serial interface is 4-wire 8-bit bi-directional interface for communication between the micro controller and the LCD driver IC. CSX, DCX, SCL, SDA and SDO are used for interface with MPU only, so it can be stopped when no communication is necessary.

3.1.5.1. 4-Wire 8-bit data serial interface write mode

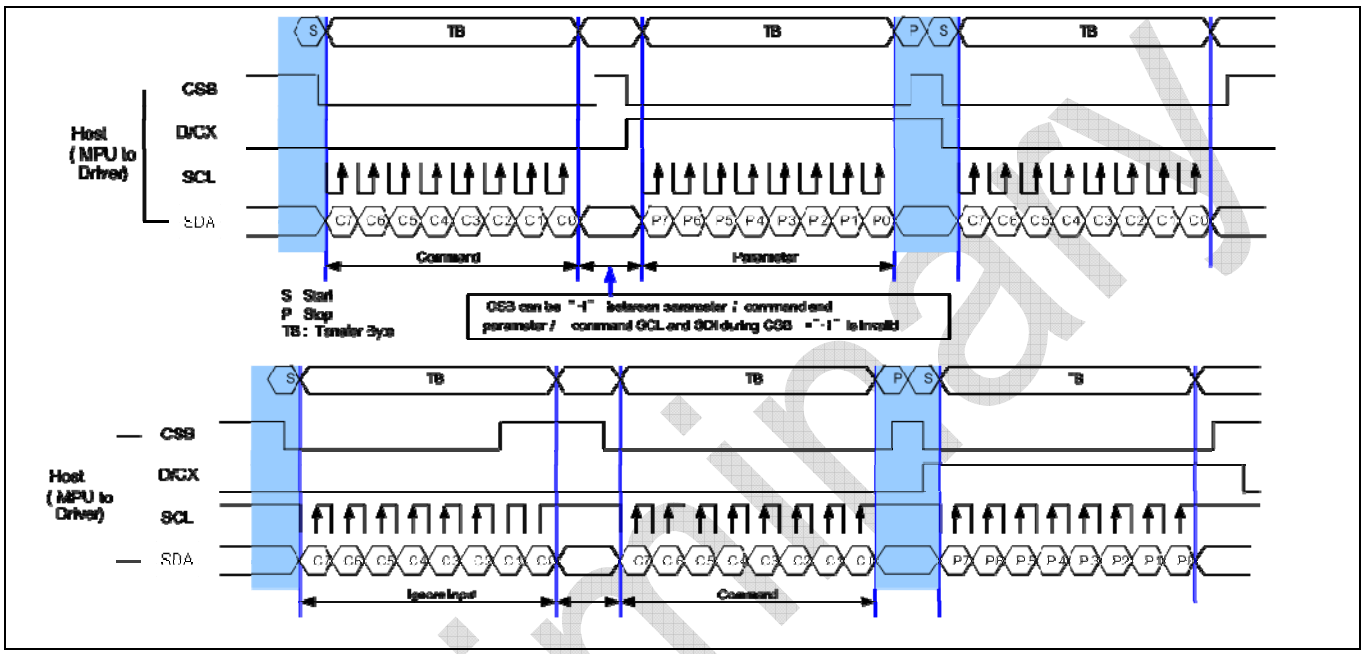

Figure26. 4-Wire 8-Bit Serial Interface I Bus Protocol, Write to Register or Display RAM

3.1.5.2. 4-Wire 8-bit data serial interface read 1-byte mode

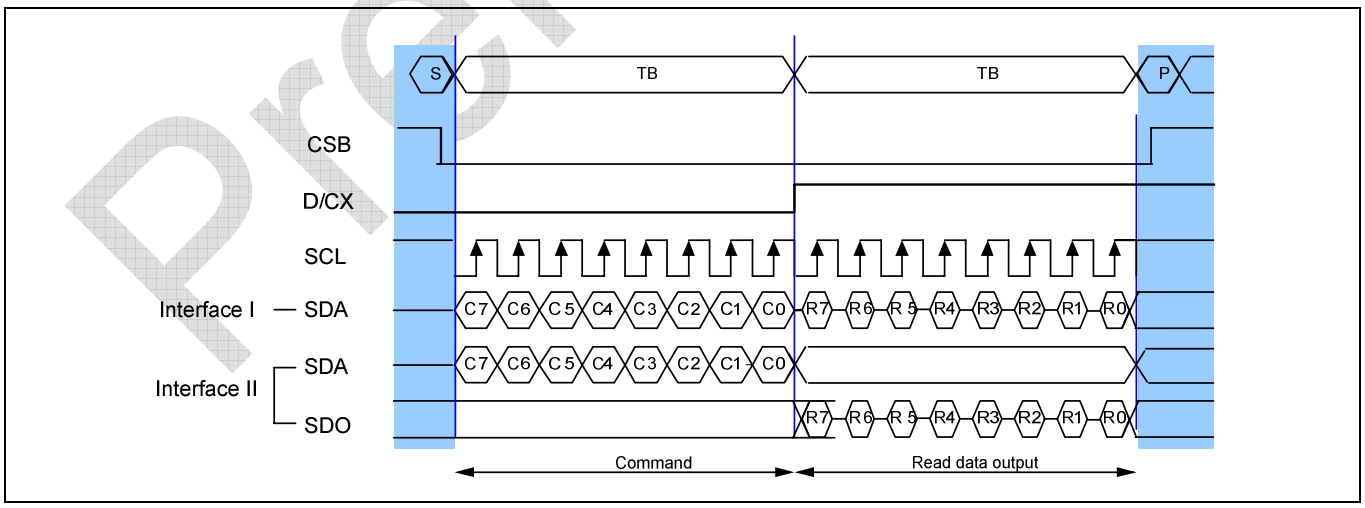

Figure27. 4-Wire 8-Bit Serial Interface I/II Bus Protocol, Read 1-Byte From Register

Preliminary

3.1.5.3. 4Wire 8-bit data serial interface read multi-byte mode

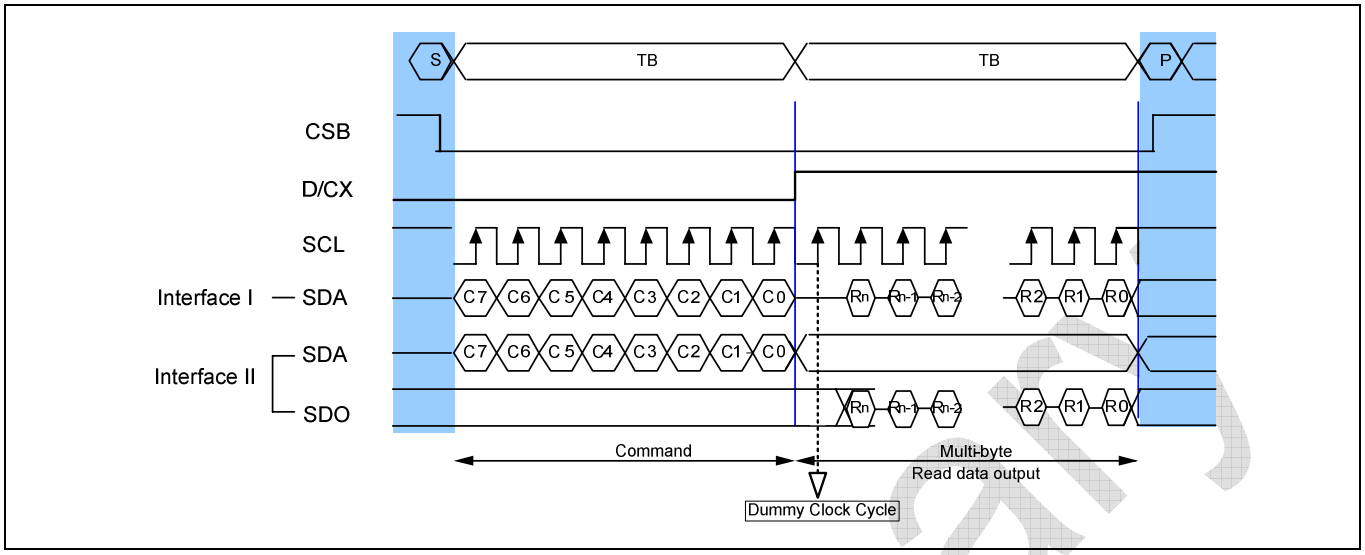

Figure28. 4-Wire 8-Bit Serial Interface I/II Bus Protocol, Read Multi-Byte From Register

Preliminary

3.1.6. 80-SERIES PARALLEL INTERFACE

3.1.6.1. 80-series MPU Parallel Interface Write Mode

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and data signals (DB[17:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

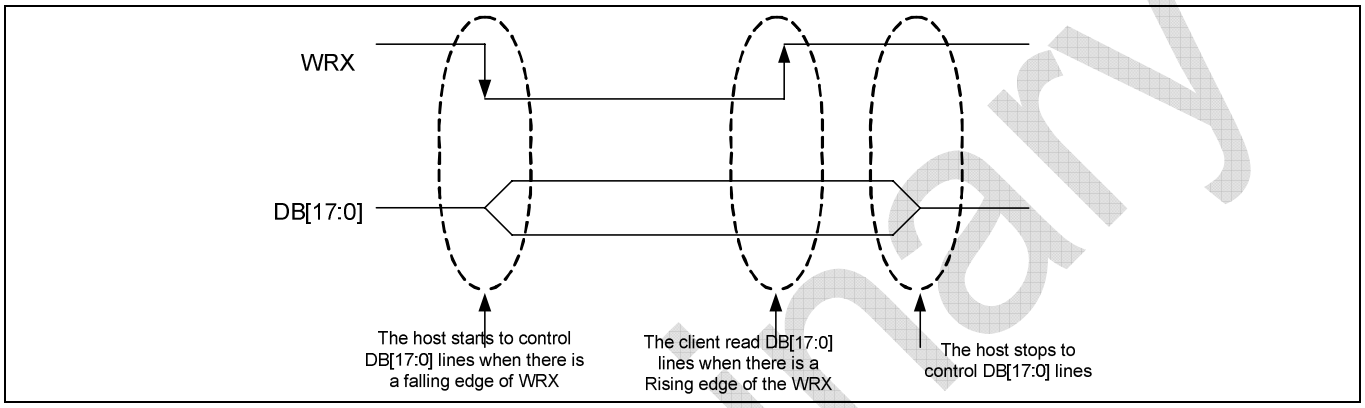

Figure29. 80-Series WRX Protocol

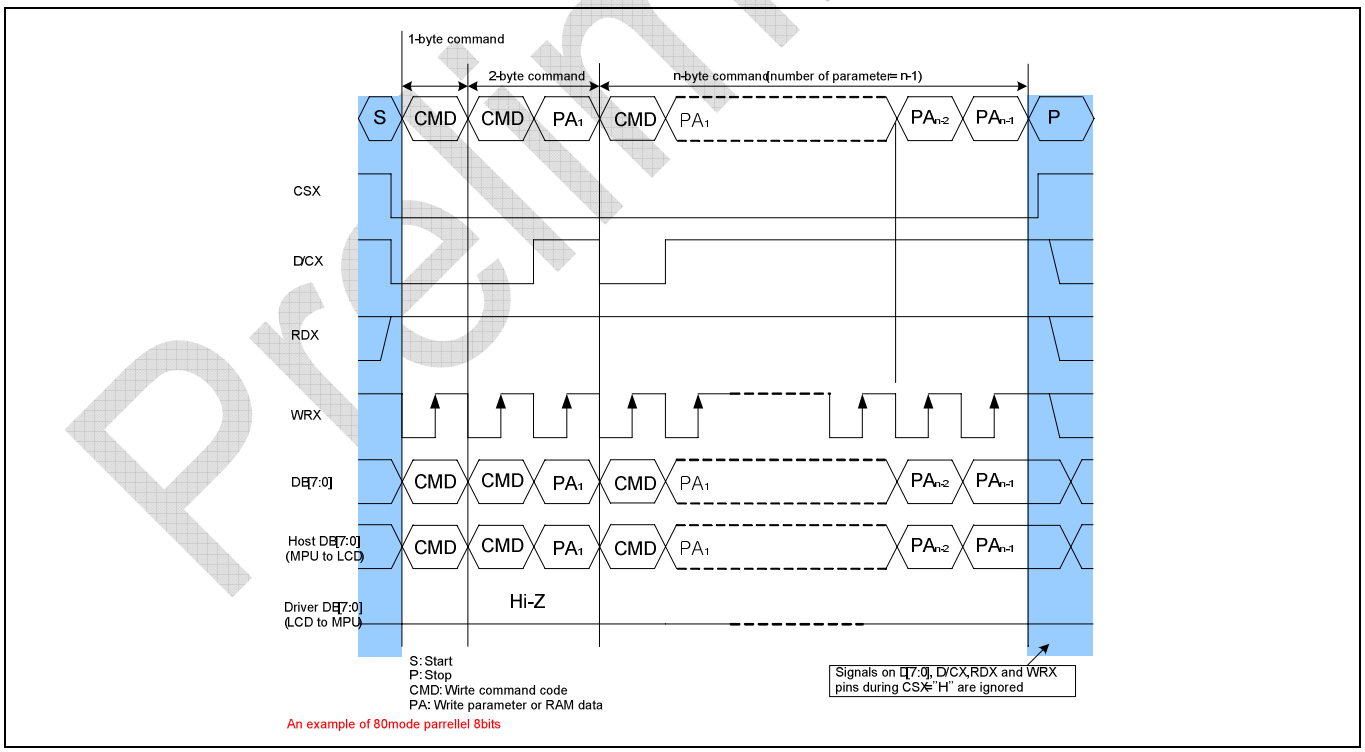

Figure30. 80-Series Parallel Bus Protocol, Write to Register or Display RAM

Preliminary

3.1.6.2. 80-Series mpu parallel interface read mode

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (DB[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

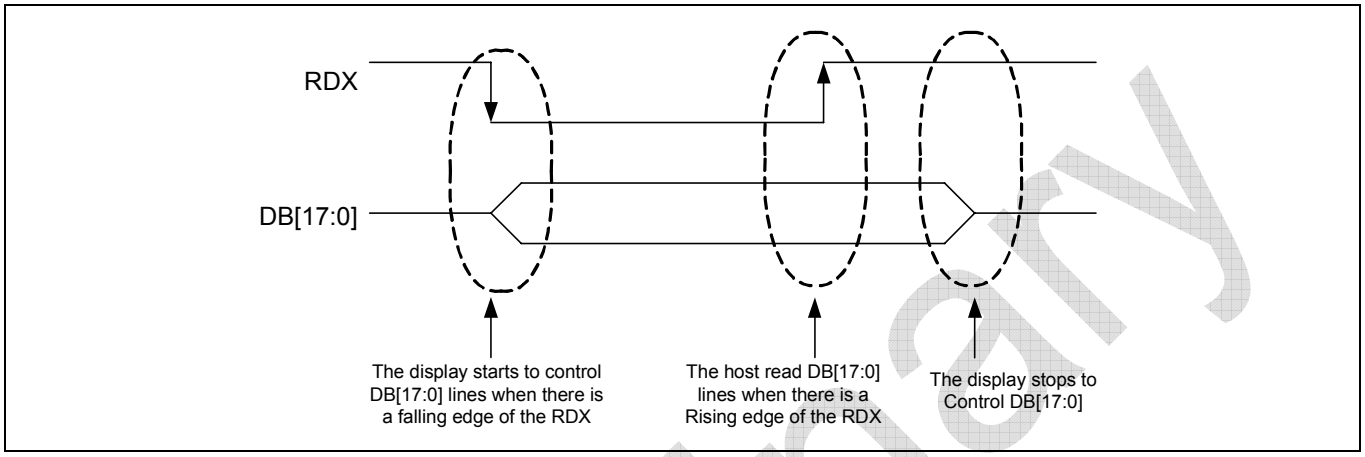

Figure31. 80-Series RDX Protocol

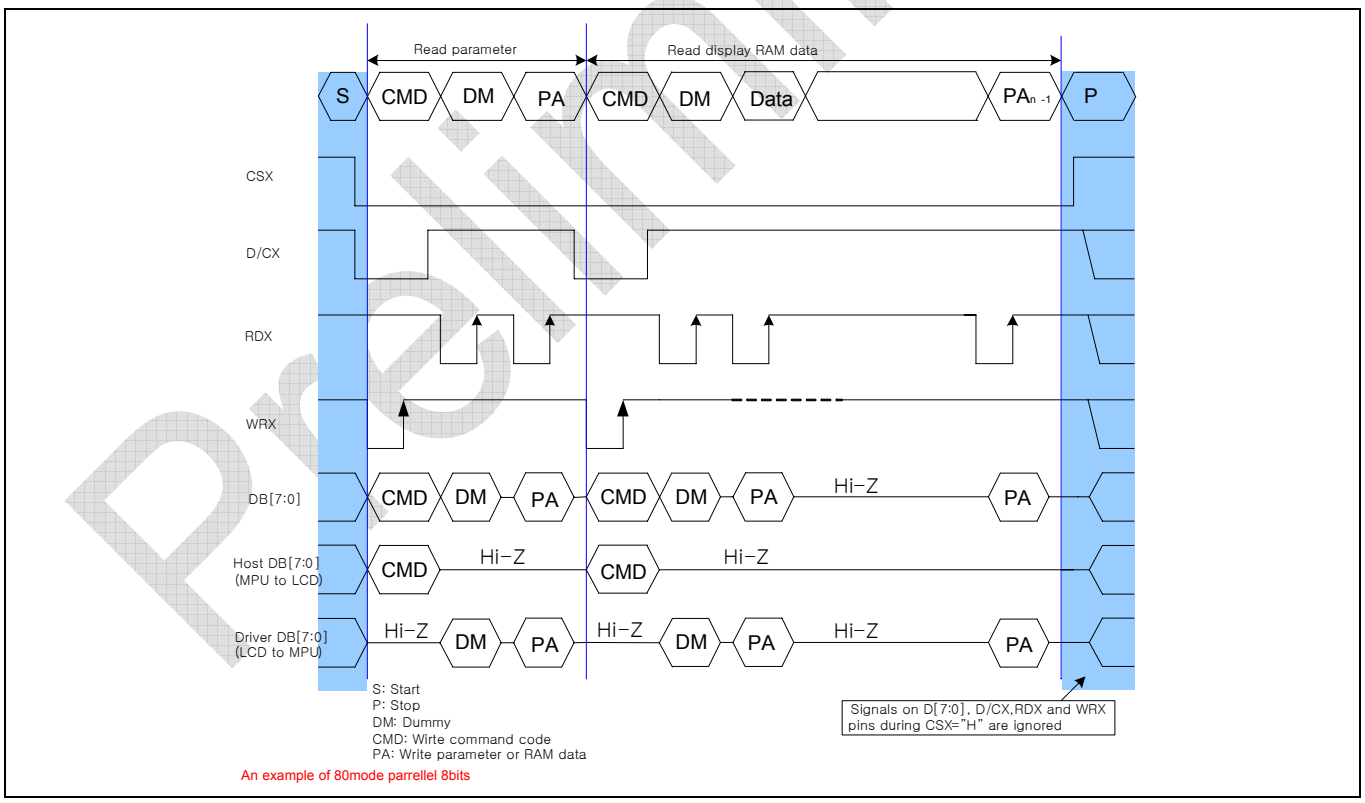

Figure32. 80-Series Parallel Bus Protocol, Read From Register

Preliminary

3.2. INTERFACE DESCRIPTION

The parallel interface of S6D04K1 can communicate with the MPU using max.18 bit bidirectional data bus (DB17 to DB0) to transfer command, parameter and display data. The serial interface uses SDI, SDO for transferring data.

3.2.1. BIDIRECTIONAL DATA BUS

The purpose of MPU interface in S6D04K1 is to communicate with the MPU in a direct connection. If the driver IC is not selected as CSX = Low, the data bus (data line) is placed in the high-impedance state to prevent the other driver ICs from adverse effects. When the driver IC is not selected, inputs through the MPU interface (DCX, RDX and WRX) have no effect.

Table 18. Description OF Data Bus for 80-Series

DCX	WRX	RDX	Description
L	↑	H	Command write Commands are input to DB7 to DB0.
H	↑	H	Parameter and display data write Parameters and display data are respectively input to DB7 to DB0 and DB17 to DB0.
L	H	↑	Parameter and display data read Parameters and display data are respectively output to DB7 to DB0 and DB17 to DB0.
L	H	↑	Dummy data is output

Table 19. Description of Data Bus for 68-Series

DCX	WRX (RWX)	RDX (E)	Description
L	L	↓	Command write Commands are input to DB7 to DB0.
H	L	↓	Parameter and display data write Parameters and display data are respectively input to DB7 to DB0 and DB17 to DB0.
L	H	↓	Parameter and display data read Parameters and display data are respectively output to DB7 to DB0 and DB17 to DB0.
L	H	↓	Dummy data is output

While using the parallel interface, the bus width which is used changes depending on the display data format. When a display data format which uses DB17 to DB8 is selected, it is necessary that DB17 to DB8 are set either HIGH or LOW as input on the MPU side although DB17 to DB8 are ignored when command and parameters are input.

Preliminary

3.2.2. DISPLAY MODULE DATA TRANSFER RECOVERY

If there is a break in data transmission while transferring a Command, Frame Memory or Multiple Parameter command data, before Bit D0 of the byte has been completed, then the Display Module will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (CSX) is next activated. See the following example;

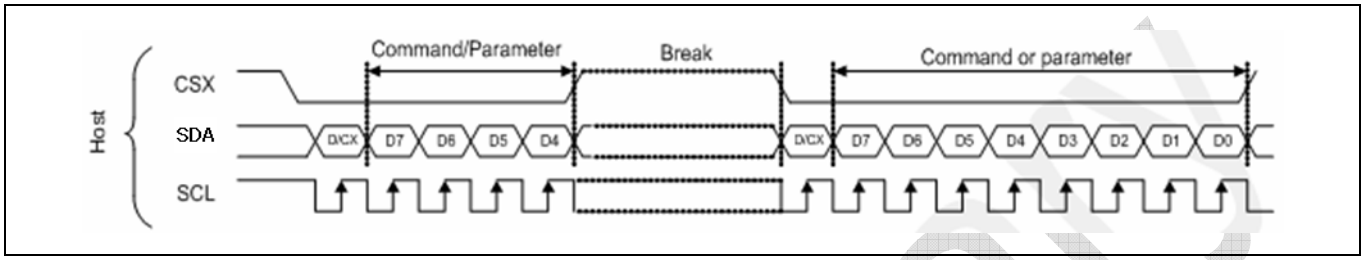

Figure33. Break During Data Transmission

If a 1 or more parameter command is being sent and a break occurs sending before the last parameter of the command and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown.

3.2.2.1. Break during middle of frame

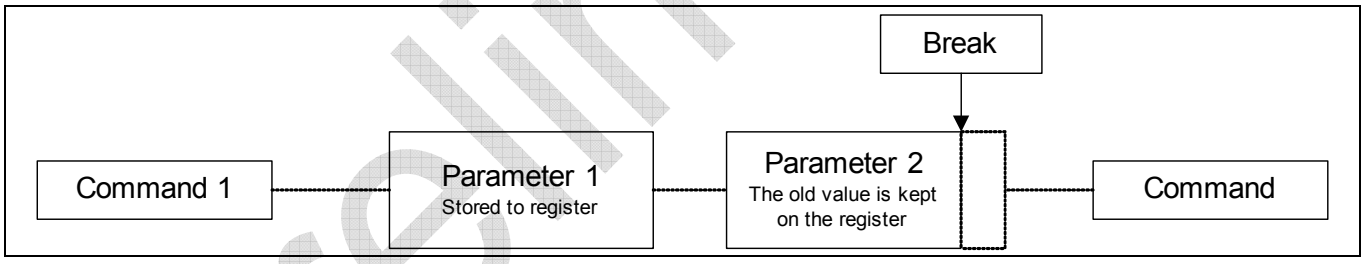

Figure34. Break During Middle of Frame

3.2.2.2. Break between frames

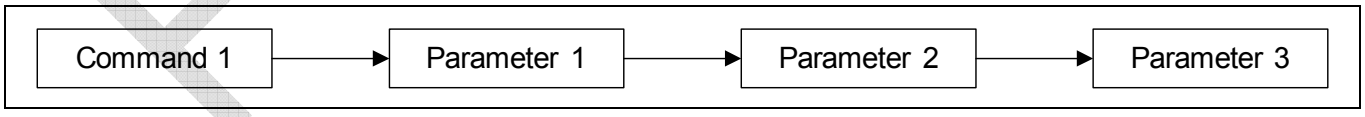

Figure35. Without Break

Preliminary

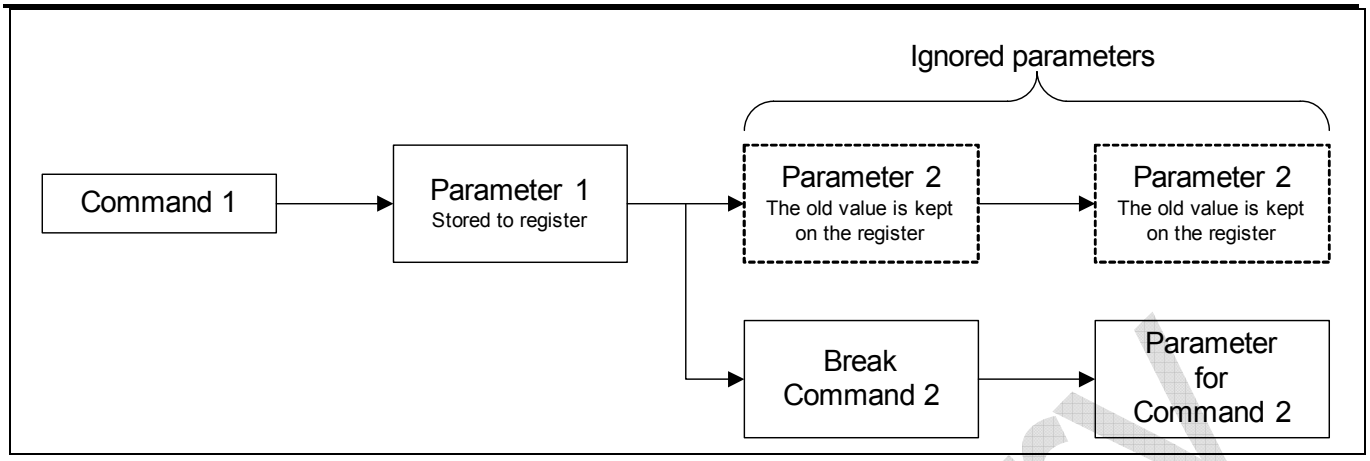

Figure36. With Break

Note.

Break can be e.g. another command or noise pulse.

Preliminary

3.2.3. DISPLAY MODULE DATA TRANSFER PAUSE

It will be possible when transferring a Command, Frame Memory Data or Multiple Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

3.2.3.1. Serial interface pause

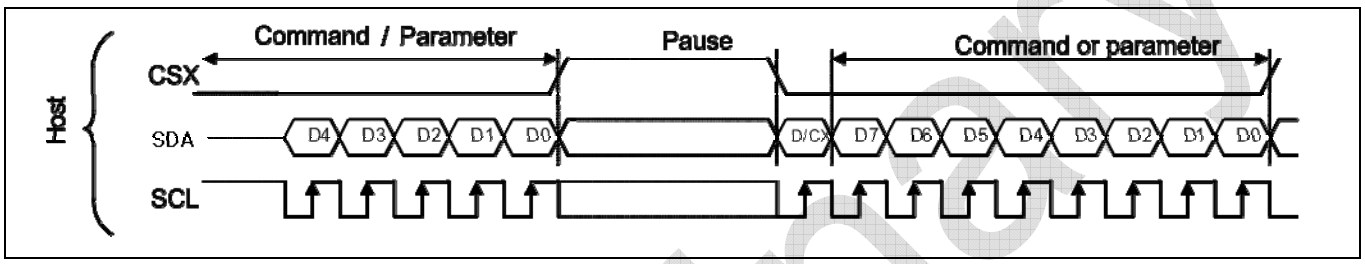

Figure37. Serial Interface Pause

This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

Preliminary

3.2.3.2. Parallel interface pause

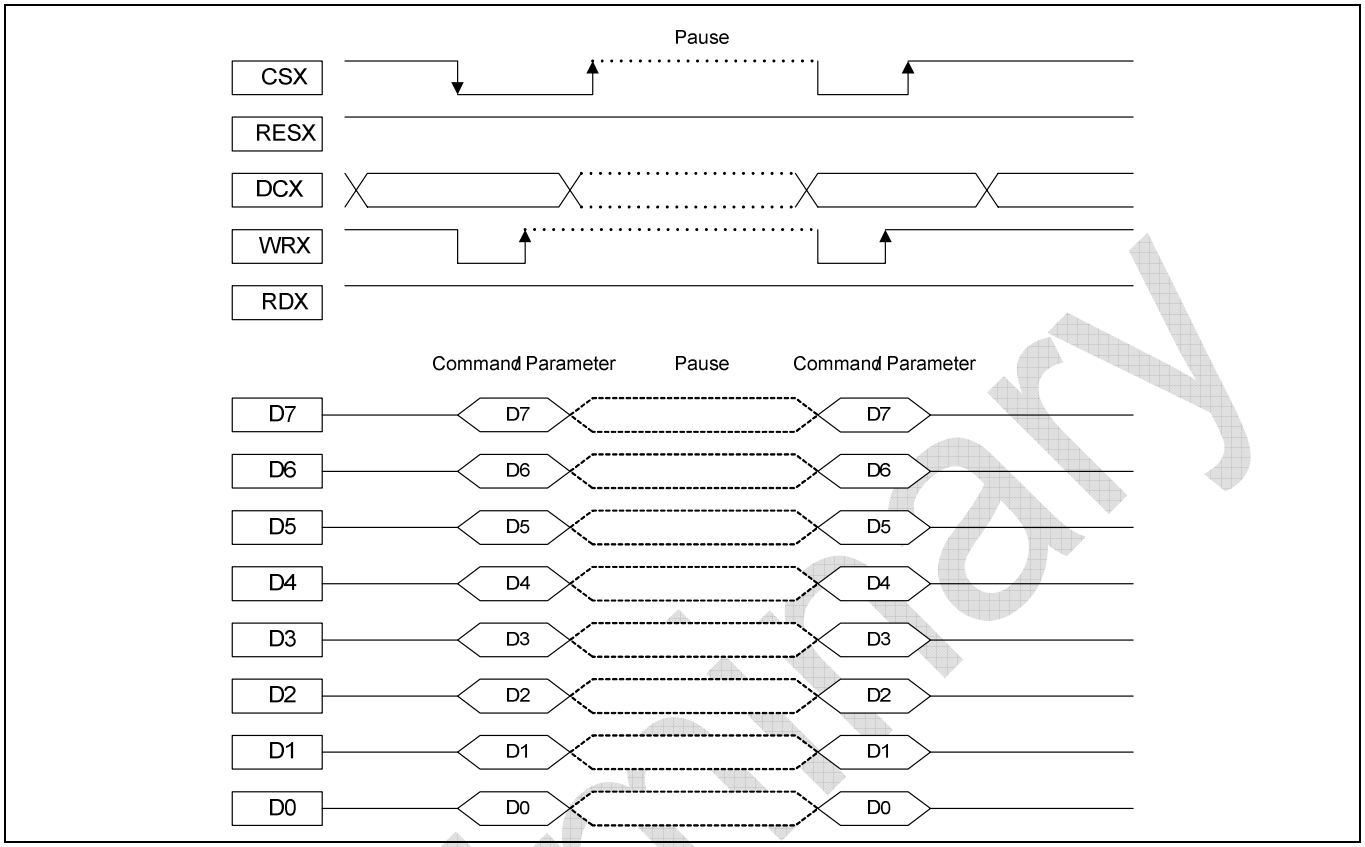

Figure38. Parallel Interface Pause

This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

Preliminary

3.2.4. DISPLAY MODULE DATA TRANSFER MODES

The module has various color modes for transferring data to the display data RAM. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

3.2.4.1. Method

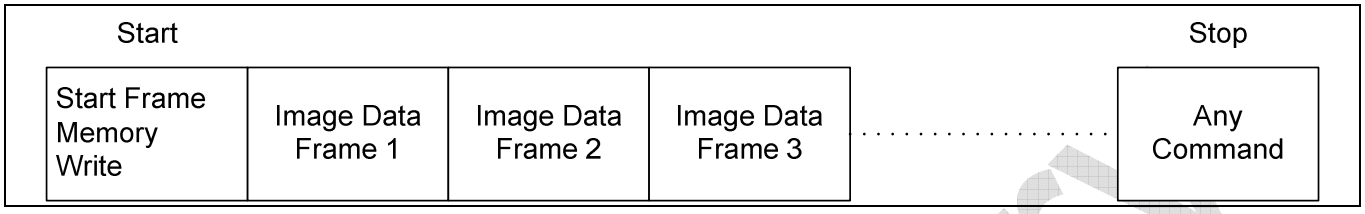

Figure39. Method of Data Transfer Mode

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start pint and the next Frame is written.

3.2.4.2. Method

The Image data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame downloaded.

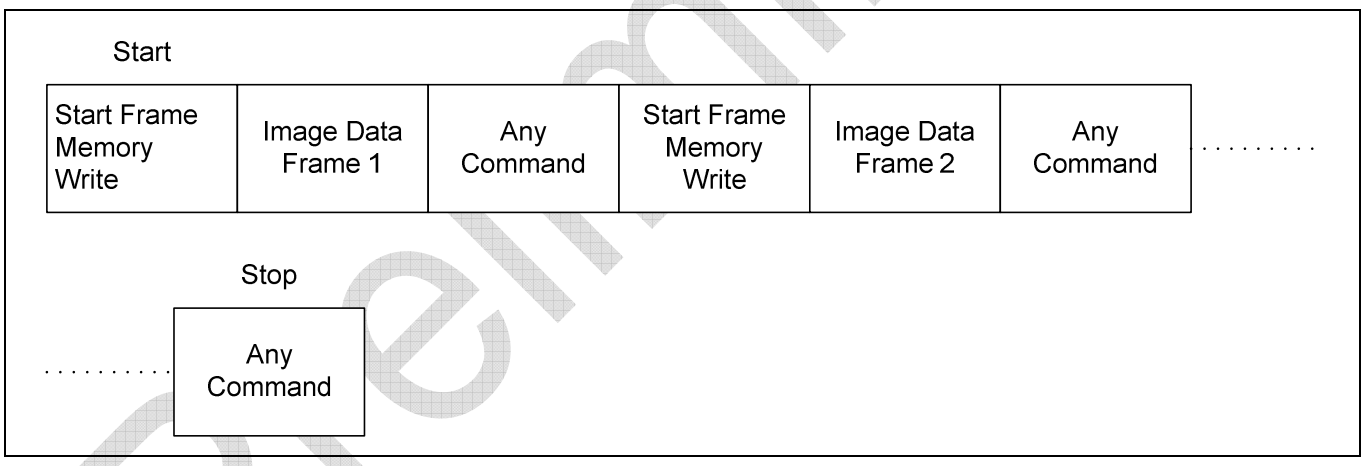

Figure40. Method 2 of Data Transfer Mode

Note.

1. These apply to all data transfer color modes on both Serial and Parallel interfaces.
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored to the Frame Memory.

Preliminary

3.3. DISPLAY DATA FORMAT

Various data formats are available in which display data can be written to the display data RAM. It is possible to choose a format suitable for the purpose of use. The data format is determined by a combination of COLMOD and MDT commands.

3.3.1. DISPLAY DATA FORMAT FOR WRITE

Table 20. Display Data Format for Write

Color Mode	Interface(IM[2:0])				
	18Bit	9Bit	16Bit	8Bit	
	011	010	001	000	
262k Color (COLMOD[2:0] = 110)	18bit 666 1/1 (MDT=00)	9bit 666 1/2 (MDT=00) 6bit 666 1/3 (MDT=01)	16bit 666 2/3 (MDT=00) 12bit 666 1/2 (MDT=01) 16bit 666 1/2 (MDT=10) 16bit 666 1/2 (MDT=11)	6bit 666 1/3 (MDT=00)	Expand by IPM Note1
65k Color (COLMOD[2:0] = 101)	16bit 565 1/1 (MDT=00)	8bit 565 1/2 (MDT=00)	16bit 565 1/1 (MDT=00)	8bit 565 1/2 (MDT=00)	Expand by IPM Note1

Note.

1. Display data expand (565 → 666) method is decided by IPM command. In default condition (IPM = "00"), MSB data are copied to LSB data for expanding. See Figure. 41 and Figure. 42.
2. Registers set related to data format (IPM, MDT) are on the F7H command (Level 2)

Table 21. MDT Description

MDT[1:0](Value)	Description
00	1pixel by 1cycle format
01	2pixel by 3cycle format
10	1pixel by 2cycle format
11	1pixel by 3cycle format

In 65k color mode (16-bit data) data bit should be expanded to 18-bit like below. It will be used "IPM=00"

Preliminary

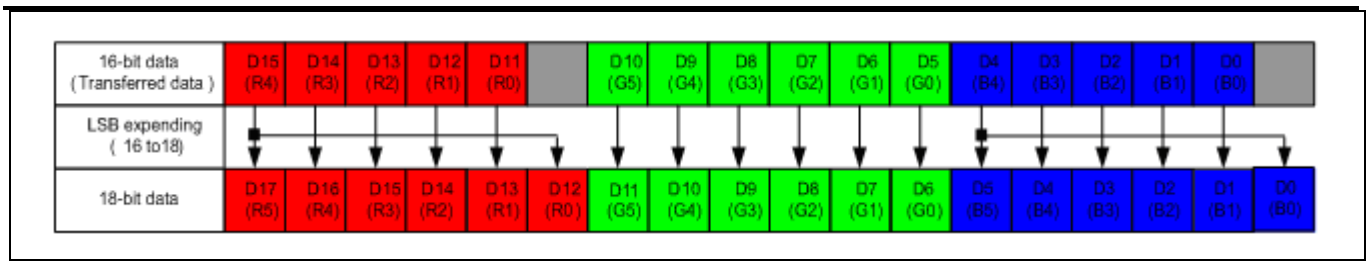

Figure41. Data Expand Method(65K Color Mode)

Preliminary

3.3.2. DISPLAY MODULE DATA COLOR CODING(262K COLOR MODE)

For the display data to be accessed in 262k color mode, it is necessary that 262k color mode be selected (B2 to B0: 110) using COLMOD command before writing or reading to or from the display data RAM. In this mode, the display data per pixel comprised of 6 bits for R, 6 bits for G and 6 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MPU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed, and the display data is read out to the MPU bus according to the format selected.

3.3.2.1. 8Bit parallel interface for 666 1/3 formats

Table 22. 8Bit Parallel Interface for 666 1/3 Formats

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

3.3.2.2. 16Bit parallel interface for 666 2/3 formats(MDT=00)

Table 23. 16Bit Parallel Interface for 666 2/3 Formats(MDT=”00”)

Count	0	1	2	3	…	358	359	360
DCX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9					…			
D8					…			
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4

Count	0	1	2	3	…	358	359	360
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1				…			
D0	C0				…			

3.3.2.3. 16Bit parallel interface for 666 1/2 formats(MDT = “01”)

Table 24. 16Bit Parallel Interface For 666 1/2 Formats(MDT = “01”)

Count	0	1	2	3	4	…	479	480
DCX	0	1	1	1	1	…	1	1
D15		0R5	0B5	1R5	1B5	…	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	239R0	239B0
D9						…		
D8						…		
D7	C7	0G5		1G5		…	239G5	
D6	C6	0G4		1G4		…	239G4	
D5	C5	0G3		1G3		…	239G3	
D4	C4	0G2		1G2		…	239G2	
D3	C3	0G1		1G1		…	239G1	
D2	C2	0G0		1G0		…	239G0	
D1	C1					…		
D0	C0					…		

3.3.2.4. 16Bit parallel interface for 666 1/2 formats(MDT = “10”)

Table 25. 16Bit Parallel Interface for 666 1/2 Formats(MDT = “10”)

Count	0	1	2	3	4	…	479	480
DCX	0	1	1	1	1	…	1	1
D15		0R5	0B1	1R5	1B1	…	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	239R4	239B0
D13		0R3		1R3		…	239R3	
D12		0R2		1R2		…	239R2	
D11		0R1		1R1		…	239R1	
D10		0R0		1R0		…	239R0	
D9		0G5		1G5		…	239G5	
D8		0G4		1G4		…	239G4	
D7	C7	0G3		1G3		…	239G3	
D6	C6	0G2		1G2		…	239G2	
D5	C5	0G1		1G1		…	239G1	
D4	C4	0G0		1G0		…	239G0	
D3	C3	0B5		1B5		…	239B5	
D2	C2	0B4		1B4		…	239B4	
D1	C1	0B3		1B3		…	239B3	
D0	C0	0B2		1B2		…	239B2	

3.3.2.5. 16Bit parallel interface for 666 1/2 formats(MDT = “11”)

Table 26. 16Bit Parallel Interface for 666 1/2 Formats(MDT = “11”)

Count	0	1	2	3	4	…	479	480
DCX	0	1	1	1	1	…	1	1
D15			0R3		1R3	…		239R3
D14			0R2		1R2	…		239R2
D13			0R1		1R1	…		239R1
D12			0R0		1R0	…		239R0
D11			0G5		1G5	…		239G5
D10			0G4		1G4	…		239G4
D9			0G3		1G3	…		239G3
D8			0G2		1G2	…		239G2
D7	C7		0G1		1G1	…		239G1

Count	0	1	2	3	4	…	479	480
D6	C6		0G0		1G0	…		239G0
D5	C5		0B5		1B5	…		239B5
D4	C4		0B4		1B4	…		239B4
D3	C3		0B3		1B3	…		239B3
D2	C2		0B2		1B2	…		239B2
D1	C1	0R5	0B1	1R5	1B1	…	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	239R4	239B0

3.3.2.6. 9Bit parallel interface for 666 1/2 formats

Table 27. 9Bit Parallel Interface for 666 1/2 Formats(MDT = 00)

Count	0	1	2	3	…	478	479	480
DCX	0	1	1	1	…	1	1	1
D8		0R5	0G2	1R5	…	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	…	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	…	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	…	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	…	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	…	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	…	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	…	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	…	238B0	239G3	239B0

Table 28. 9-Bit Parallel Interface for 666 1/3 Formats(MDT = 01)

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D8					…			
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G5	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G4	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

3.3.2.7. 18Bit parallel interface for 666 1/1 formats

Table 29. 18Bit Parallel Interface for 666 1/1 Formats

Count	0	1	2	…	239	240
DCX	0	1	1	…	1	1
D17		0R5	1R5	…	238R5	239R5
D16		0R4	1R4	…	238R4	239R4
D15		0R3	1R3	…	238R3	239R3
D14		0R2	1R2	…	238R2	239R2
D13		0R1	1R1	…	238R1	239R1
D12		0R0	1R0	…	238R0	239R0
D11		0G5	1G5	…	238G5	239G5
D10		0G4	1G4	…	238G4	239G4
D9		0G3	1G3	…	238G3	239G3
D8		0G2	1G2	…	238G2	239G2
D7	C7	0G1	1G1	…	238G1	239G1
D6	C6	0G0	1G0	…	238G0	239G0
D5	C5	0B5	1B5	…	238B5	239B5
D4	C4	0B4	1B4		238B4	239B4
D3	C3	0B3	1B3		238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

3.3.2.8. 4-Wire 8-bit serial interface for 666 1/3 formats

Table 30. 4-Wire 8-Bit Serial Interface for 666 1/3 Formats

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			

Preliminary

Count	0	1	2	3	…	718	719	720
D0	C0				…			

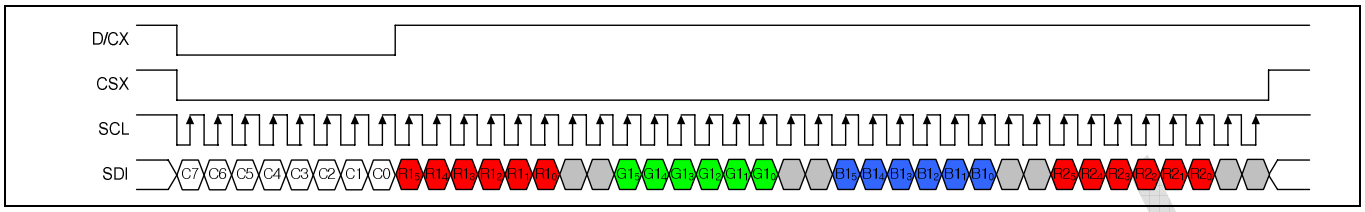

Figure42. 4-Wire 8-Bit Serial Interface for 666 1/3 Formats

3.3.2.9. 3-Wire 9-bit serial interface for 666 1/3 formats

Table 31. 3-Wire 9-Bit Serial Interface for 666 1/3 Formats

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

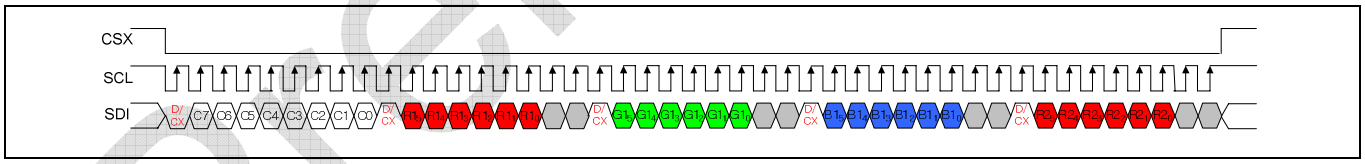

Figure43. 3-Wire 9-Bit Serial Interface for 666 1/3 Formats

Preliminary

3.3.3. DISPLAY MODULE DATA COLOR CODING (65K COLOR MODE)

For the display data to be accessed in 65k color mode, it is necessary that 65k color mode be selected (B2 to B0: 101) using COLMOD command before writing or reading to or from the display data RAM. In this mode, the display data per pixel comprised of 5 bits for R, 6 bits for G and 5 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MPU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed, and the display data is read out to the MPU bus according to the format selected.

3.3.3.1. 8Bit parallel interface for 565 1/2 formats

Table 32. 8Bit Parallel Interface for 565 1/2 Formats

Count	0	1	2	3	4	…	359	480
DCX	0	1	1	1	1	…	1	1
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

3.3.3.2. 16Bit parallel interface for 565 1/1 formats

Table 33. 16Bit Parallel Interface for 565 1/1 Formats

Count	0	1	2	…	239	240
DCX	0	1	1	…	1	1
D15		0R4	1R4	…	238R4	239R4
D14		0R3	1R3	…	238R3	239R3
D13		0R2	1R2	…	238R2	239R2
D12		0R1	1R1	…	238R1	239R1
D11		0R0	1R0	…	238R0	239R0
D10		0G5	1G5	…	238G5	239G5
D9		0G4	1G4	…	238G4	239G4
D8		0G3	1G3	…	238G3	239G3
D7	C7	0G2	1G2	…	238G2	239G2
D6	C6	0G1	1G1	…	238G1	239G1

Count	0	1	2	…	239	240
D5	C5	0G0	1G0	…	238G0	239G0
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

3.3.3.3. 9Bit parallel interface for 565 1/2 formats

Table 34. 9Bit Parallel Interface for 565 1/2 Formats

Count	0	1	2	3	4	…	359	480
DCX	0	1	1	1	1	…	1	1
D8						…		
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

3.3.3.4. 18Bit parallel interface for 565 1/1 formats

Table 35. 18Bit Parallel Interface for 565 1/1 Formats

Count	0	1	2	…	239	240
DCX	0	1	1	…	1	1
D17						
D16						
D15		0R4	1R4	…	238R4	239R4
D14		0R3	1R3	…	238R3	239R3
D13		0R2	1R2	…	238R2	239R2
D12		0R1	1R1	…	238R1	239R1
D11		0R0	1R0	…	238R0	239R0
D10		0G5	1G5	…	238G5	239G5
D9		0G4	1G4	…	238G4	239G4

Count	0	1	2	…	239	240
D8		0G3	1G3	…	238G3	239G3
D7	C7	0G2	1G2	…	238G2	239G2
D6	C6	0G1	1G1	…	238G1	239G1
D5	C5	0G0	1G0	…	238G0	239G0
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

3.3.3.5. 4-Wire 8-bit serial interface for 565 1/2 formats

Table 36. 4-Wire 8-Bit Serial Interface for 565 1/2 Formats

Count	0	1	2	3	4	…	359	480
DCX	0	1	1	1	1	…	1	1
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

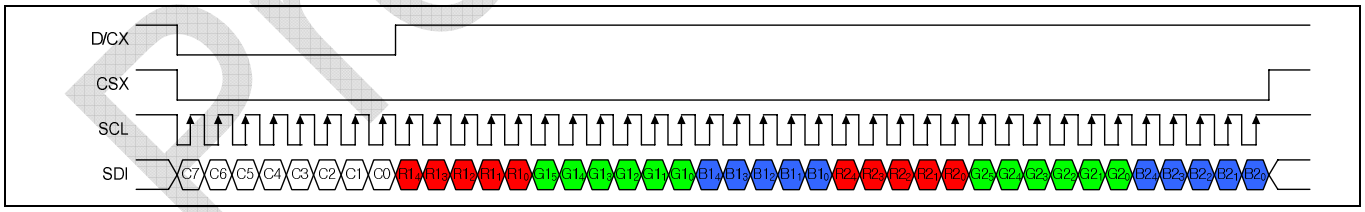

Figure44. 4-Wire 8-Bit Serial Interface for 565 1/2 Formats

3.3.3.6. 3-Wire 9-bit serial interface for 565 1/2 formats

Table 37. 3-Wire 9-Bit Serial Interface for 565 1/2 Formats

Count	0	1	2	3	4	…	359	480
DCX	0	1	1	1	1	…	1	1
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

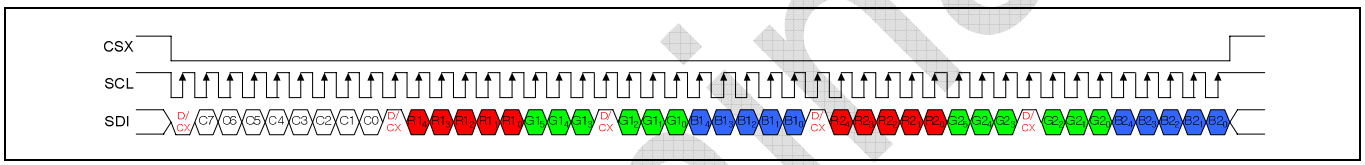

Figure45. 3-Wire 9-Bit Serial Interface for 565 1/2 Formats

Preliminary

3.4. RGB INTERFACE

3.4.1. DEFINITION

The module uses 6 or 18-bit parallel RGB interface which includes: VSYNC, HSYNC, ENABLE, DOTCLK, DB[17:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (DOTCLK) is running all the time without stopping and it is used to entering VSYNC, HSYNC, ENABLE and DB[17:0] states when there is a rising edge of the DOTCLK. The DOTCLK can not be used as continues internal clock for other functions of the display module e.g. Sleep in mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative ('0', low) active and its state is read to the display module by a rising edge of he DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is negative ('0', low) active and its state is read to the display module by a rising edge of the DOTCLK signal.

Data Enable (ENABLE) is used to tell when there is received a RGB information that should be transferred on the display. This is a positive ('1', high) active and its state is read to the display module by a rising edge of the DOTCLK signal.

DB[17:0] are used to tell what is the information of the image that is transferred on the display (When ENABLE= '1' and there is a rising edge of DOTCLK). DB[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal.

The DOTCLK cycle is described in the following figure.

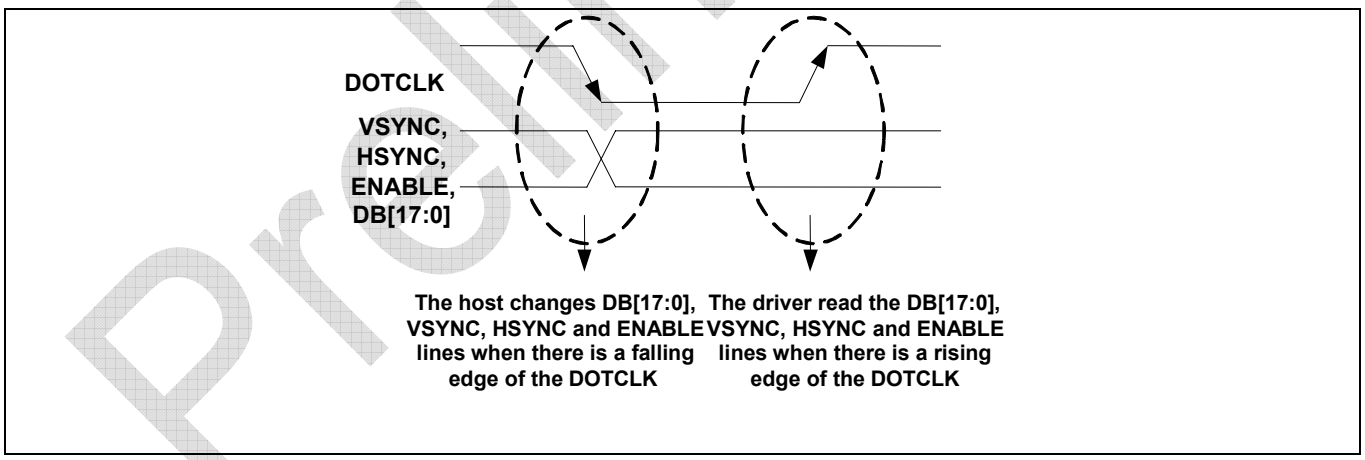

Figure46. DOTCLK Timing

Note.

DPL=0 of IFCTL (F7h) command.

Preliminary

3.4.2. MOTION PICTURE DISPLAY

S6D04K1 incorporates RGB interface to display motion pictures and GRAM to store data for display.

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK.

In the period between the completion of displaying one frame data and the next VSYNC signal, the display status will remain in front porch period.

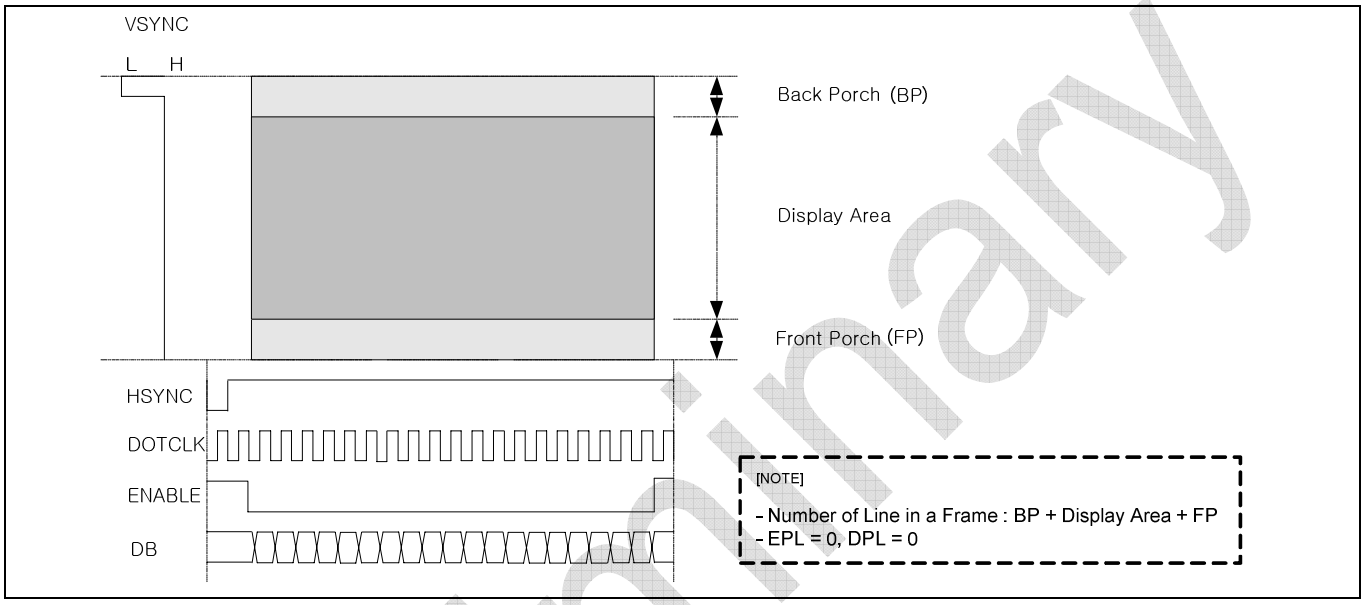

Figure47. RGB Interface

Note.

For RGB interface, VSYNC, HSYNC, DOTCLK should be supplied at much higher resolution than that of panel.

There are five timing conditions for RGB Interface that is determined according to RIM, COLMOD and each condition is described below.

Table 38. Rgb Interface Mode Selection

RIM	COLMOD[6:4]	Color Depth
0	110	262k-color (1 transfer/pixel)
	101	65k-color (1 transfer/pixel)
1	110	262k-color (3 transfer/pixel)
	101	65k-color (3 transfer/pixel)

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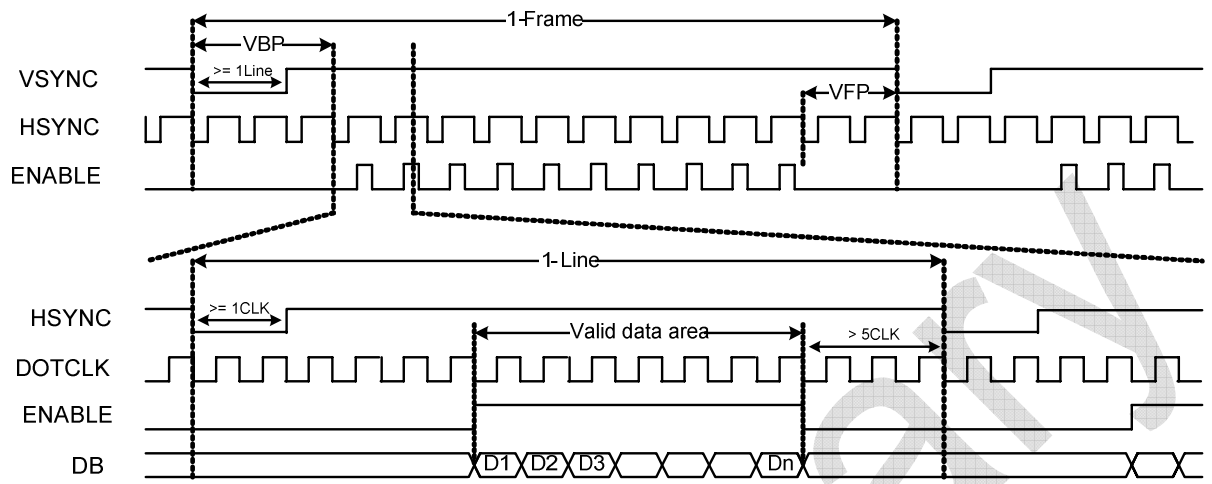
3.4.3. RGB MODE

3.4.3.1. RGB Mode – 18-bit I/F

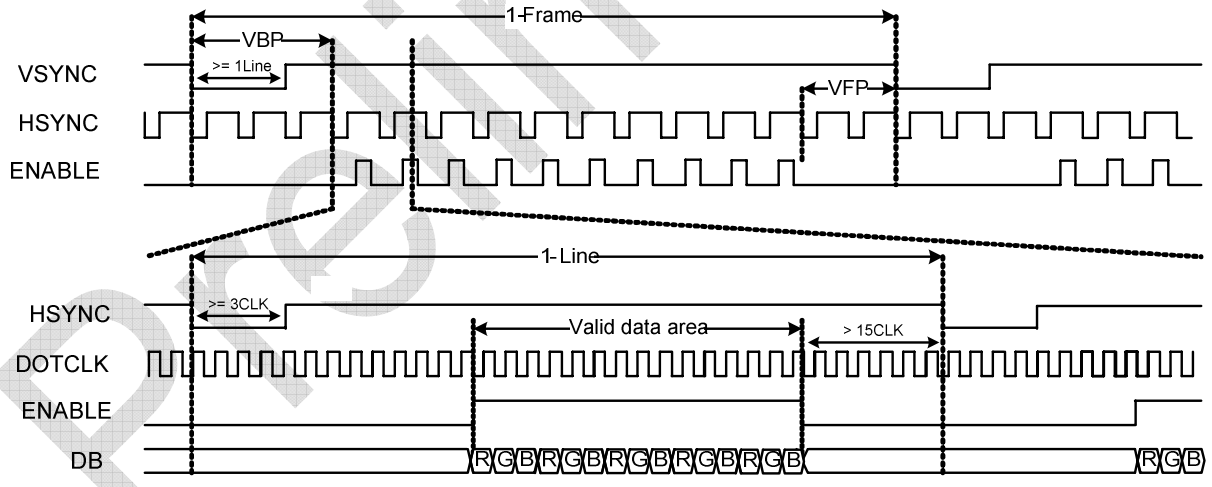


RGB mode – 18-bit I/F timing diagram (RIM = 0)

Note.

DPL=0, EPL=1, HPL=0 and VPL=0 of IFCTL (F7h) command.

3.4.3.2. RGB Mode – 6-bit I/F



RGB mode – 6-bit I/F timing diagram (RIM = 1)

Note.

DPL=0, EPL=1, HPL=0 and VPL=0 of IFCTL (F7h) command.

Preliminary

3.4.4. RGB DISPLAY DATA FORMAT

3.4.4.1. RGB 18-bit I/F – 262k-color

Table 39. 18-Bit Interface for 666 1/1 Formats

Count	1	2	…	239	240
DB17	0R5	1R5	…	238R5	239R5
DB16	0R4	1R4	…	238R4	239R4
DB15	0R3	1R3	…	238R3	239R3
DB14	0R2	1R2	…	238R2	239R2
DB13	0R1	1R1	…	238R1	239R1
DB12	0R0	1R0	…	238R0	239R0
DB11	0G5	1G5	…	238G5	239G5
DB10	0G4	1G4	…	238G4	239G4
DB9	0G3	1G3	…	238G3	239G3
DB8	0G2	1G2	…	238G2	239G2
DB7	0G1	1G1	…	238G1	239G1
DB6	0G0	1G0	…	238G0	239G0
DB5	0B5	1B5	…	238B5	239B5
DB4	0B4	1B4		238B4	239B4
DB3	0B3	1B3		238B3	239B3
DB2	0B2	1B2	…	238B2	239B2
DB1	0B1	1B1	…	238B1	239B1
DB0	0B0	1B0	…	238B0	239B0

3.4.4.2. RGB 18-Bit I/F – 65k-color

Table 40. 18-Bit Interface for 565 1/1 Formats

Count	1	2	…	239	240
DB17					
DB16					
DB15	0R4	1R4	…	238R4	239R4
DB14	0R3	1R3	…	238R3	239R3
DB13	0R2	1R2	…	238R2	239R2
DB12	0R1	1R1	…	238R1	239R1
DB11	0R0	1R0	…	238R0	239R0
DB10	0G5	1G5	…	238G5	239G5
DB9	0G4	1G4	…	238G4	239G4

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Count	1	2	…	239	240
DB8	0G3	1G3	…	238G3	239G3
DB7	0G2	1G2	…	238G2	239G2
DB6	0G1	1G1	…	238G1	239G1
DB5	0G0	1G0	…	238G0	239G0
DB4	0B4	1B4	…	238B4	239B4
DB3	0B3	1B3		238B3	239B3
DB2	0B2	1B2		238B2	239B2
DB1	0B1	1B1	…	238B1	239B1
DB0	0B0	1B0	…	238B0	239B0

3.4.4.3. RGB 6-Bit I/F – 262k-color

Table 41. 6-Bit Interface Type Ⅰ for 666 1/3 Formats

Count	1	2	3	…	718	719	720
DB5	0R5	0G5	0B5	…	239R5	239G5	239B5
DB4	0R4	0G4	0B4	…	239R4	239G4	239B4
DB3	0R3	0G3	0B3	…	239R3	239G3	239B3
DB2	0R2	0G2	0B2	…	239R2	239G2	239B2
DB1	0R1	0G1	0B1	…	239R1	239G1	239B1
DB0	0R0	0G0	0B0	…	239R0	239G0	239B0

3.4.4.4. RGB 6Bit I/F – 65k-color

Table 42. 6-Bit Interface Type Ⅰ for 565 1/3 Formats

Count	1	2	3	…	718	719	720
DB5	0R4	0G5	0B4	…	239R4	239G5	239B4
DB4	0R3	0G4	0B3	…	239R3	239G4	239B3
DB3	0R2	0G3	0B2	…	239R2	239G3	239B2
DB2	0R1	0G2	0B1	…	239R1	239G2	239B1
DB1	0R0	0G1	0B0	…	239R0	239G1	239B0
DB0		0G0		…		239G0	

3.4.5. DISPLAY TIMING OF RGB INTERFACE

3.4.5.1. Display timing when rgb data is written at shift register

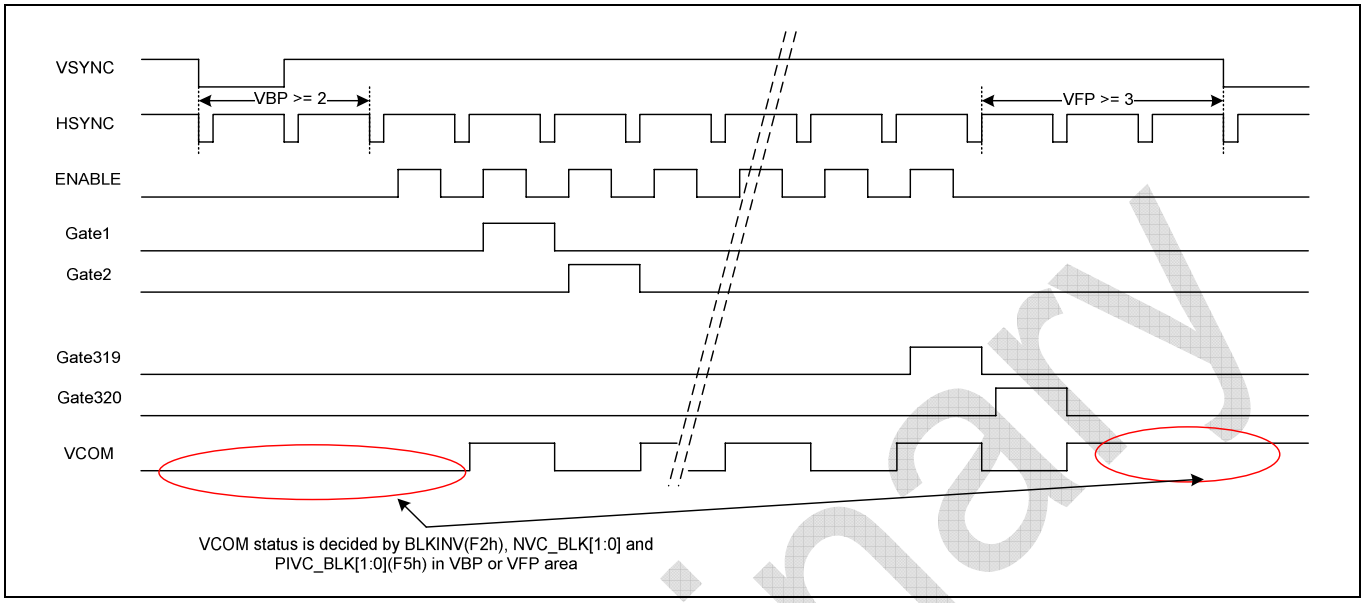

Figure48. Display Timing Diagram When RAM_ACCS = 0 (F7h)

Note.

When RAM_ACCS=0, real Vertical Back Porch is VBP + 1 and real Vertical Front Porch is VFP – 1 .

3.4.5.2. Display timing when rgb data is written at memory

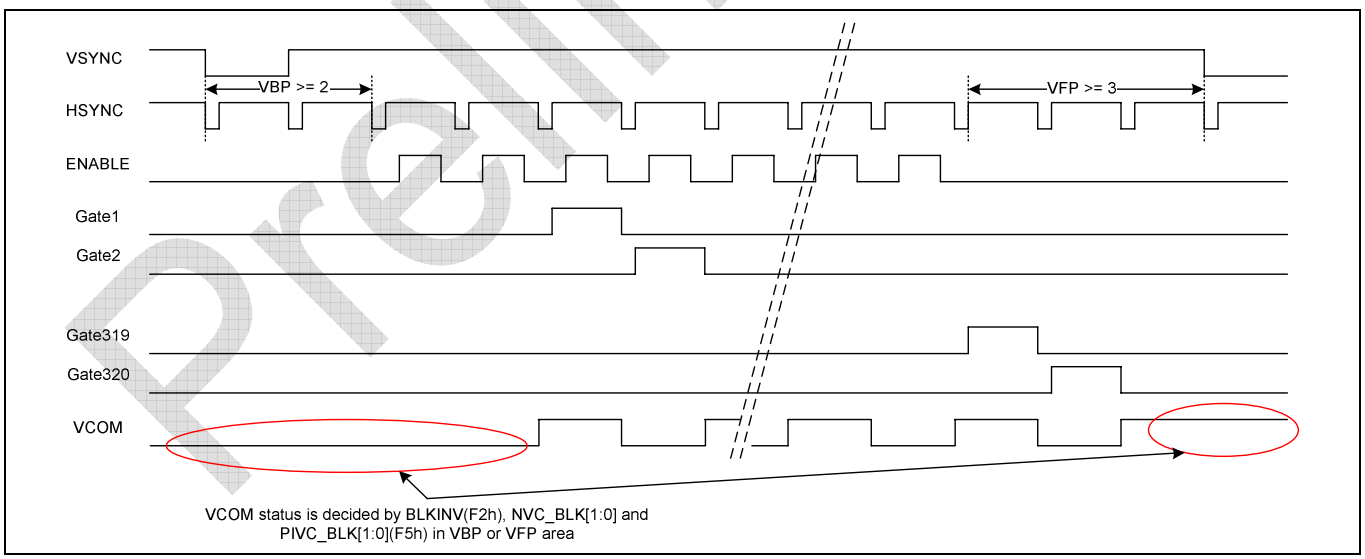

Figure49. Display Timing Diagram When RAM_ACCS = 1 (F7h)

Note.

When RAM_ACCS=1, real Vertical Back Porch is VBP + 2 and real Vertical Front Porch is VFP – 2 .

Preliminary

3.5. VSYNC INTERFACE

3.5.1. DEFINITION

The S6D04K1 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

When DM1-0="10", VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is writ
ten to RAM via the system interface with higher speed than for internal display operation. This method enables tearing-free display of motion pictures with the conventional interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

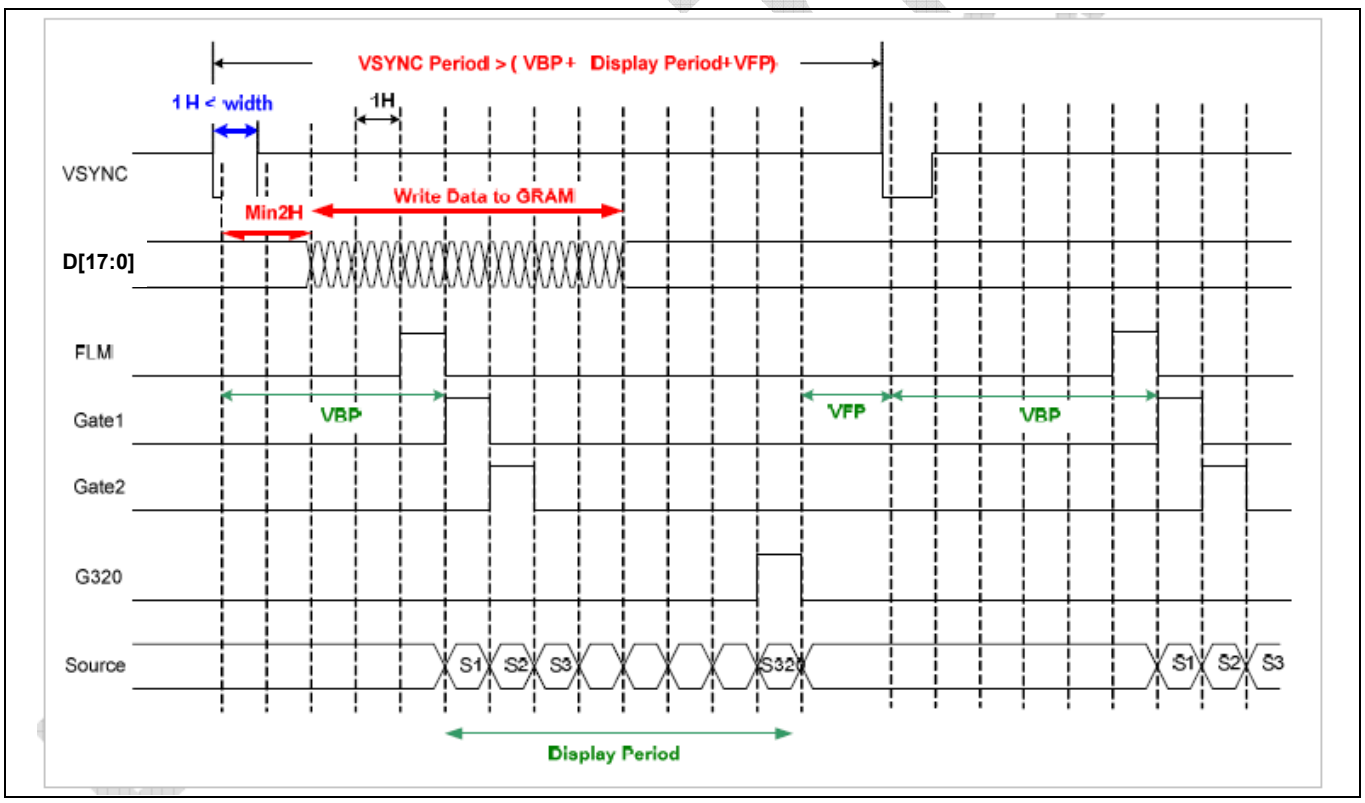

Figure50. Timing Diagram of VSYNC I/F

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below. The internal memory writing address counter is reset by VSYNC. So,

insure interval time between VSYNC falling and GRAM data writing.

Note.

1. VSYNC period should always be constant. If not, some degradation of display such as flicker may occur in LCD system.
2. Display data don't need to be written for every VSYNC period. For example, any system is working under 60Hz frame rate and 30-fps motion picture condition. So being written display data for every other frame would be enough.

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3.5.2. VSYNC INTERFACE MODE

3.5.2.1. Leading mode.

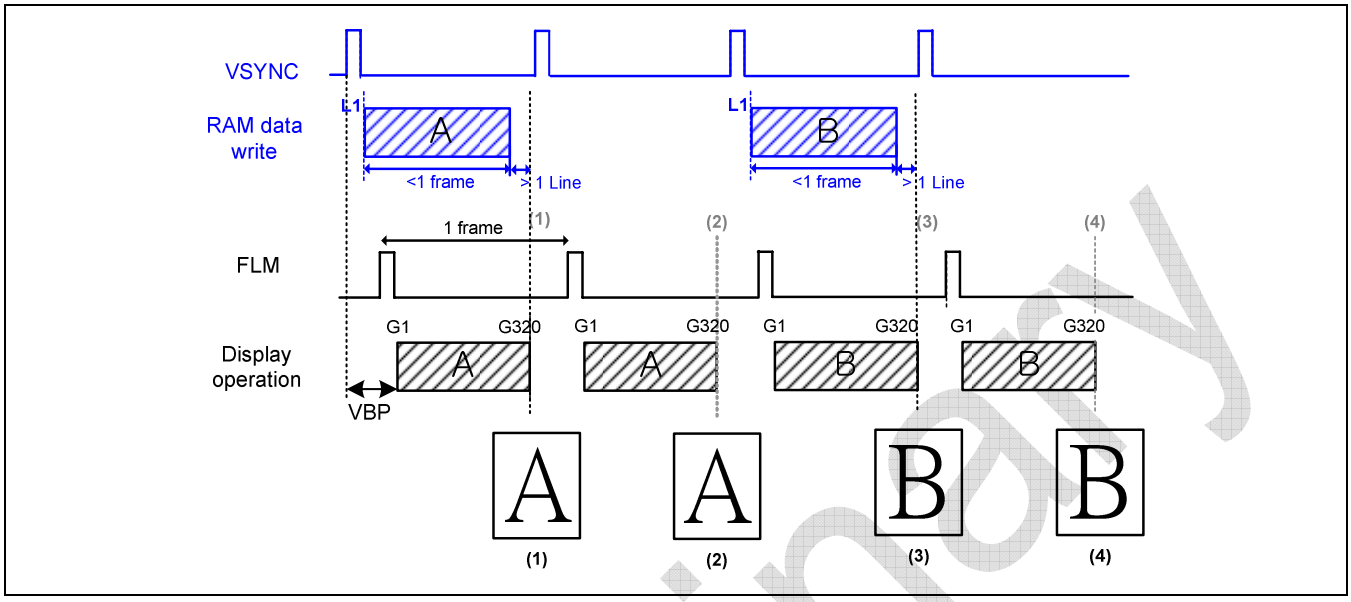

Figure51. Operation for Leading Mode of VSYNC Interface (VPL = 1)

3.5.2.2. Lagging mode.

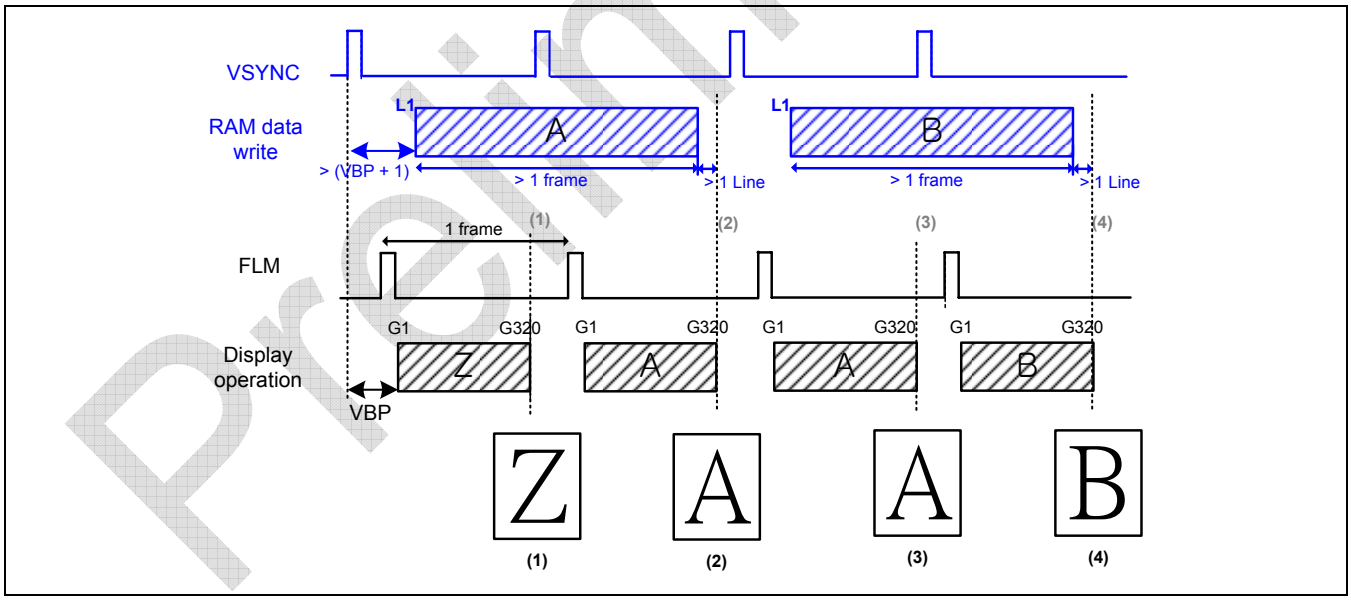

Figure52. Operation for Lagging Mode of VSYNC Interface (VPL = 1)

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*Internal clock frequency (fosc) [Hz] = Frame freq. × (Display line (NL) + Front porch (VFP) + Back porch (VBP)) × *37-Clock × Fluctuation*

Minimum speed for RAM writing [Hz] > 320 × Display line (NL) / {((Back porch (BP) + Display line (NL) – Margin) × 37 Clock) / fosc}

Note.

When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

An example is shown below.

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3.5.3. EXAMPLE

Display size	320RGB × 240 lines
Display line number	240 lines
Back/Front porch	8 lines / 8 lines (VBP / VFP)
Frame Frequency	60Hz

Internal clock frequency (fosc) [Hz] = 60 Hz × (320 + 8 + 8) lines× *37 clock × 1.1 / 0.9 = 694.61 kHz

Note.

1. Calculating the internal clock frequency requires considering the fluctuation. In the above case a 10% Fluctuation within the VSYNC period is assumed.
2. The fluctuation includes LSI production variation and air temperature fluctuation. Other fluctuations, including those for the external resistors and the supplied power, are not included in this example. Please keep in mind that a margin for these factors is also needed.
   Minimum speed for RAM writing [Hz] > 240 × 320 / {((14 + 320 – 2) lines × *37 clock) / 694.61 kHz} = 4.38 MHz
3. In this case RAM writing starts immediately after the falling edge of VSYNC.
4. The margin for display line should be two lines or more at the completion of RAM writing for one frame.

* 1H clock (default) = 148 display clock

Note) display clock = oscillator clock /3

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3.6. MDDI

3.6.1. INTRODUCTION TO MDDI

The S6D04K1 supports MDDI, mobile display driver interface. The physical layer of MDDI is based on a high-speed, differential serial interface. Both command and image data transfer can be achieved with MDDI.

MDDI host & client are linked by Data and STB line. Through Data line, either command or image data is transferred from MDDI host to MDDI client, and vice versa. Data is transferred by packet unit.

Through STB line, strobe signal is transferred. When the link is in "FORWARD direction," data is transferred from host to client; in "REVERSE direction," client transfers data to MDDI host.

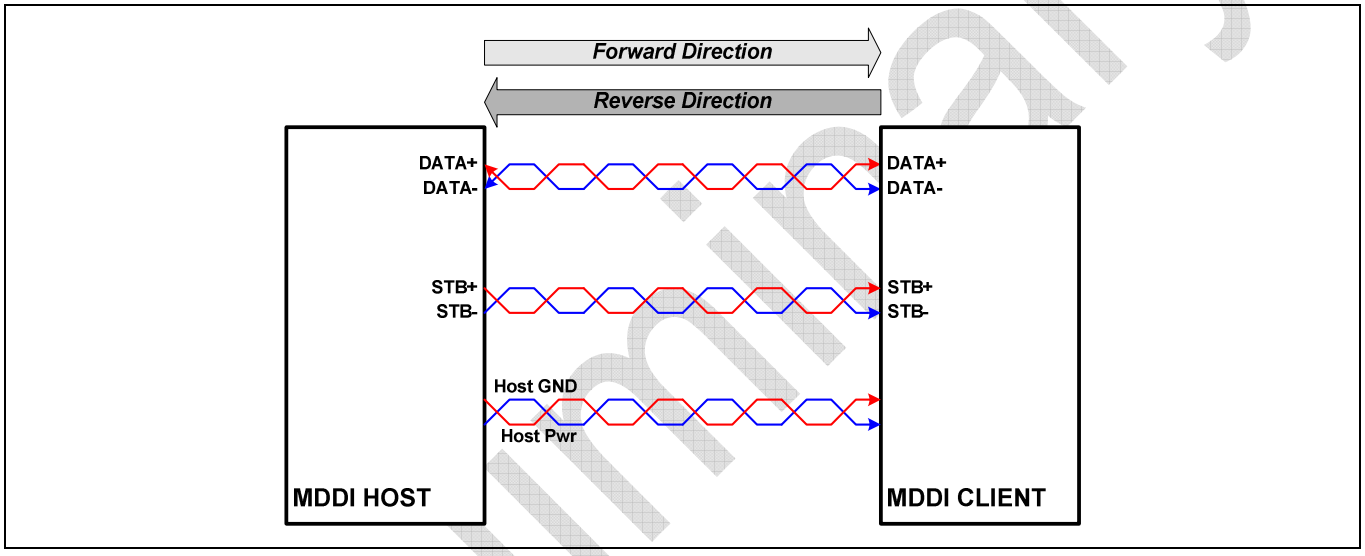

Figure53. Physical connection of MDDI host and client

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3.6.2. DATA-STB ENCODING

Data is encoded using a DATA-STB method. Data signal is bi-directional over a pair of differential cable while STB signal is unidirectional over a pair of differential cable driven by a host as shown in following Figure. Figure below illustrates how the data sequence “1110001011” is transmitted using DATA-STB encoding.

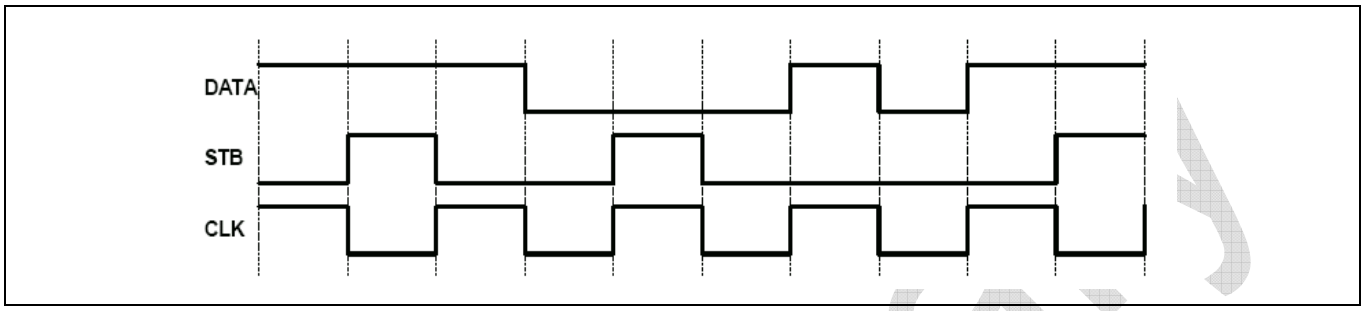

Figure54. Data-STB encoding

The Following figure shows a sample circuit to generate DATA and STB from input data, and then recover the input data from DATA and STB.

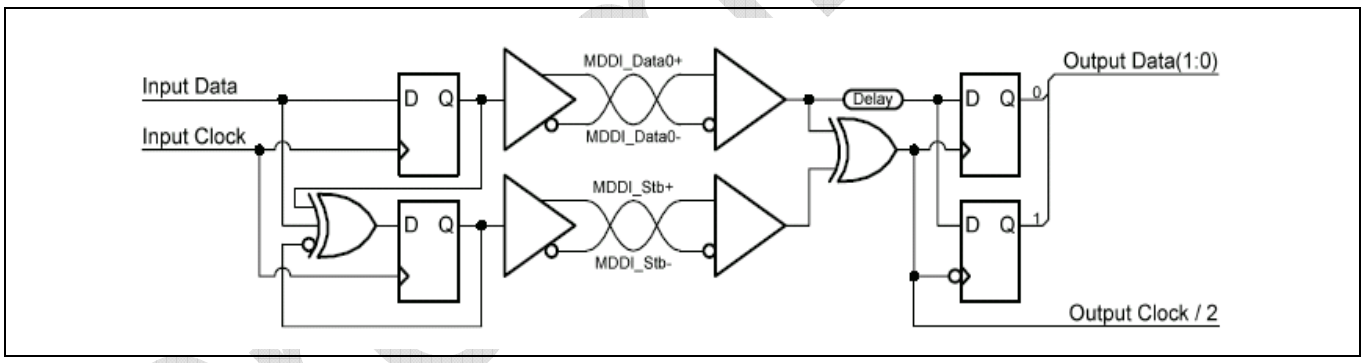

Figure55. Data / STB generation & recovery circuit

3.6.3. MDDI DATA & STB

The Data (MDP/MDN) and STB (MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets. The MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state, the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation, a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

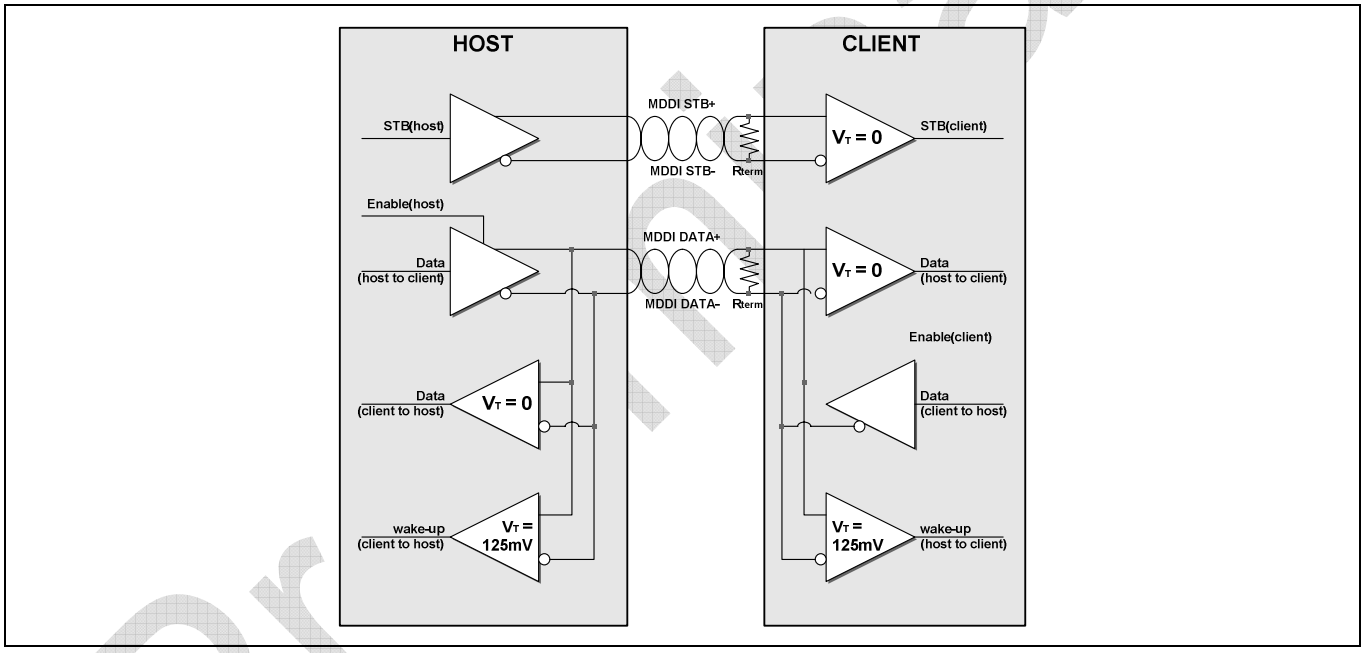

Figure56. Differential connection between host and client

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3.6.4. MDDI PACKET

MDDI transfer data in a packet format. MDDI host can generate and send packets.

In S6D04K1, several packet formats are supported. Packets are transferred from MDDI host to client (forward direction); but reverse encapsulation packet is transferred from MDDI client to host (reverse direction).

A number of packets, started by sub-frame header packet, construct 1 sub frame.

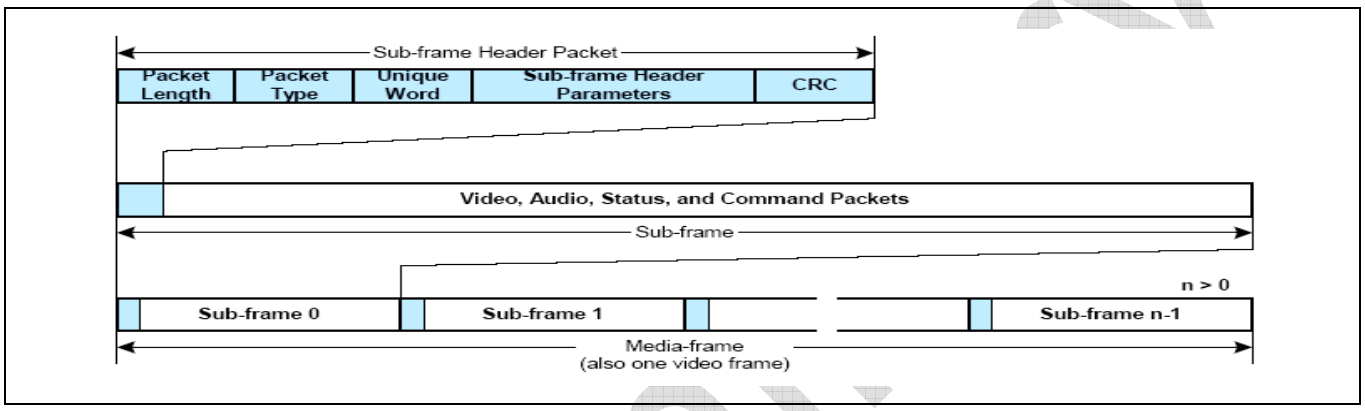

Figure57. MDDI packet structure

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frame construct media-frame together.

The following table describes 9 types of packets which are supported in S6D04K1.

Table 43. MDDI packet structure

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

Sub-frame header packet

packet length	packet type = 3bffh	unique word = 005ah	reserved1	sub-frame length	protocol version	sub-frame conut	media frame count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (sub-frame header packet is 3bffh)
unique word : Identify "This packet is sub-frame header packet"
reserved1 : not used (set zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packets
mddi frame count : specifies number of media frames
CRC : error check

Figure58. Sub-Frame header packet structure

Register access packet

Basis of Register Data List is 4byte unit. Therefore, when write 1parameter, remainders must fill by 0.

packet length	packet type = 146	bClient ID	Read / Write Info	Register Address	Paramter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	Packet Length -14byte	2 bytes

packet length : packet length not including packet length block
packet type : packet type (Register Access packet is 146 (decimal))
bClient ID : set to all zero
Read / Write Info : to write register value , bits [15:14] = " 00 "
to request register value , bits[15: 14] = " 10 "
bits [13 : 0] refer to VESA SPEC
Register Address : Register address is written here
Parameter CRC : To check error from packet length to register address
Register Data List : A list of 4byte register data values to be written to LDI
CRC : To error check register data list
※ Basis of Register Data List is 4-byte unit. Therefore, When Register Parameter is not Multiply of 4, Remainder bits must fill by 0

000000FFh
Register Data list

Figure59. Register access packet structure

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Video Stream packet

packet length	packet type=16	bClientID	video data format descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom edge	X start	Y start
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length - 26 bytes	2 bytes

packet length: packet length not including packet length block
packet type: packet type(video stream packet is 16)
bClientID: reserved, set all 0
video data format descriptor bits[15:13] = 010 : raw RGB format(fixed value)
bits [12] = 1 : Only packed type is available(fixed value)
bits [11:0] = 1000_1000_ 1000: 24 bit pixel
bits [11:0] = 0110_0110_ 0110: 18 bit pixel
bits [11:0] = 0101_0110_ 0101: 16 bit pixel
pixel data attributes bits [1:0] = 11 : displayed both eyes (fixed value)
bits [5] = 1 : X left edge. Y start edge is not defined (fixed value)
other bits are all zero
X left edge : Not used. set all zero
Y top edge : Not used. set all zero
X right edge : Not used. set all zero
Y bottom edge : Not used. set all zero
X start : Not used. set all zero
Y start : Not used. set all zero
Pixel count: Write number of pixel
Paramter CRC : To error check from packet length to pixel count.
pixel data: pixel data info. number of pixel data must not be over 65509
pixel data CRC : To pixel data error check.

Figure60. Video stream packet structure

Filler packet

packet length	packet type = 0	filler bytes (all zero)	CRC
2 bytes	2 bytes	packet length - 4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type(Filler packet is 0(decimal))
filler bytes : set to all zero(The size is under packet length availabe)
CRC : To error check

Figure61. Filler packet structure

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Link shutdown packet

packet length	packet type = 69	CRC	All zeros
2 bytes	2 bytes	2 bytes	16 bytes

packet length : packet length not including packet length block
packet type : packet type(Link shutdown packet is 69(decimal))
CRC : To error check
All zeros : write all zero (size is 16 bytes)

Figure62. Link shutdown packet structure

: fixed value

For More information about MDDI packet, refer to VESA MDDI spec.

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3.6.5. PANEL CONTROL

S6D04K1 supports video stream packet for memory write and register access packet for register write/read. Followings are some examples of memory and register write/read sequence.

3.6.5.1. Writing Video Data to Memory Sequence

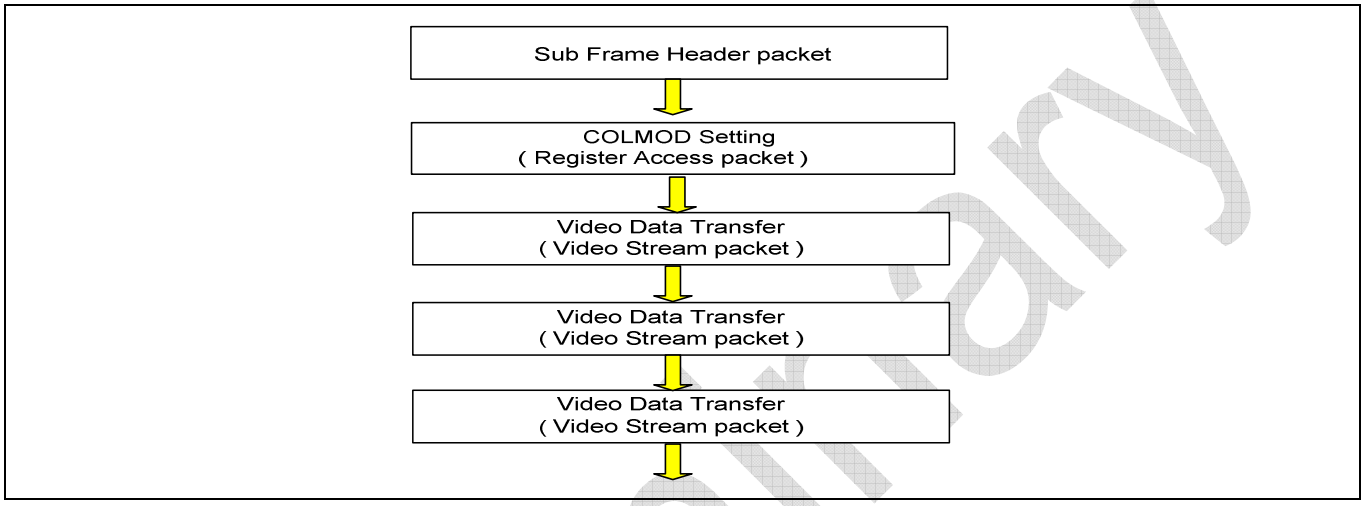

Figure63. Writing video data to memory sequence

COLMOD setting in MDDI

Video data format descriptor[11:0]	COLMOD[2:0]
1000_1000_1000	111 (16M color)
0110_0110_0110	110 (262k color)

Note: If user want to transfer 888(24bit) video data, Set COLMOD[2:0]="111" prior to Video Stream Packet

3.6.5.2. Writing Register Sequence

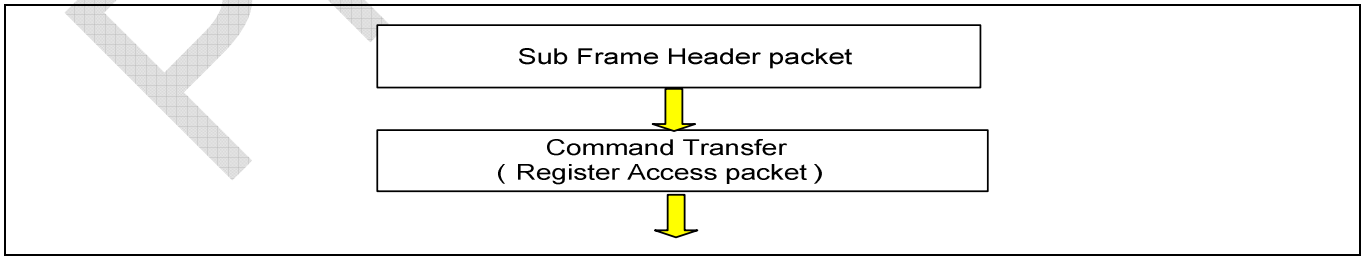

Figure64. Writing register sequence

3.6.5.3. Reading Video Data from Memory Sequence

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In order to read a pixel data from memory(readable one pixel only), the following sequence should be programmed. Memory read command (2EH) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

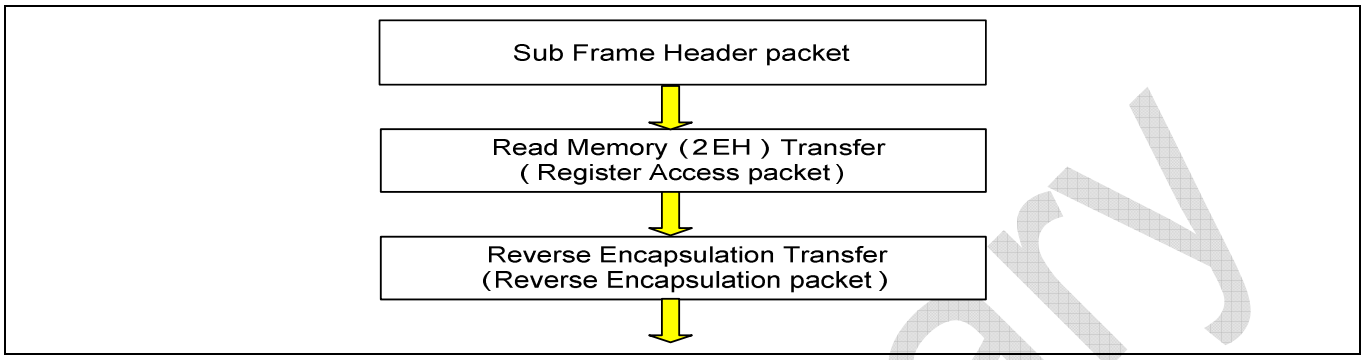

Figure65. Reading video data from memory sequence

3.6.5.4. Reading Register Sequence

In order to read registers, the following sequence should be programmed. Register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

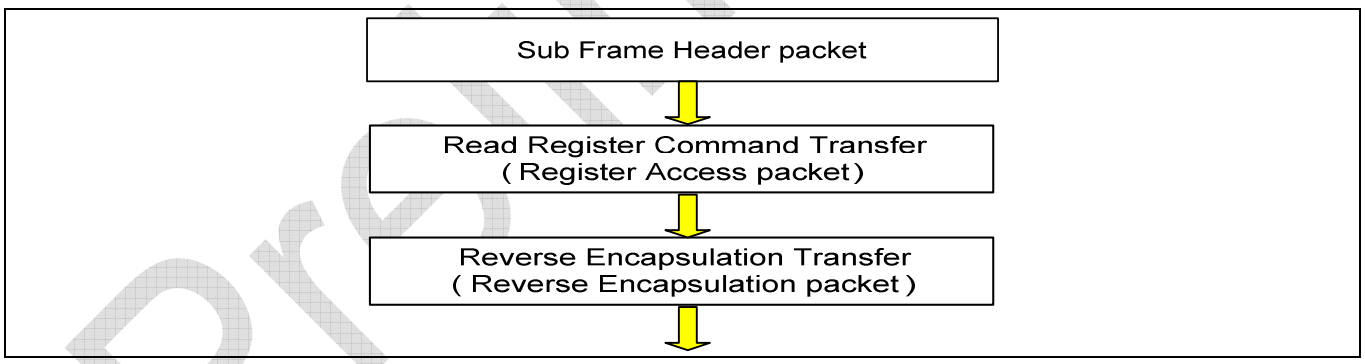

Figure66. Reading register sequence

Note: Only Level 1 Registers are readable in MDDI.

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3.6.6. TEARING-LESS DISPLAY

In S6D04K1, the matching between data writes timing and written data display timing is important. If timing is mismatched, tearing effect can occur.

To avoid display tearing effect, two possible ways are suggested.

First case is that data write is slower than speed of displaying written data. In this case, data write speed is not critical, but current consumption in interface will be increased because data transfer time is long. Data write time is selected widely in this case.

Other case is that data write is faster than speed of displaying written data. In this case, data update speed is very high so that transfer time is short. So current consumption in interface can be minimized, but it requires fast data transfer. The most important thing is to avoid data scan conflicts with data update.

The following figures describe some examples to avoid display tearing phenomenon.

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A. Display speed is slower than data write.

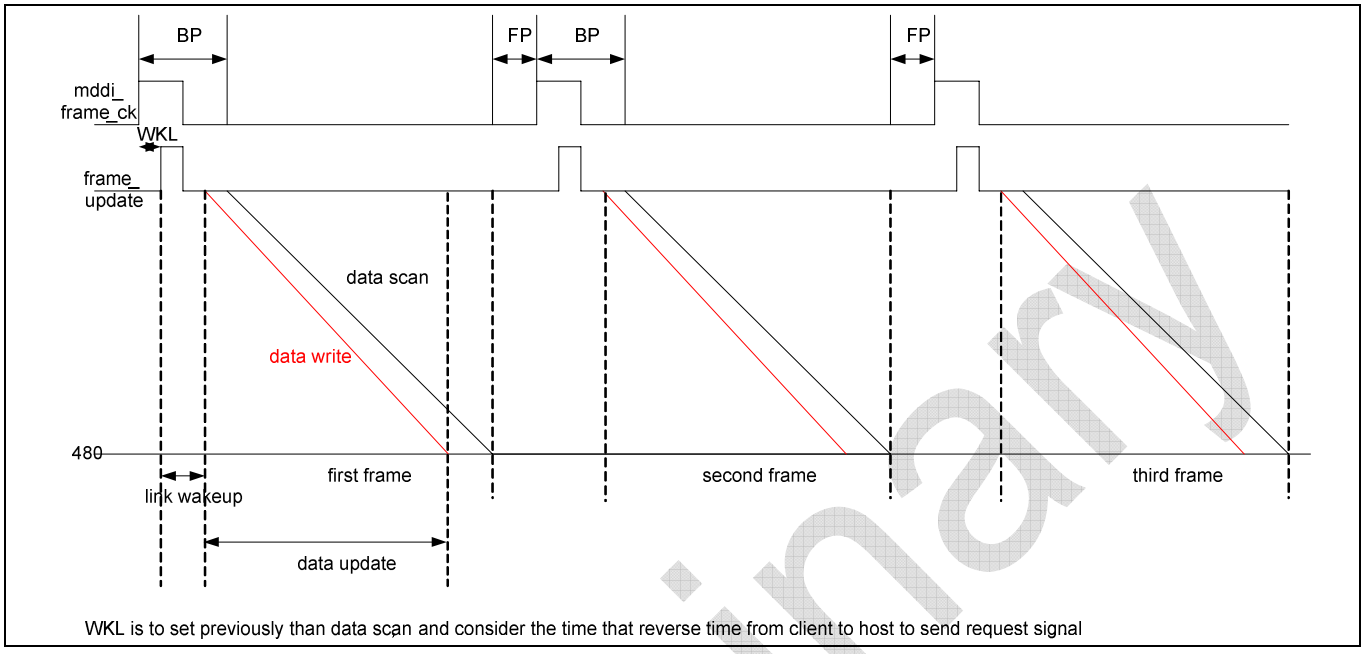

Figure67. Tearing-less display: data write speed is faster than display

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B. Display speed is faster than data write.

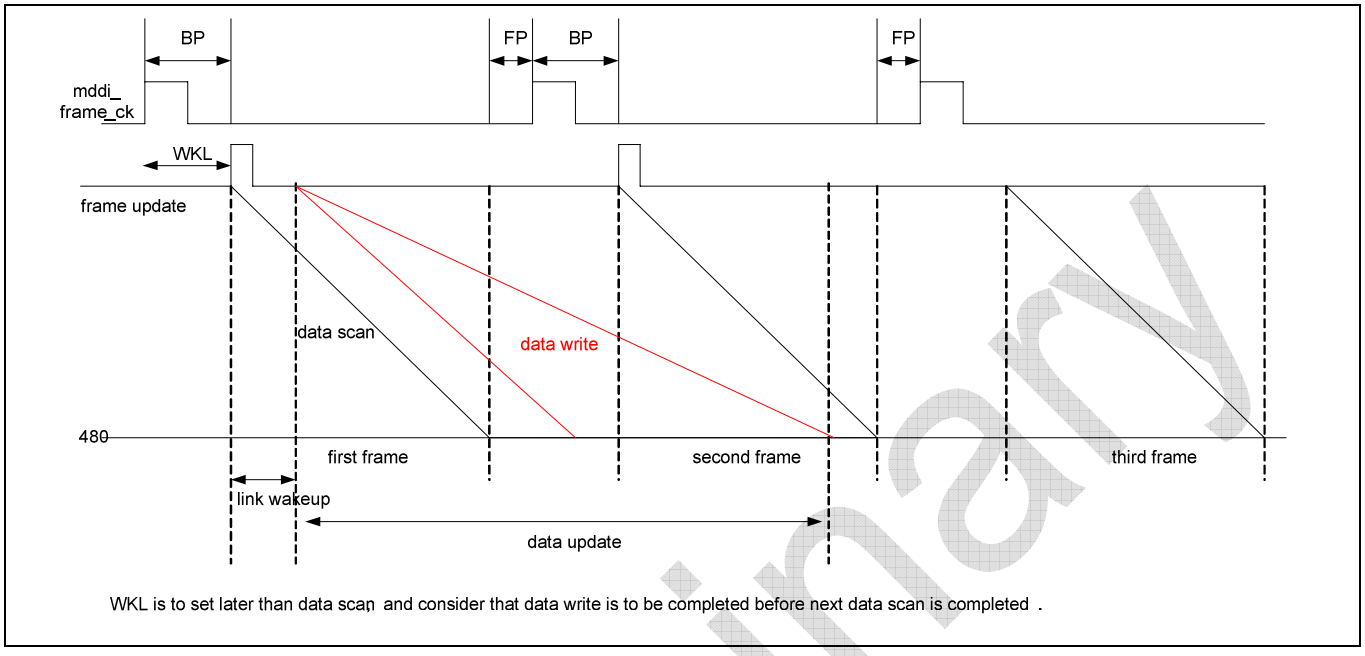

Figure68. Tearing-less display: display speed is faster than data write

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3.6.7. HIBERNATION / WAKE-UP

S6D04K1 support hibernation mode to save interface power consumption. MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force MDDI link into hibernation frequently to save power consumption.

During hibernation mode, the hi-speed transmitters and receivers are disabled and the low-speed & low-power receivers are enabled in order to detect wake-up sequence.

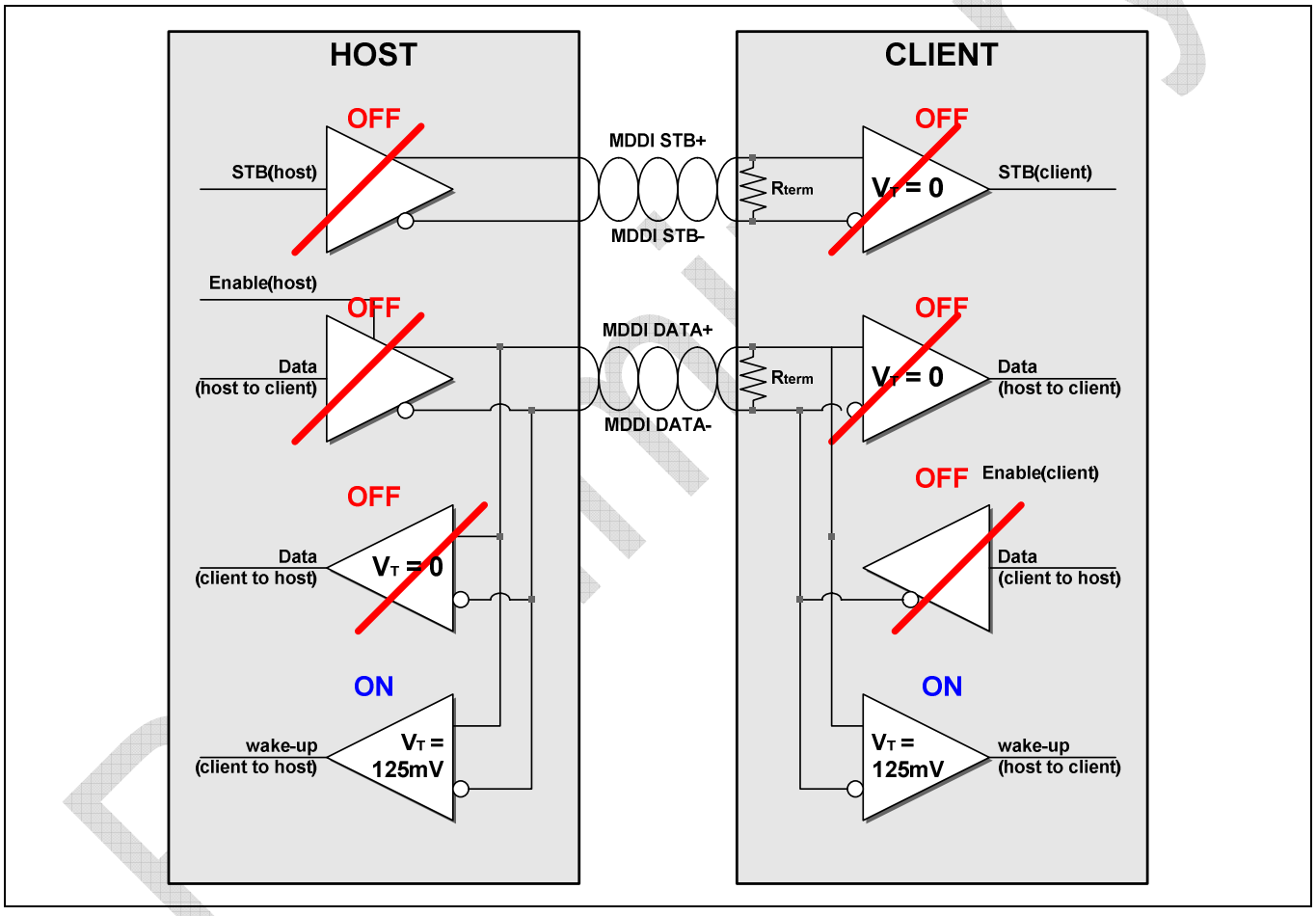

Figure69. MDDI transceiver / receiver state in hibernation

When the link wakes up from hibernation, the host and client exchange a sequence of pulses. These pulses can be detected using low-speed, low-power receivers that consume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operating speed.

Either the client or the host can wake up the link; Host-initiated link wakeup and Client-initiated link wakeup.

3.6.8. MDDI LINK WAKE-UP PROCEDURE

A. Host-initiated Link Wake-up Procedure

The simple case of a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.

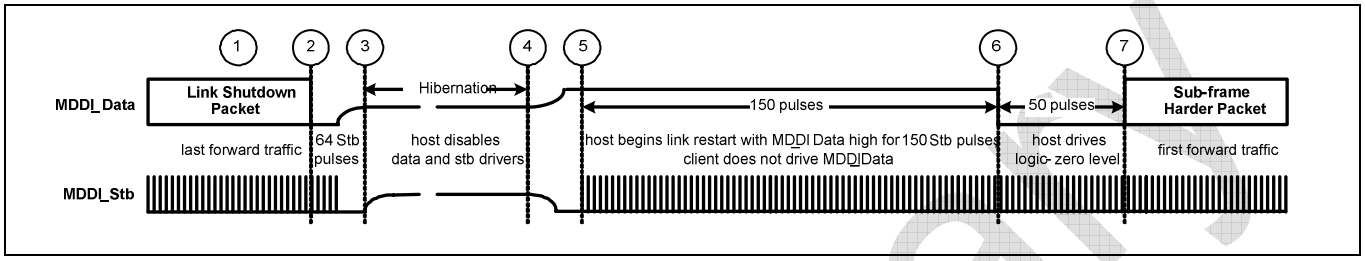

Figure70. Host-Initiated link wake-up sequence

The Detailed descriptions for labeled events are as follows:

1. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

2. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data to a logic-zero level, and then disables the MDDI_Data output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC.
It may be desirable for the client to place its high-speed receivers for MDDI_Data and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point 3.

3. The host enters the low-power hibernation state by disabling the MDDI_Data and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state.
It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation.
The client is also in the low-power hibernation state.

4. After a while, the host begins the link restart sequence by enabling the MDDI_Data and MDDI_Stb driver outputs. The host drives MDDI_Data to a logic-one level and MDDI_Stb to logic-zero level for at least the time it takes for the drivers to fully enable their outputs.
The host shall wait at least 200n sec after MDDI_Data reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive

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high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

5. The host drivers are fully enabled and MDDI_Data is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having logic-zero level on MDDI_Data for duration of 150 MDDI_Stb cycles.

6. The host drives MDDI_Data to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

7. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point 7. The MDDI host generates MDDI_Stb based on the logic level on MDDI_Data so that proper data-strobe encoding commences from point 7.

B. Client-initiated Link Wake-up Procedure

An example of a typical client-initiated service request event with no contention is illustrated in the following figure.

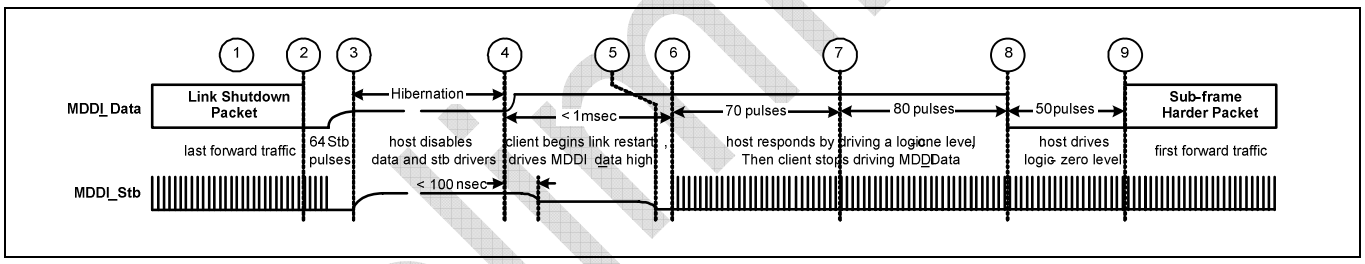

Figure71. Client-Initiated link wake-up sequence

The Detailed descriptions for labeled events are as follows:

1. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

2. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data to a logic-zero level, and then disables the MDDI_Data output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point 3.

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3. The host enters the low-power hibernation state by disabling its MDDI_Data and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

4. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logical-zero level in the client before the host enables its MDDI_Stb driver. The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client. After that, the client enables its MDDI_Data driver while driving MDDI_Data to a logic-one level. It is allowed for MDDI_Data and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200n sec.

5. Within 1m sec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_Data and MDDI_Stb driver outputs. The host drives MDDI_Data to a logic-one level and MDDI_Stb to a logical-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200n sec after MDDI_Data reaches a valid logic-one level and MDDI_Stb reaches a valid fully-driven logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

6. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data at a logic-one level for a total duration of 150 MDDI_Stb pulses through point 8. The host generates MDDI_Stb in a manner consistent with sending a logical-zero level on MDDI_Data. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.

7. The client continues to drive MDDI_Data to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data driver at point 7. The host continues to drive MDDI_Data to a logic-one level for duration of 80 additional MDDI_Stb pulses, and at point 8 drives MDDI_Data to logic-zero level.

8. The host drives MDDI_Data to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

9. After asserting MDDI_Data to logic-zero level and driving MDDI_Stb for duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point 9 by sending a Sub-frame Header Packet.
The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

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3.6.9. CLIENT-INITIATED LINK WAKE-UP

S6D04K1 supports VSYNC based client-initiated link wake-up. As client-initiated wake-up action is executed in hibernation state only, the register setting for wake-up have to be set before link shut-down.

A. VSYNC Based Link Wake-up

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register (E0h: VWAKE_EN) is set, client initiated wake-up is executed in synchronization with the vertical-sync signal which generated in S6D04K1. Using VSYNC based link wake-up, tearing-less display can be accomplished if interface speed and wake-up time is well known.

The following figure shows detailed timing for VSYNC based link wake-up.

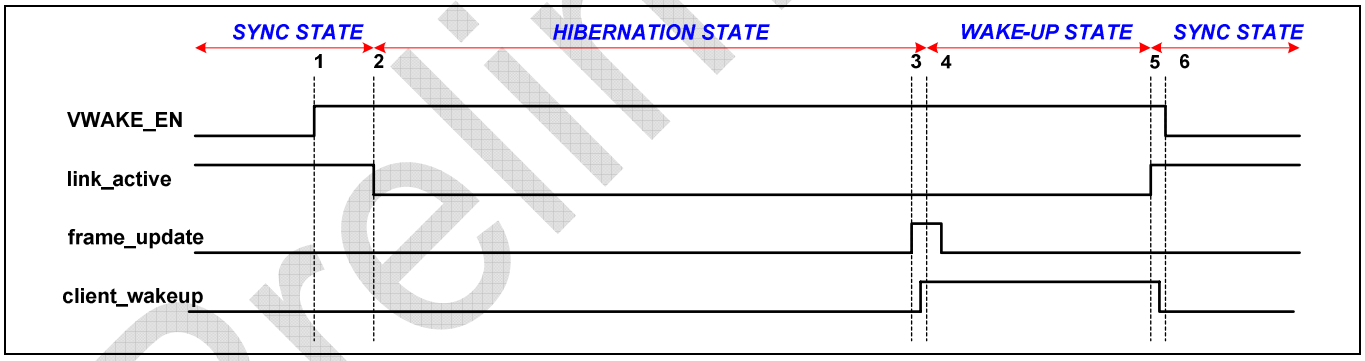

Figure72. VSYNC based link wake-up procedure

The Detailed descriptions for labeled events are as follows:

1. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.

2. Link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the S6D04K1.

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3. Frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up can be set using WKF and WKL (E1h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.

4. Client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

5. Link_active goes high after the host brings the link out of hibernation.

6. After link wake-up, client_wakeup signal and the VWAKE_EN register are cleared automatically.

3.6.10. MDDI OPERATION

In MDDI, six operation modes are available. The following table describes six modes.

Table 44. MDDI Opreration State

State	OSC	Booster Circuit	Internal Logic Status	MDDI I/O	Wake-up by
INIT_ HIBER	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link hibernation	Hibernation driver ON	Host – Initiated
WAIT	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
NORMAL	ON	Enabled	Display ON /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
SLEEP	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
HIBER	ON	Enabled	Display ON /Internal Logic ON MDDI Link hibernation	Hibernation driver ON	Host – Initiated Client –Initiated (VSYNC)
STOP	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link OFF	Driver All OFF	RESET

INIT_HIBER: Initial status when external power is connected to the IC. In this state, internal oscillator is OFF, and MDDI link is in hibernation state. As no command or signal is applied to the IC except RESET input and booster

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circuit is OFF, and internal logic is ON.

WAIT: After the wake-up sequence, the IC is in WAIT state. MDDI link is in SYNC, and internal logic is ON, and booster is still OFF because no other register access or video stream packet is transferred to the IC.

NORMAL: MDDI link, booster circuit, and internal logic circuit are ON. Register access or Video data transfer is available in NORMAL state.

HIBER: When no more video data update is needed, MDDI link is in hibernation so that interface power can be reduced. Internal booster & logic circuits are still operating. MDDI link wakeup will be accomplished when VSYNC wakeup register is set before hibernation

SLEEP: This state is set by register access. Booster is OFF, but MDDI link is ON. MDDI link and internal logic have to be in SYNC because the IC must receive commands for power save or normal operation

STOP: STOP state is set by MDDI_SLP register access (E0h). In this state, MDDI link, internal oscillator, Boosters are all OFF. But internal logic is still ON. To release STOP state, input reset signal. After reset, status is INIT_HIBER state.

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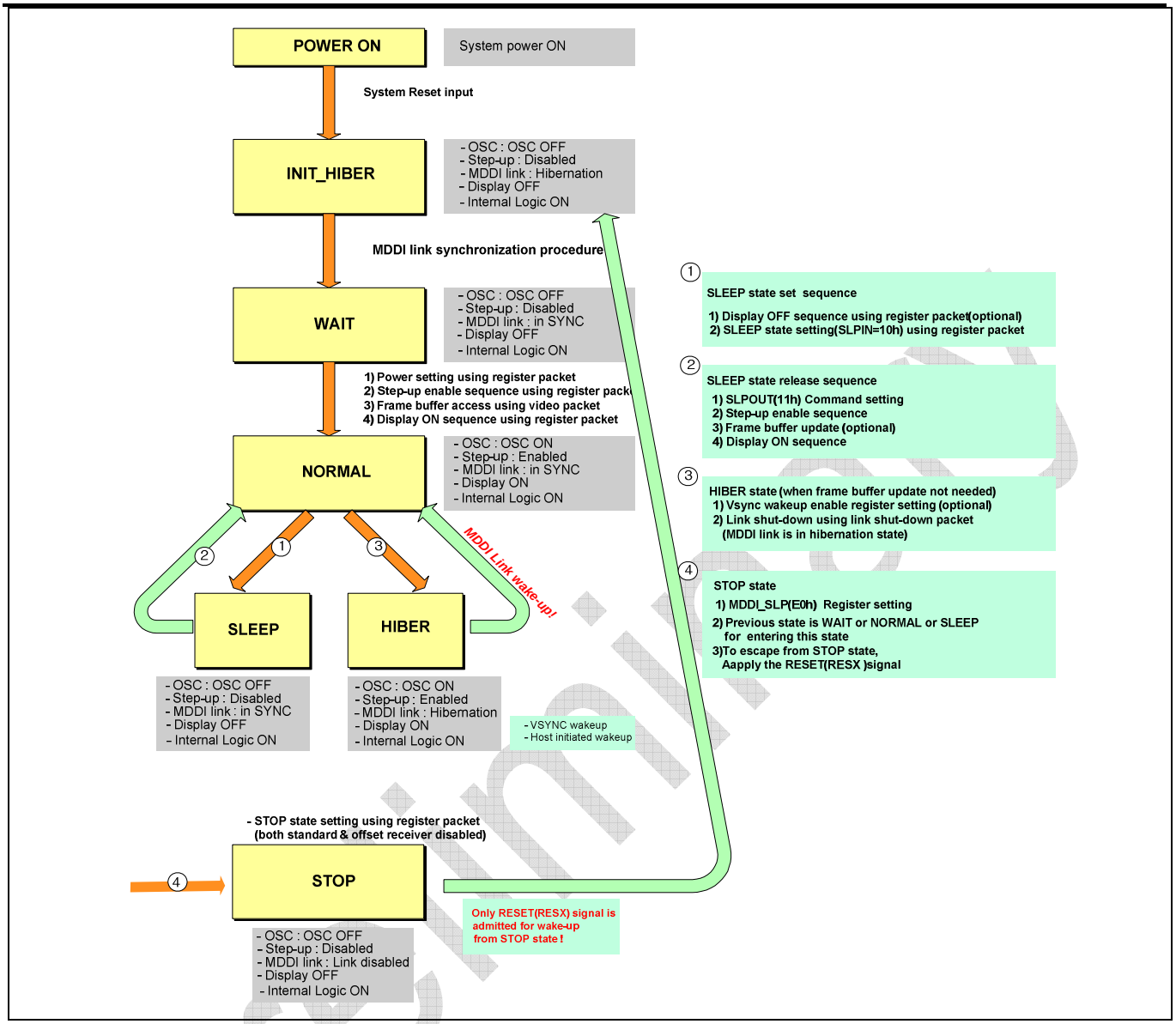

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CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 Power
4.2 Source
4.3 Display Data RAM
4.4 MTP Control
4.5 Tearing Effect Output
4.6 Sleep Out Command and Self-diagnostic Functions
4.7 MIE Function
4.8 Deep Standby Mode
4.9 Display On/Off Sequence

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4. FUNCTIONAL DESCRIPTION

4.1. POWER

4.1.1. POWER ON / OFF SEQUENCE

VDD3 and VCI can be applied in any order.

VDD3 and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDD3 must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDD3 or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note.

1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before the reception of Sleep Out command. Same is the case between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 4.1.1.1, it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

The power on/off sequence is illustrated in the next pages.

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4.1.1.1. Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDD3 have been applied – otherwise, correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

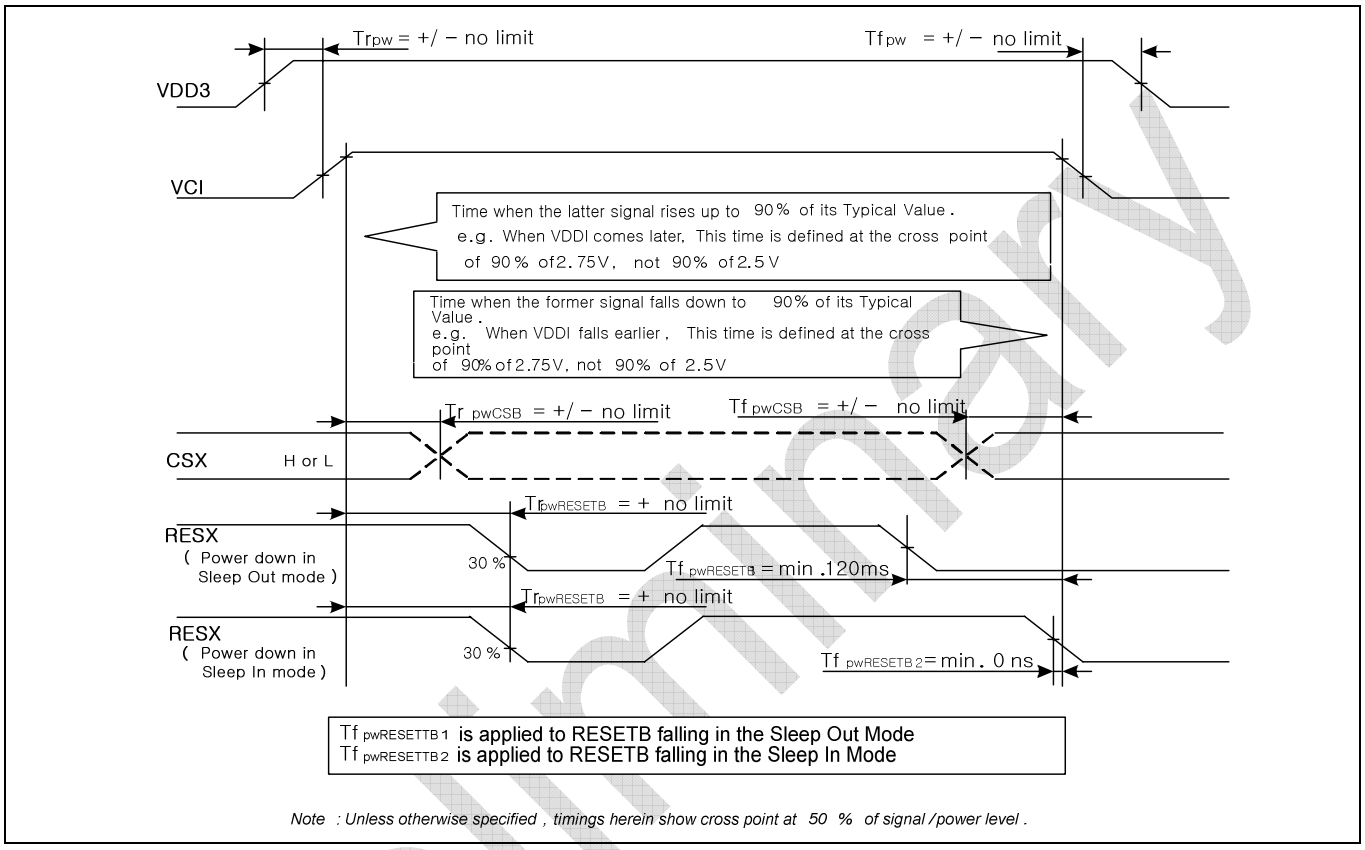

Figure73. RESX Line is Held High or Unstable by Host At Power On

Note.

Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

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4.1.1.2. Case 2 – RESX line is held low by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VCI and VDD3 have been applied.

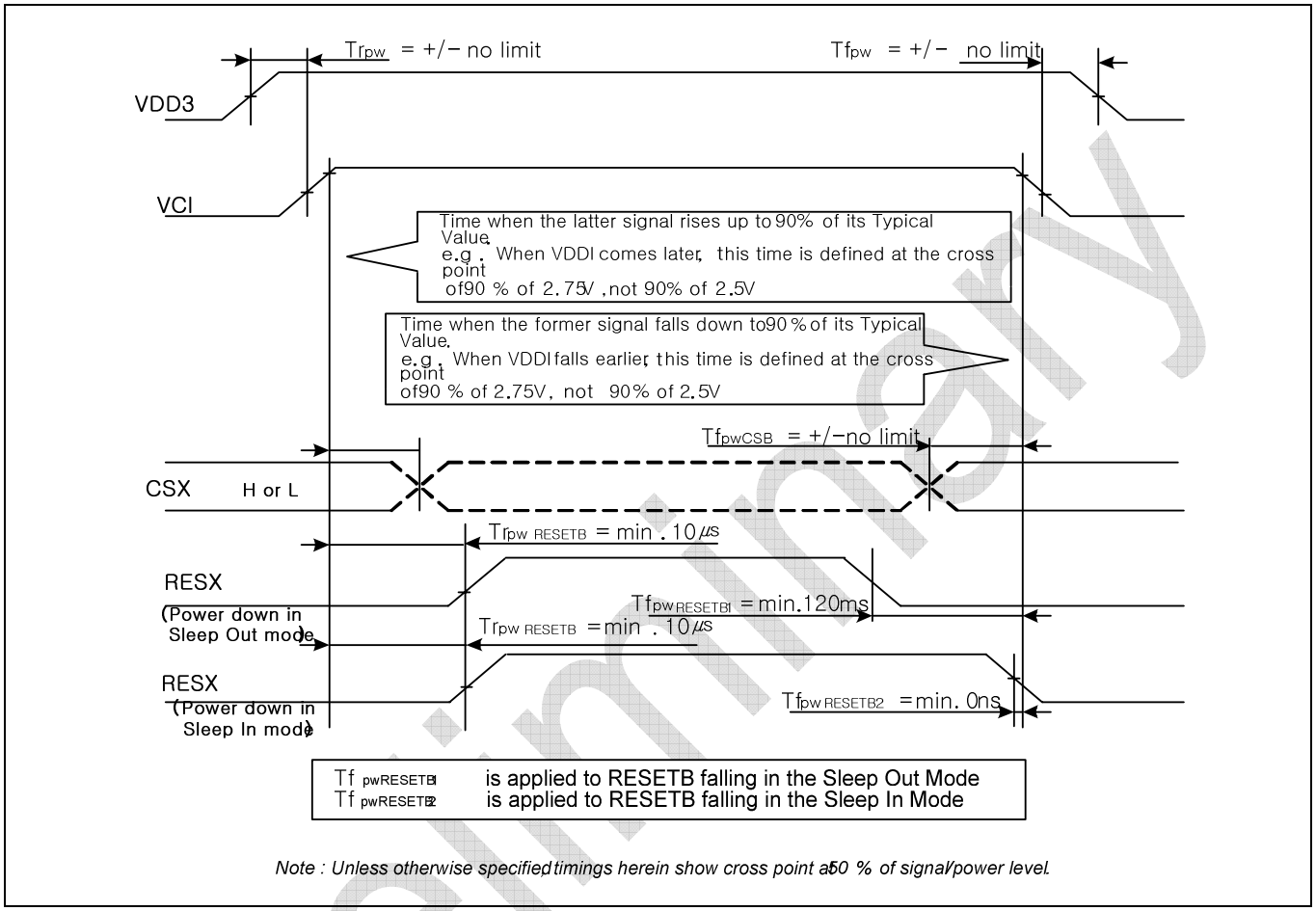

Figure74. RESX Line is Held Low by Host At Power On

Note.

Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

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4.1.2. ABRUPT POWER OFF

The abrupt power-off represents a situation where, for e.g, a battery is removed without the expected power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abrupt power-off, the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power-On Sequence” powers it up.

4.1.3. POWER LEVELS

6 level modes are defined they are in order of Maximum power consumption to Minimum power consumption.

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out
   In this mode, the full display area is used but with 8 colors,
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors
5. Sleep In Mode
   In this mode, the step up circuit, Internal oscillator and panel driver circuit are stopped. Only the MPU interface and memory works with VDD3 power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and VDD3 are removed

Note.

Transition between modes 1-5 is controllable by MPU commands. Mode 6 is entered only when both Power supplies are removed.

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4.1.4. POWER FLOW CHART FOR DIFFERENT POWER MODES

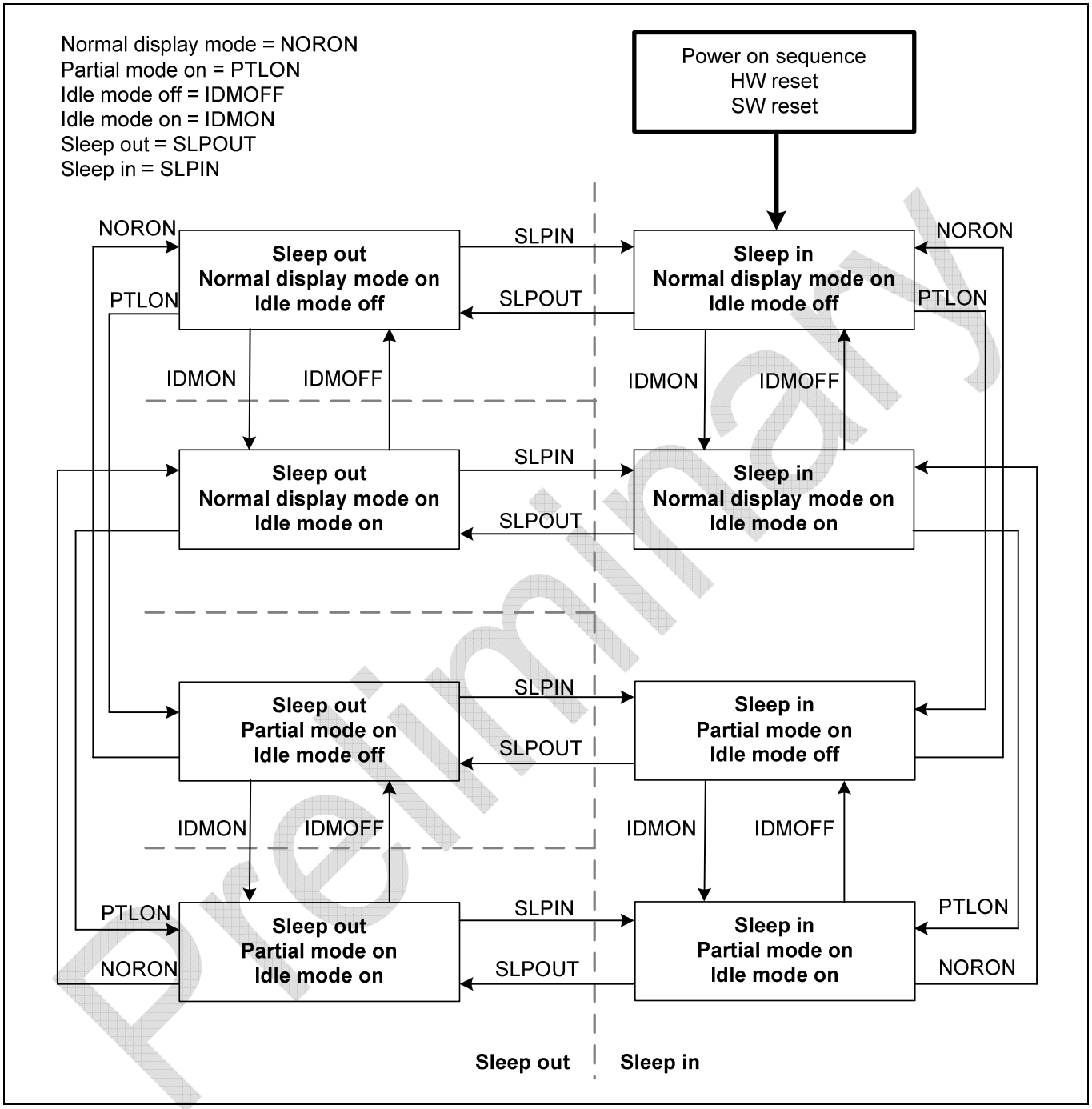

Figure75. Power Flow Chart

Note.

1. There is no abnormal visual effect when there is a change from one power mode to another power mode.
2. There is no limitation, which is not specified by this spec, when there is a change from one power mode to another power Mode

4.1.5. POWER SUPPLY

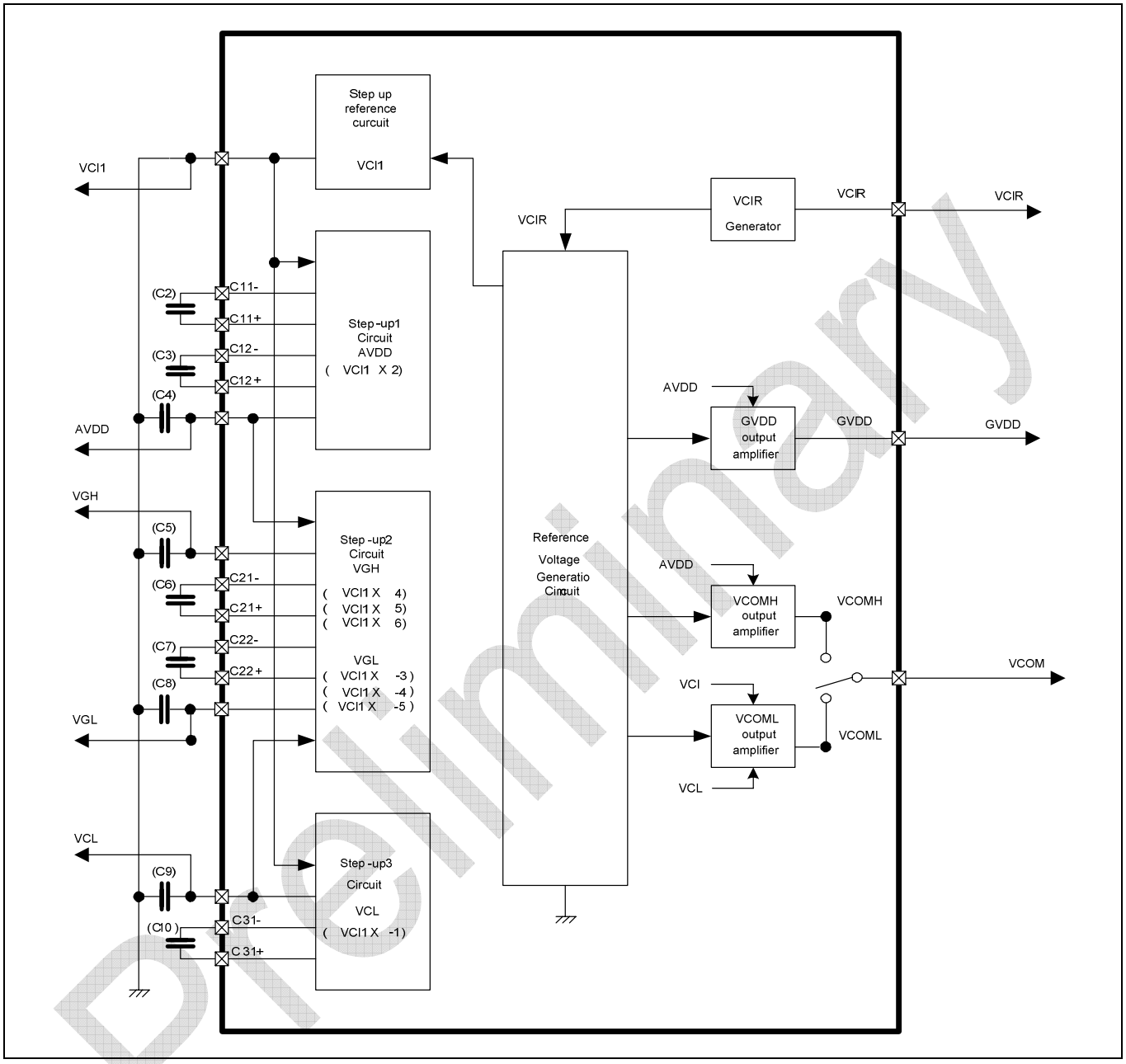

Figure76. Configuration of the Internal Power-Supply Circuit

The step-up circuits consist of step-up circuits 1 to 3. Step-up circuit 1 doubles the voltage which is supplied to VCI1 for AVDD level, and VCI1 is positively amplified by 4 or 5 or 6 times for VGH level and negatively amplified by 3 or 4 or 5 times for VGL level in step-up circuit 2. Step-up circuit 3 flips the VCI1 level and generates the VCL level. These step-up circuits generate the supply powers of AVDD, VGH, VGL and VCL in sequence after regulation. The regulated GVDD is for the grayscale voltage, another regulated VCOMH and the other regulated VCOML are for VCOM which is connected to counter electrode of TFT LCD panel, and generate each level

depending on that voltage. Connect VCOM to the TFT panel.

4.1.5.1. Pattern diagrams for voltage setting

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.

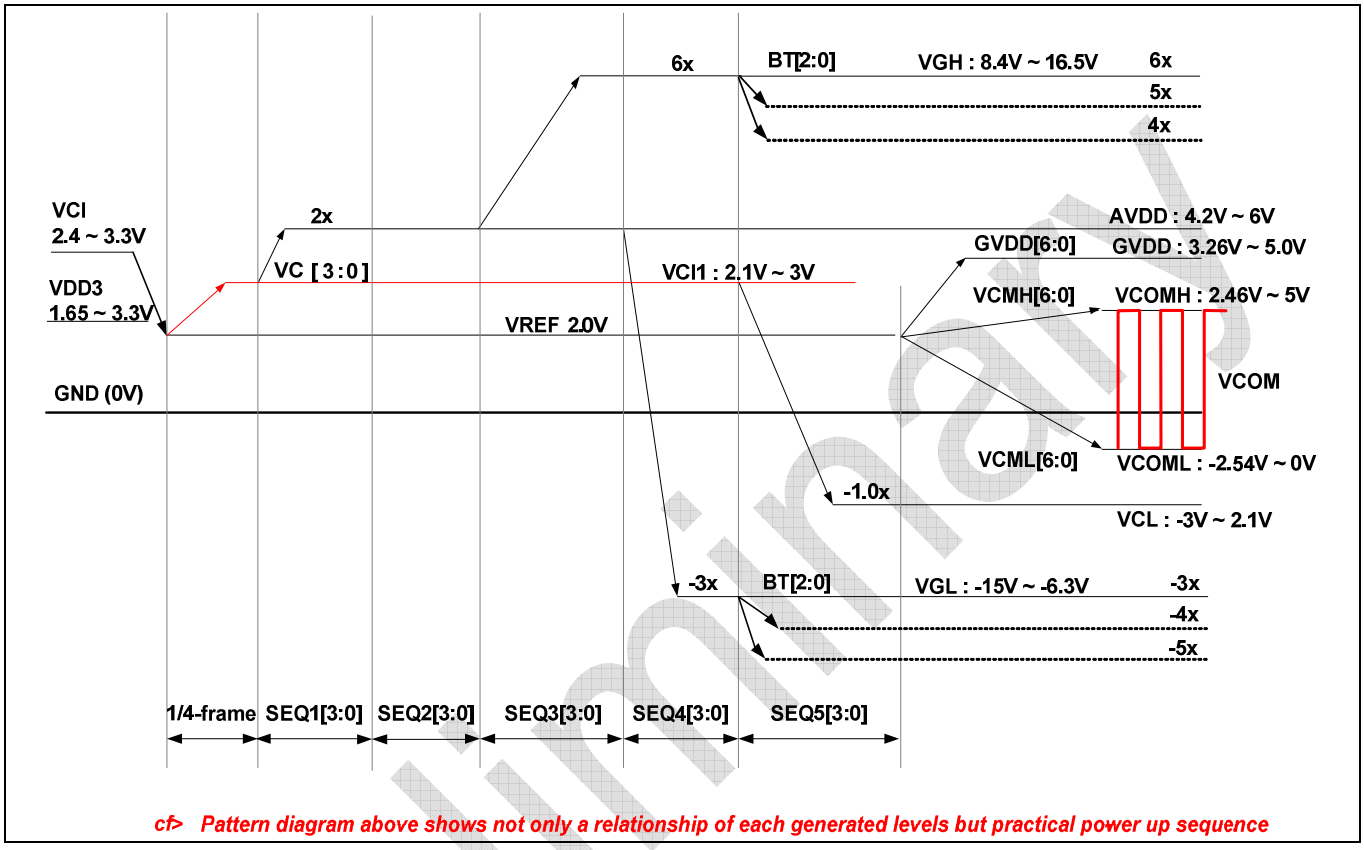

Figure77. Sequence of Power Boosting S6D04K1

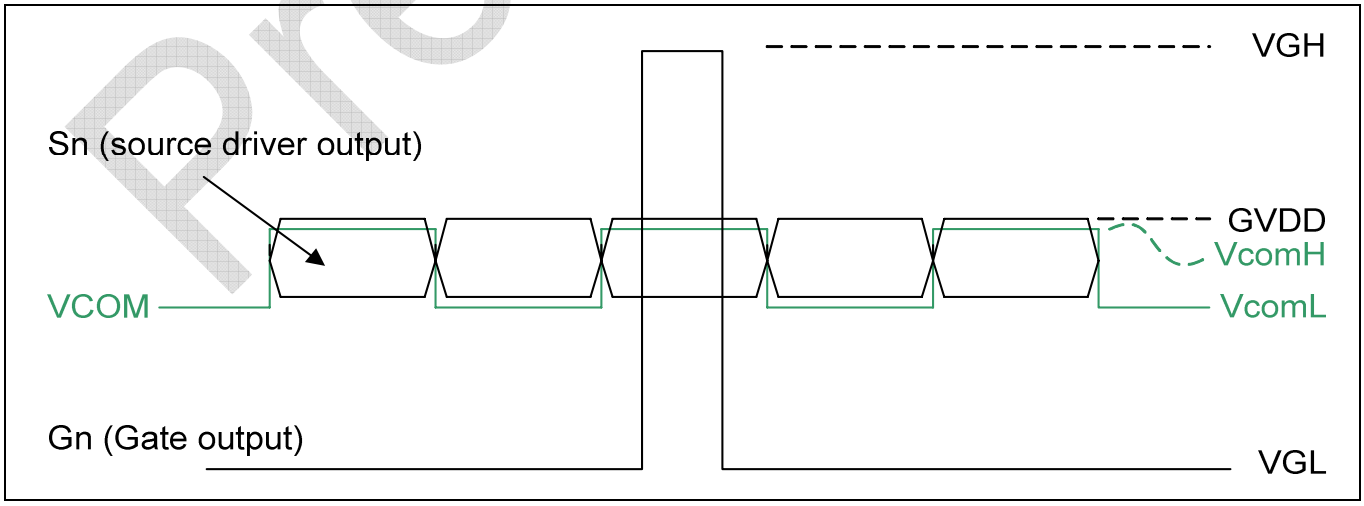

Figure78. Power-Up Pattern Diagram & An Example of Source/VCOM Waveforms

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4.2. SOURCE

4.2.1. GAMMA ADJUSTMENT FUNCTION

S6D04K1 provides the gamma adjustment function to display 262,144 colors simultaneously for each R/G/B color. The gamma adjustment executed by the high/ mid/ low level adjustment registers determines 11 grayscale reference levels. Furthermore, since the high-level adjustment register, mid-level adjustment register and the low-level adjustment register have the positive polarities and negative polarities, you can adjust them to match LCD panel and a gamma for each R/G/B color, respectively.

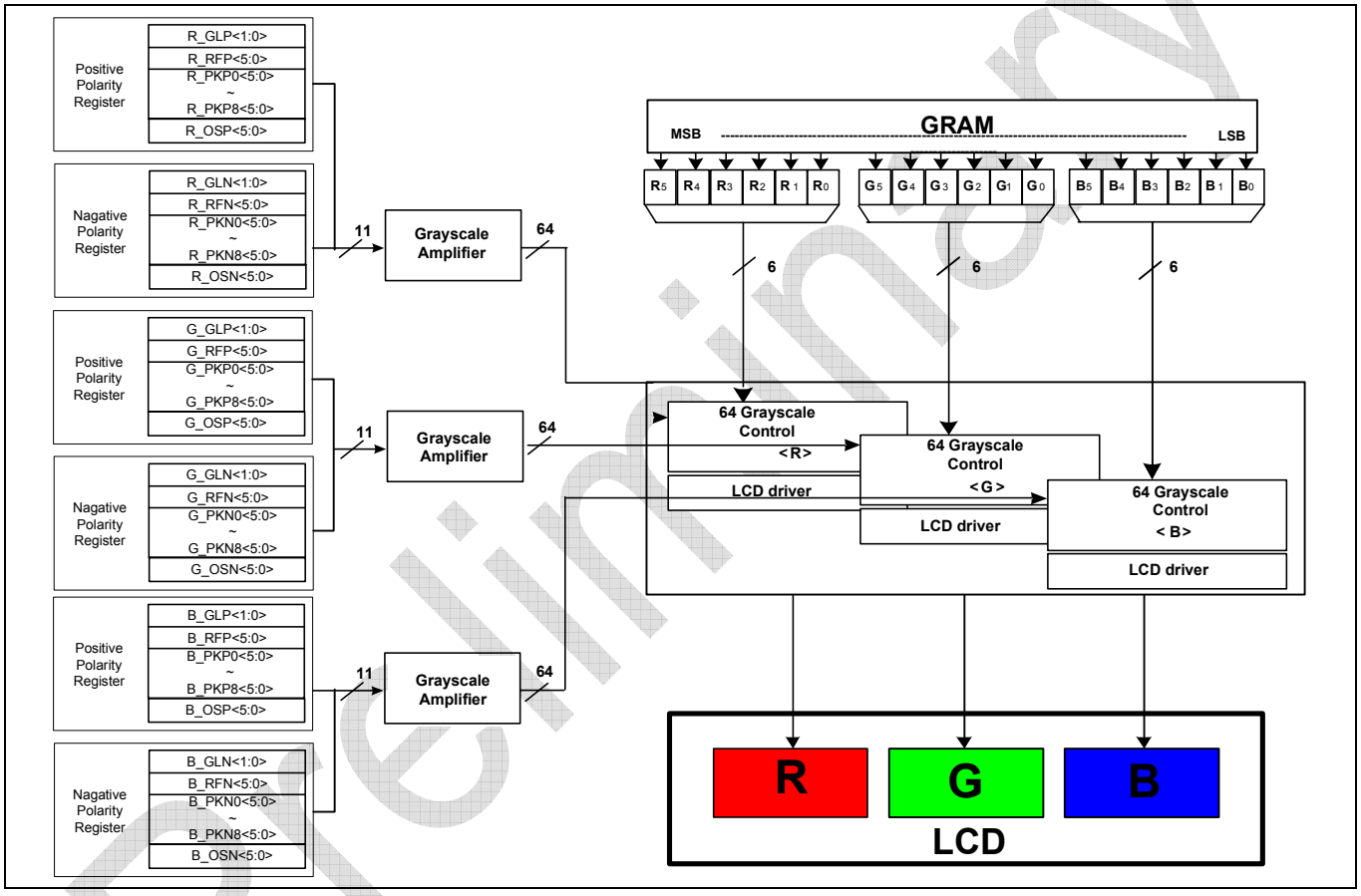

Figure79. Gamma Adjustment Block Diagram

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4.2.2. GAMMA CURVE

4.2.2.1. Gamma curve 1 (GC0)

Gamma Curve 1 (GC0), applies the function. $y = x^{2.2}$

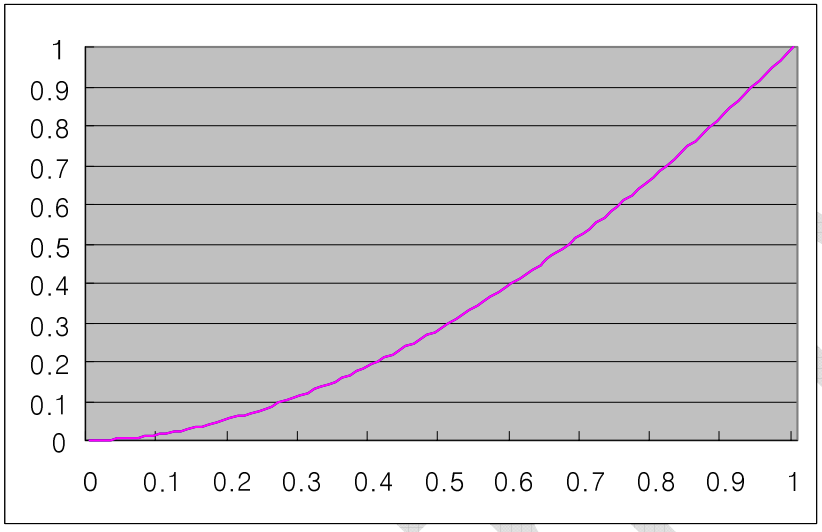

Figure80. Gamma $y = x^{2.2}$

4.2.2.2. Gamma curve 2 (GC1)

Gamma Curve 2 (GC1), applies the function. $y = x^{1.8}$

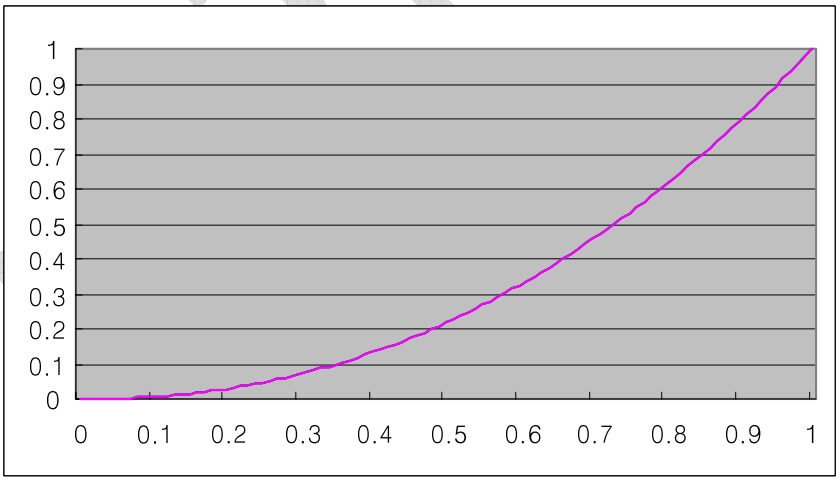

Figure81. Gamma $y = x^{1.8}$

4.2.2.3. Gamma curve 3(GC2)

Gamma Curve 3(GC2), applies the function. $y = x^{2.5}$

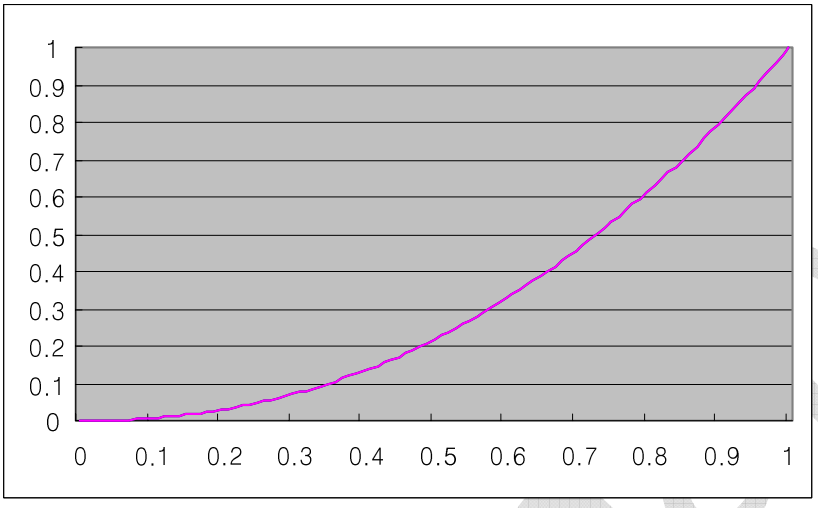

Figure82. Gamma $y = x^{2.5}$

4.2.2.4. Gamma curve 4 (GC3)

Gamma Curve 4 (GC3) is linear, i. e. $y = x^{1}$

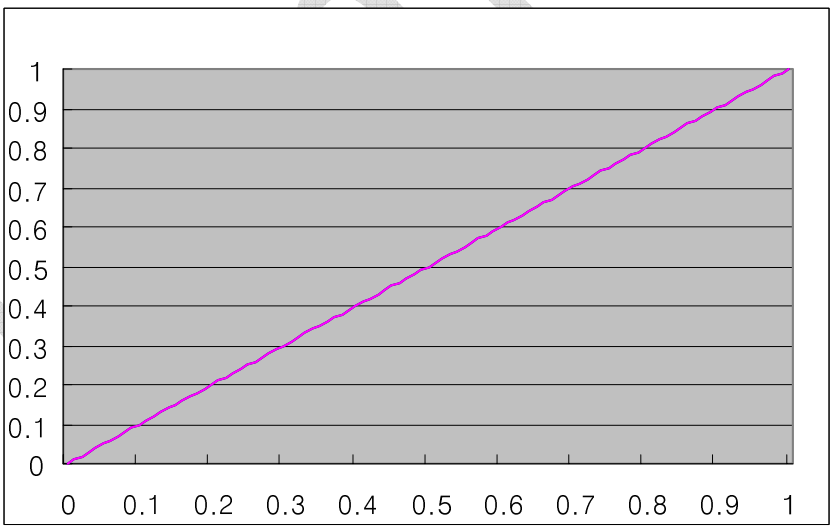

Figure83. Gamma $y = x^{1}$

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4.2.3. STRUCTURE OF GRAYSCALE AMPLIFIER

S6D04K1 provides the gamma adjustment function to display 262,114 colors simultaneously for each R/G/B color. The gamma adjustment executed by the high/ mid/ low level adjustment registers determines 11 grayscale reference levels. Furthermore, since the high-level adjustment register, mid-level adjustment register and the low-level adjustment register have the positive polarities and negative polarities, you can adjust them to match LCD panel and a gamma for each R/G/B color, respectively.

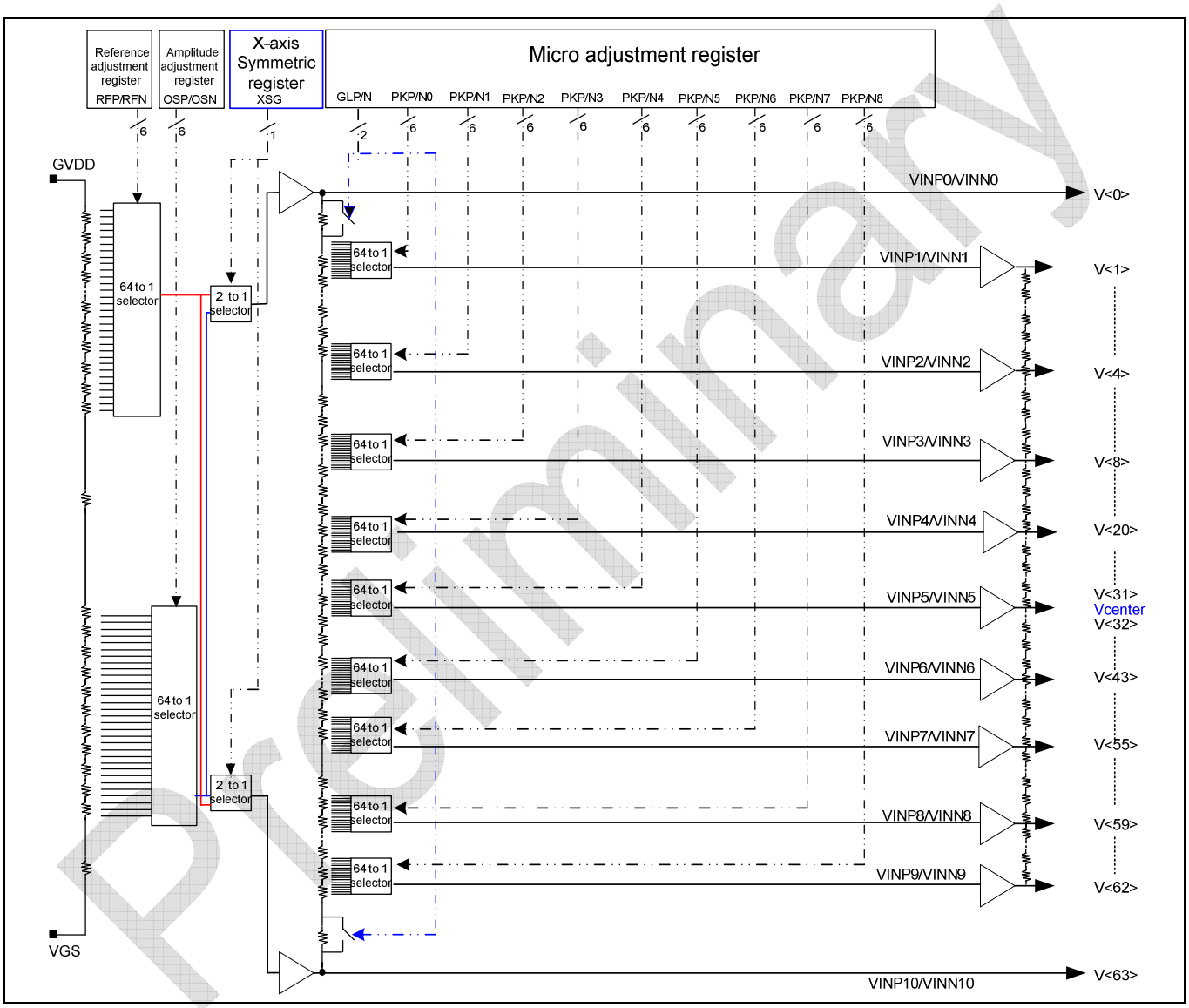

Figure84. Structure of Grayscale Amplifier

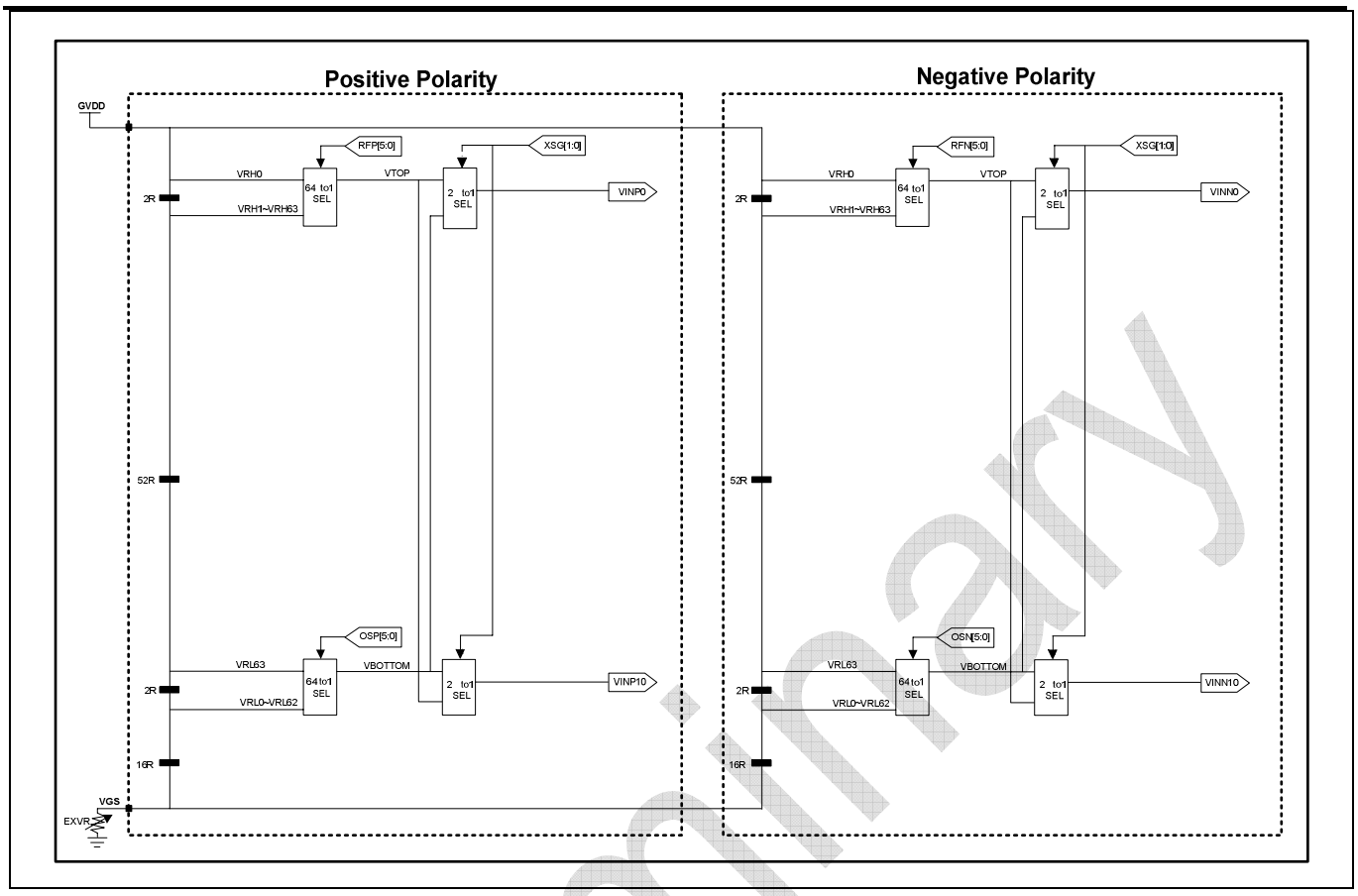

Figure85. Structure of Resistor Ladder Network I

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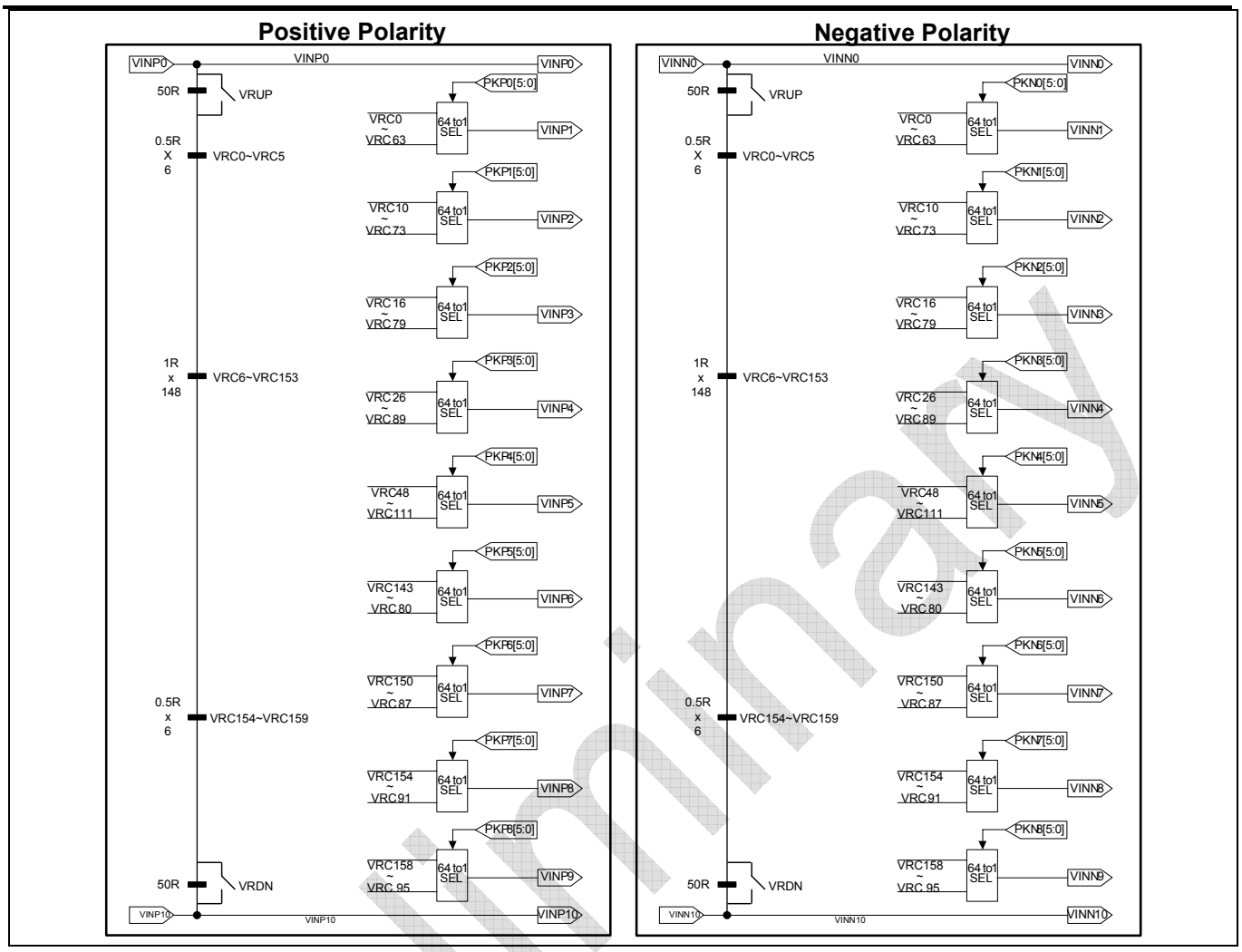

Figure86. Structure of Resistor Ladder Network II

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4.2.4. GAMMA ADJUSTMENT REGISTER

This block has registers to set up the grayscale voltage according to the gamma specification of the LCD panel. These registers can independently set up the positive/negative polarities. There are 4 types of register groups to adjust the amplitude on the grayscale characteristics of the grayscale voltage, and R/G/B gamma adjustment registers are separated. The following figures indicate the operation of each adjustment registers.

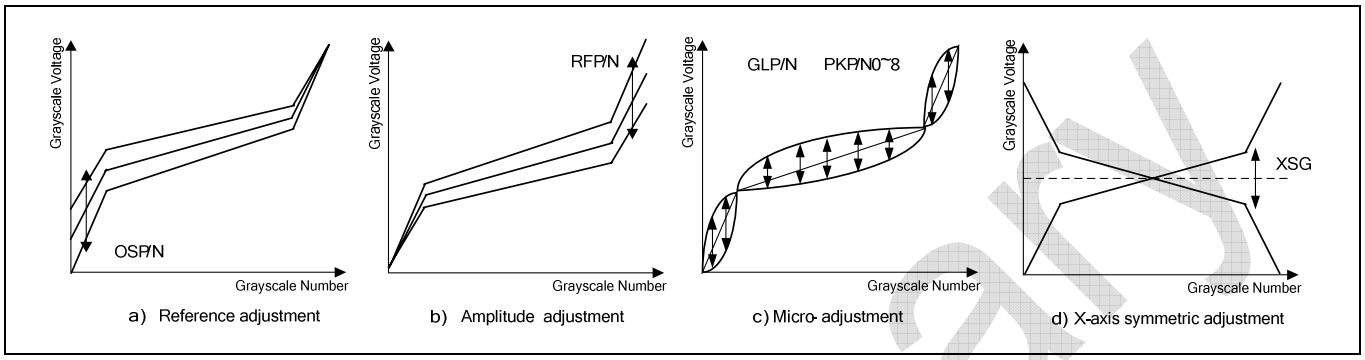

Figure87. The Operation of Adjusting Register

4.2.4.1. Reference adjustment register

The Reference adjustment register is used to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the VINP10/VINN10 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4.2.4.2. Amplitude adjustment register

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VINN0 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4.2.4.3. Micro-adjustment register

The Micro adjustment register is employed to make subtle adjustment to the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

4.2.4.4. X-axis symmetric adjustment register

The X-axis symmetric adjustment register is to adjust X-axis symmetric of the grayscale voltage. This register can be detailedly explained with NGF register selection. 1st case; when XSG=0 and NGF=1, Vp<N>+Vn<N>=Vp<0>+Vn<0> and gamma symmetric axis is (Vp<0>+Vn<0>)/2. 2nd case; when XSG=0 and NGF=0, negative gamma voltage can be changed using negative gamma register value and symmetric axis will be changed according to negative gamma voltage. 3rd case; when XSG=1 and NGF=1, Vp<N>=Vn<|63-N|>. 4th case; when XSG=1 and NGF=0, Vp<N>+Vn<N> ≠ Vp<0>+Vn<0> but can have similar value in some degree

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using both positive and negative gamma registers.

Table 45. Gamma Adjusting Register

Register	Positive Polarity	Negative Polarity	Set-up Contents
Reference adjustment Amplitude adjustment	OSP[5:0]	OSN[5:0]	The voltage of VBOTTOM is selected by the 64 to 1 selector
	RFP[5:0]	RFN[5:0]	The voltage of VTOP is selected by the 64 to 1 selector
X-axis symmetric adjustment	XSG		The voltage of VINP10/VINN10 is selected by the 2 to 1 selector
			The voltage of VINP0/VINN0 is selected by the 2 to 1 selector
Micro adjustment	GLP[1:0]	GLN[1:0]	The voltage of grayscale number from 1 to 62 is adjusted by the variable resistor
	PKP0[5:0]	PKN0[5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
	PKP1[5:0]	PKN1[5:0]	The voltage of grayscale number 4 is selected by the 64 to 1 selector
	PKP2[5:0]	PKN2[5:0]	The voltage of grayscale number 8 is selected by the 64 to 1 selector
	PKP3[5:0]	PKN3[5:0]	The voltage of grayscale number 20 is selected by the 64 to 1 selector
	PKP4[5:0]	PKN4[5:0]	The voltage of grayscale number VC (middle voltage between v<31> and V<32>) is selected by the 64 to 1 selector
	PKP5[5:0]	PKN5[5:0]	The voltage of grayscale number 43 is selected by the 64 to 1 selector
	PKP6[5:0]	PKN6[5:0]	The voltage of grayscale number 55 is selected by the 64 to 1 selector
	PKP7[5:0]	PKN7[5:0]	The voltage of grayscale number 59 is selected by the 64 to 1 selector
	PKP8[5:0]	PKN8[5:0]	The voltage of grayscale number 62 is selected by the 64 to 1 selector

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4.2.5. RESISTOR LADDER NETWORK / SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are three ladder resistors including the 64 to 1 selector selecting voltage generated by the ladder resistance voltage. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

4.2.5.1. Resistor ladder network 1 / selector

There are 2 adjustments that are for the reference / amplitude adjustment (RFP(N)/ OSP(N)) and micro adjustment (PKP(N)). The voltage level is set by the reference / amplitude adjustment registers and micro adjustments as below.

Table 46. Amplitude Adjustment

Register Value RFP(N) [5:0]	Selected Voltage VTOP	Formula of VTOP
000000	VRH0	(320R/320R) * (GVDD-VGS) + VGS
000001	VRH1	(318R/320R) * (GVDD-VGS) + VGS
000010	VRH2	(316R/320R) * (GVDD-VGS) + VGS
000011	VRH3	(314R/320R) * (GVDD-VGS) + VGS
000100	VRH4	(312R/320R) * (GVDD-VGS) + VGS
000101	VRH5	(310R/320R) * (GVDD-VGS) + VGS
000110	VRH6	(308R/320R) * (GVDD-VGS) + VGS
000111	VRH7	(306R/320R) * (GVDD-VGS) + VGS
001000	VRH8	(304R/320R) * (GVDD-VGS) + VGS
001001	VRH9	(302R/320R) * (GVDD-VGS) + VGS
001010	VRH10	(300R/320R) * (GVDD-VGS) + VGS
001011	VRH11	(298R/320R) * (GVDD-VGS) + VGS
001100	VRH12	(296R/320R) * (GVDD-VGS) + VGS
001101	VRH13	(294R/320R) * (GVDD-VGS) + VGS
001110	VRH14	(292R/320R) * (GVDD-VGS) + VGS
001111	VRH15	(290R/320R) * (GVDD-VGS) + VGS
010000	VRH16	(288R/320R) * (GVDD-VGS) + VGS
010001	VRH17	(286R/320R) * (GVDD-VGS) + VGS
010010	VRH18	(284R/320R) * (GVDD-VGS) + VGS
010011	VRH19	(282R/320R) * (GVDD-VGS) + VGS
010100	VRH20	(280R/320R) * (GVDD-VGS) + VGS
010101	VRH21	(278R/320R) * (GVDD-VGS) + VGS
010110	VRH22	(276R/320R) * (GVDD-VGS) + VGS

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Register Value RFP(N) [5:0]	Selected Voltage VTOP	Formula of VTOP
010111	VRH23	(274R/320R) * (GVDD-VGS) + VGS
011000	VRH24	(272R/320R) * (GVDD-VGS) + VGS
011001	VRH25	(270R/320R) * (GVDD-VGS) + VGS
011010	VRH26	(268R/320R) * (GVDD-VGS) + VGS
011011	VRH27	(266R/320R) * (GVDD-VGS) + VGS
011100	VRH28	(264R/320R) * (GVDD-VGS) + VGS
011101	VRH29	(262R/320R) * (GVDD-VGS) + VGS
011110	VRH30	(260R/320R) * (GVDD-VGS) + VGS
011111	VRH31	(258R/320R) * (GVDD-VGS) + VGS
100000	VRH32	(256R/320R) * (GVDD-VGS) + VGS
100001	VRH33	(254R/320R) * (GVDD-VGS) + VGS
100010	VRH34	(252R/320R) * (GVDD-VGS) + VGS
100011	VRH35	(250R/320R) * (GVDD-VGS) + VGS
100100	VRH36	(248R/320R) * (GVDD-VGS) + VGS
100101	VRH37	(246R/320R) * (GVDD-VGS) + VGS
100110	VRH38	(244R/320R) * (GVDD-VGS) + VGS
100111	VRH39	(242R/320R) * (GVDD-VGS) + VGS
101000	VRH40	(240R/320R) * (GVDD-VGS) + VGS
101001	VRH41	(238R/320R) * (GVDD-VGS) + VGS
101010	VRH42	(236R/320R) * (GVDD-VGS) + VGS
101011	VRH43	(234R/320R) * (GVDD-VGS) + VGS
101100	VRH44	(232R/320R) * (GVDD-VGS) + VGS
101101	VRH45	(230R/320R) * (GVDD-VGS) + VGS
101110	VRH46	(228R/320R) * (GVDD-VGS) + VGS
101111	VRH47	(226R/320R) * (GVDD-VGS) + VGS
110000	VRH48	(224R/320R) * (GVDD-VGS) + VGS
110001	VRH49	(222R/320R) * (GVDD-VGS) + VGS
110010	VRH50	(220R/320R) * (GVDD-VGS) + VGS
110011	VRH51	(218R/320R) * (GVDD-VGS) + VGS
110100	VRH52	(216R/320R) * (GVDD-VGS) + VGS
110101	VRH53	(214R/320R) * (GVDD-VGS) + VGS
110110	VRH54	(212R/320R) * (GVDD-VGS) + VGS
110111	VRH55	(210R/320R) * (GVDD-VGS) + VGS
111000	VRH56	(208R/320R) * (GVDD-VGS) + VGS

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Register Value RFP(N) [5:0]	Selected Voltage VTOP	Formula of VTOP
111001	VRH57	(206R/320R) * (GVDD-VGS) + VGS
111010	VRH58	(204R/320R) * (GVDD-VGS) + VGS
111011	VRH59	(202R/320R) * (GVDD-VGS) + VGS
111100	VRH60	(200R/320R) * (GVDD-VGS) + VGS
111101	VRH61	(198R/320R) * (GVDD-VGS) + VGS
111110	VRH62	(196R/320R) * (GVDD-VGS) + VGS
111111	VRH63	(194R/320R) * (GVDD-VGS) + VGS

Table 47. Reference Adjustment

Register Value OSP(N) [5:0]	Selected Voltage VBOTTOM	Formula of VBOTTOM
000000	VRL0	(16R/320R) * (GVDD-VGS) + VGS
000001	VRL1	(18R/320R) * (GVDD-VGS) + VGS
000010	VRL2	(20R/320R) * (GVDD-VGS) + VGS
000011	VRL3	(22R/320R) * (GVDD-VGS) + VGS
000100	VRL4	(24R/320R) * (GVDD-VGS) + VGS
000101	VRL5	(26R/320R) * (GVDD-VGS) + VGS
000110	VRL6	(28R/320R) * (GVDD-VGS) + VGS
000111	VRL7	(30R/320R) * (GVDD-VGS) + VGS
001000	VRL8	(32R/320R) * (GVDD-VGS) + VGS
001001	VRL9	(34R/320R) * (GVDD-VGS) + VGS
001010	VRL10	(36R/320R) * (GVDD-VGS) + VGS
001011	VRL11	(38R/320R) * (GVDD-VGS) + VGS
001100	VRL12	(40R/320R) * (GVDD-VGS) + VGS
001101	VRL13	(42R/320R) * (GVDD-VGS) + VGS
001110	VRL14	(44R/320R) * (GVDD-VGS) + VGS
001111	VRL15	(46R/320R) * (GVDD-VGS) + VGS
010000	VRL16	(48R/320R) * (GVDD-VGS) + VGS
010001	VRL17	(50R/320R) * (GVDD-VGS) + VGS
010010	VRL18	(52R/320R) * (GVDD-VGS) + VGS
010011	VRL19	(54R/320R) * (GVDD-VGS) + VGS
010100	VRL20	(56R/320R) * (GVDD-VGS) + VGS
010101	VRL21	(58R/320R) * (GVDD-VGS) + VGS
010110	VRL22	(60R/320R) * (GVDD-VGS) + VGS
010111	VRL23	(62R/320R) * (GVDD-VGS) + VGS

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Register Value OSP(N) [5:0]	Selected Voltage VBOTTOM	Formula of VBOTTOM
011000	VRL24	(64R/320R) * (GVDD-VGS) + VGS
011001	VRL25	(66R/320R) * (GVDD-VGS) + VGS
011010	VRL26	(68R/320R) * (GVDD-VGS) + VGS
011011	VRL27	(70R/320R) * (GVDD-VGS) + VGS
011100	VRL28	(72R/320R) * (GVDD-VGS) + VGS
011101	VRL29	(74R/320R) * (GVDD-VGS) + VGS
011110	VRL30	(76R/320R) * (GVDD-VGS) + VGS
011111	VRL31	(78R/320R) * (GVDD-VGS) + VGS
100000	VRL32	(80R/320R) * (GVDD-VGS) + VGS
100001	VRL33	(82R/320R) * (GVDD-VGS) + VGS
100010	VRL34	(84R/320R) * (GVDD-VGS) + VGS
100011	VRL35	(86R/320R) * (GVDD-VGS) + VGS
100100	VRL36	(88R/320R) * (GVDD-VGS) + VGS
100101	VRL37	(90R/320R) * (GVDD-VGS) + VGS
100110	VRL38	(92R/320R) * (GVDD-VGS) + VGS
100111	VRL39	(94R/320R) * (GVDD-VGS) + VGS
101000	VRL40	(96R/320R) * (GVDD-VGS) + VGS
101001	VRL41	(98R/320R) * (GVDD-VGS) + VGS
101010	VRL42	(100R/320R) * (GVDD-VGS) + VGS
101011	VRL43	(102R/320R) * (GVDD-VGS) + VGS
101100	VRL44	(104R/320R) * (GVDD-VGS) + VGS
101101	VRL45	(106R/320R) * (GVDD-VGS) + VGS
101110	VRL46	(108R/320R) * (GVDD-VGS) + VGS
101111	VRL47	(110R/320R) * (GVDD-VGS) + VGS
110000	VRL48	(112R/320R) * (GVDD-VGS) + VGS
110001	VRL49	(114R/320R) * (GVDD-VGS) + VGS
110010	VRL50	(116R/320R) * (GVDD-VGS) + VGS
110011	VRL51	(118R/320R) * (GVDD-VGS) + VGS
110100	VRL52	(120R/320R) * (GVDD-VGS) + VGS
110101	VRL53	(122R/320R) * (GVDD-VGS) + VGS
110110	VRL54	(124R/320R) * (GVDD-VGS) + VGS
110111	VRL55	(126R/320R) * (GVDD-VGS) + VGS
111000	VRL56	(128R/320R) * (GVDD-VGS) + VGS
111001	VRL57	(130R/320R) * (GVDD-VGS) + VGS

Preliminary

Register Value OSP(N) [5:0]	Selected Voltage VBOTTOM	Formula of VBOTTOM
111010	VRL58	(132R/320R) * (GVDD-VGS) + VGS
111011	VRL59	(134R/320R) * (GVDD-VGS) + VGS
111100	VRL60	(136R/320R) * (GVDD-VGS) + VGS
111101	VRL61	(138R/320R) * (GVDD-VGS) + VGS
111110	VRL62	(140R/320R) * (GVDD-VGS) + VGS
111111	VRL63	(142R/320R) * (GVDD-VGS) + VGS

4.2.5.2. Resistor ladder network 2 / selector

In the 64-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the nine types of the reference voltage, VIN1 to VIN9.

Following figure explains the relationship between the micro-adjustment register and the selected voltage

Table 48. Relationship Between Micro-Adjustment Register and Selected Voltage

Register Value	Selected Voltage								
PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9
000000	VRC0	VRC10	VRC16	VRC26	VRC48	VRC143	VRC150	VRC154	VRC158
000001	VRC1	VRC11	VRC17	VRC27	VRC49	VRC142	VRC149	VRC153	VRC157
000010	VRC2	VRC12	VRC18	VRC28	VRC50	VRC141	VRC148	VRC152	VRC156
000011	VRC3	VRC13	VRC19	VRC29	VRC51	VRC140	VRC147	VRC151	VRC155
000100	VRC4	VRC14	VRC20	VRC30	VRC52	VRC139	VRC146	VRC150	VRC154
000101	VRC5	VRC15	VRC21	VRC31	VRC53	VRC138	VRC145	VRC149	VRC153
000110	VRC6	VRC16	VRC22	VRC32	VRC54	VRC137	VRC144	VRC148	VRC152
000111	VRC7	VRC17	VRC23	VRC33	VRC55	VRC136	VRC143	VRC147	VRC151
001000	VRC8	VRC18	VRC24	VRC34	VRC56	VRC135	VRC142	VRC146	VRC150
001001	VRC9	VRC19	VRC25	VRC35	VRC57	VRC134	VRC141	VRC145	VRC149
001010	VRC10	VRC20	VRC26	VRC36	VRC58	VRC133	VRC140	VRC144	VRC148
001011	VRC11	VRC21	VRC27	VRC37	VRC59	VRC132	VRC139	VRC143	VRC147
001100	VRC12	VRC22	VRC28	VRC38	VRC60	VRC131	VRC138	VRC142	VRC146
001101	VRC13	VRC23	VRC29	VRC39	VRC61	VRC130	VRC137	VRC141	VRC145
001110	VRC14	VRC24	VRC30	VRC40	VRC62	VRC129	VRC136	VRC140	VRC144
001111	VRC15	VRC25	VRC31	VRC41	VRC63	VRC128	VRC135	VRC139	VRC143
010000	VRC16	VRC26	VRC32	VRC42	VRC64	VRC127	VRC134	VRC138	VRC142
010001	VRC17	VRC27	VRC33	VRC43	VRC65	VRC126	VRC133	VRC137	VRC141

Preliminary

Register Value	Selected Voltage								
PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9
010010	VRC18	VRC28	VRC34	VRC44	VRC66	VRC125	VRC132	VRC136	VRC140
010011	VRC19	VRC29	VRC35	VRC45	VRC67	VRC124	VRC131	VRC135	VRC139
010100	VRC20	VRC30	VRC36	VRC46	VRC68	VRC123	VRC130	VRC134	VRC138
010101	VRC21	VRC31	VRC37	VRC47	VRC69	VRC122	VRC129	VRC133	VRC137
010110	VRC22	VRC32	VRC38	VRC48	VRC70	VRC121	VRC128	VRC132	VRC136
010111	VRC23	VRC33	VRC39	VRC49	VRC71	VRC120	VRC127	VRC131	VRC135
011000	VRC24	VRC34	VRC40	VRC50	VRC72	VRC119	VRC126	VRC130	VRC134
011001	VRC25	VRC35	VRC41	VRC51	VRC73	VRC118	VRC125	VRC129	VRC133
011010	VRC26	VRC36	VRC42	VRC52	VRC74	VRC117	VRC124	VRC128	VRC132
011011	VRC27	VRC37	VRC43	VRC53	VRC75	VRC116	VRC123	VRC127	VRC131
011100	VRC28	VRC38	VRC44	VRC54	VRC76	VRC115	VRC122	VRC126	VRC130
011101	VRC29	VRC39	VRC45	VRC55	VRC77	VRC114	VRC121	VRC125	VRC129
011110	VRC30	VRC40	VRC46	VRC56	VRC78	VRC113	VRC120	VRC124	VRC128
011111	VRC31	VRC41	VRC47	VRC57	VRC79	VRC112	VRC119	VRC123	VRC127
100000	VRC32	VRC42	VRC48	VRC58	VRC80	VRC111	VRC118	VRC122	VRC126
100001	VRC33	VRC43	VRC49	VRC59	VRC81	VRC110	VRC117	VRC121	VRC125
100010	VRC34	VRC44	VRC50	VRC60	VRC82	VRC109	VRC116	VRC120	VRC124
100011	VRC35	VRC45	VRC51	VRC61	VRC83	VRC108	VRC115	VRC119	VRC123
100100	VRC36	VRC46	VRC52	VRC62	VRC84	VRC107	VRC114	VRC118	VRC122
100101	VRC37	VRC47	VRC53	VRC63	VRC85	VRC106	VRC113	VRC117	VRC121
100110	VRC38	VRC48	VRC54	VRC64	VRC86	VRC105	VRC112	VRC116	VRC120
100111	VRC39	VRC49	VRC55	VRC65	VRC87	VRC104	VRC111	VRC115	VRC119
101000	VRC40	VRC50	VRC56	VRC66	VRC88	VRC103	VRC110	VRC114	VRC118
101001	VRC41	VRC51	VRC57	VRC67	VRC89	VRC102	VRC109	VRC113	VRC117
101010	VRC42	VRC52	VRC58	VRC68	VRC90	VRC101	VRC108	VRC112	VRC116
101011	VRC43	VRC53	VRC59	VRC69	VRC91	VRC100	VRC107	VRC111	VRC115
101100	VRC44	VRC54	VRC60	VRC70	VRC92	VRC99	VRC106	VRC110	VRC114
101101	VRC45	VRC55	VRC61	VRC71	VRC93	VRC98	VRC105	VRC109	VRC113
101110	VRC46	VRC56	VRC62	VRC72	VRC94	VRC97	VRC104	VRC108	VRC112
101111	VRC47	VRC57	VRC63	VRC73	VRC95	VRC96	VRC103	VRC107	VRC111
110000	VRC48	VRC58	VRC64	VRC74	VRC96	VRC95	VRC102	VRC106	VRC110

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Register Value	Selected Voltage								
PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9
110001	VRC49	VRC59	VRC65	VRC75	VRC97	VRC94	VRC101	VRC105	VRC109
110010	VRC50	VRC60	VRC66	VRC76	VRC98	VRC93	VRC100	VRC104	VRC108
110011	VRC51	VRC61	VRC67	VRC77	VRC99	VRC92	VRC99	VRC103	VRC107
110100	VRC52	VRC62	VRC68	VRC78	VRC100	VRC91	VRC98	VRC102	VRC106
110101	VRC53	VRC63	VRC69	VRC79	VRC101	VRC90	VRC97	VRC101	VRC105
110110	VRC54	VRC64	VRC70	VRC80	VRC102	VRC89	VRC96	VRC100	VRC104
110111	VRC55	VRC65	VRC71	VRC81	VRC103	VRC88	VRC95	VRC99	VRC103
111000	VRC56	VRC66	VRC72	VRC82	VRC104	VRC87	VRC94	VRC98	VRC102
111001	VRC57	VRC67	VRC73	VRC83	VRC105	VRC86	VRC93	VRC97	VRC101
111010	VRC58	VRC68	VRC74	VRC84	VRC106	VRC85	VRC92	VRC96	VRC100

Table 49. Relationship Between Micro-Adjustment Register and Selected Voltage(Continued)

Register Value	Selected Voltage								
PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9
111011	VRC59	VRC69	VRC75	VRC85	VRC107	VRC84	VRC91	VRC95	VRC99
111100	VRC60	VRC70	VRC76	VRC86	VRC108	VRC83	VRC90	VRC94	VRC98
111101	VRC61	VRC71	VRC77	VRC87	VRC109	VRC82	VRC89	VRC93	VRC97
111110	VRC62	VRC72	VRC78	VRC88	VRC110	VRC81	VRC88	VRC92	VRC96
111111	VRC63	VRC73	VRC79	VRC89	VRC111	VRC80	VRC87	VRC91	VRC95

The grayscale levels are determined by the following formulas listed in the following equations.

Negative gamma voltages are calculated with the same equation of positive gamma voltages, but the gray scale is symmetric, which means negative V<0> is equal to positive V<63>. Rt and Ra in the below equations are determined by GL[1:0] Registers as follows.

GLP/N[1:0]=00, Rt = 154R, Ra=R

GLP/N [1:0]=01, Rt = 204R, Ra=R+50R

GLP/N [1:0]=10, Rt = 204R, Ra=R

GLP/N [1:0]=11, Rt = 254R, Ra=R+50R

Preliminary

4.2.6. GRAYSCALE LEVELS

Table 50. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC0	(153.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000000”	VNP1
VRC1	(153Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000001”	
VRC2	(152.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000010”	
VRC3	(152Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000011”	
VRC4	(151.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000100”	
VRC5	(151Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000101”	
VRC6	(150Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000110”	
VRC7	(149Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000111”	
VRC8	(148Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001000”	
VRC9	(147Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001001”	
VRC10	(146Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001010”	
VRC11	(145Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001011”	
VRC12	(144Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001100”	
VRC13	(143Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001101”	
VRC14	(142Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001110”	
VRC15	(141Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001111”	
VRC16	(140Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010000”	
VRC17	(139Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010001”	
VRC18	(138Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010010”	
VRC19	(137Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010011”	
VRC20	(136Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010100”	
VRC21	(135Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010101”	
VRC22	(134Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010110”	
VRC23	(133Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010111”	
VRC24	(132Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011000”	
VRC25	(131Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011001”	
VRC26	(130Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011010”	
VRC27	(129Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011011”	
VRC28	(128Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011100”	
VRC29	(127Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011101”	
VRC30	(126Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011110”	

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Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC31	(125Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011111”	
VRC32	(124Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100000”	
VRC33	(123Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100001”	
VRC34	(122Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100010”	
VRC35	(121Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100011”	

Table 51. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC36	(120Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100100”	VINP1
VRC37	(119Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100101”	
VRC38	(118Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100110”	
VRC39	(117Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100111”	
VRC40	(116Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101000”	
VRC41	(115Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101001”	
VRC42	(114Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101010”	
VRC43	(113Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101011”	
VRC44	(112Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101100”	
VRC45	(111Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101101”	
VRC46	(110Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101110”	
VRC47	(109Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101111”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110000”	
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110001”	
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110010”	
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110011”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110100”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110101”	
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110110”	
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110111”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111000”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111001”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111010”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111011”	

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Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111100”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111101”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111110”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111111”	
VRC10	(146Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000000”	VINP2
VRC11	(145Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000001”	
VRC12	(144Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000010”	
VRC13	(143Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000011”	
VRC14	(142Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000100”	
VRC15	(141Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000101”	
VRC16	(140Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000110”	
VRC17	(139Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000111”	

Table 52. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC18	(138Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001000”	VINP2
VRC19	(137Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001001”	
VRC20	(136Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001010”	
VRC21	(135Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001011”	
VRC22	(134Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001100”	
VRC23	(133Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001101”	
VRC24	(132Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001110”	
VRC25	(131Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001111”	
VRC26	(130Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010000”	
VRC27	(129Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010001”	
VRC28	(128Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010010”	
VRC29	(127Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010011”	
VRC30	(126Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010100”	
VRC31	(125Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010101”	
VRC32	(124Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010110”	
VRC33	(123Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010111”	
VRC34	(122Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011000”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC35	(121Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011001”	
VRC36	(120Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011010”	
VRC37	(119Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011011”	
VRC38	(118Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011100”	
VRC39	(117Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011101”	
VRC40	(116Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011110”	
VRC41	(115Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011111”	
VRC42	(114Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100000”	
VRC43	(113Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100001”	
VRC44	(112Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100010”	
VRC45	(111Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100011”	
VRC46	(110Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100100”	
VRC47	(109Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100101”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100110”	
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100111”	
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101000”	
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101001”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101010”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101011”	

Table 53. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101100”	VINP2
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101101”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101110”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101111”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110000”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110001”	
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110010”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110011”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110100”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110101”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC64	(92Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110110”	
VRC65	(91Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110111”	
VRC66	(90Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111000”	
VRC67	(89Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111001”	
VRC68	(88Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111010”	
VRC69	(87Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111011”	
VRC70	(86Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111100”	
VRC71	(85Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111101”	
VRC72	(84Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111110”	
VRC73	(83Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111111”	
VRC16	(140Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000000”	VINP3
VRC17	(139Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000001”	
VRC18	(138Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000010”	
VRC19	(137Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000011”	
VRC20	(136Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000100”	
VRC21	(135Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000101”	
VRC22	(134Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000110”	
VRC23	(133Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000111”	
VRC24	(132Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001000”	
VRC25	(131Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001001”	
VRC26	(130Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001010”	
VRC27	(129Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001011”	
VRC28	(128Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001100”	
VRC29	(127Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001101”	
VRC30	(126Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001110”	
VRC31	(125Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001111”	

Preliminary

Table 54. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC32	(124Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010000”	VINP3
VRC33	(123Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010001”	
VRC34	(122Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010010”	
VRC35	(121Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010011”	
VRC36	(120Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010100”	
VRC37	(119Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010101”	
VRC38	(118Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010110”	
VRC39	(117Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010111”	
VRC40	(116Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011000”	
VRC41	(115Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011001”	
VRC42	(114Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011010”	
VRC43	(113Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011011”	
VRC44	(112Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011100”	
VRC45	(111Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011101”	
VRC46	(110Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011110”	
VRC47	(109Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011111”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100000”	
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100001”	
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100010”	
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100011”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100100”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100101”	
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100110”	
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100111”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101000”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101001”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101010”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101011”	
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101100”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101101”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101110”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101111”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC64	(92Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110000”	
VRC65	(91Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110001”	
VRC66	(90Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110010”	
VRC67	(89Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110011”	

Table 55. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC68	(88Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110100”	VINP3
VRC69	(87Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110101”	
VRC70	(86Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110110”	
VRC71	(85Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110111”	
VRC72	(84Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111000”	
VRC73	(83Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111001”	
VRC74	(82Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111010”	
VRC75	(81Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111011”	
VRC76	(80Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111100”	
VRC77	(79Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111101”	
VRC78	(78Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111110”	
VRC79	(77Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111111”	
VRC26	(130Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000000”	VINP4
VRC27	(129Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000001”	
VRC28	(128Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000010”	
VRC29	(127Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000011”	
VRC30	(126Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000100”	
VRC31	(125Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000101”	
VRC32	(124Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000110”	
VRC33	(123Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000111”	
VRC34	(122Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001000”	
VRC35	(121Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001001”	
VRC36	(120Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001010”	
VRC37	(119Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001011”	
VRC38	(118Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001100”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC39	(117Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001101”	
VRC40	(116Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001110”	
VRC41	(115Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001111”	
VRC42	(114Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010000”	
VRC43	(113Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010001”	
VRC44	(112Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010010”	
VRC45	(111Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010011”	
VRC46	(110Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010100”	
VRC47	(109Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010101”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010110”	
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010111”	

Table 56. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011000”	VINP4
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011001”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011010”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011011”	
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011100”	
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011101”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011110”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011111”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100000”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100001”	
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100010”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100011”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100100”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100101”	
VRC64	(92Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100110”	
VRC65	(91Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100111”	
VRC66	(90Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101000”	
VRC67	(89Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101001”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC68	(88Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101010”	
VRC69	(87Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101011”	
VRC70	(86Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101100”	
VRC71	(85Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101101”	
VRC72	(84Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101110”	
VRC73	(83Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101111”	
VRC74	(82Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110000”	
VRC75	(81Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110001”	
VRC76	(80Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110010”	
VRC77	(79Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110011”	
VRC78	(78Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110100”	
VRC79	(77Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110101”	
VRC80	(76Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110110”	
VRC81	(75Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110111”	
VRC82	(74Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111000”	
VRC83	(73Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111001”	
VRC84	(72Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111010”	
VRC85	(71Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111011”	

Table 57. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference voltage
VRC86	(70Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111100”	
VRC87	(69Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111101”	VINP4
VRC88	(68Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111110”	
VRC89	(67Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111111”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000000”	VINP5
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000001”	
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000010”	
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000011”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000100”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000101”	
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000110”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference voltage
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000111”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001000”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001001”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001010”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001011”	
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001100”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001101”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001110”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001111”	
VRC64	(92Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010000”	
VRC65	(91Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010001”	
VRC66	(90Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010010”	
VRC67	(89Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010011”	
VRC68	(88Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010100”	
VRC69	(87Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010101”	
VRC70	(86Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010110”	
VRC71	(85Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010111”	
VRC72	(84Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011000”	
VRC73	(83Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011001”	
VRC74	(82Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011010”	
VRC75	(81Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011011”	
VRC76	(80Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011100”	
VRC77	(79Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011101”	
VRC78	(78Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011110”	
VRC79	(77Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011111”	

Preliminary

Table 58. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC80	(76Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100000”	VINP5
VRC81	(75Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100001”	
VRC82	(74Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100010”	
VRC83	(73Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100011”	
VRC84	(72Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100100”	
VRC85	(71Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100101”	
VRC86	(70Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100110”	
VRC87	(69Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100111”	
VRC88	(68Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101000”	
VRC89	(67Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101001”	
VRC90	(66Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101010”	
VRC91	(65Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101011”	
VRC92	(64Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101100”	
VRC93	(63Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101101”	
VRC94	(62Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101110”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101111”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110000”	
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110001”	
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110010”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110011”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110100”	
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110101”	
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110110”	
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110111”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111000”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111001”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111010”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111011”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111100”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111101”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111110”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111111”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC143	(13Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000000”	VINP6
VRC142	(14Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000001”	
VRC141	(15Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000010”	
VRC140	(16Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000011”	

Table 59. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC139	(17Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000100”	VINP6
VRC138	(18Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000101”	
VRC137	(19Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000110”	
VRC136	(20Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000111”	
VRC135	(21Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001000”	
VRC134	(22Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001001”	
VRC133	(23Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001010”	
VRC132	(24Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001011”	
VRC131	(25Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001100”	
VRC130	(26Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001101”	
VRC129	(27Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001110”	
VRC128	(28Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001111”	
VRC127	(29Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010000”	
VRC126	(30Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010001”	
VRC125	(31Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010010”	
VRC124	(32Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010011”	
VRC123	(33Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010100”	
VRC122	(34Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010101”	
VRC121	(35Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010110”	
VRC120	(36Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010111”	
VRC119	(37Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011000”	
VRC118	(38Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011001”	
VRC117	(39Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011010”	
VRC116	(40Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011011”	
VRC115	(41Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011100”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC114	(42Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011101”	
VRC113	(43Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011110”	
VRC112	(44Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011111”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100000”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100001”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100010”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100011”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100100”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100101”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100110”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100111”	

Table 60. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101000”	VINP6
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101001”	
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101010”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101011”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101100”	
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101101”	
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101110”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101111”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110000”	
VRC94	(62Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110001”	
VRC93	(63Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110010”	
VRC92	(64Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110011”	
VRC91	(65Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110100”	
VRC90	(66Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110101”	
VRC89	(67Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110110”	
VRC88	(68Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110111”	
VRC87	(69Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111000”	
VRC86	(70Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111001”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC85	(71Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111010”	
VRC84	(72Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111011”	
VRC83	(73Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111100”	
VRC82	(74Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111101”	
VRC81	(75Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111110”	
VRC80	(76Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111111”	
VRC150	(6Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000000”	
VRC149	(7Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000001”	
VRC148	(8Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000010”	
VRC147	(9Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000011”	
VRC146	(10Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000100”	
VRC145	(11Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000101”	VINP7
VRC144	(12Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000110”	
VRC143	(13Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000111”	
VRC142	(14Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001000”	
VRC141	(15Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001001”	
VRC140	(16Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001010”	
VRC139	(17Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001011”	

Table 61. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC138	(18Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001100”	VINP7
VRC137	(19Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001101”	
VRC136	(20Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001110”	
VRC135	(21Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001111”	
VRC134	(22Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010000”	
VRC133	(23Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010001”	
VRC132	(24Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010010”	
VRC131	(25Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010011”	
VRC130	(26Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010100”	
VRC129	(27Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010101”	
VRC128	(28Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010110”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC127	(29Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010111”	
VRC126	(30Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011000”	
VRC125	(31Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011001”	
VRC124	(32Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011010”	
VRC123	(33Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011011”	
VRC122	(34Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011100”	
VRC121	(35Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011101”	
VRC120	(36Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011110”	
VRC119	(37Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011111”	
VRC118	(38Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100000”	
VRC117	(39Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100001”	
VRC116	(40Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100010”	
VRC115	(41Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100011”	
VRC114	(42Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100100”	
VRC113	(43Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100101”	
VRC112	(44Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100110”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100111”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101000”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101001”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101010”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101011”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101100”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101101”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101110”	
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101111”	

Preliminary

Table 62. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110000”	VINP7
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110001”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110010”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110011”	
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110100”	
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110101”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110110”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110111”	
VRC94	(62Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111000”	
VRC93	(63Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111001”	
VRC92	(64Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111010”	
VRC91	(65Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111011”	
VRC90	(66Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111100”	
VRC89	(67Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111101”	
VRC88	(68Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111110”	
VRC87	(69Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111111”	
VRC154	(2.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000000”	VINP8
VRC153	(3Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000001”	
VRC152	(4Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000010”	
VRC151	(5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000011”	
VRC150	(6Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000100”	
VRC149	(7Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000101”	
VRC148	(8Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000110”	
VRC147	(9Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000111”	
VRC146	(10Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001000”	
VRC145	(11Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001001”	
VRC144	(12Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001010”	
VRC143	(13Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001011”	
VRC142	(14Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001100”	
VRC141	(15Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001101”	
VRC140	(16Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001110”	
VRC139	(17Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001111”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC138	(18Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010000”	
VRC137	(19Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010001”	
VRC136	(20Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010010”	
VRC135	(21Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010011”	

Table 63. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC134	(22Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010100”	VINP8
VRC133	(23Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010101”	
VRC132	(24Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010110”	
VRC131	(25Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010111”	
VRC130	(26Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011000”	
VRC129	(27Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011001”	
VRC128	(28Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011010”	
VRC127	(29Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011011”	
VRC126	(30Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011100”	
VRC125	(31Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011101”	
VRC124	(32Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011110”	
VRC123	(33Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011111”	
VRC122	(34Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100000”	
VRC121	(35Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100001”	
VRC120	(36Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100010”	
VRC119	(37Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100011”	
VRC118	(38Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100100”	
VRC117	(39Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100101”	
VRC116	(40Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100110”	
VRC115	(41Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100111”	
VRC114	(42Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101000”	
VRC113	(43Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101001”	
VRC112	(44Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101010”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101011”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101100”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101101”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101110”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101111”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110000”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110001”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110010”	
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110011”	
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110100”	
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110101”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110110”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110111”	

Table 64. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111000”	VINP8
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111001”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111010”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111011”	
VRC94	(62Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111100”	
VRC93	(63Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111101”	
VRC92	(64Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111110”	
VRC91	(65Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111111”	
VRC158	(0.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000000”	VINP9
VRC157	(1Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000001”	
VRC156	(1.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000010”	
VRC155	(2Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000011”	
VRC154	(2.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000100”	
VRC153	(3Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000101”	
VRC152	(4Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000110”	
VRC151	(5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000111”	
VRC150	(6Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001000”	
VRC149	(7Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001001”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC148	(8Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001010”	
VRC147	(9Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001011”	
VRC146	(10Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001100”	
VRC145	(11Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001101”	
VRC144	(12Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001110”	
VRC143	(13Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001111”	
VRC142	(14Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010000”	
VRC141	(15Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010001”	
VRC140	(16Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010010”	
VRC139	(17Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010011”	
VRC138	(18Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010100”	
VRC137	(19Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010101”	
VRC136	(20Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010110”	
VRC135	(21Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010111”	
VRC134	(22Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011000”	
VRC133	(23Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011001”	
VRC132	(24Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011010”	
VRC131	(25Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011011”	

Table 65. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC130	(26Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011100”	VINP9
VRC129	(27Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011101”	
VRC128	(28Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011110”	
VRC127	(29Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011111”	
VRC126	(30Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100000”	
VRC125	(31Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100001”	
VRC124	(32Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100010”	
VRC123	(33Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100011”	
VRC122	(34Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100100”	
VRC121	(35Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100101”	
VRC120	(36Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100110”	

Preliminary

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC119	(37Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100111”	
VRC118	(38Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101000”	
VRC117	(39Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101001”	
VRC116	(40Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101010”	
VRC115	(41Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101011”	
VRC114	(42Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101100”	
VRC113	(43Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101101”	
VRC112	(44Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101110”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101111”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110000”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110001”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110010”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110011”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110100”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110101”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110110”	
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110111”	
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111000”	
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111001”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111010”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111011”	
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111100”	
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111101”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111110”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111111”	

Preliminary

Table 66. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 2

Grayscale Voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	VC-(VC-V43) * (0.5/11.5)
V1	VINP1	V33	VC-(VC-V43) * (1.25/11.5)
V2	V1-(V1-V4) * (6/12)	V34	VC-(VC-V43) * (2.25/11.5)
V3	V1-(V1-V4) * (10/12)	V35	VC-(VC-V43) * (3/11.5)
V4	VINP2	V36	VC-(VC-V43) * (4/11.5)
V5	V4-(V4-V8) * (2.5/7.5)	V37	VC-(VC-V43) * (5/11.5)
V6	V4-(V4-V8) * (4.5/7.5)	V38	VC-(VC-V43) * (6/11.5)
V7	V4-(V4-V8) * (6/7.5)	V39	VC-(VC-V43) * (7/11.5)
V8	VINP3	V40	VC-(VC-V43) * (8/11.5)
V9	V8-(V8-V20) * (1.5/13.25)	V41	VC-(VC-V43) * (9/11.5)
V10	V8-(V8-V20) * (3.5/13.25)	V42	VC-(VC-V43) * (10.5/11.5)
V11	V8-(V8-V20) * (4.5/13.25)	V43	VINP6
V12	V8-(V8-V20) * (5.5/13.25)	V44	V43-(V43-V55) * (1/17.5)
V13	V8-(V8-V20) * (6.75/13.25)	V45	V43-(V43-V55) * (2.5/17.5)
V14	V8-(V8-V20) * (7.75/13.25)	V46	V43-(V43-V55) * (3.75/17.5)
V15	V8-(V8-V20) * (8.75/13.25)	V47	V43-(V43-V55) * (4.75/17.5)
V16	V8-(V8-V20) * (9.75/13.25)	V48	V43-(V43-V55) * (6.5/17.5)
V17	V8-(V8-V20) * (10.75/13.25)	V49	V43-(V43-V55) * (7.5/17.5)
V18	V8-(V8-V20) * (11.75/13.25)	V50	V43-(V43-V55) * (9/17.5)
V19	V8-(V8-V20) * (12.75/13.25)	V51	V43-(V43-V55) * (10.5/17.5)
V20	VINP4	V52	V43-(V43-V55) * (12/17.5)
V21	V20-(V20-VC) * (1.5/12.25)	V53	V43-(V43-V55) * (13.5/17.5)
V22	V20-(V20-VC) * (2.5/12.25)	V54	V43-(V43-V55) * (15.5/17.5)
V23	V20-(V20-VC) * (3.75/12.25)	V55	VINP7
V24	V20-(V20-VC) * (4.75/12.25)	V56	V55-(V55-V59) * (2/9.5)
V25	V20-(V20-VC) * (5.75/12.25)	V57	V55-(V55-V59) * (4/9.5)
V26	V20-(V20-VC) * (6.75/12.25)	V58	V55-(V55-V59) * (6.5/9.5)
V27	V20-(V20-VC) * (7.75/12.25)	V59	VINP8
V28	V20-(V20-VC) * (8.75/12.25)	V60	V59-(V59-V62) * (3.5/11.5)
V29	V20-(V20-VC) * (9.75/12.25)	V61	V59-(V59-V62) * (6.5/11.5)
V30	V20-(V20-VC) * (10.75/12.25)	V62	VINP9
V31	V20-(V20-VC) * (11.75/12.25)	V63	VINP10

Preliminary

Grayscale Voltage	Formula	Grayscale voltage	Formula
VC	VINP5		

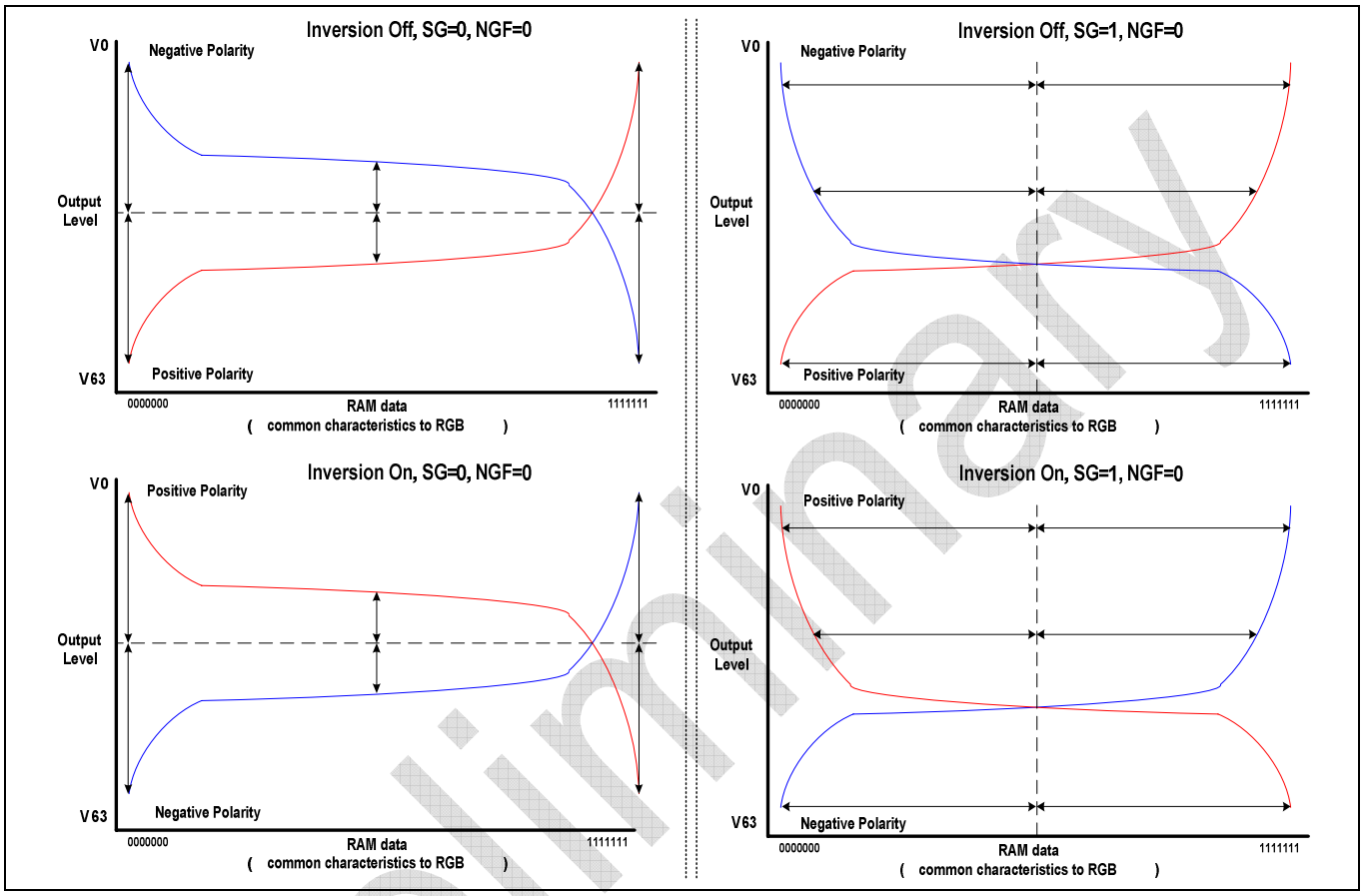
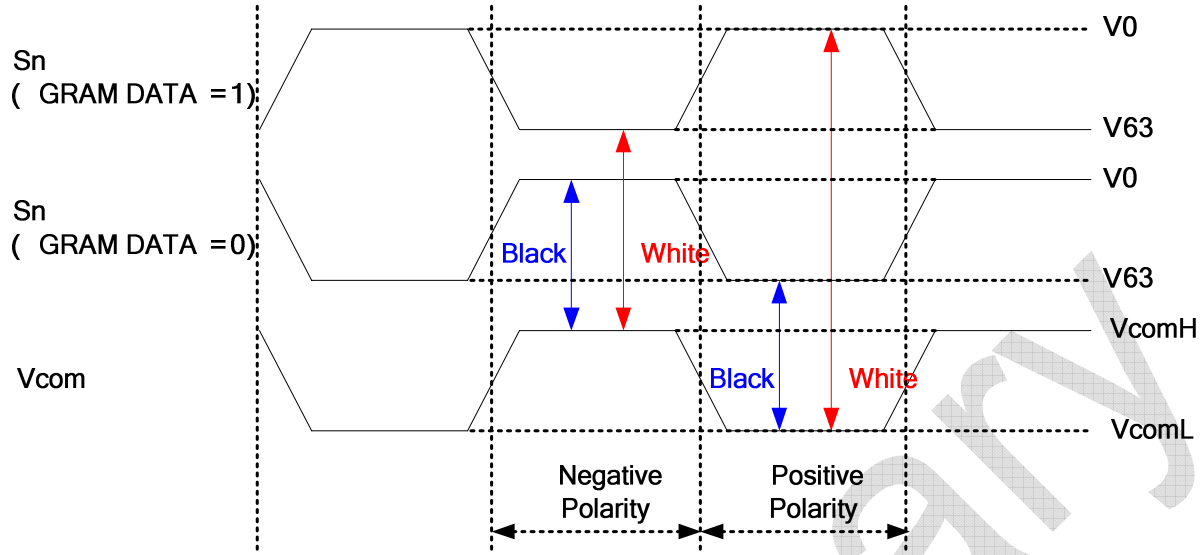
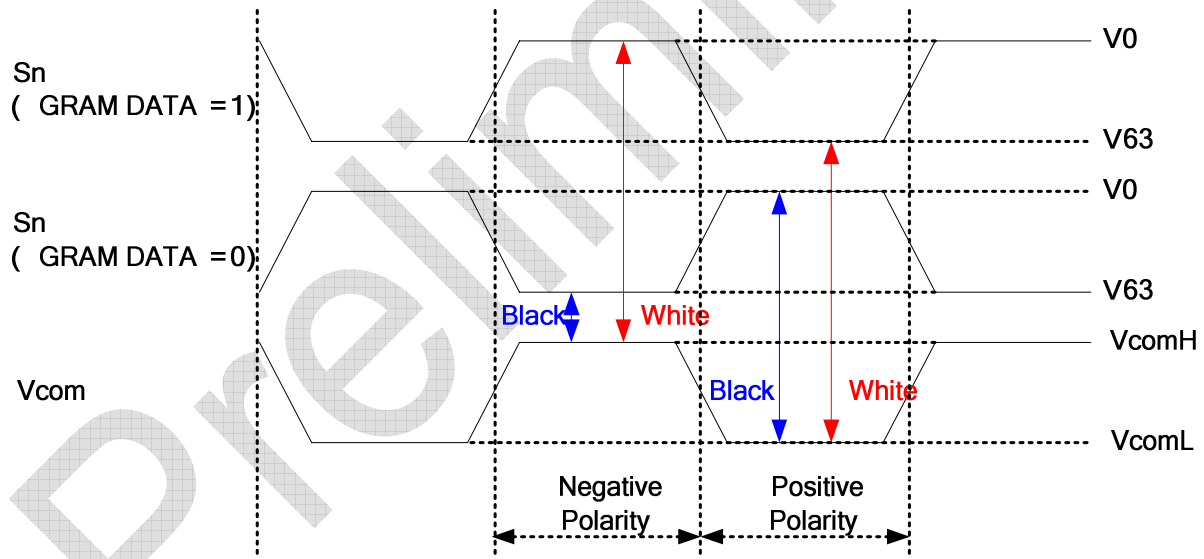


Figure88. Relationship Between RAM Data and Output Voltage

Preliminary



(a) For Normally Black Panel (Inversion Off)



(b) For Normally White Panel (Inversion On)

Preliminary

Figure89. Relationship Between Source Output and VCOM

4.3. DISPLAY DATA RAM

4.3.1. CONFIGURATION

S6D04K1 has an integrated 320x240x18-bit graphic type of static RAM. This memory allows storing on-chip a 320xRGBx240 image with 18-bit resolution. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.Memory to Display Address Mapping

4.3.1.1. When using 320RGB x 240 resolution

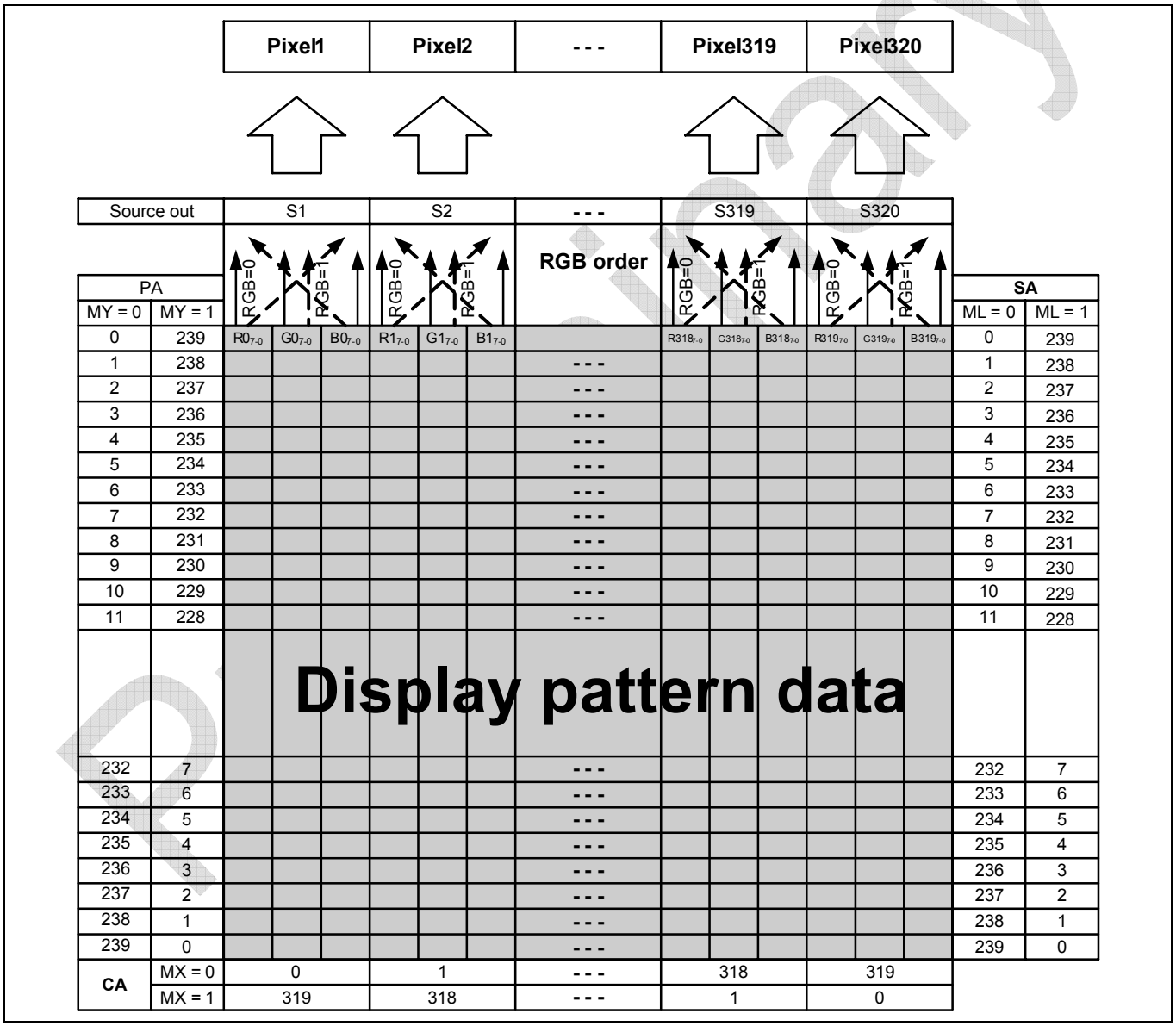


Figure90. When Using 320RGB x240 Resolution

Note.

PA = Page Address,

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), B6 parameter of MADCTL command

MY = Mirror Y-axis (Page address direction parameter), B7 parameter of MADCTL command

ML = Scan direction parameter, B4 parameter of MADCTL command

RGB= Red, Green and Blue pixel position change, B3 parameter of MADCTL command

Preliminary

4.3.2. NORMAL DISPLAY ON OR PARTIAL MODE ON, VERTICAL SCROLL OFF

4.3.2.1. When using 320RGB x 240 resolution

In this mode, contents of the frame memory within an area where column pointer is 00h to EFh and page pointer is 000h to EFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

1). Example for Normal Display On (B6 = B7 = B4 = ‘0’ on MADCTL)

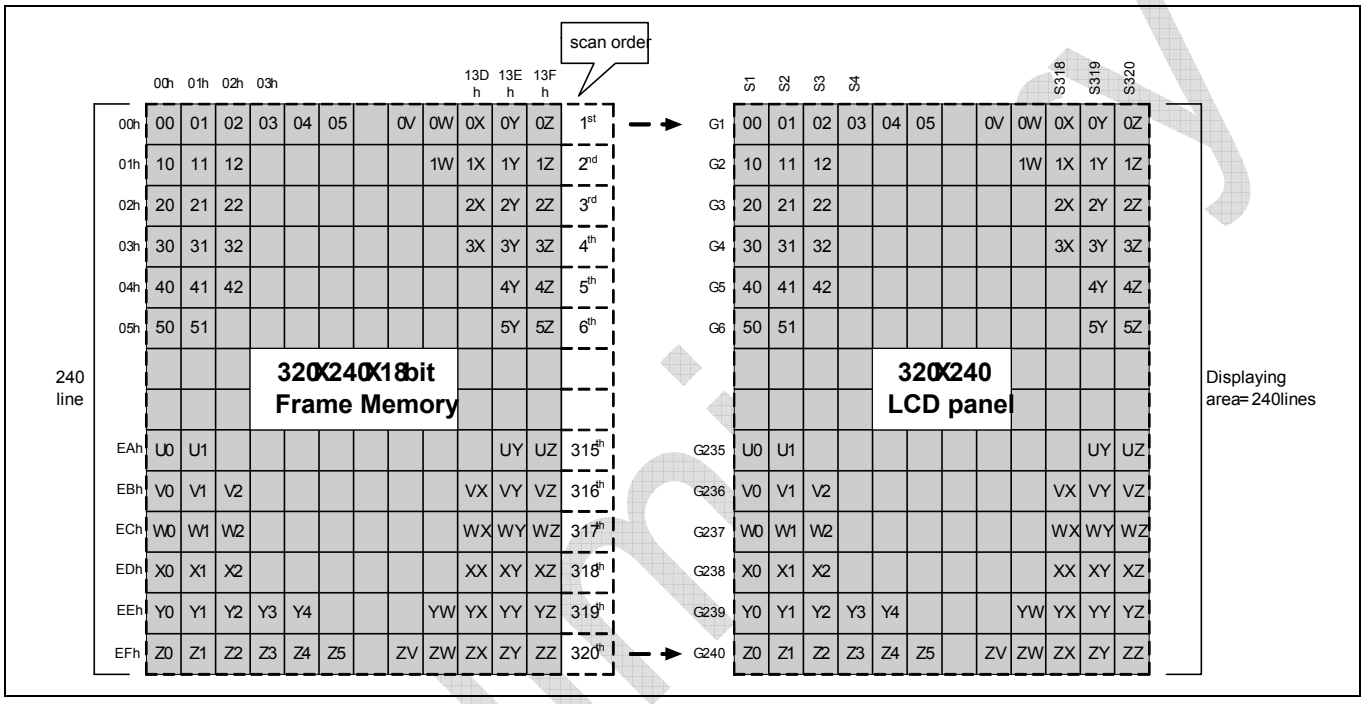


Figure91. Normal Display On (B6 = B7 = B4 = ‘0’ On MADCTL)

Preliminary

2). Partial display on: SR [15:0] = 04h, ER [15:0] = ECh, madctl (B6 = B7 = B4 = ‘0’)

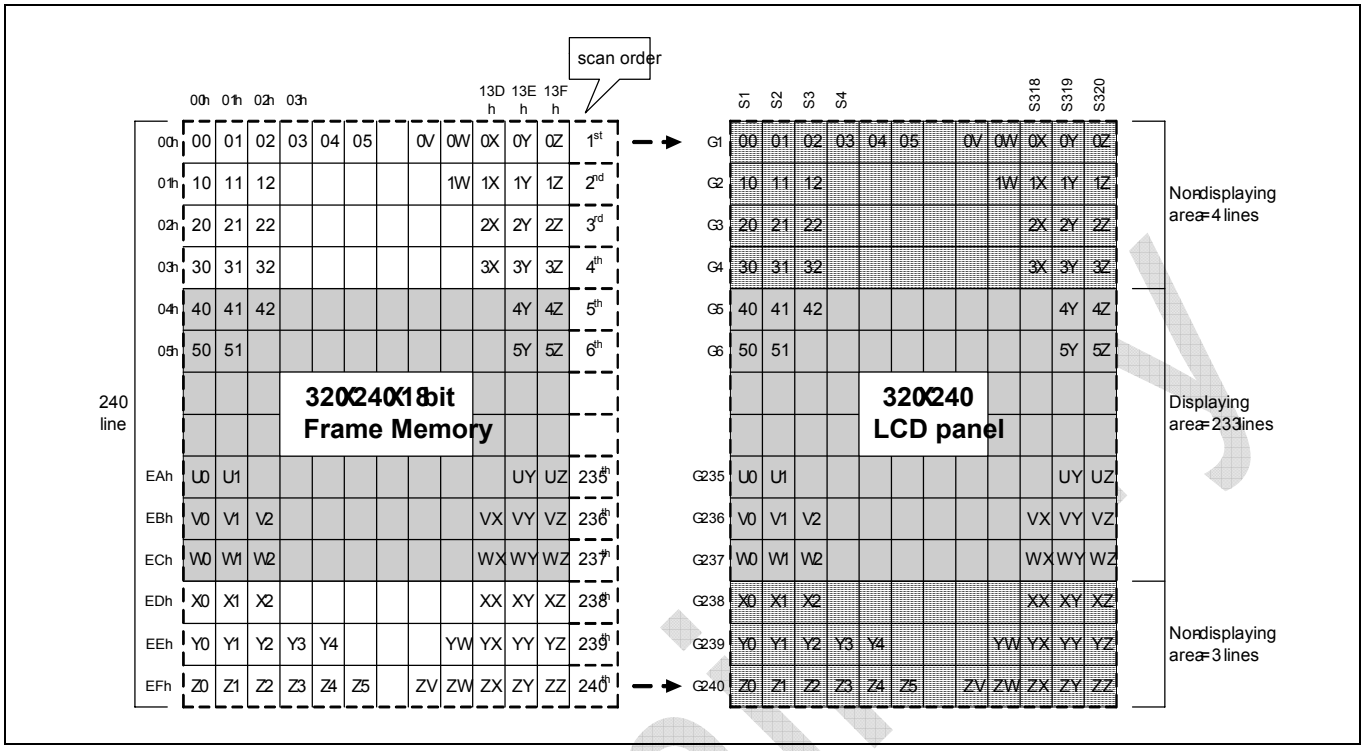
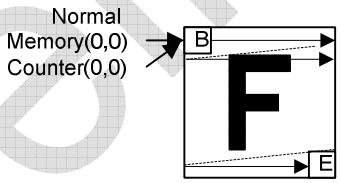
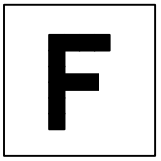
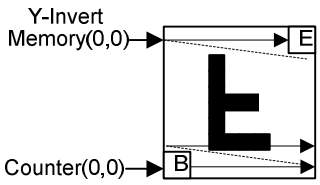
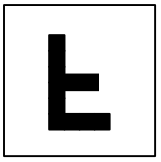
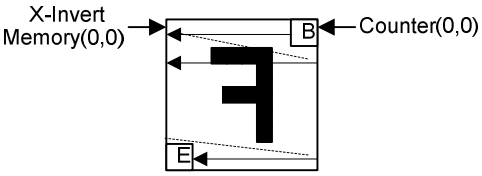
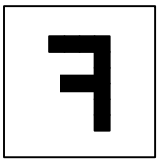
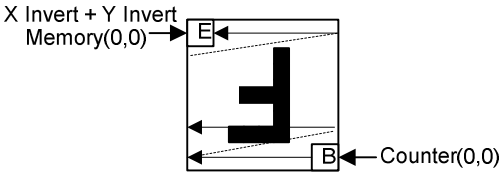
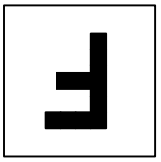
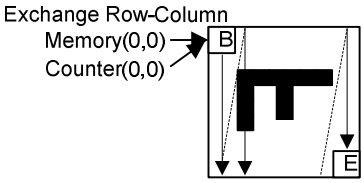
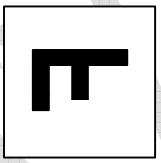
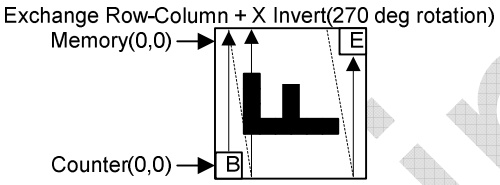
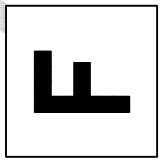
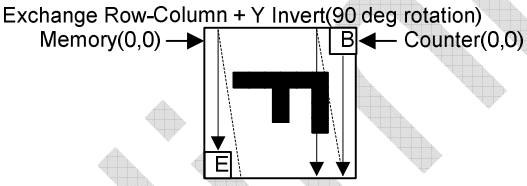
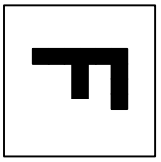
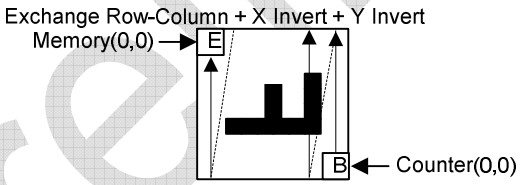
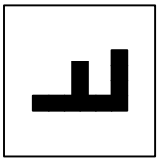


Figure92. Partial Display On: SR [15:0] = 04h, ER [15:0] = ECh, MADCTL (B6 = B7 = B4 = ‘0’)

Table 67. MPU to Memory Write/Read Direction By Madctl

B5 B6 B7 (Bits)	Image in the Memory (“→” Means “MPU to Memory Read/Write Direction”)	IMAGE in the Display
0 0 0		
0 0 1		
0 1 0		

Preliminary

B5 B6 B7 (Bits)	Image in the Memory ("→" Means "MPU to Memory Read/Write Direction")	IMAGE in the Display
0 1 1		
1 0 0		
1 0 1		
1 1 0		
1 1 1		

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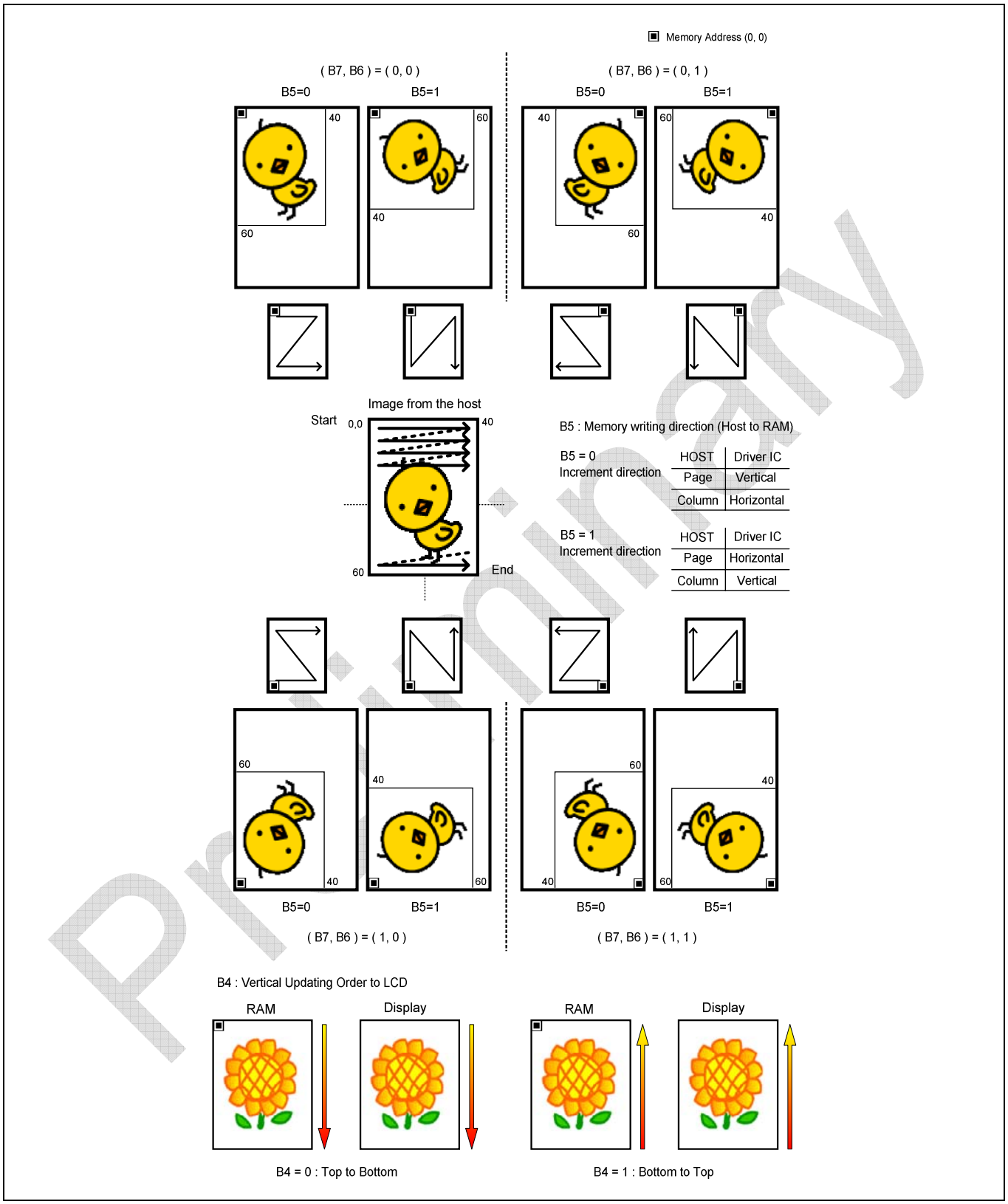


Figure93. Example for Rotation With B7, B6, B5 and B4

Preliminary

4.3.3. COMMAND DEFINITION WHICH INDEPENDENT OF THE IC MOUNT POSITION

Depending on how the MADCTL command is set, the top-bottom / left-right definitions are changed in the driver IC to adapt the mounted form.

4.3.3.1. Model of LCD module for the S6D04K1

The LCD module for the S6D04K1 is shown below. The top-bottom / left-right positions, RGB filter and white or black ground defined in this development specification are in accordance with the diagram shown below.

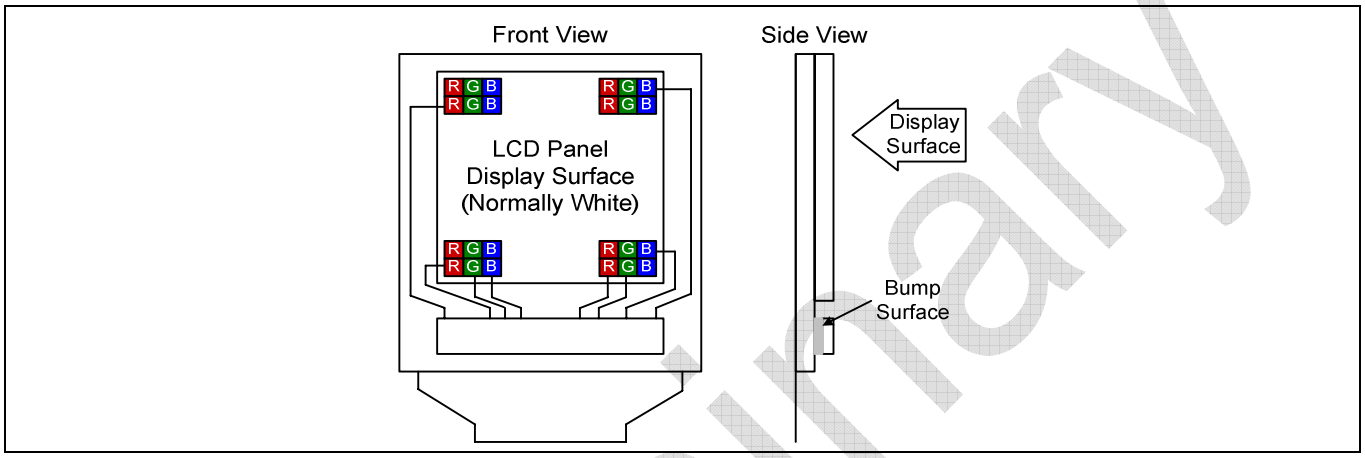


Figure94. Model of LCD Module for the S6D04K1

4.3.3.2. Position definition by IC mount

The set value of MADCTL actually used internally in the IC changes depending on how MADCTL is set. The arithmetic operation in the table below is performed on each bit.

Table 68. Position Definition by IC Mount

MADCTL(36h)	IFCTL(F7h)	IC Internal Setting Value
0	0	0
0	1	1
1	0	1
1	1	0

The set value of MADCTL in the case in which is set to “00h” make a result in the memory access control direction as onto below.

Preliminary

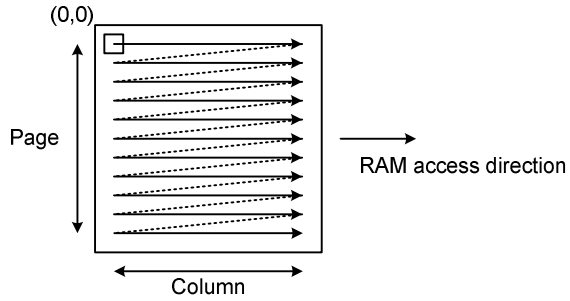
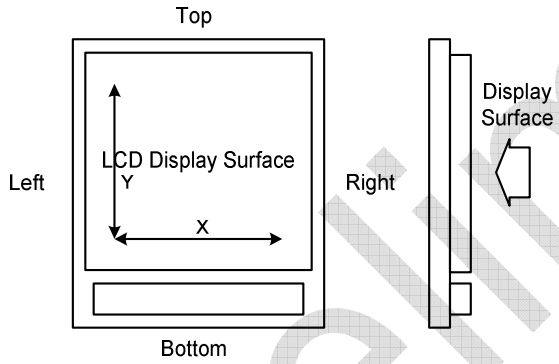


Figure95. Memory Access Control Direction

Refer to the top-bottom / left-right relationship. (The non-bump plane is the surface.)

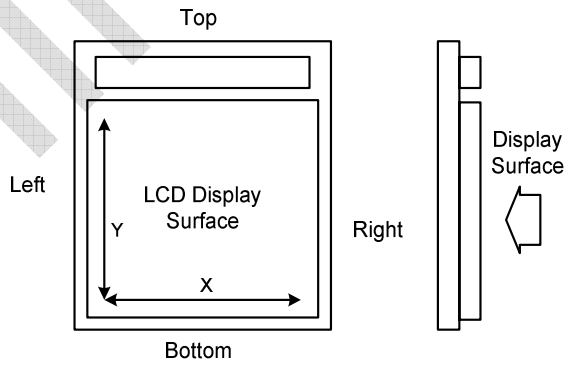
If the driver IC is left-mounted or right-mounted due to the device structure, the display data RAM to LCD display data readout and gate scan direction should be set left-right rather than top-bottom.

Case of Bottom-Mounted IC



(Example) MADCTL(00h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Top to Bottom
Gate line scan Direction	Top to Bottom

Case of Top-Mounted IC



(Example) MADCTL(D0h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Top to Bottom
Gate line scan Direction	Top to Bottom

.

Case of Left-Mounted IC

Case of Right-Mounted IC

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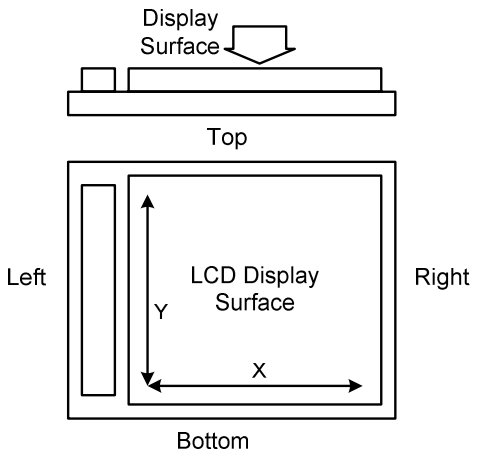
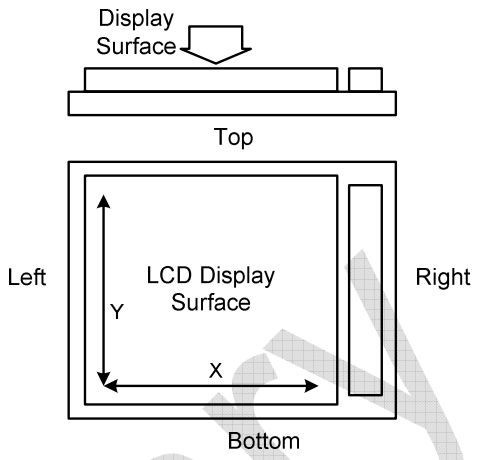


(Example) MADCTL(A0h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Right to Left
Gate line scan Direction	Right to Left



(Example) MADCTL(60h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Left to Right
Gate line scan Direction	Left to Right

Figure96. Relationship of Each Direction

Preliminary

4.3.4. 0-ADDRESS POSITION AND RAM ACCESS SCAN DIRECTION

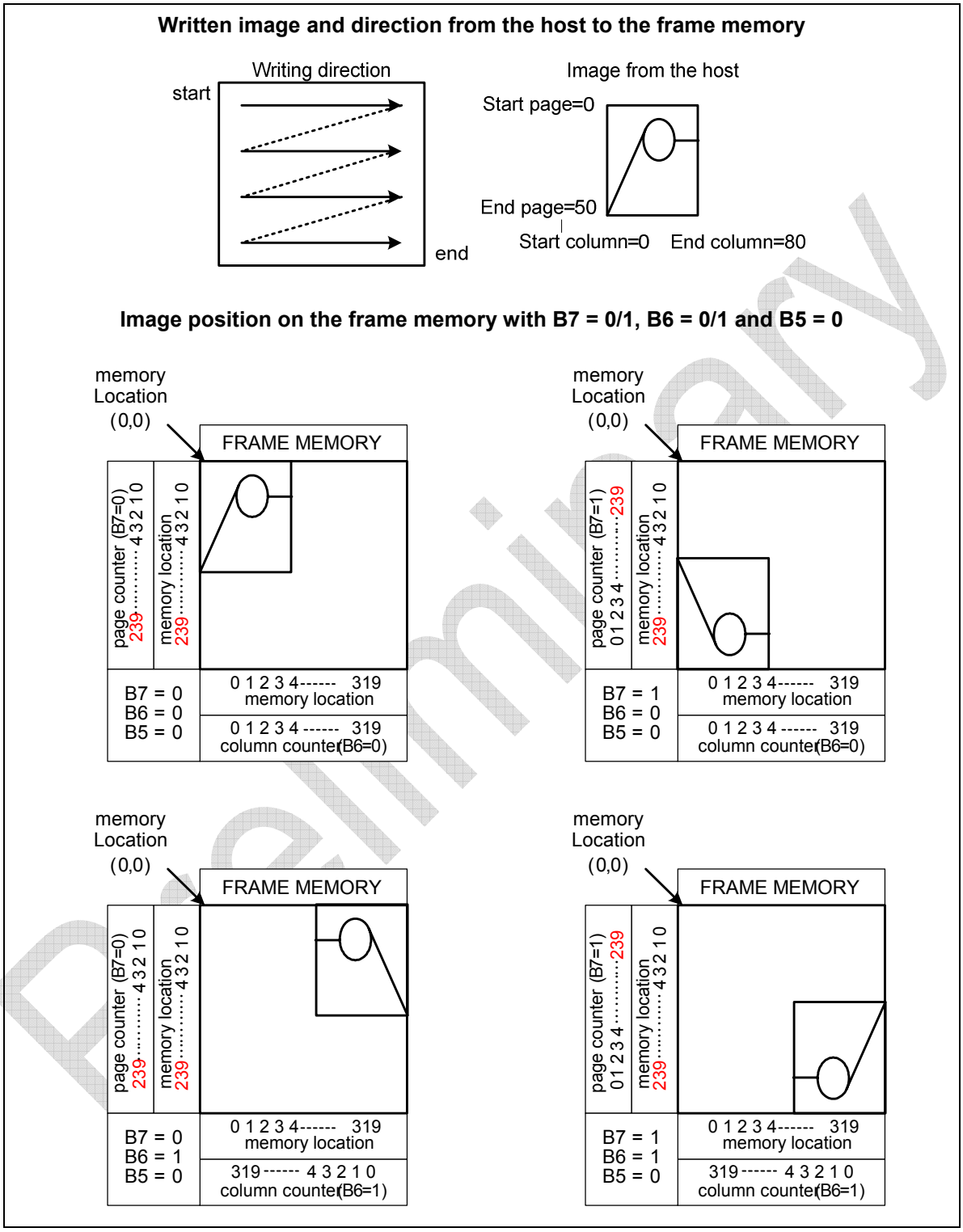


Figure97. Refer to MADCTL (MADCTL=00h)

Preliminary

Written image and direction from the host to the frame memory

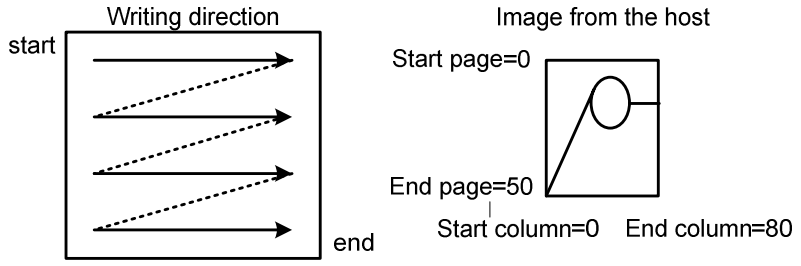


Image position on the frame memory with B7 = 0/1, B6 = 0/1 and B5 = 1

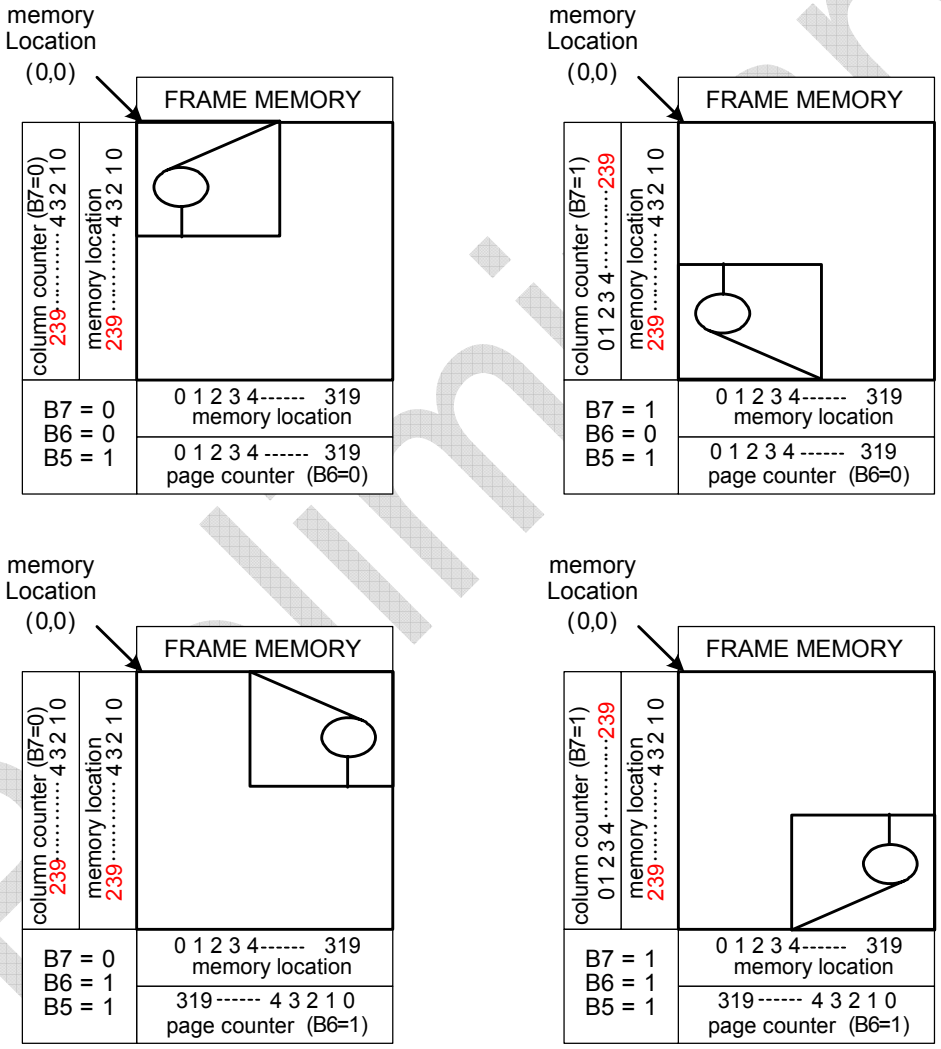


Figure98. Refer to MADCTL (MADCTL=00h)

4.4. MTP CONTROL

4.4.1. 576-BIT MTP CONTENT

The 576-bit MTP consists of MTP_LOADSEL, ID1/ID2/ID3, VCOM offset adjustment, VCOMH/L adjustment, Gamma2.2 adjustment, front/back porch control (for audible noise reduction), voltage control for different LC (Liquid Crystal), and MDDI adjustment.

Table 69. 576-bit MTP content

For Whom	Contents	# of Bits	Description
Module Maker	MTP_LOADSEL	7	Bit[0] for load control of ID1/ID2/ID3 Bit[1] for load control of VCOM offset adjustment Bit[2] VCOMH/L adjustment Bit[3] Gamma2.2 adjustment Bit[4] front/back porch control Bit[5] voltage control for different LC (Liquid Crystal) Bit[6] MDDI adjustment; If =0, no MTP load to corresponding registers If =1, load MTP to corresponding registers
Set & Module Maker (ID for Module)	ID1, ID2, ID3	8x3=24	ID1, ID2, ID3 of Nokia L1 registers
Module Maker	VCOM offset	6	VCOM offset adjustment
Module Maker	VCOMH/L	14	VCOMH/L adjustment
Module Maker	Gamma2.2	136x3 =408	Gamma2.2 adjustment
Module Maker	front/back porch	44	front/back porch control for audible noise reduction
Module Maker	voltage control	30	voltage control for different LC (Liquid Crystal)
Module Maker	MDDI	15	MDDI adjustment
Total		548	28 bits are reserved bits

Preliminary

4.4.2. 576-BIT MTP ADDRESS MAPPING

The MTP address mapping is fixed and cannot be changed. The table below shows the MTP address mapping.

Preliminary

Table 70. 576-bit MTP Address Mapping

block address	byte address	D7	D6	D5	D4	D3	D2	D1	D0
		B7	B6	B5	B4	B3	B2	B1	B0
0	0	RD2_P0_RES[7]	RD2_P0_MDDI_SET	RD2_P0_POWER_SET	RD2_P0_AUDIO_SET	RD2_P0_GAMMA_SET	RD2_P0_VCMHL_SET	RD2_P0_VCMOC_SET	RD2_P0_ID_SET
	1	RD2_P1_ID1[7:0]							
	2	RD2_P2_ID2[7:0]							
	3	RD2_P3_ID3[7:0]							
1	4	RF6_NSR_BLK[1:0]		RD2_P4_VCMCO[5:0]					
	5	RF6_SAP[2]	RD2_P5_VCMH,RF5_P2_VCMH[6:0]						
	6	RF6_SAP[1]	RD2_P6_VCML,RF5_P3_VCML[6:0]						
	7	RF6_SAP[0]	RD2_P7_VHIB_LVL,REA_P1_VHIB_LVL[2:0]			RD2_P7_IREF_LVL,REA_P1_IREF_LVL[3:0]			
2	8	RD2_P8_MDDI_SET2,REA_P2_MDDI_SET2[7:0]							
	9	RF2_REV	RF4_NGVD[6:0],RF4_PIGVD[6:0]						
	10	RF6_SG	RF4_NBT,PIBT[2:0]			RF4_VC[3:0]			
	11	RF6_PISR_BLK[1:0]		RF4_NDC3,PIDC3[1:0]		RF4_NDC2,PIDC2[1:0]		RF4_NDC1,PIDC1[1:0]	
3	12	RFA_RRFP[5:4]		RFA_RPKP0[5:0]					
	13	RFA_RRFP[3:2]		RFA_RPKP1[5:0]					
	14	RFA_RRFP[1:0]		RFA_RPKP2[5:0]					
	15	RFA_ROSP[5:4]		RFA_RPKP3[5:0]					
4	16	RFA_ROSP[3:2]		RFA_RPKP4[5:0]					
	17	RFA_ROSP[1:0]		RFA_RPKP5[5:0]					
	18	RF6_NSR_ND	RF6_PISR_ND	RFA_RPKP6[5:0]					

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	19	RD2_P9_RES1[7:6]	RFA_RPKP7[5:0]
5	20	RFA_RGLP[1:0]	RFA_RPKP8[5:0]
	21	RFB_RRFN[5:4]	RFB_RPKN0[5:0]
	22	RFB_RRFN[3:2]	RFB_RPKN1[5:0]
	23	RFB_RRFN[1:0]	RFB_RPKN2[5:0]
6	24	RFB_ROSN[5:4]	RFB_RPKN3[5:0]
	25	RFB_ROSN[3:2]	RFB_RPKN4[5:0]
	26	RFB_ROSN[1:0]	RFB_RPKN5[5:0]
	27	RD2_P10_RES2[1:0]	RFB_RPKN6[5:0]
7	28	RD2_P10_RES2[3:2]	RFB_RPKN7[5:0]
	29	RFB_RGLN[1:0]	RFB_RPKN8[5:0]
	30	GRFP[5:4]	GPKP0[5:0]
	31	GRFP[3:2]	GPKP1[5:0]
8	32	GRFP[1:0]	GPKP2[5:0]
	33	GOSP[5:4]	GPKP3[5:0]
	34	GOSP[3:2]	GPKP4[5:0]
	35	GOSP[1:0]	GPKP5[5:0]
9	36	RD2_P10_RES2[5:4]	GPKP6[5:0]
	37	RD2_P10_RES2[7:6]	GPKP7[5:0]
	38	GRGLP[1:0]	GPKP8[5:0]
	39	GRFN[5:4]	GPKN0[5:0]
10	40	GRFN[3:2]	GPKN1[5:0]

	41	GRFN[1:0]	GPKN2[5:0]
	42	GOSN[5:4]	GPKN3[5:0]
	43	GOSN[3:2]	GPKN4[5:0]
11	44	GOSN[1:0]	GPKN5[5:0]
	45	RD2_P11_RES3[1:0]	GPKN6[5:0]
	46	RD2_P11_RES3[3:2]	GPKN7[5:0]
	47	GGLN[1:0]	GPKN8[5:0]
12	48	BRFP[5:4]	BPKP0[5:0]
	49	BRFP[3:2]	BPKP1[5:0]
	50	BRFP[1:0]	BPKP2[5:0]
	51	BOSP[5:4]	BPKP3[5:0]
13	52	BOSP[3:2]	BPKP4[5:0]
	53	BOSP[1:0]	BPKP5[5:0]
	54	RD2_P11_RES3[5:4]	BPKP6[5:0]
	55	RD2_P11_RES3[7:6]	BPKP7[5:0]
14	56	BGLP[1:0]	BPKP8[5:0]
	57	BRFN[5:4]	BPKN0[5:0]
	58	BRFN[3:2]	BPKN1[5:0]
	59	BRFN[1:0]	BPKN2[5:0]
15	60	BOSN[5:4]	BPKN3[5:0]
	61	BOSN[3:2]	BPKN4[5:0]
	62	BOSN[1:0]	BPKN5[5:0]

	63	RD2_P12_RES4[1:0]	BPKN6[5:0]
16	64	RD2_P12_RES4[3:2]	BPKN7[5:0]
	65	BGLN[1:0]	BPKN8[5:0]
	66	RF2_NHW[7:0],RF2_PIHW[7:0]	
	67	RF2_NVBP[7:0],RF2_PIVBP[7:0]	
17	68	RF2_NVFP[7:0],RF2_PIVFP[7:0]	
	69	RD2_P12_RES4[5:4]	RF2_DIV_SRC[5:0]
	70	RD2_P12_RES4[7:6]	RF5_VCIR1[4:0]
	71	RFD_NFOSC[4:0],RFD_PIFOSC[4:0]	RF6_NSDT[3:0],RF6_PISDT[3:2]

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MTP CONTROL FUNCTION

MTP should be erased (data becomes all zeros) and programmed (to be one) according to the erase/program flow shown below.

During the erase flow, all bits are erased at the same time, whereas program is performed block by block. There are 32 bits per each block. MTP data are also loaded block by block when H/W reset, S/W reset or sleep-out commands is applied, which are converted to 8bit data and being read though MCU I/F.

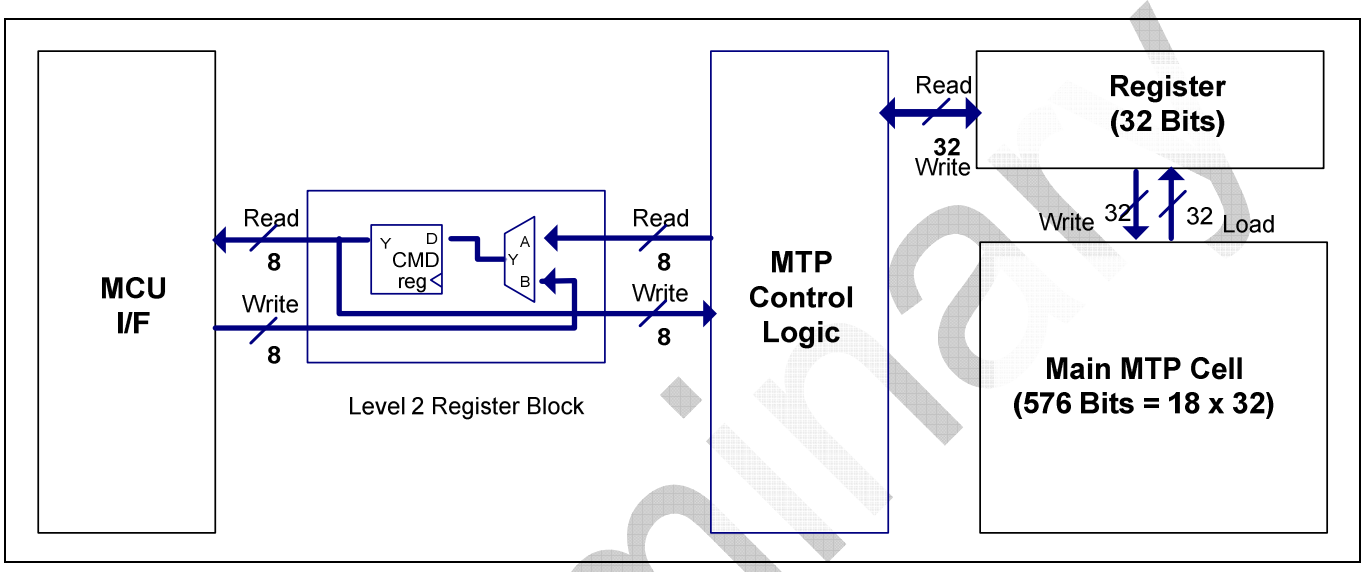

Figure99. Registers Configuration of 512-bit MTP

Preliminary

4.4.3. MTP CONTROL IN EXTERNAL MODE

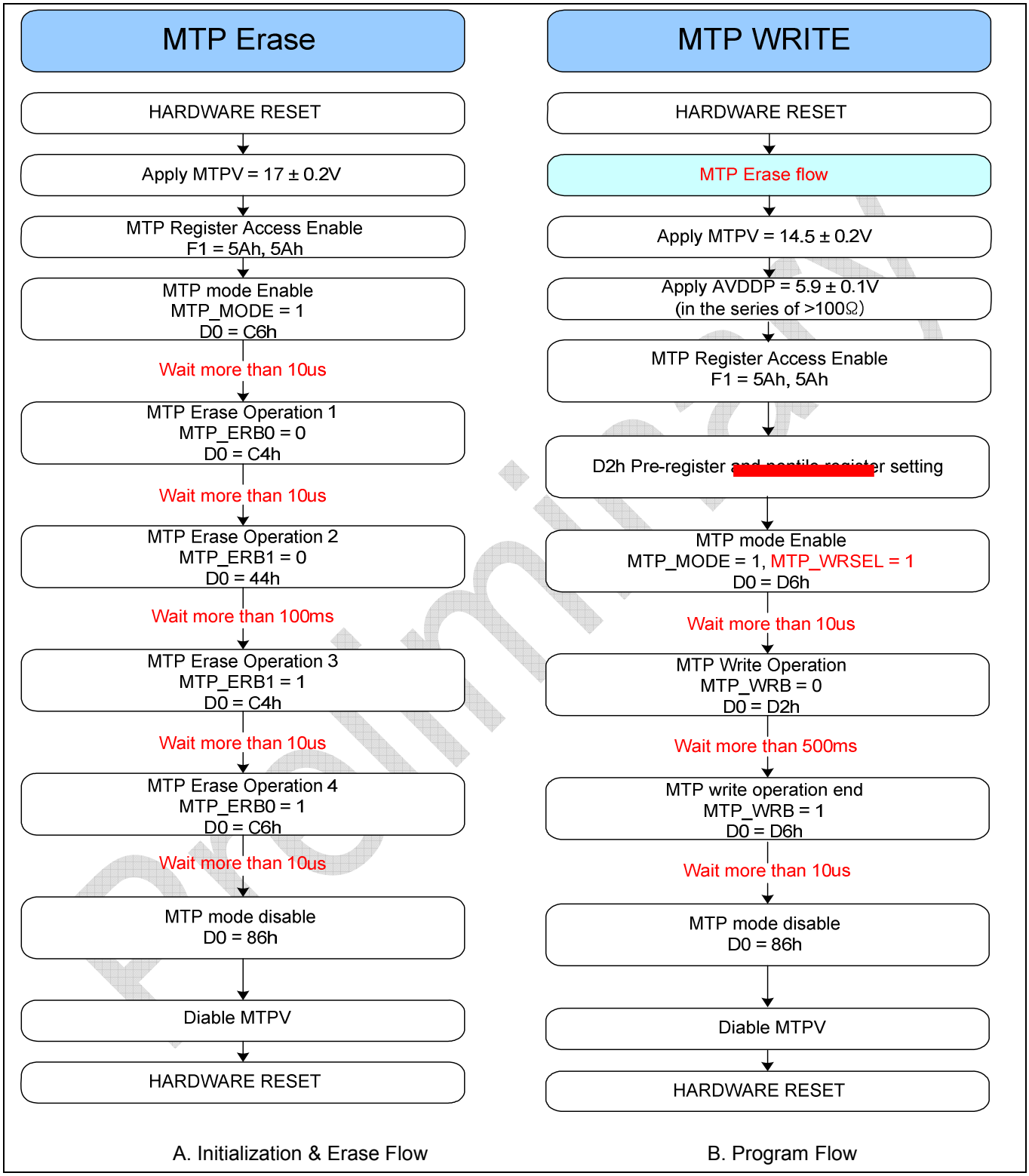

Figure100. MTP initialization, erase and program

4.5. TEARING EFFECT OUTPUT LINE

Tearing Effect is the effect that the overwritten two frames are shown as they are torn when Display Data RAM (DDRAM) is updated during Display Driver IC (DDI) scans the panel. This effect caused by the asynchronous timing between scanning of the DDI timing controller and frame transfer of the host processor.

To help the host processor avoid this effect, DDI generates Tearing Effect output line (TE) signal which has the timing of the period in which the DDI does not do panel-scan and the timing of vertical or horizontal synchronization. Host processor can avoid Tearing Effect by transfer only during TE signal is high.

The period in which the DDI does not panel-scan is the vertical blanking time. By TEON Command (35h) with parameter 0, the host can make the TE pin high in the vertical blanking time. With parameter 1, the TE signal includes the vertical blanking time and horizontal sync. By TEOFF Command (34h), the host can turn off the TE signal and this is the default state.

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4.5.1. TEARING EFFECT LINE MODES

Mode 1, TEON (35h) Command, Parameter 0: The Tearing Effect Output signal consists of V-Blanking Information only

Figure101. Tearing Effect Line Mode 1

t_{vdh} = The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory(except Invisible Line – see below).

Mode 2, TEON (35h) Command, Parameter 1: the Tearing Effect Output signal consists of V-Blanking and H-Sync

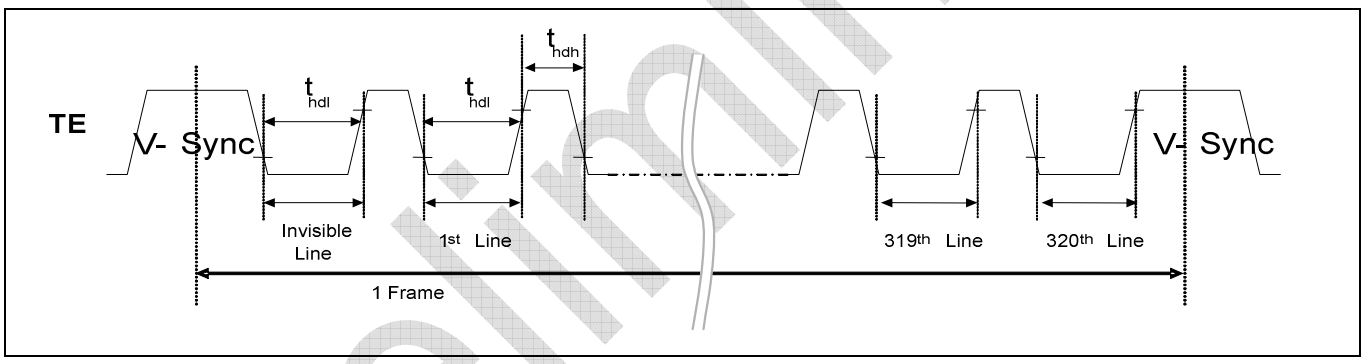

Figure102. Tearing Effect Line Mode 2

t_{hdh} = The LCD display is not updated from the Frame Memory

t_{hdl} = The LCD display is updated from the Frame Memory(except Invisible Line – see below).

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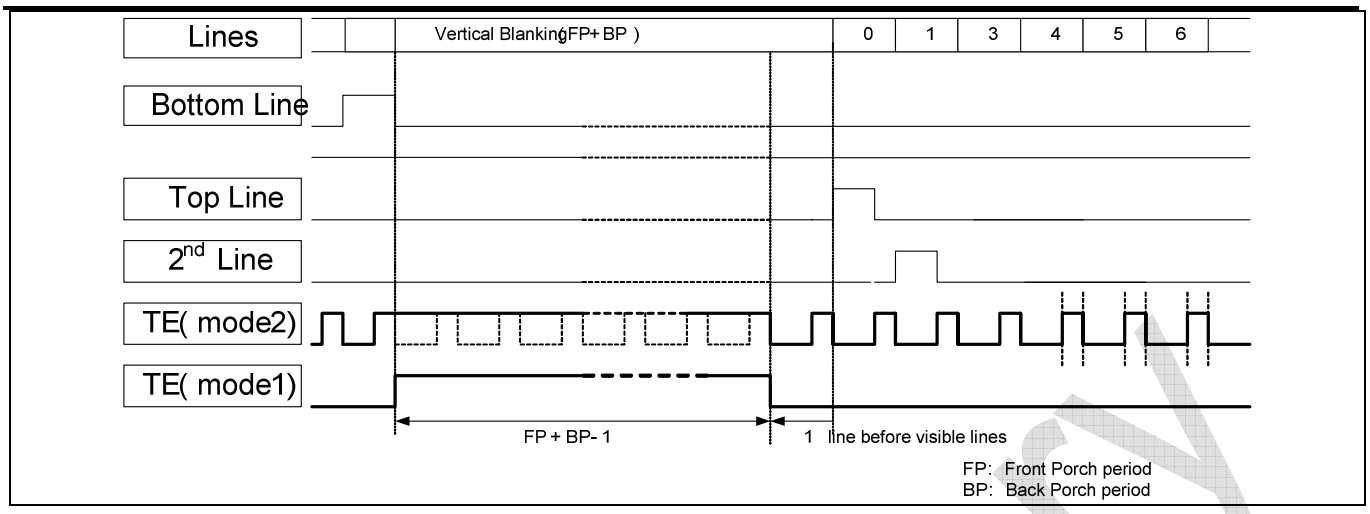

Note.

During Sleep In Mode, the Tearing Effect Pin Output is Low.

Preliminary

4.5.2. TEARING EFFECT LINE TIMINGS

The Tearing Effect signal is described below

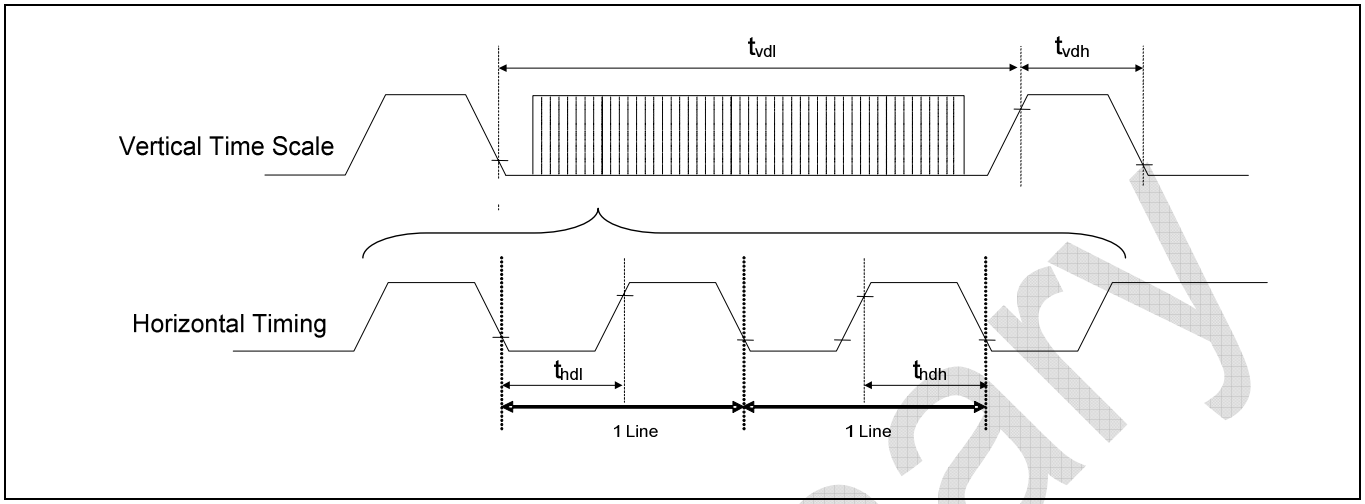

Figure103. Tearing Effect Line Timing

Table 71. AC Characteristics of Tearing Effect Signal

Symbol	Parameter	Min	Max	Unit	Description
tvdl	Vertical Timing Low Duration	-	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	-	-	µs	
thdh	Horizontal Timing High Duration	-	500	µs	

Note.

1. Idle Mode Off/On (Frame Rate = 60 Hz)
2. The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns.

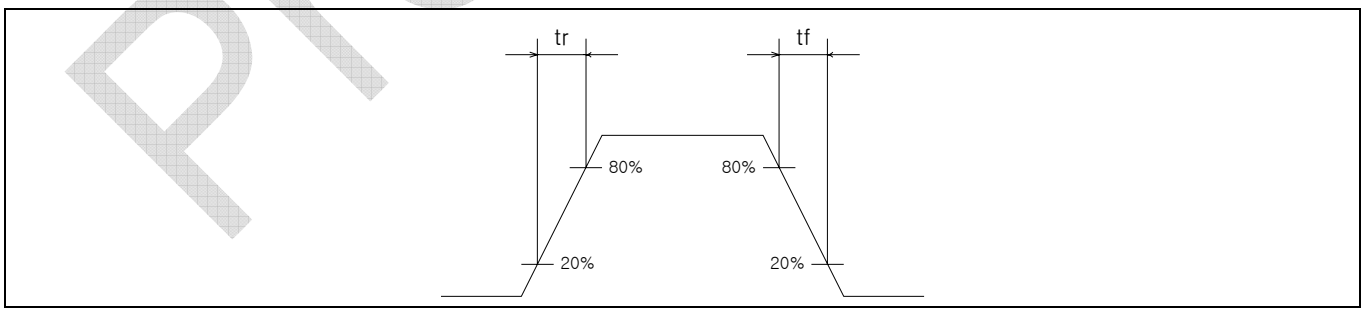

Figure104. Rising and Falling Times

The Tearing Effect Output Line is fed back to the MPU and should be below to avoid Tearing Effect.

Preliminary

4.6. SLEEP OUT COMMAND AND SELF-DIAGNOSTIC FUNCTIONS

4.6.1. REGISTER LOADING DETECTION

Sleep out command (See “Sleep out (11h) command”) is a trigger for an internal function of the display module which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: Compares register and EEPROM) values, 2nd step: Loads EEPROM value to register. If those both values (EEPROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command 5.1.10 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

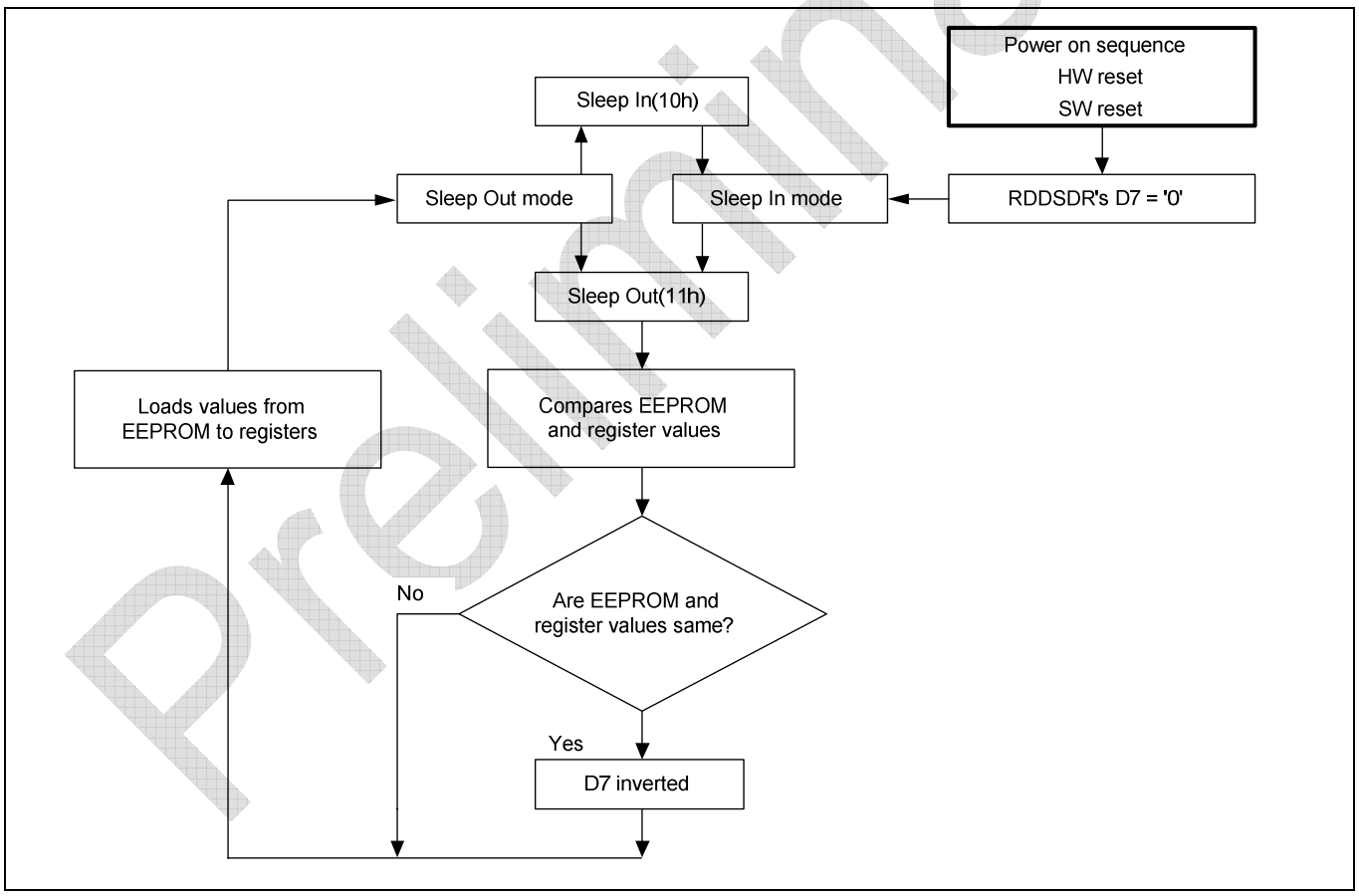

Figure105. Flowchart of Register Loading Detection

Note.

There is not compared and loaded register values, which can be changed by the display module.

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4.6.2. FUNCTIONALITY DETECTION

Sleep out command (See section 5.1.12 “Sleep Out (11h) command”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. step up circuit voltage levels, timings, etc.) If functionality requirement is met, there is inverted (=increased by 1) a bit, which defined in command 5.1.10 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

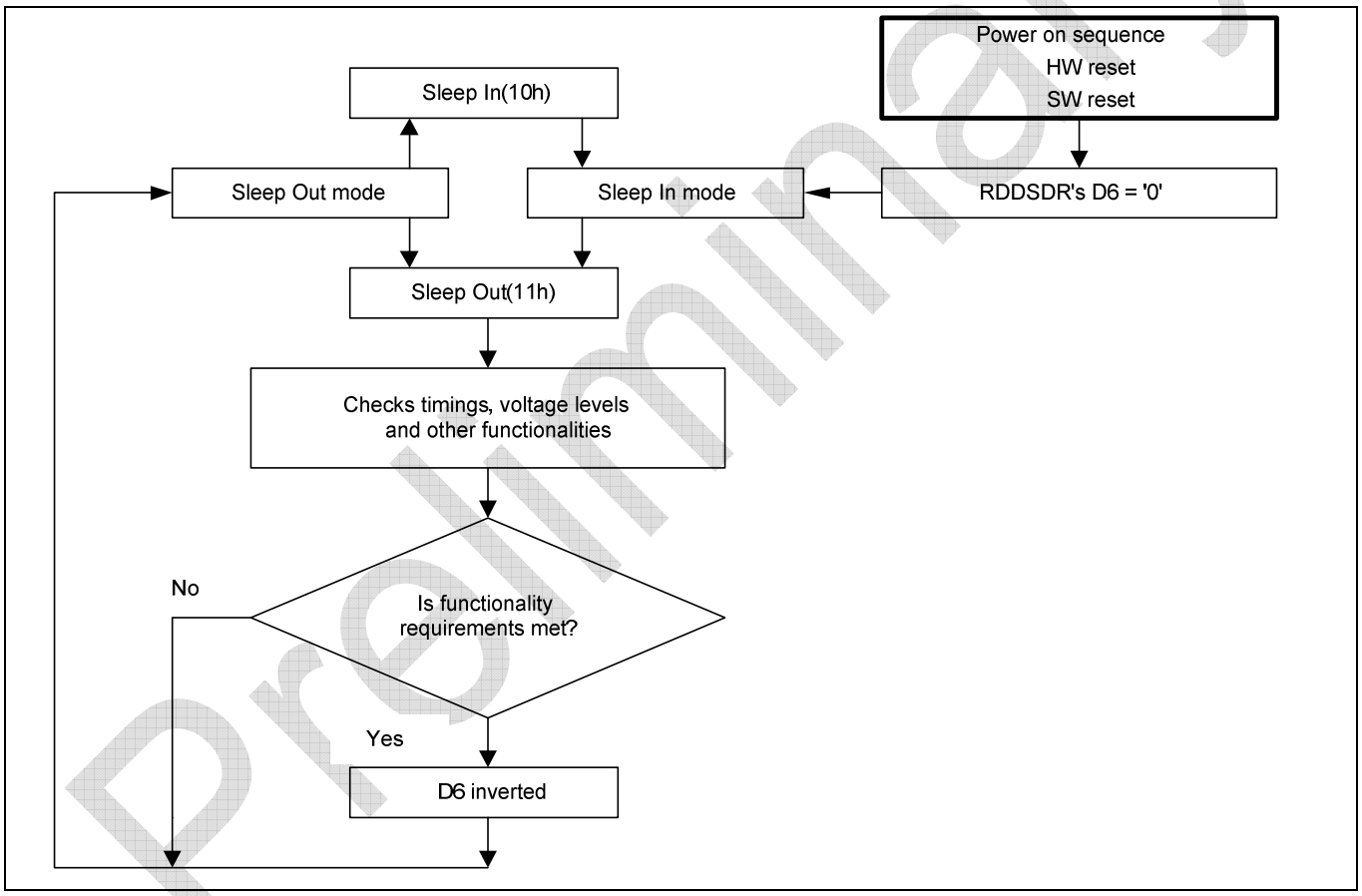

Figure106. Flowchart of Functionality Detection

Note.

There is needed 120msec after Sleep out command, when there is changing from Sleep in mode to Sleep out mode, before there is possible to check if functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep out command is sent in Sleep out mode.

Preliminary

4.7. MIE FUNCTION

S6D04K1 has a special image enhancement function. MIE (Mobile Image Enhancement) reduces power consumption of backlight unit by adaptive enhancement of luminance and contrast. According the brightness enhancement rate of input image, the power reduction of BLU is controlled automatically.'

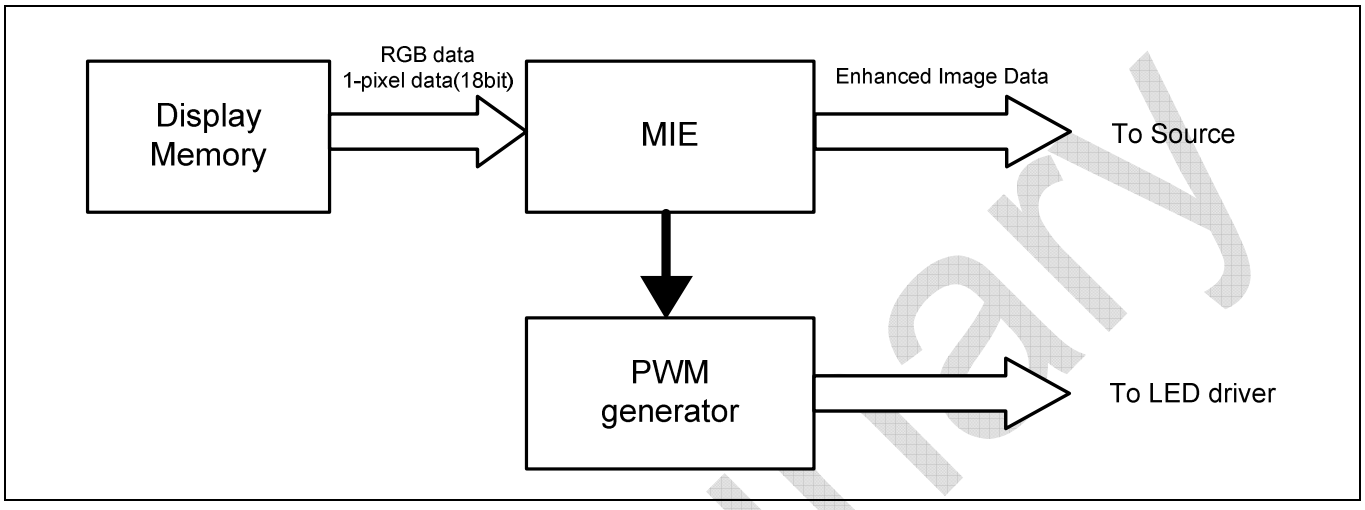

Figure107. Flowchart of MIE Function

When MIE is enabled, MIE dynamically changes the brightness of backlight unit by on-chip PWM Generator. Host can control the rate of BLU power reduction by setting RRC value (Refer to E9h Command.)

When MIE is enabled, the enhanced data is applied after written Display Memory data and in case MIE mode, data transfer shift register method to Source block. Host processor should select movie or still-Image mode (Refer to E9h Command).

*MIE applied, ML = 1'b0. Recommended MIE applied, when ML = 1 'b0.

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4.8. DEEP STANDBY MODE

4.8.1. DEEP STANDBY SEQUENCE

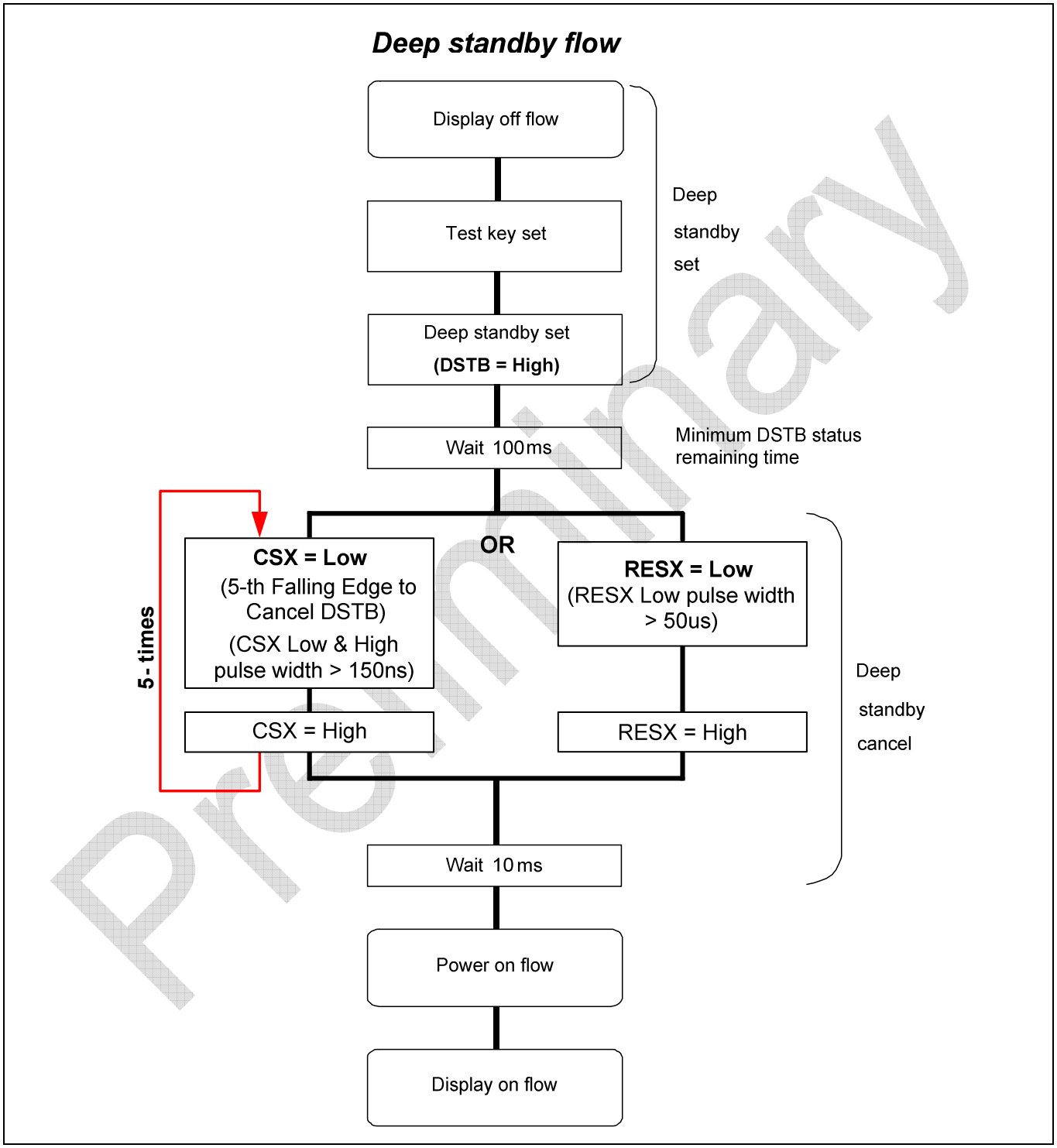

Figure108. Flowchart of Deep Standby Mode

Preliminary

4.8.2. DEEP STANDBY EXIT FLOW

4.8.2.1. Using CSX to wake-up

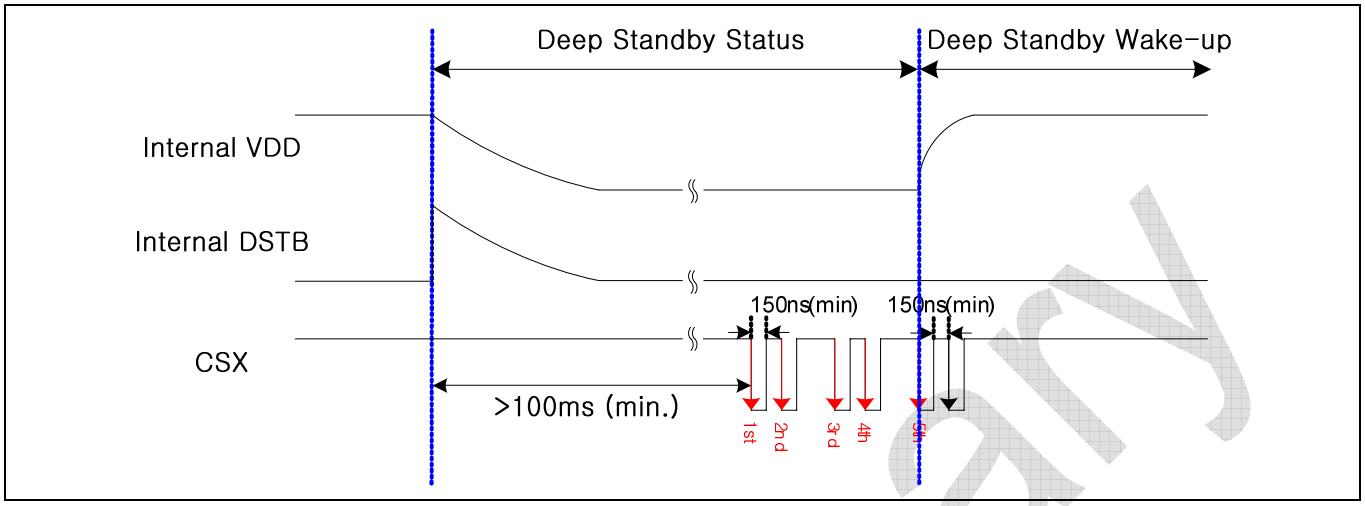

Figure109. Using CSX to Wake-Up

4.8.2.2. Using RESX to wake-up

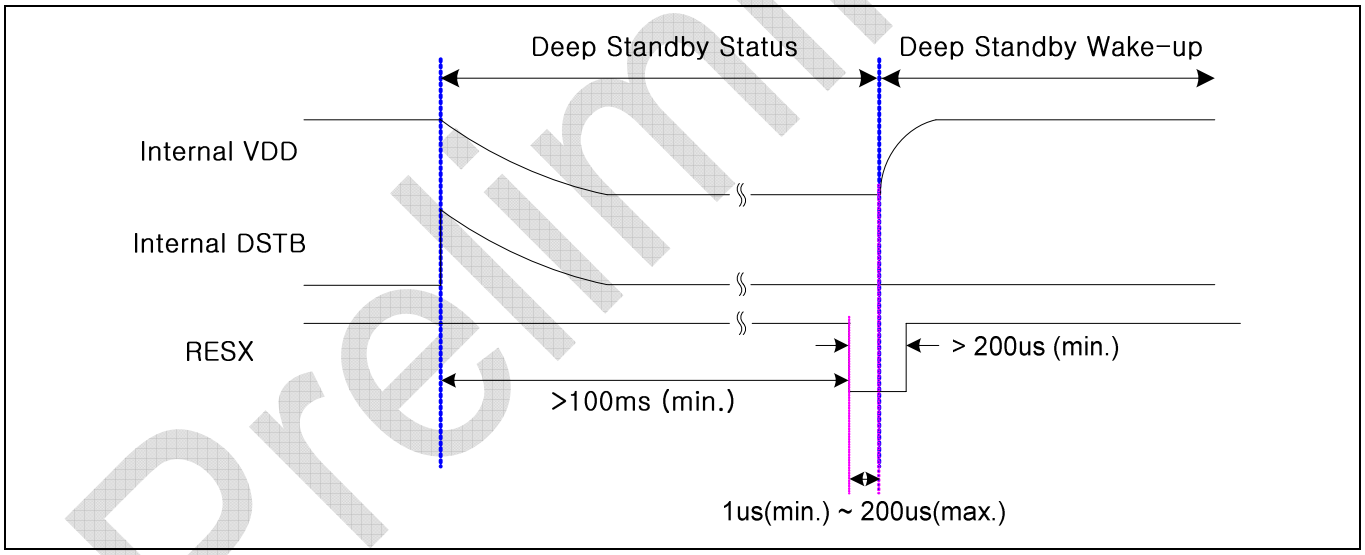

Figure110. Using RESX to Wake-Up

Preliminary

4.8.3. DEEP STANDBY ENTER FLOW

4.8.3.1. During display state

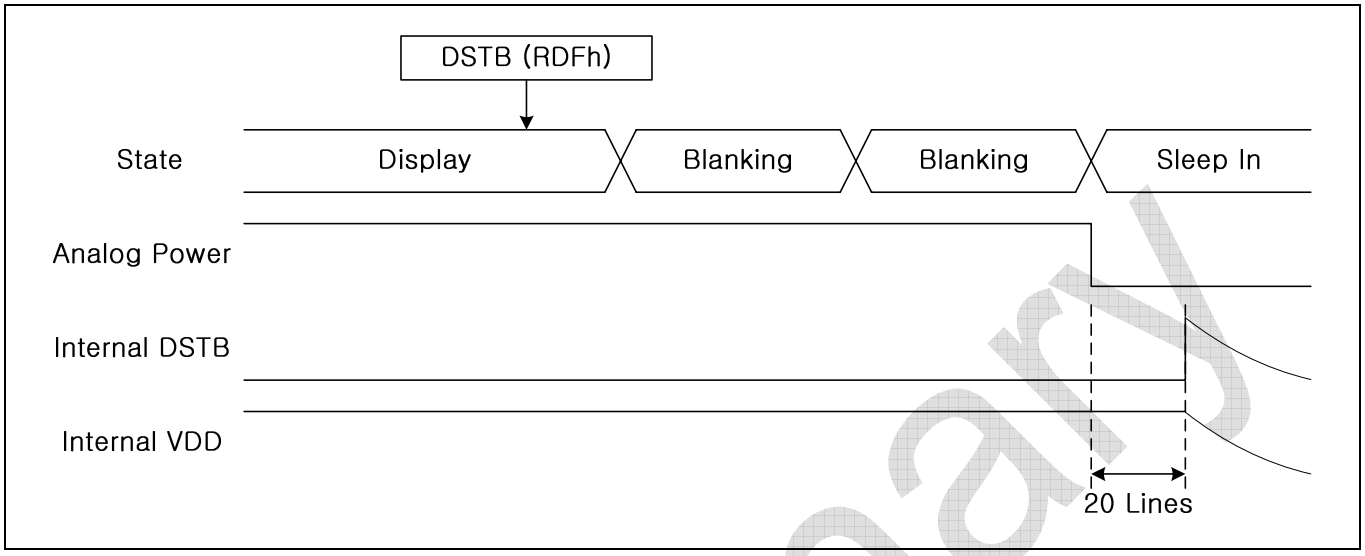

Figure111. DSTB Enter During Display State

4.8.3.2. During sleep in state

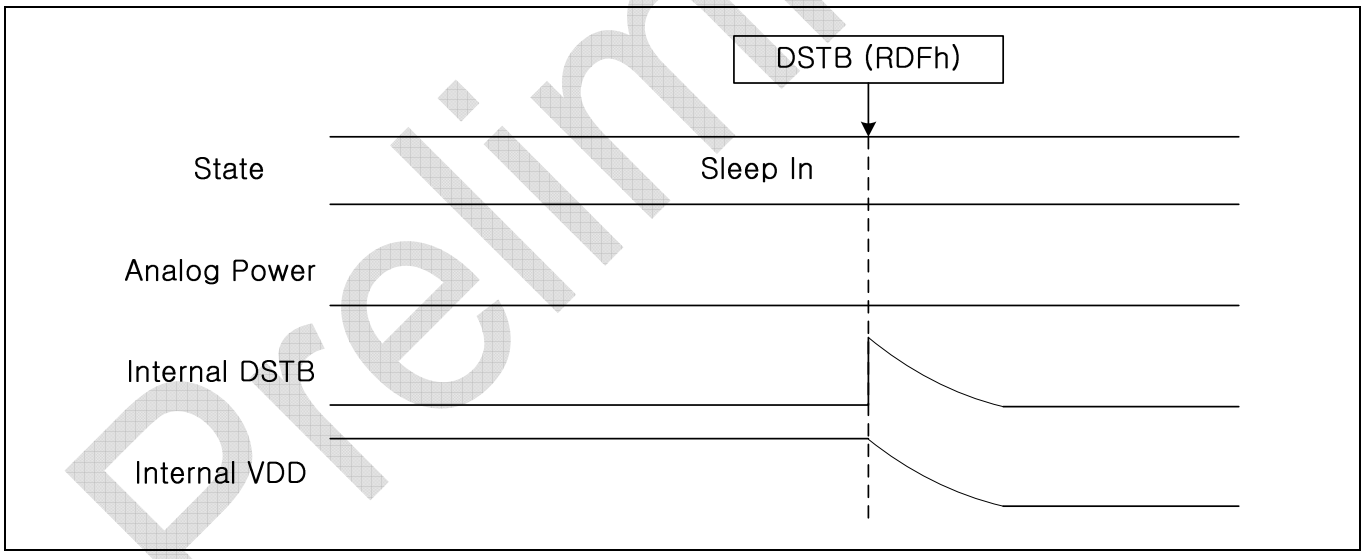

Figure112. DSTB Enter During Sleep in State

Preliminary

4.9. DISPLAY ON/OFF SEQUENCE

4.9.1. DISPLAY ON SEQUENCE

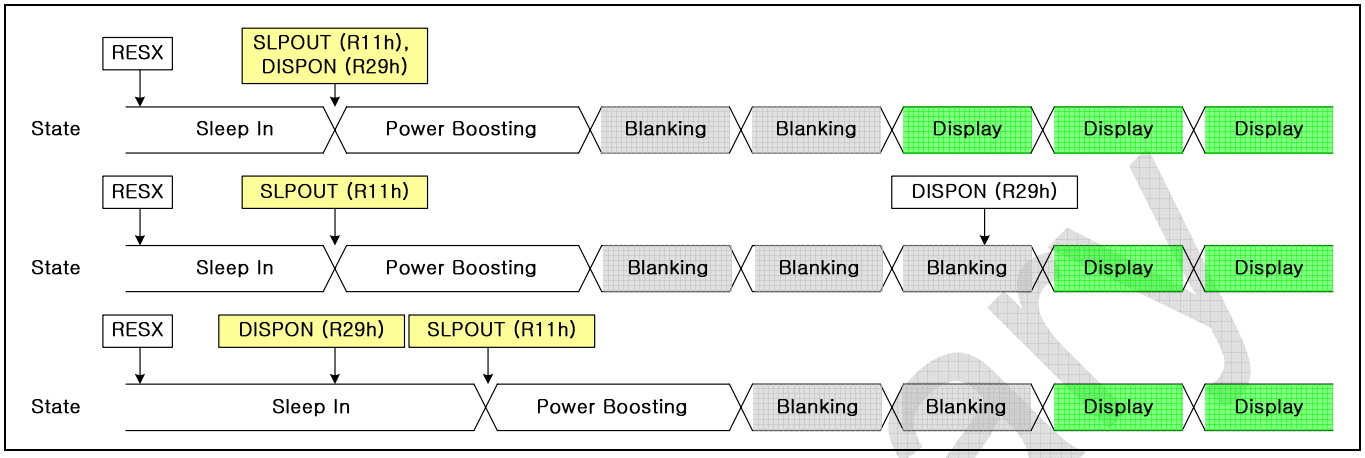

Figure113. Display On Sequence (APON=1)

4.9.2. DISPLAY OFF SEQUENCE

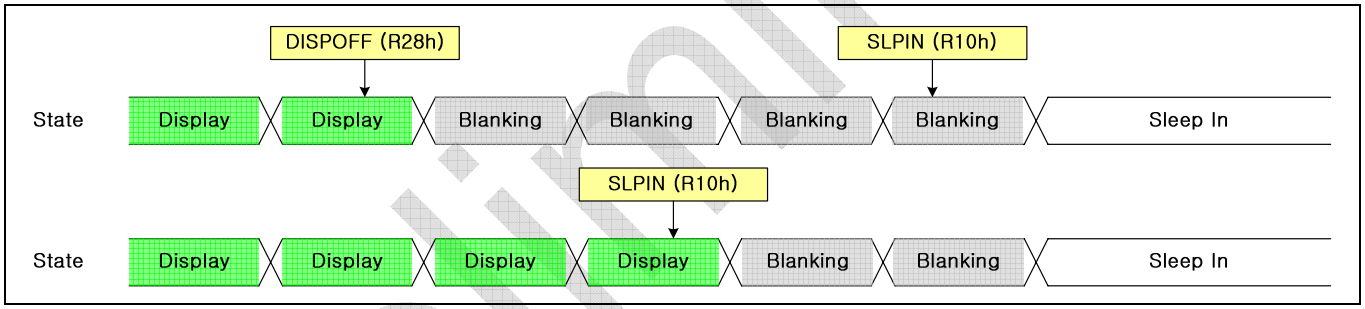

Figure114. Display Off Sequence (APON=1)

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CHAPTER 5

COMMAND

5.1 Description of Level 1 Command
5.2 Description of Level 2 Command

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5. COMMAND

5.1. DESCRIPTION OF LEVEL 1 COMMAND

Table 72. List of Level 1 Command

Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
00	No Operation	C	0	-
01	Software Reset	C	0	-
04	Read Display Identification Information	R	4	
09	Read Display Status	R	5	
0A	Read Display Power Mode	R	2	
0B	Read Display MADCTL	R	2	
0C	Read Display Pixel Format	R	2	
0D	Read Display Image Mode	R	2	
0E	Read Display Signal Mode	R	2	
0F	Read Display Self Diagnostic Result	R	2	
10	Sleep In	C	0	-
11	Sleep Out	C	0	-
12	Partial Mode On	C	0	-
13	Normal Display Mode On	C	0	-
20	Display Inversion Off	C	0	-
21	Display Inversion On	C	0	-
26	Gamma Set	W	1	format: 1 byte for curve selection
28	Display Off	C	0	-
29	Display On	C	0	-
2A	Column Address Set	W	4	format: 2 byte for leftmost Column counter 2 byte for rightmost Column counter
2B	Page Address Set	W	4	format:

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Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
				2 byte for top line pointer 2 byte for bottom line pointer
2C	Memory Write	W	Any Length	Successive video data stream Format in all color modes
2E	Memory Read	R	Any length	Successive video data stream Format in all color modes.
30	Partial Area	W	4	format: 2 byte for top line pointer 2 byte for bottom line pointer
33	Vertical Scrolling Definition	W	6	format: 2 byte for fixed area top line pointer 2 byte for scrolling area height 2 byte for fixed area bottom line pointer
34	Tearing Effect Line Off	C	0	-
35	Tearing Effect Line On	W	1	1 byte for Tearing Effect Line Mode selection
36	Memory Data Access Control	W	1	1 byte for memory scan direction
37	Vertical Scrolling Start Address	W	2	2 byte for line pointer
38	Idle Mode Off	C	0	-
39	Idle Mode On	C	0	-
3A	Interface Pixel format	W	1	Refer to Section 5.1.33
3C	Memory Write Continue	W	Any length	
3E	Memory Read Continue	R	Any length	
44	Set Tear Scanline	W	2	format: 2 byte for TE signal turns on when the display module reaches line N.
45	Get Scanline	R	2	
51	Write Manual Brightness	W	1	MAN_BRIGHT[7:0]
52	Read Display Brightness	R	2	DISP_BRIGHT[7:0]
53	Write BL Control	W	1	BCTRL, DD, BL
54	Read BL Control	R	2	BCTRL, DD, BL
55	Write MIE Mode	W	1	MIE_MODE[1:0]
56	Read MIE Mode	R	1	MIE_MODE[1:0]

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Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
5E	Write Minimum Brightness	W	1	MIN_BRIGHT[7:0]
5F	Read Minimum Brightness	R	1	MIN_BRIGHT[7:0]
A1	Read DDB Start	R	Any lenth	
A8	Read DDB Continue	R	Any lenth	
DA	Read ID1	R	2	
DB	Read ID2	R	2	
DC	Read ID3	R	2	

Note.

1. Undefined commands are treated as NOP (00h) command.
2. B0h to D9h and DEh to FFh are for factory (= display supplier) use. These commands are treated as NOP (00h) commands after shipping to factory. Default value is NOP (00h).
3. Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-sync when Module is in Sleep Out mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

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5.1.1. NO OPERATION (00H)

00H	NOP (No Operation)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER											
Description	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.											
Restriction												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

Preliminary

5.1.2. SOFTWARE RESET (01H)

01H	SWRESET (Software Reset)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER											
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command.											
Restriction	It will be necessary to wait 5 msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5 msec. If Software Reset is applied during Sleep out mode, it will be necessary to wait 120 msec before sending Sleep out command. Software Reset command cannot be sent during Sleep out sequence.											
Register Availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

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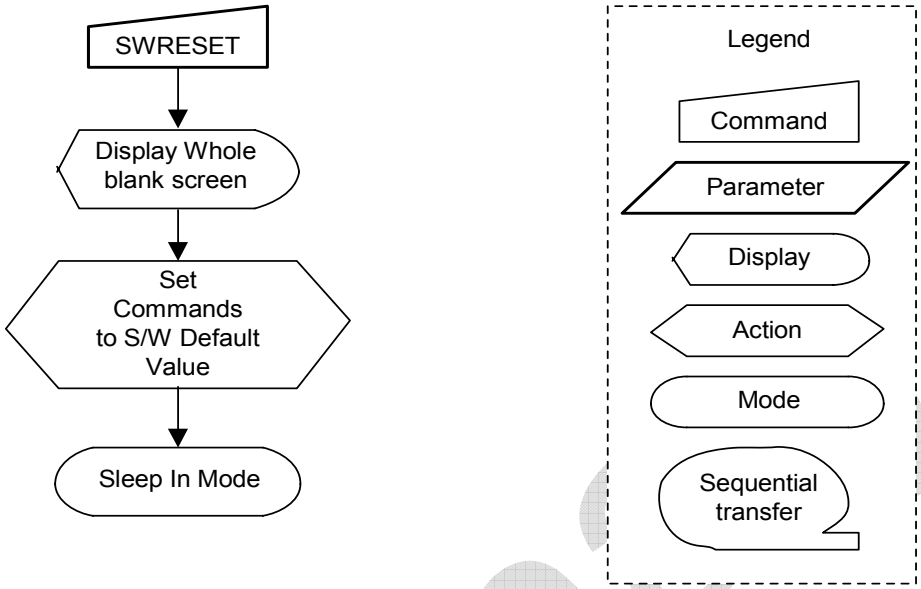
01H	SWRESET (Software Reset)
Flow Chart	

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5.1.3. READ DISPLAY IDENTIFICATION INFORMATION (04H)

04H	RDDIDIF (Read Display Identification Information)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	1	0	0	04
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd para	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th para	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

Description

This read byte returns 24-bits display identification information.

The 1st Parameter is dummy data.

The 2nd Parameter (ID17 to ID10): LCD module's manufacture ID.

The 3rd Parameter (ID27 to ID20): LCD module / driver version ID.

The 4th Parameter (ID37 to ID30): LCD module / driver.

Note: Commands RDID1 / RDID2 / RDID3 (DAh, DBh and DCh) read data correspond to the parameter 2, 3, 4 of the command 04h, respectively.

Restriction

Register Availability

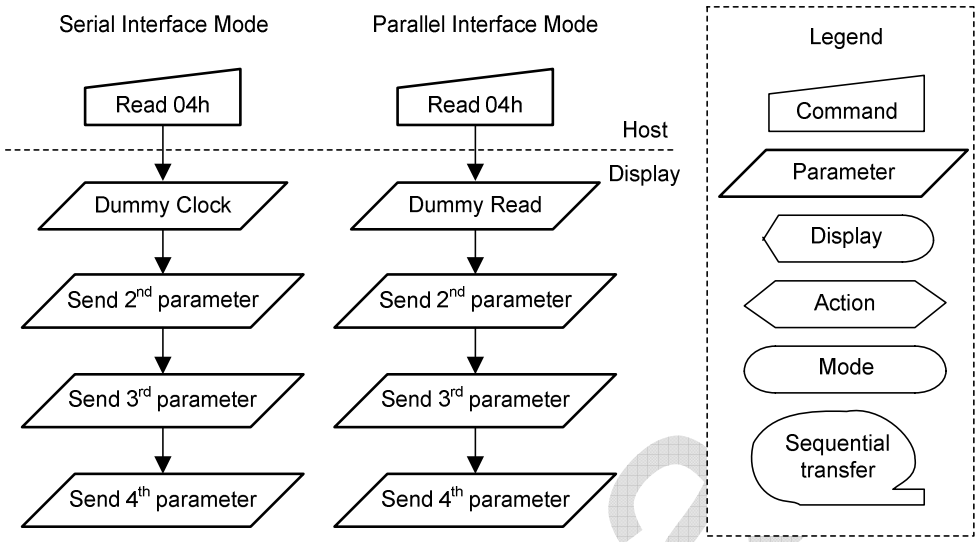
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

ID1, ID2 and ID3 default value

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	00h	00h	00h
S/W Reset	00h	00h	00h
H/W Reset	00h	00h	00h

Preliminary

04H	RDDIDIF (Read Display Identification Information)
Flow Chart	

Preliminary

5.1.4. READ DISPLAY STATUS (09H)

09H	RDDST (Read Display Status)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	0	1	09
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D31	D30	D29	D28	D27	D26	0	0	xx
3rd para	1	↑	1	0	D22	D21	D20	D19	D18	D17	D16	xx
4th para	1	↑	1	D15	0	D13	0	0	D10	D9	D8	xx
5th para	1	↑	1	D7	D6	D5	0	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

The 1st Parameter is dummy data.

Bit	Description	Comment
D31	Step up circuit Voltage Status	
D30	Page Address Order	
D29	Column Address Order	
D28	Page/Column Order	
D27	Vertical Order	
D26	RGB/BGR Order	
D25	Not used	Set to ‘0’
D24	Not used	Set to ‘0’
D23	Not used	Set to ‘0’
D22	Interface Color Pixel Format Definition	
D21		
D20		
D19	Idle Mode On/Off	
D18	Partial Mode On/Off	
D17	Sleep In/Out	
D16	Display Normal Mode On/Off	
D15	Vertical Scroll Mode On/Off	
D14	Not used	Set to ‘0’
D13	Inversion Status	
D12	Not used	Set to ‘0’
D11	Not used	Set to ‘0’
D10	Display On/Off	

Preliminary

09H	RDDST (Read Display Status)		
	D9	Tearing Effect Line On/Off	
	D8	Gamma Curve Selection	
	D7		
	D6		
	D5	Tearing Effect Output Line Mode	
	D4	Not used	Set to ‘0’
	D3	Not used	Set to ‘0’
	D2	Not used	Set to ‘0’
	D1	Not used	Set to ‘0’
	D0	Not used	Set to ‘0’

Bit Values are explained overleaf.

D31: Step up circuit Voltage status.

”0”: Step up circuit Off or has a fault.

”1”: Step up circuit On and working OK.

D30: Page Address Order.

“0”: Top to Bottom (When MADCTL B7 = ‘0’).

“1”: Bottom to Top (When MADCTL B7 = ‘1’).

D29: Column Address Order.

“0”: Left to Right (When MADCTL B6 = ‘0’).

“1”: Right to Left (When MADCTL B6 = ‘1’).

D28: Page/Column Order.

“0”: Normal Mode (When MADCTL B5 = ‘0’).

“1”: Reverse Mode (When MADCTL B5 = ‘1’).

D27: Line Address Order

“0”: LCD Refresh Top to Bottom (When MADCTL B4 = ‘0’).

“1”: LCD Refresh Bottom to Top (When MADCTL B4 = ‘1’).

D26: RGB/BGR Order

“0”: RGB (When MADCTL B3 = ‘0’).

“1”: BGR (When MADCTL B3 = ‘1’).

D25: Set to “0”

D24: Set to “0”

D23: Set to “0”

D22, D21, D20: Interface Color Pixel Format Definition.

D19: Idle Mode On/Off

Preliminary

09H	RDDST (Read Display Status)

"0": Idle Mode Off.

"1" : Idle Mode On.

D18: Partial Mode On/Off

"0": Partial Mode Off.

"1" : Partial Mode On.

D17: Sleep In/Out

"0": Sleep In Mode.

"1": S0leep Out Mode.

D16: Display Normal Mode

"0": Display Normal Mode Off.

"1": Display Normal Mode On.

D15: Vertical Scroll Mode

"0": Vertical Scroll Mode Off.

"1": Vertical Scroll Mode On.

D14: Set to "0"

D13: Inversion Status

"0": Inversion is Off.

"1": Inversion is On.

D12: Set to "0"

D11: Set to "0"

D10: Display On/Off

"0": Display is Off.

"1": Display is On.

D9: Tearing Effect Line On/Off

"0": Tearing Effect Line Off.

"1": Tearing Effect Line On.

D8, D7, D6: Gamma Curve Selection

Gamma Curve Selected	D8	D7	D6	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	-	-	Not Defined

Preliminary

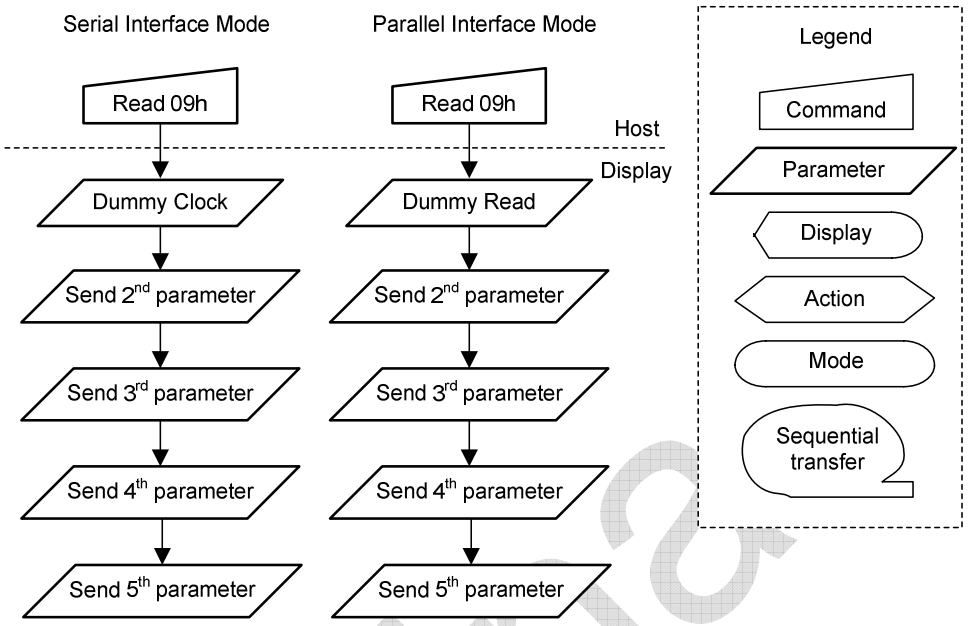
09H	RDDST (Read Display Status)
	D5: Tearing Effect Line Output Mode "0": TE Mode1. "1": TE Mode2. D4: Set to "0" D3: Set to "0" D2: Set to "0" D1: Set to "0" D0: Set to "0"
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	0000 0000_0110 0001_0000 0000_0000 0000
S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000
H/W Reset	0000 0000_0110 0001_0000 0000_0000 0000

Preliminary

09H	RDDST (Read Display Status)
Flow Chart	

Preliminary

5.1.5. READ DISPLAY POWER MODE (0AH)

0AH	RDDPM (Read Display Power Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	1	0	0A
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Step up circuit Voltage Status	
D6	Idle Mode On/Off	
D5	Partial Mode On/Off	
D4	Sleep In/Out	
D3	Display Normal Mode On/Off	
D2	Display On/Off	
D1	-	Set to ‘0’
D0	-	Set to ‘0’

Bit D7 : Step up circuit Voltage Status

“0”: Step up circuit Off or has a fault.

“1”: Step up circuit On and working OK (Meets optical requirements).

Bit D6 : Idle Mode On/Off

“0”: Idle Mode Off.

“1” : Idle Mode On.

Bit D5 : Partial Mode On/Off

“0”: Partial Mode Off.

“1”: Partial Mode On.

Bit D4 : Sleep In/Out

“0”: Sleep In Mode.

“1”: Sleep Out Mode.

Bit D3 : Display Normal Mode On/Off

“0”: Display Normal Mode Off.

“1”: Display Normal Mode On.

Bit D2 : Display On/Off

“0”: Display Off.

“1”: Display On.

Preliminary

0AH	RDDPM (Read Display Power Mode)
	Bit D1, D0 : Set to '0'
Restrictions	

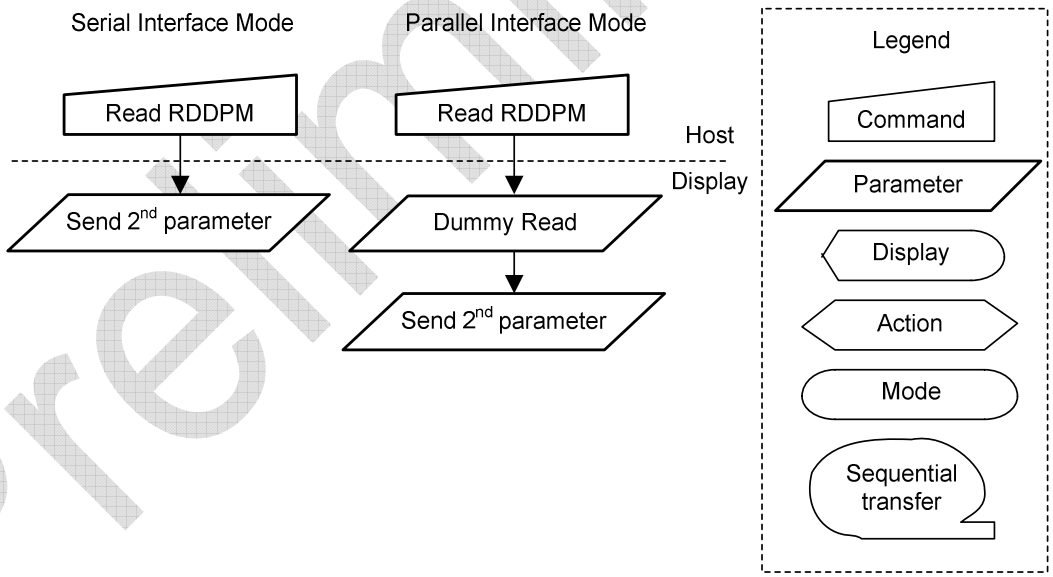
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	08HEX
S/W Reset	08HEX
H/W Reset	08HEX

Flow Chart



Preliminary

5.1.6. READ DISPLAY MADCTL (0BH)

0BH	RDDMADCTL (Read Display MADCTL)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	1	1	0B
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D7	D6	D5	D4	D3	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	
D6	Column Address Order	
D5	Page/Column Order	
D4	Line Address Order	
D3	RGB/BGR Order	
D2	-	Set to ‘0’
D1	-	Set to ‘0’
D0	-	Set to ‘0’

Bit D7 : Page Address Order

“0”: Top to Bottom (When MADCTL B7=’0’).

“1”: Bottom to Top (When MADCTL B7=’1’).

Bit D6 : Column Address Order

“0”: Left to Right (When MADCTL B6=’0’).

“1”: Right to Left (when MADCTL B6=’1’).

Bit D5 : Page/column Order

“0”: Normal Mode (When MADCTL B5=’0’).

“1”: Reverse Mode (When MADCTL B5=’1’)

Bit D4 : Line Address Order

“0”: LCD Refresh Top to Bottom (When MADCTL B4=’0’).

“1”: LCD Refresh Bottom to Top (When MADCTL B4=’1’).

Bit D3 : RGB/BGR Order

“0”: RGB (When MADCTL B3=’0’).

“1”: BGR (When MADCTL B3=’1’).

Bit D2, D1, D0 : Set to ‘0’

Restrictions

Preliminary

0BH	RDDMADCTL (Read Display MADCTL)

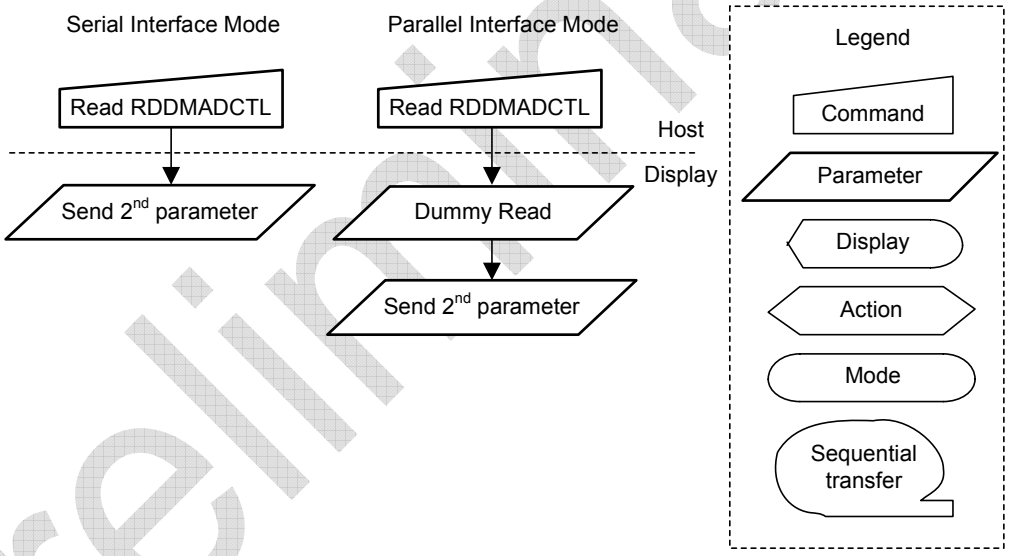
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00HEX
S/W Reset	No Change
H/W Reset	00HEX

Flow Chart



Preliminary

5.1.7. READ DISPLAY PIXEL FORMAT (0CH)

0CH	RDDCOLMOD (Read Display COLMOD)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	0	0	0C
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	0	D6	D5	D4	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	-	"0" (Not used)
D6	RGB Interface Color Format	"101"=16 bit/pixel "110"=18 bit/pixel
D5		
D4		
D3	-	"0" (Not used)
D2	Control Interface Color Format	"101"=16 bit/pixel "110"=18 bit/pixel
D1		
D0		

Restrictions

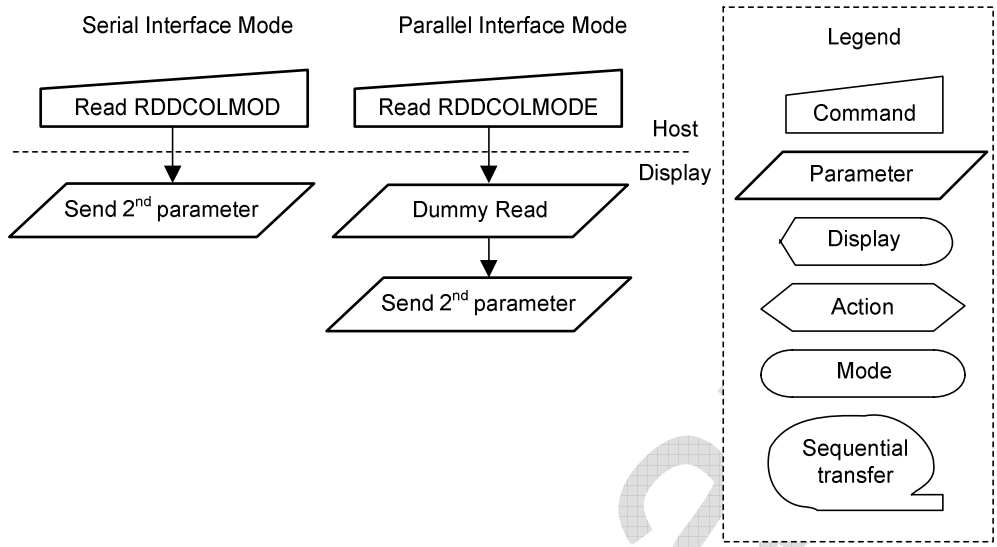
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	0000_0110 (18 bit/pixel)
S/W Reset	No change
H/W Reset	0000_0110 (18 bit/pixel)

Preliminary

0CH	RDDCOLMOD (Read Display COLMOD)
Flow Chart	

Preliminary

5.1.8. READ DISPLAY IMAGE MODE (0DH)

0DH	RDDIM (Read Display Image Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	0	1	0D
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D7	0	D5	0	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit D7 : Vertical Scroll Mode On/Off

"0": Vertical Scroll Mode Off.

"1": Vertical Scroll Mode On.

Bit D6 : Set to '0'

Bit D5 : Inversion On/Off

"0": Inversion Off.

"1": Inversion On.

Bit D4 : Set to '0'

Bit D3 : Set to '0'

Bit D2, D1, D0 : Gamma Curve Selection

Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Restrictions

Register Availability

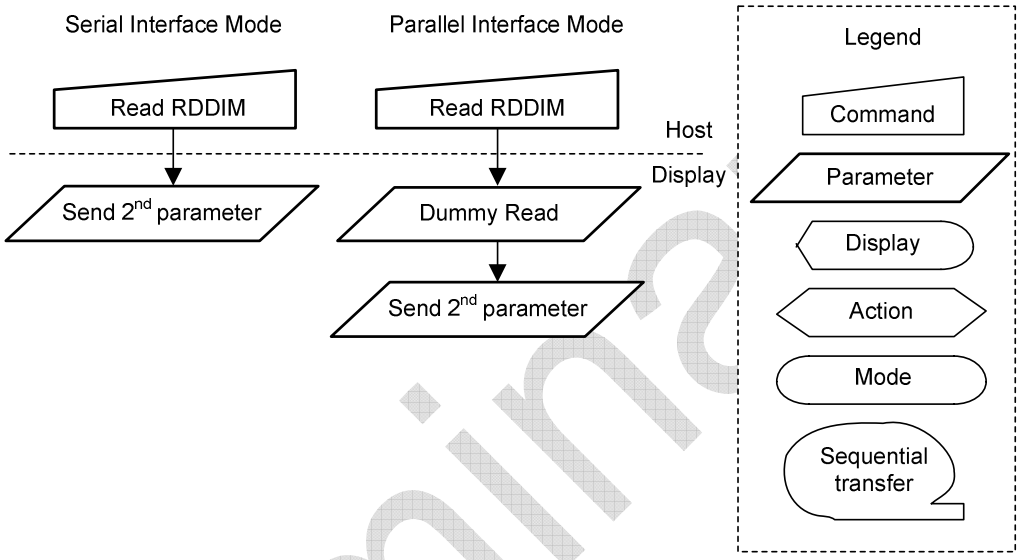
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Preliminary

0DH	RDDIM (Read Display Image Mode)
Default	

Status	Default Value
Power On Sequence	00HEX
S/W Reset	00HEX
H/W Reset	00HEX

Flow Chart



Preliminary

5.1.9. READ DISPLAY SIGNAL MODE (0EH)

0EH	RDDSM (Read Display Signal Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	1	0	0E
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D7	D6	0	0	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit D7 : Tearing Effect Line On/Off.

"0": Tearing Effect Line Off.

"1": Tearing Effect On.

Bit D6 : Tearing Effect Line Output Mode.

"0" : Mode 1.

"1" : Mode 2.

Bit D5 to D0 : Set to '0'

Restrictions

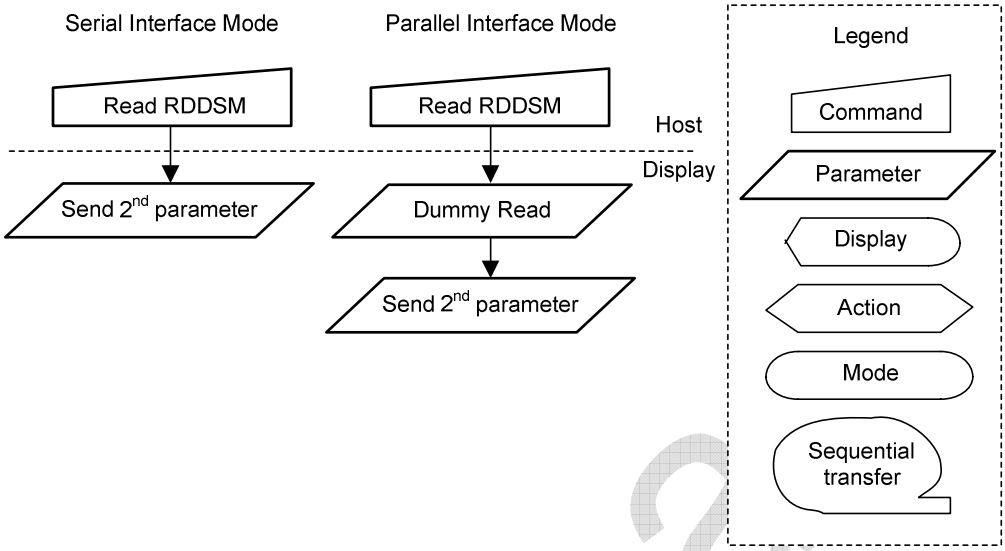
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
S/W Reset	00_{HEX}
H/W Reset	00_{HEX}

Preliminary

0EH	RDDSM (Read Display Signal Mode)
Flow Chart	

Preliminary

5.1.10. READ DISPLAY SELF-DIAGNOSTIC RESULT (0FH)

0FH	RDDSDR (Read Display Self-Diagnostic Result)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	1	1	0F
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D7	D6	0	0	0	0	0	0	xx

Description

This command indicates the status of the display self-diagnostic result after Sleep Out command as described in the table below:

Bit D7 : Register Loading Detection

Bit D6 : Functionality Detection

Bit D5 to D0 : Set to “0”

Restrictions

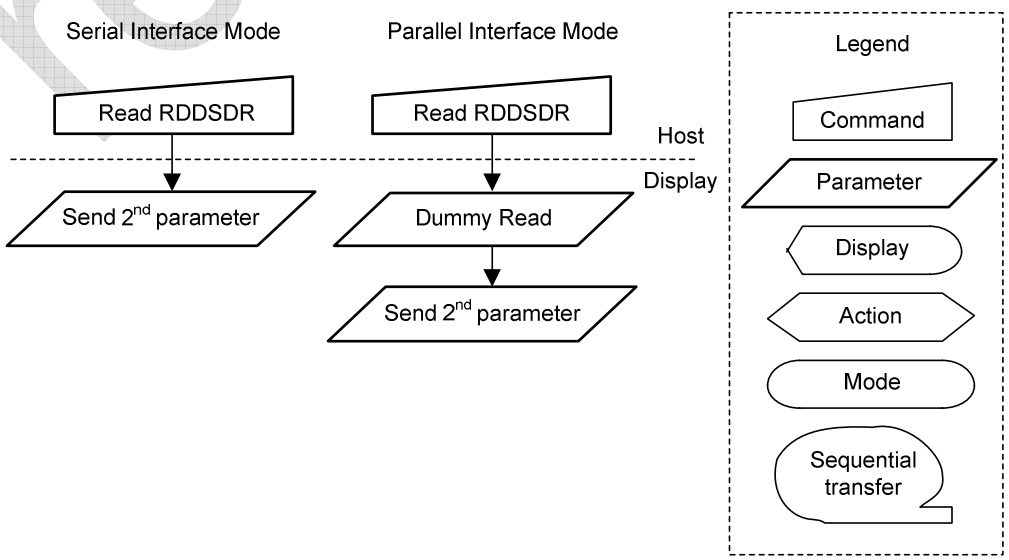
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
S/W Reset	00_{HEX}
H/W Reset	00_{HEX}

Flow Chart



Preliminary

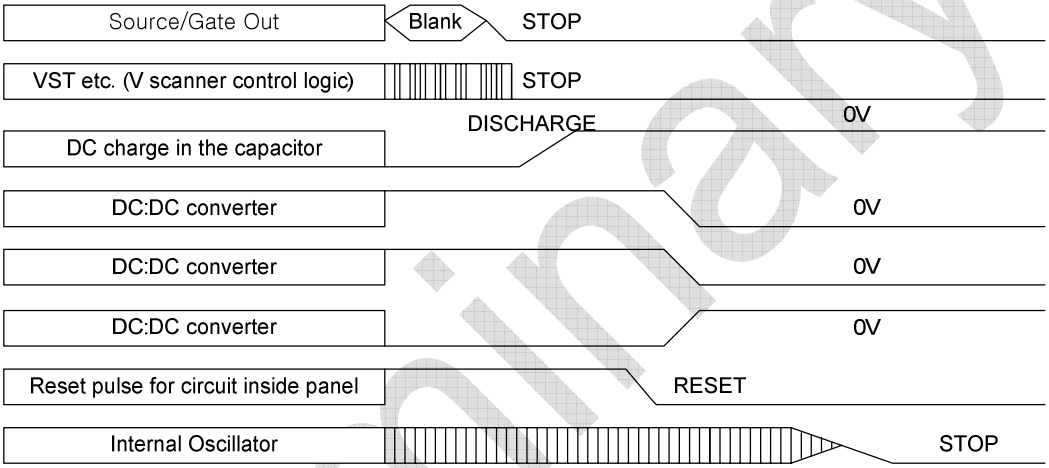
5.1.11. SLEEP IN (10H)

10H	SLPIN (Sleep In)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER											

Description

This command causes the LCD module to enter the minimum power consumption mode.

In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.



MPU interface and memory are still working and the memory keeps its contents.

Restriction

This command has no effect when module is already in Sleep In mode. Sleep In mode can only be left by the Sleep Out command (11h).

It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize.

It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In mode) before Sleep In command can be sent.

Register Availability

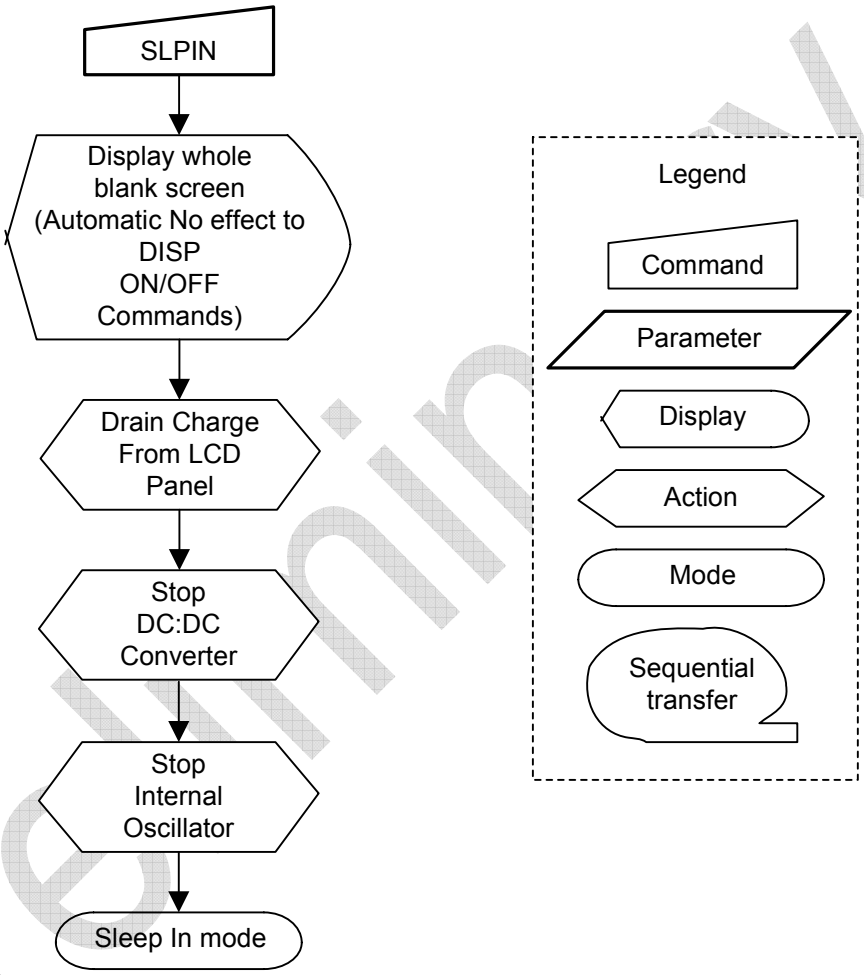
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Preliminary

10H	SLPIN (Sleep In)
Default	

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

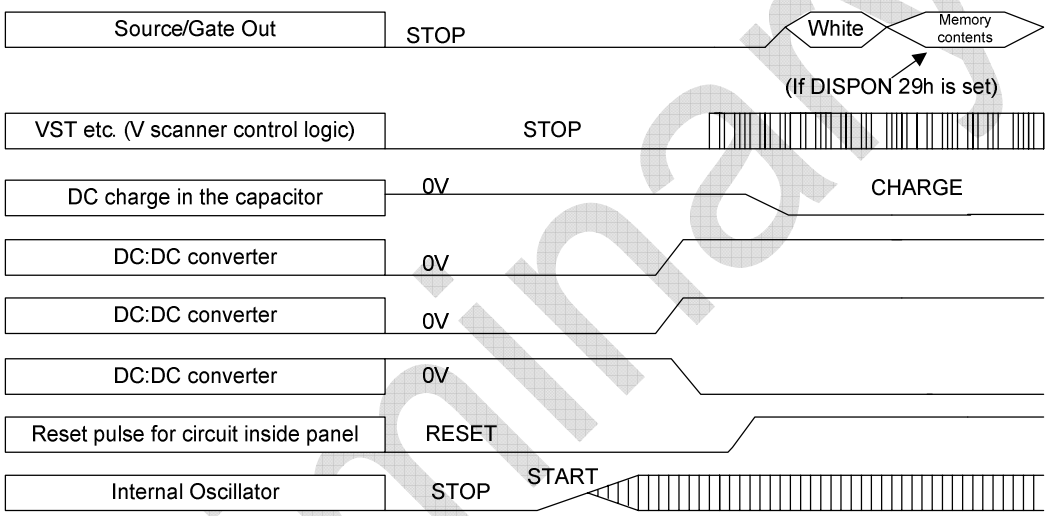
Flow Chart



It takes 120msec to get into Sleep In mode after SLPIN command issued.

Preliminary

5.1.12. SLEEP OUT (11H)

11H	SLPOUT (Sleep Out)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER											
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  											
Restriction	This command has no effect when module is already in Sleep Out mode, Sleep Out Mode can only be left by the Sleep In command (10h) It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done when the display module is already Sleep Out mode. The display module is doing self-diagnostic function during this 5msec. See also section "Sleep Out Command and Self-Diagnostic Functions of the Display Module". It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.											

Preliminary

11H	SLPOUT (Sleep Out)

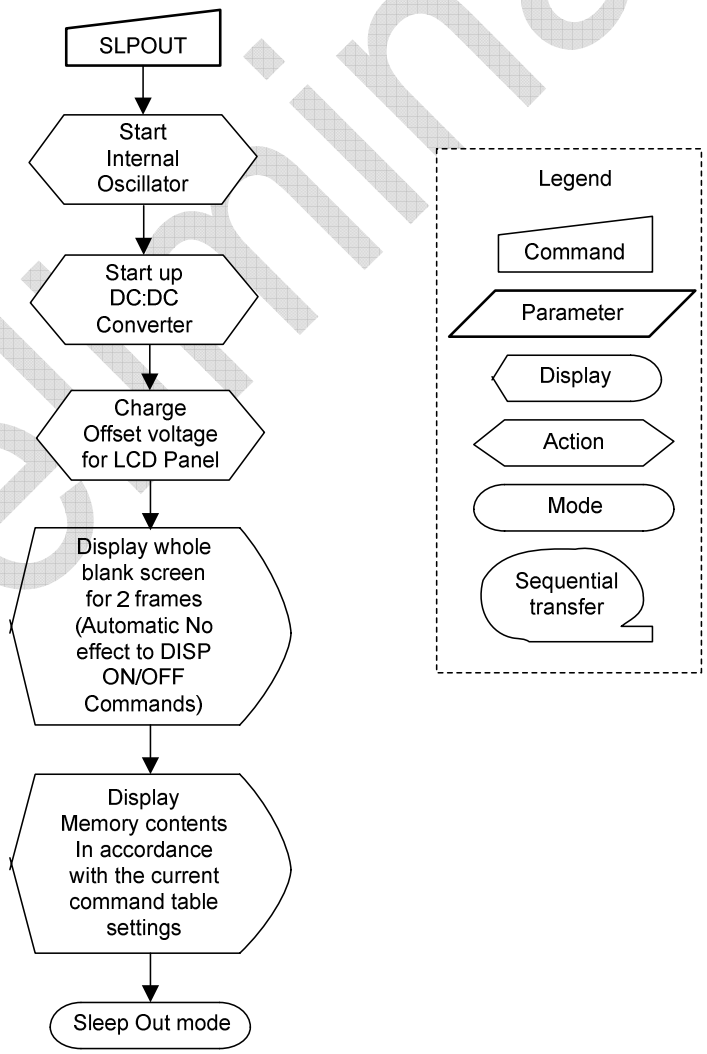
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart



It takes 120msec to become Sleep Out mode after SLPOUT command issued.

Preliminary

5.1.13. PARTIAL MODE ON (12H)

12H	PTLON (Partial Mode On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER											
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30h). To leave Partial mode, the Normal Display Mode command (13h) should be written.											
Restriction	This command has no effect when Partial mode is active.											
Register Availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart: See Partial Area (30h)

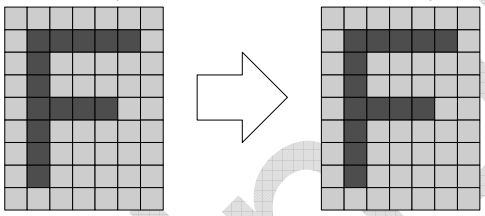
Preliminary

5.1.14. NORMAL DISPLAY MODE ON (13H)

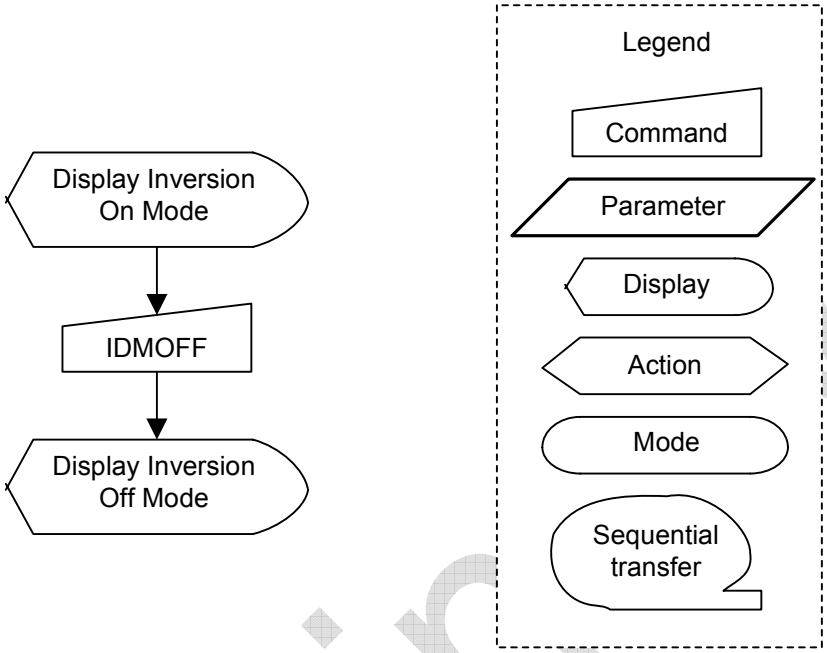
13 H	NORON (Normal Display Mode On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER											
Description	This command returns the display to normal mode. Normal Display Mode On means Partial mode off.											
Restriction	This command has no effect when Normal Display mode is active.											
Register Availability	**Status** / **Availability** Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Step up circuit Off / Yes											
Default	**Status** / **Default Value** Power On Sequence / Normal Mode On S/W Reset / Normal Mode On H/W Reset / Normal Mode On											
Flow Chart	See Partial Area Descriptions for details when use this command											

Preliminary

5.1.15. DISPLAY INVERSION OFF (20H)

20H	INVOFF (Display Inversion Off)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	0	0	0	0	20
Parameter	NO PARAMETER											
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status (Example) Memory → Display 											
Restriction	This command has no effect when module is already in inversion off mode.											
Register Availability	**Status** / **Availability** Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Step up circuit Off: Yes											
Default	**Status** / **Default Value** Power On Sequence: Display Inversion Off S/W Reset: Display Inversion Off H/W Reset: Display Inversion Off											

Preliminary

20H	INVOFF (Display Inversion Off)
Flow Chart	

Preliminary

5.1.16. DISPLAY INVERSION ON (21H)

21H	INVON (Display Inversion On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER											

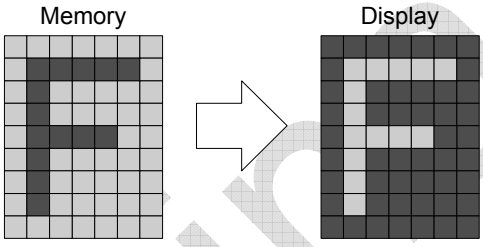
Description

This command is used to enter into display inversion mode.

This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.

This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already in inversion on mode.

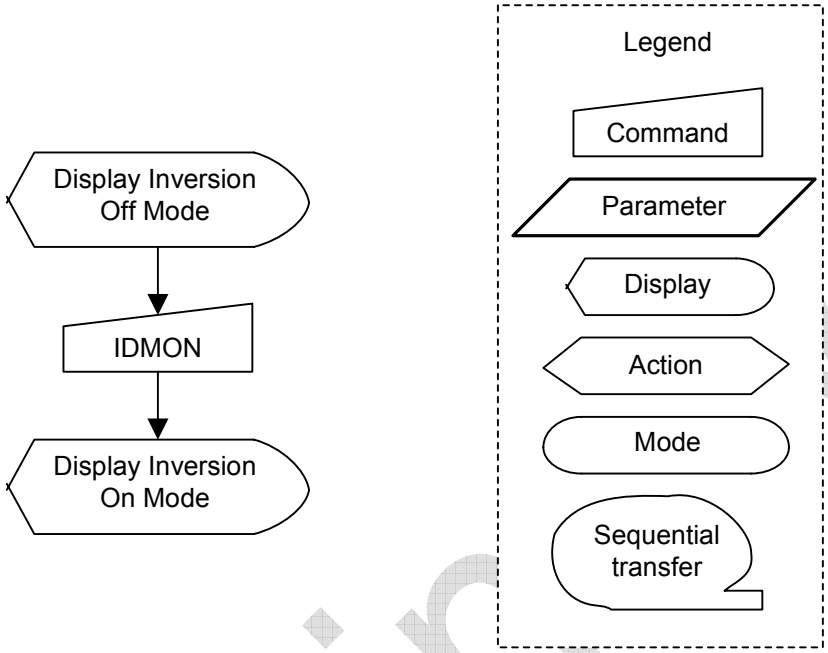
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Preliminary

21H	INVON (Display Inversion On)
Flow Chart	

Preliminary

5.1.17. GAMMA SET (26H)

26H	GAMSET (Gamma Set)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	0	1	1	0	26
Parameter	1	1	↑	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	Note

Description

This command is used to select the desired Gamma curve for the current display.

A maximum of 4 curves can be selected. Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC[7..0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note.

All other values are undefined.

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

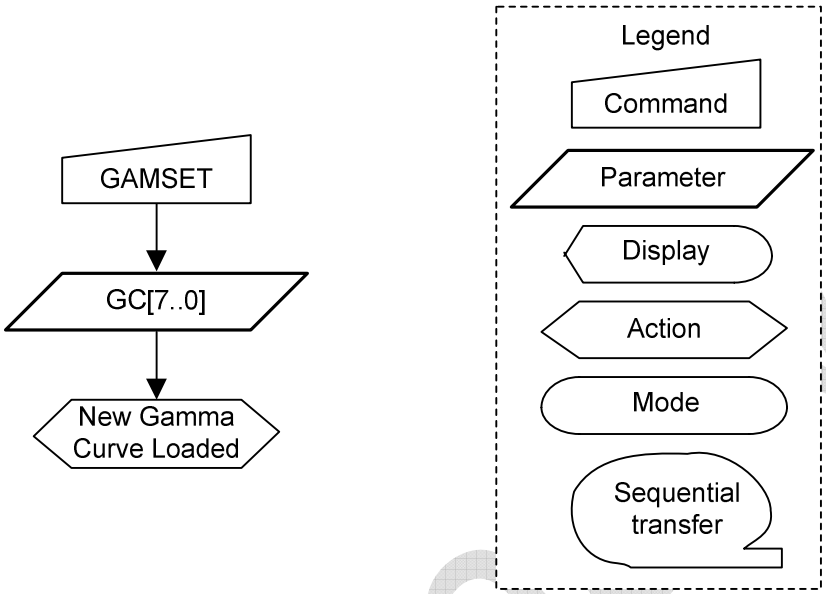
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

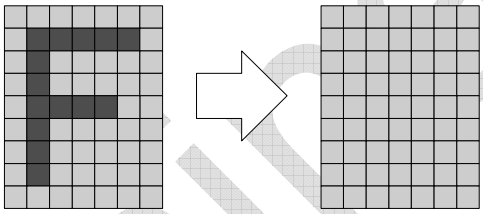
Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Preliminary

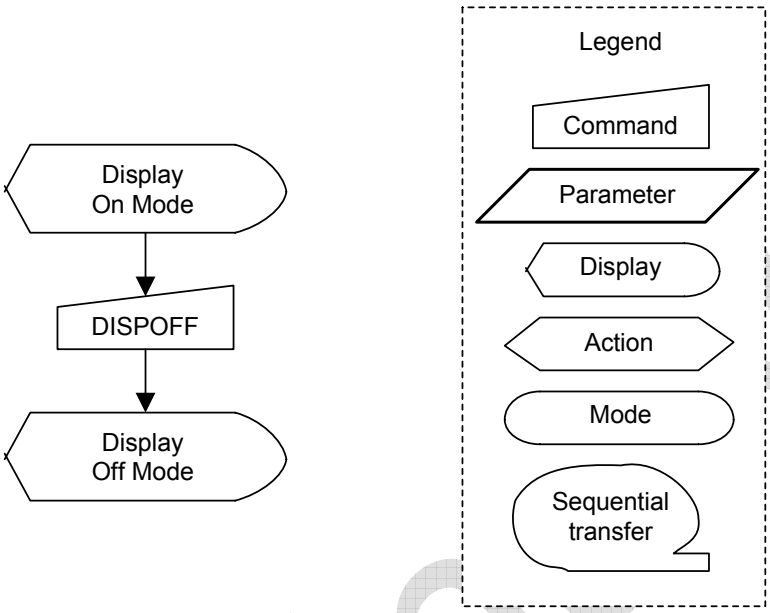
26H	GAMSET (Gamma Set)
Flow Chart	

Preliminary

5.1.18. DISPLAY OFF (28H)

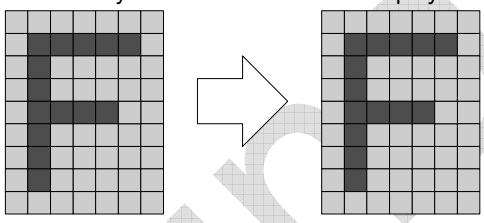
28H	DISPOFF (Display Off)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER											
Description	This command is used to enter into Display Off mode. In this mode, the output from Frame Memory is disabled and blank page is inserted. This command is makes No Change of contents of frame memory This command does not change any other status. There will be no abnormal visible effect on the display (Example) Memory Display 											
Restriction	This command has no effect when module is already in display off mode.											
Register Availability	**Status** / **Availability** Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Step up circuit Off: Yes											
Default	**Status** / **Default Value** Power On Sequence: Display Off S/W Reset: Display Off H/W Reset: Display Off											

Preliminary

28H	DISPOFF (Display Off)
Flow Chart	

Preliminary

5.1.19. DISPLAY ON (29H)

29H	DISPON (Display On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER											
Description	This command is used to recover from Display Off Mode. Output from the Frame Memory is enabled. This command makes No Change of contents of frame memory This command does not change any other status. (Example) Memory Display 											
Restriction	This command has no effect when module is already in display on mode.											

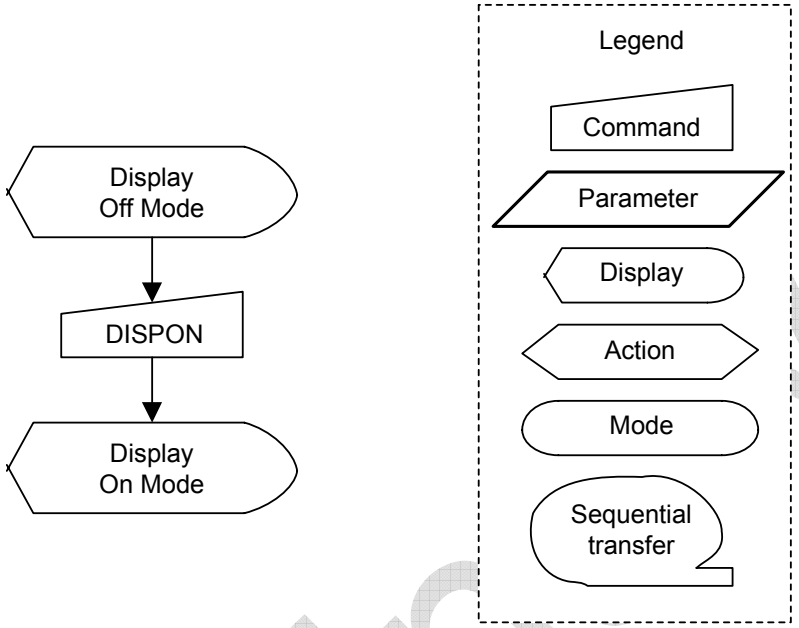
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Preliminary

29H	DISPON (Display On)
Flow Chart	

Preliminary

5.1.20. COLUMN ADDRESS SET (2AH)

2AH	CASET (Column Address Set)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	0	2A
1st para	1	1	↑	SC[15]	SC[14]	SC[13]	SC[12]	SC[11]	SC[10]	SC[9]	SC[8]	Note
2nd para	1	1	↑	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]	
3rd para	1	1	↑	EC[15]	EC[14]	EC[13]	EC[12]	EC[11]	EC[10]	EC[9]	EC[8]	Note
4th para	1	1	↑	EC[7]	EC[6]	EC[5]	EC[4]	EC[3]	EC[2]	EC[1]	EC[0]	

Description

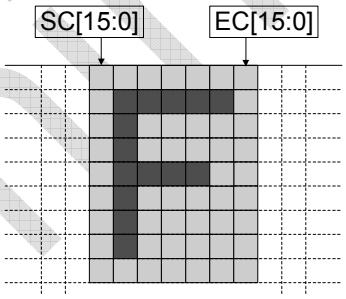
This command is used to define area of frame memory where MPU can access.

This command makes No Change on the other driver status.

The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes.

Each value represents one column line in the Frame Memory.

(Example)



Restriction

SC[15:0] always must be equal to or less than EC[15:0]. When SC[15:0] or EC[15:0] is greater than maximum address as below, data of out of range will be ignored.

Note.

(Parameter range: 0 ≤ SC[15:0], EC[15:0] ≤ 239 (00EFh) (B5=1)

(Parameter range: 0 ≤ SC[15:0], EC[15:0] ≤ 319 (013Fh) (B5=0)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

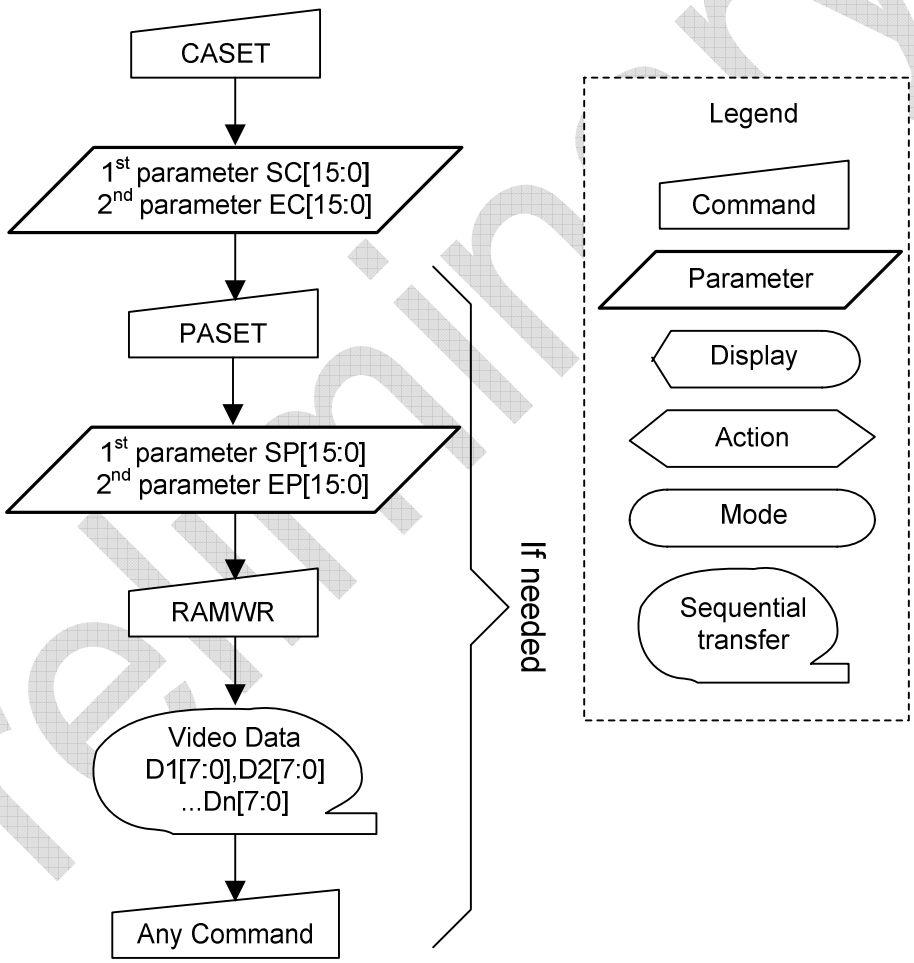
Preliminary

2AH	CASET (Column Address Set)

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000h	EC[15:0]=00EFh
S/W Reset	When MADCTL's B5=0: SC[15:0]=0000h When MADCTL's B5=1: SC[15:0]=0000h	When MADCTL's B5=0: EC[15:0]=0013Fh When MADCTL's B5=1: EC[15:0]=0EFh
H/W Reset	SC[15:0]=0000h	EC[15:0]=013Fh

Flow Chart



Preliminary

5.1.21. PAGE ADDRESS SET (2BH)

2BH	PASET (Page Address Set)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	1	2B
1st para	1	1	↑	SP[15]	SP[14]	SP[13]	SP[12]	SP[11]	SP[10]	SP[9]	SP[8]	Note
2nd para	1	1	↑	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	
3rd para	1	1	↑	EP[15]	EP[14]	EP[13]	EP[12]	EP[11]	EP[10]	EP[9]	EP[8]	Note
4th para	1	1	↑	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	

Description

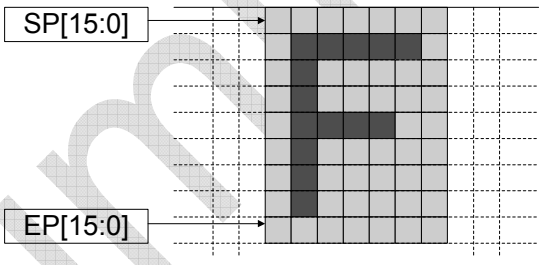
This command is used to define area of frame memory where MPU can access.

This command makes No Change on the other driver status.

The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.

Each value represents one Page line in the Frame Memory.

(Example)



Restriction

SP[15:0] always must be equal to or less than EP[15:0]. When SP[15:0] or EP[15:0] is greater than maximum address as below, data of out of range will be ignored.

Note.

(Parameter range: 0 ≤ SP[15:0], EP[15:0] ≤ 319 (013Fh) (B5=1)

(Parameter range: 0 ≤ SP[15:0], EP[15:0] ≤ 239 (00EFh) (B5=0)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

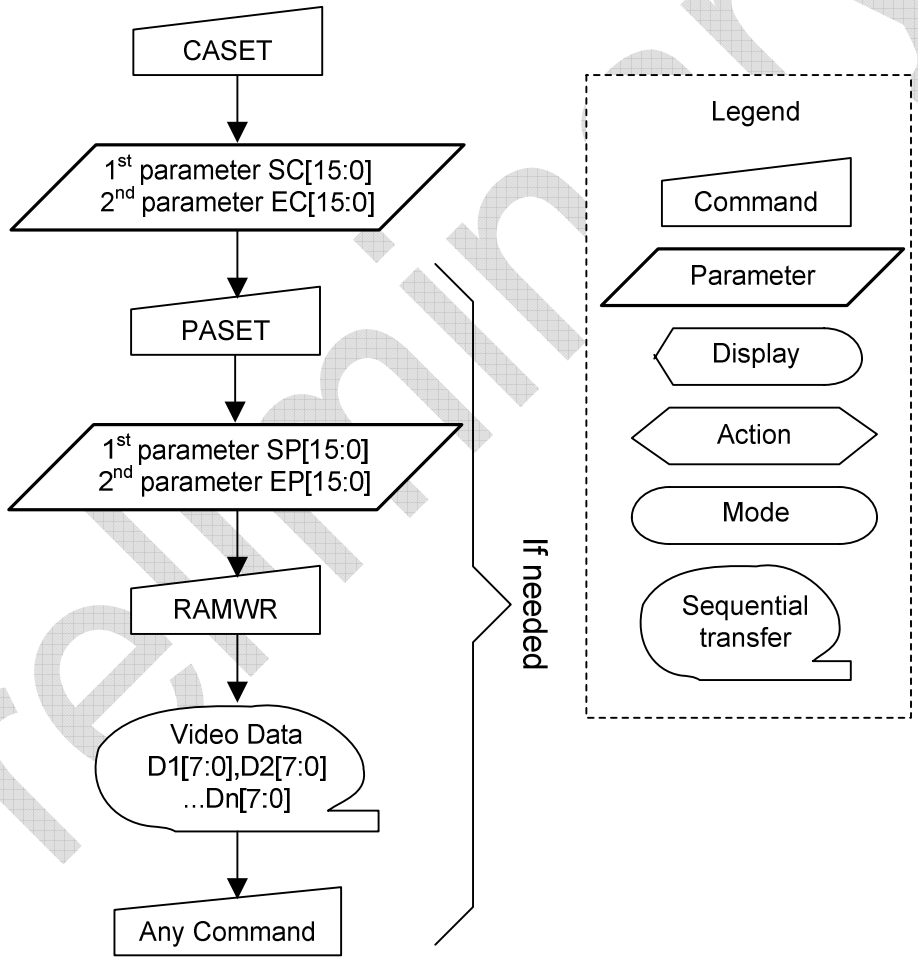
Preliminary

2BH	PASET (Page Address Set)

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000h	EC[15:0]=01AFh
S/W Reset	When MADCTL's B5=0: SC[15:0]=0000h When MADCTL's B5=1: SC[15:0]=0000h	When MADCTL's B5=0: EC[15:0]=00EFh When MADCTL's B5=1: EC[15:0]=013Fh
H/W Reset	SC[15:0]=0000h	EC[15:0]=00EFh

Flow Chart



Preliminary

5.1.22. MEMORY WRITE (2CH)

2CH	RAMWR (Memory Write)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	1	0	0	2C
1st para	1	1	↑	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00..FF
:	1	1	↑	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00..FF
Nth para	1	1	↑	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00..FF

Description

This command is used to transfer data from MPU to frame memory.

This command makes No Change to the other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page position.

The Start Column/Start Page positions are different in accordance with MADCTL setting. Then D[7:0] is stored in frame memory and the column register and the page register incremented.

Sending any other command can stop frame Write.

Restriction

In all color modes, there is no restriction on length of parameters.

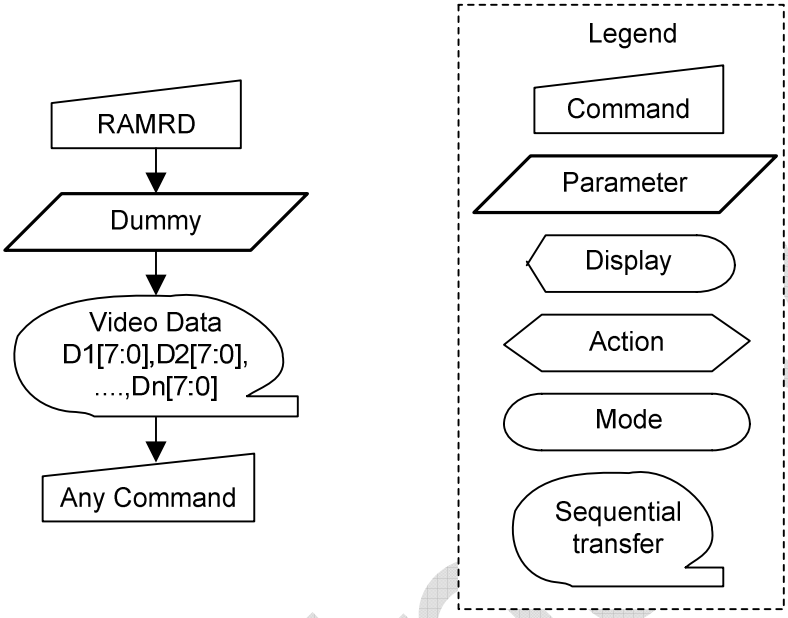
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Preliminary

2CH	RAMWR (Memory Write)
Flow Chart	

Preliminary

5.1.23. MEMORY READ (2EH)

2EH	RAMRD (Memory Read)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	1	1	0	2E
1st para	1	↑	1	X	X	X	X	X	X	X	X	00..FF
:	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00..FF
(N+1)th para	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00..FF

Description

This command is used to transfer data from frame memory to MPU.

This command makes No Change to the other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column / Start Page position.

The Start Column / Start positions are different in accordance with MADCTL setting.

Then D[7:0] is read back from the frame memory and the column register and the page register incremented. Frame memory read can be stopped by sending any other command.

Restriction

In all color modes, the frame memory read is always 18bit, so there is no restriction on length of parameters.

Note.

Frame memory read is only possible via the Parallel Interface.

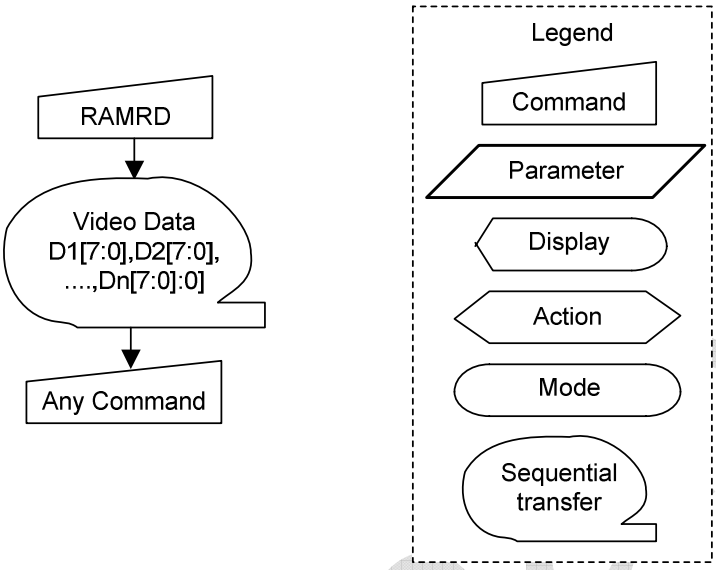
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Preliminary

2EH	RAMRD (Memory Read)
Flow Chart	

Preliminary

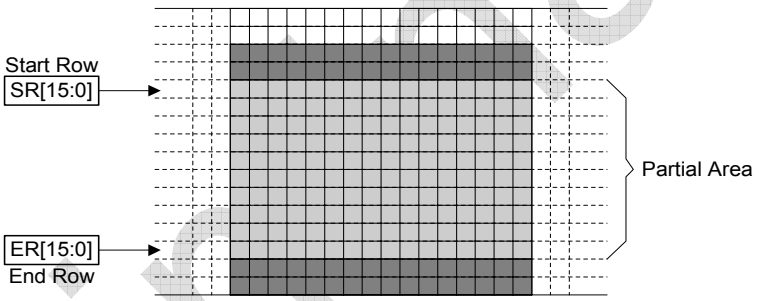
5.1.24. PARTIAL AREA (30H)

30H	PLTAR (Partial Area)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	0	0	30
1st para	1	1	↑	SR[15]	SR[14]	SR[13]	SR[12]	SR[11]	SR[10]	SR[9]	SR[8]	0000..
2nd para	1	1	↑	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	00EF
3rd para	1	1	↑	ER[15]	ER[14]	ER[13]	ER[12]	ER[11]	ER[10]	ER[9]	ER[8]	0000..
4th para	1	1	↑	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	00EF

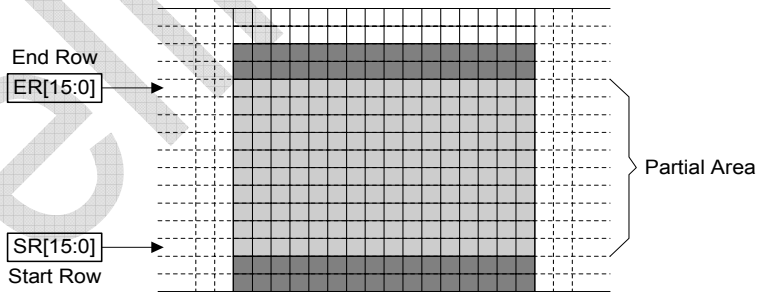
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row(SR) and the second defines the End Row(ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

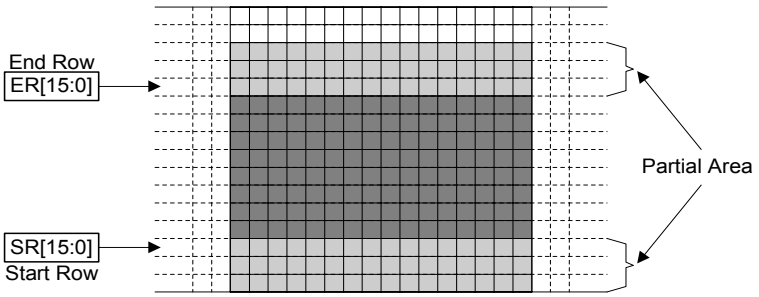
If End Row>Start Row When MADCTL B4=0:



If End Row>Start Row When MADCTL B4=1:



If End Row<Start Row When MADCTL B4=0:



If End Row=Start Row then the Partial Area will be one row deep.

Restriction

Each detail initial values by the display resolution will be updated.

Preliminary

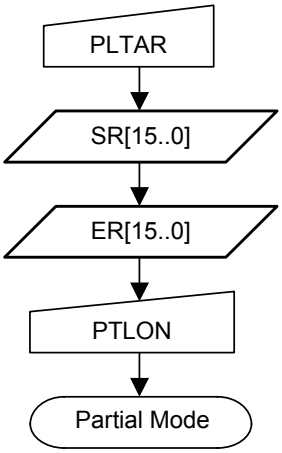
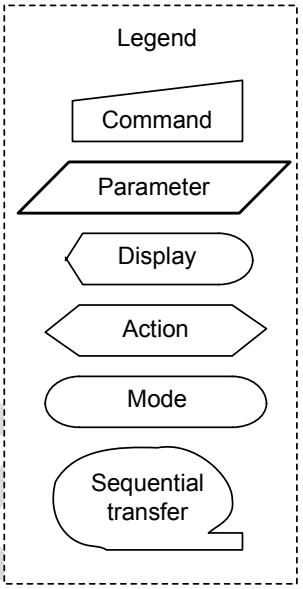
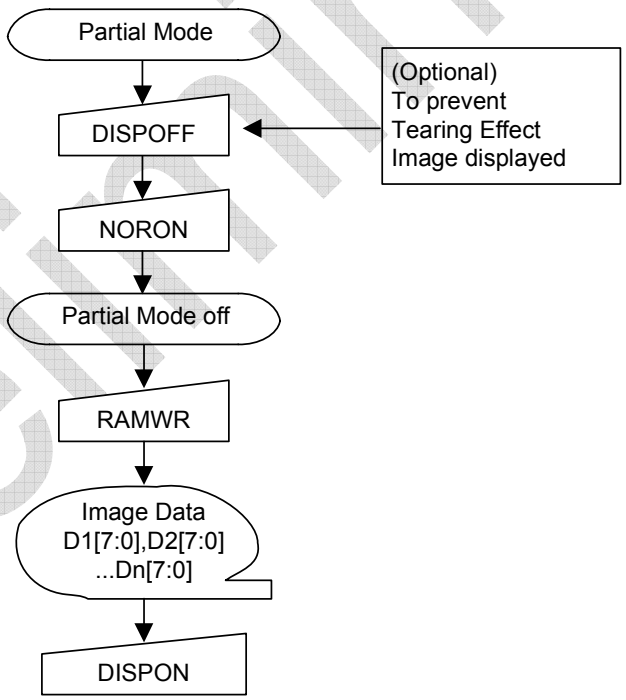
30H	PLTAR (Partial Area)
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	SR[15:0]=0000h ER[15:0]=0EFh
H/W Reset	SR[15:0]=0000h ER[15:0]=0EFh
H/W Reset	SR[15:0]=0000h ER[15:0]=0EFh

Preliminary

30H	PLTAR (Partial Area)
Flow Chart	1. To enter Partial Mode:   2. To exit Partial Mode: 

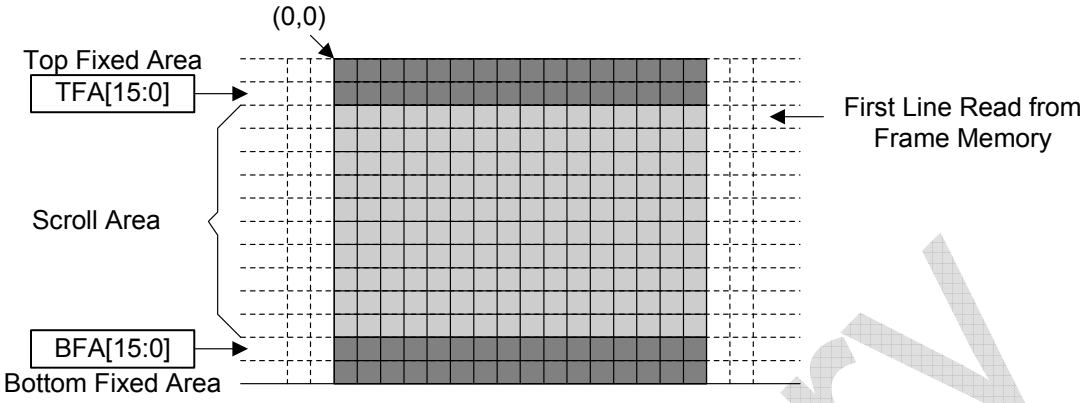
Preliminary

5.1.25. VERTICAL SCROLLING DEFINITION (33H)

33 H	VSCRDEF (Vertical Scrolling Definition)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	TFA [15]	TFA [14]	TFA [13]	TFA [12]	TFA [11]	TFA [10]	TFA [9]	TFA [8]	0000 .... 0EF
2nd parameter	1	1	↑	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA [3]	TFA [2]	TFA [1]	TFA [0]	
3rd parameter	1	1	↑	VSA [15]	VSA [14]	VSA [13]	VSA [12]	VSA [11]	VSA [10]	VSA [9]	VSA [8]	0000 .... 0EF
4th parameter	1	1	↑	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]	
5th parameter	1	1	↑	BFA [15]	BFA [14]	BFA [13]	BFA [12]	BFA [11]	BFA [10]	BFA [9]	BFA [8]	0000 .... 0EF
6th parameter	1	1	↑	BFA [7]	BFA [6]	BFA [5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]	
Description	This command defines the Vertical Scrolling Area of the display. (refer to Restriction) When MADCTL B4 = 0 The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. Of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area(in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.											

Preliminary

33 H	VSCRDEF (Vertical Scrolling Definition)



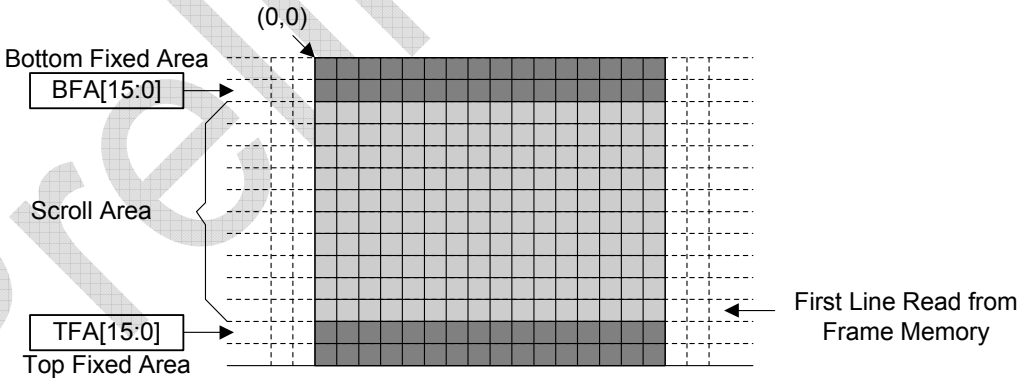
When MADCTL B4 = 1

The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area(in No. of lines from Top of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



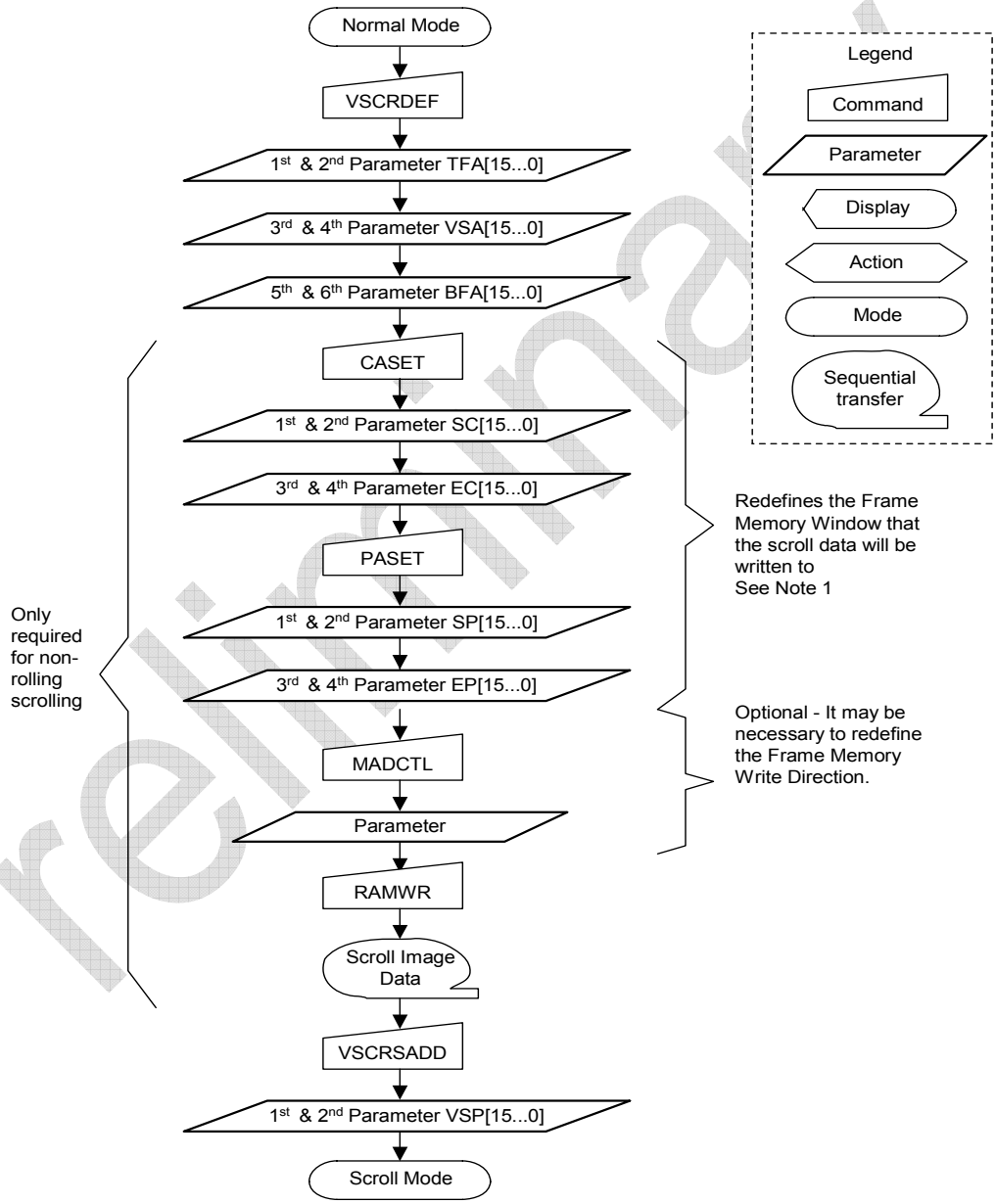
Restriction	**Note.** The condition is (TFA+VSA+BFA)≥320, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to “0” – this only affects the Frame Memory Write.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes

Preliminary

33 H	VSCRDEF (Vertical Scrolling Definition)
	Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes
Flow Chart	To enter Vertical Scroll Mode:

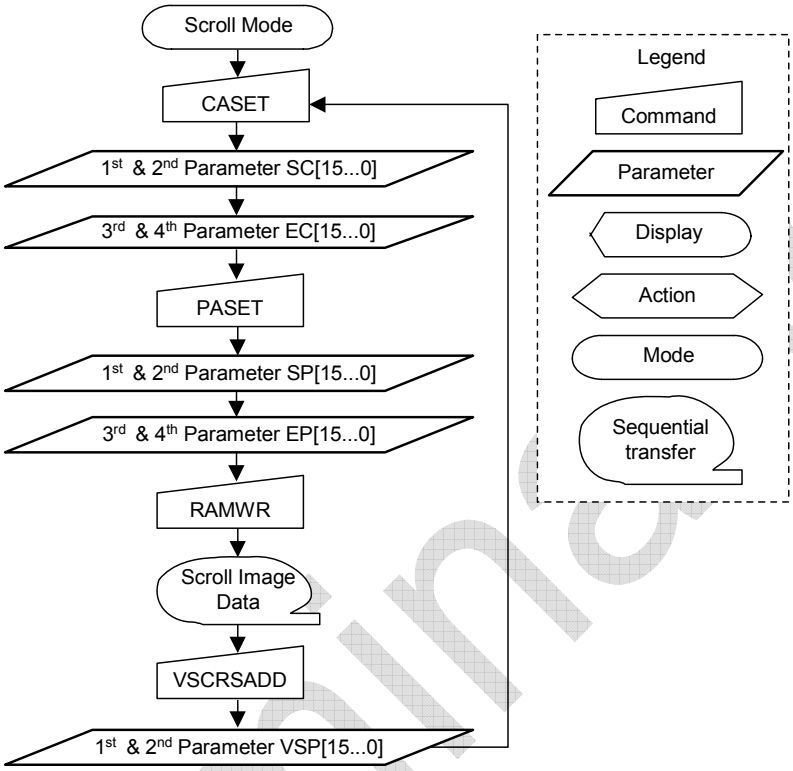


Note.

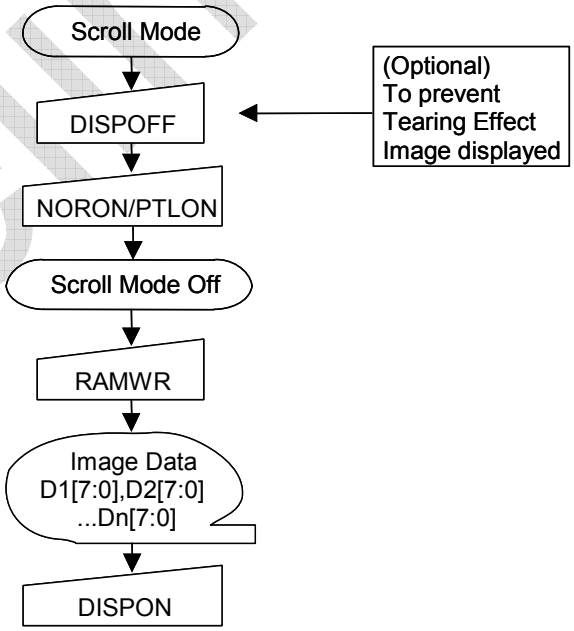
The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed

Preliminary

33 H	VSCRDEF (Vertical Scrolling Definition)
Flow Chart	Continuous Scroll:



To leave Vertical Scroll Mode:



Note.

Scroll Mode can be exit by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

Preliminary

5.1.26. TEARING EFFECT LINE OFF (34H)

34 H	TEOFF (Tearing Effect Line OFF)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER											
Description	This command is used to turn Off (Active Low) the Tearing Effect output signal from TE signal line.											
Restriction	This command has no effect when Tearing Effect output is already Off.											

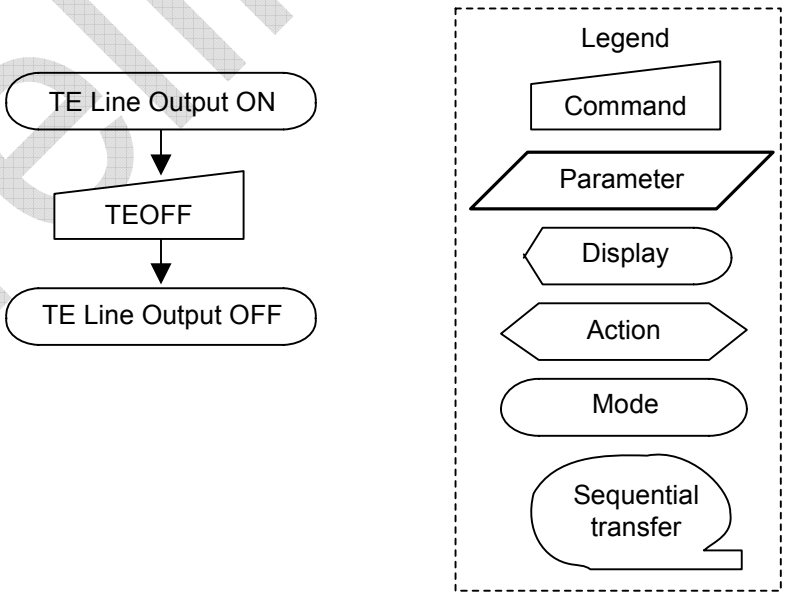
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



Preliminary

5.1.27. TEARING EFFECT LINE ON (35H)

35 H	TEON (Tearing Effect Line ON)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	X	X	X	X	X	X	X	M	xx

Description

This command is used to turn On the Tearing Effect output signal from the TE signal line.

This output is not affected by changing Memory Address Control command bit “B4”.

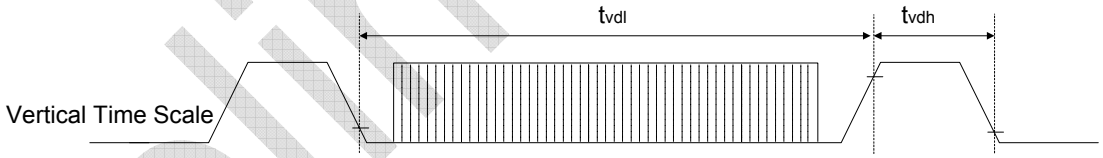
The Tearing Effect Line On has one parameter that describes the mode of the Tearing Effect Output Line. (X = don’t care).

When M=0:

The Tearing Effect Output line consists of V-Blanking information only:

When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



During Sleep In mode with Tearing Effect Line On, Tearing Effect output pin will be active low.

Restriction

This command has no effect when Tearing Effect output is already On.

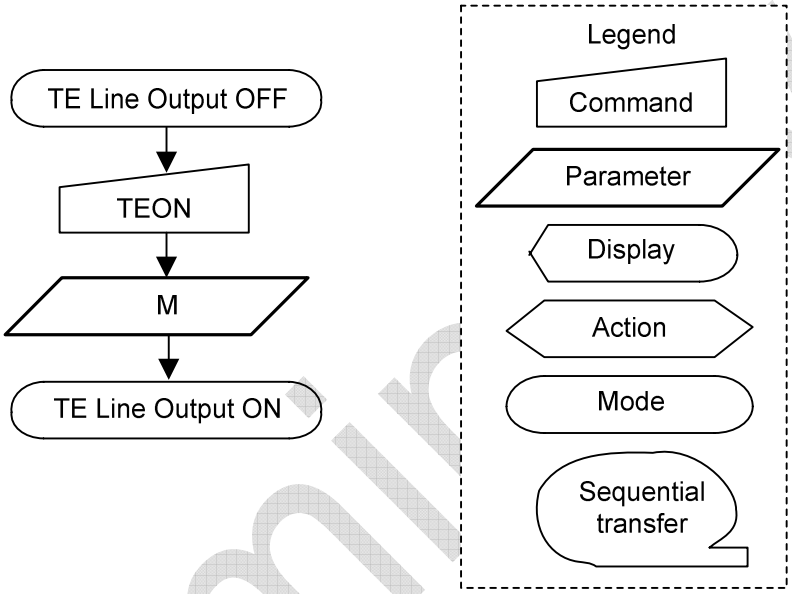
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Preliminary

35 H	TEON (Tearing Effect Line ON)
Default	
Flow Chart	

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off



Preliminary

5.1.28. MEMORY DATA ACCESS CONTROL (36H)

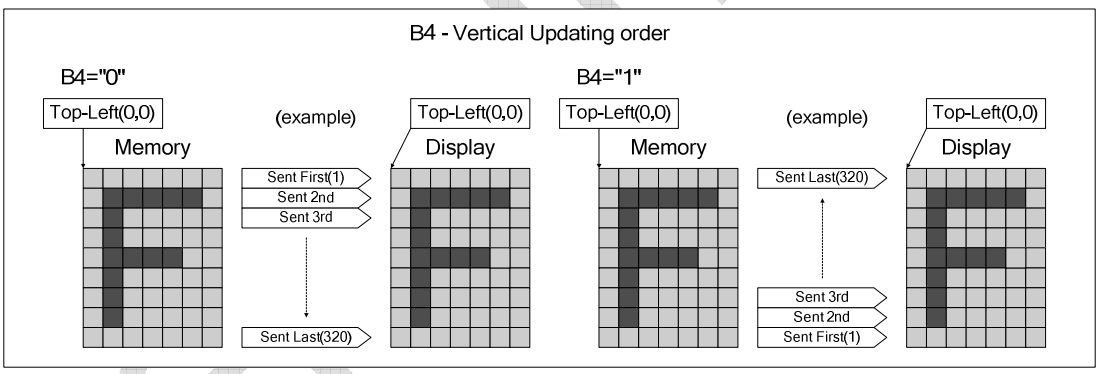
36 H	MADCTL (Memory Data Access Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	0	36
parameter	1	1	↑	B7	B6	B5	B4	B3	X	X	X	xx

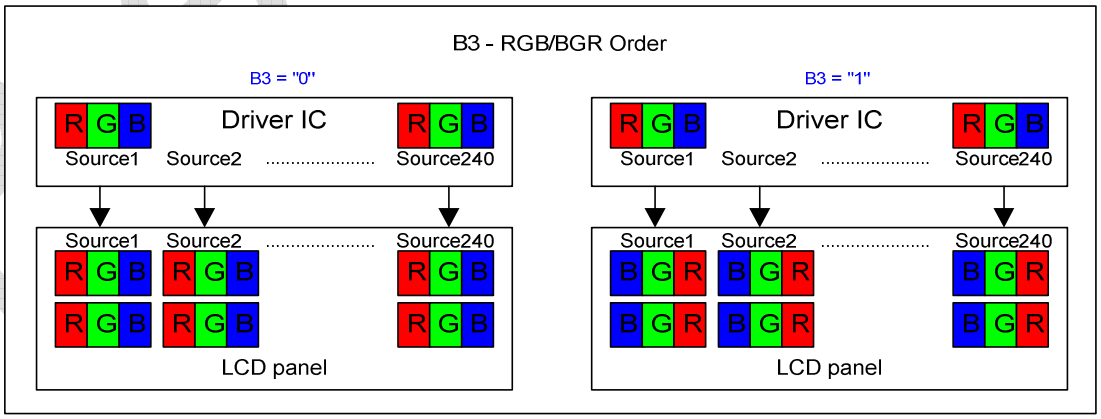
Description

This command defines read/write scanning direction of frame memory.

This command makes No Change on the other driver status.

Bit	Name	Description
B7	Page Address Order	These 3 bits control MPU to memory write/read Direction.
B6	Column Address Order	
B5	Page/Column Selection	
B4	Line Address Order	LCD refresh direction control
B3	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)





Note.

Top-Left (0,0) means a physical memory location

Restriction

D2, D1 and D0 are set to “000” internally.

36 H	MADCTL (Memory Data Access Control)

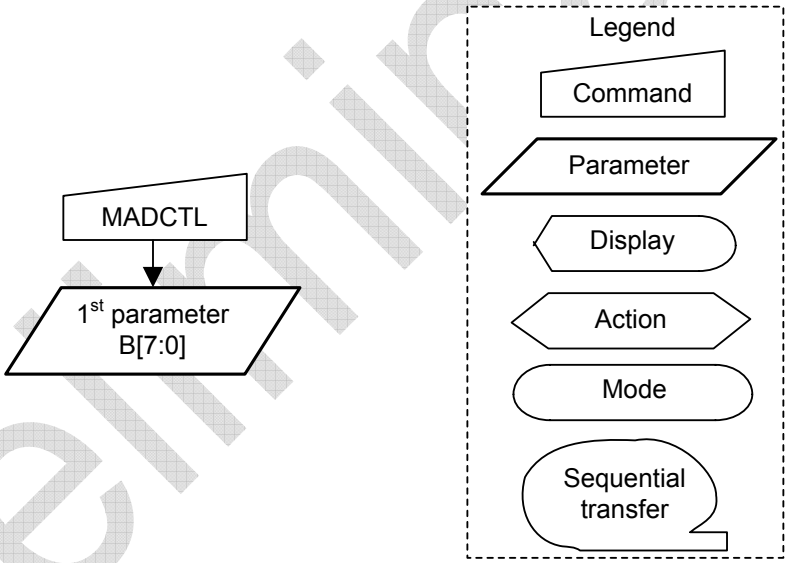
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	B7=0, B6=0, B5=0, B4=0, B3=0, B2=0, B1=0, B0=0
S/W Reset	No Change
H/W Reset	B7=0, B6=0, B5=0, B4=0, B3=0, B2=0, B1=0, B0=0

Flow Chart



Preliminary

5.1.29. VERTICAL SCROLLING START ADDRESS (37H)

37H	VSCRSADD (Vertical Scrolling Start Address)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	0000 …. 0EF
2nd parameter	1	1	↑	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	

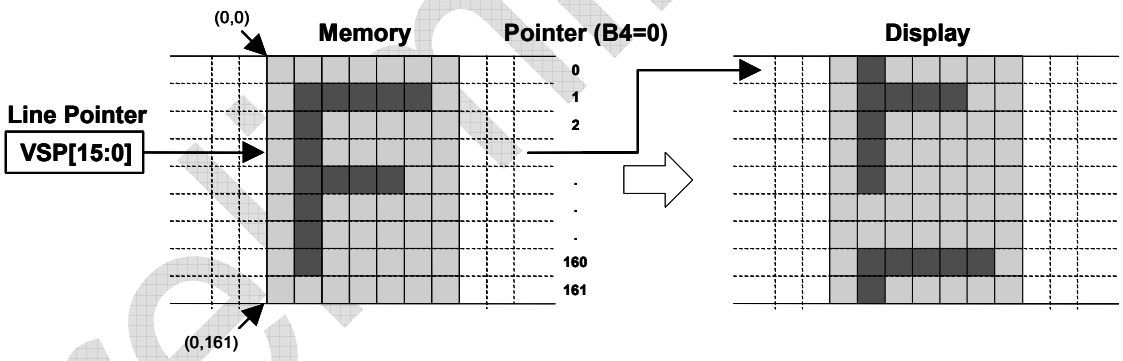
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. (refer to Restriction)

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below.

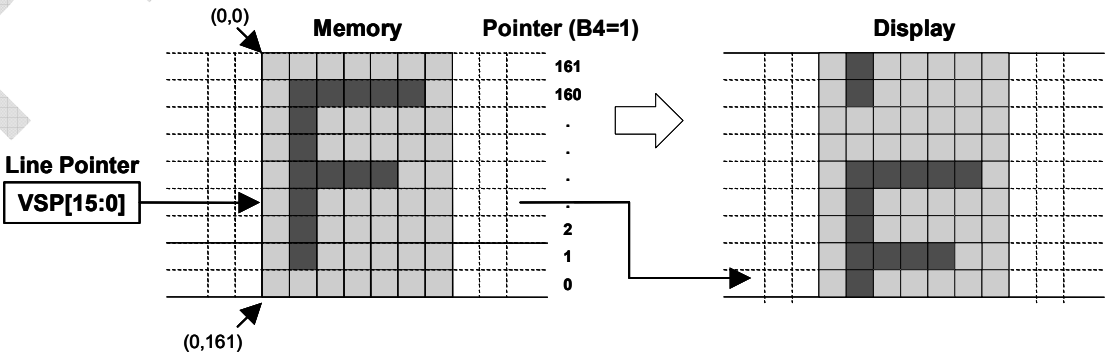
When MADCTL B4 = 0

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP= '3'.



When MADCTL B4 = 1

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP = '3'.



Note.

Preliminary

37H	VSCRSADD (Vertical Scrolling Start Address)
	1. When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. 2. VSP refers to the Vertical Scrolling Start Address.
Restriction	**Note.** Each detail initial values by the display resolution will be updated. Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition 33h) – otherwise undesirable image will be displayed on the Panel.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	0000
S/W Reset	0000
H/W Reset	0000

Flow Chart	See Vertical Scrolling Definition (33h) description.

Preliminary

5.1.30. IDLE MODE OFF (38H)

38H	IDMOFF (Idle Mode Off)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER											
Description	This command is used to recover from idle mode on. In the idle off mode, LCD can display maximum 262k-color.											
Restriction	This command has no effect when module is already in idle off mode.											

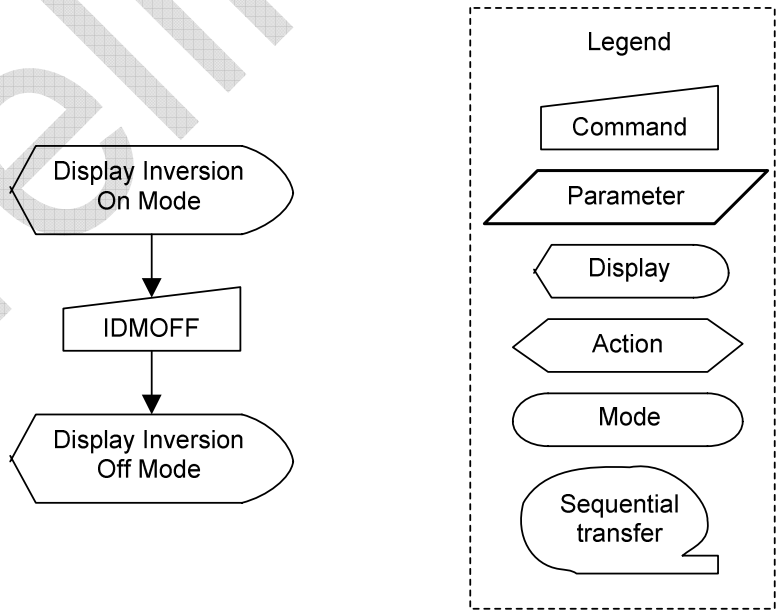
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Idle off mode
S/W Reset	Idle off mode
H/W Reset	Idle off mode

Flow Chart



Preliminary

5.1.31. IDLE MODE ON (39H)

39H	IDMON (Idle Mode On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER											

Description

This command is used to enter into idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

Memory contents vs Display Color X=don't care

Color	R5,R4,R3,R2,R1,R0	G5,G4,G3,G2,G1,G0	B5,B4,B3,B2,B1,B0
Red	1 x x x x x	0 x x x x x	0 x x x x x
Green	0 x x x x x	1 x x x x x	0 x x x x x
Blue	0 x x x x x	0 x x x x x	1 x x x x x
White	1 x x x x x	1 x x x x x	1 x x x x x
Black	0 x x x x x	0 x x x x x	0 x x x x x
Cyan	0 x x x x x	1 x x x x x	1 x x x x x
Magenta	1 x x x x x	0 x x x x x	1 x x x x x
Yellow	1 x x x x x	1 x x x x x	0 x x x x x

Restriction

This command has no effect when module is already in idle on mode.

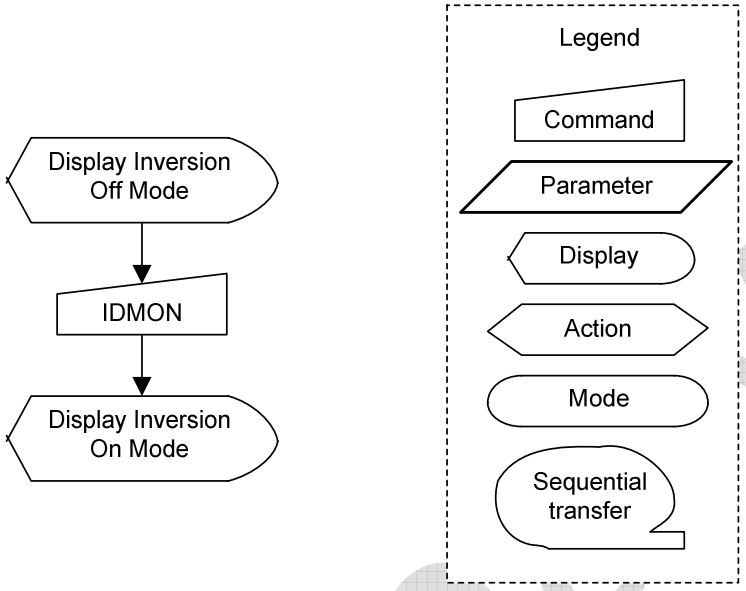
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Off Mode
S/W Reset	Idle Off Mode
H/W Reset	Idle Off Mode

Preliminary

39H	IDMON (Idle Mode On)
Flow Chart	

Preliminary

5.1.32. INTERFACE PIXEL FORMAT (3AH)

3AH	COLMOD (Interface Pixel Format)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	1	0	3A
Parameter	1	1	↑	X	D6	D5	D4	X	D2	D1	D0	xx

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MPU interface. The formats are shown in the table below:

Bit	Description	Value
D7	-	"0" (Not used)
D6	RGB Interface Color Format	"101"=16 bit/pixel "110"=18 bit/pixel
D5		
D4		
D3	-	"0" (Not used)
D2	Control Interface Color Format	"101"=16 bit/pixel "110"=18 bit/pixel
D1		
D0		

Restriction

There is no visible effect until the Frame Memory is written to.

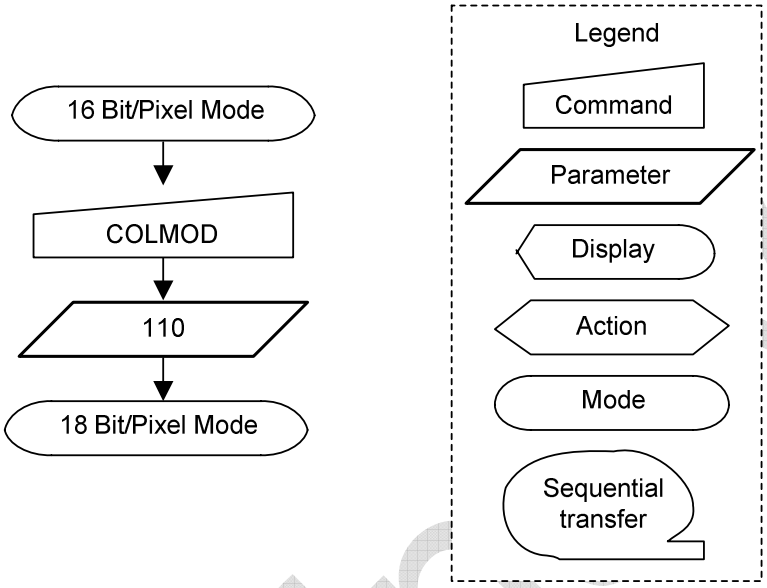
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	18 bit / pixel
S/W Reset	No Change
H/W Reset	18 bit / pixel

Preliminary

3AH	COLMOD (Interface Pixel Format)
Flow Chart	Example: 

Preliminary

5.1.33. MEMORY WRITE CONTINUE (3CH)

3CH	RAMWRC (Memory Write Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	1	0	0	3C
1st Parameter	1	1	↑	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00.. FF
:	1	1	↑	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00.. FF
Nth Parameter	1	1	↑	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00.. FF
Description	This command is transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. If set_address_mode B5=0: Data is written continuing from the pixel location after the write range of the previous write_memory_continue or write_memory_start. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to the Start Column (SC) and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC +1) * (EP – SP + 1) the extra pixels are ignored. If set_address_mode B5=1: Data is written continuing from the pixel location after the write range of the previous write_memory_continue or write_memory_start. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to the Start Page (SP) and the column register is incremented. Pixels are written to the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC +1) * (EP – SP + 1) the extra pixels are ignored.											
Restriction	A write_memory_start should follow a set_column_address, set_page_address or											

Preliminary

set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

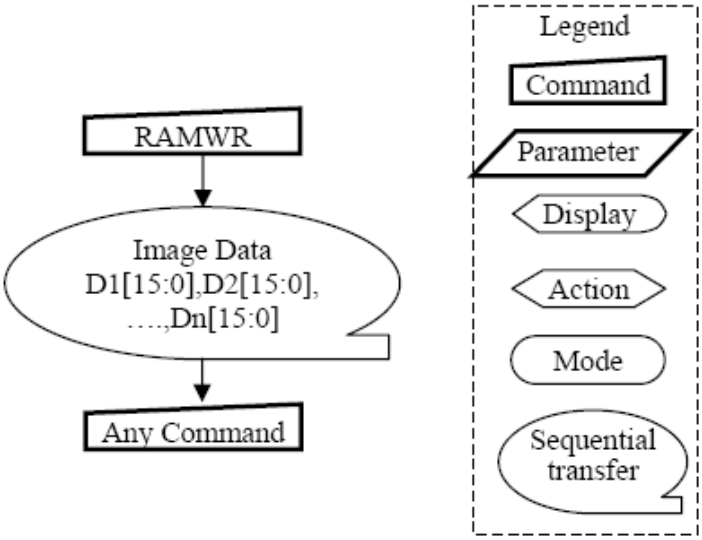
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



5.1.34. MEMORY READ CONTINUE (3EH)

3EH	RAMRDC (Memory Read Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	1	1	0	3E
1st Parameter	1	↑	1	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00.. FF
:	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00.. FF
Nth Parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00.. FF
Description	This command is transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If set_address_mode B5=0: Pixels are read continuing from the pixel location after the read range of the previous read_memory_continue or read_memory_start. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If set_address_mode B5=1: Pixels are read continuing from the pixel location after the read range of the previous read_memory_continue or read_memory_start. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.											
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 18-bit so there is no restriction on the length of data. A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read address. Otherwise, data read with read_memory_continue is undefined.											

Preliminary

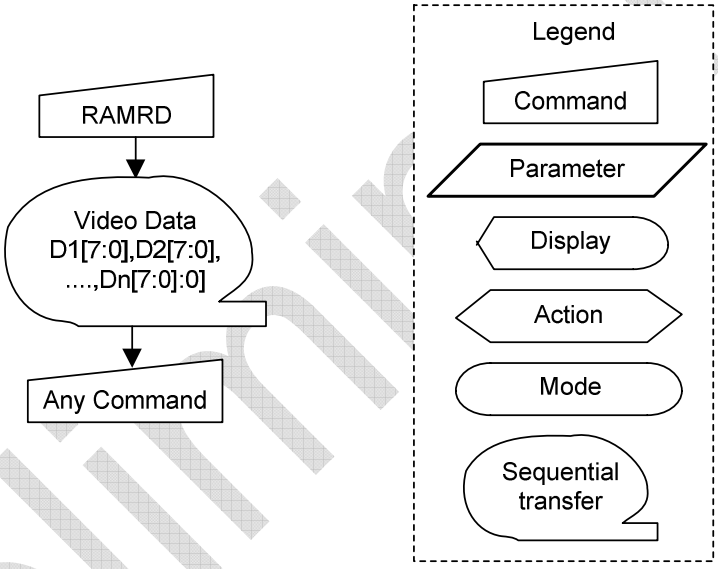
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



Preliminary

5.1.35. SET TEAR SCANLINE (44H)

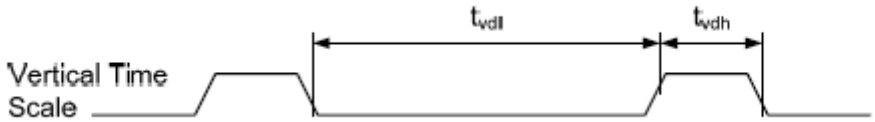
44H	TESCAN (Set Tear Scanline)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	0	0	1	0	0	44
1st Parameter	1	1	↑	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]	xx
2nd Parameter	1	1	↑	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]	xx

Description

This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing set_address_mode bit B4.

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

The Tearing Effect Output line consists of V-Blanking information only.



Note that set_tear_scanline with N=0 is equivalent to set_tear_on with M=0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

This command takes affect on the frame following the current frame. Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous set_tear_on, or set_tear_scanline, command until the end of the frame.

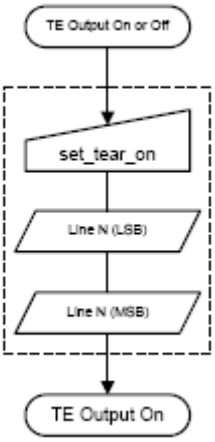
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	16'h0000
S/W Reset	16'h0000
H/W Reset	16'h0000

Preliminary

Flow Chart	

Preliminary

5.1.36. GET SCANLINE (45H)

45H	RDTESCAN (Get Scanline)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	0	0	1	0	1	45
1st Parameter	1	↑	1	N[15]	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]	xx
2nd Parameter	1	↑	1	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]	xx

Description

The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of Vsync and is denoted as Line 0.

When in Sleep Mode, the value returned by get_scanline is undefined.

Restriction

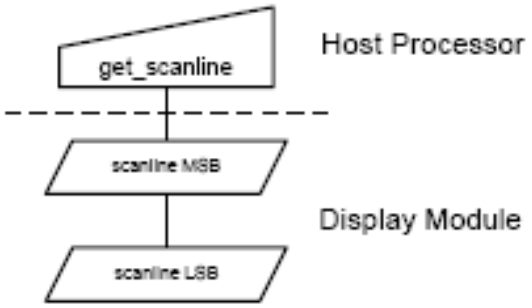
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	16'h0000
S/W Reset	16'h0000
H/W Reset	16'h0000

Flow Chart



Preliminary

5.1.37. WRITE MANUAL BRIGHTNESS (51H)

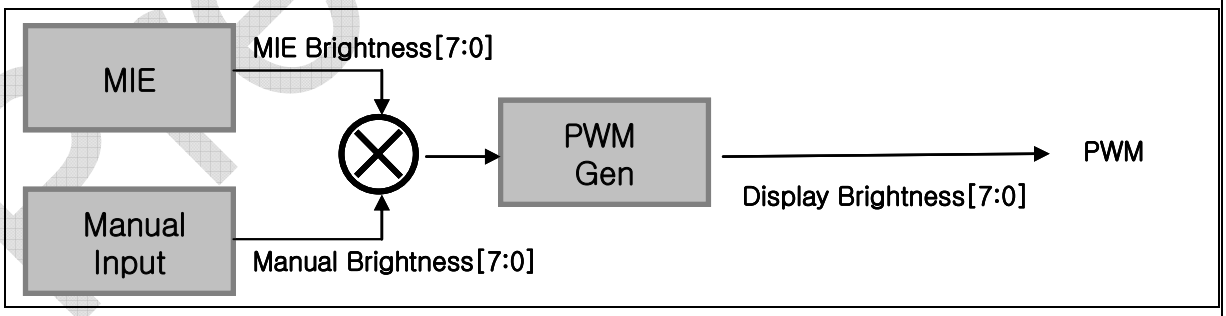
51H	WRDISBV (Write Manual Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	0	1	51
Parameter	1	1	↑	MAN_ BR[7]	MAN_ BR[6]	MAN_ BR[5]	MAN_ BR[4]	MAN_ BR[3]	MAN_ BR[2]	MAN_ BR[1]	MAN_ BR[0]	xx

Description

This command is used to set the manual brightness value. If the manual brightness is used (BC_MODE = “01” or “11”), the value of register “MAN_BR [7:0] is selected or merged with the MIE brightness to generate PWM.

MAN_BR [7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Manual Birightness



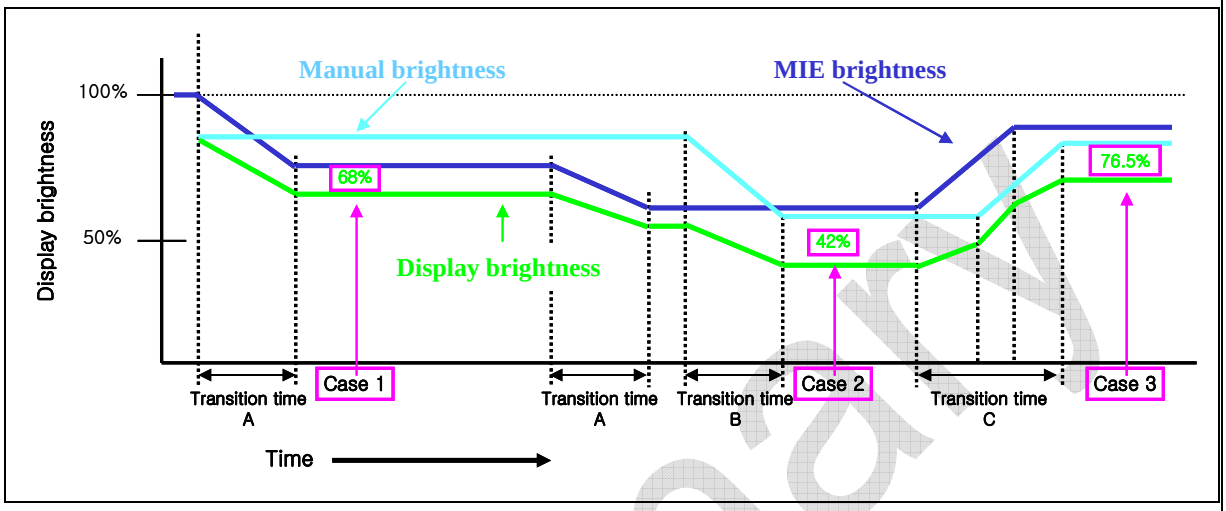
The display brightness level is calculated with the following formula.

$$Display_Brightness = MIE_Brightness \ X \ Manual_Brightness / 255$$

The MIE brightness has transition time A and the manual brightness has transition time B.

The maximum transition time is transition time C (C ≤ A + B).

Example of manual brightness



Operation Mode	Manual Brightness	MIE Brightness	Display Brightness
Case 1	85 %	80 %	68 %
Case 2	60 %	70 %	42 %
Case 3	85 %	90 %	76.5 %

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Preliminary

5.1.38. READ DISPLAY BRIGHTNESS (52H)

52H	RDDISBV (Read Display Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	1	0	52
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	BR_ OUT[7]	BR_ OUT[6]	BR_ OUT[5]	BR_ OUT[4]	BR_ OUT[3]	BR_ OUT[2]	BR_ OUT[1]	BR_ OUT[0]	xx

Description

This command is used to read the display brightness value. It is a real brightness value of PWM output which is calculated with MIE brightness and manual brightness. The value of this register is updated after display V-sync and host can read exact value after display V-sync.

BR_OUT [7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Restriction

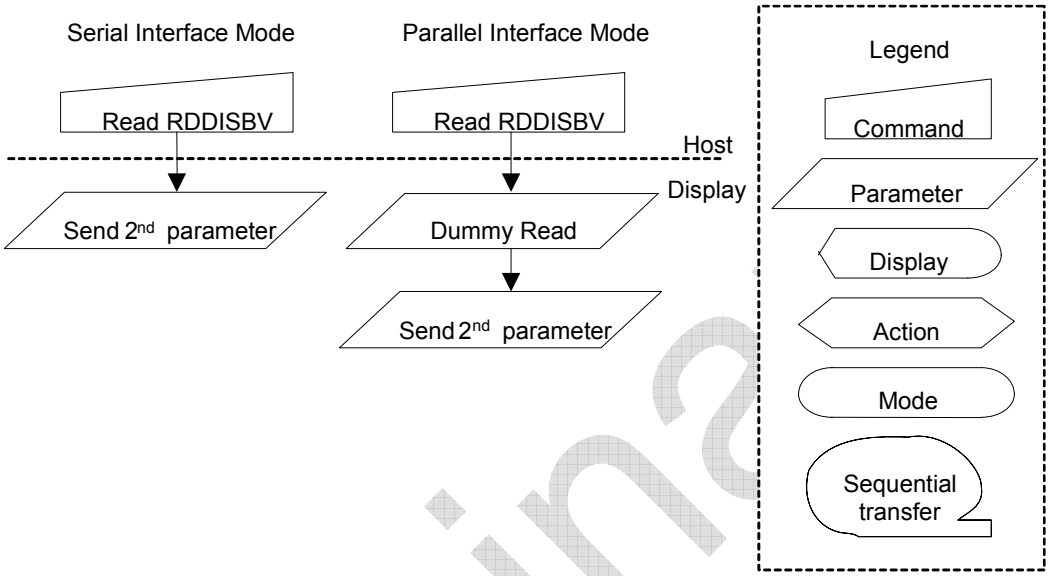
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart



Preliminary

5.1.39. WRITE BL CONTROL (53H)

53H	WRCTRLD (Write BL Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	1	1	53
Parameter	1	1	↑	0	0	BCTRL	0	DD	BL	0	0	xx

Description

- BCTRL

This register is used to enable the backlight control block. If BCTRL is turned off, the BL control block is not working and PWM output is fixed to low.

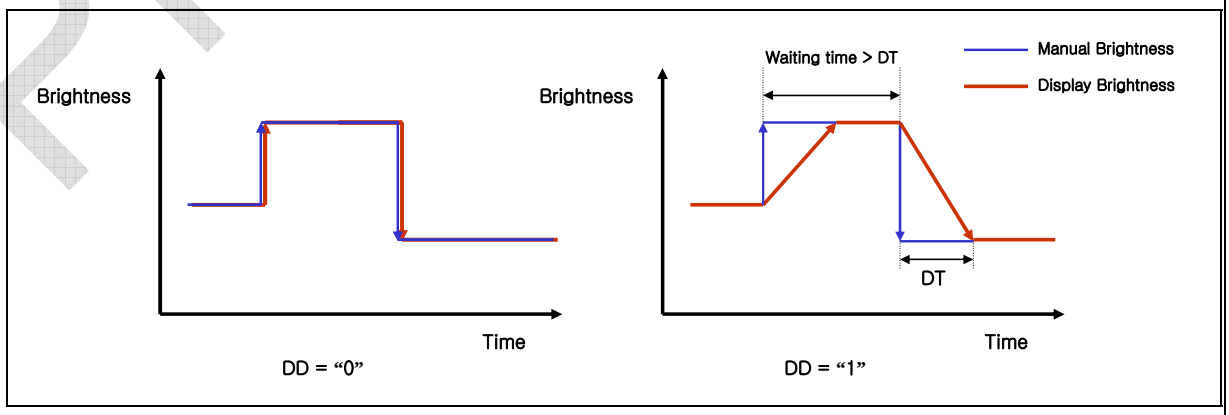
BRCTRL	BL Control
0	Off
1	On

- DD

This register is used to enable the manual brightness dimming function. The manual brightness should be changed smoothly for preventing a visible artifact, e.g. flicker. So the dimming function is needed when the transition of input manual brightness is fast to make a visible artifact. When the manual dimming is enabled, the new manual brightness value has to be changed after former dimming transition is finished. The transition time is controlled by DT[2:0].

DD	Manual Dimming Function
0	Off
1	On

Manual dimming function



- BL

Preliminary

This register is used to enable the PWM output. Even if the value of BL is “0”, the backlight control block is working when BCTRL is “1”. And the host can read the display brightness value(DISP_BRIGHT[7:0]) and control the BLU directly.

BL	PWM state
0	Low
1	Active

Restriction

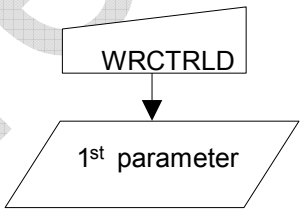
Register Availability

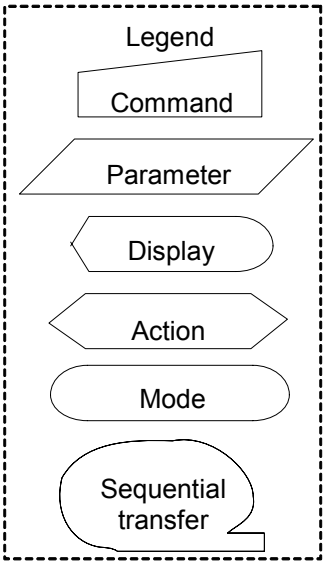
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8’h00
S/W Reset	8’h00
H/W Reset	8’h00

Flow Chart





Preliminary

5.1.40. READ BL CONTROL (54H)

54H	RDCTRLD (Read BL Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	0	0	54
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	0	0	BCTRL	0	DD	BL	0	0	xx
Description	This command is used to read BL control register. For details, refer to Write BL Control (53h).											
Restriction												

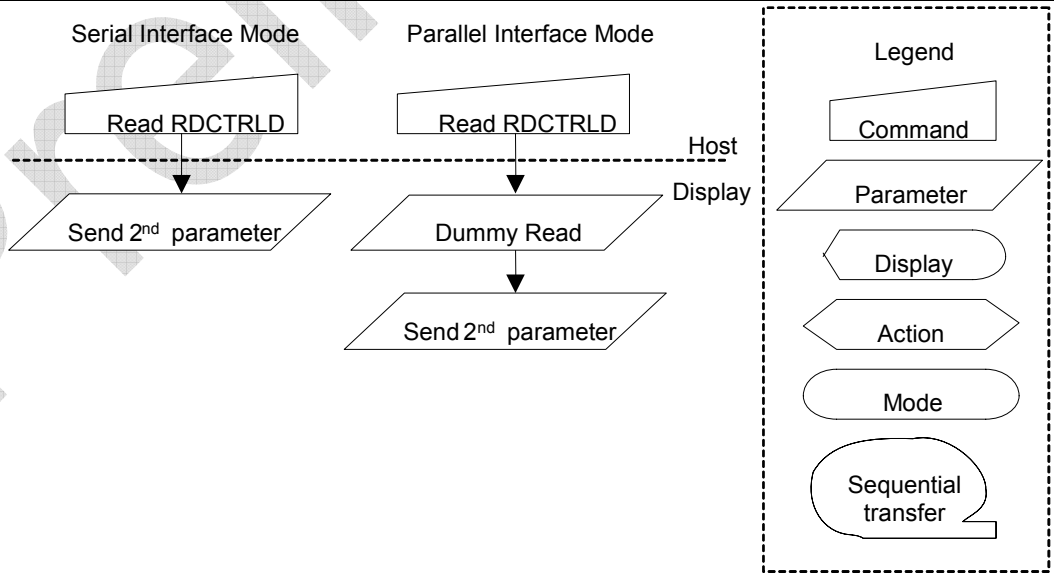
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart



Preliminary

5.1.41. WRITE MIE MODE (55H)

55H	WRCABC (Write MIE Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	0	1	55
Parameter	1	1	↑	0	0	0	0	0	0	MIE_ MODE[1]	MIE_ MODE[0]	xx

Description

This command is used to select the operation mode of MIE. In UI or Still-image mode, the host should send same image at least two times to apply MIE algorithm exactly. If the MIE is off mode, the BLU brightness value of MIE is set to 255.

MIE_MODE[1:0]	Operation Mode
00	Off
01	UI (User Interface)
10	Still Image
11	Moving Image

Restriction

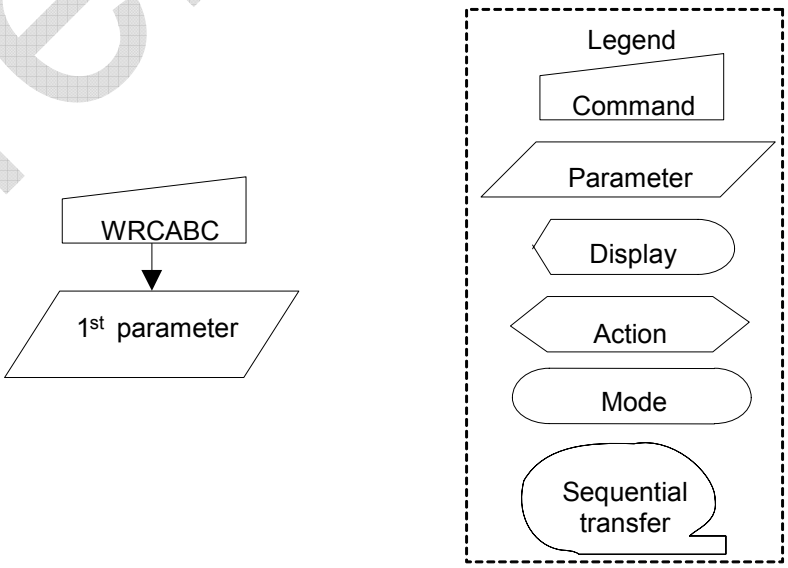
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart



Preliminary

5.1.42. READ MIE MODE (56H)

56H	RDCABC (Read MIE Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	1	0	56
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	0	0	0	0	0	0	MIE_ MODE[1]	MIE_ MODE[0]	xx
Description	This command is used to read MIE mode register. For details, refer to Write MIE Mode (55h).											
Restriction												

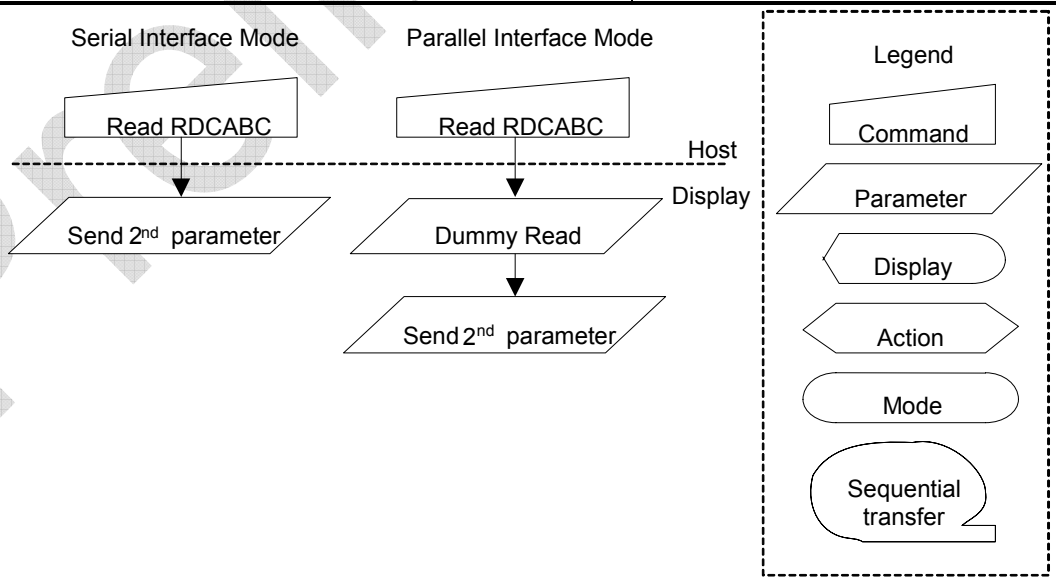
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart



Preliminary

5.1.43. WRITE MINIMUM BRIGHTNESS (5EH)

5EH	WRCABCMB (Write Minimum Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	1	1	1	0	5E
Parameter	1	1	↑	MIN_ BRIGHT [7]	MIN_ BRIGHT [6]	MIN_ BRIGHT [5]	MIN_ BRIGHT [4]	MIN_ BRIGHT [3]	MIN_ BRIGHT [2]	MIN_ BRIGHT [1]	MIN_ BRIGHT [0]	xx

Description

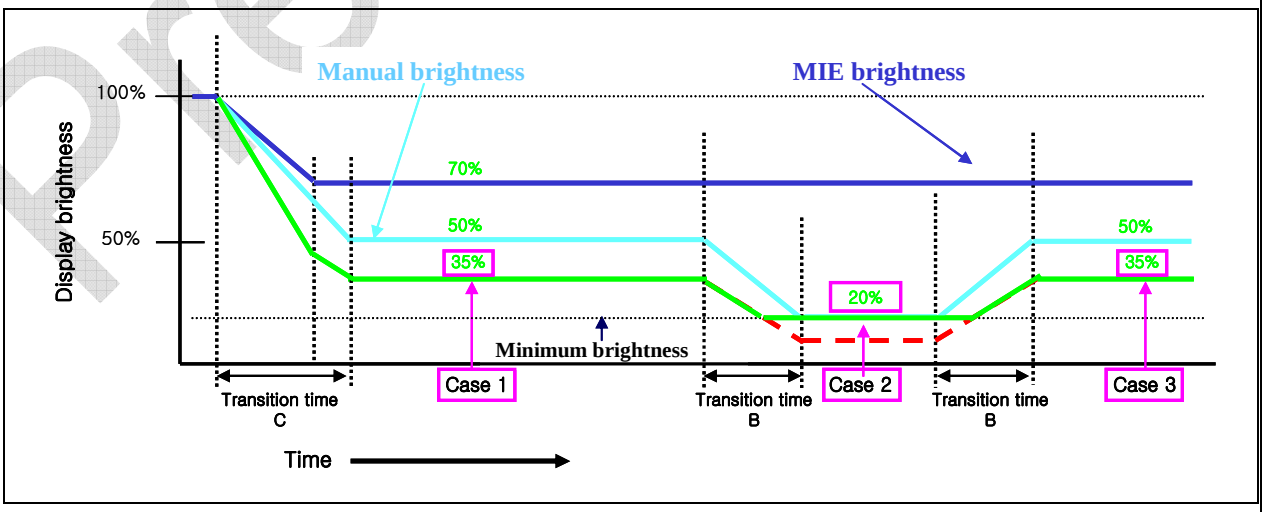
This command is used to set the minimum brightness value.

The MIE function is automatically reduced the backlight brightness based on the content of image. In the case of the combination with the manual brightness setting, the display brightness can be too dark. It must affect to image quality degradation. So the minimum brightness setting is used to avoid too much brightness reduction.

When the MIE is activated, the display brightness can not be reduced less than the value of minimum brightness setting. The image processing function is worked as normal, even if the display brightness can not be decreased by the minimum brightness setting.

This function of the manual brightness setting does not affect to the other functions. The smooth transition and dimming function can be worked as normal. The manual brightness shouldn't be set less than the minimum brightness. When the BL control block is turned off (BCTRL=0), the MIE minimum brightness setting is ignored.

Example of minimum brightness



Operation	Manual	MIE	Calculated	Display

Preliminary

Mode	Brightness	Brightness	Display Brightness	Brightness
Case 1	50 %	70 %	35%	35 %
Case 2	20 %	70 %	14%	20 %
Case 3	50 %	70 %	35%	35 %

MIN_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Status	Default Value
Initial	MIN_BRIGHT[7:0] = 0000_0000

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Preliminary

5.1.44. READ MINIMUM BRIGHTNESS (5FH)

5FH	RDCABCMB (Read Minimum Brightness)											
	DC X	RD X	WR X	D7	D6	D5	D4	D3	D2	D1	D0	HE X
Command	0	1	↑	0	1	0	1	1	1	1	1	5F
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	MIN_ BRIGHT [7]	MIN_ BRIGHT [6]	MIN_ BRIGHT [5]	MIN_ BRIGHT [4]	MIN_ BRIGHT [3]	MIN_ BRIGHT [2]	MIN_ BRIGHT [1]	MIN_ BRIGHT [0]	xx
Description	This command is used to read Minimum Brightness register. For details, refer to Write Minimum Brightness (5Eh).											
Restriction												

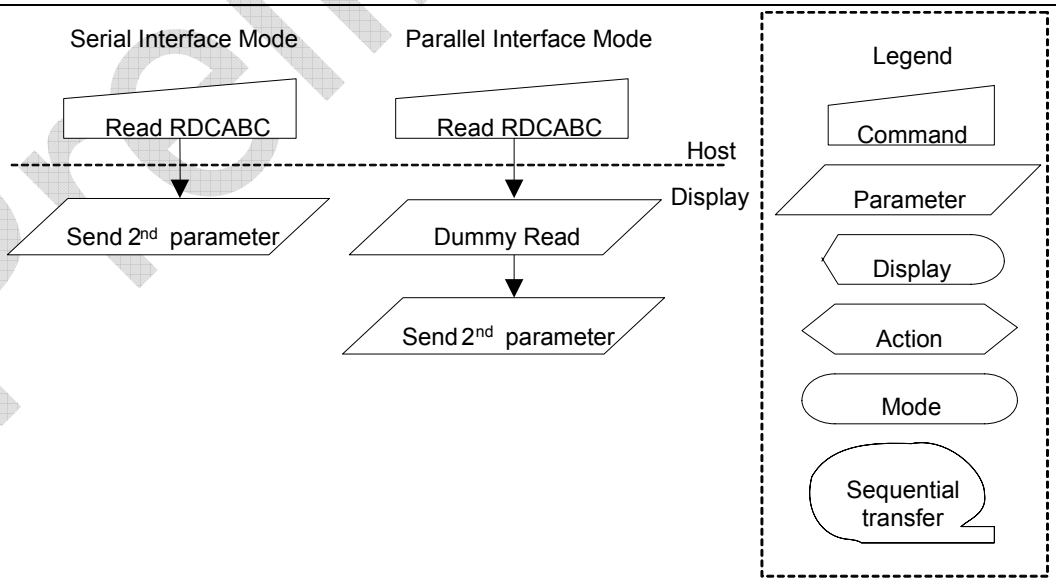
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart



Preliminary

5.1.45. READ DDB START (A1H)

A1H	RDDDBS (Read DDB Start)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	0	0	0	1	A1
1st Parameter	1	↑	1	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00.. FF
:	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00.. FF
Nth Parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00.. FF
Description	This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data. Parameter 1 : MS (most significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization. Parameter 2 : LS (least significant) byte of Supplier ID. Parameter 3 : MS (most significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example. Parameter 4 : LS (least significant) byte of Supplier Elective Data. Parameter 5 : single-byte Escape of Exit Code (EEC). The code is interpreted as follows : - FFh : Exit code - there is no more data in the Descriptor Block - 00h : Escape code - there is supplier-proprietary data in the Descriptor Block(does not conform to any MIPI Alliance standard) - Any other value : there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in MIPI Alliance Standard for Device Descriptor Block (DDB). DDBs may contain many more data fields providing information about the peripheral. In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command read_DDB_start from host processor to peripheral, which includes the bus turn-around token.											

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The peripheral then takes control of the bus and returns the requested data. The peripheral response to read_DDB_start is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command.

The response to a read_DDB_start command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a read_DDB_continue command to access the next portion of the DDB. A read_DDB_continue command begins the next read at the location following the last byte of the previous data read from the DDB.

Subsequent read_DDB_continue commands can be used to read a DDB or supplier-proprietary block of arbitary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any read_DDB_xxx command.

Restriction

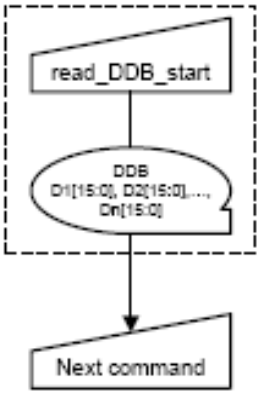
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Preliminary

Flow Chart	

Preliminary

5.1.46. READ DDB CONTINUE (A8H)

A8H	RDDDBC (Read DDB Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	1	0	0	0	A8
1st Parameter	1	↑	1	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00.. FF
:	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00.. FF
Nth Parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00.. FF
Description	See section 5.1.48 (A1h)											
Restriction	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.											

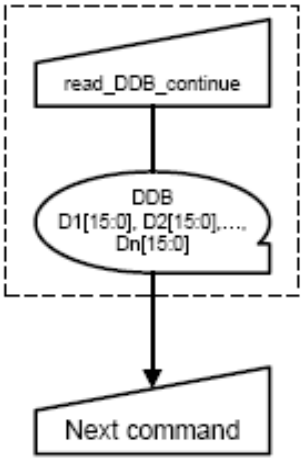
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Preliminary

Flow Chart	

Preliminary

5.1.47. READ ID1 (DAH)

DAH	RDID1 (Read ID1)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	0	DA
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	-
2nd para	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module's manufacturer.											
Restriction												

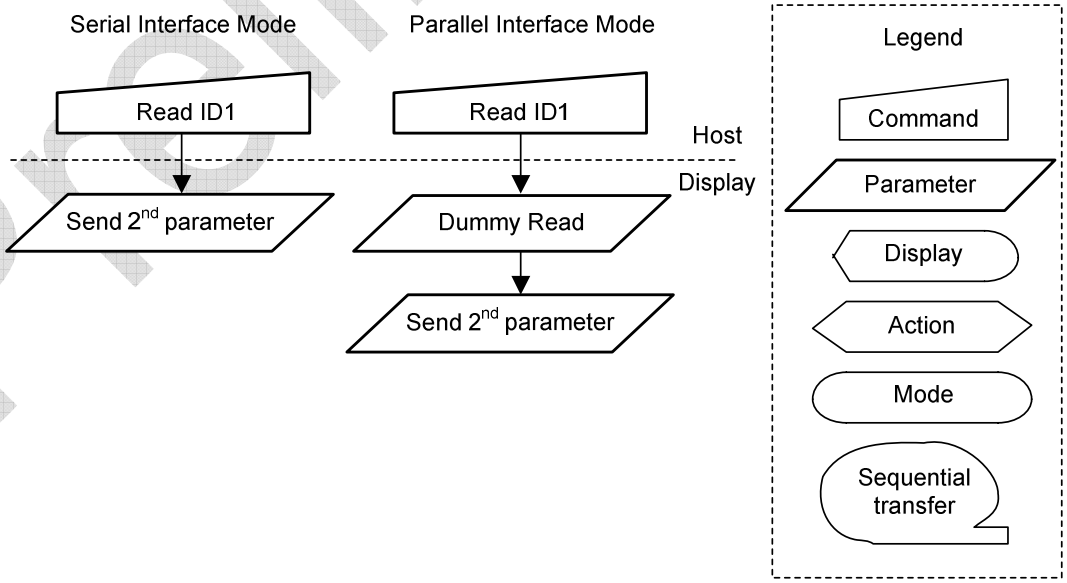
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	54h
S/W Reset	54h
H/W Reset	54h

Flow Chart



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5.1.48. READ ID2 (DBH)

DBH	RDID2 (Read ID2)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	1	DB
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	-
2nd para	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module / driver version ID.											
Restriction												

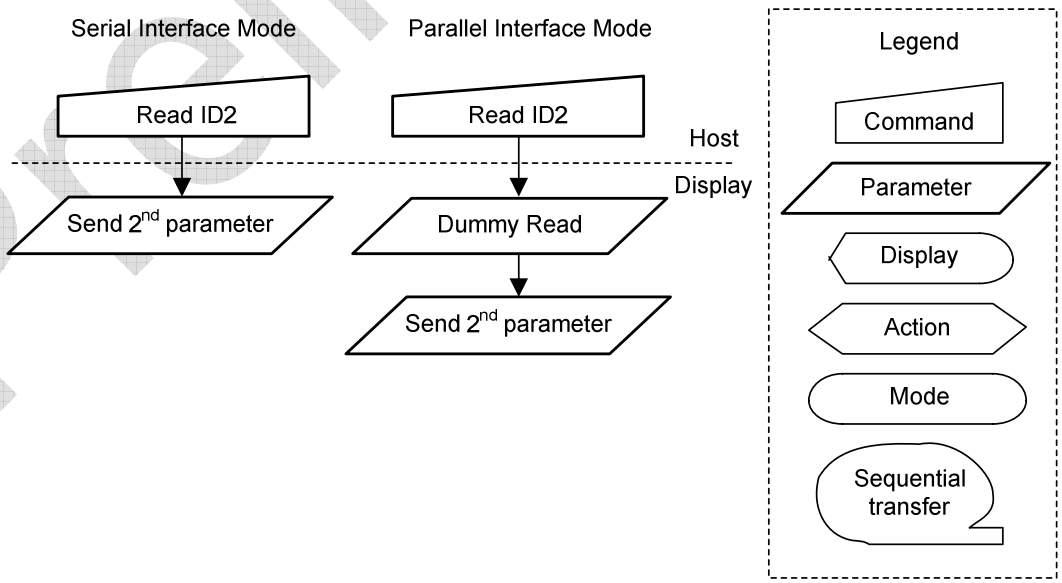
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart



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5.1.49. READ ID3 (DCH)

DCH	RDID3 (Read ID3)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	0	0	DC
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	xx
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module/driver.											
Restriction												

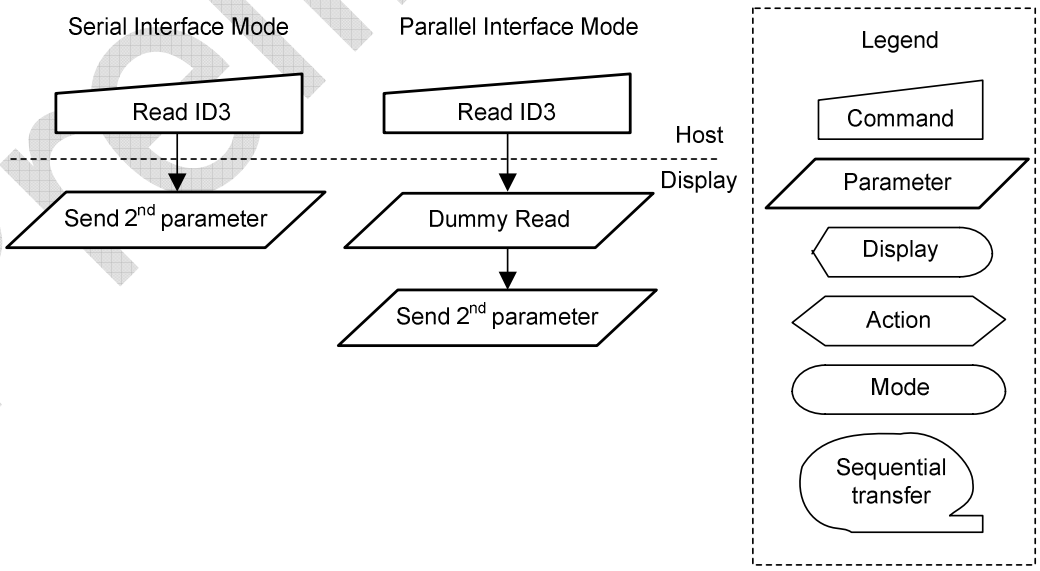
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart



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5.2. DESCRIPTION OF LEVEL 2 COMMAND

Table 73. List of level 2 command

Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
C0h	MIECTL	W	3	MIE control
C1h	BCMODE	W	1	MIE control
C2h	WRMIECTL	W	9	MIE control
C3h	WRBLCTL	W	2	MIE control
D0h	MTPCTL	W	1	MTP control
D2h	MTPACCS	W	2	MTP control
D3h	MTPRD	R	8	MTP control
DFh	DSTB	W	1	Deep Standby
F0h	PASSWD1	W	2	Test Key
F1h	PASSWD2	W	2	Test Key
F2h	DISCTL	W	17	Display control
F3h	MANPWRSEQ	W	5	Power sequence control
F4h	PWRCTL	W	20	Power control
F5h	VCMCTL	W	12	VCOM control
F6h	SRCCTL	W	9	Source control
F7h	IFCTL	W	4	Interface control
F8h	PANELCTL	W	3	Gate control
F9h	GAMMASEL	W	1	Gamma selection
FAh	PGAMMACTL	W	12	Positive gamma control
FBh	NGAMMACTL	W	12	Negative gamma control

Note: The number of parameter is the number of real parameter except dummy parameter.

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5.2.1. MIECTL1 (C0H)

C0h	MIECTL1 (MIE Control1)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	0	0	C0
1st Parameter	1	1	↑	RRC[7]	RRC[6]	RRC[5]	RRC[4]	RRC[3]	RRC[2]	RRC[1]	RRC[0]	8'h80
2nd Parameter	1	1	↑	IERC[7]	IERC[6]	IERC[5]	IERC[4]	IERC[3]	IERC[2]	IERC[1]	IERC[0]	8'h80
3rd Parameter	1	1	↑	-	-	ONOFF DIMMEN	SERC[4]	SERC[3]	SERC[2]	SERC[1]	SERC[0]	8'h10

5.2.1.1. RRC [7:0]: Reduction Rate Control of backlight power. Default value is RRC[7:0]=10000000.

$$Power_Reduction_Rate = Contents_Based_Reduction_Rate \ X \ \frac{RRC}{128}$$

Figure115. Expression of power reduction rate

Contents_Based_Reduction_Rate is the power reduction rate. Reduction range is from '0' (no reduction) to two times of contents adaptive backlight power.

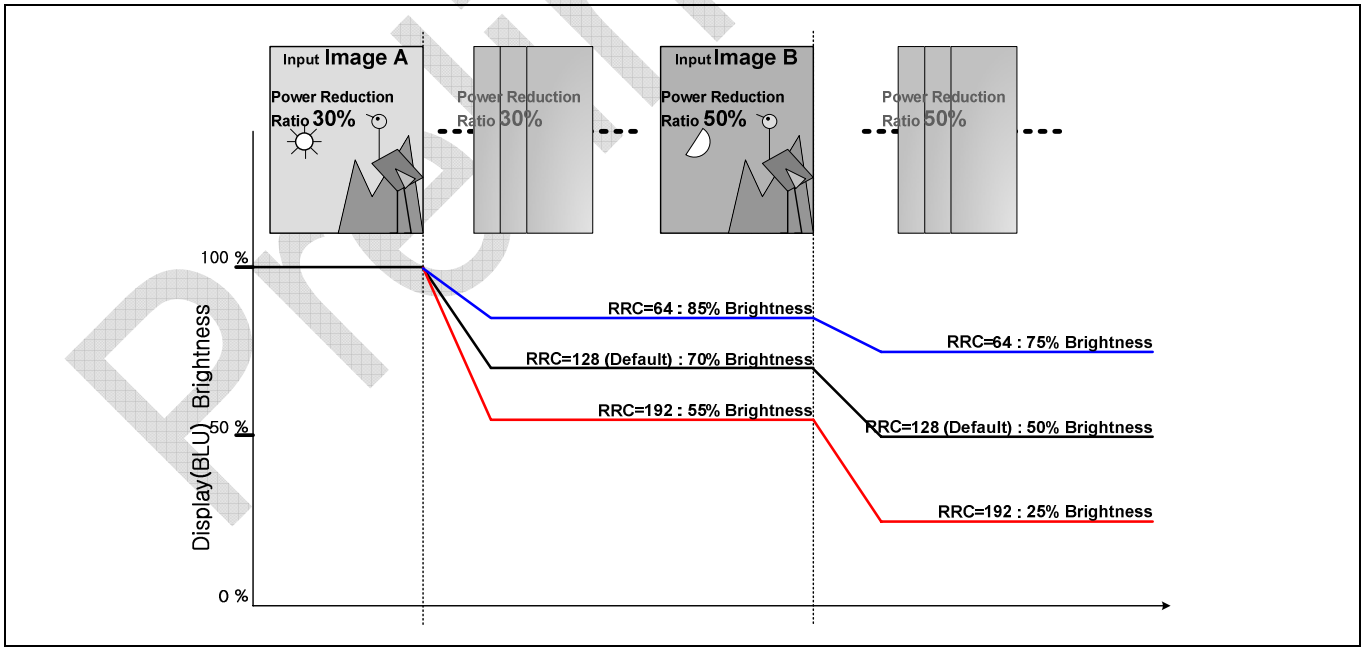

Figure116. According to RRC value, brightness variation

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5.2.1.2. IERC [7:0]: Image Enhancement Rate Control. If IERC is '0', there is no enhancement of input image. If its value is '255', enhancement rate is two times of Image_Enhancement_Rate. Default value is RRC[7:0]=10000000.

$$Adjusted_Image_Enhancement_Rate = Image_Enhancement_Rate \ X \ \frac{IERC}{128}$$

Figure117. Expression of adjusted image enhancement rate

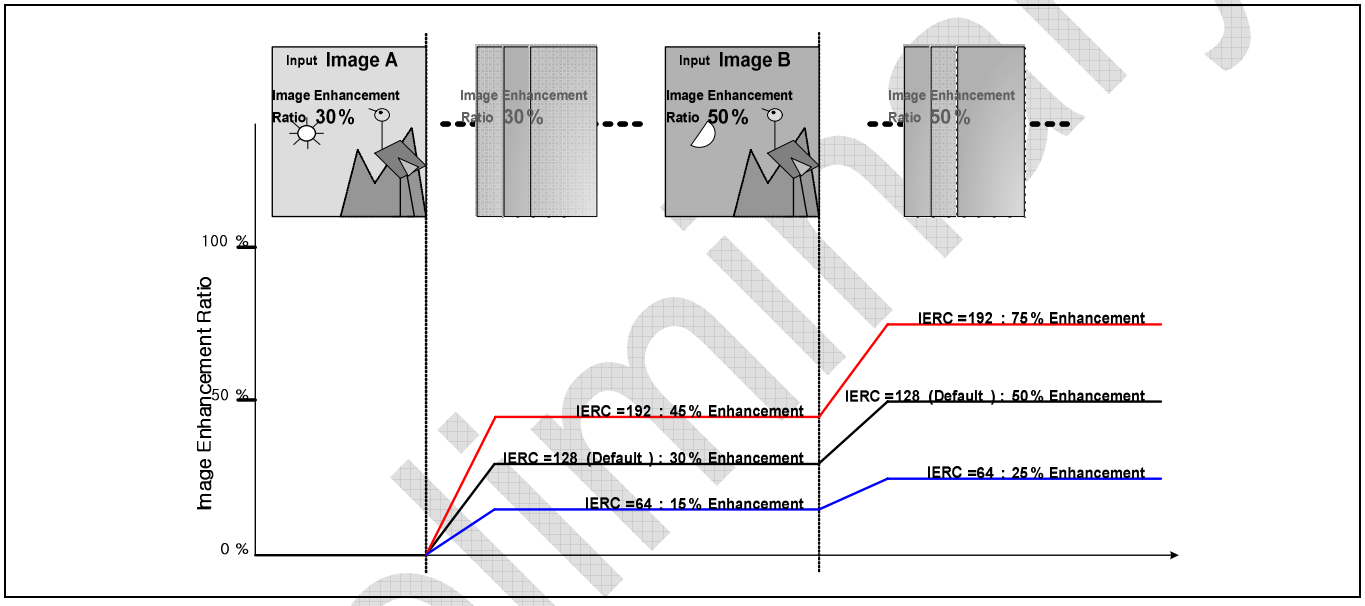

Figure118. According to IERC value, image enhancement ratio variation

Preliminary

5.2.1.3. ONOFF_DIMM_EN

This register is used to enable the on/off dimming function of MIE.

The MIE has a dimming function for preventing abnormal visible artifacts when the MIE is turning on or off.
If the ONOFF_DIMM_EN is “1”, the MIE is smoothly turning on or off. When the ONOFF_DIMM_EN is “0”, the MIE is turning on or off immediately. The transition time is controlled by CST[1:0].
If this dimming function is enabled in UI or STILL mode, the host must write frames more than the transition time of CST[1:0] to finish the dimming transition. If the MIE mode is changed during on/off dimming transition, it will be updated after finishing the dimming transition.

Table 74. ONOFF_DIMM_EN

ONOFF_DIMM_EN	On / Off Dimming Function
0	Disable
1	Enable

Status	Default Value
Initial	ONOFF_DIMM_EN = 0

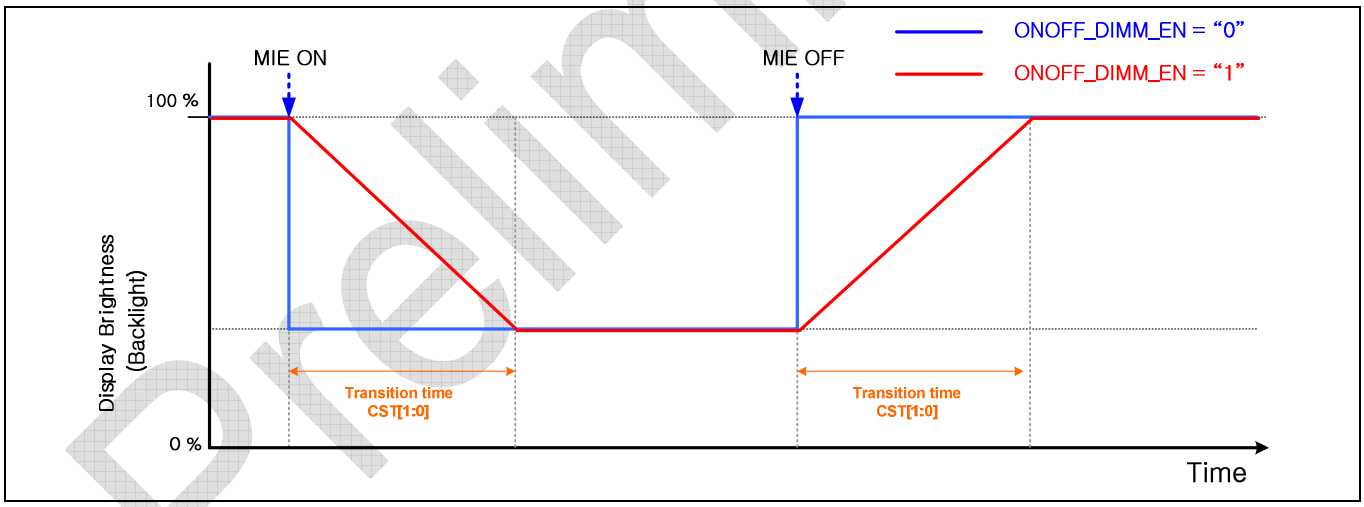

Figure119. Example of MIE On / Off dimming transition control

Preliminary

5.2.1.4. SERC[4:0]

This register is used to adjust the Image Saturation Enhancement Rate.

$$Adjusted_Saturation_Enhancement_Rate = Saturation_Enhancement_Rate\ X\ \frac{SERC}{16}$$

Figure120. Saturation enhancement rate

If the value of SERC is '0', there is no saturation enhancement in output image. If the value of SERC is increased, the saturation enhancement rate will be increased and more vivid image is obtained. The other way, if the value of SERC is decreased, the saturation enhancement rate will be decreased.

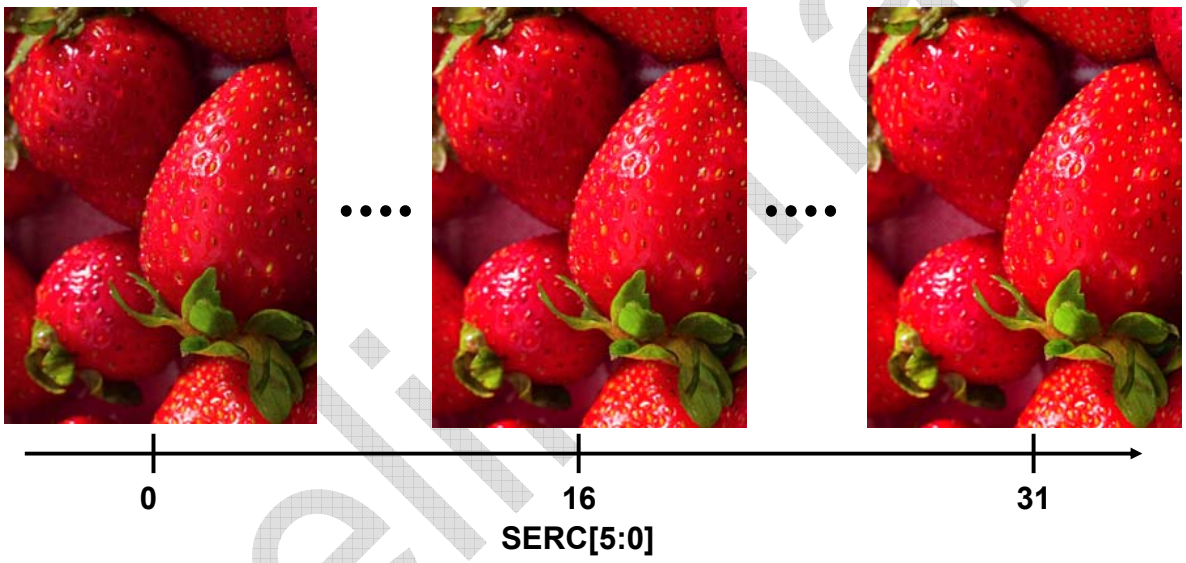

Figure121. Example of SERC

Table 75. SERC[4:0]

SERC[4:0]	Adjust Saturation Enhancement Rate
00000	Saturation Enhancement Rate x 0/16
00001	Saturation Enhancement Rate x 1/16
00010	Saturation Enhancement Rate x 2/16
…	…
10000	Saturation Enhancement Rate x 16/16
…	…
11101	Saturation Enhancement Rate x 29/16

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SERC[4:0]	Adjust Saturation Enhancement Rate
11110	Saturation Enhancement Rate x 30/16
11111	Saturation Enhancement Rate x 31/16

Status	Default Value
Initial	SERC[4:0] = 10000

Preliminary

5.2.2. BCMODE (C1H)

C1h	BCMODE											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	0	1	C1
Parameter	1	1	↑	-	-	-	-	-	-	BC_ MODE[1]	BC_ MODE[0]	8'h11

5.2.2.1. BC_MODE[1:0]

Table 76. BC_MODE[1:0]

BC_MODE[1:0]	BLU Control Mode
0	Off
1	Manual Only
2	MIE Brightness
3	Both

Status	Default Value
Initial	BC_MODE[1:0] = 11

Preliminary

5.2.3. WRMIECTL2 (C2H)

C2h	Write MIE Control 2											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	0	C2
1st Parameter	1	1	↑	-	-	-	-	CAT [1]	CAT [0]	CST [1]	CST [0]	8'h00-

5.2.3.1. CAT[1:0]

This register is used to select the abrupt transition time. The MIE has two transition times based on image contents for preventing abnormal visible artifacts (e.g. flicker). The MIE controls transition time between CAT and CST automatically in moving mode (MIE_MODE = "11").

- Abrupt transition time : If input image is changed abruptly, short transition time is needed.
- Smooth transition time : If input image is changed smoothly, long transition time is needed.

Table 77. CAT[1:0]

CAT[1:0]	Abrupt Transition Time
00	1 frame
01	2 frames
10	4 frames
11	8 frames

Status	Default Value
Initial	CAT[1:0] = 10

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5.2.3.2. CST[1 :0]

This register is used to select the smooth transition time

Table 78. CST[1:0]

CST[1:0]	Smooth Transition Time
00	32 frames
01	64 frames
10	96 frames
11	128 frames

Status	Default Value
Initial	CST[1:0] = 00

An example of MIE transition time is illustrated as below. If the input image is changed abruptly, the MIE has an abrupt transition time “case (1)” and if the input image is changed smoothly, the MIE has a smooth transition time “case (2)”. The display brightness changes to target brightness abruptly “case (4)” when the abrupt change of image is happened during the smooth transition “case (3)”.

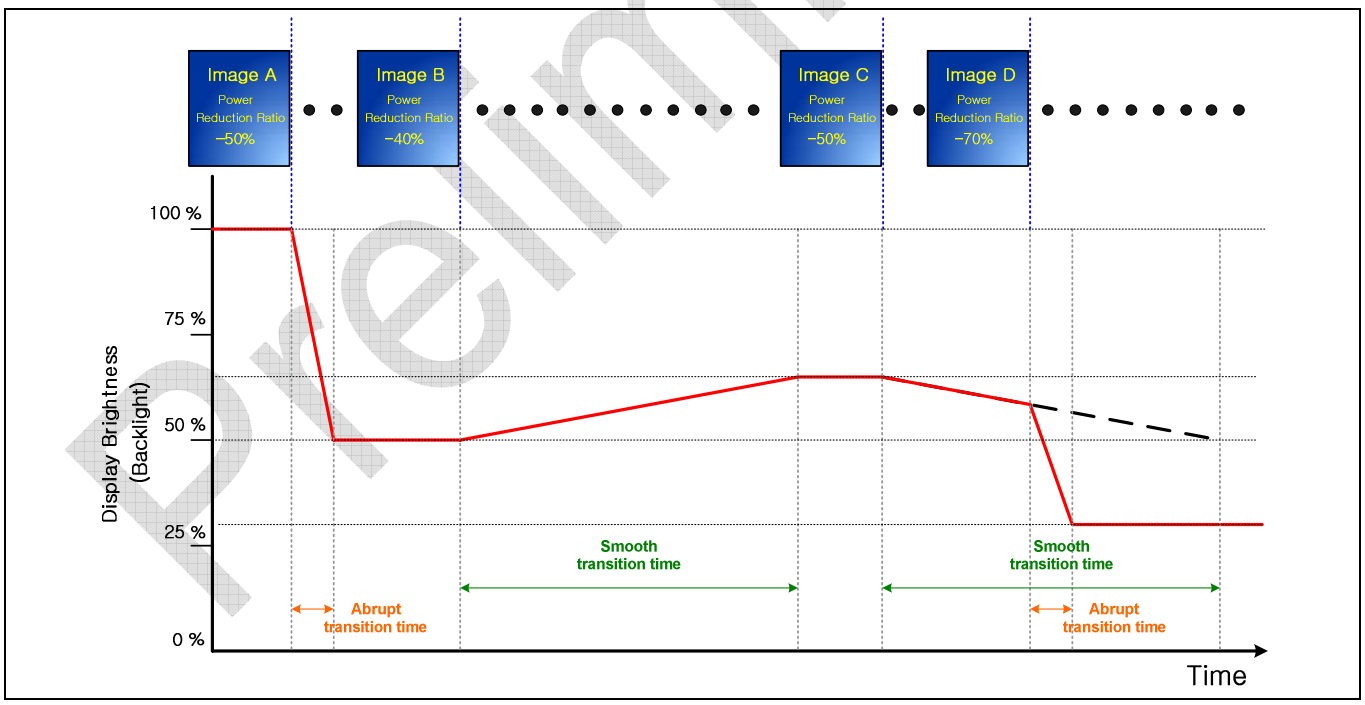

Figure122. Example of MIE transition control

Preliminary

5.2.4. WRBLCTL (C3H)

C3h	WRBLCTL											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	1	C3
1st Parameter	1	1	↑	-	BCFRQ SEL[6]	BCFRQ SEL [5]	BCFRQ SEL [4]	BCFRQ SEL [3]	BCFRQ SEL [2]	BCFRQ SEL [1]	BCFRQ SEL [0]	-
2nd Parameter	1	1	↑	BL_ MODE_ INSLP	-	DT [2]	DT [1]	DT [0]	BL_ DRV_EN	BL_ DIMM_ STEP[1]	BL_ DIMM_ STEP[0]	-

5.2.4.1. BCFRQSEL[6:0]

This register is used to select the frequency of PWM. To select the PWM frequency, two registers are needed. Those register are BCFRQSEL[6:0] and BL_DIMM_STEP[1:0].

For details, refer to the table of PWM frequency.

Status	Default Value
Initial	BCFRQSEL[6:0] = 100_0000

5.2.4.2. BL_DIMM_STEP[1:0]

This register is used to select the dimming step of PWM level. It is used to select the frequency of PWM with BCFRQSEL[6:0].

Table 79. BL_DIMM_STEP[1:0]

BL_DIMM_STEP[1:0]	Dimming Steps of PWM
00	256
01	128
10	64
11	Disable

Status	Default Value
Initial	BL_DIMM_STEP[1:0] = 00

The PWM frequency is calculated with the following formula.

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$$Num.\ of\ PWM\ /\ 1\ frame = (PWM_FRQ_SEL + 1)\ X\ 2^{BL_DIMM_SETP}$$

Figure123. Calculation formula of PWM frequency

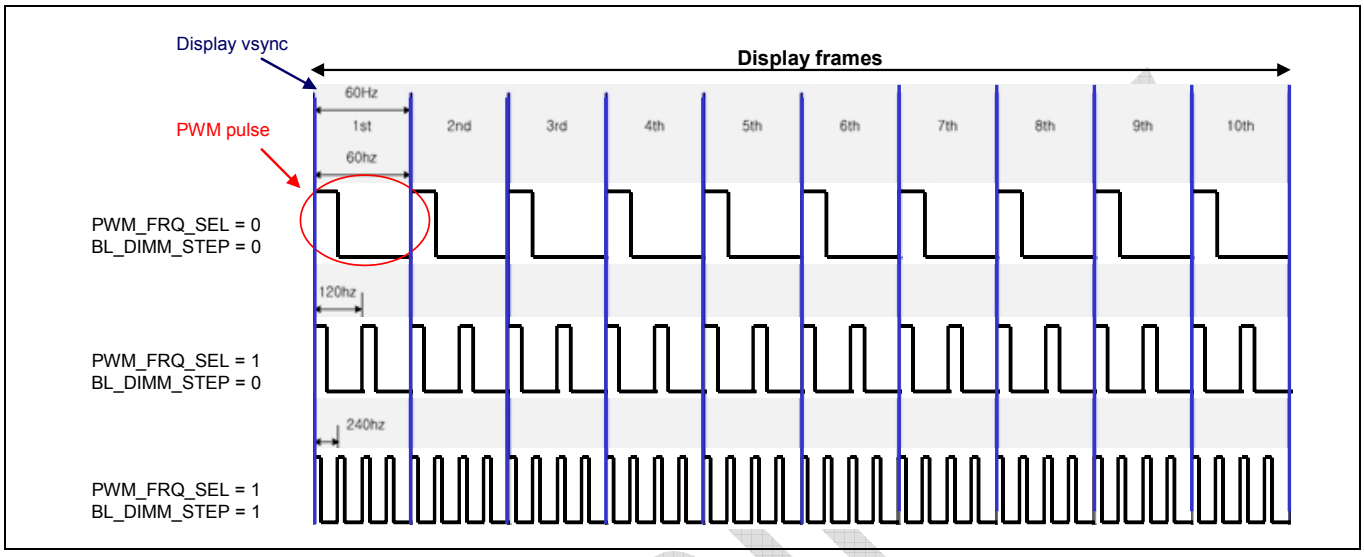

Figure124. Example of PWM frequency selection

Prelim

Table 80. PWM Frequency

		PWM Frequency [Hz]			
	BL_DIMM _STEP[1:0]	00	01	10	11
	Dimming Step No.	256	128	64	32
PWM_FRQ_SEL[6:0]	0000000	F.F. x 1	F.F. x 2	F.F. x 4	
	0000001	F.F. x 2	F.F. x 4	F.F. x 8	
	0000010	F.F. x 3	F.F. x 6	F.F. x 12	
	0000011	F.F. x 4	F.F. x 8	F.F. x 16	
	0000100	F.F. x 5	F.F. x 10	F.F. x 20	
	0000101	F.F. x 6	F.F. x 12	F.F. x 24	
	0000110	F.F. x 7	F.F. x 14	F.F. x 28	
	0000111	F.F. x 8	F.F. x 16	F.F. x 32	
	0001000	F.F. x 9	F.F. x 18	F.F. x 36	
	0001001	F.F. x 10	F.F. x 20	F.F. x 40	
	0001010	F.F. x 11	F.F. x 22	F.F. x 44	
	0001011	F.F. x 12	F.F. x 24	F.F. x 48	
	0001100	F.F. x 13	F.F. x 26	F.F. x 52	
	0001101	F.F. x 14	F.F. x 28	F.F. x 56	
	0001110	F.F. x 15	F.F. x 30	F.F. x 60	
	0001111	F.F. x 16	F.F. x 32	F.F. x 64	
	0010000	F.F. x 17	F.F. x 34	F.F. x 68	
	0010001	F.F. x 18	F.F. x 36	F.F. x 72	
	0010010	F.F. x 19	F.F. x 38	F.F. x 76	
	0010011	F.F. x 20	F.F. x 40	F.F. x 80	
	0010100	F.F. x 21	F.F. x 42	F.F. x 84	
	0010101	F.F. x 22	F.F. x 44	F.F. x 88	
	0010110	F.F. x 23	F.F. x 46	F.F. x 92	
	0010111	F.F. x 24	F.F. x 48	F.F. x 96	
	0011000	F.F. x 25	F.F. x 50	F.F. x 100	
	0011001	F.F. x 26	F.F. x 52	F.F. x 104	
	0011010	F.F. x 27	F.F. x 54	F.F. x 108	
	0011011	F.F. x 28	F.F. x 56	F.F. x 112	
	0011100	F.F. x 29	F.F. x 58	F.F. x 116	
	0011101	F.F. x 30	F.F. x 60	F.F. x 120	
	0011110	F.F. x 31	F.F. x 62	F.F. x 124	
	0011111	F.F. x 32	F.F. x 64	F.F. x 128	
	0100000	F.F. x 33	F.F. x 66	F.F. x 132	
	0100001	F.F. x 34	F.F. x 68	F.F. x 136	
	0100010	F.F. x 35	F.F. x 70	F.F. x 140	
	0100011	F.F. x 36	F.F. x 72	F.F. x 144	
	0100100	F.F. x 37	F.F. x 74	F.F. x 148	
	0100101	F.F. x 38	F.F. x 76	F.F. x 152	
	0100110	F.F. x 39	F.F. x 78	F.F. x 156	
	0100111	F.F. x 40	F.F. x 80	F.F. x 160	
	0101000	F.F. x 41	F.F. x 82	F.F. x 164	
	0101001	F.F. x 42	F.F. x 84	F.F. x 168	
	0101010	F.F. x 43	F.F. x 86	F.F. x 172	
	0101011	F.F. x 44	F.F. x 88	F.F. x 176	
	0101100	F.F. x 45	F.F. x 90	F.F. x 180	
	0101101	F.F. x 46	F.F. x 92	F.F. x 184	
	0101110	F.F. x 47	F.F. x 94	F.F. x 188	
	0101111	F.F. x 48	F.F. x 96	F.F. x 192	
	0110000	F.F. x 49	F.F. x 98	F.F. x 196	
	0110001	F.F. x 50	F.F. x 100	F.F. x 200	
	0110010	F.F. x 51	F.F. x 102	F.F. x 204	
	0110011	F.F. x 52	F.F. x 104	F.F. x 208	
	0110100	F.F. x 53	F.F. x 106	F.F. x 212	
	0110101	F.F. x 54	F.F. x 108	F.F. x 216	
	0110110	F.F. x 55	F.F. x 110	F.F. x 220	
	0110111	F.F. x 56	F.F. x 112	F.F. x 224	
	0111000	F.F. x 57	F.F. x 114	F.F. x 228	
	0111001	F.F. x 58	F.F. x 116	F.F. x 232	
	0111010	F.F. x 59	F.F. x 118	F.F. x 236	
	0111011	F.F. x 60	F.F. x 120	F.F. x 240	
	0111100	F.F. x 61	F.F. x 122	F.F. x 244	
	0111101	F.F. x 62	F.F. x 124	F.F. x 248	
	0111110	F.F. x 63	F.F. x 126	F.F. x 252	
	0111111	F.F. x 64	F.F. x 128	F.F. x 256	

		PWM Frequency [Hz]			
	BL_DIMM _STEP[1:0]	00	01	10	11
	Dimming Step No.	256	128	64	32
PWM_FRQ_SEL[6:0]	1000000	F.F. x 65	F.F. x 130	F.F. x 260	
	1000001	F.F. x 66	F.F. x 132	F.F. x 264	
	1000010	F.F. x 67	F.F. x 134	F.F. x 268	
	1000011	F.F. x 68	F.F. x 136	F.F. x 272	
	1000100	F.F. x 69	F.F. x 138	F.F. x 276	
	1000101	F.F. x 70	F.F. x 140	F.F. x 280	
	1000110	F.F. x 71	F.F. x 142	F.F. x 284	
	1000111	F.F. x 72	F.F. x 144	F.F. x 288	
	1001000	F.F. x 73	F.F. x 146	F.F. x 292	
	1001001	F.F. x 74	F.F. x 148	F.F. x 296	
	1001010	F.F. x 75	F.F. x 150	F.F. x 300	
	1001011	F.F. x 76	F.F. x 152	F.F. x 304	
	1001100	F.F. x 77	F.F. x 154	F.F. x 308	
	1001101	F.F. x 78	F.F. x 156	F.F. x 312	
	1001110	F.F. x 79	F.F. x 158	F.F. x 316	
	1001111	F.F. x 80	F.F. x 160	F.F. x 320	
	1010000	F.F. x 81	F.F. x 162	F.F. x 324	
	1010001	F.F. x 82	F.F. x 164	F.F. x 328	
	1010010	F.F. x 83	F.F. x 166	F.F. x 332	
	1010011	F.F. x 84	F.F. x 168	F.F. x 336	
	1010100	F.F. x 85	F.F. x 170	F.F. x 340	
	1010101	F.F. x 86	F.F. x 172	F.F. x 344	
	1010110	F.F. x 87	F.F. x 174	F.F. x 348	
	1010111	F.F. x 88	F.F. x 176	F.F. x 352	
	1011000	F.F. x 89	F.F. x 178	F.F. x 356	
	1011001	F.F. x 90	F.F. x 180	F.F. x 360	
	1011010	F.F. x 91	F.F. x 182	F.F. x 364	
	1011011	F.F. x 92	F.F. x 184	F.F. x 368	
	1011100	F.F. x 93	F.F. x 186	F.F. x 372	
	1011101	F.F. x 94	F.F. x 188	F.F. x 376	
	1011110	F.F. x 95	F.F. x 190	F.F. x 380	
	1011111	F.F. x 96	F.F. x 192	F.F. x 384	
	1100000	F.F. x 97	F.F. x 194	F.F. x 388	
	1100001	F.F. x 98	F.F. x 196	F.F. x 392	
	1100010	F.F. x 99	F.F. x 198	F.F. x 396	
	1100011	F.F. x 100	F.F. x 200	F.F. x 400	
	1100100	F.F. x 101	F.F. x 202	F.F. x 404	
	1100101	F.F. x 102	F.F. x 204	F.F. x 408	
	1100110	F.F. x 103	F.F. x 206	F.F. x 412	
	1100111	F.F. x 104	F.F. x 208	F.F. x 416	
	1101000	F.F. x 105	F.F. x 210	F.F. x 420	
	1101001	F.F. x 106	F.F. x 212	F.F. x 424	
	1101010	F.F. x 107	F.F. x 214	F.F. x 428	
	1101011	F.F. x 108	F.F. x 216	F.F. x 432	
	1101100	F.F. x 109	F.F. x 218	F.F. x 436	
	1101101	F.F. x 110	F.F. x 220	F.F. x 440	
	1101110	F.F. x 111	F.F. x 222	F.F. x 444	
	1101111	F.F. x 112	F.F. x 224	F.F. x 448	
	1110000	F.F. x 113	F.F. x 226	F.F. x 452	
	1110001	F.F. x 114	F.F. x 228	F.F. x 456	
	1110010	F.F. x 115	F.F. x 230	F.F. x 460	
	1110011	F.F. x 116	F.F. x 232	F.F. x 464	
	1110100	F.F. x 117	F.F. x 234	F.F. x 468	
	1110101	F.F. x 118	F.F. x 236	F.F. x 472	
	1110110	F.F. x 119	F.F. x 238	F.F. x 476	
	1110111	F.F. x 120	F.F. x 240	F.F. x 480	
	1111000	F.F. x 121	F.F. x 242	F.F. x 484	
	1111001	F.F. x 122	F.F. x 244	F.F. x 488	
	1111010	F.F. x 123	F.F. x 246	F.F. x 492	
	1111011	F.F. x 124	F.F. x 248	F.F. x 496	
	1111100	F.F. x 125	F.F. x 250	F.F. x 500	
	1111101	F.F. x 126	F.F. x 252	F.F. x 504	
	1111110	F.F. x 127	F.F. x 254	F.F. x 508	
	1111111	F.F. x 128	F.F. x 256	F.F. x 512	

Note: F.F. means Frame Frequency.

When the display frame frequency is 60Hz, PWM frequency is represented at the table below.

Table 81. Example of PWM Frequency Selection

		PWM Frequency [Hz]			
	BL_DIMM _STEP[1:0]	00	01	10	11
	Dimming Step No.	256	128	64	32
PWM_FRQ_SEL[6:0]	0000000	60	120	240	
	0000001	120	240	480	
	0000010	180	360	720	
	0000011	240	480	960	
	0000100	300	600	1200	
	0000101	360	720	1440	
	0000110	420	840	1680	
	0000111	480	960	1920	
	0001000	540	1080	2160	
	0001001	600	1200	2400	
	0001010	660	1320	2640	
	0001011	720	1440	2880	
	0001100	780	1560	3120	
	0001101	840	1680	3360	
	0001110	900	1800	3600	
	0001111	960	1920	3840	
	0010000	1020	2040	4080	
	0010001	1080	2160	4320	
	0010010	1140	2280	4560	
	0010011	1200	2400	4800	
	0010100	1260	2520	5040	
	0010101	1320	2640	5280	
	0010110	1380	2760	5520	
	0010111	1440	2880	5760	
	0011000	1500	3000	6000	
	0011001	1560	3120	6240	
	0011010	1620	3240	6480	
	0011011	1680	3360	6720	
	0011100	1740	3480	6960	
	0011101	1800	3600	7200	
	0011110	1860	3720	7440	
	0011111	1920	3840	7680	
	0100000	1980	3960	7920	
	0100001	2040	4080	8160	
	0100010	2100	4200	8400	
	0100011	2160	4320	8640	
	0100100	2220	4440	8880	
	0100101	2280	4560	9120	
	0100110	2340	4680	9360	
	0100111	2400	4800	9600	
	0101000	2460	4920	9840	
	0101001	2520	5040	10080	
	0101010	2580	5160	10320	
	0101011	2640	5280	10560	
	0101100	2700	5400	10800	
	0101101	2760	5520	11040	
	0101110	2820	5640	11280	
	0101111	2880	5760	11520	
	0110000	2940	5880	11760	
	0110001	3000	6000	12000	
	0110010	3060	6120	12240	
	0110011	3120	6240	12480	
	0110100	3180	6360	12720	
	0110101	3240	6480	12960	
	0110110	3300	6600	13200	
	0110111	3360	6720	13440	
	0111000	3420	6840	13680	
	0111001	3480	6960	13920	
	0111010	3540	7080	14160	
	0111011	3600	7200	14400	
	0111100	3660	7320	14640	
	0111101	3720	7440	14880	
	0111110	3780	7560	15120	
	0111111	3840	7680	15360	

		PWM Frequency [Hz]			
	BL_DIMM _STEP[1:0]	00	01	10	11
	Dimming Step No.	256	128	64	32
PWM_FRQ_SEL[6:0]	1000000	3900	7800	15600	
	1000001	3960	7920	15840	
	1000010	4020	8040	16080	
	1000011	4080	8160	16320	
	1000100	4140	8280	16560	
	1000101	4200	8400	16800	
	1000110	4260	8520	17040	
	1000111	4320	8640	17280	
	1001000	4380	8760	17520	
	1001001	4440	8880	17760	
	1001010	4500	9000	18000	
	1001011	4560	9120	18240	
	1001100	4620	9240	18480	
	1001101	4680	9360	18720	
	1001110	4740	9480	18960	
	1001111	4800	9600	19200	
	1010000	4860	9720	19440	
	1010001	4920	9840	19680	
	1010010	4980	9960	19920	
	1010011	5040	10080	20160	
	1010100	5100	10200	20400	
	1010101	5160	10320	20640	
	1010110	5220	10440	20880	
	1010111	5280	10560	21120	
	1011000	5340	10680	21360	
	1011001	5400	10800	21600	
	1011010	5460	10920	21840	
	1011011	5520	11040	22080	
	1011100	5580	11160	22320	
	1011101	5640	11280	22560	
	1011110	5700	11400	22800	
	1011111	5760	11520	23040	
	1100000	5820	11640	23280	
	1100001	5880	11760	23520	
	1100010	5940	11880	23760	
	1100011	6000	12000	24000	
	1100100	6060	12120	24240	
	1100101	6120	12240	24480	
	1100110	6180	12360	24720	
	1100111	6240	12480	24960	
	1101000	6300	12600	25200	
	1101001	6360	12720	25440	
	1101010	6420	12840	25680	
	1101011	6480	12960	25920	
	1101100	6540	13080	26160	
	1101101	6600	13200	26400	
	1101110	6660	13320	26640	
	1101111	6720	13440	26880	
	1110000	6780	13560	27120	
	1110001	6840	13680	27360	
	1110010	6900	13800	27600	
	1110011	6960	13920	27840	
	1110100	7020	14040	28080	
	1110101	7080	14160	28320	
	1110110	7140	14280	28560	
	1110111	7200	14400	28800	
	1111000	7260	14520	29040	
	1111001	7320	14640	29280	
	1111010	7380	14760	29520	
	1111011	7440	14880	29760	
	1111100	7500	15000	30000	
	1111101	7560	15120	30240	
	1111110	7620	15240	30480	
	1111111	7680	15360	30720	

5.2.4.3. BL_MODE_IN_SLP

This register is used to select the state of PWM when driver IC is sleep in mode.

Table 82. BL_MODE_IN_SLP

BL_MODE_IN_SLP	State of PWM
0	Low
1	High

Status	Default Value
Initial	BL_MODE_IN_SLP = 0

Table 83. State of PWM

Pin	State					
	Hard Reset	SW Reset	SLPIN		SPLOUT	
			Display On	Display Off	Display On	Display Off
PWM	Low	Low	Fixed as BL_MODE_IN_SLP		Active	Low

5.2.4.4. BL_DRV_EN

This register is used to enable the LED driver IC when the IC needs the chip enable signal.

Table 84. BL_DRV_EN

BL_DRV_EN	State of BL_DRV_EN Pin
0	Low
1	High

Status	Default Value
Initial	BL_DRV_EN = 1

Preliminary

5.2.4.5. DT[2:0]

This register is used to select the transition time of the manual dimming function.

Table 85. DT[2:0]

DT[2:0]	Transition Time	Dimming Step
000	16 frames	16
001	24 frames	24
010	32 frames	32
011	40 frames	40
100	48 frames	48
101	56 frames	56
110	64 frames	64
111	72 frames	72

※ $Transition_Time = (DT[2:0] + 2) \times 8 \times \frac{1}{Display_Frequency}$

Figure125. Transition time of manual dimming function

Status	Default Value
Initial	DT[2:0] = 010

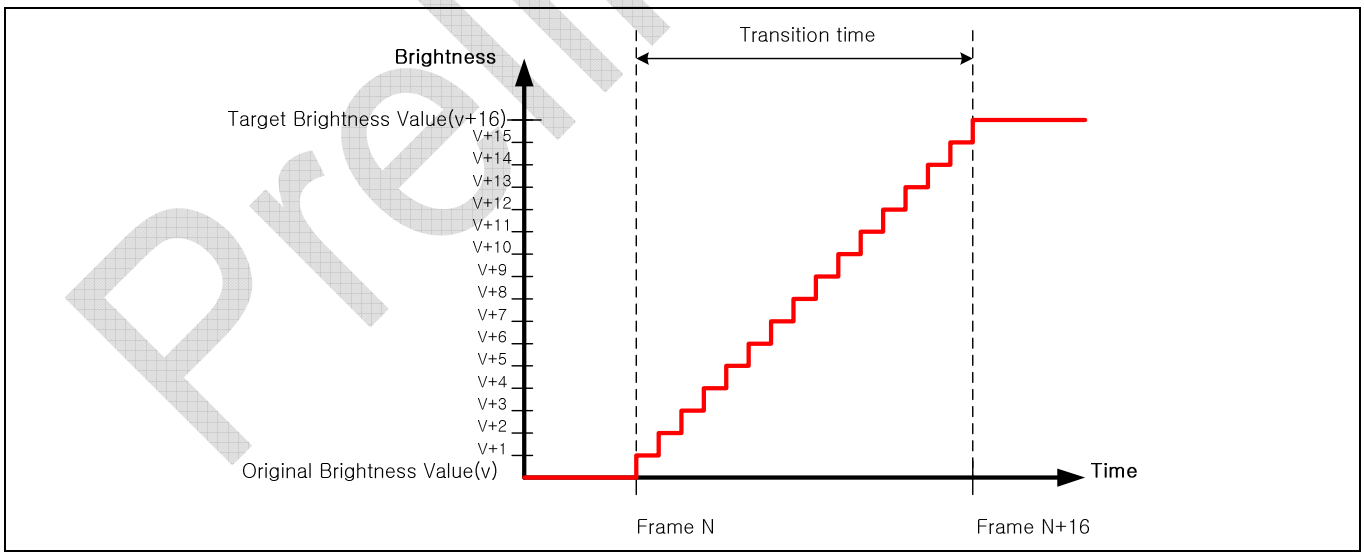

Figure126. Example of dimming function (DT[2:0] = 000)

Preliminary

5.2.5. MTPCTL (D0H)

D0h	MTPCTL (MTP control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	0	0	D0
Parameter	1	1	↑	-	MTP_ MODE	-	RDMTPO FFSET	MTP_ SEL	MTP_ WRB	MTP_ ERB	MTP_ LOAD	-

This command is used to control MTP.

5.2.5.1. MTP_MODE

: Set the 2nd booster operating condition.

MTP_MODE = 0: The 2nd booster operates as a user-specified condition. VGH/VGL voltages are generated as a designated level by BT2-0 setting.

MTP_MODE = 1: Available BT2-0 settings are limited only '101'.

MTP_MODE	MTP operation mode
0	All BT2-0 settings are available (Normal operating condition)
1	Setting of BT2-0 is limited. (An MTP-programming / erasing condition)

Note. Do not execute MTP programming / erasing operation when MTP_MODE = 0.

5.2.5.2. RDMTPOFFSET

: This command selects whether reading data of 4th Parameter(D3h) is VCMOC_PO, VCMOC[4:0] or VCMH_SET[6:0].

RDMTPOFFSET	Reading data of 4th Parameter(D3h)
0	VCMOC_PO, VCMOC[4:0]
1	VCMH_SET[6:0] = VCMH[6:0] ± VCMOC[4:0]

5.2.5.3. MTP_ERB

: This command is a setting for using MTP Data Initialization or Erase.

MTP_ERB	Description
0	MTP Data Initialization or Erase Enable
1	MTP Data Initialization or Erase Disable

Preliminary

5.2.5.4. MTP_LOAD

: This command is a setting for using MTP data load from MTP to post-register.

MTP_LOAD	Description
0	MTP data load disable.
1	MTP data load enable.

5.2.5.5. MTP_SEL

: This command is to select ID1[7:0],ID2[7:0],ID3[7:0], VCMOC_PO, VCMOC[4:0] for using MTP value or register value.

MTP_SEL	Description
0	select ID1[7:0],ID2[7:0],ID3[7:0], VCMOC_PO, VCMOC[4:0] from pre-register value
1	select ID1[7:0],ID2[7:0],ID3[7:0], VCMOC_PO, VCMOC[4:0] from post-register(loaded data from MTP) value

5.2.5.6. MTP_WRB

: This command is used to MTP programming

MTP_WRB	Description
0	MTP writing enable
1	MTP writing disable

Preliminary

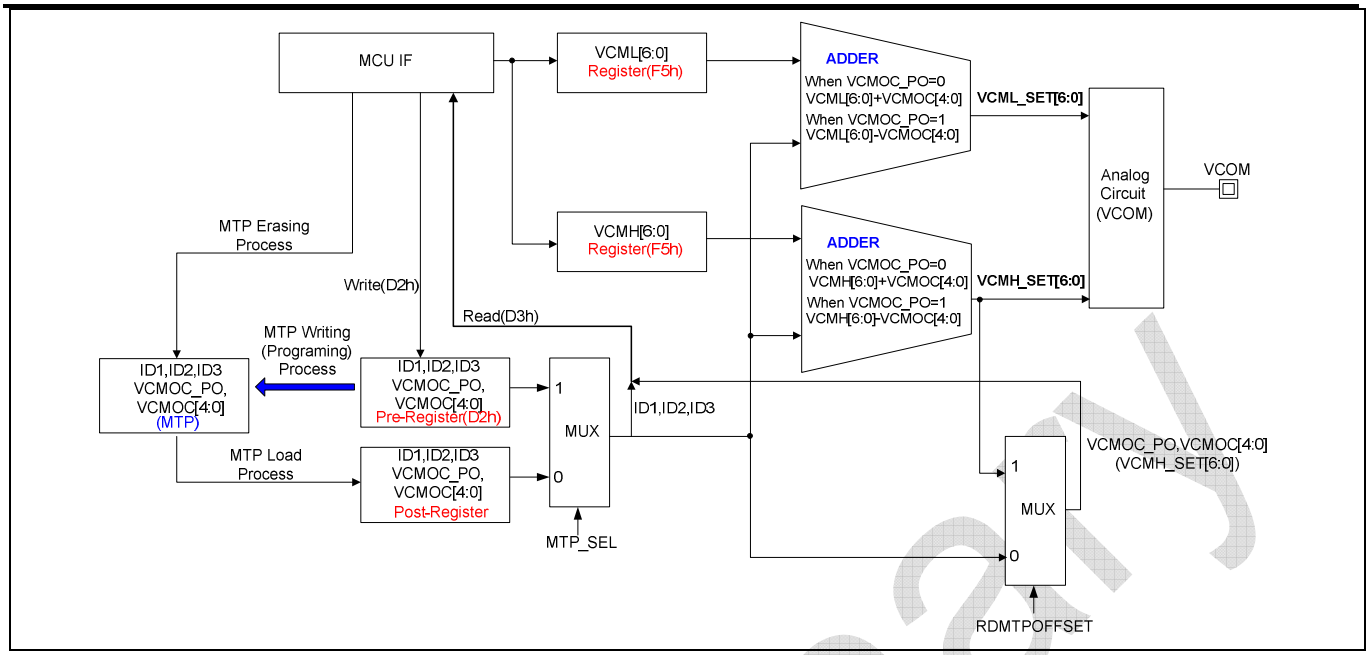

Figure127. MTP block diagram

Status	Default Value
Initial	MTP_MODE = 0, RDMTPOFFSET=0, MTP_SEL=0, MTP_WRB=1,MTP_ERB=1, MTP_LOAD=0

Preliminary

5.2.6. MTPACCS (D2H)

D2h	MTPACCS											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	1	0	D2
1st Parameter	1	1	↑	ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]	-
2nd Parameter	1	1	↑	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]	-

This command writes pre-registers.

5.2.6.1. ADDR[7:0]

This is the address (Parameter) of pre-register. Refer to MTPRD(D3h) command.

Ex) When ADDR[7:0] = 1, This command accesses ID1[7:0] of pre-register.

5.2.6.2. DATA[7:0]

This is the writing data of pre-register.

Status	Default Value
Initial	ADDR[7:0]=00h, DATA[7:0]=00h

Pre-Register table

DATA / Address	D7	D6	D5	D4	D3	D2	D1	D0
1	MTPLOAD _SEL[7]	MTPLOAD _SEL[6]	MTPLOAD _SEL[5]	MTPLOAD _SEL[4]	MTPLOAD _SEL[3]	MTPLOAD _SEL[2]	MTPLOAD _SEL[]	MTPLOAD _SEL[0]
2	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]
3	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]
4	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]
5	-	-	VCMOC_PO	VCMOC [4]	VCMOC [3]	VCMOC [2]	VCMOC [1]	VCMOC [0]
6								
7								
8	-	VHIB_LVL [2]	VHIB_LVL [1]	VHIB_LVL [0]	IREF_LVL [3]	IREF_LVL [2]	IREF_LVL [1]	IREF_LVL [0]
9	MDDI_SET2 [7]	MDDI_SET2 [6]	MDDI_SET2 [5]	MDDI_SET2 [4]	MDDI_SET2 [3]	MDDI_SET2 [2]	MDDI_SET2 [1]	MDDI_SET2 [0]

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10	MIPIIDMS[7]	MIPIIDMS[6]	MIPIIDMS[5]	MIPIIDMS[4]	MIPIIDMS[3]	MIPIIDMS[2]	MIPIIDMS[1]	MIPIIDMS[0]
11	MIPIIDLS[7]	MIPIIDLS[6]	MIPIIDLS[5]	MIPIIDLS[4]	MIPIIDLS[3]	MIPIIDLS[2]	MIPIIDLS[1]	MIPIIDLS[0]

Preliminary

5.2.7. MTPRD (D3H)

After finishing all the erase and program process, users can check the whole MTP content by consecutive reads from this D3h register.

D3h	MTPRD											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	1	1	D3
1st Parameter				MTPLOAD_SEL[7]	MTPLOAD_SEL[6]	MTPLOAD_SEL[5]	MTPLOAD_SEL[4]	MTPLOAD_SEL[3]	MTPLOAD_SEL[2]	MTPLOAD_SEL[]	MTPLOAD_SEL[0]	
2nd Parameter	1	↑	1	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	-
3rd Parameter	1	↑	1	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	-
4th Parameter	1	↑	1	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	-
5th Parameter	1	↑	1	-	-	VCMOC[5]	VCMOC[4]	VCMOC[3]	VCMOC[2]	VCMOC[1]	VCMOC[0]	-
6th Parameter	1	↑	1	-	VCMH[6]	VCMH[5]	VCMH[4]	VCMH[3]	VCMH[2]	VCMH[1]	VCMH[0]	-
7th Parameter	1	↑	1	-	VCML[6]	VCML[5]	VCML[4]	VCML[3]	VCML[2]	VCML[1]	VCML[0]	-
8th Parameter	1	↑	1	-	VHIB_LVL [2]	VHIB_LVL [1]	VHIB_LVL [0]	IREF_LVL[3]	IREF_LVL[2]	IREF_LVL[1]	IREF_LVL[0]	-
9th Parameter	1	↑	1	MDDI_SET2[7]	MDDI_SET2[6]	MDDI_SET2[5]	MDDI_SET2[4]	MDDI_SET2[3]	MDDI_SET2[2]	MDDI_SET2[1]	MDDI_SET2[0]	-
14~37th parameters	1	↑	1	gamma2.2 red values								
38~61th parameters	1	↑	1	gamma2.2 green values								
62~85th parameters	1	↑	1	gamma2.2 blue values								

5.2.7.1. MTP_LOADSEL[7:0]

5.2.7.2. ID1[7:0]

This read byte identifies the LCD module's manufacturer.

5.2.7.3. ID2[7:0]

This read byte identifies the LCD module / driver version ID.

5.2.7.4. ID3[7:0]

This read byte identifies the LCD module/driver.

Preliminary

5.2.7.5. VCMOC[5:0]

This read byte identifies the VCOM Offset.

VCMH_SET[6:0] = VCMH[6:0] ± VCMOC[5:0]

VCML_SET[6:0] = VCML[6:0] ± VCMOC[5:0]

5.2.7.6. IREF_LVL[3:0](1100)

Preliminary

Table 86. VCMOC[5:0]

VCMOC[5:0]	VCM_OFFSET	VCMOC[5:0]	VCM_OFFSET
000000	0	100000	0
000001	+1	100001	-1
000010	+2	100010	-2
000011	+3	100011	-3
000100	+4	100100	-4
000101	+5	100101	-5
000110	+6	100110	-6
000111	+7	100111	-7
001000	+8	101000	-8
001001	+9	101001	-9
001010	+10	101010	-10
001011	+11	101011	-11
001100	+12	101100	-12
001101	+13	101101	-13
001110	+14	101110	-14
001111	+15	101111	-15
010000	+16	110000	-16
010001	+17	110001	-17
010010	+18	110010	-18
010011	+19	110011	-19
010100	+20	110100	-20
010101	+21	110101	-21
010110	+22	110110	-22
010111	+23	110111	-23
011000	+24	111000	-24
011001	+25	111001	-25
011010	+26	111010	-26
011011	+27	111011	-27
011100	+28	111100	-28
011101	+29	111101	-29
011110	+30	111110	-30
011111	+31	111111	-31

For example, if VCMH[6:0] = “1001101”(4.0V) and VCML[6:0] = “1100110”(-0.5V) and VCMOC[5:0] = 100011 are selected, then VCM_OFFSET is “-3,” and therefore VCMH_SET[6:0] is “1001010,” which results in VCOM high level voltage = 3.94V from VCMH[6:0] table, VCML_SET[6:0] is “1100011,” which results in VCOM low level voltage = 0.56V from VCML[6:0] table.

Note that VCMH_SET[6:0]/VCML_SET[6:0] cannot be set to the value above “1111111” or below “0000000,” that is, 128 ≥ VCMH[6:0](VCML[6:0]) + VCMOC[5:0] ≥ 0.

Note: VCMH_SET[6:0] is VCMH[6:0] ± Post-register(VCOMOC) when MTP_SEL=0 and is VCMH[6:0] ± Pre-register(VCOMOC) when MTP_SEL=1. Refer to figure 112. MTP block diagram.

Preliminary

5.2.8. DSTB (DFH)

DFh	DSTB											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	1	1	DF
Parameter	1	1	↑	-	-	-	-	-	-	-	DSTB	-

This command enters deep standby mode. Refer to 4.8 Deep Standby Mode.

Table 87. DSTB

DSTB	State
0	Deep Standby Off
1	Deep Standby In

Status	Default Value
Initial	DSTB = 0

Preliminary

5.2.9. MDDI1 (E7H)

E7h	MDDI1 (MDDI Control 1)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	1	1	1	E7
1st Parameter	1	1	↑			WKL [9]	WKL [8]	WKL [7]	WKL [6]	WKL [5]	WKL [4]	-
2nd Parameter	1	1	↑	WKL [3]	WKL [2]	WKL [1]	WKL [0]	WKF [3]	WKF [2]	WKF [1]	WKF [0]	

When the Parameter (TEST_KEY[7:0]) of this command is inputted by 5Ah, this command enable level 2 command input.

Status	Default Value
Initial	TEST_KEY[7:0]=8'b01011010(5Ah)

5.2.9.1 WKL[9:0]

These register defines the number of line at which the client initiated wakeup starts. If WKL is updated to '000h', client-initialed wakeup up starts automatically at the first line after vertical front porch.

WKL[9:0]

WKL[9:0]	Value
0000000000	Disabled
0000000001	1 H
0000000010	2 H
…..	….
0001000110	70 H
…..	……
1111111110	1022 H
1111111111	1023 H

Status	Default Value
Initial	WKL[9:0] = 0000000000

Preliminary

5.2.9.2 WKF[3:0]

This register defines the number of frame at which the client-initiated wakeup starts. If WKF is updated to '0000h' client-initiated wakeup starts at the beginning of next frame, and if '1111h', wakeup starts after 16th frame.

Set WKF and WKL together for client-initiated wakeup. If WKF is '0011' and WKL is '003h', VBP is '03h', wakeup starts at the first display line of the third frame.

WKF[3:0]

WKF[3:0]	Value
0000	1 V
0001	2 V
0011	3 V
....	....
1000	8 V
....	....
1110	15 V
1111	16 V

Status	Default Value
Initial	WKF[3:0] = 0000 (0)

Preliminary

5.2.10. MDDI2 (E8H)

E8h	MDDI2 (MDDI Control 2)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	0	0	E8
1st parameter	1	1	↑							MDDI_SLP	VWAKE_EN	-

5.2.10.1. MDDI_SLP

: If MDDI_SLP is high, MDDI operation state denotes the STOP state. To release the STOP state, input reset is needed.

MDDI_SLP

MDDI_SLP	State
0	No Action
1	Goto STOP state

Status	Default Value
Initial	MDDI_SLP = 0

5.2.10.2 VWAKE EN

: If VWAKE_EN is high, Client-initiated wakeup is enabled.

VWAKE_EN

VWAKE_EN	State
0	Disabled
1	Enabled

Status	Default Value
Initial	VWAKE_EN = 0

Preliminary

5.2.11. PASSWD1 (F0H)

F0h	Password command for level 2											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	0	F0
1st Parameter	1	1	↑	TEST_KEY[7]	TEST_KEY[6]	TEST_KEY[5]	TEST_KEY[4]	TEST_KEY[3]	TEST_KEY[2]	TEST_KEY[1]	TEST_KEY[0]	-
2nd Parameter	1	1	↑	TEST_KEY[7]	TEST_KEY[6]	TEST_KEY[5]	TEST_KEY[4]	TEST_KEY[3]	TEST_KEY[2]	TEST_KEY[1]	TEST_KEY[0]	-

When the Parameter (TEST_KEY[7:0]) of this command is inputted by 5Ah, this command enable level 2 command input.

Status	Default Value
Initial	TEST_KEY[7:0]=8'b01011010(5Ah)

5.2.12. PASSWD2 (F1H)

F1h	Password command for level 2											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	1	F1
1st Parameter	1	1	↑	TEST_KEY7	TEST_KEY6	TEST_KEY5	TEST_KEY4	TEST_KEY3	TEST_KEY2	TEST_KEY1	TEST_KEY0	-
2nd Parameter	1	1	↑	TEST_KEY7	TEST_KEY6	TEST_KEY5	TEST_KEY4	TEST_KEY3	TEST_KEY2	TEST_KEY1	TEST_KEY0	-

When the Parameter (TEST_KEY[7:0]) of this command is inputted by 5Ah, this command enable level 2 command input.

Status	Default Value
Initial	TEST_KEY[7:0]=8'b01011010(5Ah)

Preliminary

5.2.13. DISCTL (F2H)

F2h	DISCTL (Display Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	1	0	F2
1st Parameter	1	1	↑	-	-	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	-
2nd Parameter	1	1	↑	NHW [7]	NHW [6]	NHW [5]	NHW [4]	NHW [3]	NHW [2]	NHW [1]	NHW [0]	-
3rd Parameter	1	1	↑	-	BLKINV	PINDINV	PNDINV	PIINV	IINV	PINV	NINV	-
4th Parameter	1	1	↑	NVBP [7]	NVBP [6]	NVBP [5]	NVBP [4]	NVBP [3]	NVBP [2]	NVBP [1]	NVBP [0]	-
5th Parameter	1	1	↑	NVFP [7]	NVFP [6]	NVFP [5]	NVFP [4]	NVFP [3]	NVFP [2]	NVFP [1]	NVFP [0]	-
6th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
7th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
8th Parameter	1	1	↑	DIV_SRC [5]	DIV_SRC [4]	DIV_SRC [3]	DIV_SRC [2]	DIV_SRC [1]	DIV_SRC [0]	TE_ST [9]	TE_ST [8]	-
9th Parameter	1	1	↑	TE_ST [7]	TE_ST [6]	TE_ST [5]	TE_ST [4]	TE_ST [3]	TE_ST [2]	TE_ST [1]	TE_ST [0]	-
10th Parameter	1	1	↑	-	-	-	-	-	TE_SEL	TE_ED [9]	TE_ED [8]	-
11th Parameter	1	1	↑	TE_ED [7]	TE_ED [6]	TE_ED [5]	TE_ED [4]	TE_ED [3]	TE_ED [2]	TE_ED [1]	TE_ED [0]	-
12th Parameter	1	1	↑	-	-	-	-	-	-	-	REV	-
13th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
14th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
15th Parameter	1	1	↑	PIHW [7]	PIHW [6]	PIHW [5]	PIHW [4]	PIHW [3]	PIHW [2]	PIHW [1]	PIHW [0]	-
16th Parameter	1	1	↑	PIVBP [7]	PIVBP [6]	PIVBP [5]	PIVBP [4]	PIVBP [3]	PIVBP [2]	PIVBP [1]	PIVBP [0]	-
17th Parameter	1	1	↑	PIVFP [7]	PIVFP [6]	PIVFP [5]	PIVFP [4]	PIVFP [3]	PIVFP [2]	PIVFP [1]	PIVFP [0]	-

Preliminary

5.2.13.1. NL[5:0]

: Set the display duty. The total number of scan line can be set in the range between 8-line and 240-line. A step size is 8-line.

Table 88. NL[5:0]

NL[5:0]	Total number of scan line
000000	Setting disabled
000001	8
000010	16
….	….
011110	240
011110~111111	Setting disabled

Status	Default Value
Initial	NL[5:0] = 011110 (240)

Note: ML (MADCTL D4) setting low when Display size < 240.

5.2.13.2. NHW[7:0]/PIHW[7:0]

: Set the horizontal clock (CL1) period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

Table 89. NHW[7:0]/PIHW[7:0]

*HW[7:0]	Number of internal Clock
00000000~00011010	Setting disabled
00011011	27
00011100	28
…….	……
11111110	254
11111111	255

Note: Internal Clock is 3Mhz clock.

Status	Default Value
Initial	NHW[7:0] = 11000011 (195) PIHW[7:0] =11000011 (195)

Preliminary

5.2.13.3. NINV / PINV / IINV / PIINV / PNDINV / PINDINV / BLKINV

: Select the panel driving method in the Normal mode / Partial mode (display area) / Idle mode / Partial-Idle mode (display area) / Partial mode (non-display area) / Partial-Idle mode (non-display area) / Blanking display, respectively. Either frame inversion method or line inversion method can be selected.

Table 90. NINV/PINV/IINV/PIINV/PNDINV/PINDINV/BLKINV

*INV	Panel driving method
0	Frame inversion
1	Line inversion

Status	Default Value
Initial	NINV, PINV = 1 IINV, PIINV, PNDINV, PINDINV,BLKINV = 0

*non-display area is (porch + non display area) when partial mode.

5.2.13.4. NVBP[7:0]/ PIVBP[7:0]

: Set the vertical back-porch period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

Table 91. NVBP[7.0]/ PIVBP[7.0]

*VBP[7:0]	Number of Horizontal Line
00000000	Setting disable
00000001	Setting disable
00000010	Setting disable
00000011	Setting disable
00000100	Setting disable
00000101	5
…….	……
11111110	254
11111111	255

Status	Default Value
Initial	*BP[7:0] = 00001000 (8)

Preliminary

5.2.13.5. NVFP[7:0]/PIVFP[7:0]

: Set the vertical front-porch period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

Table 92. NVFP[7:0]/PIVFP[7:0]

*VFP[7:0]	Number of Horizontal Line
00000000	Setting disable
00000001	Setting disable
00000010	Setting disable
00000011	Setting disable
00000100	Setting disable
00000101	5
…….	……
11111110	254
11111111	255

Status	Default Value
Initial	*FP[7:0] = 00001000 (8)

Preliminary

5.2.13.6. REV

: Select whether the liquid crystal type is normally white type or normally black type.

Table 93. REV

REV	Liquid crystal type
0	Normally black
1	Normally white

Status	Default Value
Initial	REV = 0

5.2.13.7. DIV_SRC[5:0]

: This controls the period of internal track signal.

Table 94. DIV_SRC[5:0]

DIV_SRC	Track Period(number of oscillator clock or DOTCLK)
000000	Settting disable
…..	…..
000100	Setting disable
000101	5
000110	6
…..	…..
001101	13
001110	14
001111	15
010000	16
010001	17
010010	18
010011	19
…..	….
111111	Setting disable

Status	Default Value
Initial	DIV_SRC [5:0] = 001001

*note : This function is depend on Frame Frequency(HW setting).

Oscillator clock is 9Mhz clock.

Preliminary

5.2.13.8. TE_ST[9:0]

: Select the time when TE signal rises to high level(VDD3).

This command is available when TE_SEL = 1 .

Status	Default Value
Initial	TE_ST[9:0] = 00_1111_1000(248)

5.2.13.9. TE_SEL

: Select whether the liquid crystal type is normally white type or normally black type.

Table 95. TE_SEL

TE_SEL	TE Output Select
0	Level1 TE Ouptut
1	Level2 TE Output

Status	Default Value
Initial	TE_SEL = 0

5.2.13.10. TE_ED[9:0]

: Select the time when TE signal falls to low level(VSS3).

This command is available when TE_SEL = 1 .

Status	Default Value
Initial	TE_ED[9:0] = 00_0000_0111(7)

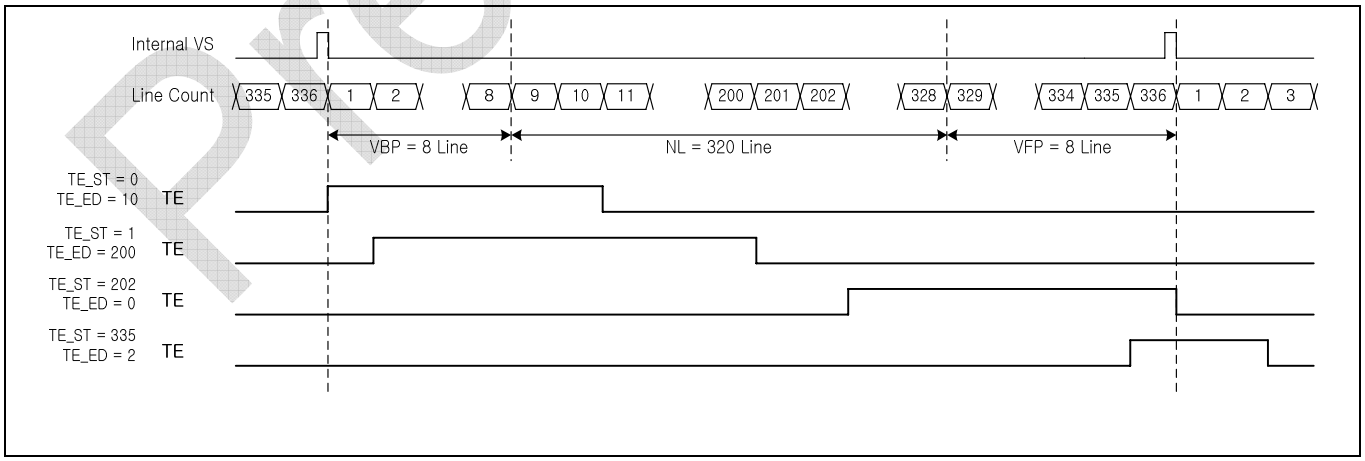

Figure128. TE Timing diagram

Preliminary

5.2.14. MANPWRSEQ (F3H)

F3h	MANPWRSEQ (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	1	1	F3
1st Parameter	1	1	↑	-	-	-	-	-	-	-	APON	-
2nd Parameter	1	1	↑	VCL_EN	VGL_EN	VGH_EN	VGHFREE1_EN	AVDD_EN	VCI1_2ND_EN	VCI1_1ST_EN	VCIR_EN	-
3rd Parameter	1	1	↑	-	-	-	GATE_ON	VCOM_EN	GVDD_EN	VGHFREE2_EN	AVDD2_EN	-
4th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
5th Parameter	1	1	↑	-	-	-	-	-	-	D1	D0	-

5.2.14.1. APON

: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the automatic boosting sequence starter is halted and the booster circuits are operated independently by AVDD_EN, VGH_EN, VGL_EN and VCL_EN bits. In case of APON=1, booster circuits are operated automatically and sequentially.

Status	Default Value
Initial	APON = 1

5.2.14.2. VCIR_EN

: Internal VCIR generation amplifier operation control bit. When VCIR_EN=0, VCIR voltage is not generated.

Status	Default Value
Initial	VCIR_EN = 0

Preliminary

5.2.14.3. VCI1_1ST_EN/VCI1_2ND_EN

: Internal VCI1 generation amplifier operation control bit. When VCI1_1ST_EN=0, VCI1 voltage is not generated.

Status	Default Value
Initial	VCI1_1ST_EN = 0, VCI1_2ND_EN = 0

5.2.14.4. AVDD_EN

: This is an operation-starting bit for the booster circuit1. In case of AVDD_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the AVDD_EN = 1

Status	Default Value
Initial	AVDD_EN = 0

5.2.14.5. VGHFREE1_EN/VGHFREE2_EN

: These are about the booster circuit 2(VGH). These prevent latch-up event.

Status	Default Value
Initial	VGHFREE1_EN = 0,VGHFREE2_EN = 0

5.2.14.6. VGH_EN

: This is an operation-starting bit for the booster circuit 2(VGH). In case of VGH_EN, the circuit is stopped and vice versa. For further information about timing for adjusting to the VGH_EN= 1.

Status	Default Value
Initial	VGH_EN = 0

5.2.14.7. VGL_EN

: This is an operation-starting bit for the booster circuit 2(VGL). In case of VGL_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the VGL_EN = 1.

Status	Default Value
Initial	VGL_EN = 0

Preliminary

5.2.14.8. VCL_EN

: This is an operation-starting bit for the booster circuit 3(VCL). In case of VCL_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the VCL_EN= 1.

Status	Default Value
Initial	VCL_EN = 0

5.2.14.9. VCOM_EN/GVDD_EN

: This is an operation-starting bit for GVDD/VCOM amplifiers. In case of VCOM/_ENVCOM_EN = 0, the amplifier circuits are stopped. On the other hand, the operation of the amplifiers is getting started when VCOM_EN/GVDD_EN = 1. For further information about timing for adjusting to VCOM_EN/GVDD_EN = 1.

Status	Default Value
Initial	VCOM_EN = 0, GVDD_EN = 0

5.2.14.10. GATE_ON

: This is a gate on/off control signal. All gate outputs are set to be gate off level when GATE_ON = 0.
When GATE_ON = 1, gate driver is working: G1 to G320 output is either VGH or VGL level.

Status	Default Value
Initial	GATE_ON = 0

Preliminary

5.2.14.11. D[1:0]

: This controls the status of source, VCOM, gate.

Table 96. D[1:0]

D[1:0]	GATE_ON	Source	VCOM	Gate
00	Don't care	AVSS	AVSS	AVSS
01	0	AVSS	AVSS	VGL
01	1	AVSS	AVSS	Operate
10	0	Binary	Operate	VGL
10	1	Binary	Operate	Operate
11	0	Amplifier	Operate	VGL
11	1	Amplifier	Operate	Operate

Status	Default Value
Initial	D[1:0] = 00

Preliminary

5.2.15. PWRCTL (F4H)

F4h	PWRCTL (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	0	0	F4
1st Parameter	1	1	↑	-	-	-	-	VC[3]	VC[2]	VC[1]	VC[0]	-
2nd Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
3rd Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
4th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
5th Parameter	1	1	↑	-	SEQ2 [2]	SEQ2 [1]	SEQ2 [0]	-	SEQ1 [2]	SEQ1 [1]	SEQ1 [0]	-
6th Parameter	1	1	↑	-	SEQ4 [2]	SEQ4 [1]	SEQ4 [0]	FREE2_SEL-	SEQ3 [2]	SEQ3 [1]	SEQ3 [0]	-
7th Parameter	1	1	↑	-	-	-	-	-	SEQ5 [2]	SEQ5 [1]	SEQ5 [0]	-
8th Parameter	1	1	↑	-	-	BLK_SEL	BLK_OFF	-	-	BLK_FRAME[1]	BLK_FRAM[0]	-
9th Parameter	1	1	↑	-	-	NDC3[1]	NDC3[0]	NDC2[1]	NDC2[0]	NDC1[1]	NDC1[0]	-
10th Parameter	1	1	↑	-	NGVD[6]	NGVD[5]	NGVD[4]	NGVD[3]	NGVD[2]	NGVD[1]	NGVD[0]	-
11th Parameter	1	1	↑	-	-	-	-	-	NBT[2]	NBT[1]	NBT[0]	-
12th Parameter	1	1	↑	-	-	PIDC3[1]	PIDC3[0]	PIDC2[1]	PIDC2[0]	PIDC1[1]	PIDC1[0]	-
13th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
14th Parameter	1	1	↑	-	-	-	-	-	PIBT[2]	PIBT[1]	PIBT[0]	-
15th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
16th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
17th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
18th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
19th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
20th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-

Preliminary

5.2.15.1. VC[3:0]

: This register is used to set the VCI1 voltage. These bits set the VCI1 voltage up to 3V as the nominal output (upper limit value may depend on VCI voltage)

Table 97. VC[3:0]

VC3	VC2	VC1	VC0	VCI1
0	0	0	0	2.100V
0	0	0	1	2.160V
0	0	1	0	2.220V
0	0	1	1	2.280V
0	1	0	0	2.340V
0	1	0	1	2.400V
0	1	1	0	2.460V
0	1	1	1	2.520V
1	0	0	0	2.580V
1	0	0	1	2.640V
1	0	1	0	2.700V
1	0	1	1	2.760V
1	1	0	0	2.820V
1	1	0	1	2.880V
1	1	1	0	2.940V
1	1	1	1	3.000V

Note: Do not set any higher VCI1 level than VCI -0.15V.

Status	Default Value
Initial	VC[3:0] = 1011

Preliminary

5.2.15.2. SEQ1[2:0]

: : This register is used to set the period between from start of AVDD boosting to start of VGH charging (VGHFREE1_EN) when sleep-out command is applied on sleep-in mode. (APON = 1)

Table 98. SEQ1[2:0]

SEQ1[2:0]	VGHFREE1_EN on timing
	Period from AVDD boosting start to VGH charging start (unit : frame=16.7ms)
000	Setting disable
001	1/4
010	2/4
011	3/4
100	1
101	5/4
110	6/4
111	7/4

Status	Default Value
Initial	SEQ1[2:0] = 001

5.2.15.3. SEQ2[2:0]

: This register is used to set the period between from start of VGH charging (VGHFREE1_EN) to start of VGH boosting when sleep-out command is applied on sleep-in mode. (APON = 1)

Table 99. SEQ2[2:0]

SEQ2[2:0]	VGH_EN on timing
	Period from VGH charging start to VGH boosting start (unit : frame=16.7ms)
000	Setting disable
001	Setting disable
010	2/4
011	3/4
100	1
101	5/4
110	6/4
111	7/4

Status	Default Value
Initial	SEQ2[2:0] = 010

Preliminary

5.2.15.4. SEQ3[2:0]

: This register is used to set the period between from start of VGH boosting to start of VGL boosting when sleep-out command is applied on sleep-in mode. (APON = 1)

Table 100. SEQ3[2:0]

SEQ3[2:0]	VGL_EN on timing
	Period from VGH boosting start to VGL boosting start (unit : frame=16.7ms)
000	Setting disable
001	Setting disable
010	Setting disable
011	Setting disable
100	Setting disable
101	Setting disable
110	Setting disable
111	7/4

Status	Default Value
Initial	SEQ3[2:0] = 111

5.2.15.5. FREE2_SEL

: This register is used to set the period between from start of VGH boosting to start of VGHFREE2_EN when sleep-out command is applied on sleep-in mode. (APON = 1).

SEQ3[2:0]	VGHFREE2_EN on timing
	Period from VGH boosting start to VGHFREE2_EN start (unit : frame=16.7ms)
0	Setting disable
1	5/4

Status	Default Value
Initial	FREE2_SEL = 1

5.2.15.6. SEQ4[2:0]

: This register is used to set the period between from start of VGL boosting to VCL boosting when sleep-out command is applied on sleep-in mode. (APON = 1)

Table 101. SEQ4[2:0]

SEQ4[2:0]	VCL_EN on timing
	Period from VGL boosting start to VCL boosting start (unit : frame=16.7ms)
000	Setting disable

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001	Setting disable
010	Setting disable
011	Setting disable
100	1
101	5/4
110	6/4
111	7/4

Status	Default Value
Initial	SEQ4[2:0] = 100

5.2.15.7. SEQ5[2:0]

: This register is used to set the period between from VCL boosting to GVDD/VCOM amplifier turn-on when sleep-out command is applied on sleep-in mode(APON = 1)

Table 102. SEQ5[2:0]

SEQ5[2:0]	VGL_EN on timing
	Period from VCL boosting start to AMP_EN boosting start (unit : frame=16.7ms)
000	Setting disable
001	1/4
010	2/4
011	3/4
100	1
101	5/4
110	6/4
111	7/4

Status	Default Value
Initial	SEQ5[2:0] = 001

5.2.15.8. BLK_SEL

: BLK_SEL selects the source driving method(Amplifier or Binary mode) in blanking display period.

BLK_SEL = 0 : Source operates in amplifier mode in normal display mode, Source operates in binary mode in idle display mode.

BLK_SEL = 1 : Source only operates in binary mode.

Status	Default Value
Initial	BLK_SEL=0

Preliminary

5.2.15.9. BLK_OFF

: BLK_OFF selects whether blanking display uses or not on display off sequence.

BLK_OFF = 0 : Blanking display uses on display off sequence.

BLK_OFF = 1 : Blanking display don't use on display off sequence.

Status	Default Value
Initial	BLK_OFF=0

5.2.15.10. BLK_FRAME[1:0]

: BLK_FRAME[1:0] select the period of blanking display(0~ 3frames) on display on/off sequence.

Status	Default Value
Initial	BLK_FRAME[1:0] = 10 (2frames)

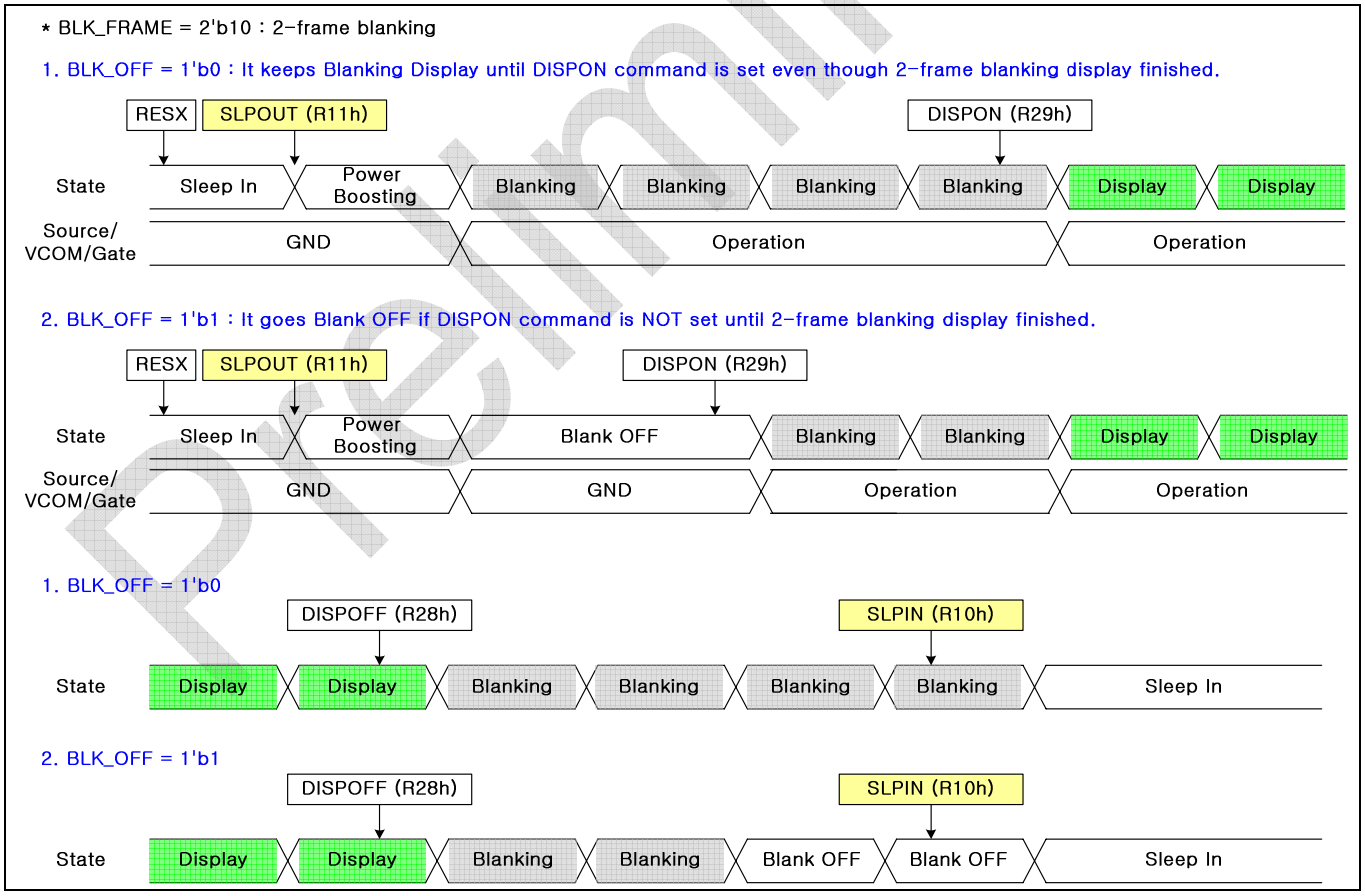


Figure129. BLK_OFF Timing diagram

Preliminary

5.2.15.11. NDC3[1:0] / PIDC3[1:0]

: The operating frequency in the booster circuit 3 is selected. PIDC3 is applied in Idle Partial mode.

Table 103. NDC3[1:0] / PIDC3[1:0]

NDC31/ PIDC31	NDC30/ PIDC30	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK3)
0	0	1:4
0	1	1:2
1	0	1:1
1	1	Setting disabled

Note. DCCLK3 is pumping clock for booster circuit3

Status	Default Value
Initial	NDC3[1:0], PIDC3[1:0] = 10

5.2.15.12. NDC2[1:0] / PIDC2[1:0]

: The operating frequency in the booster circuit 2 is selected. PIDC2 is applied in Idle Partial mode.

Table 104. NDC2[1:0] / PIDC2[1:0]

NDC21/ PIDC21	DC20/ PIDC20	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK2)
0	0	1:2
0	1	1:1
1	0	1:0.5
1	1	1:0.25

Note. DCCLK2 is pumping clock for booster circuit2

Status	Default Value
Initial	NDC2[1:0], PIDC2[1:0] = 10

Preliminary

5.2.15.13. NDC1[1:0] / PIDC1[1:0]

: The operating frequency in the booster circuit1 is selected. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption. PIDC1 is applied in Idle Partial mode.

Table 105.NDC1[1:0] / PIDC1[1:0]

NDC11/ PIDC11	NDC10/ PIDC10	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK1)
0	0	1:4
0	1	1:2
1	0	1:1
1	1	Setting disabled

Note. DCCLK1 is pumping clock for booster circuit1. f(1H) is horizontal frequency (1 raster-row)

Status	Default Value
Initial	NDC1[1:0], PIDC1[1:0] = 10

Preliminary

5.2.15.14. NBT[2:0] / PIBT[2:0]

: The output factor of booster is switched. Adjust scale factor of the booster circuit by the voltage used. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

PIBT is applied in Idle Partial mode.

Table 106. NBT[2:0] / PIBT[2:0]

PIBT1/ NBT2	PIBT1/ NBT1	IPBP0/ NBT0	VGH	VGL	Notes*	
0	0	0	4 X VCI1	-3 X VCI1	11.00V	-8.25V
0	0	1	4 X VCI1	-4 X VCI1	11.00V	-11.00V
0	1	0	5 X VCI1	-3 X VCI1	13.75V	-8.25V
0	1	1	5 X VCI1	-4 X VCI1	13.75V	-11.00V
1	0	0	5 X VCI1	-5 X VCI1	13.75V	-13.75V
1	0	1	6 X VCI1	-3 X VCI1	16.50V	-8.25V
1	1	0	6 X VCI1	-4 X VCI1	16.50V	-11.00V
1	1	1	6 X VCI1	-5 X VCI1	16.50V	-13.75V

Note: The values in table above are example of nominal upper-limit by register setting when VCI1=2.75V.

Do not set any higher VGH level than 16.5V.

Status	Default Value
Initial	PIBT[2:0], NBT[2:0] = 110

Preliminary

5.2.15.15. NGVD[6:0] / PIGVD[6:0]

: This register is used to set the amplifying factor of the GVDD voltage on Normal Mode (the voltage for the Gamma voltage). It allows ranging from 3.26V to 5.00V.

Table 107. NGVD[6:0] / PIGVD[6:0]

NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage
0000000	3.26V	0100000	3.90V	1000000	4.54V	1100000	Inhibit
0000001	3.28V	0100001	3.92V	1000001	4.56V	1100001	Inhibit
0000010	3.30V	0100010	3.94V	1000010	4.58V	1100010	Inhibit
0000011	3.32V	0100011	3.96V	1000011	4.60V	1100011	Inhibit
0000100	3.34V	0100100	3.98V	1000100	4.62V	1100100	Inhibit
0000101	3.36V	0100101	4.00V	1000101	4.64V	1100101	Inhibit
0000110	3.38V	0100110	4.02V	1000110	4.66V	1100110	Inhibit
0000111	3.40V	0100111	4.04V	1000111	4.68V	1100111	Inhibit
0001000	3.42V	0101000	4.06V	1001000	4.70V	1101000	Inhibit
0001001	3.44V	0101001	4.08V	1001001	4.72V	1101001	Inhibit
0001010	3.46V	0101010	4.10V	1001010	4.74V	1101010	Inhibit
0001011	3.48V	0101011	4.12V	1001011	4.76V	1101011	Inhibit
0001100	3.50V	0101100	4.14V	1001100	4.78V	1101100	Inhibit
0001101	3.52V	0101101	4.16V	1001101	4.80V	1101101	Inhibit
0001110	3.54V	0101110	4.18V	1001110	4.82V	1101110	Inhibit
0001111	3.56V	0101111	4.20V	1001111	4.84V	1101111	Inhibit
0010000	3.58V	0110000	4.22V	1010000	4.86V	1110000	Inhibit
0010001	3.60V	0110001	4.24V	1010001	4.88V	1110001	Inhibit
0010010	3.62V	0110010	4.26V	1010010	4.90V	1110010	Inhibit
0010011	3.64V	0110011	4.28V	1010011	4.92V	1110011	Inhibit
0010100	3.66V	0110100	4.20V	1010100	4.94V	1110100	Inhibit
0010101	3.68V	0110101	4.32V	1010101	4.96V	1110101	Inhibit
0010110	3.70V	0110110	4.34V	1010110	4.98V	1110110	Inhibit
0010111	3.72V	0110111	4.36V	1010111	5.00V	1110111	Inhibit
0011000	3.74V	0111000	4.38V	1011000	Inhibit	1111000	Inhibit
0011001	3.76V	0111001	4.40V	1011001	Inhibit	1111001	Inhibit
0011010	3.78V	0111010	4.42V	1011010	Inhibit	1111010	Inhibit
0011011	3.80V	0111011	4.44V	1011011	Inhibit	1111011	Inhibit
0011100	3.82V	0111100	4.46V	1011100	Inhibit	1111100	Inhibit
0011101	3.84V	0111101	4.48V	1011101	Inhibit	1111101	Inhibit
0011110	3.86V	0111110	4.50V	1011110	Inhibit	1111110	Inhibit
0011111	3.88V	0111111	4.52V	1011111	Inhibit	1111111	Inhibit

Note. Don't set any higher GVDD level than AVDD-0.3V

Status	Default Value
Initial	NGVD[5:0] = 0111010 (4.42V) / PIGVD[5:0] = 0111010 (4.42V)

Preliminary

5.2.16. VCMCTL (F5H)

F5h	VCMCTL (VCOM Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	0	1	F5
1st Parameter	1	1	↑	-	-	-	-	-	-	-	VCOMG	-
2nd Parameter	1	1	↑	-	VCMH[6]	VCMH[5]	VCMH[4]	VCMH[3]	VCMH[2]	VCMH[1]	VCMH[0]	-
3rd Parameter	1	1	↑	-	VCML[6]	VCML[5]	VCML[4]	VCML[3]	VCML[2]	VCML[1]	VCML[0]	-
4th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
5th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
6th Parameter	1	1	↑	-	-	-	VCIR1[4]	VCIR1[3]	VCIR1[2]	VCIR1[1]	VCIR1[0]	-
7th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
8th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
9th Parameter	1	1	↑	-	-	-	-	NVC_BLK[1]	NVC_BLK[0]	-	NVC_ND	-
10th Parameter	1	1	↑	-	-	-	-	PIVC_BLK[1]	PIVC_BLK[0]	-	PIVC_ND	-
11th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
12th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-

5.2.16.1. VCOMG

When VCOMG = 1, low level of VCOM signal is to be fixed at VSSA. Therefore, the amplitude of VCOM signal is determined as |VCOMH – VSSA| regardless of VCML setting.

Status	Default Value
Initial	VCOMG = 0

Preliminary

5.2.16.2. VCMH[6:0]

Set the VCOMH voltage (a high level voltage at the Vcom alternating drive), It allows ranging from 2.46V to 5.00V.

Table 108. VCOMH setting

VCMH6-0	VCOMH Voltage	VCMH6-0	VCOMH Voltage	VCMH6-0	VCOMH Voltage	VCMH6-0	VCOMH Voltage
0000000	2.46V	0100000	3.10V	1000000	3.74V	1100000	4.38V
0000001	2.48V	0100001	3.12V	1000001	3.76V	1100001	4.40V
0000010	2.50V	0100010	3.14V	1000010	3.78V	1100010	4.42V
0000011	2.52V	0100011	3.16V	1000011	3.80V	1100011	4.44V
0000100	2.54V	0100100	3.18V	1000100	3.82V	1100100	4.46V
0000101	2.56V	0100101	3.20V	1000101	3.84V	1100101	4.48V
0000110	2.58V	0100110	3.22V	1000110	3.86V	1100110	4.50V
0000111	2.60V	0100111	3.24V	1000111	3.88V	1100111	4.52V
0001000	2.62V	0101000	3.26V	1001000	3.90V	1101000	4.54V
0001001	2.64V	0101001	3.28V	1001001	3.92V	1101001	4.56V
0001010	2.66V	0101010	3.30V	1001010	3.94V	1101010	4.58V
0001011	2.68V	0101011	3.32V	1001011	3.96V	1101011	4.60V
0001100	2.70V	0101100	3.34V	1001100	3.98V	1101100	4.62V
0001101	2.72V	0101101	3.36V	1001101	4.00V	1101101	4.64V
0001110	2.74V	0101110	3.38V	1001110	4.02V	1101110	4.66V
0001111	2.76V	0101111	3.40V	1001111	4.04V	1101111	4.68V
0010000	2.78V	0110000	3.42V	1010000	4.06V	1110000	4.70V
0010001	2.78V	0110001	3.44V	1010001	4.08V	1110001	4.72V
0010010	2.80V	0110010	3.46V	1010010	4.10V	1110010	4.74V
0010011	2.82V	0110011	3.48V	1010011	4.12V	1110011	4.76V
0010100	2.84V	0110100	3.50V	1010100	4.14V	1110100	4.78V
0010101	2.86V	0110101	3.52V	1010101	4.16V	1110101	4.80V
0010110	2.88V	0110110	3.54V	1010110	4.18V	1110110	4.82V
0010111	2.90V	0110111	3.56V	1010111	4.20V	1110111	4.84V
0011000	2.92V	0111000	3.58V	1011000	4.22V	1111000	4.86V
0011001	2.94V	0111001	3.60V	1011001	4.24V	1111001	4.88V
0011010	2.96V	0111010	3.62V	1011010	4.26V	1111010	4.90V
0011011	2.98V	0111011	3.64V	1011011	4.28V	1111011	4.92V
0011100	3.02V	0111100	3.66V	1011100	4.20V	1111100	4.94V
0011101	3.04V	0111101	3.68V	1011101	4.32V	1111101	4.96V
0011110	3.06V	0111110	3.70V	1011110	4.34V	1111110	4.98V
0011111	3.08V	0111111	3.72V	1011111	4.36V	1111111	5.00V

Note. Don't set any higher VCOM high level than AVDD-0.3V. VCOMH voltage should be higher than VCI.

Status	Default Value
Initial	VCMH[6:0] = 100 0110 (3.86V)

Preliminary

5.2.16.3. VCML[6:0]

Set the VCOML voltage (a low level voltage at the Vcom alternating drive), It allows ranging from -2.54V to 0V.

Table 109. VCOML setting

VCML6-0	VCOML Voltage	VCML6-0	VCOML Voltage	VCML6-0	VCOML Voltage	VCML6-0	VCOML Voltage
0000000	-2.54V	0100000	-1.90V	1000000	-1.26V	1100000	-0.62V
0000001	-2.52V	0100001	-1.88V	1000001	-1.24V	1100001	-0.60V
0000010	-2.50V	0100010	-1.86V	1000010	-1.22V	1100010	-0.58V
0000011	-2.48V	0100011	-1.84V	1000011	-1.10V	1100011	-0.56V
0000100	-2.46V	0100100	-1.82V	1000100	-1.18V	1100100	-0.54V
0000101	-2.44V	0100101	-1.80V	1000101	-1.16V	1100101	-0.52V
0000110	-2.42V	0100110	-1.78V	1000110	-1.14V	1100110	-0.50V
0000111	-2.40V	0100111	-1.76V	1000111	-1.12V	1100111	-0.48V
0001000	-2.38V	0101000	-1.74V	1001000	-1.10V	1101000	-0.46V
0001001	-2.36V	0101001	-1.72V	1001001	-1.08V	1101001	-0.44V
0001010	-2.34V	0101010	-1.70V	1001010	-1.06V	1101010	-0.42V
0001011	-2.32V	0101011	-1.68V	1001011	-1.04V	1101011	-0.40V
0001100	-2.30V	0101100	-1.66V	1001100	-1.02V	1101100	-0.38V
0001101	-2.28V	0101101	-1.64V	1001101	-1.00V	1101101	-0.36V
0001110	-2.26V	0101110	-1.62V	1001110	-0.98V	1101110	-0.34V
0001111	-2.24V	0101111	-1.60V	1001111	-0.96V	1101111	-0.32V
0010000	-2.22V	0110000	-1.58V	1010000	-0.94V	1110000	-0.30V
0010001	-2.20V	0110001	-1.56V	1010001	-0.92V	1110001	-0.28V
0010010	-2.18V	0110010	-1.54V	1010010	-0.90V	1110010	-0.26V
0010011	-2.16V	0110011	-1.52V	1010011	-0.88V	1110011	-0.24V
0010100	-2.14V	0110100	-1.50V	1010100	-0.86V	1110100	-0.22V
0010101	-2.12V	0110101	-1.48V	1010101	-0.84V	1110101	-0.20V
0010110	-2.10V	0110110	-1.46V	1010110	-0.82V	1110110	-0.18V
0010111	-2.08V	0110111	-1.44V	1010111	-0.80V	1110111	-0.16V
0011000	-2.06V	0111000	-1.42V	1011000	-0.78V	1111000	-0.14V
0011001	-2.04V	0111001	-1.40V	1011001	-0.76V	1111001	-0.12V
0011010	-2.02V	0111010	-1.38V	1011010	-0.74V	1111010	-0.10V
0011011	-2.00V	0111011	-1.36V	1011011	-0.72V	1111011	-0.08V
0011100	-1.98V	0111100	-1.34V	1011100	-0.70V	1111100	-0.06V
0011101	-1.96V	0111101	-1.32V	1011101	-0.68V	1111101	-0.04V
0011110	-1.94V	0111110	-1.30V	1011110	-0.66V	1111110	-0.02V
0011111	-1.92V	0111111	-1.28V	1011111	-0.64V	1111111	-0.00V

Note. Available setting range of VCOM low level is from VCL+0.5V to 0V.

Status	Default Value
Initial	VCML[6:0] = 0110110 (-0.5V)

Preliminary

5.2.16.4. VCIR1[4:0]

VCI recycling clock cycle of VCOM driver is sustained for the number of clock cycles that is set in VCIR1[4:0].

Note. When VCI Recycling is used. VCOMH level must be larger than VCI level.

Table 110. VCIR1 setting

VCIR14-0	Recycling Period (number of display clock)	VCIR14-0	Recycling Period (number of display clock)
00000	0	10000	64
00001	4	10001	68
00010	8	10010	72
00011	12	10011	76
00100	16	10100	80
00101	20	10101	84
00110	24	10110	88
00111	28	10111	92
01000	32	11000	96
01001	36	11001	100
01010	40	11010	104
01011	44	11011	108
01100	48	11100	112
01101	52	11101	116
01110	56	11110	120
01111	60	11111	124

Status	Default Value
Initial	VCIR1[4:0] = 10010 (72)

5.2.16.5. NVC_BLK/PIVC_BLK

: This register controls VCOM state in porch period.

Table 111. NVC_BLK/PIVC_BLK

VC_BLK	Operation
00	VCOM is GND in porch period.
01	VCOM is GND in porch period.
10	VCOM holds end line polarity in porch period.
11	VCOM is continuously toggled in porch period.

Status	Default Value
Initial	PIVC_BLK[1:0]=00, NVC_BLK[1:0] = 11

Preliminary

5.2.16.6. NVC_ND/PIVC_ND

: This register controls VCOM state in nod-display period.

Table 112. NVC_ND/PIVC_ND

VC_ND	Operation
0	VCOM is the opposite polarity with Source.
1	VCOM is the same polarity with Source.

Status	Default Value
Initial	PIVC_ND =1, NVC_ND = 1

Preliminary

5.2.17. SRCCTL (F6H)

F6h	SRCCTL (Source Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	1	0	F6
1st Parameter	1	1	↑	-	-	-	-	-	SVCIR[2]	SVCIR[1]	SVCIR[0]	-
2nd Parameter	1	1	↑	-	-	-	-	-	-	-	SG	-
3rd Parameter	1	1	↑	-	-	-	-	-	SAP[2]	SAP[1]	SAP[0]	-
4th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
5th Parameter	1	1	↑	-	-	-	-	NSDT[3]	NSDT[2]	NSDT[1]	NSDT[0]	-
6th Parameter	1	1	↑	-	-	-	-	NSR_BLK [1]	NSR_BLK [0]	-	NSR_ND	-
7th Parameter	1	1	↑	-	-	-	-	PISDT[3]	PISDT[2]	PISDT[1]	PISDT[0]	-
8th Parameter	1	1	↑	-	-	-	-	PISR_BL K[1]	PISR_BL K[0]	-	PISR_ND	-
9th Parameter	1	1	↑	-	-	-	-	-	HBLK_SR C[2]	HBLK_SR C[1]	HBLK_SR C[0]	-

5.2.17.1. SVCIR[2 :0]

: This controls the period of source VCI recycling

Table 113.SVCIR[2:0]

SVCIR	Source VCI Recycling Period
000	VCI Recycling Off
001	VCI Recycling On (HBLK_SRC+15*DIV_SRC)
010	VCI Recycling On (HBLK_SRC+16*DIV_SRC)
011	VCI Recycling On (HBLK_SRC+17*DIV_SRC)
100	VCI Recycling On (HBLK_SRC+18*DIV_SRC)
101	VCI Recycling On (HBLK_SRC+19*DIV_SRC)
110	VCI Recycling On (HBLK_SRC+20*DIV_SRC)
111	VCI Recycling On (HBLK_SRC+21*DIV_SRC)

Status	Default Value
Initial	SVCIR[2:0] = 001

Preliminary

5.2.17.2. HBLK_SRC [2:0]

: This controls the high pulse width of internal track0 signal.

Table 114. HB LK_SRC[2:0]

HBLK_SRC[2:0]	Track0 width Period
000	Set disable
001	1 * DIV_SRC
010	2 * DIV_SRC
011	3 * DIV_SRC
100	4 * DIV_SRC
101	5 * DIV_SRC
110	6 * DIV_SRC
111	7 * DIV_SRC

Status	Default Value
Initial	HBLK_SRC [2:0] = 011

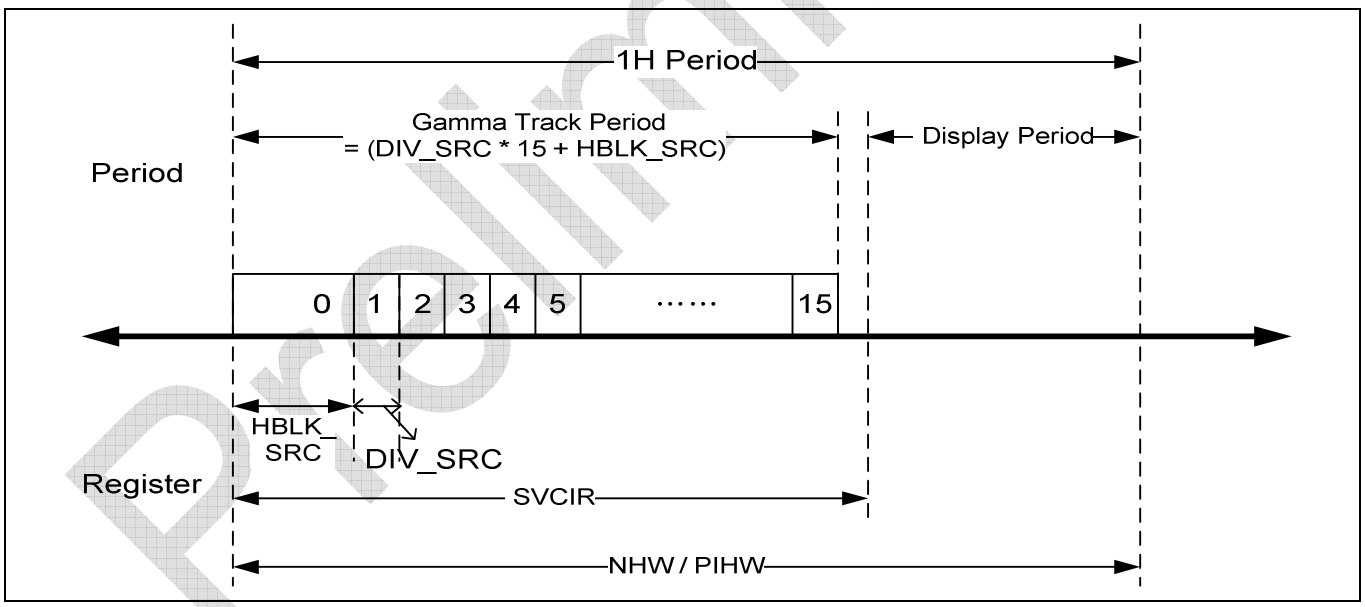


Figure130. 1H period control timing

Preliminary

5.2.17.3. NSR_BLK/PISR_BLK

: This register controls source state in porch period.

Table 115. NSR_BLK/PISR_BLK

SR_BLK	Operation
00	Source is hi-z in porch period.
01	Source is GND in porch period.
10	Source is binary driving mode in porch period.
11	Source is amplifier driving mode in porch period.

Status	Default Value
Initial	PISR_BLK[1:0]=10, NSR_BLK[1:0] = 01

5.2.17.4. NSR_ND/PISR_ND

: This register controls source state in nod-display period.

Table 116. NSR_ND/PISR_ND

SR_ND	Operation
0	Source is binary driving mode in non-display period.
1	Source is amplifier driving mode in non-display period.

Status	Default Value
Initial	PISR_ND =0, NSR_ND = 0

5.2.17.5. SG

: This controls the gamma symmetric axis.

SG = 0 : The adjustment register is to adjust X-axis symmetric of the grayscale voltage.

SG = 1 : The adjustment register is to adjust Y-axis symmetric of the grayscale voltage.

Status	Default Value
Initial	SG = 0

Preliminary

5.2.17.6. SAP[2:0]

: Adjust the slew-rate of the operational amplifier for the source driver. If higher SAP2-0 is set, LCD panel having higher resolution or higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But these bits must be set as adequate value because the amount of fixed current of the operational amplifier is also adjusted. During non-display, when SAP2-0 ="000," operational amplifiers are turned off, so current consumption can be reduced.

Table 117. SAP[2:0]

SAP2	SAP1	SAP0	Source Amp. Current Level	Slew rate of Operational amplifier
0	0	0	Amp. Stop	
0	0	1	Setting Disable	
0	1	0	Setting Disable	
0	1	1	Slow	
1	0	0	Medium Slow 1	
1	0	1	Medium Slow 2	
1	1	0	Medium Slow 3	
1	1	1	Medium Slow 4	

Status	Default Value
Initial	SAP[2:0]= 100

Preliminary

5.2.17.7. NSDT[3:0] / PISDT[3:0]

: This register is used to set delay amount from gate falling(end) to source output. PISDT is applied in Idle Partial mode.

Table 118. NSDT[3:0] / PISDT[3:0]

NSDT3/ PISDT3	NSDT2/ PISDT2	NSDT1/ PISDT1	NSDT0/ PISDT0	Delay amount of the source output		
				Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)	
					18-bit RGB	6-bit RGB
0	0	0	0	Setting Disable	Setting Disable	Setting Disable
0	0	0	1	1 INCLK	2 DOTCLK	2 * 3 DOTCLK
0	0	1	0	2 INCLK	4 DOTCLK	4 * 3 DOTCLK
0	0	1	1	3 INCLK	6 DOTCLK	6 * 3 DOTCLK
0	1	0	0	4 INCLK	8 DOTCLK	8 * 3 DOTCLK
0	1	0	1	5 INCLK	10 DOTCLK	10 * 3 DOTCLK
0	1	1	0	6 INCLK	12 DOTCLK	12 * 3 DOTCLK
0	1	1	1	7 INCLK	14 DOTCLK	14 * 3 DOTCLK
1	0	0	0	8 INCLK	16 DOTCLK	16 * 3 DOTCLK
1	0	0	1	9 INCLK	18 DOTCLK	18 * 3 DOTCLK
1	0	1	0	10 INCLK	20 DOTCLK	20 * 3 DOTCLK
1	0	1	1	11 INCLK	22 DOTCLK	22 * 3 DOTCLK
1	1	0	0	12 INCLK	24 DOTCLK	24 * 3 DOTCLK
1	1	0	1	13 INCLK	26 DOTCLK	26 * 3 DOTCLK
1	1	1	0	14 INCLK	28 DOTCLK	28 * 3 DOTCLK
1	1	1	1	15 INCLK	30 DOTCLK	30 * 3 DOTCLK

Status	Default Value
Initial	PISDT[3:0], NSDT[3:0] = 0100

*note : INCLK is about 3Mhz.

When 18-bit RGB I/F, DOTCLK is about 5~6Mhz.

When 6-bit RGB I/F, DOTCLK is about 15~18Mhz .

Preliminary

5.2.18. IFCTL (F7H)

F7h	IFCTL (Interface Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	1	1	F7
1st Parameter	1	1	↑	MY_EOR	MX_EOR	MV_EOR	-	BGR_EOR	-	GS	SS	-
2nd Parameter	1	1	↑	-	IPM[1]	IPM[0]	MDT[1]	MDT[0]	CM	DM[1]	DM[0]	-
3rd Parameter	1	1	↑	VPL	HPL	DPL	EPL	ENDIAN	-	-	RIM	-
4th Parameter	1	1	↑	RAM_ACCS	-	-	SPR_SEL	-	-	-	-	-

5.2.18.1. MY_EOR / MX_EOR / MV_EOR / BGR_EOR

: Each of these register will be used inside the IC. The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

Status	Default Value
Initial	MY_EOR, MX_EOR, MV_EOR, BGR_EOR = 0

5.2.18.2. GS

: Set the order of Gate Clock generation. When GS = 0, the order of GATE_ON is from G1 to G320, and then GS = 1, from G320 to G1.

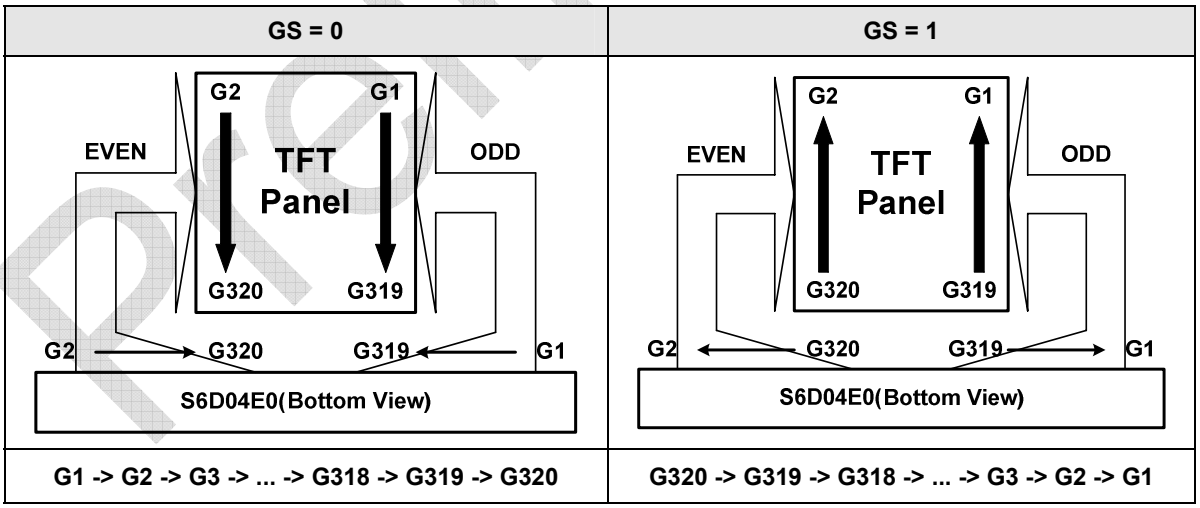


Figure131. Gate Clock order selection

Status	Default Value
Initial	GS = 0

Preliminary

5.2.18.3. SS

: Set the order of Shift Register. When SS = 0, the order of Shift Register is from S1 to S720, and then SS = 1, from S720 to S1.

This command is available when MIE_ON or RAM_ACCS=0 in RGB mode .

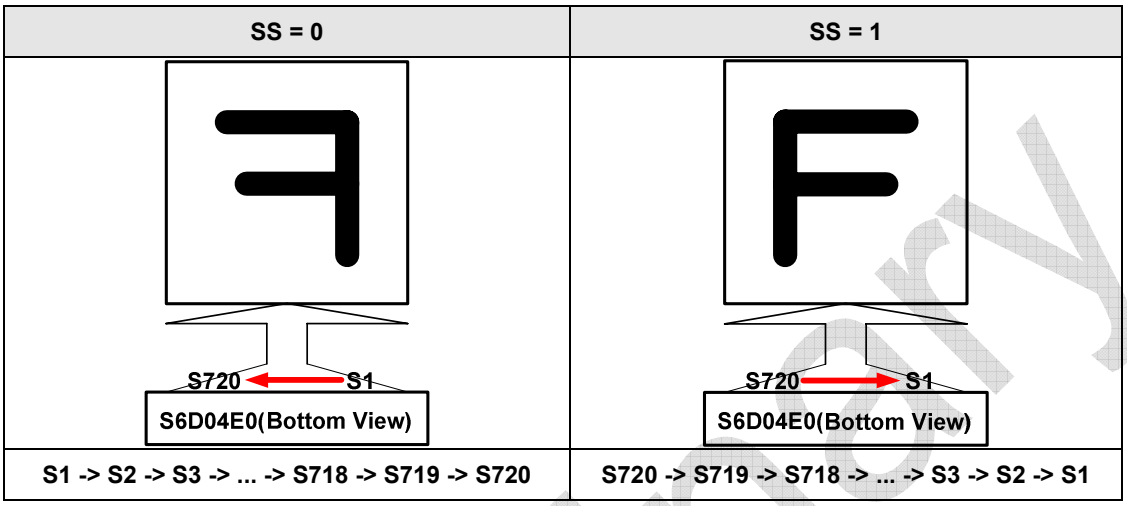


Figure132. Shift Register order selection

Status	Default Value
Initial	SS = 0

5.2.18.4. IPM[2:0]

Controls what value the lowest 1 bits (565→666) are set to in the 65k color mode.

Table 119. IPM[1:0]

IPM1	IPM0	Value of the Lowest 1 Bits in the 65k Color MODE
0	0	Normal 65k color mode operation
0	1	Copy the highest 1-bit
1	0	0
1	1	1

Status	Default Value
Initial	IPM[1:0] = 00

5.2.18.5. MDT[1:0]

: refer to the 3.3 Display Data Format section.

Status	Default Value
Initial	MDT[1:0] = 00

Preliminary

5.2.18.6. DM[1:0]

: Specify the display operation mode. The interface can be set based on the bits of DM. This setting enables switching interface between internal operation and the external display interface.

Table 120. DM[1:0]

DM1	DM0	Display Operation Mode
0	0	CPU interface mode
0	1	RGB interface mode
1	0	VSYNC interface mode
1	1	Setting disabled

Status	Default Value
Initial	DM = 00

5.2.18.7. CM

: Select the color depth conversion (565 → 666) operation.

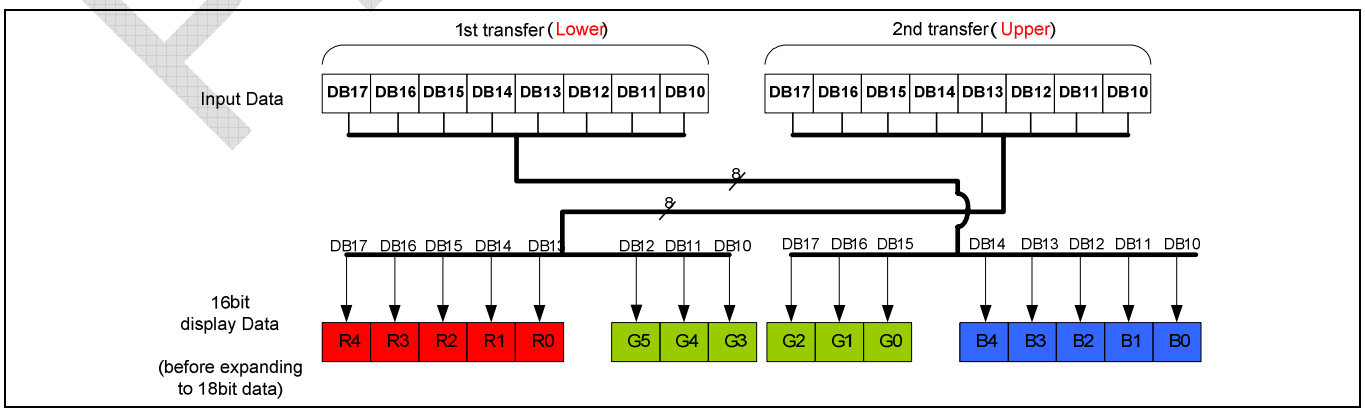
Table 121. CM

CM	Operation Mode
0	IPM
1	LUT

Status	Default Value
Initial	CM = 0

5.2.18.8. ENDIAN

: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.



Preliminary

Figure133. Little endian (65K 8bit I/F type II)

Table 122. ENDIAN

ENDIAN	Data transfer mode
0	Normal (MSB first)
1	Little Endian (LSB first)

Note. Little Endian is valid on only 65K 8bit, 9bit I/F mode.

Status	Default Value
Initial	ENDIAN = 0

Preliminary

5.2.18.9. VPL

: Reverse the polarity of the VSYNC signal.

Table 123. VPL

VPL	Operation
0	VSYNC is low active
1	VSYNC is high active

Status	Default Value
Initial	VPL = 0

5.2.18.10. HPL

: Reverse the polarity of the HSYNC signal.

Table 124. HPL

HPL	Operation
0	HSYNC is low active
1	HSYNC is high active

Status	Default Value
Initial	HPL = 0

5.2.18.11. DPL

: Reverse the polarity of the DOTCLK signal.

Table 125. DPL

DPL	Operation
0	Display data is fetched at DOTCLK's rising edge
1	Display data is fetched at DOTCLK's falling edge

Status	Default Value
Initial	DPL = 0

Preliminary

5.2.18.12. EPL

: Set the polarity of ENABLE pad while using RGB interface.

Table 126. Relationship between EPL, ENABLE and RAM Access

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
0	1	Invalid	Held
1	0	Invalid	Held
1	1	Valid	Update

Status	Default Value
Initial	EPL = 1

5.2.18.13. RIM

: Specify the RGB interface mode when the RGB interface is used. Specifically, this setting specifies the mode when the bit of DM is set to RGB interface. These bits should be set before display operation through the RGB interface and should not be set during operation.

Table 127. RIM

RIM	RGB Interface Mode
0	18-bit RGB interface (one transfer/pixel)
1	6-bit RGB interface (three transfer /pixel)

Status	Default Value
Initial	RIM = 0

You should notice that some display functions, which will be described later, cannot be used according to the display mode shown below.

Table 128. Display functions and display modes

Function	RGB interface	Internal Clock Operation Mode
Partial Display	Cannot be used	Can be used
Scroll Function	Cannot be used	Can be used
Rotation	Cannot be used	Can be used
Mirroring	Cannot be used	Can be used
Window Function	Cannot be used	Can be used

Depending on the external display interface setting, various interfaces can be specified to match the display state. While displaying motion pictures (RGB interface), the data for display can be written in high-speed write mode, which achieves both low power consumption and high-speed access.

Preliminary

5.2.18.14. RAM_ACCS

: Select display data path whether Memory or Shift register when RGB Interface .

Table 129. RAM_ACCS

RAM_ACCS	Display Data Path
0	Shift Register
1	Memory

Status	Default Value
Initial	RAM_ACCS = 0

5.2.18.15. SPR_SEL

: Select the usage of Short Pulse Rejection (SPR) circuit to Logic input signals.

Table 130. SPR_SEL

SPR_SEL	Description
0	Apply SPR circuit
1	Do not apply SPR circuit

Status	Default Value
Initial	SPR_SEL = 0

Preliminary

5.2.19. PANELCTL (F8H)

F8h	PANELCTL (Panel Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	0	0	F8
1st Parameter	1	1	↑	PINO[3]	PINO[2]	PINO[1]	PINO[0]	NNO[3]	NNO[2]	NNO[1]	NNO[0]	-
2nd Parameter	1	1	↑	-	-	SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]	-
3rd Parameter	1	1	↑	-	-	-	-	-	-	-	-	-

5.2.19.1. PINO[3:0] / NNO[3:0]

: Set amount of non-overlap for the gate output. PINO is applied in Idle Partial mode.

Table 131. PINO[3:0] / NNO[3:0]

PINO3 / NNO3	PINO2 / NNO2	PINO1 / NNO1	PINO0 /NNO0	Amount of non-overlap		
				Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)	
					18-bit RGB	6-bit RGB
0	0	0	0	Setting disable	Setting disable	Setting disable
0	0	0	1	3 INCLK	6 DOTCLK	6 *3 DOTCLK
0	0	1	0	6 INCLK	12 DOTCLK	12 *3 DOTCLK
0	0	1	1	9 INCLK	18 DOTCLK	18 *3 DOTCLK
0	1	0	0	12 INCLK	24 DOTCLK	24 *3 DOTCLK
0	1	0	1	15 INCLK	30 DOTCLK	30 *3 DOTCLK
0	1	1	0	18 INCLK	36 DOTCLK	36 *3 DOTCLK
0	1	1	1	21 INCLK	42 DOTCLK	42 *3 DOTCLK
1	0	0	0	24 INCLK	48 DOTCLK	48 *3 DOTCLK
1	0	0	1	27 INCLK	54 DOTCLK	54 *3 DOTCLK
1	0	1	0	30 INCLK	60 DOTCLK	60 *3 DOTCLK
1	0	1	1	33 INCLK	66 DOTCLK	66 *3 DOTCLK
1	1	0	0	36 INCLK	72 DOTCLK	72 *3 DOTCLK
1	1	0	1	39 INCLK	78 DOTCLK	78 *3 DOTCLK
1	1	1	0	42 INCLK	84 DOTCLK	84 *3 DOTCLK
1	1	1	1	45 INCLK	90 DOTCLK	90 *3 DOTCLK

Note: The amount of non-overlap time is defined from starting time of 1H.

Status	Default Value
Initial	PINO[3:0], NNO[3:0] = 0011

Preliminary

5.2.19.2. SCN[5:0]

: Set the gate output start position.

Table 132. SCN[5:0]

SCN[5:0]	Gate Start position	
	GS = 0	GS = 1
000000	G1	G320
000001	G9	G312
000010	G17	G304
….	….	….
100110	G305	G16
100111	G313	G8
101000~111111	Setting disabled	Setting disabled

Status	Default Value
Initial	SCN[5:0] = 000000

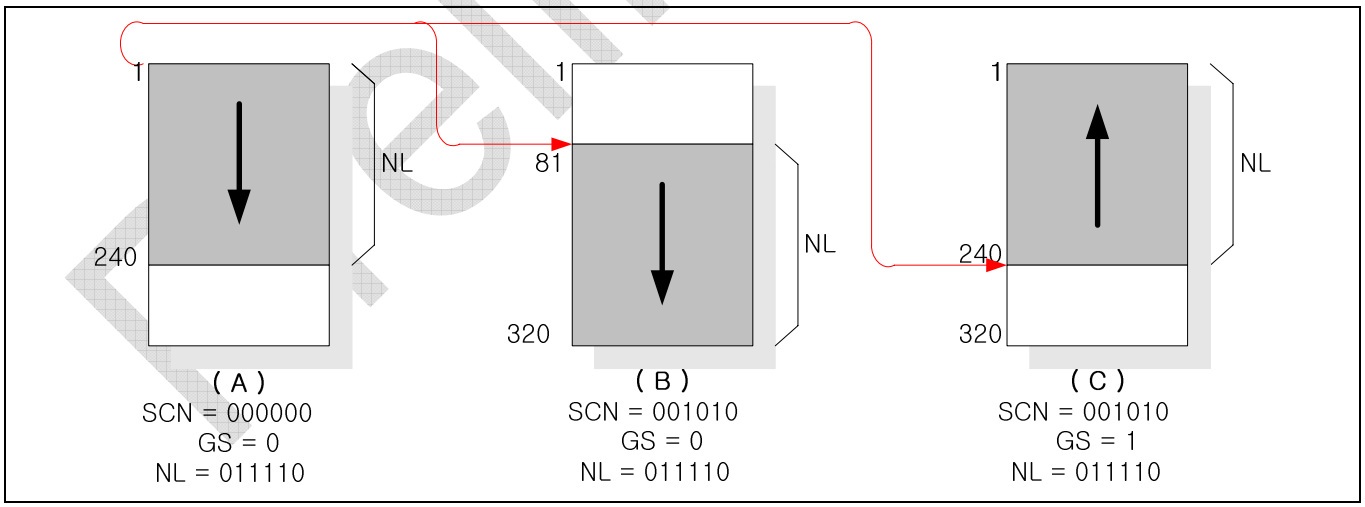


Figure134. SCN

Preliminary

5.2.20. GAMMASEL (F9H)

F9h	GAMMASEL(Gamma Selection)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	0	1	F9
Parameter	1	1	↑	-	-	-	NGF	-	R	G	B	-

5.2.20.1. NGF

: Set the negative polarity gamma register to positive polarity gamma register or user setting value. Refer to the section 4.2

NGF = 0 : negative polarity gamma is applied by the negative polarity gamma register.

NGF = 1 : negative polarity gamma is applied by the same data as positive polarity gamma register.

5.2.20.2. R,G,B

: These register selects the RBG seperate gamma register. Refer to the section 4.2

Table 133. R,G,B

R	G	B	Selected gamma preset register
1	0	0	Red gamma preset register is selected.
0	1	0	Green gamma preset register is selected.
0	0	1	Blue gamma preset register is selected.
1	1	0	Red/Green gamma preset register is selected.
0	1	1	Green/Bule gamma preset register is selected.
1	0	1	Red/Bule gamma preset register is selected.
1	1	1	Red/Green/Blue gamma preset register is selected.
others			Setting disable

Status	Default Value
Initial	NGF = 0, R = 1, G =0, B = 0

Preliminary

5.2.21. PGAMMACTL (FAH)

FAh	PGAMMACTL (Positive Gamma Control Register)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	0	FA
1st Parameter	1	1	↑	-	-	RFP[5]	RFP[4]	RFP[3]	RFP[2]	RFP[1]	RFP[0]	--
2nd Parameter	1	1	↑	-	-	OSP[5]	OSP[4]	OSP[3]	OSP[2]	OSP[1]	OSP[0]	--
3rd Parameter	1	1	↑	-	-	PKP0[5]	PKP0[4]	PKP0[3]	PKP0[2]	PKP0[1]	PKP[0]	--
4th Parameter	1	1	↑	-	-	PKP1[5]	PKP1[4]	PKP1[3]	PKP1[2]	PKP1[1]	PKP1[0]	--
5th Parameter	1	1	↑	-	-	PKP2[5]	PKP2[4]	PKP2[3]	PKP2[2]	PKP2[1]	PKP2[0]	--
6th Parameter	1	1	↑	-	-	PKP3[5]	PKP3[4]	PKP3[3]	PKP3[2]	PKP3[1]	PKP3[0]	--
7th Parameter	1	1	↑	-	-	PKP4[5]	PKP4[4]	PKP4[3]	PKP4[2]	PKP4[1]	PKP4[0]	--
8th Parameter	1	1	↑	-	-	PKP5[5]	PKP5[4]	PKP5[3]	PKP5[2]	PKP5[1]	PKP5[0]	--
9th Parameter	1	1	↑	-	-	PKP6[5]	PKP6[4]	PKP6[3]	PKP6[2]	PKP6[1]	PKP6[0]	--
10th Parameter	1	1	↑	-	-	PKP7[5]	PKP7[4]	PKP7[3]	PKP7[2]	PKP7[1]	PKP7[0]	--
11th Parameter	1	1	↑	-	-	PKP8[5]	PKP8[4]	PKP8[3]	PKP8[2]	PKP8[1]	PKP8[0]	--
12th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
13th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
14th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
15th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
16th Parameter	1	1	↑	-	-	-	-	-	-	GLP[1]	GLP[0]	--

This command is used to set the gamma preset register for positive.

GLP[1:0] : The positive voltage of grayscale number from V1 or V62 is mainly adjusted.

RFP[5:0] : The positive voltage of grayscale number from V0 is mainly adjusted.

OSP[5:0] : The positive voltage of grayscale number from V63 is mainly adjusted.

PKP0[5:0] ~ PKP10[5:0] : The positive voltage of grayscale number from V1 to V62 is finely adjusted.

Table 134. Gamma preset for positive

Status	Default Value
Initial	RFP[5:0],OSP[5:0],PKP0[5:0]~PKP8[5:0],GLP[1:0] 00h,00h,0Ah,14h,25h,34h,2Bh,22h,28h,27h,20h,00h,00h

Preliminary

5.2.22. NGAMMACTL (FBH)

FBh	NGAMMACTL (Negative Gamma Control Register)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	0	FB
1st Parameter	1	1	↑	-	-	RFN[5]	RFN[4]	RFN[3]	RFN[2]	RFN[1]	RFN[0]	--
2nd Parameter	1	1	↑	-	-	OSN[5]	OSN[4]	OSN[3]	OSN[2]	OSN[1]	OSN[0]	--
3rd Parameter	1	1	↑	-	-	PKN0[5]	PKN0[4]	PKN0[3]	PKN0[2]	PKN0[1]	PKN[0]	--
4th Parameter	1	1	↑	-	-	PKN1[5]	PKN1[4]	PKN1[3]	PKN1[2]	PKN1[1]	PKN1[0]	--
5th Parameter	1	1	↑	-	-	PKN2[5]	PKN2[4]	PKN2[3]	PKN2[2]	PKN2[1]	PKN2[0]	--
6th Parameter	1	1	↑	-	-	PKN3[5]	PKN3[4]	PKN3[3]	PKN3[2]	PKN3[1]	PKN3[0]	--
7th Parameter	1	1	↑	-	-	PKN4[5]	PKN4[4]	PKN4[3]	PKN4[2]	PKN4[1]	PKN4[0]	--
8th Parameter	1	1	↑	-	-	PKN5[5]	PKN5[4]	PKN5[3]	PKN5[2]	PKN5[1]	PKN5[0]	--
9th Parameter	1	1	↑	-	-	PKN6[5]	PKN6[4]	PKN6[3]	PKN6[2]	PKN6[1]	PKN6[0]	--
10th Parameter	1	1	↑	-	-	PKN7[5]	PKN7[4]	PKN7[3]	PKN7[2]	PKN7[1]	PKN7[0]	--
11th Parameter	1	1	↑	-	-	PKN8[5]	PKN8[4]	PKN8[3]	PKN8[2]	PKN8[1]	PKN8[0]	--
12th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
13th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
14th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
15th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
16th Parameter	1	1	↑	-	-	-	-	-	-	GLN[1]	GLN[0]	--

This command is used to set the gamma preset register for negative.

GLN[1:0] : The negative voltage of grayscale number from V1 or V62 is mainly adjusted.

RFN[5:0] : The negative voltage of grayscale number from V0 is mainly adjusted.

OSN[5:0] : The negative voltage of grayscale number from V63 is mainly adjusted.

PKN0[5:0] ~ PKN10[5:0] : The negative voltage of grayscale number from V1 to V62 is finely adjusted.

Table 135. Gamma preset for negative

Status	Default Value
Initial	RFN[5:0],OSN[5:0],PKN0[5:0]~PKN8[5:0],GLN[1:0] 00h,0Ah,0Ah,14h,19h,27h,27h,24h,2Ah,29h,20h,00h,00h

Preliminary

5.3. DESCRIPTION OF LEVEL 3 COMMAND

Table 136. List of level 3 command

Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
CAh	MIEFIXED	W	1	MIE control
CBh	MIE_READ	R	2	MIE control
CCh	MIEMODECTL	W	1	MIE control
CDh	MIEACCS	W	2	MIE control
CEh	MIE_TEST	W	3	MIE control
CFh	RDTESTDO	R	2	MIE control
FCh	PASSWD3	W	2	Test key command for level 3
FDh	ANALOGTEST	W	11	Analog test command for level 3
FEh	LOGICTEST	W	3	Logic test command for level 3
FFh	EDSTEST	W	4	EDS test command for level 3

Preliminary

5.3.1. MIEFIXED (CAH)

CAh	MIEFIXED											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	1	0	CA
Parameter	1	1	↑	-	-	-	-	-	-	-	MIEFIXED	-

MIEFIXED : Default value is Low. If this register becomes enable, BC_SAVE and TMF_GAIN value of regardless MIE MODE are fixed to metal fix value.

5.3.2. MIE_READ (CBH)

This command indicates the current status of the MIE registers as described in the below

CBh	MIE_READ											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	1	1	CB
1st Parameter	1	↑	1	MIEBR [7]	MIEBR [6]	MIEBR [5]	MIEBR [4]	MIEBR [3]	MIEBR [2]	MIEBR [1]	MIEBR [0]	-
2nd Parameter	1	↑	1	TMFPRE [3]	TMFPRE [2]	TMFPRE [1]	TMFPRE [0]	TMFCUR [3]	TMFCUR [2]	TMFCUR [1]	TMFCUR [0]	-

MIEBR : Brightness value of only MIE.

TMFPRE : TMF value of previous frame.

TMECUR : TMF value of current frame.

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5.3.3. MIEMODECTL (CCH)

CCh	MIEMODECTL											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	1	0	0	CC
Parameter	1	1	↑	-	-	-	-	SEL_MODE	BCSV_TMF	MIEMODE [1]	MIEMODE [0]	-

If you control TMF_GAIN or BC_SAVE value, you use there register.

SEL_MODE : If you use register value of TMF_GAIN and BC_SAVE, you have to this register enabled.

BCSV_TMF : Select BC_SAVE or TMF_GAIN.

MIEMODE : Select UI, STILL, MOVE mode.

5.3.3.1. MIE_MODE[1:0]

Table 137. MIE_MODE[1:0]

MIE_MODE[1:0]	Operation Mode
0	Off (default)
1	UI (User Interface)
2	Still Image
3	Moving Image

Preliminary

5.3.4. MIEACCS (CDH)

CDh	MIEACCS											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	1	0	1	CD
1st Parameter	1	1	↑	-	-	-	-	MIEADDR [3]	MIEADDR [2]	MIEADDR [1]	MIEADDR [0]	-
2nd Parameter	1	1	↑	MIEDATA [7]	MIEDATA [6]	MIEDATA [5]	MIEDATA [4]	MIEDATA [3]	MIEDATA [2]	MIEDATA [1]	MIEDATA [0]	-

If you control TMF_GAIN or BC_SAVE value, you use there register.

MIEADDR : Select address of BC_SAVE or TMF_GAIN.

MIEDATA : Setting value of BC_SAVE or TMF_GAIN.

If you chage the BC_SAVE_U10 value to 80h, you have to SEL_MODE and BCSV_TMF set high, MIE_MODE set 1, MIEADDR set 10 and MIEDATA set 80h.

5.3.5. MIE_TEST (CEH)

CEh	MIE_TEST											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	1	1	0	CE
1st Parameter	1	1	↑	-	-	TEST_ MODE [3]	TEST_ MODE [2]	TEST_ MODE [1]	TEST_ MODE [0]	TESTDI [17]	TESTDI [16]	-
2nd Parameter	1	1	↑	TESTDI [15]	TESTDI [14]	TESTDI [13]	TESTDI [12]	TESTDI [11]	TESTDI [10]	TESTDI [9]	TESTDI [8]	-
3rd Parameter	1	1	↑	TESTDI [7]	TESTDI [6]	TESTDI [5]	TESTDI [4]	TESTDI [3]	TESTDI [2]	TESTDI [1]	TESTDI [0]	-

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5.3.5.1. TEST_MODE[3:0]

Table 138. TEST_MODE[3:0]

TEST_MODE[3:0]	Operation Mode
4'b0000	TM_NORMAL, Not test mode
4'b0010	TM_CDF_WRITE, Direct CDF register write
4'b0011	TM_CDF_READ, Direct CDF register read
4'b0100	TM_TMF_WRITE, Direct TMF register write
4'b0101	TM_TMF_READ, Direct TMF register read
4'b0110	TM_LPF_WRITE, Direct LPF register write
4'b0111	TM_LPF_READ, Direct LPF register read
4'b1000	TM_CNT_WRITE, Direct CNT register write
4'b1001	TM_CNT_READ, Direct CNT register read
4'b1010	TM_CTRL_GEN, Direct Control Signal write
4'b1111	TM_NOP, No operation

TESTDI : Write data when TEST_MODE is write mode.

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5.3.6. RDTESTDO (CFH)

CFh	RDTESTDO											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	1	1	1	CF
1st Parameter	1	↑	1	TESTDO [15]	TESTDO [14]	TESTDO [13]	TESTDO [12]	TESTDO [11]	TESTDO [10]	TESTDO [9]	TESTDO [8]	-
2nd Parameter	1	↑	1	TESTDO [7]	TESTDO [6]	TESTDO [5]	TESTDO [4]	TESTDO [3]	TESTDO [2]	TESTDO [1]	TESTDO [0]	-

TESTDO : Read data when TEST_MODE is read mode.

5.3.7. PASSWD3 (FCH)

FCh	Password command for level 3											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	0	0	FC
1st Parameter	1	1	↑	TEST_KEY[7]	TEST_KEY[6]	TEST_KEY[5]	TEST_KEY[4]	TEST_KEY[3]	TEST_KEY[2]	TEST_KEY[1]	TEST_KEY[0]	-
2nd Parameter	1	1	↑	TEST_KEY[7]	TEST_KEY[6]	TEST_KEY[5]	TEST_KEY[4]	TEST_KEY[3]	TEST_KEY[2]	TEST_KEY[1]	TEST_KEY[0]	-

When the Parameter (TEST_KEY[7:0]) of this command is inputted by 5Ah, this command enable level 3 command input.

Status	Default Value
Initial	TEST_KEY[7:0]=8'b10100101(A5h)

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5.3.8. ANALOGTEST (FDH)

FDh	Analog Test Command											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	0	1	FD
1st Parameter	1	1	↑	VCL_OFF	VGL_OFF	VGH_OFF	VGHFREE1_OFF	AVDD_OFF	VCI1_2ND_OFF	VCI1_1ST_OFF	VCIR_OFF	-
2nd Parameter	1	1	↑	-	SDFREE_OFF	VGLFREE_OFF	GATE_OFF	VCOM_OFF	GVDD_OFF	VGHFREE2_OFF	AVDD2_OFF	-
3rd Parameter	1	1	↑	-	IGVDD2[2]	IGVDD2[1]	IGVDD2[0]	-	IGVDD1[2]	IGVDD1[1]	IGVDD1[0]	-
4th Parameter	1	1	↑	-	IVCOM2[2]	IVCOM2[1]	IVCOM2[0]	-	IVCOM1[2]	IVCOM1[1]	IVCOM1[0]	-
5th Parameter	1	1	↑	-	-	VCLOPEN_EN	VGHDT_EN	GVDD_HIZ	AB	VREF_EN	VCIREX_EN	-
6th Parameter	1	1	↑	-	-	-	-	TST_VCM[2]	TST_VCM[1]	TST_VCM[0]	VCOM_MODE	-
7th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
8th Parameter	1	1	↑	GAM_TEST	GSAP[2]	GSAP[1]	GSAP[0]	HGLSR_SET[1]	HGLSR_SET[0]	HSR_SET[1]	HSR_SET[0]	-
9th Parameter	1	1	↑	STV_SEL[1]	STV_SEL[0]	-	TH_SEL	-	-	TRACK_SRC[1]	TRACK_SRC[0]	-
10th Parameter	1	1	↑	OSC_TEST	-	-	NFOSC[4]	NFOSC[3]	NFOSC[2]	NFOSC[1]	NFOSC[0]	-
11th Parameter	1	1	↑	-	-	-	PIFOSC[4]	PIFOSC[3]	PIFOSC[2]	PIFOSC[1]	PIFOSC[0]	-

VCIR_OFF : When VCIR_OFF = 1, set VCIR_EN to “L” in auto power sequence.

VCI1_1ST_OFF : When VCI1_1ST_OFF = 1, set VCI1_1ST_EN to “L” in auto power sequence.

VCI1_2ND_OFF : When VCI1_2ST_OFF = 1, set VCI1_2ST_EN to “L” in auto power sequence.

AVDD_OFF : When AVDD_OFF = 1, set AVDD_EN to “L” in auto power sequence.

VGHFREE1_OFF : When VGHFREE1_OFF = 1, set VGHFREE1_EN to “L” in auto power sequence.

VGH_OFF : When VGH_OFF = 1, set VGH_EN to “L” in auto power sequence.

VGL_OFF : When VGL_OFF = 1, set VGL_EN to “L” in auto power sequence.

VCL_OFF : When VCL_OFF = 1, set VCL_EN to “L” in auto power sequence.

AVDD2_OFF : When AVDD2_OFF = 1, set AVDD2_EN to “L” in auto power sequence.

VGHFREE2_OFF : When VGHFREE2_OFF = 1, set VGHFREE2_EN to “L” in auto power sequence.

GVDD_OFF : When GVDD_OFF = 1, set GVDD_EN to “L” in auto power sequence.

VCOM_OFF : When VCOM_OFF = 1, set VCOM_EN to “L” in auto power sequence.

VGHFREE2_OFF : When VGHFREE2_OFF = 1, set VGHFREE2_EN to “L” in auto power sequence.

GATE_OFF : When GATE_OFF = 1, set GON to “L” in auto power sequence.

VGLFREE_OFF : When VGLFREE_OFF = 1 , disable schottky free mode. This is valid only when APON = 1.

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SDFREE_OFF : When SDFREE_OFF = 1 , disable schottky free mode. This is valid only when APON = 1.

IGVDD2[2:0] : This register controls the second stage bias current of GVDD Amplifier.

IGVDD1[2:0] : This register controls the first stage bias current of GVDD Amplifier.

IVCOM2[2:0] : This register controls the second stage bias current of VCOM Amplifier.

IVCOM1[2:0] : This register controls the first stage bias current of VCOM Amplifier.

VCLOPEN_EN : This register controls the connection between VCL and VSSC. When VCLOPEN_EN = 1, disconnection between VCL and VSSC.

VGHDT_EN : This register enables to check whether is a normally VGH voltage.

GVDD_HIZ : Control GVDD amp status when GVDD amp off.

AB: Set VCI1 output equal to VCI. VCI1 output is internally connected to VCI via switching circuit when AB="H."

VCIREX_EN : When VCIREX_EN = 1, use external reference voltage in VCIR_EXIN pad.

VREF_EN : When VREF_EN = 0, use external reference voltage in VCIR_EXIN pad.

Table 139. VCIR and VCIR_EXIN pad status

VCIREX_EN	VREF_EN	VCIR_EXIN pad	VCIR	Remark
0	0	Not available		
0	1	Floating	Band-gap reference output	Normal operating
1	0	VCIR input	VCIR_EXIN pad input value	For EDS, GVDD/VCOM/VREF P1 test
1	1	VCIR output	Band-gap reference output	For EDS, VCIR P1 test

TST_VCM[2:0] : Control VCOM amp status.

Table 140. Outputs of VCOM

TST_VCM2	TST_VCM1	TST_VCM0	VCOM
0	0	0	Normal Operation
1	0	0	VCOML
1	0	1	VSSA
1	1	0	VCI
1	1	1	VCOMH
Else			Reserved

VCOM_MODE : When VCOM_MODE = 1, VCOM amp turn on without regard to power transition.

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GAM_TEST : Set the Gamma DFT Test

GSAP[2:0] : This register controls the slew rate of global amplifier.

HGLSR_SET[1:0] : This register controls the stability of global driver amplifier.

HSR_SET[1:0] : This register controls the stability of source driver amplifier.

STV_SET[1:0] : Select the length of STV for Shift register

Table 141. STV_SET[1:0]

STV_SEL1	STV_SEL0	Delay Time
0	0	5ns
0	1	10ns
1	0	15ns
1	1	20ns

TH_SEL : When TH_SEL = 1, track and hold scheme is used in binary mode.

TRACK_SRC[1:0] : This register controls the delay time between TRACK_P and GRAY_CNT.

Table 142. TRACK_SRC[1:0]

TRACK_SRC1	TRACK_SRC0	Delay Time
0	0	10ns
0	1	20ns
1	0	30ns
1	1	40ns

OSC_TEST : When OSC_TEST = 1, ET_FOSC_SET[4:0] is 4'b0000 irrelatively with NFOSC/PIFOSC registers..

NFOSC/PIFOSC : These registers are used to select the oscillation frequency of internal oscillator. PIFOSC4-0 is applied in Idle Partial mode.

When FOSC[4:0] is larger than 5'b10110.The oscillation frequency increase.

When FOSC[4:0] is smaller than 5'b10110.The oscillation frequency decrease.

Note. If the default oscillation frequency is 9 MHz and register setting of FOSC [4:0] is 10110.

Status	Default Value
Initial	1st Parameter: 0000_0000 2nd Parameter: 0000_0000

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	3rd Parameter: 0001_0000 4th Parameter: 0001_1000 5th Parameter: 0001_0010 6th Parameter: 0000_0001 7th Parameter: 0000_0100 8th Parameter: 0100_0100 9th Parameter: 0100_0000 10th Parameter: 0001_0110 11th Parameter: 0001_0110

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5.3.9. LOGICTEST (FEH)

FEh	Logic Test Command											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	1	0	FE
1st Parameter	1	1	↑	MEM_CK_SEL1	SLP_SEL	-	-	-	IE_RGB	IOB	DSTB_LINE	-
2nd Parameter	1	1	↑	ODTS[4]	ODTS[3]	ODTS[2]	ODTS[1]	ODTS[0]	IE_CSX	-	SER_OEN_SEL	-
3rd Parameter	1	1	↑	MCS[3]	MCS[2]	MCS[1]	MCS[0]	MCS_SEL	BIRA_SEL	MEM_CK_SEL	-	-
4th Parameter	1	1	↑								RB_SEL	
5th Parameter	1	1	↑	RB[39]	RB[38]	RB[37]	RB[36]	RB[35]	RB[34]	RB[33]	RB[32]	
6th Parameter	1	1	↑	RB[31]	RB[30]	RB[29]	RB[28]	RB[27]	RB[26]	RB[25]	RB[24]	
7th Parameter	1	1	↑	RB[23]	RB[22]	RB[21]	RB[20]	RB[19]	RB[18]	RB[17]	RB[16]	
8th Parameter	1	1	↑	RB[15]	RB[14]	RB[13]	RB[12]	RB[11]	RB[10]	RB[9]	RB[8]	
9th Parameter	1	1	↑	RB[7]	RB[6]	RB[5]	RB[4]	RB[3]	RB[2]	RB[1]	RB[0]	

SLP_SEL : When APON=0, select SLP In command reset.

IE_RGB : IO blocking about RGB Interface Input signal

IOB : When IOB = 1, enable IO blocking.

DSTB_LINE : Select the Line to start DSTB_EN signal

0 : 20-Line, 1 : 100-Line

ODTS[4:0] : Control delay for AC timing (ODTS : output data hold time in Parameterllel mode)

IE_CSX : IO blocking about CPU Interface Input signal

SER_OEN_SEL : SDA OEN control. When SER_OEN_SEL = 0, OEN is effected by SCK signal.

MCS[3:0] : Memory Speed control.

MCS_SEL : When MCS_SEL = 1, MCS is set by register.

BIRA_SEL : When BIRA_SEL = 1, BIRA ChipID is refreshed every frame.

MEM_CK_SEL/MEM_CK_SEL1 : Memory Write Clock delay control.

MEM_CK_SEL, MEM_CK_SEL1	WCK delay
00	10ns delay
01	15ns delay
10	20ns delay
11	25ns delay

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RB_SEL :

RB[39:0] :

Status	Default Value
Initial	1st Parameter: 1000_0100 2nd Parameter: 0100_1000 3rd Parameter: 0101_0000 4th Parameter: 0000_0001 5th Parameter: 1111_1111 6th Parameter: 1111_1111 7th Parameter: 1111_1111 8th Parameter: 1111_1111 9th Parameter: 1111_1111

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5.3.10. EDSTEST (FFH)

FFh	EDS Test Command											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	1	1	FF
1st Parameter	1	1	↑	-	-	-	GAON	-	-	-	CHIPIDON	-
2nd Parameter	1	1	↑	MON_SEL[3]	MON_SEL[2]	MON_SEL[1]	MON_SEL[0]	VOHL_TEST	VOHL_VAL	LVTH	EN_EXCLK	-
3rd Parameter	1	1	↑	BLK_SKIP	-	M_CON	INV_FIX	-	-	-	DC_INV	-

GAON : Gate all ON (0: disable, 1: enable)

CHIPIDON : Chip ID test enable signal. (0: disable, 1: enable)

MON_SEL[3:0] : : Control monitoring pin.

Table 143. Outputs of CL1, BC,BC_CTRL and TE

MON_SEL[3:0]	TOUT1[2](SDO,CL1)	TOU1[1](BC)	TOUT1[0] (BC_CTRL)	TE
0000	SDO / CL1	BC	BC_CTRL	TE
0001	CL1	FLM	M	TE
0010	VCM_CLK	RCY_CLK	SD_MREV_IN	M
0011	GL_PRECH_CK	GL_GNO_CK	GL_ALLON_EN	GL_LATCHB_CK
0100	SD_OUT_EN	SD_RCY_EN	SD_BIN_EN	M
0101	SD_SLATCH_IN	SD_MREV_IN	SD_XGM_EN	BT_VGHFLAG_OUT
0110	SD_GRAY_CNT_SET0	SD_TRACK_IN_0	SD_TRACK_IN_XOR	I(SD_MUX_SEL)
0111	EC_OSC_CK/32	EC_RESETB_OUT	BT_AVDD_CK	BT_VGHL_CK
1000	VGHFREE1_FLAG	VGH_FLAG	VGL_FLAG	VGHFREE2_EN

LVTH : MTP Low Vth test command.

VOHL_TEST : VOH/ VOL test for output pads. (0: disable, 1: enable)

VOHL_VAL : When VOLH_TEST = high, Output pads drive the value of VOHL_VAL.

EN_EXCLK : Enable EXCLK.

BLK_SKIP : Skip the first 2-frame(white display)

M_CON : VCOM level fix.

INV_FIX: When M_CON=high, VCOM controlled by INV_FIX. (0: fixed to low, 1: fixed to high)

DC_INV : When DC_INV=high, DCCLK1/2/3 are inversion every frame.

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Status	Default Value
Initial	1st Parameter: 0000_0000 2nd Parameter: 0000_0000 3rd Parameter: 0000_0000

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CHAPTER 6

APPENDIX

6.1 Application Circuit
6.2 External Components
6.3 PAD Center Coordinates
6.4 Display Module Default Position

Preliminary

6. APPENDIX

6.1. APPLICATION CIRCUIT

A typical application circuit is shown in following figure. All black-colored capacitors are 1uF capacitors.

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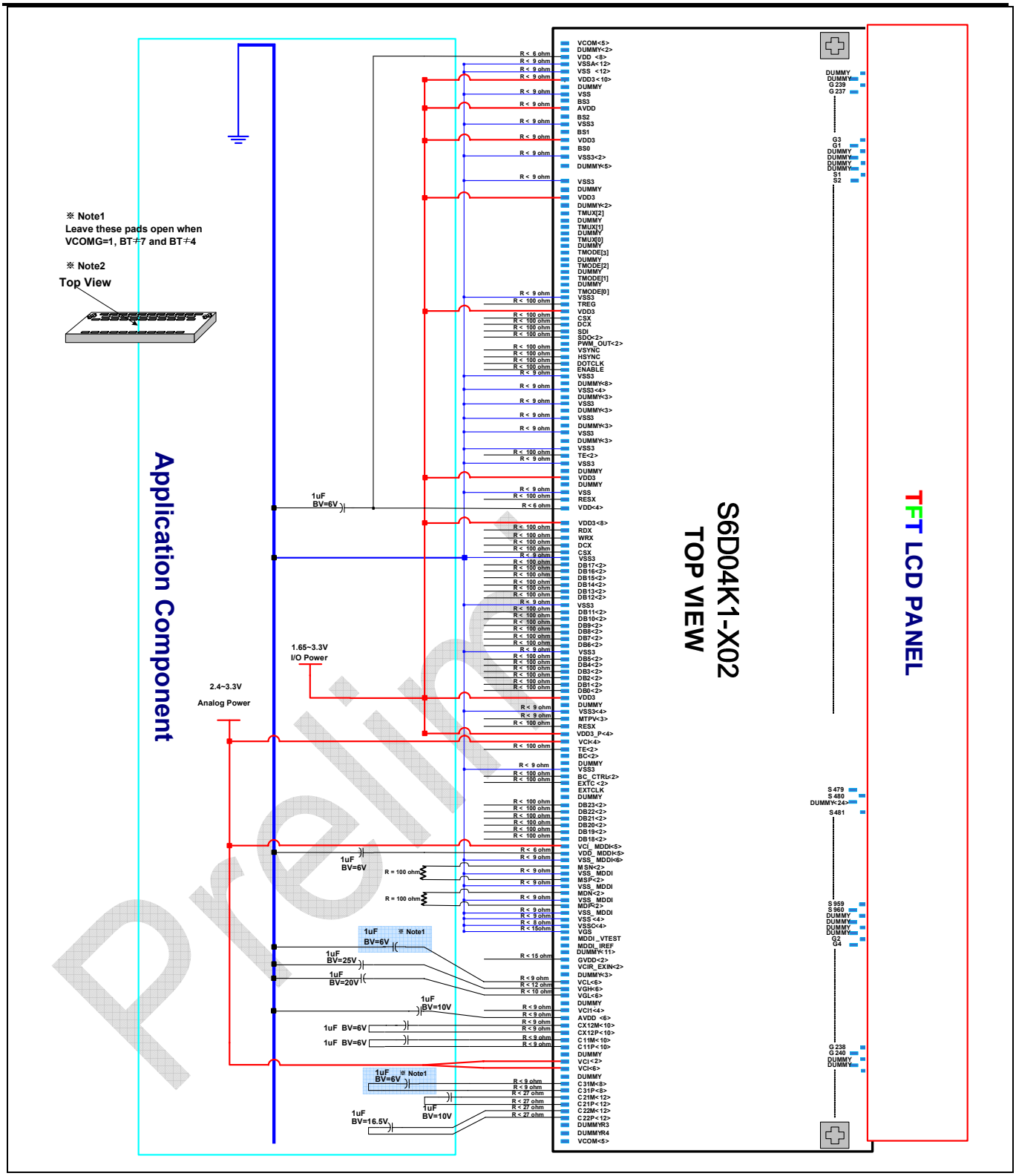

Figure135. Application circuit.

6.2. EXTERNAL COMPONENTS

Table 144. External Components

Name	Device	Value	Connection	Note	
C1	Capacitor	1uF	AVDD – GND	Maximum Ratings Voltage	10V
C2	Capacitor	1uF	VGH – GND		25V
C3	Capacitor	1uF	VGL – GND		20V
C4	Capacitor	1uF	C11P – C11M		6V
C5	Capacitor	1uF	C12P – C12M		6V
C6	Capacitor	1uF	C21P – C21M		10V
C7	Capacitor	1uF	C22P – C22M		16.5V
C8	Capacitor	1uF	C31P – C31M		6V
C9	Capacitor	1uF	VCL-GND		6V
C10	Capacitor	1uF	RVDD – GND		6V
D1	Diode	-	(+)VGL – GND(-)	VF < 0.4V (@ IF = 20mA, Ta = 25℃) VR ≥ max.25V (Option)	

Note: It is optional to connect S/D between VGL and GND

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6.3. PAD CENTER COORDINATES

6.3.1. INPUT PAD

Table 145. Pad Center Coordinates [Unit: μm]

6.4.

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1	VCOM	-9029	-228.5	51	VSS3	-7029	-228.5	101	DUMMY	-5029	-257.0
2	VCOM	-8989	-228.5	52	IM<3>	-6989	-228.5	102	DUMMY	-4989	-257.0
3	VCOM	-8949	-228.5	53	VDD3	-6949	-228.5	103	DUMMY	-4949	-228.5
4	VCOM	-8909	-228.5	54	IM<2>	-6909	-228.5	104	DUMMY	-4909	-228.5
5	VCOM	-8869	-228.5	55	VSS3	-6869	-228.5	105	DUMMY	-4869	-228.5
6	DUMMYR1	-8829	-257.0	56	IM<1>	-6829	-228.5	106	DUMMY	-4829	-228.5
7	DUMMYR2	-8789	-257.0	57	VDD3	-6789	-228.5	107	VSS3	-4789	-228.5
8	VDD	-8749	-257.0	58	IM<0>	-6749	-228.5	108	VSS3	-4749	-228.5
9	VDD	-8709	-257.0	59	VSS3	-6709	-228.5	109	VSS3	-4709	-228.5
10	VDD	-8669	-257.0	60	VSS3	-6669	-228.5	110	VSS3	-4669	-228.5
11	VDD	-8629	-228.5	61	DUMMY	-6629	-228.5	111	DUMMY	-4629	-228.5
12	VDD	-8589	-228.5	62	DUMMY	-6589	-228.5	112	DUMMY	-4589	-228.5
13	VDD	-8549	-228.5	63	DUMMY	-6549	-228.5	113	DUMMY	-4549	-228.5
14	VDD	-8509	-228.5	64	DUMMY	-6509	-228.5	114	VSS3	-4509	-228.5
15	VDD	-8469	-228.5	65	DUMMY	-6469	-228.5	115	DUMMY	-4469	-257.0
16	VSSA	-8429	-228.5	66	VSS3	-6429	-228.5	116	DUMMY	-4429	-257.0
17	VSSA	-8389	-228.5	67	DUMMY	-6389	-228.5	117	DUMMY	-4389	-257.0
18	VSSA	-8349	-228.5	68	VDD3	-6349	-228.5	118	VSS3	-4349	-257.0
19	VSSA	-8309	-228.5	69	DUMMY	-6309	-228.5	119	DUMMY	-4309	-228.5
20	VSSA	-8269	-228.5	70	DUMMY	-6269	-228.5	120	DUMMY	-4269	-228.5
21	VSSA	-8229	-228.5	71	TMUX<2>	-6229	-228.5	121	DUMMY	-4229	-228.5
22	VSSA	-8189	-228.5	72	DUMMY	-6189	-228.5	122	VSS3	-4189	-228.5
23	VSSA	-8149	-228.5	73	TMUX<1>	-6149	-228.5	123	DUMMY	-4149	-228.5
24	VSSA	-8109	-228.5	74	DUMMY	-6109	-228.5	124	DUMMY	-4109	-228.5
25	VSSA	-8069	-228.5	75	TMUX<0>	-6069	-228.5	125	DUMMY	-4069	-228.5
26	VSSA	-8029	-228.5	76	DUMMY	-6029	-228.5	126	VSS3	-4029	-228.5
27	VSSA	-7989	-228.5	77	TMODE<3>	-5989	-228.5	127	TE	-3989	-228.5
28	VSS	-7949	-228.5	78	DUMMY	-5949	-228.5	128	TE	-3949	-228.5
29	VSS	-7909	-228.5	79	TMODE<2>	-5909	-228.5	129	VSS3	-3909	-228.5
30	VSS	-7869	-228.5	80	DUMMY	-5869	-228.5	130	DUMMY	-3869	-228.5
31	VSS	-7829	-228.5	81	TMODE<1>	-5829	-228.5	131	VDD3	-3829	-228.5
32	VSS	-7789	-228.5	82	DUMMY	-5789	-228.5	132	DUMMY	-3789	-228.5
33	VSS	-7749	-228.5	83	TMODE<0>	-5749	-228.5	133	VSS3	-3749	-228.5
34	VSS	-7709	-228.5	84	VSS3	-5709	-228.5	134	RESX	-3709	-228.5
35	VSS	-7669	-228.5	85	TREGB	-5669	-228.5	135	VDD	-3669	-228.5
36	VSS	-7629	-228.5	86	VDD3	-5629	-228.5	136	VDD	-3629	-228.5
37	VSS	-7589	-228.5	87	CSX	-5589	-228.5	137	VDD	-3589	-228.5
38	VSS	-7549	-228.5	88	DCX	-5549	-228.5	138	VDD	-3549	-228.5
39	VSS	-7509	-228.5	89	SDI	-5509	-228.5	139	VDD3	-3509	-228.5
40	VDD3	-7469	-228.5	90	SDA	-5469	-228.5	140	VDD3	-3469	-228.5
41	VDD3	-7429	-228.5	91	SDA	-5429	-228.5	141	VDD3	-3429	-228.5
42	VDD3	-7389	-228.5	92	BC	-5389	-228.5	142	VDD3	-3389	-228.5
43	VDD3	-7349	-228.5	93	BC	-5349	-228.5	143	VDD3	-3349	-228.5
44	VDD3	-7309	-228.5	94	VSYNC	-5309	-228.5	144	VDD3	-3309	-228.5
45	VDD3	-7269	-228.5	95	HSYNC	-5269	-228.5	145	VDD3	-3269	-228.5
46	VDD3	-7229	-228.5	96	DOTCLK	-5229	-228.5	146	VDD3	-3229	-228.5
47	VDD3	-7189	-228.5	97	ENABLE	-5189	-228.5	147	RDX	-3189	-228.5
48	VDD3	-7149	-228.5	98	VSS3	-5149	-228.5	148	WRX	-3149	-228.5
49	VDD3	-7109	-228.5	99	DUMMY	-5109	-228.5	149	DCX	-3109	-228.5
50	DUMMY	-7069	-228.5	100	DUMMY	-5069	-257.0	150	CSX	-3069	-228.5

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
151	VSS3	-3029	-228.5		201	VDD3	-1029	-228.5		251	MSP	1549	-228.5
152	DB<17>	-2989	-228.5		202	VDD3_P	-989	-228.5		252	MSP	1589	-228.5
153		-2949	-228.5		203	VDD3_P	-949	-228.5		253	VSS3	1629	-228.5
154	DB<16>	-2909	-228.5		204	VCI	-909	-228.5		254	MDN	1669	-228.5
155		-2869	-228.5		205	VCI	-869	-228.5		255	MDN	1709	-228.5
156	DB<15>	-2829	-228.5		206	VCI	-829	-228.5		256	VSS3	1749	-228.5
157		-2789	-228.5		207	VCI	-789	-228.5		257	MDP	1789	-228.5
158	DB<14>	-2749	-228.5		208	TE	-749	-228.5		258	MDP	1829	-228.5
159		-2709	-228.5		209	TE	-709	-228.5		259	VSS3	1869	-228.5
160	DB<13>	-2669	-228.5		210	BC	-669	-228.5		260	VSS	1909	-228.5
161		-2629	-228.5		211	BC	-629	-228.5		261	VSS	1949	-228.5
162	DB<12>	-2589	-228.5		212	DUMMY	-589	-228.5		262	VSS	1989	-228.5
163		-2549	-228.5		213	VSS3	-549	-228.5		263	VSS	2029	-228.5
164	VSS3	-2509	-228.5		214	BC_CTRL	-509	-228.5		264	VSSC	2069	-228.5
165	DB<11>	-2469	-228.5		215	BC_CTRL	-469	-228.5		265	VSSC	2109	-228.5
166		-2429	-228.5		216	EXTC	-429	-228.5		266	VSSC	2149	-228.5
167	DB<10>	-2389	-228.5		217	EXTC	-389	-228.5		267	VSSC	2189	-228.5
168		-2349	-228.5		218	EXTCLK	-349	-228.5		268	VGS	2229	-228.5
169	DB<9>	-2309	-228.5		219	DUMMY	-309	-228.5		269	MDDI_VTEST	2269	-228.5
170		-2269	-228.5		220	DB<23>	309	-228.5		270	MDDI_IREF	2309	-228.5
171	DB<8>	-2229	-228.5		221		349	-228.5		271	DUMMY	2349	-228.5
172		-2189	-228.5		222	DB<22>	389	-228.5		272	DUMMY	2389	-228.5
173	DB<7>	-2149	-228.5		223		429	-228.5		273	DUMMY	2429	-228.5
174		-2109	-228.5		224	DB<21>	469	-228.5		274	DUMMY	2469	-228.5
175	DB<6>	-2069	-228.5		225		509	-228.5		275	DUMMY	2509	-228.5
176		-2029	-228.5		226	DB<20>	549	-257.0		276	DUMMY	2549	-228.5
177	VSS3	-1989	-228.5		227		589	-257.0		277	DUMMY	2589	-228.5
178	DB<5>	-1949	-228.5		228	DB<19>	629	-257.0		278	DUMMY	2629	-228.5
179		-1909	-228.5		229		669	-228.5		279	DUMMY	2669	-228.5
180	DB<4>	-1869	-228.5		230	DB<18>	709	-228.5		280	DUMMY	2709	-228.5
181		-1829	-228.5		231		749	-228.5		281	DUMMY	2749	-228.5
182	DB<3>	-1789	-228.5		232	VCI_MDDI	789	-228.5		282	GVDD	2789	-228.5
183		-1749	-228.5		233	VCI_MDDI	829	-228.5		283	GVDD	2829	-228.5
184	DB<2>	-1709	-228.5		234	VCI_MDDI	869	-228.5		284	VCIR_EXIN	2869	-228.5
185		-1669	-228.5		235	VCI_MDDI	909	-228.5		285	VCIR_EXIN	2909	-228.5
186	DB<1>	-1629	-228.5		236	VCI_MDDI	949	-228.5		286	DUMMY	2949	-228.5
187		-1589	-228.5		237	VDD_MDDI	989	-228.5		287	DUMMY	2989	-228.5
188	DB<0>	-1549	-228.5		238	VDD_MDDI	1029	-228.5		288	DUMMY	3029	-228.5
189		-1509	-228.5		239	VDD_MDDI	1069	-257.0		289	VCL	3069	-228.5
190	VDD3	-1469	-228.5		240	VDD_MDDI	1109	-257.0		290	VCL	3109	-228.5
191	DUMMY	-1429	-228.5		241	VDD_MDDI	1149	-228.5		291	VCL	3149	-228.5
192	VSS3	-1389	-228.5		242	VSS_MDDI	1189	-228.5		292	VCL	3189	-228.5
193	VSS3	-1349	-228.5		243	VSS_MDDI	1229	-228.5		293	VCL	3229	-228.5
194	VSS3	-1309	-228.5		244	VSS_MDDI	1269	-257.0		294	VCL	3269	-228.5
195	VSS3	-1269	-228.5		245	VSS_MDDI	1309	-257.0		295	VGH	3309	-228.5
196	MTPV	-1229	-228.5		246	VSS_MDDI	1349	-257.0		296	VGH	3349	-228.5
197	MTPV	-1189	-228.5		247	VSS_MDDI	1389	-228.5		297	VGH	3389	-228.5
198	MTPV	-1149	-228.5		248	MSN	1429	-228.5		298	VGH	3429	-228.5
199	RESX	-1109	-228.5		249	MSN	1469	-228.5		299	VGH	3469	-257.0
200	VDD3	-1069	-228.5		250	VSS3	1509	-228.5		300	VGH	3509	-257.0

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
301	VGL	3549	-257.0		351	C11P	5549	-228.5		401	C21P	7549	-228.5
302	VGL	3589	-257.0		352	C11P	5589	-228.5		402	C21P	7589	-228.5
303	VGL	3629	-257.0		353	C11P	5629	-228.5		403	C21P	7629	-228.5
304	VGL	3669	-257.0		354	C11P	5669	-228.5		404	C21P	7669	-228.5
305	VGL	3709	-257.0		355	C11P	5709	-228.5		405	C21P	7709	-228.5
306	VGL	3749	-257.0		356	C11P	5749	-228.5		406	C21P	7749	-228.5
307	DUMMY	3789	-257.0		357	C11P	5789	-228.5		407	C21P	7789	-228.5
308	VCI1	3829	-228.5		358	DUMMY	5829	-228.5		408	C22M	7829	-228.5
309	VCI1	3869	-228.5		359	VCI_RCYC	5869	-228.5		409	C22M	7869	-228.5
310	VCI1	3909	-228.5		360	VCI_RCYC	5909	-228.5		410	C22M	7909	-228.5
311	VCI1	3949	-228.5		361	VCI	5949	-228.5		411	C22M	7949	-228.5
312	AVDD	3989	-228.5		362	VCI	5989	-228.5		412	C22M	7989	-228.5
313	AVDD	4029	-228.5		363	VCI	6029	-228.5		413	C22M	8029	-228.5
314	AVDD	4069	-228.5		364	VCI	6069	-228.5		414	C22M	8069	-228.5
315	AVDD	4109	-228.5		365	VCI	6109	-228.5		415	C22M	8109	-228.5
316	AVDD	4149	-228.5		366	VCI	6149	-228.5		416	C22M	8149	-228.5
317	AVDD	4189	-228.5		367	DUMMY	6189	-228.5		417	C22M	8189	-228.5
318	C12M	4229	-228.5		368	C31M	6229	-228.5		418	C22M	8229	-228.5
319	C12M	4269	-228.5		369	C31M	6269	-228.5		419	C22M	8269	-228.5
320	C12M	4309	-228.5		370	C31M	6309	-228.5		420	C22P	8309	-228.5
321	C12M	4349	-228.5		371	C31M	6349	-228.5		421	C22P	8349	-228.5
322	C12M	4389	-228.5		372	C31M	6389	-228.5		422	C22P	8389	-228.5
323	C12M	4429	-228.5		373	C31M	6429	-228.5		423	C22P	8429	-228.5
324	C12M	4469	-228.5		374	C31M	6469	-228.5		424	C22P	8469	-228.5
325	C12M	4509	-228.5		375	C31M	6509	-228.5		425	C22P	8509	-228.5
326	C12M	4549	-228.5		376	C31P	6549	-228.5		426	C22P	8549	-228.5
327	C12M	4589	-228.5		377	C31P	6589	-228.5		427	C22P	8589	-228.5
328	C12P	4629	-228.5		378	C31P	6629	-228.5		428	C22P	8629	-228.5
329	C12P	4669	-228.5		379	C31P	6669	-228.5		429	C22P	8669	-228.5
330	C12P	4709	-228.5		380	C31P	6709	-228.5		430	C22P	8709	-228.5
331	C12P	4749	-228.5		381	C31P	6749	-228.5		431	C22P	8749	-228.5
332	C12P	4789	-228.5		382	C31P	6789	-228.5		432	DUMMYR3	8789	-228.5
333	C12P	4829	-228.5		383	C31P	6829	-228.5		433	DUMMYR4	8829	-228.5
334	C12P	4869	-228.5		384	C21M	6869	-228.5		434	VCOM	8869	-228.5
335	C12P	4909	-228.5		385	C21M	6909	-228.5		435	VCOM	8909	-228.5
336	C12P	4949	-228.5		386	C21M	6949	-228.5		436	VCOM	8949	-228.5
337	C12P	4989	-228.5		387	C21M	6989	-228.5		437	VCOM	8989	-228.5
338	C11M	5029	-228.5		388	C21M	7029	-228.5		438	VCOM	9029	-228.5
339	C11M	5069	-228.5		389	C21M	7069	-228.5		439	DUMMY	9035	239
340	C11M	5109	-228.5		390	C21M	7109	-228.5		440	DUMMY	9019	113
341	C11M	5149	-228.5		391	C21M	7149	-228.5		441	G240	9003	239
342	C11M	5189	-228.5		392	C21M	7189	-228.5		442	G238	8987	113
343	C11M	5229	-228.5		393	C21M	7229	-228.5		443	G236	8971	239
344	C11M	5269	-228.5		394	C21M	7269	-228.5		444	G234	8955	113
345	C11M	5309	-228.5		395	C21M	7309	-228.5		445	G232	8939	239
346	C11M	5349	-228.5		396	C21P	7349	-228.5		446	G230	8923	113
347	C11M	5389	-228.5		397	C21P	7389	-228.5		447	G228	8907	239
348	C11P	5429	-228.5		398	C21P	7429	-228.5		448	G226	8891	113
349	C11P	5469	-228.5		399	C21P	7469	-228.5		449	G224	8875	239
350	C11P	5509	-228.5		400	C21P	7509	-228.5		450	G222	8859	113

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
451	G220	8843	239		501	G120	8043	239		551	G20	7243	239
452	G218	8827	113		502	G118	8027	113		552	G18	7227	113
453	G216	8811	239		503	G116	8011	239		553	G16	7211	239
454	G214	8795	113		504	G114	7995	113		554	G14	7195	113
455	G212	8779	239		505	G112	7979	239		555	G12	7179	239
456	G210	8763	113		506	G110	7963	113		556	G10	7163	113
457	G208	8747	239		507	G108	7947	239		557	G8	7147	239
458	G206	8731	113		508	G106	7931	113		558	G6	7131	113
459	G204	8715	239		509	G104	7915	239		559	G4	7115	239
460	G202	8699	113		510	G102	7899	113		560	G2	7099	113
461	G200	8683	239		511	G100	7883	239		561	DUMMY	7083	239
462	G198	8667	113		512	G98	7867	113		562	DUMMY	7067	113
463	G196	8651	239		513	G96	7851	239		563	DUMMY	7051	239
464	G194	8635	113		514	G94	7835	113		564	DUMMY	7037	113
465	G192	8619	239		515	G92	7819	239		565	S960	7023	239
466	G190	8603	113		516	G90	7803	113		566	S959	7009	113
467	G188	8587	239		517	G88	7787	239		567	S958	6995	239
468	G186	8571	113		518	G86	7771	113		568	S957	6981	113
469	G184	8555	239		519	G84	7755	239		569	S956	6967	239
470	G182	8539	113		520	G82	7739	113		570	S955	6953	113
471	G180	8523	239		521	G80	7723	239		571	S954	6939	239
472	G178	8507	113		522	G78	7707	113		572	S953	6925	113
473	G176	8491	239		523	G76	7691	239		573	S952	6911	239
474	G174	8475	113		524	G74	7675	113		574	S951	6897	113
475	G172	8459	239		525	G72	7659	239		575	S950	6883	239
476	G170	8443	113		526	G70	7643	113		576	S949	6869	113
477	G168	8427	239		527	G68	7627	239		577	S948	6855	239
478	G166	8411	113		528	G66	7611	113		578	S947	6841	113
479	G164	8395	239		529	G64	7595	239		579	S946	6827	239
480	G162	8379	113		530	G62	7579	113		580	S945	6813	113
481	G160	8363	239		531	G60	7563	239		581	S944	6799	239
482	G158	8347	113		532	G58	7547	113		582	S943	6785	113
483	G156	8331	239		533	G56	7531	239		583	S942	6771	239
484	G154	8315	113		534	G54	7515	113		584	S941	6757	113
485	G152	8299	239		535	G52	7499	239		585	S940	6743	239
486	G150	8283	113		536	G50	7483	113		586	S939	6729	113
487	G148	8267	239		537	G48	7467	239		587	S938	6715	239
488	G146	8251	113		538	G46	7451	113		588	S937	6701	113
489	G144	8235	239		539	G44	7435	239		589	S936	6687	239
490	G142	8219	113		540	G42	7419	113		590	S935	6673	113
491	G140	8203	239		541	G40	7403	239		591	S934	6659	239
492	G138	8187	113		542	G38	7387	113		592	S933	6645	113
493	G136	8171	239		543	G36	7371	239		593	S932	6631	239
494	G134	8155	113		544	G34	7355	113		594	S931	6617	113
495	G132	8139	239		545	G32	7339	239		595	S930	6603	239
496	G130	8123	113		546	G30	7323	113		596	S929	6589	113
497	G128	8107	239		547	G28	7307	239		597	S928	6575	239
498	G126	8091	113		548	G26	7291	113		598	S927	6561	113
499	G124	8075	239		549	G24	7275	239		599	S926	6547	239
500	G122	8059	113		550	G22	7259	113		600	S925	6533	113

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
601	S924	6519	239		651	S874	5819	239		701	S824	5119	239
602	S923	6505	113		652	S873	5805	113		702	S823	5105	113
603	S922	6491	239		653	S872	5791	239		703	S822	5091	239
604	S921	6477	113		654	S871	5777	113		704	S821	5077	113
605	S920	6463	239		655	S870	5763	239		705	S820	5063	239
606	S919	6449	113		656	S869	5749	113		706	S819	5049	113
607	S918	6435	239		657	S868	5735	239		707	S818	5035	239
608	S917	6421	113		658	S867	5721	113		708	S817	5021	113
609	S916	6407	239		659	S866	5707	239		709	S816	5007	239
610	S915	6393	113		660	S865	5693	113		710	S815	4993	113
611	S914	6379	239		661	S864	5679	239		711	S814	4979	239
612	S913	6365	113		662	S863	5665	113		712	S813	4965	113
613	S912	6351	239		663	S862	5651	239		713	S812	4951	239
614	S911	6337	113		664	S861	5637	113		714	S811	4937	113
615	S910	6323	239		665	S860	5623	239		715	S810	4923	239
616	S909	6309	113		666	S859	5609	113		716	S809	4909	113
617	S908	6295	239		667	S858	5595	239		717	S808	4895	239
618	S907	6281	113		668	S857	5581	113		718	S807	4881	113
619	S906	6267	239		669	S856	5567	239		719	S806	4867	239
620	S905	6253	113		670	S855	5553	113		720	S805	4853	113
621	S904	6239	239		671	S854	5539	239		721	S804	4839	239
622	S903	6225	113		672	S853	5525	113		722	S803	4825	113
623	S902	6211	239		673	S852	5511	239		723	S802	4811	239
624	S901	6197	113		674	S851	5497	113		724	S801	4797	113
625	S900	6183	239		675	S850	5483	239		725	S800	4783	239
626	S899	6169	113		676	S849	5469	113		726	S799	4769	113
627	S898	6155	239		677	S848	5455	239		727	S798	4755	239
628	S897	6141	113		678	S847	5441	113		728	S797	4741	113
629	S896	6127	239		679	S846	5427	239		729	S796	4727	239
630	S895	6113	113		680	S845	5413	113		730	S795	4713	113
631	S894	6099	239		681	S844	5399	239		731	S794	4699	239
632	S893	6085	113		682	S843	5385	113		732	S793	4685	113
633	S892	6071	239		683	S842	5371	239		733	S792	4671	239
634	S891	6057	113		684	S841	5357	113		734	S791	4657	113
635	S890	6043	239		685	S840	5343	239		735	S790	4643	239
636	S889	6029	113		686	S839	5329	113		736	S789	4629	113
637	S888	6015	239		687	S838	5315	239		737	S788	4615	239
638	S887	6001	113		688	S837	5301	113		738	S787	4601	113
639	S886	5987	239		689	S836	5287	239		739	S786	4587	239
640	S885	5973	113		690	S835	5273	113		740	S785	4573	113
641	S884	5959	239		691	S834	5259	239		741	S784	4559	239
642	S883	5945	113		692	S833	5245	113		742	S783	4545	113
643	S882	5931	239		693	S832	5231	239		743	S782	4531	239
644	S881	5917	113		694	S831	5217	113		744	S781	4517	113
645	S880	5903	239		695	S830	5203	239		745	S780	4503	239
646	S879	5889	113		696	S829	5189	113		746	S779	4489	113
647	S878	5875	239		697	S828	5175	239		747	S778	4475	239
648	S877	5861	113		698	S827	5161	113		748	S777	4461	113
649	S876	5847	239		699	S826	5147	239		749	S776	4447	239
650	S875	5833	113		700	S825	5133	113		750	S775	4433	113

Preliminary

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
751	S774	4419	239		801	S724	3719	239		851	S674	3019	239
752	S773	4405	113		802	S723	3705	113		852	S673	3005	113
753	S772	4391	239		803	S722	3691	239		853	S672	2991	239
754	S771	4377	113		804	S721	3677	113		854	S671	2977	113
755	S770	4363	239		805	S720	3663	239		855	S670	2963	239
756	S769	4349	113		806	S719	3649	113		856	S669	2949	113
757	S768	4335	239		807	S718	3635	239		857	S668	2935	239
758	S767	4321	113		808	S717	3621	113		858	S667	2921	113
759	S766	4307	239		809	S716	3607	239		859	S666	2907	239
760	S765	4293	113		810	S715	3593	113		860	S665	2893	113
761	S764	4279	239		811	S714	3579	239		861	S664	2879	239
762	S763	4265	113		812	S713	3565	113		862	S663	2865	113
763	S762	4251	239		813	S712	3551	239		863	S662	2851	239
764	S761	4237	113		814	S711	3537	113		864	S661	2837	113
765	S760	4223	239		815	S710	3523	239		865	S660	2823	239
766	S759	4209	113		816	S709	3509	113		866	S659	2809	113
767	S758	4195	239		817	S708	3495	239		867	S658	2795	239
768	S757	4181	113		818	S707	3481	113		868	S657	2781	113
769	S756	4167	239		819	S706	3467	239		869	S656	2767	239
770	S755	4153	113		820	S705	3453	113		870	S655	2753	113
771	S754	4139	239		821	S704	3439	239		871	S654	2739	239
772	S753	4125	113		822	S703	3425	113		872	S653	2725	113
773	S752	4111	239		823	S702	3411	239		873	S652	2711	239
774	S751	4097	113		824	S701	3397	113		874	S651	2697	113
775	S750	4083	239		825	S700	3383	239		875	S650	2683	239
776	S749	4069	113		826	S699	3369	113		876	S649	2669	113
777	S748	4055	239		827	S698	3355	239		877	S648	2655	239
778	S747	4041	113		828	S697	3341	113		878	S647	2641	113
779	S746	4027	239		829	S696	3327	239		879	S646	2627	239
780	S745	4013	113		830	S695	3313	113		880	S645	2613	113
781	S744	3999	239		831	S694	3299	239		881	S644	2599	239
782	S743	3985	113		832	S693	3285	113		882	S643	2585	113
783	S742	3971	239		833	S692	3271	239		883	S642	2571	239
784	S741	3957	113		834	S691	3257	113		884	S641	2557	113
785	S740	3943	239		835	S690	3243	239		885	S640	2543	239
786	S739	3929	113		836	S689	3229	113		886	S639	2529	113
787	S738	3915	239		837	S688	3215	239		887	S638	2515	239
788	S737	3901	113		838	S687	3201	113		888	S637	2501	113
789	S736	3887	239		839	S686	3187	239		889	S636	2487	239
790	S735	3873	113		840	S685	3173	113		890	S635	2473	113
791	S734	3859	239		841	S684	3159	239		891	S634	2459	239
792	S733	3845	113		842	S683	3145	113		892	S633	2445	113
793	S732	3831	239		843	S682	3131	239		893	S632	2431	239
794	S731	3817	113		844	S681	3117	113		894	S631	2417	113
795	S730	3803	239		845	S680	3103	239		895	S630	2403	239
796	S729	3789	113		846	S679	3089	113		896	S629	2389	113
797	S728	3775	239		847	S678	3075	239		897	S628	2375	239
798	S727	3761	113		848	S677	3061	113		898	S627	2361	113
799	S726	3747	239		849	S676	3047	239		899	S626	2347	239
800	S725	3733	113		850	S675	3033	113		900	S625	2333	113

Preliminary

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
901	S624	2319	239		951	S574	1619	239		1001	S524	919	239
902	S623	2305	113		952	S573	1605	113		1002	S523	905	113
903	S622	2291	239		953	S572	1591	239		1003	S522	891	239
904	S621	2277	113		954	S571	1577	113		1004	S521	877	113
905	S620	2263	239		955	S570	1563	239		1005	S520	863	239
906	S619	2249	113		956	S569	1549	113		1006	S519	849	113
907	S618	2235	239		957	S568	1535	239		1007	S518	835	239
908	S617	2221	113		958	S567	1521	113		1008	S517	821	113
909	S616	2207	239		959	S566	1507	239		1009	S516	807	239
910	S615	2193	113		960	S565	1493	113		1010	S515	793	113
911	S614	2179	239		961	S564	1479	239		1011	S514	779	239
912	S613	2165	113		962	S563	1465	113		1012	S513	765	113
913	S612	2151	239		963	S562	1451	239		1013	S512	751	239
914	S611	2137	113		964	S561	1437	113		1014	S511	737	113
915	S610	2123	239		965	S560	1423	239		1015	S510	723	239
916	S609	2109	113		966	S559	1409	113		1016	S509	709	113
917	S608	2095	239		967	S558	1395	239		1017	S508	695	239
918	S607	2081	113		968	S557	1381	113		1018	S507	681	113
919	S606	2067	239		969	S556	1367	239		1019	S506	667	239
920	S605	2053	113		970	S555	1353	113		1020	S505	653	113
921	S604	2039	239		971	S554	1339	239		1021	S504	639	239
922	S603	2025	113		972	S553	1325	113		1022	S503	625	113
923	S602	2011	239		973	S552	1311	239		1023	S502	611	239
924	S601	1997	113		974	S551	1297	113		1024	S501	597	113
925	S600	1983	239		975	S550	1283	239		1025	S500	583	239
926	S599	1969	113		976	S549	1269	113		1026	S499	569	113
927	S598	1955	239		977	S548	1255	239		1027	S498	555	239
928	S597	1941	113		978	S547	1241	113		1028	S497	541	113
929	S596	1927	239		979	S546	1227	239		1029	S496	527	239
930	S595	1913	113		980	S545	1213	113		1030	S495	513	113
931	S594	1899	239		981	S544	1199	239		1031	S494	499	239
932	S593	1885	113		982	S543	1185	113		1032	S493	485	113
933	S592	1871	239		983	S542	1171	239		1033	S492	471	239
934	S591	1857	113		984	S541	1157	113		1034	S491	457	113
935	S590	1843	239		985	S540	1143	239		1035	S490	443	239
936	S589	1829	113		986	S539	1129	113		1036	S489	429	113
937	S588	1815	239		987	S538	1115	239		1037	S488	415	239
938	S587	1801	113		988	S537	1101	113		1038	S487	401	113
939	S586	1787	239		989	S536	1087	239		1039	S486	387	239
940	S585	1773	113		990	S535	1073	113		1040	S485	373	113
941	S584	1759	239		991	S534	1059	239		1041	S484	359	239
942	S583	1745	113		992	S533	1045	113		1042	S483	345	113
943	S582	1731	239		993	S532	1031	239		1043	S482	331	239
944	S581	1717	113		994	S531	1017	113		1044	S481	317	113
945	S580	1703	239		995	S530	1003	239		1045	DUMMY	303	239
946	S579	1689	113		996	S529	989	113		1046	DUMMY	289	113
947	S578	1675	239		997	S528	975	239		1047	DUMMY	275	239
948	S577	1661	113		998	S527	961	113		1048	DUMMY	247	239
949	S576	1647	239		999	S526	947	239		1049	DUMMY	219	239
950	S575	1633	113		1000	S525	933	113		1050	DUMMY	191	239

Preliminary

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
1051	DUMMY	163	239		1101	S448	-765	113		1151	S398	-1465	113
1052	DUMMY	135	239		1102	S447	-779	239		1152	S397	-1479	239
1053	DUMMY	107	239		1103	S446	-793	113		1153	S396	-1493	113
1054	DUMMY	79	239		1104	S445	-807	239		1154	S395	-1507	239
1055	DUMMY	51	239		1105	S444	-821	113		1155	S394	-1521	113
1056	DUMMY	23	239		1106	S443	-835	239		1156	S393	-1535	239
1057	DUMMY	-23	239		1107	S442	-849	113		1157	S392	-1549	113
1058	DUMMY	-51	239		1108	S441	-863	239		1158	S391	-1563	239
1059	DUMMY	-79	239		1109	S440	-877	113		1159	S390	-1577	113
1060	DUMMY	-107	239		1110	S439	-891	239		1160	S389	-1591	239
1061	DUMMY	-135	239		1111	S438	-905	113		1161	S388	-1605	113
1062	DUMMY	-163	239		1112	S437	-919	239		1162	S387	-1619	239
1063	DUMMY	-191	239		1113	S436	-933	113		1163	S386	-1633	113
1064	DUMMY	-219	239		1114	S435	-947	239		1164	S385	-1647	239
1065	DUMMY	-247	239		1115	S434	-961	113		1165	S384	-1661	113
1066	DUMMY	-275	239		1116	S433	-975	239		1166	S383	-1675	239
1067	DUMMY	-289	113		1117	S432	-989	113		1167	S382	-1689	113
1068	DUMMY	-303	239		1118	S431	-1003	239		1168	S381	-1703	239
1069	S480	-317	113		1119	S430	-1017	113		1169	S380	-1717	113
1070	S479	-331	239		1120	S429	-1031	239		1170	S379	-1731	239
1071	S478	-345	113		1121	S428	-1045	113		1171	S378	-1745	113
1072	S477	-359	239		1122	S427	-1059	239		1172	S377	-1759	239
1073	S476	-373	113		1123	S426	-1073	113		1173	S376	-1773	113
1074	S475	-387	239		1124	S425	-1087	239		1174	S375	-1787	239
1075	S474	-401	113		1125	S424	-1101	113		1175	S374	-1801	113
1076	S473	-415	239		1126	S423	-1115	239		1176	S373	-1815	239
1077	S472	-429	113		1127	S422	-1129	113		1177	S372	-1829	113
1078	S471	-443	239		1128	S421	-1143	239		1178	S371	-1843	239
1079	S470	-457	113		1129	S420	-1157	113		1179	S370	-1857	113
1080	S469	-471	239		1130	S419	-1171	239		1180	S369	-1871	239
1081	S468	-485	113		1131	S418	-1185	113		1181	S368	-1885	113
1082	S467	-499	239		1132	S417	-1199	239		1182	S367	-1899	239
1083	S466	-513	113		1133	S416	-1213	113		1183	S366	-1913	113
1084	S465	-527	239		1134	S415	-1227	239		1184	S365	-1927	239
1085	S464	-541	113		1135	S414	-1241	113		1185	S364	-1941	113
1086	S463	-555	239		1136	S413	-1255	239		1186	S363	-1955	239
1087	S462	-569	113		1137	S412	-1269	113		1187	S362	-1969	113
1088	S461	-583	239		1138	S411	-1283	239		1188	S361	-1983	239
1089	S460	-597	113		1139	S410	-1297	113		1189	S360	-1997	113
1090	S459	-611	239		1140	S409	-1311	239		1190	S359	-2011	239
1091	S458	-625	113		1141	S408	-1325	113		1191	S358	-2025	113
1092	S457	-639	239		1142	S407	-1339	239		1192	S357	-2039	239
1093	S456	-653	113		1143	S406	-1353	113		1193	S356	-2053	113
1094	S455	-667	239		1144	S405	-1367	239		1194	S355	-2067	239
1095	S454	-681	113		1145	S404	-1381	113		1195	S354	-2081	113
1096	S453	-695	239		1146	S403	-1395	239		1196	S353	-2095	239
1097	S452	-709	113		1147	S402	-1409	113		1197	S352	-2109	113
1098	S451	-723	239		1148	S401	-1423	239		1198	S351	-2123	239
1099	S450	-737	113		1149	S400	-1437	113		1199	S350	-2137	113
1100	S449	-751	239		1150	S399	-1451	239		1200	S349	-2151	239

Preliminary

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
1201	S348	-2165	113		1251	S298	-2865	113		1301	S248	-3565	113
1202	S347	-2179	239		1252	S297	-2879	239		1302	S247	-3579	239
1203	S346	-2193	113		1253	S296	-2893	113		1303	S246	-3593	113
1204	S345	-2207	239		1254	S295	-2907	239		1304	S245	-3607	239
1205	S344	-2221	113		1255	S294	-2921	113		1305	S244	-3621	113
1206	S343	-2235	239		1256	S293	-2935	239		1306	S243	-3635	239
1207	S342	-2249	113		1257	S292	-2949	113		1307	S242	-3649	113
1208	S341	-2263	239		1258	S291	-2963	239		1308	S241	-3663	239
1209	S340	-2277	113		1259	S290	-2977	113		1309	S240	-3677	113
1210	S339	-2291	239		1260	S289	-2991	239		1310	S239	-3691	239
1211	S338	-2305	113		1261	S288	-3005	113		1311	S238	-3705	113
1212	S337	-2319	239		1262	S287	-3019	239		1312	S237	-3719	239
1213	S336	-2333	113		1263	S286	-3033	113		1313	S236	-3733	113
1214	S335	-2347	239		1264	S285	-3047	239		1314	S235	-3747	239
1215	S334	-2361	113		1265	S284	-3061	113		1315	S234	-3761	113
1216	S333	-2375	239		1266	S283	-3075	239		1316	S233	-3775	239
1217	S332	-2389	113		1267	S282	-3089	113		1317	S232	-3789	113
1218	S331	-2403	239		1268	S281	-3103	239		1318	S231	-3803	239
1219	S330	-2417	113		1269	S280	-3117	113		1319	S230	-3817	113
1220	S329	-2431	239		1270	S279	-3131	239		1320	S229	-3831	239
1221	S328	-2445	113		1271	S278	-3145	113		1321	S228	-3845	113
1222	S327	-2459	239		1272	S277	-3159	239		1322	S227	-3859	239
1223	S326	-2473	113		1273	S276	-3173	113		1323	S226	-3873	113
1224	S325	-2487	239		1274	S275	-3187	239		1324	S225	-3887	239
1225	S324	-2501	113		1275	S274	-3201	113		1325	S224	-3901	113
1226	S323	-2515	239		1276	S273	-3215	239		1326	S223	-3915	239
1227	S322	-2529	113		1277	S272	-3229	113		1327	S222	-3929	113
1228	S321	-2543	239		1278	S271	-3243	239		1328	S221	-3943	239
1229	S320	-2557	113		1279	S270	-3257	113		1329	S220	-3957	113
1230	S319	-2571	239		1280	S269	-3271	239		1330	S219	-3971	239
1231	S318	-2585	113		1281	S268	-3285	113		1331	S218	-3985	113
1232	S317	-2599	239		1282	S267	-3299	239		1332	S217	-3999	239
1233	S316	-2613	113		1283	S266	-3313	113		1333	S216	-4013	113
1234	S315	-2627	239		1284	S265	-3327	239		1334	S215	-4027	239
1235	S314	-2641	113		1285	S264	-3341	113		1335	S214	-4041	113
1236	S313	-2655	239		1286	S263	-3355	239		1336	S213	-4055	239
1237	S312	-2669	113		1287	S262	-3369	113		1337	S212	-4069	113
1238	S311	-2683	239		1288	S261	-3383	239		1338	S211	-4083	239
1239	S310	-2697	113		1289	S260	-3397	113		1339	S210	-4097	113
1240	S309	-2711	239		1290	S259	-3411	239		1340	S209	-4111	239
1241	S308	-2725	113		1291	S258	-3425	113		1341	S208	-4125	113
1242	S307	-2739	239		1292	S257	-3439	239		1342	S207	-4139	239
1243	S306	-2753	113		1293	S256	-3453	113		1343	S206	-4153	113
1244	S305	-2767	239		1294	S255	-3467	239		1344	S205	-4167	239
1245	S304	-2781	113		1295	S254	-3481	113		1345	S204	-4181	113
1246	S303	-2795	239		1296	S253	-3495	239		1346	S203	-4195	239
1247	S302	-2809	113		1297	S252	-3509	113		1347	S202	-4209	113
1248	S301	-2823	239		1298	S251	-3523	239		1348	S201	-4223	239
1249	S300	-2837	113		1299	S250	-3537	113		1349	S200	-4237	113
1250	S299	-2851	239		1300	S249	-3551	239		1350	S199	-4251	239

Preliminary

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
1351	S198	-4265	113		1401	S148	-4965	113		1451	S98	-5665	113
1352	S197	-4279	239		1402	S147	-4979	239		1452	S97	-5679	239
1353	S196	-4293	113		1403	S146	-4993	113		1453	S96	-5693	113
1354	S195	-4307	239		1404	S145	-5007	239		1454	S95	-5707	239
1355	S194	-4321	113		1405	S144	-5021	113		1455	S94	-5721	113
1356	S193	-4335	239		1406	S143	-5035	239		1456	S93	-5735	239
1357	S192	-4349	113		1407	S142	-5049	113		1457	S92	-5749	113
1358	S191	-4363	239		1408	S141	-5063	239		1458	S91	-5763	239
1359	S190	-4377	113		1409	S140	-5077	113		1459	S90	-5777	113
1360	S189	-4391	239		1410	S139	-5091	239		1460	S89	-5791	239
1361	S188	-4405	113		1411	S138	-5105	113		1461	S88	-5805	113
1362	S187	-4419	239		1412	S137	-5119	239		1462	S87	-5819	239
1363	S186	-4433	113		1413	S136	-5133	113		1463	S86	-5833	113
1364	S185	-4447	239		1414	S135	-5147	239		1464	S85	-5847	239
1365	S184	-4461	113		1415	S134	-5161	113		1465	S84	-5861	113
1366	S183	-4475	239		1416	S133	-5175	239		1466	S83	-5875	239
1367	S182	-4489	113		1417	S132	-5189	113		1467	S82	-5889	113
1368	S181	-4503	239		1418	S131	-5203	239		1468	S81	-5903	239
1369	S180	-4517	113		1419	S130	-5217	113		1469	S80	-5917	113
1370	S179	-4531	239		1420	S129	-5231	239		1470	S79	-5931	239
1371	S178	-4545	113		1421	S128	-5245	113		1471	S78	-5945	113
1372	S177	-4559	239		1422	S127	-5259	239		1472	S77	-5959	239
1373	S176	-4573	113		1423	S126	-5273	113		1473	S76	-5973	113
1374	S175	-4587	239		1424	S125	-5287	239		1474	S75	-5987	239
1375	S174	-4601	113		1425	S124	-5301	113		1475	S74	-6001	113
1376	S173	-4615	239		1426	S123	-5315	239		1476	S73	-6015	239
1377	S172	-4629	113		1427	S122	-5329	113		1477	S72	-6029	113
1378	S171	-4643	239		1428	S121	-5343	239		1478	S71	-6043	239
1379	S170	-4657	113		1429	S120	-5357	113		1479	S70	-6057	113
1380	S169	-4671	239		1430	S119	-5371	239		1480	S69	-6071	239
1381	S168	-4685	113		1431	S118	-5385	113		1481	S68	-6085	113
1382	S167	-4699	239		1432	S117	-5399	239		1482	S67	-6099	239
1383	S166	-4713	113		1433	S116	-5413	113		1483	S66	-6113	113
1384	S165	-4727	239		1434	S115	-5427	239		1484	S65	-6127	239
1385	S164	-4741	113		1435	S114	-5441	113		1485	S64	-6141	113
1386	S163	-4755	239		1436	S113	-5455	239		1486	S63	-6155	239
1387	S162	-4769	113		1437	S112	-5469	113		1487	S62	-6169	113
1388	S161	-4783	239		1438	S111	-5483	239		1488	S61	-6183	239
1389	S160	-4797	113		1439	S110	-5497	113		1489	S60	-6197	113
1390	S159	-4811	239		1440	S109	-5511	239		1490	S59	-6211	239
1391	S158	-4825	113		1441	S108	-5525	113		1491	S58	-6225	113
1392	S157	-4839	239		1442	S107	-5539	239		1492	S57	-6239	239
1393	S156	-4853	113		1443	S106	-5553	113		1493	S56	-6253	113
1394	S155	-4867	239		1444	S105	-5567	239		1494	S55	-6267	239
1395	S154	-4881	113		1445	S104	-5581	113		1495	S54	-6281	113
1396	S153	-4895	239		1446	S103	-5595	239		1496	S53	-6295	239
1397	S152	-4909	113		1447	S102	-5609	113		1497	S52	-6309	113
1398	S151	-4923	239		1448	S101	-5623	239		1498	S51	-6323	239
1399	S150	-4937	113		1449	S100	-5637	113		1499	S50	-6337	113
1400	S149	-4951	239		1450	S99	-5651	239		1500	S49	-6351	239

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No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
1501	S48	-6365	113		1551	DUMMY	-7067	113		1601	G97	-7867	113
1502	S47	-6379	239		1552	DUMMY	-7083	239		1602	G99	-7883	239
1503	S46	-6393	113		1553	G1	-7099	113		1603	G101	-7899	113
1504	S45	-6407	239		1554	G3	-7115	239		1604	G103	-7915	239
1505	S44	-6421	113		1555	G5	-7131	113		1605	G105	-7931	113
1506	S43	-6435	239		1556	G7	-7147	239		1606	G107	-7947	239
1507	S42	-6449	113		1557	G9	-7163	113		1607	G109	-7963	113
1508	S41	-6463	239		1558	G11	-7179	239		1608	G111	-7979	239
1509	S40	-6477	113		1559	G13	-7195	113		1609	G113	-7995	113
1510	S39	-6491	239		1560	G15	-7211	239		1610	G115	-8011	239
1511	S38	-6505	113		1561	G17	-7227	113		1611	G117	-8027	113
1512	S37	-6519	239		1562	G19	-7243	239		1612	G119	-8043	239
1513	S36	-6533	113		1563	G21	-7259	113		1613	G121	-8059	113
1514	S35	-6547	239		1564	G23	-7275	239		1614	G123	-8075	239
1515	S34	-6561	113		1565	G25	-7291	113		1615	G125	-8091	113
1516	S33	-6575	239		1566	G27	-7307	239		1616	G127	-8107	239
1517	S32	-6589	113		1567	G29	-7323	113		1617	G129	-8123	113
1518	S31	-6603	239		1568	G31	-7339	239		1618	G131	-8139	239
1519	S30	-6617	113		1569	G33	-7355	113		1619	G133	-8155	113
1520	S29	-6631	239		1570	G35	-7371	239		1620	G135	-8171	239
1521	S28	-6645	113		1571	G37	-7387	113		1621	G137	-8187	113
1522	S27	-6659	239		1572	G39	-7403	239		1622	G139	-8203	239
1523	S26	-6673	113		1573	G41	-7419	113		1623	G141	-8219	113
1524	S25	-6687	239		1574	G43	-7435	239		1624	G143	-8235	239
1525	S24	-6701	113		1575	G45	-7451	113		1625	G145	-8251	113
1526	S23	-6715	239		1576	G47	-7467	239		1626	G147	-8267	239
1527	S22	-6729	113		1577	G49	-7483	113		1627	G149	-8283	113
1528	S21	-6743	239		1578	G51	-7499	239		1628	G151	-8299	239
1529	S20	-6757	113		1579	G53	-7515	113		1629	G153	-8315	113
1530	S19	-6771	239		1580	G55	-7531	239		1630	G155	-8331	239
1531	S18	-6785	113		1581	G57	-7547	113		1631	G157	-8347	113
1532	S17	-6799	239		1582	G59	-7563	239		1632	G159	-8363	239
1533	S16	-6813	113		1583	G61	-7579	113		1633	G161	-8379	113
1534	S15	-6827	239		1584	G63	-7595	239		1634	G163	-8395	239
1535	S14	-6841	113		1585	G65	-7611	113		1635	G165	-8411	113
1536	S13	-6855	239		1586	G67	-7627	239		1636	G167	-8427	239
1537	S12	-6869	113		1587	G69	-7643	113		1637	G169	-8443	113
1538	S11	-6883	239		1588	G71	-7659	239		1638	G171	-8459	239
1539	S10	-6897	113		1589	G73	-7675	113		1639	G173	-8475	113
1540	S9	-6911	239		1590	G75	-7691	239		1640	G175	-8491	239
1541	S8	-6925	113		1591	G77	-7707	113		1641	G177	-8507	113
1542	S7	-6939	239		1592	G79	-7723	239		1642	G179	-8523	239
1543	S6	-6953	113		1593	G81	-7739	113		1643	G181	-8539	113
1544	S5	-6967	239		1594	G83	-7755	239		1644	G183	-8555	239
1545	S4	-6981	113		1595	G85	-7771	113		1645	G185	-8571	113
1546	S3	-6995	239		1596	G87	-7787	239		1646	G187	-8587	239
1547	S2	-7009	113		1597	G89	-7803	113		1647	G189	-8603	113
1548	S1	-7023	239		1598	G91	-7819	239		1648	G191	-8619	239
1549	DUMMY	-7037	113		1599	G93	-7835	113		1649	G193	-8635	113
1550	DUMMY	-7051	239		1600	G95	-7851	239		1650	G195	-8651	239

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No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
1651	G197	-8667	113										
1652	G199	-8683	239										
1653	G201	-8699	113										
1654	G203	-8715	239										
1655	G205	-8731	113										
1656	G207	-8747	239										
1657	G209	-8763	113										
1658	G211	-8779	239										
1659	G213	-8795	113										
1660	G215	-8811	239										
1661	G217	-8827	113										
1662	G219	-8843	239										
1663	G221	-8859	113										
1664	G223	-8875	239										
1665	G225	-8891	113										
1666	G227	-8907	239										
1667	G229	-8923	113										
1668	G231	-8939	239										
1669	G233	-8955	113										
1670	G235	-8971	239										
1671	G237	-8987	113										
1672	G239	-9003	239										
1673	DUMMY	-9019	113										
1674	DUMMY	-9035	239										

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6.5. DISPLAY MODULE DEFAULT POSITION

The default position (display driver, glass, filter order, etc) of the display module is always as follow, when MADCTL's (36h) parameter is 00h. The color filter is always RGB (if color filters are used).

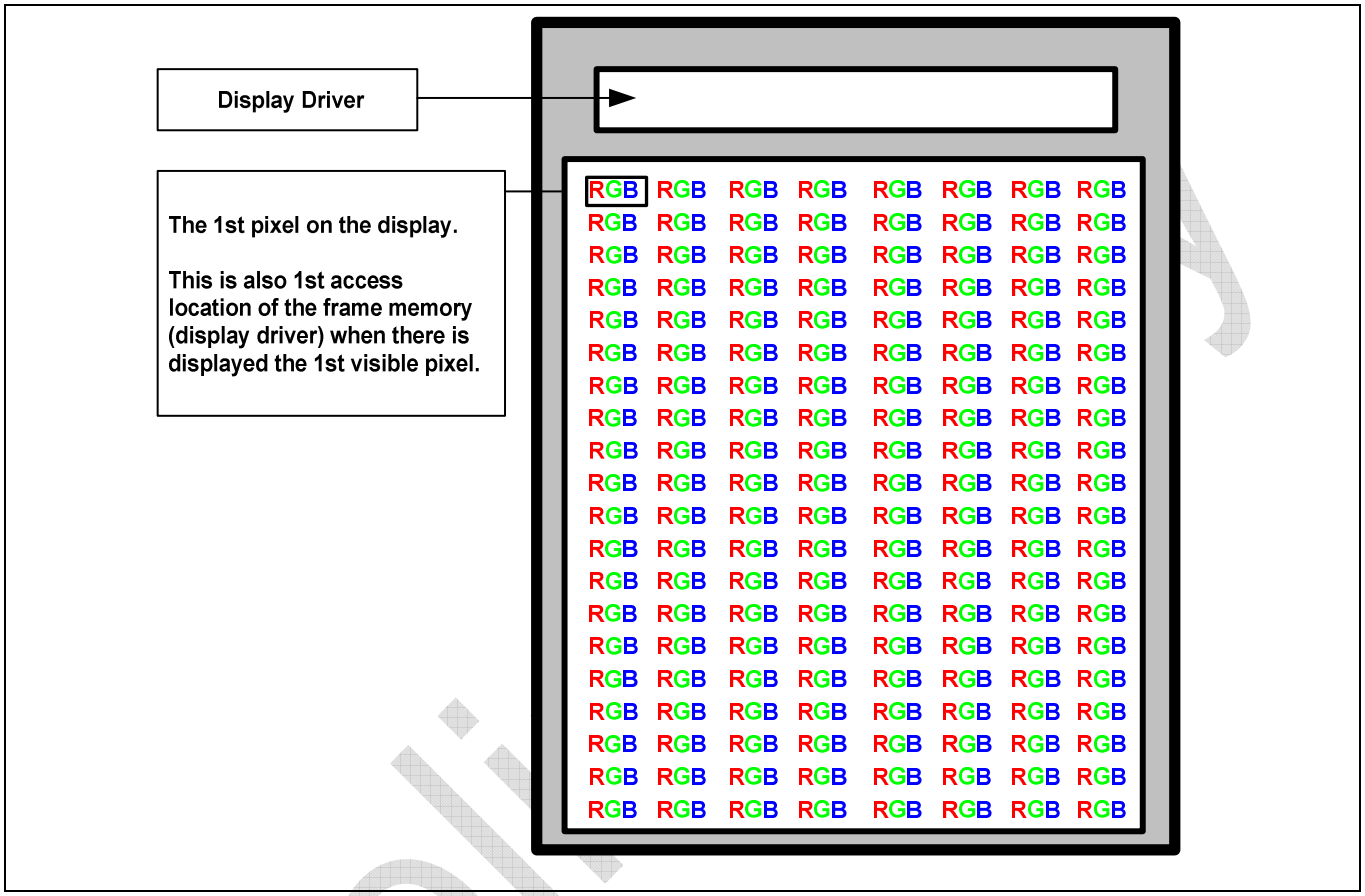

Figure136. Display Module Default Position

Preliminary

With collaboration of https://www.displayfuture.com