OVERVIEW

The NT7450 family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The drivers are available in two configurations. The NT7450 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.
These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

- The NT7450 which is able to drive two lines of twelve characters each.
- The NT7451 which is able to drive 80 segments for extention.

FEATURES

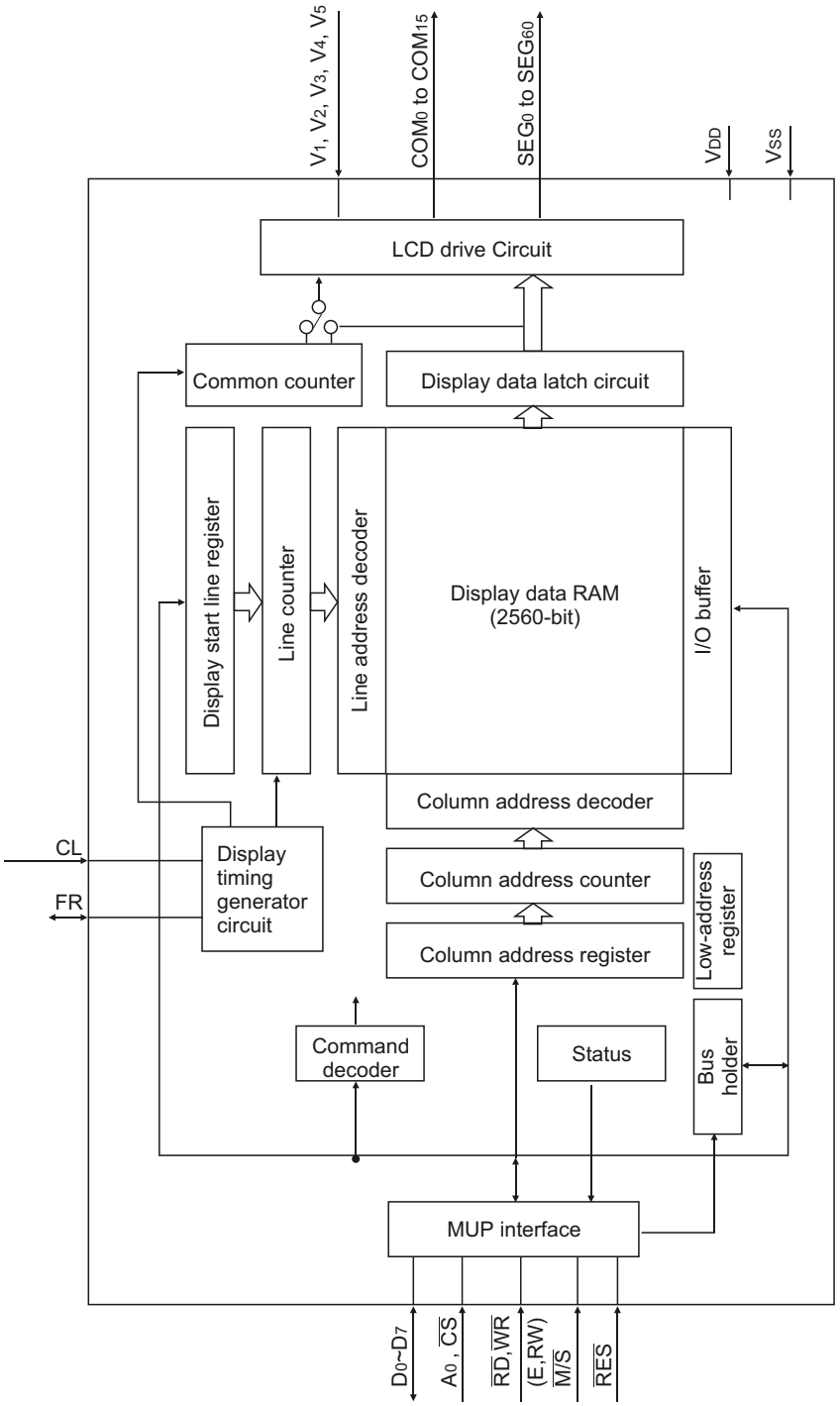
- Fast 8-bit MPU interface compatible with 80-and 68-family microcomputers
- Many command set
- Total 80 (segment+common) drive sets
- Low power—30 μW at 2 kHz external clock
- Wide range of supply voltages
  VDD-Vss : +2.7~+5.5V
  VDD-V5 : +3.5~+13.0V
- Low-power CMOS

Line-up

Product Name	Clock Frequency		Applicable Driver	Number of SEG Drivers	Number of CMOS Drivers	Duty
	On-Chip	External				
NT7450OA	18kHz	18kHz	NT7450OA , NT7451OA	61	16	1/16 , 1/32
NT7451OA	-	18kHz	NT7450OA	80	0	1/8 to 1/32
NT7450AA	-	2kHz	NT7450OA , NT7451OA	61	16	1/16 , 1/32
NT7451AA	-	2kHz	NT7450OA	80	0	1/8 to 1/32

BLOCK DIAGRAM

An example of NT7450AA



PIN DESCRIPTION

(1) Power Pins

Name	Description
V_{DD}	Connected to the +5V dc power. Common to the Vcc MPU power pin.
V_{SS}	0 Vdc pin connected to the system ground.
V_1, V_2, V_3, V_4, V_5	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$

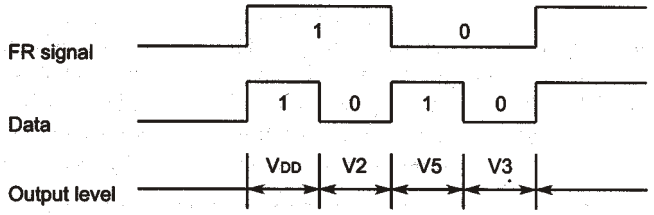
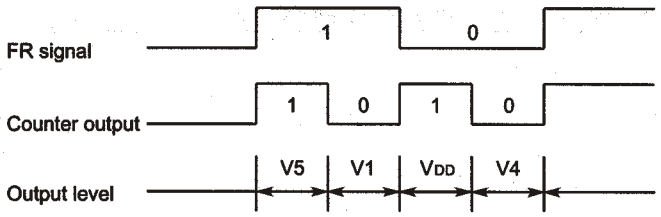
(2) System Bus Connection Pins

D7 to D0	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: D0 to D7 are display control data. A0=1: D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ⌐└⌐ the 68-series MPU is initialized, and when it goes _┌└_ , the 80-series MPU is initialized. The system is reset during edge sense of the $\overline{RES}$ signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows:High level: 68-series MPU interface Low level : 80-series MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only. An address bus signal is usually decoded by use of chip select signal, and it is entered. If the system has a built-in oscillator, this is used as an input pin to the oscillator amp and an Rf oscillator resistor is connected to it. In such case, the $\overline{RD}$, $\overline{WR}$ and E signals must be $\overline{OR}$ed with the $\overline{CS}$ signals and entered.
E ($\overline{RD}$)	· <u>If the 68-series MPU is connected:</u> Input. Active high. Used as an enable clock input of the 68-series MPU. · <u>If the 80-series MPU is connected:</u> Input. Active low. The $\overline{RD}$ signal of the 80series MPU is entered in this pin. When this signal is kept low, the NT7450 data bus is in the the output status.
R/W ($\overline{WR}$)	· If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is high) or write control signals (if low). · If the 80-series MPU is connected: Input. Active low. The $\overline{WR}$ signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of $\overline{WR}$ signal.

Product Name	Pad Number					
	74	75	96 to 100, 1 to 11	93	94	95
NT7450OA	OSC1	OSC2	COM0 to COM15*	M/S	V4	V1
NT7451OA	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
NT7450AA	CS	CL	COM0 to COM15*	M/S	V4	V1
NT7451AA	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77

NT7450: Common outputs COM0 to COM15 of the master LSI correspond to COM31 to COM16 of the slave LSI.

(3) LCD Drive Circuit Signals

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>CL</td><td>Input. Effective for an external clock operation model only.
This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges. If the system has a built-in oscillator. this is used as an output pin for the oscillator amp and an Rf oscillator resistor is connected to it.</td></tr>
<tr><td>FR</td><td>Input/output.
This is an I/P pin of LCD AC signals, and connected to the M terminal of common driver.
I/O selection
· Common oscillator buit-in model: Output if M/S is 1;
Intput if M/S is 0
· Dedicate segment model: Input</td></tr>
<tr><td>SEGn</td><td>Output.
The output pin for LCD column (segment) driving. A single level of V_{DD}, V_2, V_3 and V_5 is selected by the combination of display RAM contents and RF signal.
 
</td></tr>
<tr><td>COMn</td><td>Output.
The Output pin for LCD common (low) driving. A single level of V_{DD}, V_1, V_4 and V_5 is selected by the combination of common counter output and RF signal. The slave LSI has the reverse common output scan sequence than the master LSI.
 
</td></tr>
<tr><td>M/S</td><td>Input.
The master or slave LSI operation select pin for the NT7450.
Connected to V_{DD} (to select the master LSI operation mode) or Vss (to select the slave LSI operation mode).
When this M/S pin is set, the functions of FR, COM0 to COM15, OSC1 ($\overline{CS}$), and OSC2 (CL) pins are changed.
NT7450OA
<table>
<tr><th>M/S</th><th>FR</th><th>COM output</th><th>OSC1</th><th>OSC2</th></tr>
<tr><td>V_{DD}</td><td>Output</td><td>COM0 to COM15</td><td>Input</td><td>Output</td></tr>
<tr><td>Vss</td><td>Input</td><td>COM31 to COM16</td><td>NC</td><td>Input</td></tr>
</table>
*The slave driver has the reverse common output scan sequence than the master driver.</td></tr>
</table>

BLOCK DESCRIPTION

System Bus

MPU interface

1.Selecting an interface type

The NT7450 series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of high or low $\overline{RES}$ signal level after reset (see Table 1).

When the $\overline{CS}$ signal is high, the NT7450 series is disconnected from the MPU bus and set to stand by. However, the reset signal is entered regardless of the internal setup status.

Table1

$\overline{RES}$ signal input level	MPU type	A0	E	R/W	CS	D0 to D7
Active low	68-series	↑	↑	↑	↑	↑
Active high	80-series	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

Data transfer

The NT7450 and NT7451 drivers use the A0, E(or $\overline{RD}$) and R/W (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow.

In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.

No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	WR	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

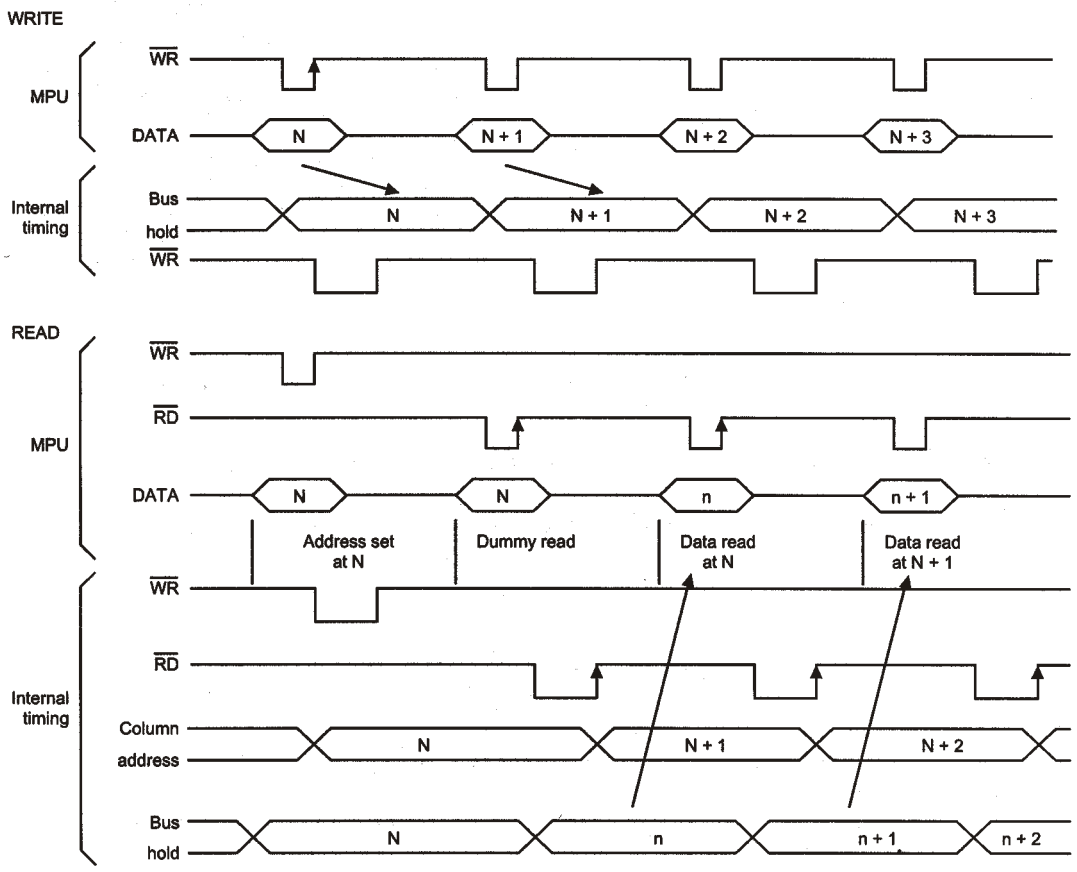


Figure 1 Bus Buffer Delay

Data transfer

When the Busy flag is logical 1, the NT7450 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and , therefore, the MPU processing capacity can greatly be enhanced.

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command.

The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

Column Address Counter

The column address counter is a 7-bit preset table counter that supplies the column address for MPU access to the display data RAM. See figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

Page Register

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

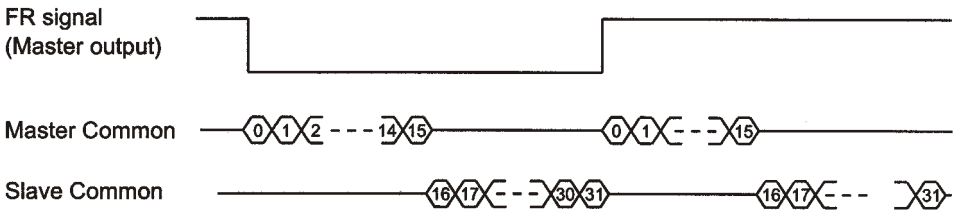
Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2.

Common Timing Generator Circuit

Generates common timing signals and FR frame signals from the CL basic clock. The 1/16 or 1/32 duty (for NT7450) can be selected by the Duty Select command. If the 1/32 duty is selected for the NT7450 the 1/32 duty is provided by two chips consisting of the master and slave chips in the common multi-chip mode.

NT7450



Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF and Static Drive ON/OFF commands.

LCD Driver Circuit

The LCD driver circuitry generates the 80-4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

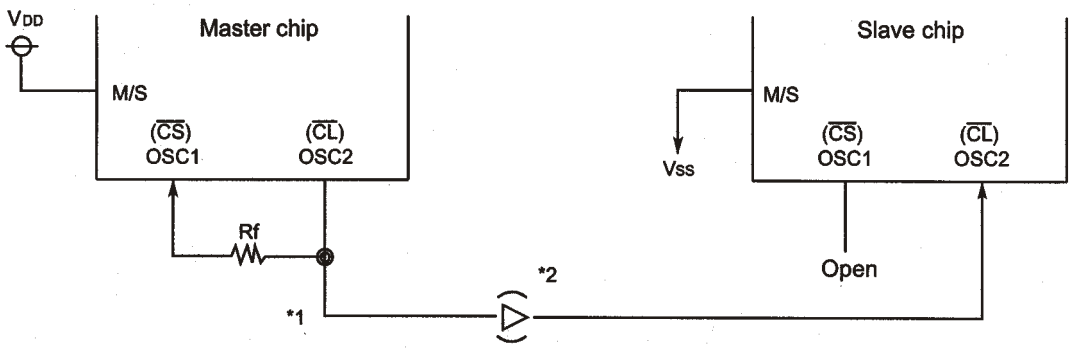
Display Timing Generator

This circuit generates the internal display timing signal using the basic clock, CL, and the frame signals, FR.
FR is used to generate the dual frame AC-drive wave-from (type B drive) and to lock the line counter and common timing generator to the system frame rate.
CL is used to lock the line counter to the system line scan rate. If a system uses both NT7450s and NT7451s they must have the same CL frequency rating.

Oscillator Circuit (NT7450OA)

A low power-consumption CR oscillator for adjusting the oscillation frequency using Rf oscillation resistor only. This circuit generates a display timing signal. Some of NT7450 series models have a built-in oscillator and others use an external clock. This difference must be checked before use.
Connect the Rf oscillation resistor as follows. To suppress the built-in oscillator circuit and drive the MPU using an external clock, the clock having the same phase as the OSC2of mater chip into OSC2 of the slave chip.

· MPU having a built-in oscillator



*1 If the parasitic capacitance of this section increases, the oscillation frequency may shift to the lower frequency. Therefore, the Rf oscillation frequency must be reduced below the specified level.
*2 A CMOS buffer is required if the oscillation circuit is connected to two or more slave MPU chips.

Resst Cricuit

Detects a rising or falling edge of an $\overline{RES}$ input and initializes the MPU during power-on.

· Initialization status

1. Display is off.
2. Display start line register is set to line 1.
3. Static drive is turned off.
4. Column address counter is set to address 0.
5. Page address register is set to page 3.
6. 1/32 duty NT7450 is selected.
7. Forward ADC is selected (ADC command D0 is 0 and ADC status flag is 1).
8. Read-modify-write is turned off.

The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1.
For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.
As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.
If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.
When the Reset command id issued, initialization.

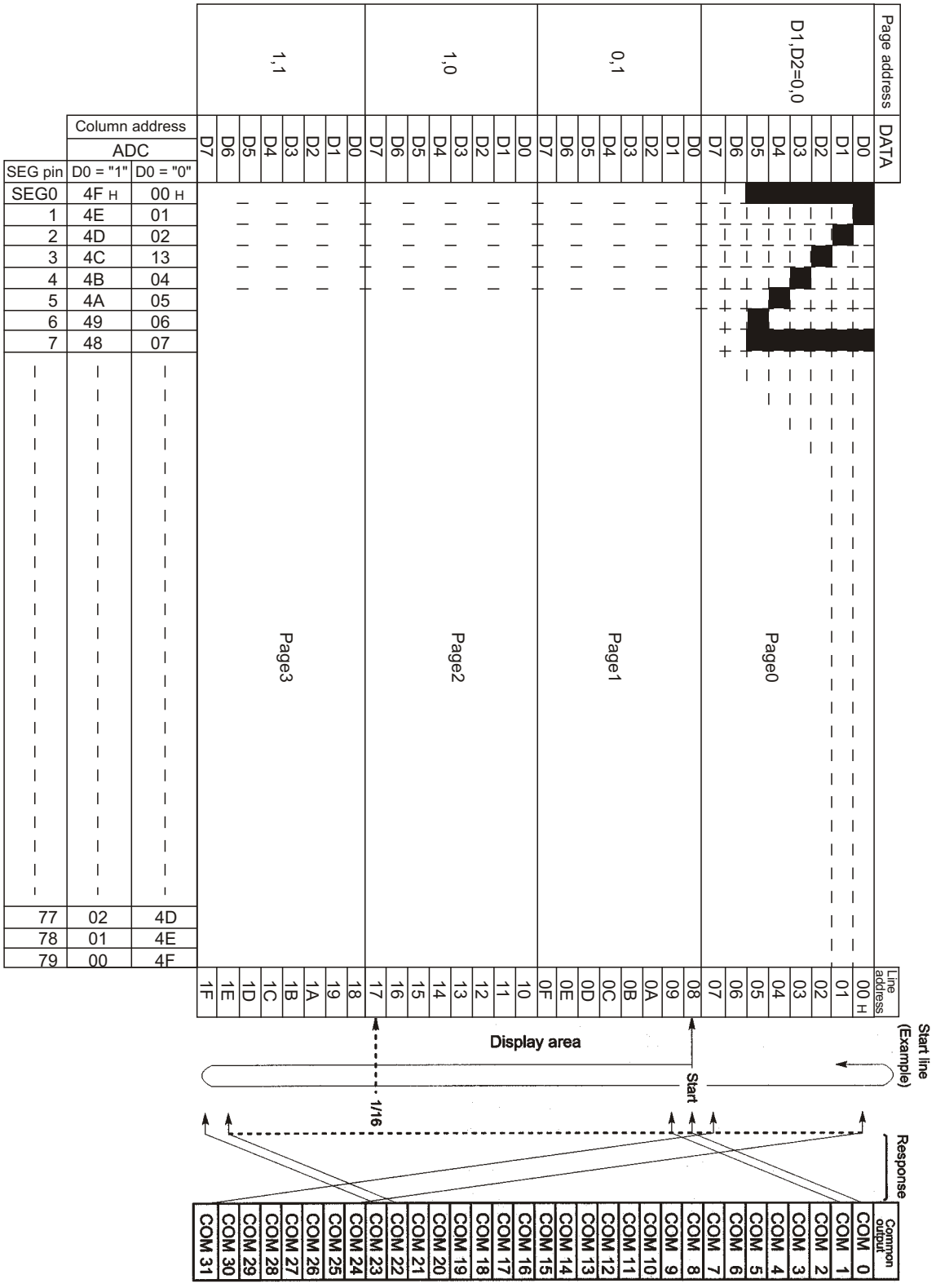


Figure 2 Display Data RAM Addressing

1/5 bias, 1/16 duty
1/6 bias, 1/32 duty

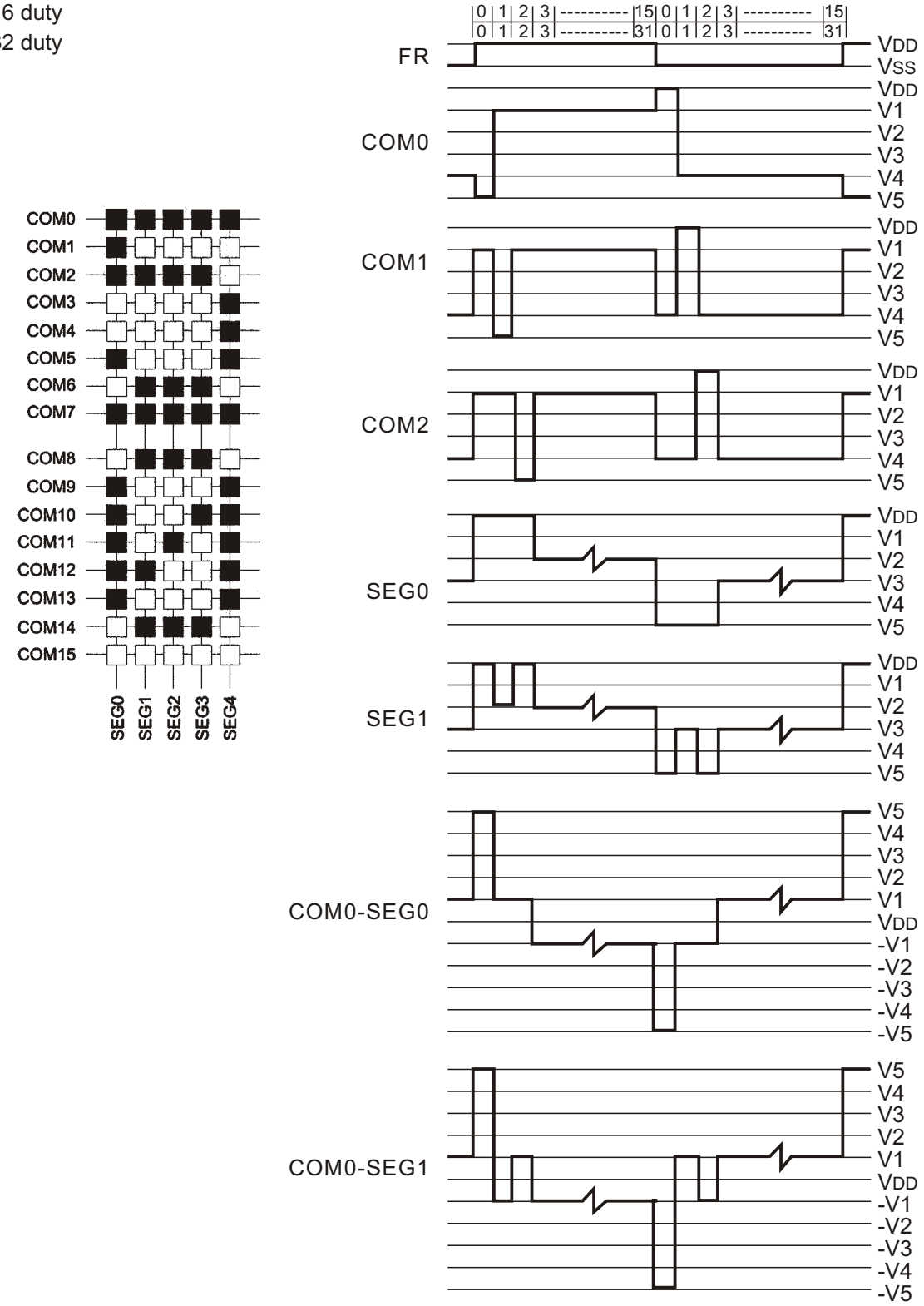


Figure 4 LCD drive waveforms example

COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display On/Off	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (Segment) address	0	1	0	0	Column address (0 to 79)							Sets Display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output NO/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Nomal
Write display data	1	1	0									Writes data from data bus into display RAM.
Read display data	1	0	1									Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0:CW output, 1:CCW output
Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1:Static frive, 0:Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1:1/32, 0:1/16
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description

Table 3 is the command table. The NT7450 series identifies a data bus using a combination of A0 and R/W (RD or WR) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

Display ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	0	1	0	1	1	1	D	AEH,AFH

This command turns the display on and off .

- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	0	A4	A3	A2	A1	A0	C0H to DFH

This command loads the display start line register.

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	0	1
					⋮
					⋮
1	1	1	1	1	31

See Figure 2.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H to BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	A6	A5	A4	A3	A2	A1	A0	00H to 4FH

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
							:
							:
1	0	0	1	1	1	1	79

Read Status

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	$\overline{0}$	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-u →segment driver u.
- The ON/OFF bit indicates the current status of the disply.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operation mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

Write Display Data

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	Write data							

Read Display Data

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	$\overline{0}$	1	Read data							

Reads 8-bit of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH,...(inverted)
D=0: SEG0 ← column address 00H,...(normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

Select Duty

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the NT7450. It is invalid for the NT7451 which performs passive operation. The duty cycle of the NT7451 is determined by the externally generated FR signal.
NT7450
D=1: 1/32 duty cycle
D=0: 1/16 duty cycle
When using the NT7450OA, (having a built-in oscillator) and the NT7451OA continuously, set the duty as follows:l

NT7450OA	NT7451OA
1/32	1/32
1/16	1/16

Read-Modify-Write

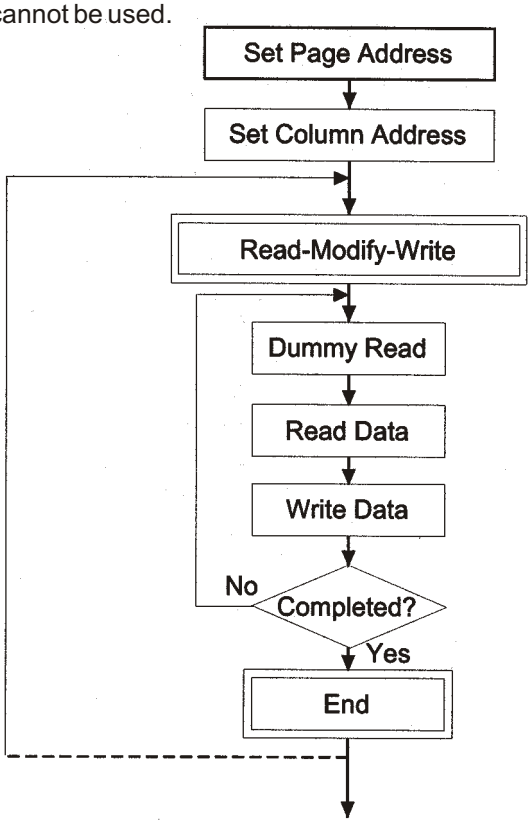
A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-incerment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

· Operation wequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This Function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

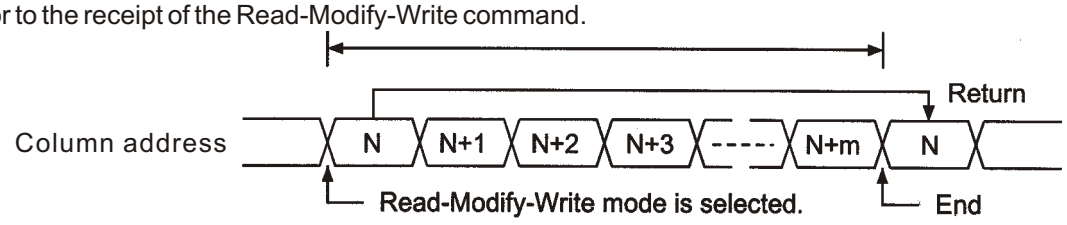
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



End

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



Reset

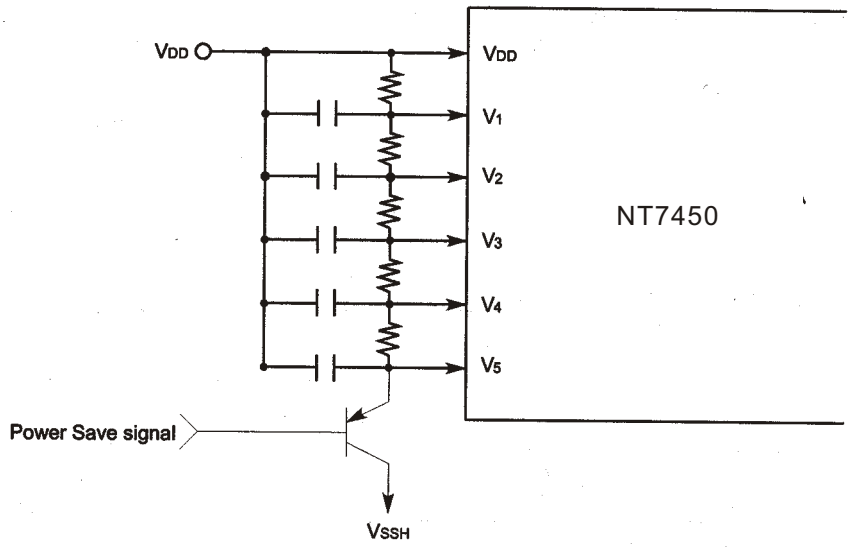
A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears
- the display start line register.
- and set page address register to 3 page.

It does not affect the contents of the display data RAM.
When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command connot be used instead of this Reset signal.

Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the V_{DD} level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



If the LCD drive power is generated by resistance division, the resistance and capacitance are determined by the LCD panel size. After the panel size has been determined, reduce the resistance to the level where the display quality is not affected and reduce the power consumption using the divider resistor.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage(1)	Vss	-8.0 to +0.3	V
Supply voltage(2)	V5	-16.5 to +0.3	V
Supply voltage(3)	V1,V4,V2,V3	V5 to +0.3	V
Input voltage	V_{IN}	Vss-0.3 to +0.3	V
Output voltage	V_O	Vss-0.3 to +0.3	V
Power dissipation	P_D	250	mW
Operating temperature	Topr	-40 to +85	deg. C
Storage temperature	Tstg	-65 to +150	deg. C
Soldering temperature time at lead	Tsol	260, 10	deg. C, sec

Notes: 1. All voltages are specified relative to VDD=0V.

2. The following relation must be always hold
   $V_{DD} \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

Ta=-20 to 75 deg. C, V_{DD}=0V unless stated otherwise

Parameter		Symbol	Condition		Rating			Unit	Applicable Pin
					Min.	Typ.	Max.		
Operating voltage(1) See note1. Recommended		Vss			-5.5	-	-2.7	V	Vss
Operating voltage(2)	Recommended	V5			-13.0	-	-3.5	V	V5
	Allowable				-13.0	-	-		See note 10.
	Allowable	V1,V2			0.6xV5	-	V_{DD}	V	V1,V2
	Allowable	V3,V4			V5	-	0.4xV5	V	V3,V4
High-level input voltage		V_{IHT}			Vss+2.0	-	V_{DD}	V	See note 2 & 3.
		V_{IHC}			0.2xVss	-	V_{DD}		
		V_{IHT}	Vss=-3V		0.2xVss	-	V_{DD}		See note 2 & 3.
		V_{IHC}	Vss=-3V		0.2xVss	-	V_{DD}		
Low-level input voltage		V_{ILT}			Vss		Vss+0.8		See note 2 & 3.
		V_{ILC}			Vss		0.8xVss		
		V_{ILT}	Vss=-3V		Vss		0.85xVss		See note 2 & 3.
		V_{ILC}	Vss=-3V		Vss		0.8xVss		
Hight-level output voltage		V_{OHT}	I_{OH}=-3.0mA		Vss+2.4	-	-	V	OSC2 See note 4 & 5.
		V_{OHC1}	I_{OH}=-2.0mA		Vss+2.4	-	-		
		V_{OHC2}	I_{OH}=-120 μA		0.2xVss	-	-		
		V_{OHT}	Vss=-3V	I_{OH}=-2mA	0.2xVss			V	See note 4 & 5. OSC2
		V_{OHC1}	Vss=-3V	I_{OH}=-2mA	0.2xVss				
		V_{OHC2}	Vss=-3V	I_{OH}=-2 μA	0.2xVss				

DC Characteristics(Cont'd)

Ta=-20 to 75 deg. C, V_{DD}=0V unless stated otherwise

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Pin
Low-level output voltage	V_{OLT}	I_{OL} = 3.0mA		-	-	Vss+0.4	V	OSC2 See note 4 & 5.
	V_{OLC1}	I_{OL} = 2.0mA		-	-	Vss+0.4		
	V_{OLC2}	I_{OL} = 120 μA		-	-	0.8xVss		
	V_{OLT}	Vss = -3V	I_{OL} = 2mA			0.8xVss	V	See note 4 & 5. OSC2
	V_{OLC1}	Vss = -3V	I_{OL} = 3mA			0.8xVss		
	V_{OLC2}	Vss = -3V	I_{OL} = 50 μA			0.8xVss		
Input leakage current	I_{IL1}			-1.0	-	1.0	μA	See note 6.
Output leakage current	I_{IL0}			-3.0	-	3.0	μA	See note 7.
LCD driver ON resistance	R_{ON}	Ta = 25deg. C	V5 = -5.0V	-	-	7.5	kΩ	SEG0 to 79, COM0 to 15, See note 11
			V5 = -3.5V	-	-	50.0		
Static current dissipation	I_{DDQ}	CS = CL = VDD		-	-	1.0	μA	V_{DD}
Dynamic current dissipation	$I_{DD(1)}$	During display V5 = -5.0V	f_{CL} = 2kHz	-	-	10	μA	V_{DD} See note 12, 13 & 14.
			Rf = 1MΩ	-	-	40		
			f_{CL} = 18kHz	-	-	25		
		During display V5 = -5V Vss = -3V	f_{CL} = 2kHz		-	9	μA	VDD See note 12 & 13.
			Rf = 1MΩ		-	25		
	$I_{DD(2)}$	During access tycy = 200kHz		-	300	500	μA	See note 8.
		Vss = -3V, Druing access tcyc = 200kHz			150	300		
Input leakage current	C_{IN}	Ta = 25 deg. C, f = 1 MHz		-	5.0	8.0	pF	All input pins
Oscillation frequency	fosc	Rf = 1.0MΩ $\pm$ 2% Vss = -0.5V Rf = 1.0MΩ $\pm$ 2% Vss = -3.0V		15 11	18 16	21 21	kHz	See note 9.
Reset time	tR			1.0	-		μs	RES See note 15.

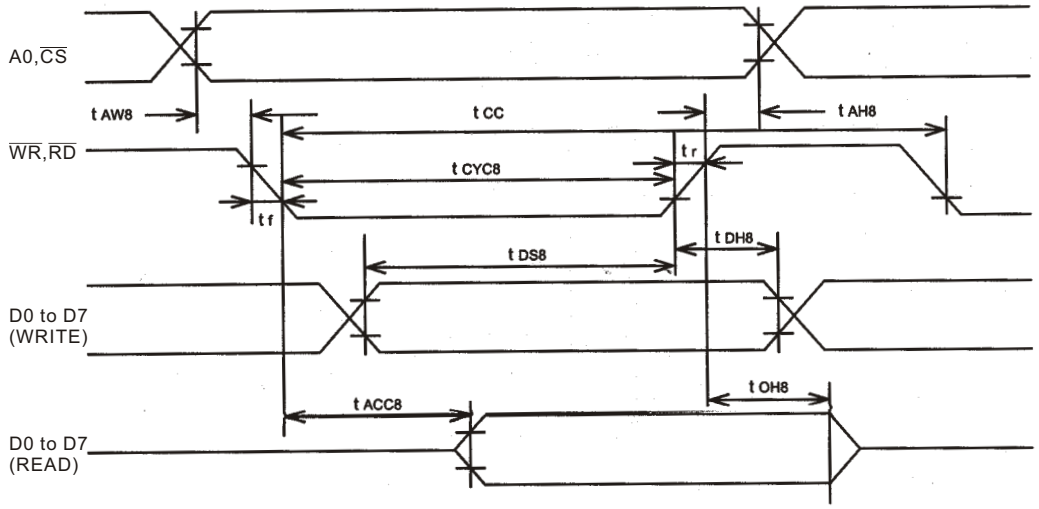
Notes: 1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.

2. A0, D0 to D7, E(or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL, M/$\overline{S}$ and $\overline{RES}$

7. When D0 to D7 and FR are high impedance.
8. During continual write access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V1,..., V4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
12. NT7450 and NT7451 only. Does not include transient currents due to stray and panel capacitances.
13. NT7450 only. Does not include transient currents due to stray and panel capacitances.
14. NT7451 only. Does not include transient currents due to stray and panel capacitances.
15. tR (Rest time) represents the time from the RES signal edge to the completion of rest of the internal circuit. Therefore, the NT7450 series enters the normal operation status after this tR.

AC Characteristics

· MPU Bs Read/Write I (in-family MPU)



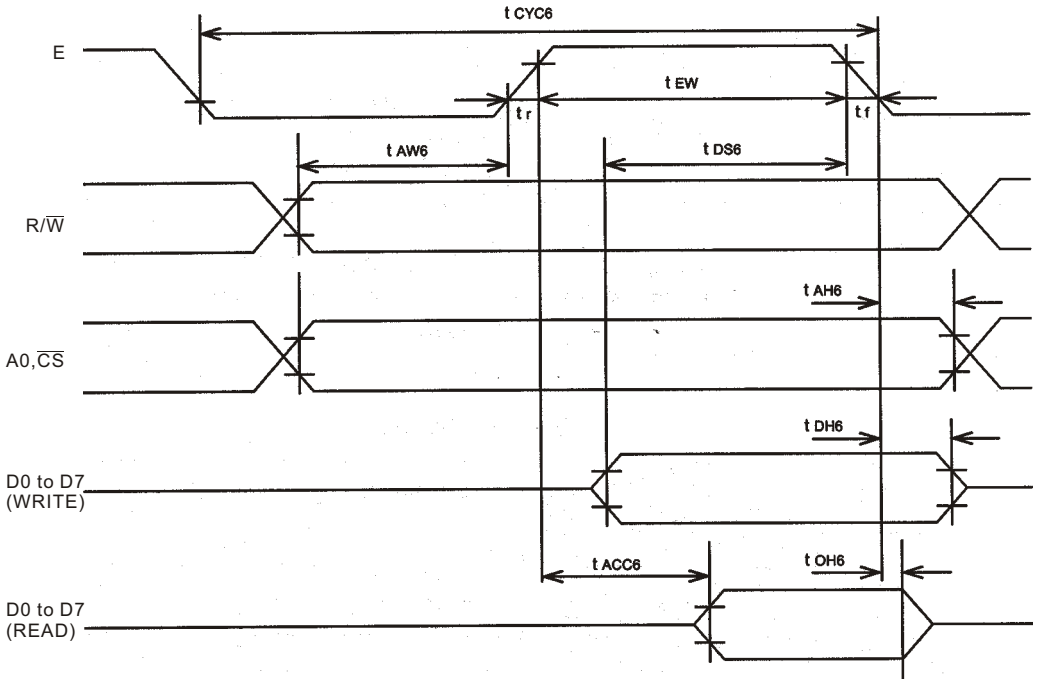
Ta=-20 to 75 deg. C, Vss=-5.0V± 10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	t_{AH8}		10	-	ns	A0, CS
Address setup time	t_{AW8}		20	-	ns	
System cycle time	t_{CYC8}		1000	-	ns	$\overline{WR}$,$\overline{RD}$
Control pulsewidth	t_{CC}		200	-	ns	
Data setup time	t_{DS8}		80	-	ns	D0 to D7
Date hold time	t_{DH8}		10	-	ns	
$\overline{RD}$ access time	t_{ACC8}	C_{L}=100pF	-	90	ns	
Output disable time	t_{CH8}		10	60	ns	
Rise and fall time	tr, tf	-	-	15	ns	-

(Vss=-2.7 to -4.5V, Ta=-20 to +75℃)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	t_{AH8}		20	-	ns	A0, CS
Address setup time	t_{AW8}		40	-	ns	
System cycle time	t_{CYC8}		2000	-	ns	$\overline{WR}$,$\overline{RD}$
Control pulsewidth	t_{CC}		400	-	ns	
Data setup time	t_{DS8}		160	-	ns	D0 to D7
Date hold time	t_{DH8}		20	-	ns	
$\overline{RD}$ access time	t_{ACC8}	C_{L}=100pF	-	180	ns	
Output disable time	t_{CH8}		20	120	ns	
Rise and fall time	tr, tf	-	-	15	ns	-

· MPU Bs Read/Write II (68-family MPU)



Ta=-20 to 75 deg. C, Vss=-5.0V± 10% unless stated otherwise

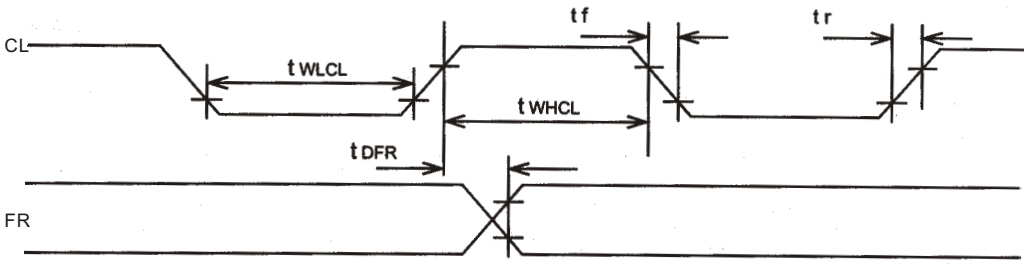
Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		tCYC6		1000	-	ns	A0, CS,R/W
Address setup time		tAW6		20	-	ns	
Address hold time		tAH6		10	-	ns	
Data setup time		tDS6		80	-	ns	D0 to D7
Data hold time		tDH6		10	-	ns	
Output disable time		tOH6	CL=100pF	10	60	ns	
Access time		tACC6		-	90	ns	
Enable pulsewidth	Read	tEW		100	-	ns	E
	Write			80	-	ns	
Rise and fall time		tr, tf	-	-	15	ns	-

(Vss=-2.7 to -4.5V, Ta=-20 to +75℃)

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time*1		tCYC6		2000	-	ns	A0, CS,R/W
Address setup time		tAW6		40	-	ns	
Address hold time		tAH6		20	-	ns	
Data setup time		tDS6		160	-	ns	D0 to D7
Data hold time		tDH6		20	-	ns	
Output disable time		tOH6	CL=100pF	20	120	ns	
Access time		tACC6		-	180	ns	
Enable pulsewidth	Read	tEW		200	-	ns	E
	Write			160	-	ns	
Rise and fall time		tr, tf	-	-	15	ns	-

Notes:1.tcyc6 is the cycle time of CS. E=H, not the cycle time of E.

· Display Control Signal Timing



Input

Ta=-20 to 75 deg. C, Vss=-5.0V± 10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulsewidth	tWLCL		35	-	-	μs	CL
High-level pulsewidth	tWHCL		35	-	-	μs	
Rise time	tr		-	30	150	n s	
Fall time	tf		-	30	150	n s	
FR delay time	tDFR		-2.0	0.2	2.0	μs	FR

Vss=-2.7 to -4.5V , Ta=-20 to +75℃

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulsewidth	tWLCL	-	70	-	-	μs	CL
High-level pulsewidth	tWHCL	-	70	-	-	μs	
Rise time	tr	-	-	60	300	n s	
Fall time	tf	-	-	60	300	n s	
FR delay time	tDFR	-	-4.0	0.4	4.0	μs	FR

Note: The listed input tDFR applies to the NT7450 and NT7451 in slave mode.

Output

Ta=-20 to 75 deg. C, Vss=-5.0V± 10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delary time	tDFR	CL=100pF	-	0.2	0.4	μs	FR

Vss=-2.7 to -4.5V , Ta=-20 to +75℃

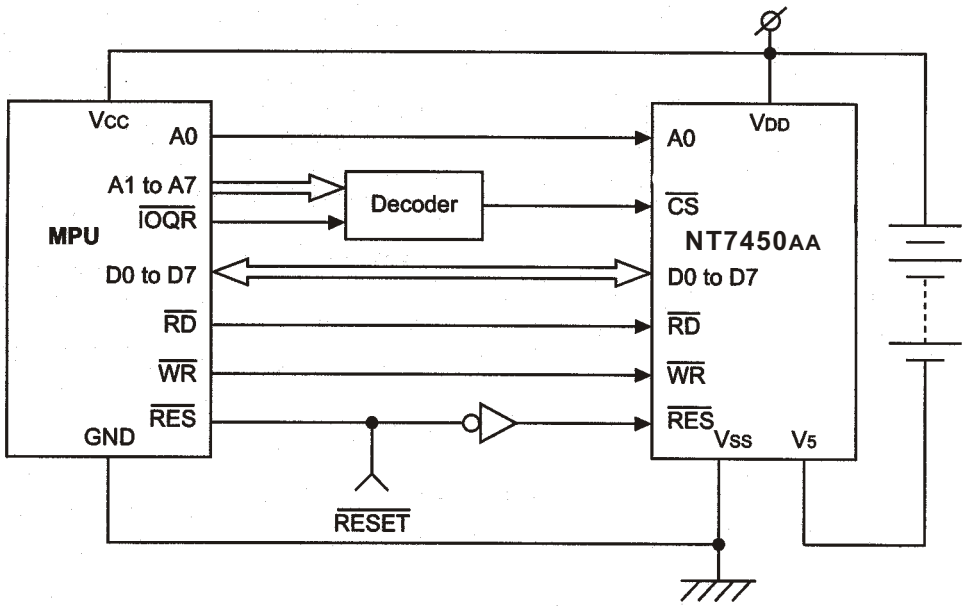
Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delary time	tDFR	CL=100pF	-	0.4	0.8	μs	FR

Note: The listed input tDFR applies to the NT7450 and NT7451 in slave mode.

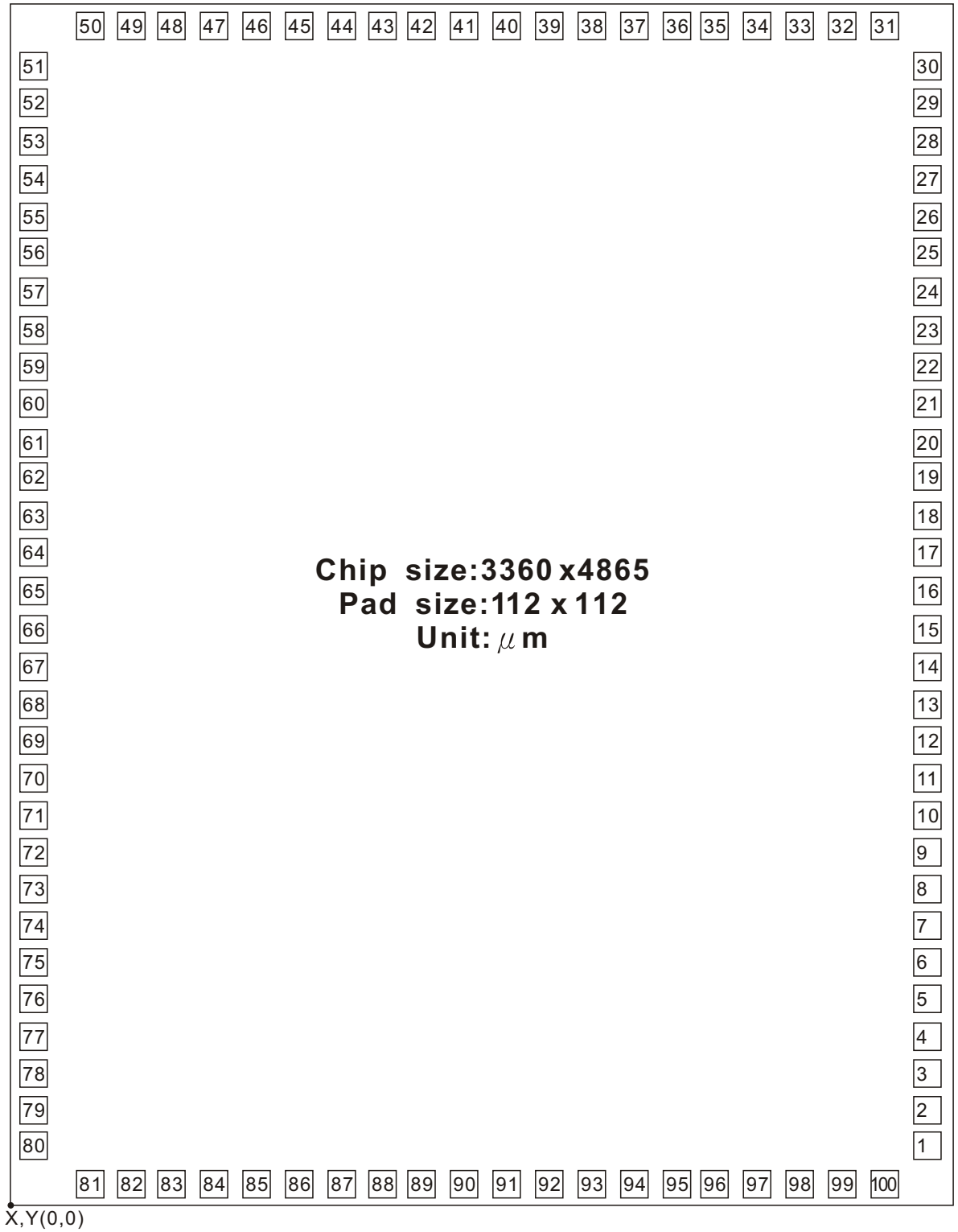
APPLICATION NOTES

MPU Interface Configuration

80 Family MPU



PAD DIAGRAM


50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31
51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100
Chip size:3360 x4865
Pad size:112 x 112
Unit: μm
X,Y(0,0)

PAD DIAGRAM(NT7450)

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	COM5	3264	380	51	SEG21	95	4481
2	COM6	3264	522	52	SEG20	95	4340
3	COM7	3264	663	53	SEG19	95	4198
4	COM8	3264	805	54	SEG18	95	4057
5	COM9	3264	946	55	SEG17	95	3915
6	COM10	3264	1087	56	SEG16	95	3774
7	COM11	3264	1229	57	SEG15	95	3633
8	COM12	3264	1370	58	SEG14	95	3491
9	COM13	3264	1512	59	SEG13	95	3350
10	COM14	3264	1653	60	SEG12	95	3208
11	COM15	3264	1794	61	SEG11	95	3067
12	SEG60	3264	1936	62	SEG10	95	2926
13	SEG59	3264	2077	63	SEG9	95	2784
14	SEG58	3264	2219	64	SEG8	95	2643
15	SEG57	3264	2360	65	SEG7	95	2501
16	SEG56	3264	2501	66	SEG6	95	2360
17	SEG55	3264	2643	67	SEG5	95	2219
18	SEG54	3264	2784	68	SEG4	95	2077
19	SEG53	3264	2926	69	SEG3	95	1936
20	SEG52	3264	3067	70	SEG2	95	1794
21	SEG51	3264	3208	71	SEG1	95	1653
22	SEG50	3264	3350	72	SEG0	95	1512
23	SEG49	3264	3491	73	A0	95	1334
24	SEG48	3264	3633	74	OSC1*/CS	95	1194
25	SEG47	3264	3774	75	OSC2*/CL	95	1054
26	SEG46	3264	3915	76	$\overline{RD}$	95	914
27	SEG45	3264	4057	77	$\overline{WR}$	95	874
28	SEG44	3264	1498	78	Vss	95	634
29	SEG43	3264	4340	79	DB0	95	494
30	SEG42	3264	4481	80	DB1	95	354
31	SEG41	3037	4474	81	DB2	385	95
32	SEG40	2895	4474	82	DB3	526	95
33	SEG39	2754	4474	83	DB4	681	95
34	SEG38	2612	4474	84	DB5	826	95
35	SEG37	2471	4474	85	DB6	974	95
36	SEG36	2330	4474	86	Db7	1117	95
37	SEG35	2188	4474	87	V_{DD}	1257	95
38	SEG34	2047	4474	88	$\overline{RES}$	1397	95
39	SEG33	1905	4474	89	FR	1537	95
40	SEG32	1764	4474	90	V5	1679	95
41	SEG31	1623	4474	91	V3	1820	95
42	SEG30	1481	4474	92	V2	1962	95
43	SEG29	1340	4474	93	M/S	2097	95
44	SEG28	1198	4474	94	V4	2231	95
45	SEG27	1057	4474	95	V1	2365	95
46	SEG26	916	4474	96	COM0	2500	95
47	SEG25	774	4474	97	COM1	2634	95
48	SEG24	633	4474	98	COM2	2769	95
49	SEG23	491	4474	99	COM3	2903	95
50	SEG22	350	4474	100	COM4	3037	95

PAD DIAGRAM(NT7451)

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	SEG71	3264	380	51	SEG21	95	4481
2	SEG70	3264	522	52	SEG20	95	4340
3	SEG69	3264	663	53	SEG19	95	4198
4	SEG68	3264	805	54	SEG18	95	4057
5	SEG67	3264	946	55	SEG17	95	3915
6	SEG66	3264	1087	56	SEG16	95	3774
7	SEG65	3264	1229	57	SEG15	95	3633
8	SEG64	3264	1370	58	SEG14	95	3491
9	SEG63	3264	1512	59	SEG13	95	3350
10	SEG62	3264	1653	60	SEG12	95	3208
11	SEG61	3264	1794	61	SEG11	95	3067
12	SEG60	3264	1936	62	SEG10	95	2926
13	SEG59	3264	2077	63	SEG9	95	2784
14	SEG58	3264	2219	64	SEG8	95	2643
15	SEG57	3264	2360	65	SEG7	95	2501
16	SEG56	3264	2501	66	SEG6	95	2360
17	SEG55	3264	2643	67	SEG5	95	2219
18	SEG54	3264	2784	68	SEG4	95	2077
19	SEG53	3264	2926	69	SEG3	95	1936
20	SEG52	3264	3067	70	SEG2	95	1794
21	SEG51	3264	3208	71	SEG1	95	1653
22	SEG50	3264	3350	72	SEG0	95	1512
23	SEG49	3264	3491	73	A0	95	1334
24	SEG48	3264	3633	74	OSC1*/CS	95	1194
25	SEG47	3264	3774	75	OSC2*/CL	95	1054
26	SEG46	3264	3915	76	$\overline{RD}$	95	914
27	SEG45	3264	4057	77	$\overline{WR}$	95	874
28	SEG44	3264	1498	78	Vss	95	634
29	SEG43	3264	4340	79	DB0	95	494
30	SEG42	3264	4481	80	DB1	95	354
31	SEG41	3037	4474	81	DB2	385	95
32	SEG40	2895	4474	82	DB3	526	95
33	SEG39	2754	4474	83	DB4	681	95
34	SEG38	2612	4474	84	DB5	826	95
35	SEG37	2471	4474	85	DB6	974	95
36	SEG36	2330	4474	86	Db7	1117	95
37	SEG35	2188	4474	87	V_{DD}	1257	95
38	SEG34	2047	4474	88	$\overline{RES}$	1397	95
39	SEG33	1905	4474	89	FR	1537	95
40	SEG32	1764	4474	90	V5	1679	95
41	SEG31	1623	4474	91	V3	1820	95
42	SEG30	1481	4474	92	V2	1962	95
43	SEG29	1340	4474	93	SEG79	2097	95
44	SEG28	1198	4474	94	SEG78	2231	95
45	SEG27	1057	4474	95	SEG77	2365	95
46	SEG26	916	4474	96	SEG76	2500	95
47	SEG25	774	4474	97	SEG75	2634	95
48	SEG24	633	4474	98	SEG74	2769	95
49	SEG23	491	4474	99	SEG73	2903	95
50	SEG22	350	4474	100	SEG72	3037	95