LGDP4532

720-Channel, 262,144-Color One-Chip Driver with RAM, Power Supply and Gate Circuits for Amorphous TFT LCD Panels

Rev 0.12
2007-4-19

Description

The LGDP4532 is a one-chip liquid crystal controller driver LSI, comprising RAM of 240 RGB x 320 dots at maximum, a source driver, a gate driver and a power supply circuit. For effective data transfer, the LGDP4532 supports high-speed 8-/9-/16-/18-bit bus interfaces as a system interface to microcomputer and high-speed RAM write mode.
As a moving picture interface, the LGDP4532 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0).
Also, the LGDP4532 incorporates step-up circuits and voltage follower circuits to generate TFT liquid crystal panel drive voltages.
The LGDP4532's power management functions such as 8-color display and deep standby and so on make this LSI an ideal driver for the medium or small sized portable products with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- A one-chip controller driver incorporating a gate circuit and a power supply circuit for 240RGB x320 dots graphics display on an amorphous TFT panel in 262k colors
- System interface
  - High-speed interfaces via 8-, 9-, 16-, 18-bit parallel ports
  - Serial interface
- Interface for moving picture display
  - 6-, 16-, 18-bit bus RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  - VSYNC interface (System interface + VSYNC)
  - FMARK interface (System interface + FMARK)
- Window address function to specify a rectangular area on the internal RAM to write data
- Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
  - Resizing function (x 1/2, x 1/4)
- Abundant color display and drawing functions
  - Programmable γ -correction function for 262k-color display
  - RGB independent control
  - Partial display function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
  - Standby, Deep standby, sleep function
  - 8-color display function
  - Input power supply voltages: Vcc = 2.5V ~ 3.3 V (logic regulator power supply)
IOVcc = 1.65V ~ 3.3 V (interface I/O power supply)
Vci = 2.5V ~ 3.3 V (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/Vcom power supply: DDVDH-GND = 4.5V ~ 6.0 V
  - Gate drive power supply: VGH-GND = 10.0V ~ 15.0 V
VGL-GND = -4.5V ~ -12.5V
VGH-VGL ≤ 25V
- Liquid crystal power supply startup sequence
- TFT storage capacitance: Cst only (common Vcom formula)
- 172,800-byte internal RAM
- Internal 720-channel source driver and 320-channel gate driver
- Configures a COG module with one chip by arranging gate lines on both sides

Block Diagram

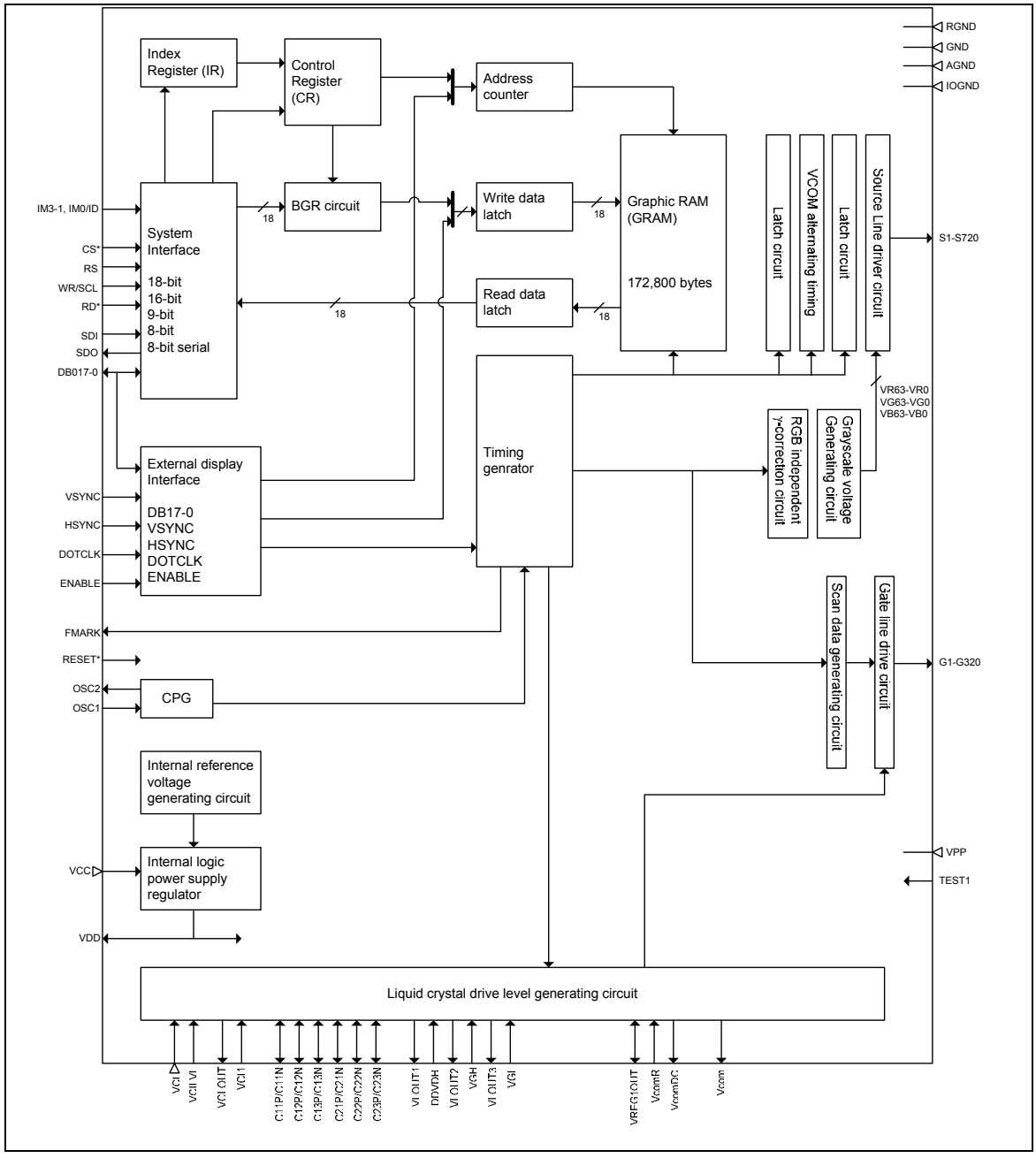


Figure 1

Pin Function

Table 1

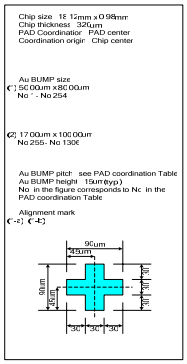
<table>
<tr><th>Signal</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>IM3-1, IM0/ID</td><td>I</td><td>GND/ IOVcc</td><td>Select a mode to interface to an MPU. In SPI mode, the IM0 pin is used to set the ID of device code.
<table>
<tr><th>IM[3:0]</th><th>Interface Mode</th><th>DB Pins</th></tr>
<tr><td>000*</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>0010</td><td>80-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0011</td><td>80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>010*</td><td>Serial peripheral interface (SPI)</td><td>SDI, SDO</td></tr>
<tr><td>011*</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>100*</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1010</td><td>80-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1011</td><td>80-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>11**</td><td>Setting disabled</td><td>-</td></tr>
</table></td></tr>
<tr><td>CS*</td><td>I</td><td>MPU</td><td>A chip select signal. Amplitude: IOVCC-GND.
Low: LGDP4532 is selected and accessible.
High: LGDP4532 is not selected and not accessible.
Fix to the GND level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>A register select signal. Amplitude: IOVCC-GND.
Low: select the index/status register.
High: select a control register.</td></tr>
<tr><td>WR*/SCL</td><td>I</td><td>MPU</td><td>Outputs a write strobe signal in 80-system bus interface mode and enables an operation to write data when the signal is low.
In SPI mode, a synchronizing clock signal is output.</td></tr>
<tr><td>RD*</td><td>I</td><td>MPU</td><td>Outputs a read strobe signal in 80-system bus interface mode and enables an operation to read data when the signal is low. In SPI mode, fix to either IOVcc or GND level.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>A serial data input (SDI) pin in SPI mode. Data are input on the rising edge of the SCL signal. Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>SDO</td><td>I/O</td><td>MPU</td><td>A serial data output (SDO) pin in SPI mode. Data are output on the falling edge of the SCL signal. Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>DB0 ~ DB17</td><td>I/O</td><td>MPU</td><td>An 18-bit parallel bidirectional data bus. Unused pins must be fixed either IOVcc or GND level.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU</td><td>A data enable signal in RGB interface mode.
Low: Select (accessible)
High: Not select (inaccessible)
The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>A frame synchronizing signal.
When VSPL = “0”, it is active low.
When VSPL = “1”, it is active high.
Fix to the IOVcc level when not in use.</td></tr>
</table>

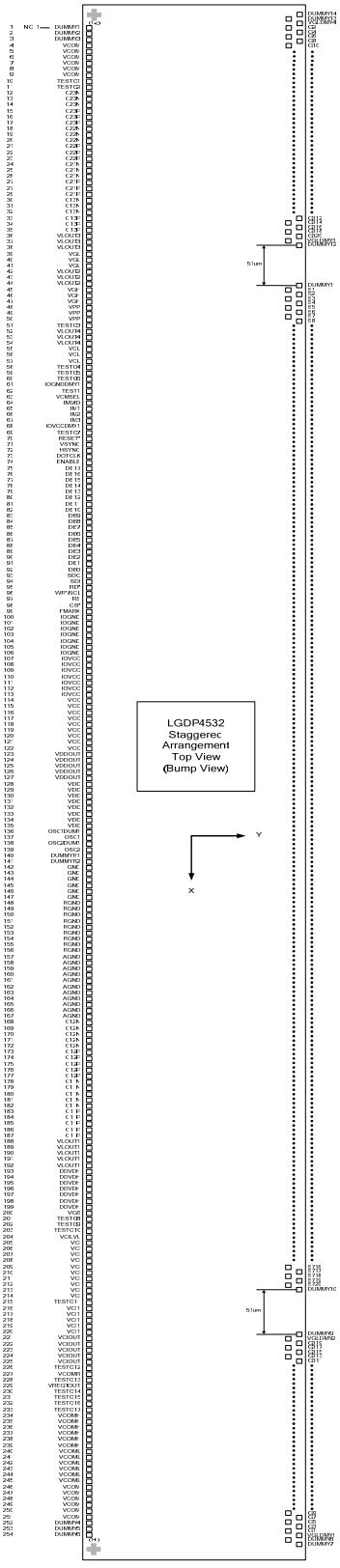
HSYNC	I	MPU	A line synchronizing signal. When HSPL = “0”, it is active low. When HSPL = “1”, it is active high. Fix to the IOVcc level when not in use.
DOTCLK	I	MPU	A dot clock signal. When DPL = “0”, input data on the rising edge of DOTCLK. When DPL = “1”, input data on the falling edge of DOTCLK. Fix to the IOVcc level when not in use.
RESET*	I	MPU or External RC circuit	A reset pin. Initializes the LGDP4532 with a low input. Be sure to execute a power-on reset after supplying power.
VCMSEL	I	IOVcc or GND	If VCMSEL is set to high, VCOM level control comes from EPROM block. If VCMSEL is set to low, VCOM level control comes from internal registers set by MPU. If the setting by this pin is not to be preferable, it is connected to IOVcc or GND.
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal GRAM.
OSC1 OSC2	I/O	Oscillation Resistor	Connect to an external resistor for R-C oscillation.
VCC	I	Power supply	Power supply to internal logic regulator circuit: Vcc =2.5V ~ 3.3 V, Vcc ≥ IOVcc
GND	-	Power supply	Internal logic GND : GND = 0V
RGND	-	Power supply	Internal RAM GND : RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDD	O	Stabilizing capacitor	Internal logic regulator output to be used as a power supply to internal logic. Connect a stabilizing capacitor.
IOVCC	I	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVcc = 1.65V ~ 3.3V. Vcc ≥ IOVcc. . In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent nosie.
IOGND	-	Power supply	GND for the interface pins : RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	I	Power supply	Power supply to liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
VCIOUT	O	Stabilizing capactor, Vci1	Internal reference voltage generated between Vci and GND. The output level is set by instruction (VC).
VCI1	I/O	VciOUT or Vci	Reference voltage for the step-up circuit 1. Vci1 must be set to a level, which will generate the VLOUT1, VLOUT2 and VLOUT3 levels within the respective setting ranges.
VLOUT1	O	Stabilizing capacitor, DDVDH	Output from the step-up circuit 1, generated from Vci1. The step-up factor for the VLOUT1 level is set by instruction (BT). VLOUT1 = 4.5V ~ 6.0V

DDVDH	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and Vcom drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V
VLOUT2	O	Stabilizing capacitor, VGH	Output from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor for VLOUT2 is set by instruction (BT). VLOUT2 = max 15.0V
VGH	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.
VLOUT3	O	Stabilizing capacitor, VGL	Output from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor for VLOUT2 is set by instruction (BT). VLOUT3 = min –12.5V
VGL	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.
VLOUT4	O	Stabilizing capacitor, VCL	A voltage level of Vci1 x (-1) generated in the step=ip circuit 2. Connect to a stabilizing capacitor when using the VLOUT4 output.
VCL	I	VLOUT4	Power supply for operating VCOML. Vci1 is multiplied by 1 and output by internal step-up circuit 2. VCL = 0 to -3.3(V)
C11P, C11N C12P, C12N	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 1.
C13P, C13N C21P, C21N C22P, C22N C23P, C23N	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.
VREG1OUT	O	Stabilizing capacitor	Output generated from a reference voltage VciLVL by amplifying by the factor, which is set by instruction (VRH). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor when it is in use. VREG1OUT = 3.0V ~ (DDVDH – 0.5)V
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. Output AC voltage with the amplitude VCOMH and VCOML. The alternating cycle is changeable by register setting. Also Vcom output can be started and halted by register setting.
VCOMH	O	Stabilizing capacitor	Output for the high level of VCOM. This output voltage is adjusted by an instruction (VCM) setting. VCOMH = 3.0 to (DDVDH -0.5) (V)
VCOML	O	Stabilizing capacitor	Output for the low level of VCOM. This output voltage is adjusted by an instruction (VDV) setting or fixed to GND by a register (VCOMG) setting. In this case, a capacitor for stabilization is not necessary. VCOML = (VCL +0.5)to 1 (V)
VCOMR	I	Variable resistor or open	If a variable resistor is used to adjust VCOMH, it is attached to this pin. In this case, use an instruction (VCM) setting to stop the internal digital potentiometer circuit of VCOMH, and insert the variable resistor for use in adjustment of VCOM between VREG1OUT
VGS	I	GND	Reference level for grayscale voltage generating circuit.

S1 ~ S720	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal outputs, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S720.
G1 ~ G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level
IOVCCDMY 1	-	-	Use it to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
IOGNDDMY 1	-	-	Use it to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VGLDMY 1-4	-	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave them open.
OSC1DUM 1	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
OSC2DUM 1	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
DUMMYR 1-2	-	-	DUMMYR1 and DUMMYR2 are short-circuited within the chip for COG contact resistance measurement.
DUMMY 1-14	-	-	Dummy pins. Leave them open.
TEST1	I	GND	Test pin. Connect to GND.
TESTO1 - 17	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
VPP	I	Power supply	Power supply pin for EPROM write operation. Connect to GND or open when EPROM is not used.

PAD Arrangement





PAD Coordinate

Pad # .	PAD Name	X	Y
1	DUMMY1	-8855.0	-425.0
2	DUMMY2	-8785.0	-425.0
3	DUMMY3	-8715.0	-425.0
4	VCOM	-8645.0	-425.0
5	VCOM	-8575.0	-425.0
6	VCOM	-8505.0	-425.0
7	VCOM	-8435.0	-425.0
8	VCOM	-8365.0	-425.0
9	VCOM	-8295.0	-425.0
10	TESTO1	-8225.0	-425.0
11	TESTO2	-8155.0	-425.0
12	C23N	-8085.0	-425.0
13	C23N	-8015.0	-425.0
14	C23N	-7945.0	-425.0
15	C23P	-7875.0	-425.0
16	C23P	-7805.0	-425.0
17	C23P	-7735.0	-425.0
18	C22N	-7665.0	-425.0
19	C22N	-7595.0	-425.0
20	C22N	-7525.0	-425.0
21	C22P	-7455.0	-425.0
22	C22P	-7385.0	-425.0
23	C22P	-7315.0	-425.0
24	C21N	-7245.0	-425.0
25	C21N	-7175.0	-425.0
26	C21N	-7105.0	-425.0
27	C21P	-7035.0	-425.0
28	C21P	-6965.0	-425.0
29	C21P	-6895.0	-425.0
30	C13N	-6825.0	-425.0
31	C13N	-6755.0	-425.0
32	C13N	-6685.0	-425.0
33	C13P	-6615.0	-425.0
34	C13P	-6545.0	-425.0
35	C13P	-6475.0	-425.0
36	VLOUT3	-6405.0	-425.0
37	VLOUT3	-6335.0	-425.0
38	VLOUT3	-6265.0	-425.0
39	VGL	-6195.0	-425.0
40	VGL	-6125.0	-425.0
41	VGL	-6055.0	-425.0
42	VLOUT2	-5985.0	-425.0
43	VLOUT2	-5915.0	-425.0
44	VLOUT2	-5845.0	-425.0
45	VGH	-5775.0	-425.0
46	VGH	-5705.0	-425.0
47	VGH	-5635.0	-425.0
48	VPP	-5565.0	-425.0
49	VPP	-5495.0	-425.0
50	VPP	-5425.0	-425.0
51	TESTO3	-5355.0	-425.0
52	VLOUT4	-5285.0	-425.0
53	VLOUT4	-5215.0	-425.0
54	VLOUT4	-5145.0	-425.0
55	VCL	-5075.0	-425.0
56	VCL	-5005.0	-425.0
57	VCL	-4935.0	-425.0
58	TESTO4	-4865.0	-425.0
59	TESTO5	-4795.0	-425.0
60	TESTO6	-4725.0	-425.0
61	IOGNDDMY1	-4655.0	-425.0
62	TEST1	-4585.0	-425.0
63	VCMSEL	-4515.0	-425.0
64	IM0/ID	-4445.0	-425.0
65	IM1	-4375.0	-425.0
66	IM2	-4305.0	-425.0
67	IM3	-4235.0	-425.0
68	IOVCCDMY1	-4165.0	-425.0
69	TESTO7	-4095.0	-425.0
70	RESET*	-4025.0	-425.0
71	VSYNC	-3955.0	-425.0
72	HSYNC	-3885.0	-425.0
73	DOTCLK	-3815.0	-425.0
74	ENABLE	-3745.0	-425.0
75	DB17	-3675.0	-425.0
76	DB16	-3605.0	-425.0
77	DB15	-3535.0	-425.0
78	DB14	-3465.0	-425.0
79	DB13	-3395.0	-425.0
80	DB12	-3325.0	-425.0
81	DB11	-3255.0	-425.0
82	DB10	-3185.0	-425.0
83	DB9	-3115.0	-425.0
84	DB8	-3045.0	-425.0

Pad # .	PAD Name	X	Y
85	DB7	-2975.0	-425.0
86	DB6	-2905.0	-425.0
87	DB5	-2835.0	-425.0
88	DB4	-2765.0	-425.0
89	DB3	-2695.0	-425.0
90	DB2	-2625.0	-425.0
91	DB1	-2555.0	-425.0
92	DB0	-2485.0	-425.0
93	SDO	-2415.0	-425.0
94	SDI	-2345.0	-425.0
95	RD*	-2275.0	-425.0
96	WR*/SCL	-2205.0	-425.0
97	RS	-2135.0	-425.0
98	CS*	-2065.0	-425.0
99	FMARK	-1995.0	-425.0
100	IOGND	-1925.0	-425.0
101	IOGND	-1855.0	-425.0
102	IOGND	-1785.0	-425.0
103	IOGND	-1715.0	-425.0
104	IOGND	-1645.0	-425.0
105	IOGND	-1575.0	-425.0
106	IOGND	-1505.0	-425.0
107	IOVCC	-1435.0	-425.0
108	IOVCC	-1365.0	-425.0
109	IOVCC	-1295.0	-425.0
110	IOVCC	-1225.0	-425.0
111	IOVCC	-1155.0	-425.0
112	IOVCC	-1085.0	-425.0
113	IOVCC	-1015.0	-425.0
114	VCC	-945.0	-425.0
115	VCC	-875.0	-425.0
116	VCC	-805.0	-425.0
117	VCC	-735.0	-425.0
118	VCC	-665.0	-425.0
119	VCC	-595.0	-425.0
120	VCC	-525.0	-425.0
121	VCC	-455.0	-425.0
122	VCC	-385.0	-425.0
123	VDDOUT	-315.0	-425.0
124	VDDOUT	-245.0	-425.0
125	VDDOUT	-175.0	-425.0
126	VDDOUT	-105.0	-425.0
127	VDDOUT	-35.0	-425.0
128	VDD	35.0	-425.0
129	VDD	105.0	-425.0
130	VDD	175.0	-425.0
131	VDD	245.0	-425.0
132	VDD	315.0	-425.0
133	VDD	385.0	-425.0
134	VDD	455.0	-425.0
135	VDD	525.0	-425.0
136	OSC1DUM1	595.0	-425.0
137	OSC1	665.0	-425.0
138	OSC2DUM1	735.0	-425.0
139	OSC2	805.0	-425.0
140	DUMMYR1	875.0	-425.0
141	DUMMYR2	945.0	-425.0
142	GND	1015.0	-425.0
143	GND	1085.0	-425.0
144	GND	1155.0	-425.0
145	GND	1225.0	-425.0
146	GND	1295.0	-425.0
147	GND	1365.0	-425.0
148	RGND	1435.0	-425.0
149	RGND	1505.0	-425.0
150	RGND	1575.0	-425.0
151	RGND	1645.0	-425.0
152	RGND	1715.0	-425.0
153	RGND	1785.0	-425.0
154	RGND	1855.0	-425.0
155	RGND	1925.0	-425.0
156	RGND	1995.0	-425.0
157	AGND	2065.0	-425.0
158	AGND	2135.0	-425.0
159	AGND	2205.0	-425.0
160	AGND	2275.0	-425.0
161	AGND	2345.0	-425.0
162	AGND	2415.0	-425.0
163	AGND	2485.0	-425.0
164	AGND	2555.0	-425.0
165	AGND	2625.0	-425.0
166	AGND	2695.0	-425.0
167	AGND	2765.0	-425.0
168	C12N	2835.0	-425.0

Pad # .	PAD Name	X	Y
169	C12N	2905.0	-425.0
170	C12N	2975.0	-425.0
171	C12N	3045.0	-425.0
172	C12N	3115.0	-425.0
173	C12P	3185.0	-425.0
174	C12P	3255.0	-425.0
175	C12P	3325.0	-425.0
176	C12P	3395.0	-425.0
177	C12P	3465.0	-425.0
178	C11N	3535.0	-425.0
179	C11N	3605.0	-425.0
180	C11N	3675.0	-425.0
181	C11N	3745.0	-425.0
182	C11N	3815.0	-425.0
183	C11P	3885.0	-425.0
184	C11P	3955.0	-425.0
185	C11P	4025.0	-425.0
186	C11P	4095.0	-425.0
187	C11P	4165.0	-425.0
188	VLOUT1	4235.0	-425.0
189	VLOUT1	4305.0	-425.0
190	VLOUT1	4375.0	-425.0
191	VLOUT1	4445.0	-425.0
192	VLOUT1	4515.0	-425.0
193	DDVDH	4585.0	-425.0
194	DDVDH	4655.0	-425.0
195	DDVDH	4725.0	-425.0
196	DDVDH	4795.0	-425.0
197	DDVDH	4865.0	-425.0
198	DDVDH	4935.0	-425.0
199	DDVDH	5005.0	-425.0
200	VGS	5075.0	-425.0
201	TESTO8	5145.0	-425.0
202	TESTO9	5215.0	-425.0
203	TESTO10	5285.0	-425.0
204	VCILVL	5355.0	-425.0
205	VCI	5425.0	-425.0
206	VCI	5495.0	-425.0
207	VCI	5565.0	-425.0
208	VCI	5635.0	-425.0
209	VCI	5705.0	-425.0
210	VCI	5775.0	-425.0
211	VCI	5845.0	-425.0
212	VCI	5915.0	-425.0
213	VCI	5985.0	-425.0
214	VCI	6055.0	-425.0
215	TESTO11	6125.0	-425.0
216	VCI1	6195.0	-425.0
217	VCI1	6265.0	-425.0
218	VCI1	6335.0	-425.0
219	VCI1	6405.0	-425.0
220	VCI1	6475.0	-425.0
221	VCIOUT	6545.0	-425.0
222	VCIOUT	6615.0	-425.0
223	VCIOUT	6685.0	-425.0
224	VCIOUT	6755.0	-425.0
225	VCIOUT	6825.0	-425.0
226	TESTO12	6895.0	-425.0
227	VCOMR	6965.0	-425.0
228	TESTO13	7035.0	-425.0
229	VREG1OUT	7105.0	-425.0
230	TESTO14	7175.0	-425.0
231	TESTO15	7245.0	-425.0
232	TESTO16	7315.0	-425.0
233	TESTO17	7385.0	-425.0
234	VCOMH	7455.0	-425.0
235	VCOMH	7525.0	-425.0
236	VCOMH	7595.0	-425.0
237	VCOMH	7665.0	-425.0
238	VCOMH	7735.0	-425.0
239	VCOMH	7805.0	-425.0
240	VCOML	7875.0	-425.0
241	VCOML	7945.0	-425.0
242	VCOML	8015.0	-425.0
243	VCOML	8085.0	-425.0
244	VCOML	8155.0	-425.0
245	VCOML	8225.0	-425.0
246	VCOM	8295.0	-425.0
247	VCOM	8365.0	-425.0
248	VCOM	8435.0	-425.0
249	VCOM	8505.0	-425.0
250	VCOM	8575.0	-425.0
251	VCOM	8645.0	-425.0
252	DUMMY4	8715.0	-425.0

Pad # .	PAD Name	X	Y
253	DUMMY5	8785.0	-425.0
254	DUMMY6	8855.0	-425.0
255	DUMMY7	8976.0	415.0
256	DUMMY8	8959.0	290.0
257	VGLDMY1	8942.0	415.0
258	G1	8925.0	290.0
259	G3	8908.0	415.0
260	G5	8891.0	290.0
261	G7	8874.0	415.0
262	G9	8857.0	290.0
263	G11	8840.0	415.0
264	G13	8823.0	290.0
265	G15	8806.0	415.0
266	G17	8789.0	290.0
267	G19	8772.0	415.0
268	G21	8755.0	290.0
269	G23	8738.0	415.0
270	G25	8721.0	290.0
271	G27	8704.0	415.0
272	G29	8687.0	290.0
273	G31	8670.0	415.0
274	G33	8653.0	290.0
275	G35	8636.0	415.0
276	G37	8619.0	290.0
277	G39	8602.0	415.0
278	G41	8585.0	290.0
279	G43	8568.0	415.0
280	G45	8551.0	290.0
281	G47	8534.0	415.0
282	G49	8517.0	290.0
283	G51	8500.0	415.0
284	G53	8483.0	290.0
285	G55	8466.0	415.0
286	G57	8449.0	290.0
287	G59	8432.0	415.0
288	G61	8415.0	290.0
289	G63	8398.0	415.0
290	G65	8381.0	290.0
291	G67	8364.0	415.0
292	G69	8347.0	290.0
293	G71	8330.0	415.0
294	G73	8313.0	290.0
295	G75	8296.0	415.0
296	G77	8279.0	290.0
297	G79	8262.0	415.0
298	G81	8245.0	290.0
299	G83	8228.0	415.0
300	G85	8211.0	290.0
301	G87	8194.0	415.0
302	G89	8177.0	290.0
303	G91	8160.0	415.0
304	G93	8143.0	290.0
305	G95	8126.0	415.0
306	G97	8109.0	290.0
307	G99	8092.0	415.0
308	G101	8075.0	290.0
309	G103	8058.0	415.0
310	G105	8041.0	290.0
311	G107	8024.0	415.0
312	G109	8007.0	290.0
313	G111	7990.0	415.0
314	G113	7973.0	290.0
315	G115	7956.0	415.0
316	G117	7939.0	290.0
317	G119	7922.0	415.0
318	G121	7905.0	290.0
319	G123	7888.0	415.0
320	G125	7871.0	290.0
321	G127	7854.0	415.0
322	G129	7837.0	290.0
323	G131	7820.0	415.0
324	G133	7803.0	290.0
325	G135	7786.0	415.0
326	G137	7769.0	290.0
327	G139	7752.0	415.0
328	G141	7735.0	290.0
329	G143	7718.0	415.0
330	G145	7701.0	290.0
331	G147	7684.0	415.0
332	G149	7667.0	290.0
333	G151	7650.0	415.0
334	G153	7633.0	290.0
335	G155	7616.0	415.0
336	G157	7599.0	290.0
337	G159	7582.0	415.0
338	G161	7565.0	290.0
339	G163	7548.0	415.0

Pad # .	PAD Name	X	Y
340	G165	7531.0	290.0
341	G167	7514.0	415.0
342	G169	7497.0	290.0
343	G171	7480.0	415.0
344	G173	7463.0	290.0
345	G175	7446.0	415.0
346	G177	7429.0	290.0
347	G179	7412.0	415.0
348	G181	7395.0	290.0
349	G183	7378.0	415.0
350	G185	7361.0	290.0
351	G187	7344.0	415.0
352	G189	7327.0	290.0
353	G191	7310.0	415.0
354	G193	7293.0	290.0
355	G195	7276.0	415.0
356	G197	7259.0	290.0
357	G199	7242.0	415.0
358	G201	7225.0	290.0
359	G203	7208.0	415.0
360	G205	7191.0	290.0
361	G207	7174.0	415.0
362	G209	7157.0	290.0
363	G211	7140.0	415.0
364	G213	7123.0	290.0
365	G215	7106.0	415.0
366	G217	7089.0	290.0
367	G219	7072.0	415.0
368	G221	7055.0	290.0
369	G223	7038.0	415.0
370	G225	7021.0	290.0
371	G227	7004.0	415.0
372	G229	6987.0	290.0
373	G231	6970.0	415.0
374	G233	6953.0	290.0
375	G235	6936.0	415.0
376	G237	6919.0	290.0
377	G239	6902.0	415.0
378	G241	6885.0	290.0
379	G243	6868.0	415.0
380	G245	6851.0	290.0
381	G247	6834.0	415.0
382	G249	6817.0	290.0
383	G251	6800.0	415.0
384	G253	6783.0	290.0
385	G255	6766.0	415.0
386	G257	6749.0	290.0
387	G259	6732.0	415.0
388	G261	6715.0	290.0
389	G263	6698.0	415.0
390	G265	6681.0	290.0
391	G267	6664.0	415.0
392	G269	6647.0	290.0
393	G271	6630.0	415.0
394	G273	6613.0	290.0
395	G275	6596.0	415.0
396	G277	6579.0	290.0
397	G279	6562.0	415.0
398	G281	6545.0	290.0
399	G283	6528.0	415.0
400	G285	6511.0	290.0
401	G287	6494.0	415.0
402	G289	6477.0	290.0
403	G291	6460.0	415.0
404	G293	6443.0	290.0
405	G295	6426.0	415.0
406	G297	6409.0	290.0
407	G299	6392.0	415.0
408	G301	6375.0	290.0
409	G303	6358.0	415.0
410	G305	6341.0	290.0
411	G307	6324.0	415.0
412	G309	6307.0	290.0
413	G311	6290.0	415.0
414	G313	6273.0	290.0
415	G315	6256.0	415.0
416	G317	6239.0	290.0
417	G319	6222.0	415.0
418	VGLDMY2	6205.0	290.0
419	DUMMY9	6188.0	415.0
420	DUMMY10	6137.0	415.0
421	S720	6120.0	290.0
422	S719	6103.0	415.0
423	S718	6086.0	290.0
424	S717	6069.0	415.0
425	S716	6052.0	290.0
426	S715	6035.0	415.0

Pad # .	PAD Name	X	Y
427	S714	6018.0	290.0
428	S713	6001.0	415.0
429	S712	5984.0	290.0
430	S711	5967.0	415.0
431	S710	5950.0	290.0
432	S709	5933.0	415.0
433	S708	5916.0	290.0
434	S707	5899.0	415.0
435	S706	5882.0	290.0
436	S705	5865.0	415.0
437	S704	5848.0	290.0
438	S703	5831.0	415.0
439	S702	5814.0	290.0
440	S701	5797.0	415.0
441	S700	5780.0	290.0
442	S699	5763.0	415.0
443	S698	5746.0	290.0
444	S697	5729.0	415.0
445	S696	5712.0	290.0
446	S695	5695.0	415.0
447	S694	5678.0	290.0
448	S693	5661.0	415.0
449	S692	5644.0	290.0
450	S691	5627.0	415.0
451	S690	5610.0	290.0
452	S689	5593.0	415.0
453	S688	5576.0	290.0
454	S687	5559.0	415.0
455	S686	5542.0	290.0
456	S685	5525.0	415.0
457	S684	5508.0	290.0
458	S683	5491.0	415.0
459	S682	5474.0	290.0
460	S681	5457.0	415.0
461	S680	5440.0	290.0
462	S679	5423.0	415.0
463	S678	5406.0	290.0
464	S677	5389.0	415.0
465	S676	5372.0	290.0
466	S675	5355.0	415.0
467	S674	5338.0	290.0
468	S673	5321.0	415.0
469	S672	5304.0	290.0
470	S671	5287.0	415.0
471	S670	5270.0	290.0
472	S669	5253.0	415.0
473	S668	5236.0	290.0
474	S667	5219.0	415.0
475	S666	5202.0	290.0
476	S665	5185.0	415.0
477	S664	5168.0	290.0
478	S663	5151.0	415.0
479	S662	5134.0	290.0
480	S661	5117.0	415.0
481	S660	5100.0	290.0
482	S659	5083.0	415.0
483	S658	5066.0	290.0
484	S657	5049.0	415.0
485	S656	5032.0	290.0
486	S655	5015.0	415.0
487	S654	4998.0	290.0
488	S653	4981.0	415.0
489	S652	4964.0	290.0
490	S651	4947.0	415.0
491	S650	4930.0	290.0
492	S649	4913.0	415.0
493	S648	4896.0	290.0
494	S647	4879.0	415.0
495	S646	4862.0	290.0
496	S645	4845.0	415.0
497	S644	4828.0	290.0
498	S643	4811.0	415.0
499	S642	4794.0	290.0
500	S641	4777.0	415.0
501	S640	4760.0	290.0
502	S639	4743.0	415.0
503	S638	4726.0	290.0
504	S637	4709.0	415.0
505	S636	4692.0	290.0
506	S635	4675.0	415.0
507	S634	4658.0	290.0
508	S633	4641.0	415.0
509	S632	4624.0	290.0
510	S631	4607.0	415.0
511	S630	4590.0	290.0
512	S629	4573.0	415.0
513	S628	4556.0	290.0

Pad # .	PAD Name	X	Y
514	S627	4539.0	415.0
515	S626	4522.0	290.0
516	S625	4505.0	415.0
517	S624	4488.0	290.0
518	S623	4471.0	415.0
519	S622	4454.0	290.0
520	S621	4437.0	415.0
521	S620	4420.0	290.0
522	S619	4403.0	415.0
523	S618	4386.0	290.0
524	S617	4369.0	415.0
525	S616	4352.0	290.0
526	S615	4335.0	415.0
527	S614	4318.0	290.0
528	S613	4301.0	415.0
529	S612	4284.0	290.0
530	S611	4267.0	415.0
531	S610	4250.0	290.0
532	S609	4233.0	415.0
533	S608	4216.0	290.0
534	S607	4199.0	415.0
535	S606	4182.0	290.0
536	S605	4165.0	415.0
537	S604	4148.0	290.0
538	S603	4131.0	415.0
539	S602	4114.0	290.0
540	S601	4097.0	415.0
541	S600	4080.0	290.0
542	S599	4063.0	415.0
543	S598	4046.0	290.0
544	S597	4029.0	415.0
545	S596	4012.0	290.0
546	S595	3995.0	415.0
547	S594	3978.0	290.0
548	S593	3961.0	415.0
549	S592	3944.0	290.0
550	S591	3927.0	415.0
551	S590	3910.0	290.0
552	S589	3893.0	415.0
553	S588	3876.0	290.0
554	S587	3859.0	415.0
555	S586	3842.0	290.0
556	S585	3825.0	415.0
557	S584	3808.0	290.0
558	S583	3791.0	415.0
559	S582	3774.0	290.0
560	S581	3757.0	415.0
561	S580	3740.0	290.0
562	S579	3723.0	415.0
563	S578	3706.0	290.0
564	S577	3689.0	415.0
565	S576	3672.0	290.0
566	S575	3655.0	415.0
567	S574	3638.0	290.0
568	S573	3621.0	415.0
569	S572	3604.0	290.0
570	S571	3587.0	415.0
571	S570	3570.0	290.0
572	S569	3553.0	415.0
573	S568	3536.0	290.0
574	S567	3519.0	415.0
575	S566	3502.0	290.0
576	S565	3485.0	415.0
577	S564	3468.0	290.0
578	S563	3451.0	415.0
579	S562	3434.0	290.0
580	S561	3417.0	415.0
581	S560	3400.0	290.0
582	S559	3383.0	415.0
583	S558	3366.0	290.0
584	S557	3349.0	415.0
585	S556	3332.0	290.0
586	S555	3315.0	415.0
587	S554	3298.0	290.0
588	S553	3281.0	415.0
589	S552	3264.0	290.0
590	S551	3247.0	415.0
591	S550	3230.0	290.0
592	S549	3213.0	415.0
593	S548	3196.0	290.0
594	S547	3179.0	415.0
595	S546	3162.0	290.0
596	S545	3145.0	415.0
597	S544	3128.0	290.0
598	S543	3111.0	415.0
599	S542	3094.0	290.0
600	S541	3077.0	415.0

Pad # .	PAD Name	X	Y
601	S540	3060.0	290.0
602	S539	3043.0	415.0
603	S538	3026.0	290.0
604	S537	3009.0	415.0
605	S536	2992.0	290.0
606	S535	2975.0	415.0
607	S534	2958.0	290.0
608	S533	2941.0	415.0
609	S532	2924.0	290.0
610	S531	2907.0	415.0
611	S530	2890.0	290.0
612	S529	2873.0	415.0
613	S528	2856.0	290.0
614	S527	2839.0	415.0
615	S526	2822.0	290.0
616	S525	2805.0	415.0
617	S524	2788.0	290.0
618	S523	2771.0	415.0
619	S522	2754.0	290.0
620	S521	2737.0	415.0
621	S520	2720.0	290.0
622	S519	2703.0	415.0
623	S518	2686.0	290.0
624	S517	2669.0	415.0
625	S516	2652.0	290.0
626	S515	2635.0	415.0
627	S514	2618.0	290.0
628	S513	2601.0	415.0
629	S512	2584.0	290.0
630	S511	2567.0	415.0
631	S510	2550.0	290.0
632	S509	2533.0	415.0
633	S508	2516.0	290.0
634	S507	2499.0	415.0
635	S506	2482.0	290.0
636	S505	2465.0	415.0
637	S504	2448.0	290.0
638	S503	2431.0	415.0
639	S502	2414.0	290.0
640	S501	2397.0	415.0
641	S500	2380.0	290.0
642	S499	2363.0	415.0
643	S498	2346.0	290.0
644	S497	2329.0	415.0
645	S496	2312.0	290.0
646	S495	2295.0	415.0
647	S494	2278.0	290.0
648	S493	2261.0	415.0
649	S492	2244.0	290.0
650	S491	2227.0	415.0
651	S490	2210.0	290.0
652	S489	2193.0	415.0
653	S488	2176.0	290.0
654	S487	2159.0	415.0
655	S486	2142.0	290.0
656	S485	2125.0	415.0
657	S484	2108.0	290.0
658	S483	2091.0	415.0
659	S482	2074.0	290.0
660	S481	2057.0	415.0
661	S480	2040.0	290.0
662	S479	2023.0	415.0
663	S478	2006.0	290.0
664	S477	1989.0	415.0
665	S476	1972.0	290.0
666	S475	1955.0	415.0
667	S474	1938.0	290.0
668	S473	1921.0	415.0
669	S472	1904.0	290.0
670	S471	1887.0	415.0
671	S470	1870.0	290.0
672	S469	1853.0	415.0
673	S468	1836.0	290.0
674	S467	1819.0	415.0
675	S466	1802.0	290.0
676	S465	1785.0	415.0
677	S464	1768.0	290.0
678	S463	1751.0	415.0
679	S462	1734.0	290.0
680	S461	1717.0	415.0
681	S460	1700.0	290.0
682	S459	1683.0	415.0
683	S458	1666.0	290.0
684	S457	1649.0	415.0
685	S456	1632.0	290.0
686	S455	1615.0	415.0
687	S454	1598.0	290.0

Pad # .	PAD Name	X	Y
688	S453	1581.0	415.0
689	S452	1564.0	290.0
690	S451	1547.0	415.0
691	S450	1530.0	290.0
692	S449	1513.0	415.0
693	S448	1496.0	290.0
694	S447	1479.0	415.0
695	S446	1462.0	290.0
696	S445	1445.0	415.0
697	S444	1428.0	290.0
698	S443	1411.0	415.0
699	S442	1394.0	290.0
700	S441	1377.0	415.0
701	S440	1360.0	290.0
702	S439	1343.0	415.0
703	S438	1326.0	290.0
704	S437	1309.0	415.0
705	S436	1292.0	290.0
706	S435	1275.0	415.0
707	S434	1258.0	290.0
708	S433	1241.0	415.0
709	S432	1224.0	290.0
710	S431	1207.0	415.0
711	S430	1190.0	290.0
712	S429	1173.0	415.0
713	S428	1156.0	290.0
714	S427	1139.0	415.0
715	S426	1122.0	290.0
716	S425	1105.0	415.0
717	S424	1088.0	290.0
718	S423	1071.0	415.0
719	S422	1054.0	290.0
720	S421	1037.0	415.0
721	S420	1020.0	290.0
722	S419	1003.0	415.0
723	S418	986.0	290.0
724	S417	969.0	415.0
725	S416	952.0	290.0
726	S415	935.0	415.0
727	S414	918.0	290.0
728	S413	901.0	415.0
729	S412	884.0	290.0
730	S411	867.0	415.0
731	S410	850.0	290.0
732	S409	833.0	415.0
733	S408	816.0	290.0
734	S407	799.0	415.0
735	S406	782.0	290.0
736	S405	765.0	415.0
737	S404	748.0	290.0
738	S403	731.0	415.0
739	S402	714.0	290.0
740	S401	697.0	415.0
741	S400	680.0	290.0
742	S399	663.0	415.0
743	S398	646.0	290.0
744	S397	629.0	415.0
745	S396	612.0	290.0
746	S395	595.0	415.0
747	S394	578.0	290.0
748	S393	561.0	415.0
749	S392	544.0	290.0
750	S391	527.0	415.0
751	S390	510.0	290.0
752	S389	493.0	415.0
753	S388	476.0	290.0
754	S387	459.0	415.0
755	S386	442.0	290.0
756	S385	425.0	415.0
757	S384	408.0	290.0
758	S383	391.0	415.0
759	S382	374.0	290.0
760	S381	357.0	415.0
761	S380	340.0	290.0
762	S379	323.0	415.0
763	S378	306.0	290.0
764	S377	289.0	415.0
765	S376	272.0	290.0
766	S375	255.0	415.0
767	S374	238.0	290.0
768	S373	221.0	415.0
769	S372	204.0	290.0
770	S371	187.0	415.0
771	S370	170.0	290.0
772	S369	153.0	415.0
773	S368	136.0	290.0
774	S367	119.0	415.0

Pad # .	PAD Name	X	Y
775	S366	102.0	290.0
776	S365	85.0	415.0
777	S364	68.0	290.0
778	S363	51.0	415.0
779	S362	34.0	290.0
780	S361	17.0	415.0
781	S360	-17.0	415.0
782	S359	-34.0	290.0
783	S358	-51.0	415.0
784	S357	-68.0	290.0
785	S356	-85.0	415.0
786	S355	-102.0	290.0
787	S354	-119.0	415.0
788	S353	-136.0	290.0
789	S352	-153.0	415.0
790	S351	-170.0	290.0
791	S350	-187.0	415.0
792	S349	-204.0	290.0
793	S348	-221.0	415.0
794	S347	-238.0	290.0
795	S346	-255.0	415.0
796	S345	-272.0	290.0
797	S344	-289.0	415.0
798	S343	-306.0	290.0
799	S342	-323.0	415.0
800	S341	-340.0	290.0
801	S340	-357.0	415.0
802	S339	-374.0	290.0
803	S338	-391.0	415.0
804	S337	-408.0	290.0
805	S336	-425.0	415.0
806	S335	-442.0	290.0
807	S334	-459.0	415.0
808	S333	-476.0	290.0
809	S332	-493.0	415.0
810	S331	-510.0	290.0
811	S330	-527.0	415.0
812	S329	-544.0	290.0
813	S328	-561.0	415.0
814	S327	-578.0	290.0
815	S326	-595.0	415.0
816	S325	-612.0	290.0
817	S324	-629.0	415.0
818	S323	-646.0	290.0
819	S322	-663.0	415.0
820	S321	-680.0	290.0
821	S320	-697.0	415.0
822	S319	-714.0	290.0
823	S318	-731.0	415.0
824	S317	-748.0	290.0
825	S316	-765.0	415.0
826	S315	-782.0	290.0
827	S314	-799.0	415.0
828	S313	-816.0	290.0
829	S312	-833.0	415.0
830	S311	-850.0	290.0
831	S310	-867.0	415.0
832	S309	-884.0	290.0
833	S308	-901.0	415.0
834	S307	-918.0	290.0
835	S306	-935.0	415.0
836	S305	-952.0	290.0
837	S304	-969.0	415.0
838	S303	-986.0	290.0
839	S302	-1003.0	415.0
840	S301	-1020.0	290.0
841	S300	-1037.0	415.0
842	S299	-1054.0	290.0
843	S298	-1071.0	415.0
844	S297	-1088.0	290.0
845	S296	-1105.0	415.0
846	S295	-1122.0	290.0
847	S294	-1139.0	415.0
848	S293	-1156.0	290.0
849	S292	-1173.0	415.0
850	S291	-1190.0	290.0
851	S290	-1207.0	415.0
852	S289	-1224.0	290.0
853	S288	-1241.0	415.0
854	S287	-1258.0	290.0
855	S286	-1275.0	415.0
856	S285	-1292.0	290.0
857	S284	-1309.0	415.0
858	S283	-1326.0	290.0
859	S282	-1343.0	415.0
860	S281	-1360.0	290.0
861	S280	-1377.0	415.0

Pad # .	PAD Name	X	Y
862	S279	-1394.0	290.0
863	S278	-1411.0	415.0
864	S277	-1428.0	290.0
865	S276	-1445.0	415.0
866	S275	-1462.0	290.0
867	S274	-1479.0	415.0
868	S273	-1496.0	290.0
869	S272	-1513.0	415.0
870	S271	-1530.0	290.0
871	S270	-1547.0	415.0
872	S269	-1564.0	290.0
873	S268	-1581.0	415.0
874	S267	-1598.0	290.0
875	S266	-1615.0	415.0
876	S265	-1632.0	290.0
877	S264	-1649.0	415.0
878	S263	-1666.0	290.0
879	S262	-1683.0	415.0
880	S261	-1700.0	290.0
881	S260	-1717.0	415.0
882	S259	-1734.0	290.0
883	S258	-1751.0	415.0
884	S257	-1768.0	290.0
885	S256	-1785.0	415.0
886	S255	-1802.0	290.0
887	S254	-1819.0	415.0
888	S253	-1836.0	290.0
889	S252	-1853.0	415.0
890	S251	-1870.0	290.0
891	S250	-1887.0	415.0
892	S249	-1904.0	290.0
893	S248	-1921.0	415.0
894	S247	-1938.0	290.0
895	S246	-1955.0	415.0
896	S245	-1972.0	290.0
897	S244	-1989.0	415.0
898	S243	-2006.0	290.0
899	S242	-2023.0	415.0
900	S241	-2040.0	290.0
901	S240	-2057.0	415.0
902	S239	-2074.0	290.0
903	S238	-2091.0	415.0
904	S237	-2108.0	290.0
905	S236	-2125.0	415.0
906	S235	-2142.0	290.0
907	S234	-2159.0	415.0
908	S233	-2176.0	290.0
909	S232	-2193.0	415.0
910	S231	-2210.0	290.0
911	S230	-2227.0	415.0
912	S229	-2244.0	290.0
913	S228	-2261.0	415.0
914	S227	-2278.0	290.0
915	S226	-2295.0	415.0
916	S225	-2312.0	290.0
917	S224	-2329.0	415.0
918	S223	-2346.0	290.0
919	S222	-2363.0	415.0
920	S221	-2380.0	290.0
921	S220	-2397.0	415.0
922	S219	-2414.0	290.0
923	S218	-2431.0	415.0
924	S217	-2448.0	290.0
925	S216	-2465.0	415.0
926	S215	-2482.0	290.0
927	S214	-2499.0	415.0
928	S213	-2516.0	290.0
929	S212	-2533.0	415.0
930	S211	-2550.0	290.0
931	S210	-2567.0	415.0
932	S209	-2584.0	290.0
933	S208	-2601.0	415.0
934	S207	-2618.0	290.0
935	S206	-2635.0	415.0
936	S205	-2652.0	290.0
937	S204	-2669.0	415.0
938	S203	-2686.0	290.0
939	S202	-2703.0	415.0
940	S201	-2720.0	290.0
941	S200	-2737.0	415.0
942	S199	-2754.0	290.0
943	S198	-2771.0	415.0
944	S197	-2788.0	290.0
945	S196	-2805.0	415.0
946	S195	-2822.0	290.0
947	S194	-2839.0	415.0
948	S193	-2856.0	290.0

Pad # .	PAD Name	X	Y
949	S192	-2873.0	415.0
950	S191	-2890.0	290.0
951	S190	-2907.0	415.0
952	S189	-2924.0	290.0
953	S188	-2941.0	415.0
954	S187	-2958.0	290.0
955	S186	-2975.0	415.0
956	S185	-2992.0	290.0
957	S184	-3009.0	415.0
958	S183	-3026.0	290.0
959	S182	-3043.0	415.0
960	S181	-3060.0	290.0
961	S180	-3077.0	415.0
962	S179	-3094.0	290.0
963	S178	-3111.0	415.0
964	S177	-3128.0	290.0
965	S176	-3145.0	415.0
966	S175	-3162.0	290.0
967	S174	-3179.0	415.0
968	S173	-3196.0	290.0
969	S172	-3213.0	415.0
970	S171	-3230.0	290.0
971	S170	-3247.0	415.0
972	S169	-3264.0	290.0
973	S168	-3281.0	415.0
974	S167	-3298.0	290.0
975	S166	-3315.0	415.0
976	S165	-3332.0	290.0
977	S164	-3349.0	415.0
978	S163	-3366.0	290.0
979	S162	-3383.0	415.0
980	S161	-3400.0	290.0
981	S160	-3417.0	415.0
982	S159	-3434.0	290.0
983	S158	-3451.0	415.0
984	S157	-3468.0	290.0
985	S156	-3485.0	415.0
986	S155	-3502.0	290.0
987	S154	-3519.0	415.0
988	S153	-3536.0	290.0
989	S152	-3553.0	415.0
990	S151	-3570.0	290.0
991	S150	-3587.0	415.0
992	S149	-3604.0	290.0
993	S148	-3621.0	415.0
994	S147	-3638.0	290.0
995	S146	-3655.0	415.0
996	S145	-3672.0	290.0
997	S144	-3689.0	415.0
998	S143	-3706.0	290.0
999	S142	-3723.0	415.0
1000	S141	-3740.0	290.0
1001	S140	-3757.0	415.0
1002	S139	-3774.0	290.0
1003	S138	-3791.0	415.0
1004	S137	-3808.0	290.0
1005	S136	-3825.0	415.0
1006	S135	-3842.0	290.0
1007	S134	-3859.0	415.0
1008	S133	-3876.0	290.0
1009	S132	-3893.0	415.0
1010	S131	-3910.0	290.0
1011	S130	-3927.0	415.0
1012	S129	-3944.0	290.0
1013	S128	-3961.0	415.0
1014	S127	-3978.0	290.0
1015	S126	-3995.0	415.0
1016	S125	-4012.0	290.0
1017	S124	-4029.0	415.0
1018	S123	-4046.0	290.0
1019	S122	-4063.0	415.0
1020	S121	-4080.0	290.0
1021	S120	-4097.0	415.0
1022	S119	-4114.0	290.0
1023	S118	-4131.0	415.0
1024	S117	-4148.0	290.0
1025	S116	-4165.0	415.0
1026	S115	-4182.0	290.0
1027	S114	-4199.0	415.0
1028	S113	-4216.0	290.0
1029	S112	-4233.0	415.0
1030	S111	-4250.0	290.0
1031	S110	-4267.0	415.0
1032	S109	-4284.0	290.0
1033	S108	-4301.0	415.0
1034	S107	-4318.0	290.0
1035	S106	-4335.0	415.0

Pad # .	PAD Name	X	Y
1036	S105	-4352.0	290.0
1037	S104	-4369.0	415.0
1038	S103	-4386.0	290.0
1039	S102	-4403.0	415.0
1040	S101	-4420.0	290.0
1041	S100	-4437.0	415.0
1042	S99	-4454.0	290.0
1043	S98	-4471.0	415.0
1044	S97	-4488.0	290.0
1045	S96	-4505.0	415.0
1046	S95	-4522.0	290.0
1047	S94	-4539.0	415.0
1048	S93	-4556.0	290.0
1049	S92	-4573.0	415.0
1050	S91	-4590.0	290.0
1051	S90	-4607.0	415.0
1052	S89	-4624.0	290.0
1053	S88	-4641.0	415.0
1054	S87	-4658.0	290.0
1055	S86	-4675.0	415.0
1056	S85	-4692.0	290.0
1057	S84	-4709.0	415.0
1058	S83	-4726.0	290.0
1059	S82	-4743.0	415.0
1060	S81	-4760.0	290.0
1061	S80	-4777.0	415.0
1062	S79	-4794.0	290.0
1063	S78	-4811.0	415.0
1064	S77	-4828.0	290.0
1065	S76	-4845.0	415.0
1066	S75	-4862.0	290.0
1067	S74	-4879.0	415.0
1068	S73	-4896.0	290.0
1069	S72	-4913.0	415.0
1070	S71	-4930.0	290.0
1071	S70	-4947.0	415.0
1072	S69	-4964.0	290.0
1073	S68	-4981.0	415.0
1074	S67	-4998.0	290.0
1075	S66	-5015.0	415.0
1076	S65	-5032.0	290.0
1077	S64	-5049.0	415.0
1078	S63	-5066.0	290.0
1079	S62	-5083.0	415.0
1080	S61	-5100.0	290.0
1081	S60	-5117.0	415.0
1082	S59	-5134.0	290.0
1083	S58	-5151.0	415.0
1084	S57	-5168.0	290.0
1085	S56	-5185.0	415.0
1086	S55	-5202.0	290.0
1087	S54	-5219.0	415.0
1088	S53	-5236.0	290.0
1089	S52	-5253.0	415.0
1090	S51	-5270.0	290.0
1091	S50	-5287.0	415.0
1092	S49	-5304.0	290.0
1093	S48	-5321.0	415.0
1094	S47	-5338.0	290.0
1095	S46	-5355.0	415.0
1096	S45	-5372.0	290.0
1097	S44	-5389.0	415.0
1098	S43	-5406.0	290.0
1099	S42	-5423.0	415.0
1100	S41	-5440.0	290.0
1101	S40	-5457.0	415.0
1102	S39	-5474.0	290.0
1103	S38	-5491.0	415.0
1104	S37	-5508.0	290.0
1105	S36	-5525.0	415.0
1106	S35	-5542.0	290.0
1107	S34	-5559.0	415.0
1108	S33	-5576.0	290.0
1109	S32	-5593.0	415.0
1110	S31	-5610.0	290.0
1111	S30	-5627.0	415.0
1112	S29	-5644.0	290.0
1113	S28	-5661.0	415.0
1114	S27	-5678.0	290.0
1115	S26	-5695.0	415.0
1116	S25	-5712.0	290.0
1117	S24	-5729.0	415.0
1118	S23	-5746.0	290.0
1119	S22	-5763.0	415.0
1120	S21	-5780.0	290.0
1121	S20	-5797.0	415.0
1122	S19	-5814.0	290.0

Pad # .	PAD Name	X	Y
1123	S18	-5831.0	415.0
1124	S17	-5848.0	290.0
1125	S16	-5865.0	415.0
1126	S15	-5882.0	290.0
1127	S14	-5899.0	415.0
1128	S13	-5916.0	290.0
1129	S12	-5933.0	415.0
1130	S11	-5950.0	290.0
1131	S10	-5967.0	415.0
1132	S9	-5984.0	290.0
1133	S8	-6001.0	415.0
1134	S7	-6018.0	290.0
1135	S6	-6035.0	415.0
1136	S5	-6052.0	290.0
1137	S4	-6069.0	415.0
1138	S3	-6086.0	290.0
1139	S2	-6103.0	415.0
1140	S1	-6120.0	290.0
1141	DUMMY11	-6137.0	415.0
1142	DUMMY12	-6188.0	415.0
1143	VGLDMY3	-6205.0	290.0
1144	G320	-6222.0	415.0
1145	G318	-6239.0	290.0
1146	G316	-6256.0	415.0
1147	G314	-6273.0	290.0
1148	G312	-6290.0	415.0
1149	G310	-6307.0	290.0
1150	G308	-6324.0	415.0
1151	G306	-6341.0	290.0
1152	G304	-6358.0	415.0
1153	G302	-6375.0	290.0
1154	G300	-6392.0	415.0
1155	G298	-6409.0	290.0
1156	G296	-6426.0	415.0
1157	G294	-6443.0	290.0
1158	G292	-6460.0	415.0
1159	G290	-6477.0	290.0
1160	G288	-6494.0	415.0
1161	G286	-6511.0	290.0
1162	G284	-6528.0	415.0
1163	G282	-6545.0	290.0
1164	G280	-6562.0	415.0
1165	G278	-6579.0	290.0
1166	G276	-6596.0	415.0
1167	G274	-6613.0	290.0
1168	G272	-6630.0	415.0
1169	G270	-6647.0	290.0
1170	G268	-6664.0	415.0
1171	G266	-6681.0	290.0
1172	G264	-6698.0	415.0
1173	G262	-6715.0	290.0
1174	G260	-6732.0	415.0
1175	G258	-6749.0	290.0
1176	G256	-6766.0	415.0
1177	G254	-6783.0	290.0
1178	G252	-6800.0	415.0
1179	G250	-6817.0	290.0
1180	G248	-6834.0	415.0
1181	G246	-6851.0	290.0
1182	G244	-6868.0	415.0
1183	G242	-6885.0	290.0
1184	G240	-6902.0	415.0
1185	G238	-6919.0	290.0
1186	G236	-6936.0	415.0
1187	G234	-6953.0	290.0
1188	G232	-6970.0	415.0
1189	G230	-6987.0	290.0
1190	G228	-7004.0	415.0
1191	G226	-7021.0	290.0
1192	G224	-7038.0	415.0
1193	G222	-7055.0	290.0
1194	G220	-7072.0	415.0
1195	G218	-7089.0	290.0
1196	G216	-7106.0	415.0
1197	G214	-7123.0	290.0
1198	G212	-7140.0	415.0
1199	G210	-7157.0	290.0
1200	G208	-7174.0	415.0
1201	G206	-7191.0	290.0
1202	G204	-7208.0	415.0
1203	G202	-7225.0	290.0
1204	G200	-7242.0	415.0
1205	G198	-7259.0	290.0
1206	G196	-7276.0	415.0
1207	G194	-7293.0	290.0
1208	G192	-7310.0	415.0
1209	G190	-7327.0	290.0

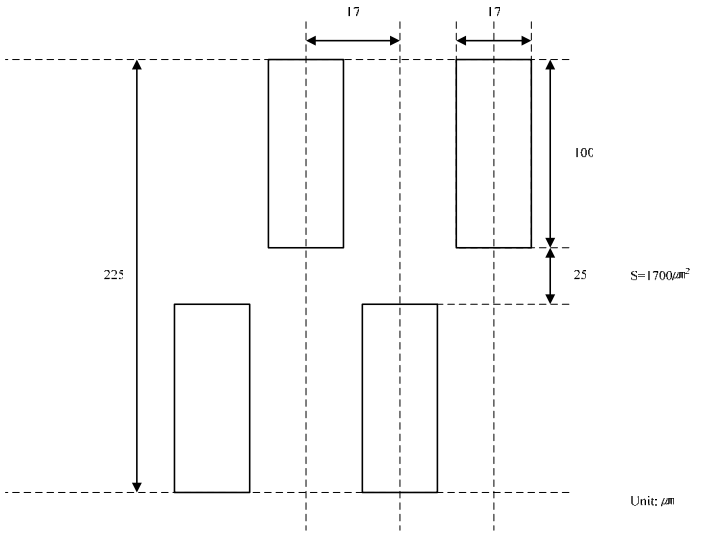
Pad # .	PAD Name	X	Y
1210	G188	-7344.0	415.0
1211	G186	-7361.0	290.0
1212	G184	-7378.0	415.0
1213	G182	-7395.0	290.0
1214	G180	-7412.0	415.0
1215	G178	-7429.0	290.0
1216	G176	-7446.0	415.0
1217	G174	-7463.0	290.0
1218	G172	-7480.0	415.0
1219	G170	-7497.0	290.0
1220	G168	-7514.0	415.0
1221	G166	-7531.0	290.0
1222	G164	-7548.0	415.0
1223	G162	-7565.0	290.0
1224	G160	-7582.0	415.0
1225	G158	-7599.0	290.0
1226	G156	-7616.0	415.0
1227	G154	-7633.0	290.0
1228	G152	-7650.0	415.0
1229	G150	-7667.0	290.0
1230	G148	-7684.0	415.0
1231	G146	-7701.0	290.0
1232	G144	-7718.0	415.0
1233	G142	-7735.0	290.0
1234	G140	-7752.0	415.0
1235	G138	-7769.0	290.0
1236	G136	-7786.0	415.0
1237	G134	-7803.0	290.0
1238	G132	-7820.0	415.0
1239	G130	-7837.0	290.0
1240	G128	-7854.0	415.0
1241	G126	-7871.0	290.0
1242	G124	-7888.0	415.0
1243	G122	-7905.0	290.0
1244	G120	-7922.0	415.0
1245	G118	-7939.0	290.0
1246	G116	-7956.0	415.0
1247	G114	-7973.0	290.0
1248	G112	-7990.0	415.0
1249	G110	-8007.0	290.0
1250	G108	-8024.0	415.0
1251	G106	-8041.0	290.0
1252	G104	-8058.0	415.0
1253	G102	-8075.0	290.0
1254	G100	-8092.0	415.0
1255	G98	-8109.0	290.0
1256	G96	-8126.0	415.0
1257	G94	-8143.0	290.0
1258	G92	-8160.0	415.0
1259	G90	-8177.0	290.0
1260	G88	-8194.0	415.0
1261	G86	-8211.0	290.0
1262	G84	-8228.0	415.0
1263	G82	-8245.0	290.0
1264	G80	-8262.0	415.0
1265	G78	-8279.0	290.0
1266	G76	-8296.0	415.0
1267	G74	-8313.0	290.0
1268	G72	-8330.0	415.0
1269	G70	-8347.0	290.0
1270	G68	-8364.0	415.0
1271	G66	-8381.0	290.0
1272	G64	-8398.0	415.0
1273	G62	-8415.0	290.0
1274	G60	-8432.0	415.0
1275	G58	-8449.0	290.0
1276	G56	-8466.0	415.0
1277	G54	-8483.0	290.0
1278	G52	-8500.0	415.0
1279	G50	-8517.0	290.0
1280	G48	-8534.0	415.0
1281	G46	-8551.0	290.0
1282	G44	-8568.0	415.0
1283	G42	-8585.0	290.0
1284	G40	-8602.0	415.0
1285	G38	-8619.0	290.0
1286	G36	-8636.0	415.0
1287	G34	-8653.0	290.0
1288	G32	-8670.0	415.0
1289	G30	-8687.0	290.0
1290	G28	-8704.0	415.0
1291	G26	-8721.0	290.0
1292	G24	-8738.0	415.0
1293	G22	-8755.0	290.0
1294	G20	-8772.0	415.0
1295	G18	-8789.0	290.0
1296	G16	-8806.0	415.0

Pad # .	PAD Name	X	Y
1297	G14	-8823.0	290.0
1298	G12	-8840.0	415.0
1299	G10	-8857.0	290.0
1300	G8	-8874.0	415.0
1301	G6	-8891.0	290.0
1302	G4	-8908.0	415.0
1303	G2	-8925.0	290.0
1304	VGLDMY4	-8942.0	415.0
1305	DUMMY13	-8959.0	290.0
1306	DUMMY14	-8976.0	415.0

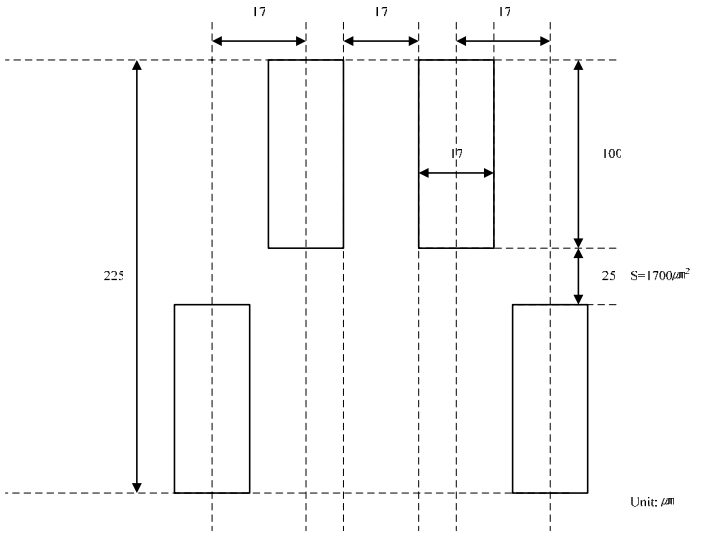
Alignment mark	X	Y
1-a	-8977.0	-407.0
1-b	8977.0	-407.0

Bump Arrangement

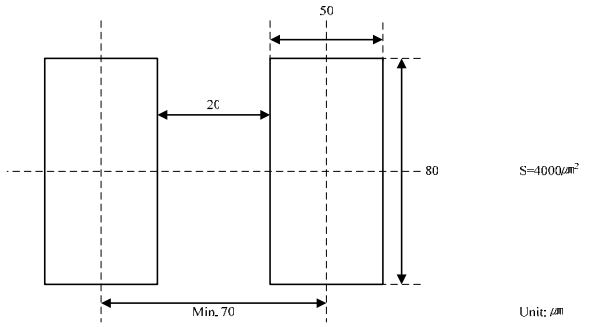
S1 ~ S720
G1 ~ G320
DUMMY7 ~ 14
VGLDMY1 ~ 4
(No. 255 ~ No. 1306)



S360 ~ S361
(No. 780 ~ No. 781)



I/O PINS
(No. 1 ~ No. 254)



Block Function

System Interface

The LGDP4532 supports 2-system high-speed interfaces: 80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and a Serial Peripheral Interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

The LGDP4532 has a 16-bit index register (IR); an 18-bit write-data register (WDR); and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the LGDP4532 read the first data from the internal GRAM. Valid data are read out after the LGDP4532 performs the second read operation.

Instructions are written consecutively as the instruction execution time except starting oscillator takes 0 clock cycle.

Table 2 Register Selection (80-system 8-/9-/16-/18-bit Parallel Interface)

80-system I/F			Function
WR*	RD*	RS	
0	1	0	Write an index to IR
1	0	0	Read an internal status
0	1	1	Write to control registers or the internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 3 Register Selection (Serial Peripheral Interface)

Start Byte (SPI)		Function
R/W	RS	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

External Display Interface

The LGDP4532 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB[17:0]) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section.

The LGDP4532 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 172,800 (240 x 320x 18bit) bytes, using 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Register" section.

Timing Generator

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

The LGDP4532 generates RC oscillation with an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency is changed according to the value of an external resistor. Adjust the oscillation frequency in accordance to the operating voltage or the frame frequency. An operating clock can be input externally. During standby mode, RC oscillation is halted to reduce power consumption. For details, see "Oscillator."

LCD Driver Circuit

The LCD driver circuit of the LGDP4532 consists of a 528-output source driver (S1 ~ S528) and a 240-output gate driver (G1~G240). Display pattern data are latched when the 528th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

Internal logic power supply regulator

The internal logic power supply regulator generates internal logic power supply VDD.

GRAM Address MAP

Table 4 GRAM address and display panel position (SS = "0", BGR = "0")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	…	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G320	"00000"H			"00001"H			"00002"H			"00003"H			…	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			…	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			…	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			…	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			…	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G315	"00500"H			"00501"H			"00502"H			"00503"H			…	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G314	"00600"H			"00601"H			"00602"H			"00603"H			…	"006EC"H			"006ED"H			"006EE"H			"006EF"H		
G8	G313	"00700"H			"00701"H			"00702"H			"00703"H			…	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G312	"00800"H			"00801"H			"00802"H			"00803"H			…	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G311	"00900"H			"00901"H			"00902"H			"00903"H			…	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G310	"00A00"H			"00A01"H			"00A02"H			"00A03"H			…	"00AEC"H			"00AED"H			"00AEE"H			"00AEF"H		
G12	G309	"00B00"H			"00B01"H			"00B02"H			"00B03"H			…	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G308	"00C00"H			"00C01"H			"00C02"H			"00C03"H			…	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G307	"00D00"H			"00D01"H			"00D02"H			"00D03"H			…	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G306	"00E00"H			"00E01"H			"00E02"H			"00E03"H			…	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G305	"00F00"H			"00F01"H			"00F02"H			"00F03"H			…	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G304	"01000"H			"01001"H			"01002"H			"01003"H			…	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G303	"01100"H			"01101"H			"01102"H			"01103"H			…	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G302	"01200"H			"01201"H			"01202"H			"01203"H			…	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G301	"01300"H			"01301"H			"1302"H			"01303"H			…	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
:	:	:			:			:			:			…	:			:			:			:		
:	:	:			:			:			:			…	:			:			:			:		
G313	G8	"13800"H			"13801"H			"13802"H			"13803"H			…	"138EC"H			"138ED"H			"138EE"H			"138EF"H		
G314	G7	"13900"H			"13901"H			"13902"H			"13903"H			…	"139EC"H			"139ED"H			"139EE"H			"139EF"H		
G315	G6	"13A00"H			"13A01"H			"13A02"H			"13A03"H			…	"13AEC"H			"13AED"H			"13AEE"H			"13AEF"H		
G316	G5	"13B00"H			"13B01"H			"13B02"H			"13B03"H			…	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			…	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			…	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			…	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			…	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		

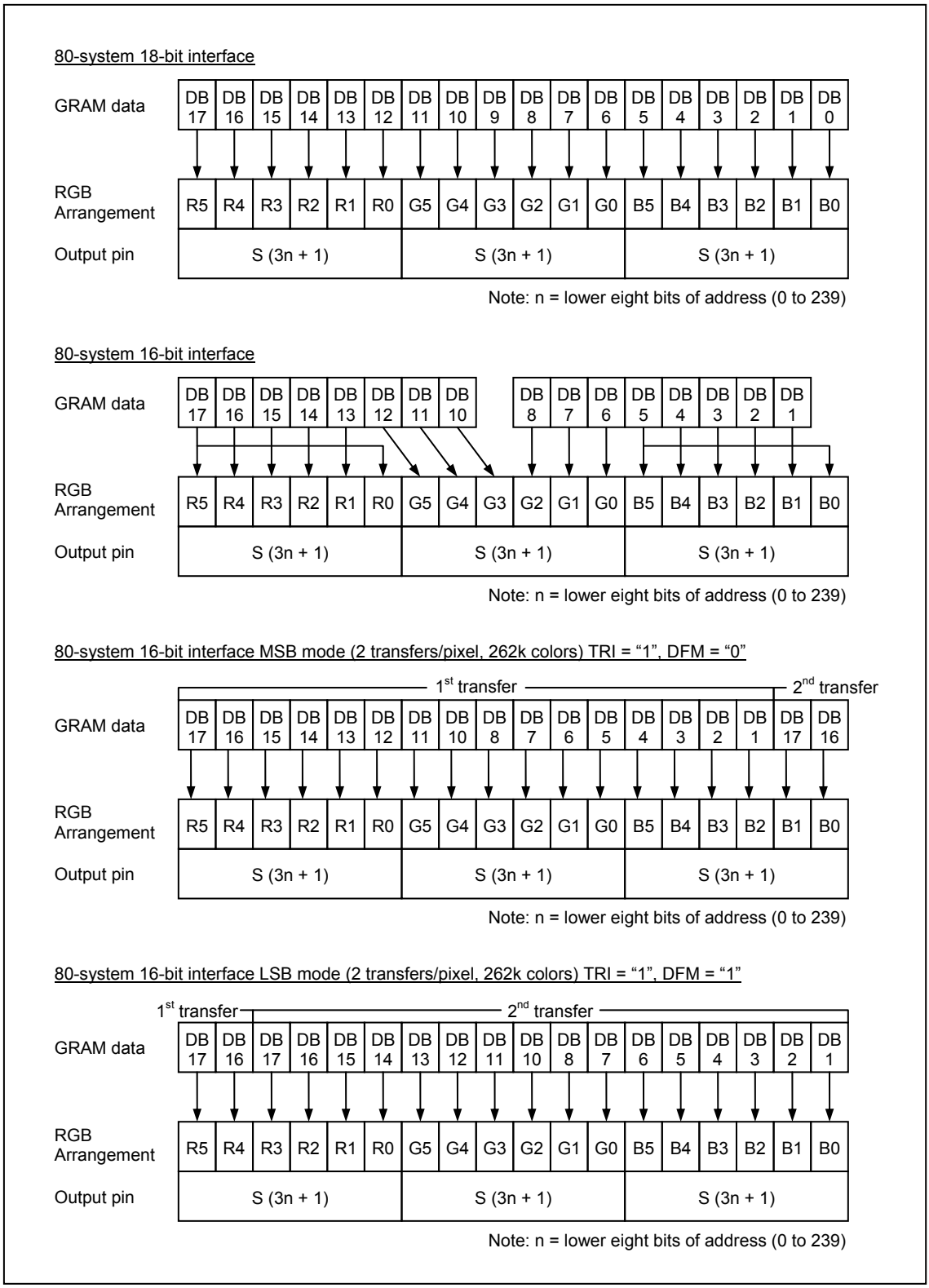


Figure 2 GRAM data and display data: system interface (SS = "0", BGR = "0")

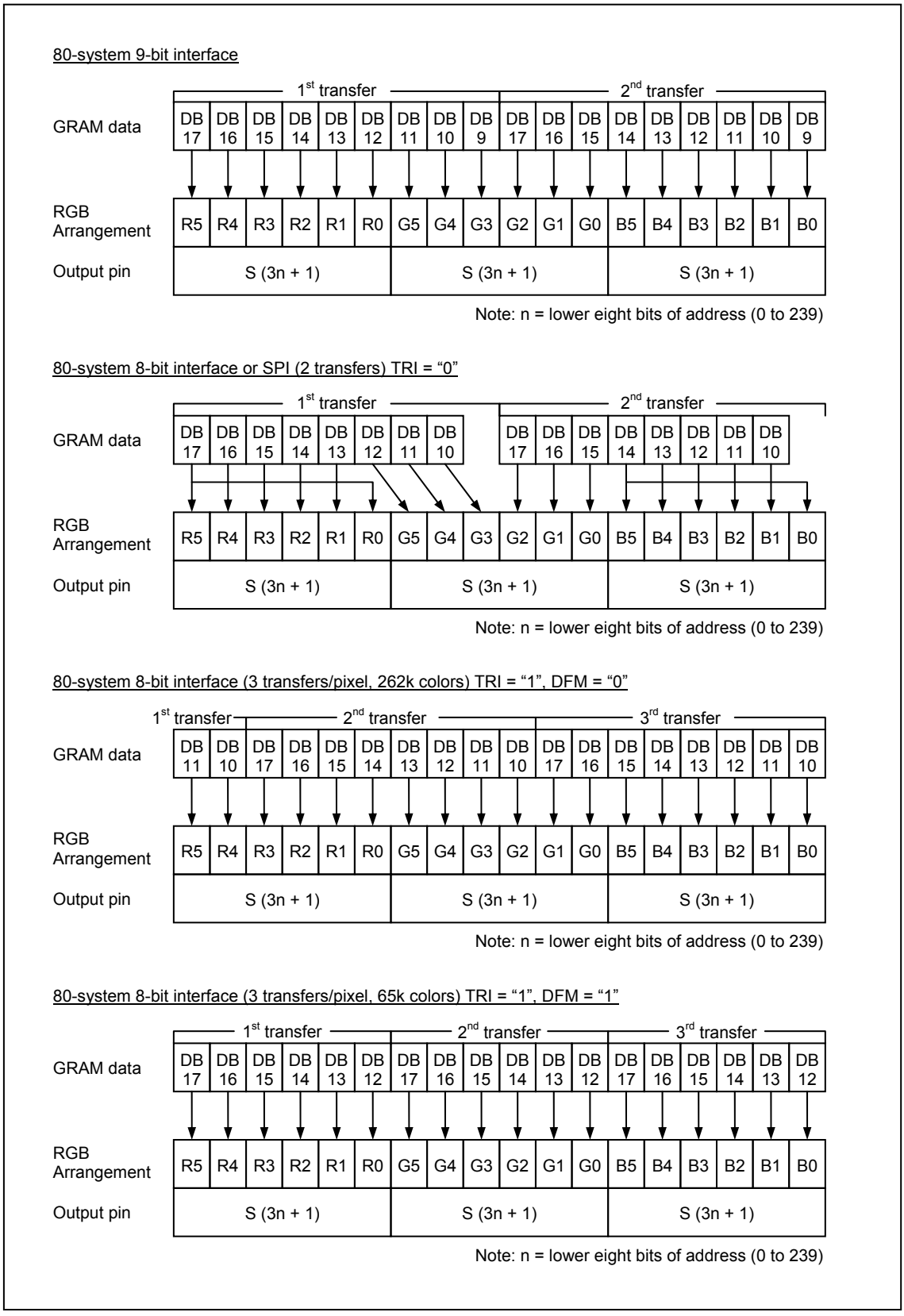


Figure 3 GRAM data and display data: system interface (SS = "0", BGR = "0")

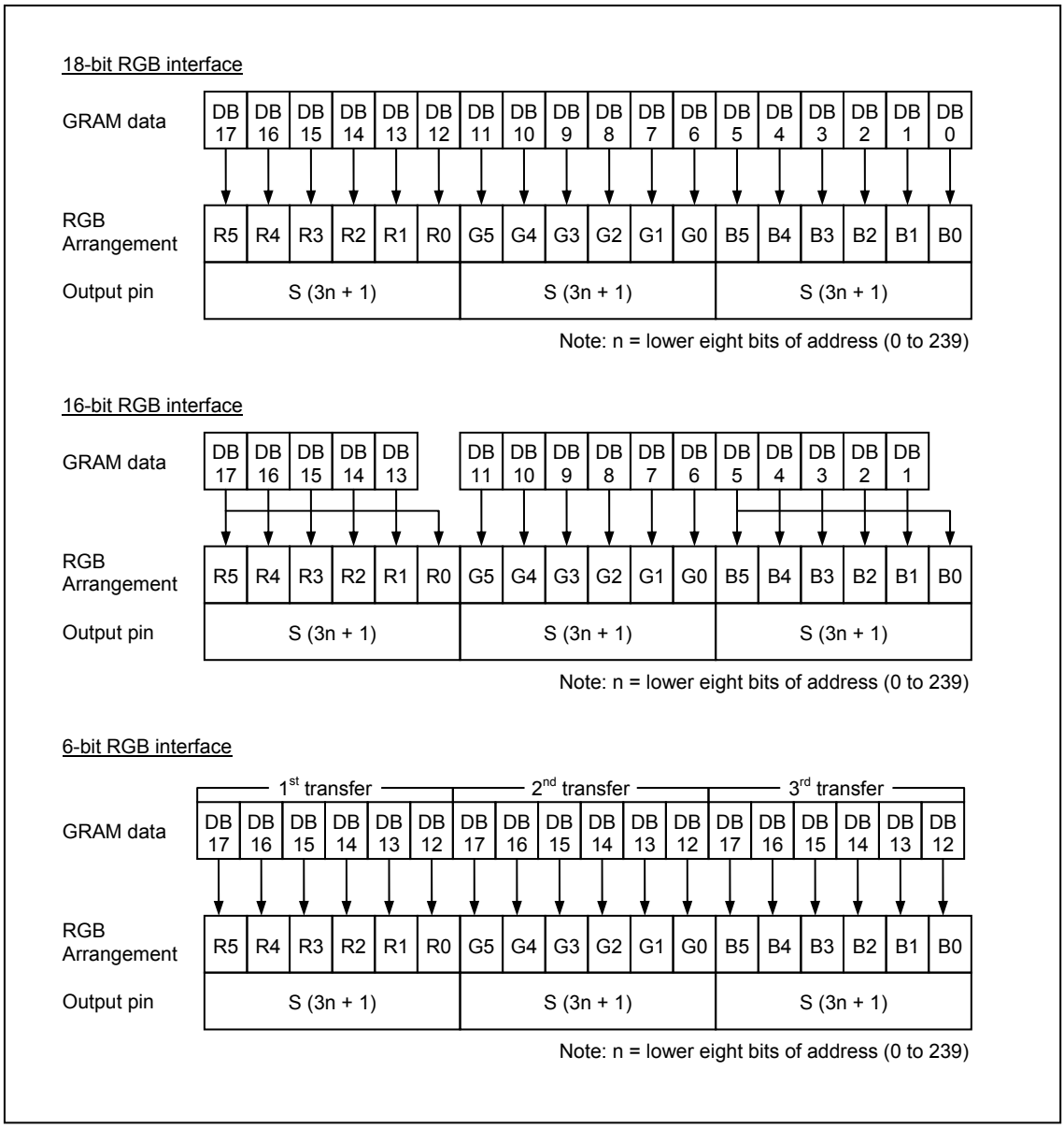


Figure 4 GRAM data and display data: system interface (SS = "0", BGR = "0")

Table 5 GRAM address and display panel position (SS = "1", BGR = "1")

S/G pin		S720	S719	S718	S717	S716	S715	S714	S713	S712	S711	S710	S709	…	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G320	"00000"H			"00001"H			"00002"H			"00003"H			…	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			…	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			…	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			…	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			…	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G315	"00500"H			"00501"H			"00502"H			"00503"H			…	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G314	"00600"H			"00601"H			"00602"H			"00603"H			…	"006EC"H			"006ED"H			"006EE"H			"006EF"H		
G8	G313	"00700"H			"00701"H			"00702"H			"00703"H			…	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G312	"00800"H			"00801"H			"00802"H			"00803"H			…	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G311	"00900"H			"00901"H			"00902"H			"00903"H			…	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G310	"00A00"H			"00A01"H			"00A02"H			"00A03"H			…	"00AEC"H			"00AED"H			"00AEE"H			"00AEF"H		
G12	G309	"00B00"H			"00B01"H			"00B02"H			"00B03"H			…	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G308	"00C00"H			"00C01"H			"00C02"H			"00C03"H			…	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G307	"00D00"H			"00D01"H			"00D02"H			"00D03"H			…	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G306	"00E00"H			"00E01"H			"00E02"H			"00E03"H			…	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G305	"00F00"H			"00F01"H			"00F02"H			"00F03"H			…	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G304	"01000"H			"01001"H			"01002"H			"01003"H			…	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G303	"01100"H			"01101"H			"01102"H			"01103"H			…	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G302	"01200"H			"01201"H			"01202"H			"01203"H			…	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G301	"01300"H			"01301"H			"1302"H			"01303"H			…	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
:	:	:			:			:			:			…	:			:			:			:		
:	:	:			:			:			:			…	:			:			:			:		
G313	G8	"13800"H			"13801"H			"13802"H			"13803"H			…	"138EC"H			"138ED"H			"138EE"H			"138EF"H		
G314	G7	"13900"H			"13901"H			"13902"H			"13903"H			…	"139EC"H			"139ED"H			"139EE"H			"139EF"H		
G315	G6	"13A00"H			"13A01"H			"13A02"H			"13A03"H			…	"13AEC"H			"13AED"H			"13AEE"H			"13AEF"H		
G316	G5	"13B00"H			"13B01"H			"13B02"H			"13B03"H			…	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			…	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			…	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			…	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			…	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		

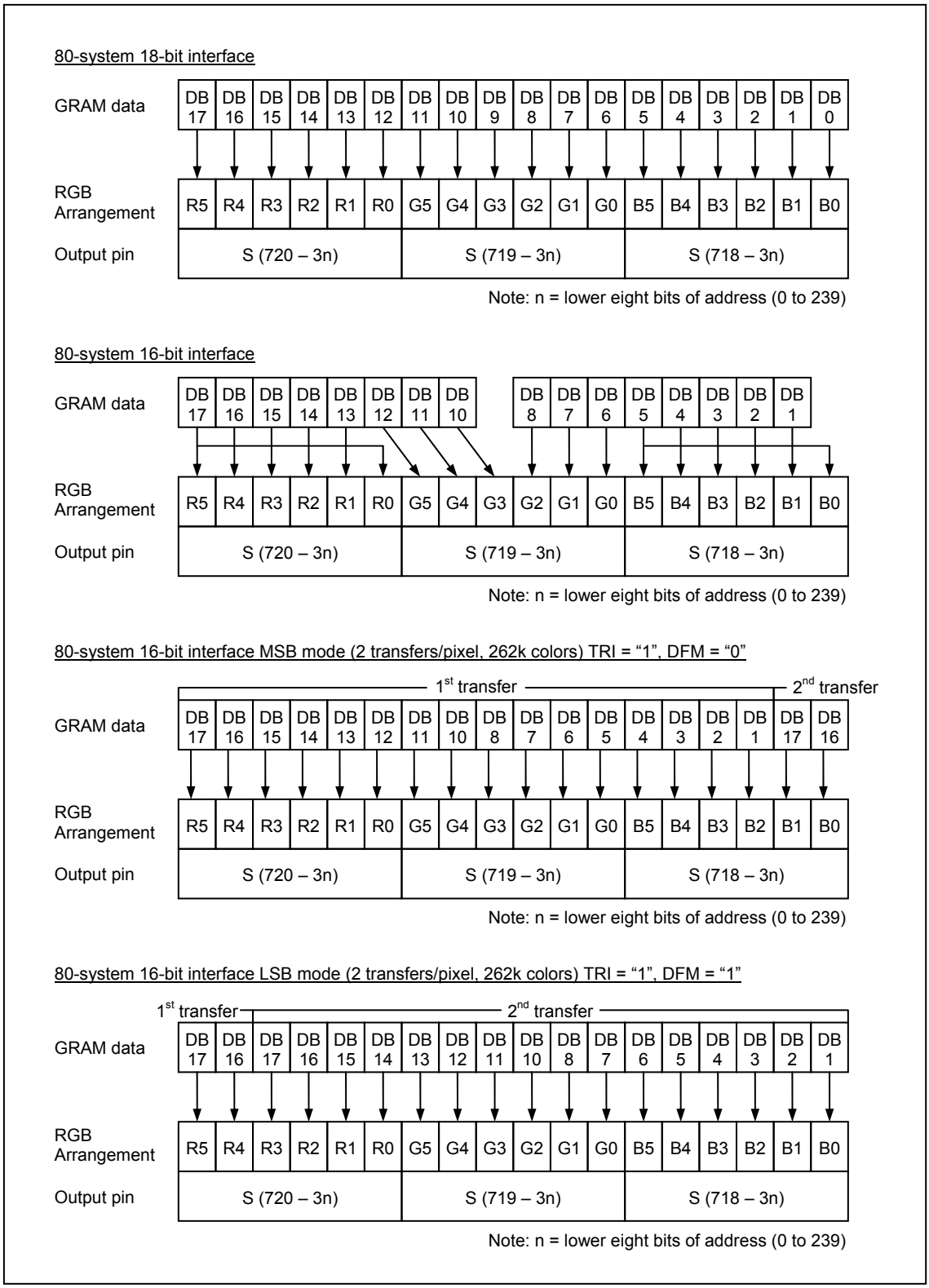


Figure 5 GRAM data and display data: system interface (SS = "1", BGR = "1")

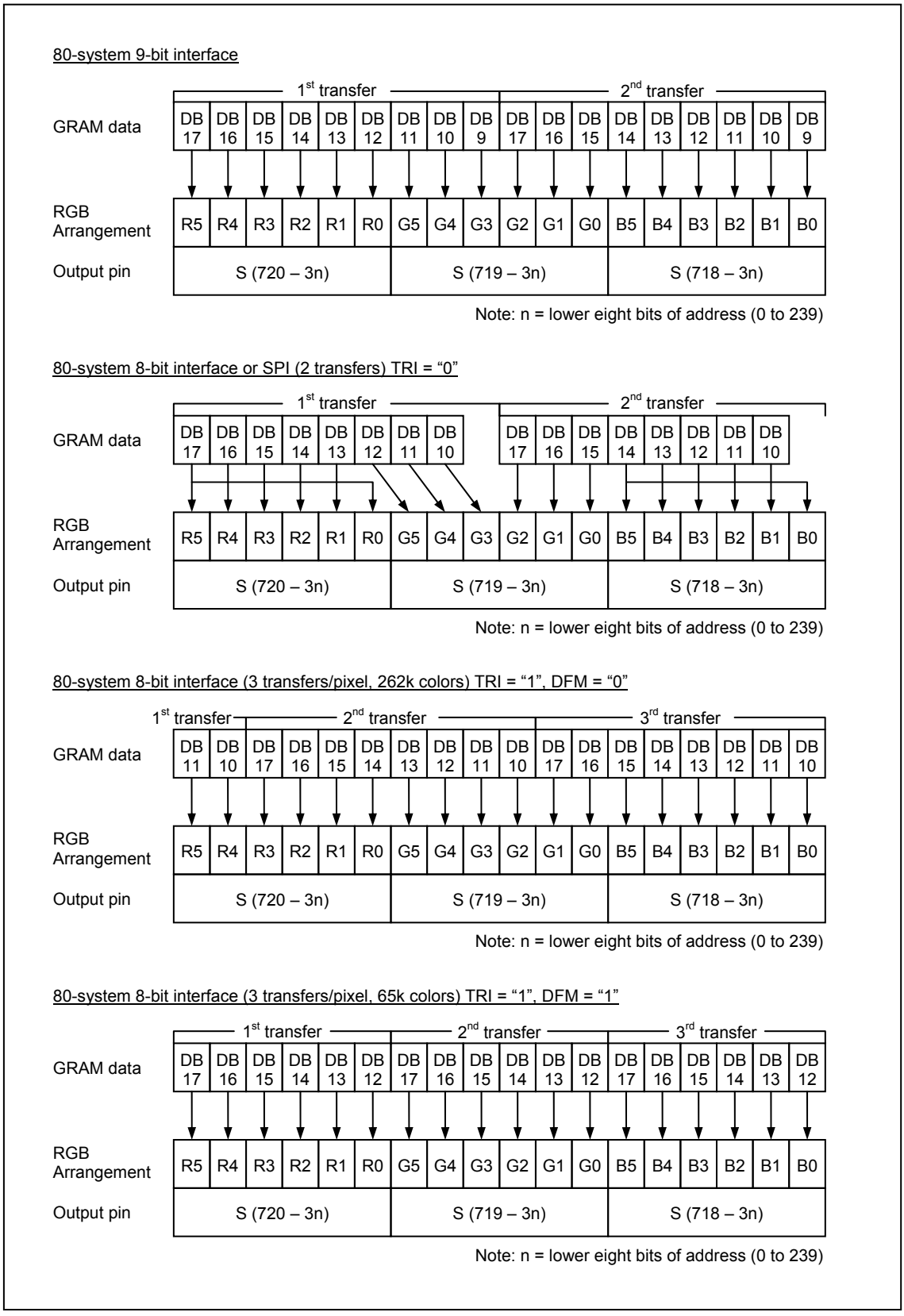


Figure 6 GRAM data and display data: system interface (SS = "1", BGR = "1")

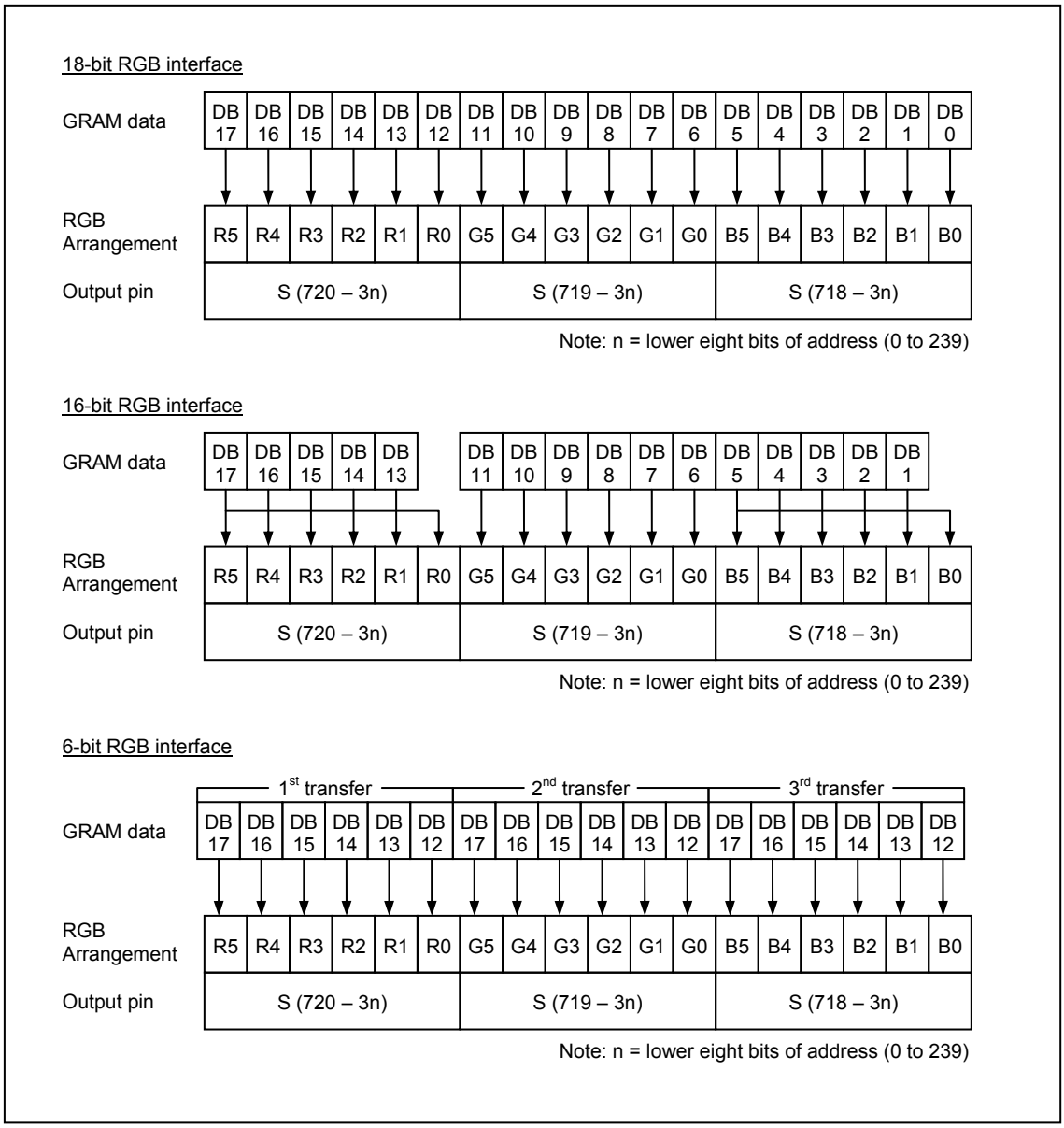


Figure 7 GRAM data and display data: system interface (SS = "1", BGR = "1")

Instructions

Outline

The LGDP4532 adopts 18-bit bus architecture to interface to a high-performance microcomputer. The LGDP4532 starts internal processing after storing control information of externally sent 18-, 16-, 9-, 8-bit data in the instruction register (IR) and the data register (DR). Since internal operations of the LGDP4532 are controlled by the signals sent from the microcomputer, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 to IB0) are called instructions. The LGDP4532 use the 18-bit format internally for operations involving internal GRAM access. The instructions of the LGDP4532 are categorized into the following groups.

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

Normally, the instruction for writing data to the internal GRAM is used the most often. Since the LGDP4532 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there is less load on the program in the microcomputer. Since instructions are executed in 0 cycles, it is possible to write instructions consecutively.

Instruction Data Format

Note that as the following figure shows, the assignment of 16 instruction bits(IB15-0) to the data bus differs in different interface operations. Write instruction according to the data transfer format of the interface in use.

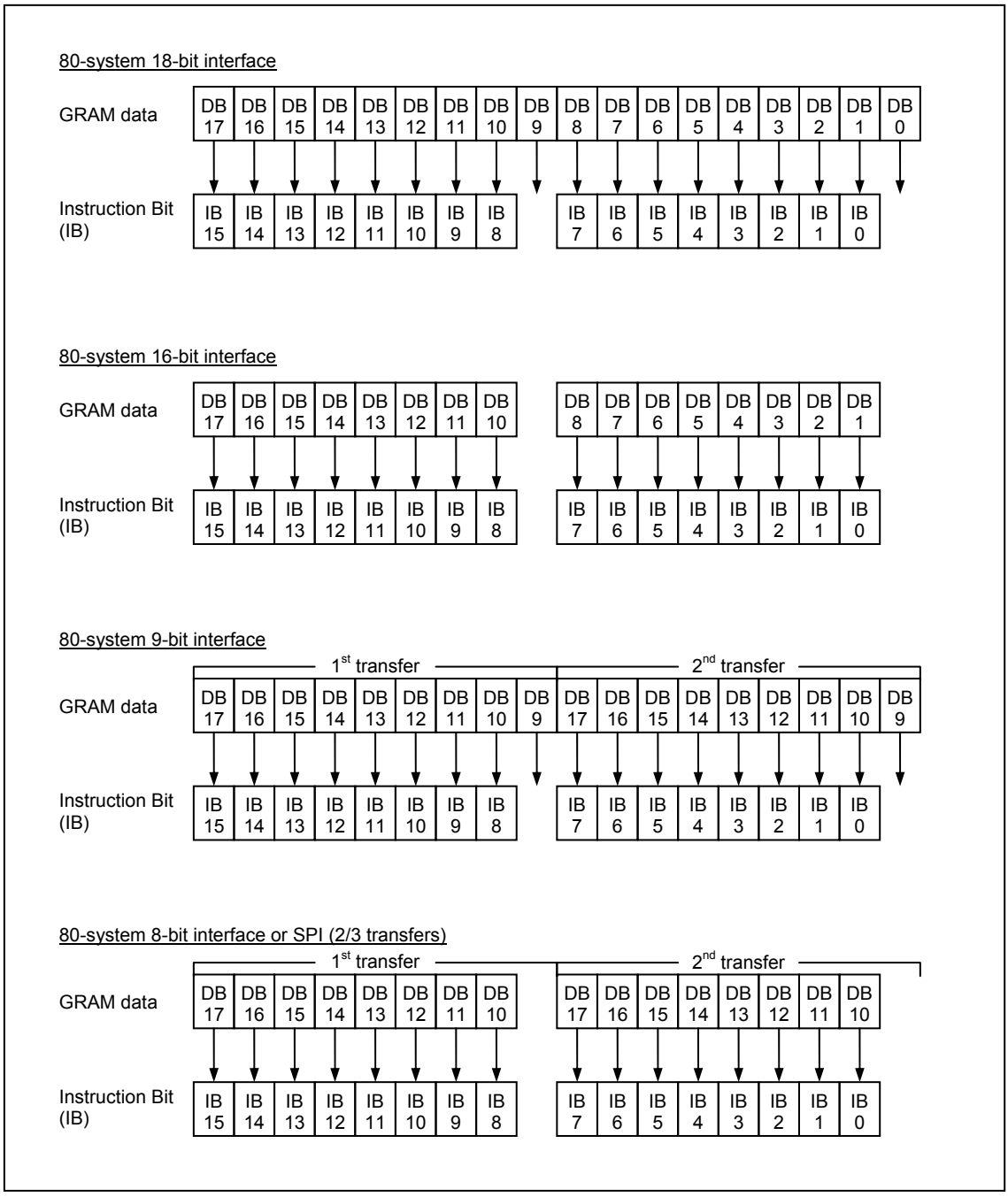


Figure 8 Instruction bits

Instruction Description

The following are detailed explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h - RFFh) of a control register or RAM control to be accessed using binary numbers “0000_0000” to “1111_1111”. An access to the register as well as instruction bits contained in it is disabled unless its index is represented in this register.

Device code read (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	1	0	0	0	1	0	1	0	0	1	1	0	0	1	0

The device code “4532”H is read out when reading out this register forcibly.

Driver output control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS – Selects the shift direction of outputs from the source pins.

If SS = “0”, the source pins output from S1 to S720.
If SS = “1”, the source pins output from S720 to S1.

The combination of SS and BGR bits controls the order of assigning RGB dots to the source driver pins S1 to S720.

If SS = “0” and BGR = “0”, RGB dots are assigned interchangeably from S1 to S720.
If SS = “1” and BGR = “1”, RGB dots are assigned interchangeably from S720 to S1.

When changing SS or BGR bits, RAM data must be rewritten.

SM – Sets gate driver assignment in combination with the GS bit according to the LC module. See “Scan mode setting”.

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	BC0	EOR	0	0	NW[5:0]					

NW[5:0] – Specify n, the number of raster-rows from 1 to 64, where alternations occurs every n+1 raster-rows when C-pattern saveform is generatd(BC0=1).

EOR – When EOR=1, alternation occured by applying EOR(Exclusive OR) operatin to an odd/even frame selecting signal and n-raster-row inversion signal while a C-pattenr waveform is generated(BC0=1).

This instruction is used when liquid crystal alternation drive is not available due t combination of numvers of LCD raster-rows and the value of "x n". For details, see n-raster-row Inversion Alternating Drive.

BC0 – Selects the liquid crystal drive waveform VCOM. See "Line Inversion AC Drive" for details.
BC0 = 0: frame inversion waveform is selected.
BC0 = 1: Line inversion waveform is selected.
In either liquid crystal drive method, the polarity inversion is halted in blank periods (back and front porch periods).

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D[1:0]		AM	0	0	0

The LGDP4532 modifies data sent from a microcomputer before writing them to the internal GRAM in order to write the GRAM data in high speed and reduce software processing load on the microcomputer. See "Graphics Operation Function" for details.

TRI – Selects the RAM data transfer mode in 80-system 8-bit/16-bit bus interface operation.
In 8-bit interface operation,
TRI = 0: 16-bit RAM data is transferred in two transfers.
TRI = 1: 18-bit RAM data is transferred in three transfers.
In 16-bit bus interface operation,
TRI = 0: 16-bit RAM data is transferred in one transfer.
TRI = 1: 18-bit RAM data is transferred in two transfers.
Make sure TRI = 0 when not using either 16-bit or 8-bit interface. Also, set TRI = 0 during read operation.

DFM – Sets the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.

Table 6

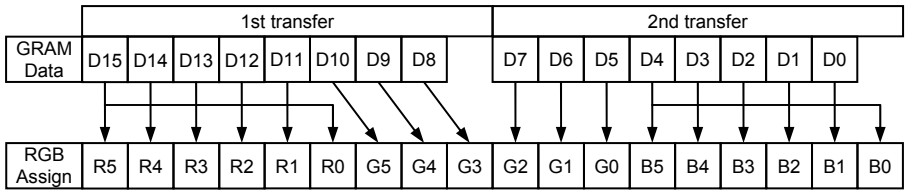
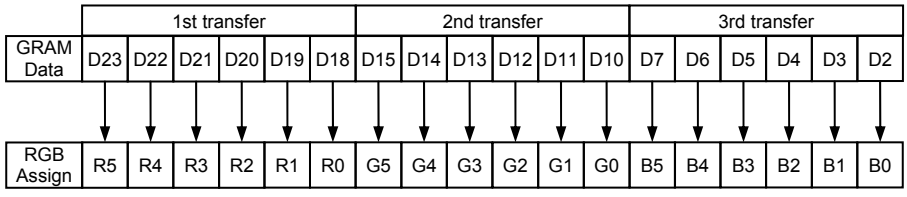
<table>
<tr><th>TRI</th><th>DFM</th><th>RAM write data transfer via serial peripheral interface (SPI)</th></tr>
<tr><td>0</td><td>*</td><td>SPI (2 transfers/pixel) – 65k colors available
 
</td></tr>
<tr><td>1</td><td>0</td><td>SPI (3 transfers/pixel) – 262k colors available
 
</td></tr>
<tr><td>1</td><td>1</td><td>Setting disabled</td></tr>
</table>

Table 7

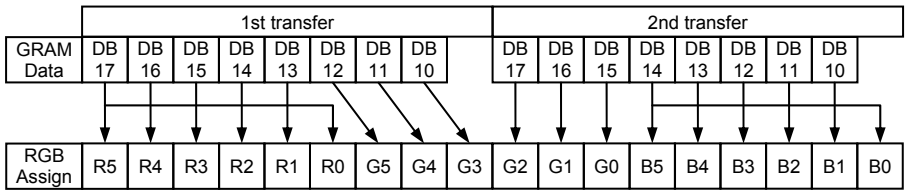
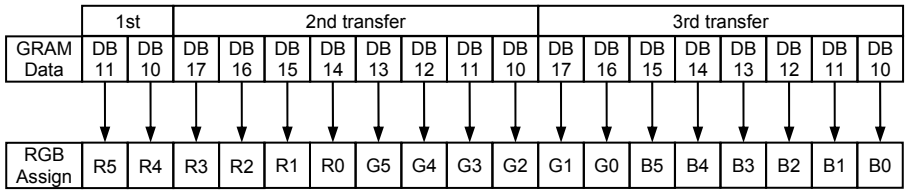
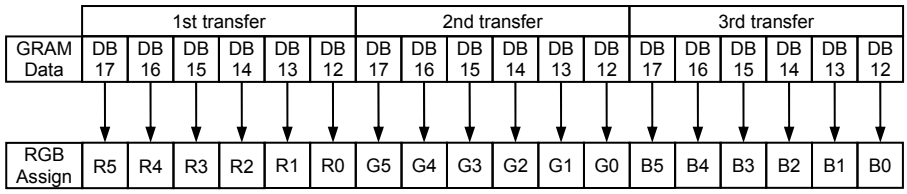
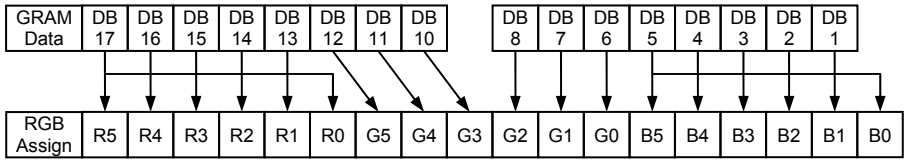
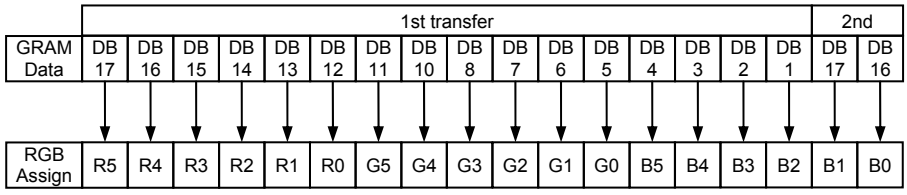
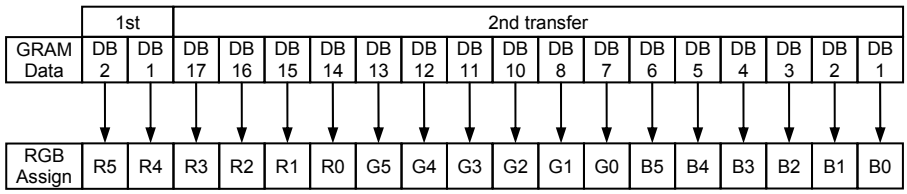
TRI	DFM	RAM write data transfer via 8-bit interface
0	*	80-system 8-bit interface (2 transfers/pixel) – 65k colors 
1	0	80-system 8-bit interface (3 transfers/pixel) – 262k colors 
1	1	80-system 8-bit interface (3 transfers/pixel) – 65k colors 

Table 8

TRI	DFM	RAM write data transfer via 16-bit interface
0	*	80-system 16-bit interface (1 transfers/pixel) – 65k colors 
1	0	80-system 16-bit interface MSB mode(2 transfers/pixel) – 262k colors available 
1	1	80-system 16-bit interface LSB mode(2 transfers/pixel) – 262k colors available 

BGR – Reverses the order of RGB dots to BGR when writing 18-bit pixel data to the internal GRAM. Note that the orders of RGB dots in both WM[17:0] and CP[17:0] bits are automatically changed upon setting BGR = “1”.

ORG – Moves the origin of a window address area in combination with the ID setting. This function is enabled when writing data within the window address area.

I/D[1:0] – The address counter is automatically incremented by 1 as writing data to the internal GRAM when I/D[1:0] = “1”. The address counter is automatically decremented by 1 as writing data to the internal GRAM when I/D[1:0] = “0”. The increment/decrement can be set separately to each upper (AD[15:8]) / lower (AD[7:0]) byte of address. The transition direction of address (vertical/horizontal) when writing data to the internal GRAM is set with the AM bit.

AM – Sets the direction of automatically updating address for writing data to the internal RAM in the address counter (AC). When AM = “0”, the address is updated in horizontal writing direction. When AM = “1”, the address is updated in vertical writing direction. When a window address area is set, data are written only to the GRAM area specified with window address in the writing direction set with I/D[1:0] and AM bits.

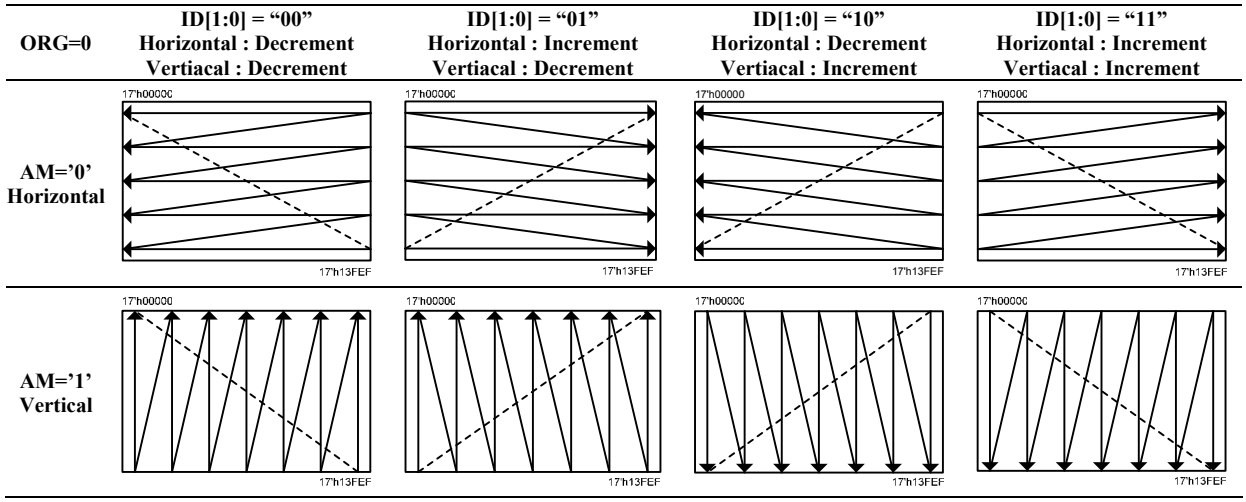


Figure 9 Automatic address update (ORG=0, AM, ID)

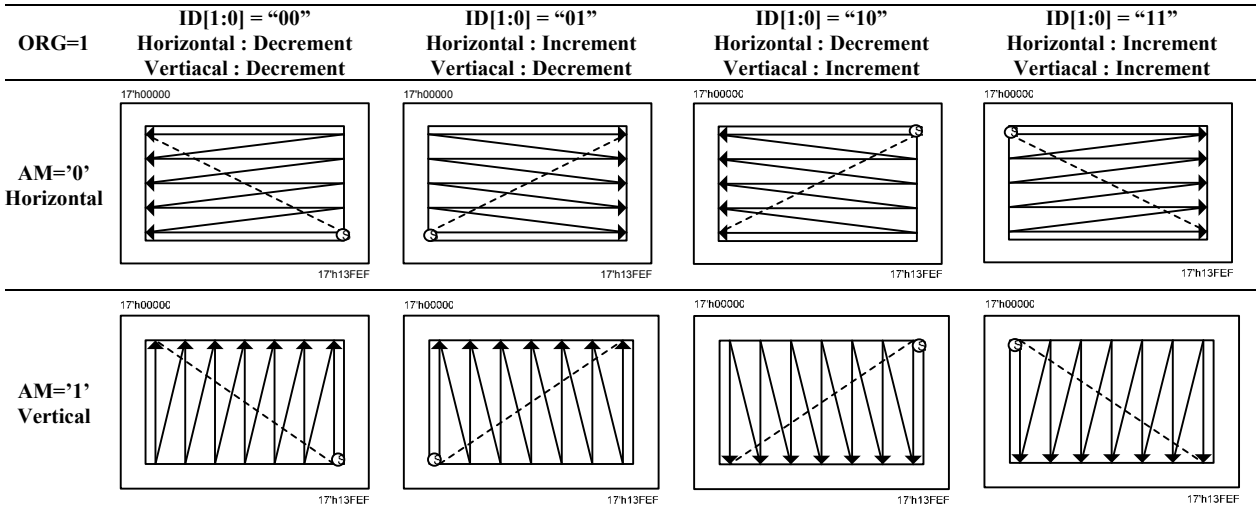


Figure 10 Automatic address update (ORG=1, AM, ID)

Resizing Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV[1:0]		0	0	RCH[1:0]		0	0	RSZ[1:0]	

RSZ[1:0] – Sets the resizing factor. When the RSZ bits are set for resizing, the LGDP4532 writes the data of the resized image in both horizontal and vertical directions according to the resizing factor on the internal GRAM. See “Resizing fuction”.

RCH[1:0] – Sets the number of pixels made as the remainder in horizontal direction as a result of resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2’h0 when not using the resizing function (RSZ=2’h0) or there are no remainder pixels.

RCV[1:0] – Sets the number of pixels made as the remainder in vertical direction as a result of resizing a picture. By specifying the number of remainder pixels with RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2’h0 when not using the resizing function (RSZ=2’h0) or there are no remainder pixels.

Table 9

RSZ[1:0]	Resizing scale
2’h0	No resizing (x1)
2’h1	x 1/2
2’h2	Setting disabled
2’h3	x 1/4

Table 10

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
2’h0	0 pixel
2’h1	1 pixel
2’h2	2 pixels
2’h3	3 pixels

Table 11

RCV[1:0]	Number of remainder Pixels in Vertical Direction
2’h0	0 pixel
2’h1	1 pixel
2’h2	2 pixels
2’h3	3 pixels

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE[1:0]		0	0	0	BASEE	0	0	GON	DTE	COL	0	D[1:0]	

D[1:0] – A graphics display appears on the screen when D[1] = "1", and is turned off upon setting D[1] = "0". When setting D[1] = "0", the graphics display data are retained in the internal GRAM and the display appears instantly on the screen upon setting D[1] to "1". When the D[1] bit is "0", i.e. while no display is shown on the screen, all source outputs are at the GND level to reduce charging/discharging current on liquid crystal cells, which is generated during liquid crystal AC drive.

When the display is turned off by setting D[1:0] = 2'h1, the LGDP4532 continues internal display operation. When the display is turned off by setting D[1:0] = 2'h0, the LGDP4532's internal display operation is halted completely. In combination with GON bit, the D[1:0] bits control ON/OFF of graphics display. For details, see "Instruction setting".

Table 12

D[1:0]	BASEE	Source Output (S1-720)	FMARK signal	Internal Operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-display	Operation	Operation
2'h3	0	Non-display	Operation	Operation
	1	Base-image display	Operation	Operation

Notes: 1. The data write operation from the microcomputer is not affected by the setting in the D[1:0] bits.
2. The PTS bits set the source output level for "non-lit display"

COL – When COL = "1", the 8-color display mode is selected. For details, see the "8-color Display Mode" section. The 8-color display mode is not available in external interface mode.

Table 13

COL	Operating amplifier	Display color
1'h0	64	262,144
1'h1	2	8

Note: When COL=1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

GON, DTE – The combination of settings in GON and DTE bits sets the output level form gate lines(G1-G320). When GON=0, the Vcom output level becomes the GND level.

Table 14

GON	DTE	G1-G320
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

BASEE – Base image display enable bit.

BASEE = 0 : No base image is displayed. The LGDP4532 drives liquid crystal at no-display level or shows only partial images on the screen.

BASEE = 1 : A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE[1:0] – PTDE[0] is the display enable bit of partial image 1. PTDE[1] is the display enable bit of partial image 2. When PTDE[1]/[0]=0, the partial image is turned off and only base image is displayed on the screen. When PTDE[1]/[0]= 1, the partial image is displayed on the screen. In this case, turn off the base image by setting BASEE = 0.

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP[3:0]				0	0	0	0	BP[3:0]			

FP[3:0]/BP[3:0] – Sets the blank period made at the beginning and the end of a display (front porch and back porch, respectively). The FP[3:0] and BP[3:0] bits specify the number of lines for the front and back porch periods, respectively. In setting, be sure:

BP + FP ≤ 16 lines
FP ≥ 2 lines
BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal.

Table 15

FP[3:0]/BP[3:0]	Number of lines for the front/back porches
4'h0	Setting disabled
4'h1	Setting disabled
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting disabled

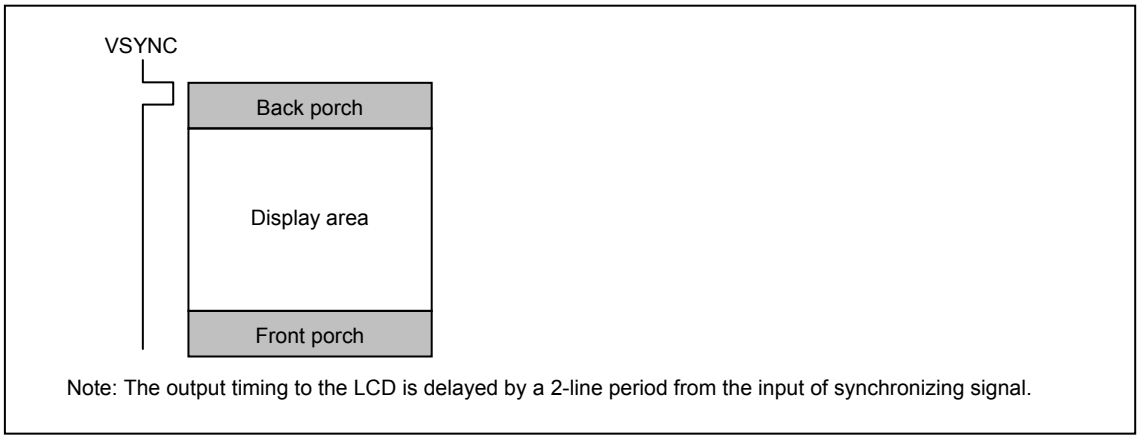


Figure 11 Back/front porches

Set the BP[3:0], FP[3:0] bits as follows in each operation mode.

Table 16

Internal clock operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS[2:0]			0	0	PTG[1:0]		ISC[3:0]			

ISC[3:0] – Set the interval of scan when PTG[1:0] sets the interval scan. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal is inverted in the same cycle as the interval scan.

Table 17

ISC[3:0]	Scan cycle	Time for interval when(fFLM)=60Hz
4'h0	Setting disabled	-
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTG[1:0] – Set the scan mode in non-display area, which is made between partial display periods of the first and the second images, or turning off both base and partial images(full-screen non display). The setting is commonly applied to all non-display drive period.

Table 18

PTG[1:0]	Gate drive operation In non-display area	Source output level In non-display area	Vcom output
2'h0	Normal scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h1	Setting disabled	-	-
2'h2	Interval scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h3	Setting disabled	-	-

Note: Select frame-inversion AC drive when setting interval scan.

PTS[2:0] – Set the source output in non-display drive period.

Table 19

PTS[2:0]	Source output level		Grayscale amplifier In operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3h0	V63	V0	V0 to V63	Register setting(DC0,DC1)
3h1	Setting disabled	Setting disabled	-	-
3h2	GND	GND	V0 to V63	Register setting(DC0,DC1)
3h3	Hi-Z	Hi-Z	V0 to V63	Register setting(DC0,DC1)
3'h4	V63	V0	V0 and V63	1/2 the frequency set with DC0,DC1
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0 and V63	1/2 the frequency set with DC0,DC1
3'h7	Hi-Z	Hi-Z	V0 and V63	1/2 the frequency set with DC0,DC1

Notes: 1.The gate output level in non-display drive period is controlled by the PTG setting(off-scan mode).

Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI[2:0]		

FMI[2:0] – Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE – When FMARKOE=1, the LGDP4532 starts outputting FMARK signal from the FMARK pin in the output interval set with the FMI[2:0] bits. See "FMARK" for details.

Table 20

FMI[2:0]	Output interval
3'h0	1 frame
3'h1	2frame
3'h3	4 frame
3'h5	6 frame
Others settings	Setting disabled

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	ENC[1:0]		0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	

ENC[1:0] – Sets the RAM data write cycle in RGB interface mode.

Table 21 ENC[1:0] bits

ENC[1:0]	RAM data write cycle
2'h00	Write data to RAM every frame cycle
2'h01	Setting disabled
2'h10	Write data to RAM every 2 frame cycles
2'h11	Write data to RAM every 4 frame cycles

RM – Selects the interface to access the LGDP4532's internal GRAM. The RAM access is possible only via the interface selected with the RM bit. Set RM to "1" when writing display data via the RGB interface. The LGDP4532 allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 22 RM bit

RM	Interface for RAM access
1'h0	System interface/VSYNC interface
1'h1	RGB interface

RIM[1:0] – Selects one of the following RGB interface modes when the RGB interface mode is selected with the RM and DM bits. Make this setting before display operation via external display interface. Do not make changes to the setting during display operation.

Table 23 RIM[1:0] bits

RIM[1:0]	RGB interface mode
2'h00	18-bit RGB interface (1 transfer/pixel)
2'h01	16-bit RGB interface (1 transfer/pixel)
2'h10	6-bit RGB interface (3 transfers/pixel)
2'h11	Setting disabled

DM[1:0] – Sets the display operation mode. By setting DM[1:0] as follows, it is possible to switch between the internal clock operation mode and the external display interface mode. Do not switch between different external interface modes (RGB interface and VSYNC interface).

Table 24 DM[1:0] bits

DM[1:0]	Display operation mode
2'h00	Internal clock operation
2'h01	RGB interface
2'h10	VSYNC interface
2'h11	Setting disabled

Notes:

1. Instructions are set only via the system interface.

2. Be sure that data transfer and dot clock input are performed in units of RGB dots in 6-bit RGB interface mode.

As the following table, the optimum interface for the state of display can be selected by setting the external display interface mode.

Table 25

Display State	Operation mode	RAM access (RM)	Display mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 01)
Rewrite still picture area while display moving pictures	RGB interface (2)	System interface (RM = 0)	RGB interface (DM = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM = 10)

Notes:
1. Instructions are set only via the system interface.
2. The RGB-I/F and the VSYNC-I/F are not used simultaneously.
3. Do not make changes to the RGB-I/F mode setting (RIM) while the RGB I/F is in operation.
4. See the “External Display Interface” section for the flowcharts to follow when switching from one mode to another.

Internal clock operation mode

All display operations are synchronized with the signals generated from the internal operating clock in this mode. None of inputs via the external display interface are valid. The internal RAM is accessible only via the system interface.

RGB interface mode (1)

In RGB interface mode, display operations are synchronized with the frame synchronizing signal (VSYNC), the line synchronizing signal (HSYNC), and the dot clock (DOTCLK). These signals must be supplied through a display period using the RGB interface.

Display data are transferred in units of pixels via the DB[17:0] pins. All display data are stored in the internal RAM. The combined use of the high-speed RAM write mode and the widow address function enables not only displaying data in moving picture area and data in the internal RAM in other than the moving picture area at a time but also minimizing data transfer by transferring data only when rewriting screen.

The front porch (FP) and back porch (BP) periods, and the display duration period (NL) are automatically calculated inside the LGDP4532 by internally counting the number of line synchronizing signal clocks (HSYNC) from the falling edge of the frame synchronizing signal (VSYNC). Take this into consideration when transferring RGB data via the DB[17:0] pins.

RGB interface mode (2)

The LGDP4532 enables rewriting RAM data via the system interface while the RGB interface is selected for display operation. In this case, Be sure to write RAM data while display data are not being transferred via the RGB interface (ENABLE = High). To return to the display data transfer mode via the RGB interface, change the ENABLE bit first and then set a new address (AD[15:0]) in the AC and the index register to R22h.

VSYNC interface mode

In VSYNC interface mode, internal display operations are synchronized with the frame synchronizing signal (VSYNC). In this mode, a moving picture can be displayed via the system interface by writing data to the internal RAM at more than the minimum speed from the falling edge of frame synchronizing signal (VSYNC). In this case, there are constraints in the RAM writing speed and method. For details, see "External Display Interface".

No external signal input except VSYNC input is accepted in VSYNC interface mode.

The timings and durations of front porch (FP), back porch (BP) periods and display duration period (NL) are automatically calculated from the falling edge of the frame synchronization signal (VSYNC) according to the instructions set in the relevant registers.

Frame Marker Position (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	FMP[8:0]								

FMP[8:0] – Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is output at the start of back porch period for 1H period (IOVcc-IOGND amplitude signal). FMARK can be used as a trigger signal for frame synchronous write operation. See "FMARK" for details.

Make sure 9'h000 <=FMP <= BP+NL+FP

Table 26

FMP[8:0]	FMARK output position
9'h000	0th line
9'h001	1st line
9'h002	2nd line
:	:
9'h14D	333rd line
9'h14E	334th line
9'h14F	335th line

External Display Interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

DPL – Sets the signal polarity of DOTCLK pin.

DPL = 0 : input data on the rising edge of DOTCLK
DPL = 1 : input data on the falling edge of DOTCLK

EPL – Sets the signal polarity of ENABLE pin.

EPL = 0 : writes data DB[17:0] when ENABLE = 0 and disables data write operation when ENABLE = 1.
EPL = 1 : writes data DB[17:0] when ENABLE = 1 and disables data write operation when ENABLE = 0.

HSPL – Sets the signal polarity of HSYNC pin.
HSPL = 0 : Low active
HSPL = 1 : High active

VSPL – Sets the signal polarity of VSYNC pin.
VSPL = 0 : Low active
VSPL = 1 : High active

Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	SAP[2:0]				BT[2:0]			0	AP[2:0]			DK	DSTB	SLP	STB

STB – When STB = "1", the LGDP4532 enters the standby mode. In standby mode, the display operation completely halts, and the internal operation, including internal RC oscillation and reception of external clock pulses, completely halts. Only instructions to release the LGDP4532 from the standby mode (STB = "0") and to start oscillators are accepted during the standby mode. To set the standby mode, follow the sequence of standby mode setting.

SLP – When SLP = 1, the LGDP4532 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change of GRAM data or instruction is accepted in sleep mode. The GRAM data and the instruction bits remain unchanged.

DSTB – When DSTB = 1, the LGDP4532 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and the instruction bit setting are destroyed and must be reset after exiting deep standby mode.

DK – Activates DDVDH. When DK = 0, DDVDH activates at the same timing as VGH. When DK = 1, DDVDH activates separately from VGH.

Table 27

DK	Step-up Cycle in Step-up Circuit 1
1'h0	Startup DDVDH simultaneously with VGH. Startup steup-up circuit 1 (VLOUT1 output) accordint to AP[2:0]
1'h1	Halt step-up circuit 1 (VLOUT1). (Default)

AP[2:0] – Adjusts the constant current in the operation amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0]=3'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.
Adjust the amount of fixed current from the fixed-current source in the internal operational amplifier circuit. VGH operates when AP is not 000. Complete setting AP before setting PON = 1. (While setting PON = 1, setting of AP bit cannot be changed.) For the details of sequences, refer to Flow of "Power Supply Setting".

Table 28

AP[2:0]	LCD power supply circuits	Grayscale voltage generating circuit
3'h0	Halt operation	Halt operation
3'h1	Setting disabled	Setting disabled
3'h2	Normal operation	0.5
3'h3	Normal operation	0.75
3'h4	Normal operation	1
3'h5	Normal operation	1.25
3'h6	Normal operation	1.5
3'h7	Setting disabled	Setting disabled

Note: In this table, the constant current in operational amplifiers is shown by the ratio to the constant current when AP[1:0] is set to 2'h3.

BT[2:0] – Sets the factor used in the step-up circuits. Use an optimal step-up factor for the voltage in use. To reduce power consumption, set a smaller factor.

Table 29 Step up factor and output voltage level

BT[2:0]	DDVDH	VGH	VGL	Capacitor connection Pins
3'h0	Vci1 x 2 [x 2]	DDVDH x 4 [x 8]	–(Vci1 + DDVDH x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
3'h1			–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
3'h2			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
3'h3		Vci1 + DDVDH x 3 [x 7]	–(Vci1 + DDVDH x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
3'h4			–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
3'h5			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
3'h6		DDVDH x 3 [x 6]	–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
3'h7			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±

Note: 1. The step-up factor from Vci1 are shown in the brackets [ ].
2. Connect capacitors where required when using DDVDH, VGH, VGL voltages.
3. Set the following voltages within the respective ranges:
DDVDH = 6.0V(max.), VGH = 15.0V (max.) and VGL = -12.5V (max.)

SAP[2:0] – Adjust the constant current for the operational amplifer circuit in the source driver. A larger constant current stabilizes the operational ampilifer circuit, but current consumption increases. Adjust the constant current taking the display quality-current consumprion trade-off into account. During a period showing no display, set SAP = 0 to halt the operational amplifier circuit to reduce current consumption.

Table 30

SAP[2:0]	Constant current (ratio to 3)
3'h0	Halt operational amplifier
3'h1	Constant current (ratio to 3) : 0.65
3'h2	Constant current (ratio to 3) : 0.8
3'h3	Constant current (ratio to 3) : 1.00
3'h4	Constant current (ratio to 3) : 1.35
3'h5	Constant current (ratio to 3) : 1.60
3'h6	Setting disabled
3'h7	Setting disabled

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC1[2:0]			0	DC0[2:0]			0	VC[2:0]		

Table 31 Step-up frequency (Step-up Circuit 1)

DC0[2:0]	Step-up circuit 1 : step-up frequency (f_{DCDC1})
3'h0	fosc/8
3'h1	fosc/16
3'h2	fosc/32
3'h3	fosc/64
3'h4	fosc/128
3'h5	fosc/4
3'h6	Halt step-up circuit 1
3'h7	fosc/2

Note : Make sure to set DC0 and DC1 to maintain $f_{DCDC1} \geq f_{DCDC2}$.

Table 32 Step-up frequency (Step-up Circuit 2)

DC1[2:0]	Step-up circuit 2 : step-up frequency (f_{DCDC2})
3'h0	fosc/128
3'h1	fosc/256
3'h2	fosc/512
3'h3	fosc/1024
3'h4	fosc/2048
3'h5	fosc/64
3'h6	Halt step-up circuit 2
3'h7	fosc/32

Note : Make sure to set DC0 and DC1 to maintain $f_{DCDC1} \geq f_{DCDC2}$.

Table 33 VciOUT output level

VC[2:0]	VciOUT (Reference Voltage) (Vci1 Voltage)
3'h0	1.00 x VciLVL
3'h1	0.92 x VciLVL
3'h2	0.90 x VciLVL
3'h3	0.87 x VciLVL
3'h4	0.85 x VciLVL
3'h5	0.83 x VciLVL
3'h6	0.73 x VciLVL
3'h7	Setting disabled

Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH[3:0]			

VRH[3:0] – Sets the factor to generate VREG1OUT from VciLVL.

Table 34 VREG1OUT

VRH[3:0]	VREG1OUT Voltage
4'h0	VciOUT x 1.27
4'h1	VciOUT x 1.32
4'h2	VciOUT x 1.37
4'h3	VciOUT x 1.42
4'h4	VciOUT x 1.47
4'h5	VciOUT x 1.52
4'h6	VciOUT x 1.57
4'h7	Setting disabled
4'h8	Setting disabled
4'h9	VciOUT x 1.62
4'hA	VciOUT x 1.67
4'hB	VciOUT x 1.72
4'hC	VciOUT x 1.77
4'hD	VciOUT x 1.82
4'hE	VciOUT x 1.87
4'hF	VciOUT x 1.92

Note: Set the VC and VRH bits to maintain the VREG1OUT voltage at (DDVDH – 0.5) V or less.

PON – Controls the operation to generate VLOUT3. In setting the PON bit, follows the power-supply startup sequence.

PON = 0 : Halts the step-up operation to generate VLOUT3.
PON = 1 : Starts the step-up operation to generate VLOUT3.

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV[4:0]					0	VCM[6:0]						

VCM[6:0] – Sets the VcomH level (the higher voltage of Vcom alternating drive). VCM[6:0] specifies the voltage by VREG1OUT x n, where n is a discrete number from 0.400 to 0.875. To halt internal volume and adjust VcomH with an external resistor from VcomR, set VCM[6:0] = "1111111".

Table 35

VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH
7'h00	VREG1OUT x 0.400	7'h20	VREG1OUT x 0.560	7'h40	VREG1OUT x 0.720	7'h60	VREG1OUT x 0.880
7'h01	VREG1OUT x 0.405	7'h21	VREG1OUT x 0.565	7'h41	VREG1OUT x 0.725	7'h61	VREG1OUT x 0.885
7'h02	VREG1OUT x 0.410	7'h22	VREG1OUT x 0.570	7'h42	VREG1OUT x 0.730	7'h62	VREG1OUT x 0.890
7'h03	VREG1OUT x 0.415	7'h23	VREG1OUT x 0.575	7'h43	VREG1OUT x 0.735	7'h63	VREG1OUT x 0.895
7'h04	VREG1OUT x 0.420	7'h24	VREG1OUT x 0.580	7'h44	VREG1OUT x 0.740	7'h64	VREG1OUT x 0.900
7'h05	VREG1OUT x 0.425	7'h25	VREG1OUT x 0.585	7'h45	VREG1OUT x 0.745	7'h65	VREG1OUT x 0.905
7'h06	VREG1OUT x 0.430	7'h26	VREG1OUT x 0.590	7'h46	VREG1OUT x 0.750	7'h66	VREG1OUT x 0.910
7'h07	VREG1OUT x 0.435	7'h27	VREG1OUT x 0.595	7'h47	VREG1OUT x 0.755	7'h67	VREG1OUT x 0.915
7'h08	VREG1OUT x 0.440	7'h28	VREG1OUT x 0.600	7'h48	VREG1OUT x 0.760	7'h68	VREG1OUT x 0.920
7'h09	VREG1OUT x 0.445	7'h29	VREG1OUT x 0.605	7'h49	VREG1OUT x 0.765	7'h69	VREG1OUT x 0.925
7'h0A	VREG1OUT x 0.450	7'h2A	VREG1OUT x 0.610	7'h4A	VREG1OUT x 0.770	7'h6A	VREG1OUT x 0.930
7'h0B	VREG1OUT x 0.455	7'h2B	VREG1OUT x 0.615	7'h4B	VREG1OUT x 0.775	7'h6B	VREG1OUT x 0.935
7'h0C	VREG1OUT x 0.460	7'h2C	VREG1OUT x 0.620	7'h4C	VREG1OUT x 0.780	7'h6C	VREG1OUT x 0.940
7'h0D	VREG1OUT x 0.465	7'h2D	VREG1OUT x 0.625	7'h4D	VREG1OUT x 0.785	7'h6D	VREG1OUT x 0.945
7'h0E	VREG1OUT x 0.470	7'h2E	VREG1OUT x 0.630	7'h4E	VREG1OUT x 0.790	7'h6E	VREG1OUT x 0.950
7'h0F	VREG1OUT x 0.475	7'h2F	VREG1OUT x 0.635	7'h4F	VREG1OUT x 0.795	7'h6F	VREG1OUT x 0.955
7'h10	VREG1OUT x 0.480	7'h30	VREG1OUT x 0.640	7'h50	VREG1OUT x 0.800	7'h70	VREG1OUT x 0.960
7'h11	VREG1OUT x 0.485	7'h31	VREG1OUT x 0.645	7'h51	VREG1OUT x 0.805	7'h71	VREG1OUT x 0.965
7'h12	VREG1OUT x 0.490	7'h32	VREG1OUT x 0.650	7'h52	VREG1OUT x 0.810	7'h72	VREG1OUT x 0.970
7'h13	VREG1OUT x 0.495	7'h33	VREG1OUT x 0.655	7'h53	VREG1OUT x 0.815	7'h73	VREG1OUT x 0.975
7'h14	VREG1OUT x 0.500	7'h34	VREG1OUT x 0.660	7'h54	VREG1OUT x 0.820	7'h74	VREG1OUT x 0.980
7'h15	VREG1OUT x 0.505	7'h35	VREG1OUT x 0.665	7'h55	VREG1OUT x 0.825	7'h75	Setting disabled
7'h16	VREG1OUT x 0.510	7'h36	VREG1OUT x 0.670	7'h56	VREG1OUT x 0.830	7'h76	Setting disabled
7'h17	VREG1OUT x 0.515	7'h37	VREG1OUT x 0.675	7'h57	VREG1OUT x 0.835	7'h77	Setting disabled
7'h18	VREG1OUT x 0.520	7'h38	VREG1OUT x 0.680	7'h58	VREG1OUT x 0.840	7'h78	Setting disabled
7'h19	VREG1OUT x 0.525	7'h39	VREG1OUT x 0.685	7'h59	VREG1OUT x 0.845	7'h79	Setting disabled
7'h1A	VREG1OUT x 0.530	7'h3A	VREG1OUT x 0.690	7'h5A	VREG1OUT x 0.850	7'h7A	Setting disabled
7'h1B	VREG1OUT x 0.535	7'h3B	VREG1OUT x 0.695	7'h5B	VREG1OUT x 0.855	7'h7B	Setting disabled
7'h1C	VREG1OUT x 0.540	7'h3C	VREG1OUT x 0.700	7'h5C	VREG1OUT x 0.860	7'h7C	Setting disabled
7'h1D	VREG1OUT x 0.545	7'h3D	VREG1OUT x 0.705	7'h5D	VREG1OUT x 0.865	7'h7D	Setting disabled
7'h1E	VREG1OUT x 0.550	7'h3E	VREG1OUT x 0.710	7'h5E	VREG1OUT x 0.870	7'h7E	Setting disabled
7'h1F	VREG1OUT x 0.555	7'h3F	VREG1OUT x 0.715	7'h5F	VREG1OUT x 0.875	7'h7F	Halt internal volume.

Note : Set the VcomH voltage from 2.5V to (DDVDH – 0.5) V.

VDV[4:0] – Sets the alternating amplitudes of VCOM AC voltage. These bits amplify VCOM by from 0.6 to 1.23 times the VREG1OUT voltage. If VCOMG = 0, VDV[4:0] bits are disabled.

Table 36

VDV[4:0]	Vcom amplitude	VDV[4:0]	Vcom amplitude
5'h00	VREG1OUT x 0.60	5'h10	VREG1OUT x 1.05
5'h01	VREG1OUT x 0.63	5'h11	VREG1OUT x 1.08
5'h02	VREG1OUT x 0.66	5'h12	VREG1OUT x 1.11
5'h03	VREG1OUT x 0.69	5'h13	VREG1OUT x 1.14
5'h04	VREG1OUT x 0.72	5'h14	VREG1OUT x 1.17
5'h05	VREG1OUT x 0.75	5'h15	VREG1OUT x 1.20
5'h06	VREG1OUT x 0.78	5'h16	VREG1OUT x 1.23
5'h07	VREG1OUT x 0.81	5'h17	VREG1OUT x 1.26
5'h08	VREG1OUT x 0.84	5'h18	VREG1OUT x 1.29
5'h09	VREG1OUT x 0.87	5'h19	VREG1OUT x 1.32
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.35
5'h0B	VREG1OUT x 0.93	5'h1B	VREG1OUT x 1.38
5'h0C	VREG1OUT x 0.96	5'h1C	VREG1OUT x 1.41
5'h0D	VREG1OUT x 0.99	5'h1D	VREG1OUT x 1.44
5'h0E	VREG1OUT x 1.02	5'h1E	VREG1OUT x 1.47
5'h0F	Setting disabled	5'h1F	VREG1OUT x 1.50

Note : Set the VcomH voltage from 2.5V to (DDVDH – 0.5) V.

VCOMG – When VCOMG = 1, the LGDP4532 can output a negative voltage level for VCOML (1.0 ~ -Vci + 0.5V max). When VCOMG = 0, the LGDP4532 halts the amplifier for negative voltage to save power. When VCOMG = 0, the VDV[4:0] bits are disabled. In this case, adjust the amplitude of VCOM AV voltage with VCM[4:0] bits (VCOMH setting). Set PON = 1 before setting VCOMG = 1.
When VCOMG = 1, voltage of VCOML can be set to any level, and instruction (VDV) becomes valid. VCOMG = 1 is valid when PON = 1. When COMG = 0, output of VCOML if fixed to GND level, and setting of instruction (VDV) becomes invalid. When VCOMG = 0, output of VCOML and VCL stop.

Regulator Control (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RSET			0	RI[2:0]			0	RV[2:0]			0	RCONT[2:0]		

RCONT[2:0] – These bits control the input voltage of main bias op_amp.

Table 37

RCONT[2:0]	Input voltage
3'h0	Vci x 0.25
3'h1	Setting diabled
3'h2	Open
3'h3	Vci x 0.30
3'h4	Setting disabled
3'h5	Setting disabled
3'h6	Vci x 0.20
3'h7	Setting disabled

RV[2:0] – These bits control the output voltage of internal logic regulator.

Table 38

RV [2:0]	Vdd voltage
3'h0	Vci x 0.80
3'h1	Vci x 0.75
3'h2	Vci x 0.70
3'h3	Vci x 0.65
3'h4	Vci x 0.60
3'h5	Vci x 0.55
3'h6	Vci x 0.50
3'h7	Vci x 0.45

RI[2:0] – These bits control the bias current of internal logic regulator.

Table 39

RI [2:0]	Constant current
3'h0	0.2
3'h1	0.1
3'h2	2.2
3'h3	3
3'h4	3.2
3'h5	4
3'h6	5.2
3'h7	6

Note : In this table, the constant current is shown by the ratio to the constant current when RI[2:0] is set to 3'h3.

RSET[2:0] – These bits control the main bias.

Gamma Select Control (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SGE	0	0	0	EN_MA	0	0	0	PS

PS – This bit specify the VA mode enable signal.

Table 40

PS	Mode
1'h0	TN mode
1'h1	VA mode

EN_MA – This bit specify the PFN0-5/PFP0-1/PMN/PMP registers Manaul setting enable signal.

Table 41

		EN_MA	PS
Auto	TN mode	0	0
	VA mode	0	1
Manual	User setting	1	x

SGE – Sets the R/G/B gamma register.

Table 42

SGE	
0	R/G/B gamma register: R30h-R3Fh
1	R gamma register : R30h ~ R3Fh G gamma register : RB0h ~RBFh B gamma register : RC0h ~RCFh

Vcom Control (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	LSZ[2:0]			0	HSZ[2:0]			0	0	0	CMFPD

CMFPD – This bit controls feedback power-down of VCOM amplifier.
CMFPD = 0 : Enable the internal feedback of VCOM amplifier.
CMFPD = 1 : Disable the internal feedback of VCOM amplifier.

HSZ[2:0] – These bits control the feedback bias of VCOMH amplifier.

LSZ[2:0] – These bits control the feedback bias of VCOML amplifier.

RAM Address Set (Horizontal Address) (R20h)

RAM Address Set (Vertical Address) (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD[7:0]							
W	1	0	0	0	0	0	0	0	AD[16:8]								

AD[16:0] – A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as data is written to the internal GRAM in order to write data consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM='1'), the address AD[16:0] is set in the address counter every frame on the falling edge of VSYNC.
Note 2: In internal clock operation and VSYNC interface operation (RM='0'), the address AD[16:0] is set when executing the instruction.

Table 43

AD[16:0]	**GRAM Data Setting**
17'h00000 – 17'h000EF	Bitmap data on the first line
17'h00100 – 17'h001EF	Bitmap data on the second line
17'h00200 – 17'h002EF	Bitmap data on the third line
:	:
17'h16500 – 17'h13DEF	Bitmap data on the 318th line
17'h16600 – 17'h13EEF	Bitmap data on the 319th line
17'h16700 – 17'h13FEF	Bitmap data on the 320th line

Write Data to RAM (R22h)

R/W	RS	The bit assignment between RAM write data WD[17:0] and DB[17:0] differs according to the selected interface.
W	1	WD[17:0]

WD[17:0] – The LGDP4532 write data to the internal GRAM by expanding into 18 bits internally. The data expansion fomat into 18 bits differs according to the interface.

The GRAM data represents the grayscale level. The LGDP4532 automatically updates the address according to AM and I/D[1:0] as it writes data in the GRAM. In standby mode, the GRAM is not accessible. The data in 16-bit format is developed into 18 bits according to the register setting (DFM) in 8-/16-bit interface operation.

Note : When writing data in the GRAM via system interface while using the RGB interface, make sure that write operation via two interface do not conflict.

Table 44 GRAM data and corresponding LCD Grayscale level (REV = 1)

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h00	V63	V0
6'h01	V62	V1
6'h02	V61	V2
6'h03	V60	V3
6'h04	V59	V4
6'h05	V58	V5
6'h06	V57	V6
6'h07	V56	V7
6'h08	V55	V8
6'h09	V54	V9
6'h0A	V53	V10
6'h0B	V52	V11
6'h0C	V51	V12
6'h0D	V50	V13
6'h0E	V49	V14
6'h0F	V48	V15
6'h10	V47	V16
6'h11	V46	V17
6'h12	V45	V18
6'h13	V44	V19
6'h14	V43	V20
6'h15	V42	V21
6'h16	V41	V22
6'h17	V40	V23
6'h18	V39	V24
6'h19	V38	V25
6'h1A	V37	V26
6'h1B	V36	V27
6'h1C	V35	V28
6'h1D	V34	V29
6'h1E	V33	V30
6'h1F	V32	V31

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h20	V31	V32
6'h21	V30	V33
6'h22	V29	V34
6'h23	V28	V35
6'h24	V27	V36
6'h25	V26	V37
6'h26	V25	V38
6'h27	V24	V39
6'h28	V23	V40
6'h29	V22	V41
6'h2A	V21	V42
6'h2B	V20	V43
6'h2C	V19	V44
6'h2D	V18	V45
6'h2E	V17	V46
6'h2F	V16	V47
6'h30	V15	V48
6'h31	V14	V49
6'h32	V13	V50
6'h33	V12	V51
6'h34	V11	V52
6'h35	V10	V53
6'h36	V9	V54
6'h37	V8	V55
6'h38	V7	V56
6'h39	V6	V57
6'h3A	V5	V58
6'h3B	V4	V59
6'h3C	V3	V60
6'h3D	V2	V61
6'h3E	V1	V62
6'h3F	V0	V63

Table45 GRAM data and corresponding LCD Grayscale level (REV = 0)

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h00	V0	V63
6'h01	V1	V62
6'h02	V2	V61
6'h03	V3	V60
6'h04	V4	V59
6'h05	V5	V58
6'h06	V6	V57
6'h07	V7	V56
6'h08	V8	V55
6'h09	V9	V54
6'h0A	V10	V53
6'h0B	V11	V52
6'h0C	V12	V51
6'h0D	V13	V50
6'h0E	V14	V49
6'h0F	V15	V48
6'h10	V16	V47
6'h11	V17	V46
6'h12	V18	V45
6'h13	V19	V44
6'h14	V20	V43
6'h15	V21	V42
6'h16	V22	V41
6'h17	V23	V40
6'h18	V24	V39
6'h19	V25	V38
6'h1A	V26	V37
6'h1B	V27	V36
6'h1C	V28	V35
6'h1D	V29	V34
6'h1E	V30	V33
6'h1F	V31	V32

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h20	V32	V31
6'h21	V33	V30
6'h22	V34	V29
6'h23	V35	V28
6'h24	V36	V27
6'h25	V37	V26
6'h26	V38	V25
6'h27	V39	V24
6'h28	V40	V23
6'h29	V41	V22
6'h2A	V42	V21
6'h2B	V43	V20
6'h2C	V44	V19
6'h2D	V45	V18
6'h2E	V46	V17
6'h2F	V47	V16
6'h30	V48	V15
6'h31	V49	V14
6'h32	V50	V13
6'h33	V51	V12
6'h34	V52	V11
6'h35	V53	V10
6'h36	V54	V9
6'h37	V55	V8
6'h38	V56	V7
6'h39	V57	V6
6'h3A	V58	V5
6'h3B	V59	V4
6'h3C	V60	V3
6'h3D	V61	V2
6'h3E	V62	V1
6'h3F	V63	V0

Read Data from RAM (R22h)

R/W	RS	The bit assignment between RAM write data RD[17:0] and DB[17:0] differs according to the selected interface.
R	1	RD[17:0]

RD[17:0] – 18-bit data read from the GRAM. The bit assignment between RD[17:0] and DB[17:0] (data on the data bus) differs according to the selected interface.

When the LGDP4532 read data from the GRAM to the microcomputer, the first word read immediately after RAM address set is taken in the intenal read-data latch and inbalid data is sent to the data bus DB[17:0]. Vaild data is sent to the data bus as the LGDP4532 reads out the second and subsequence words.

When either 8-bit or 16-bit interface is selected, the LSB of R and B dot data are not read out.

Note : This register is not available in RGB interface operation.

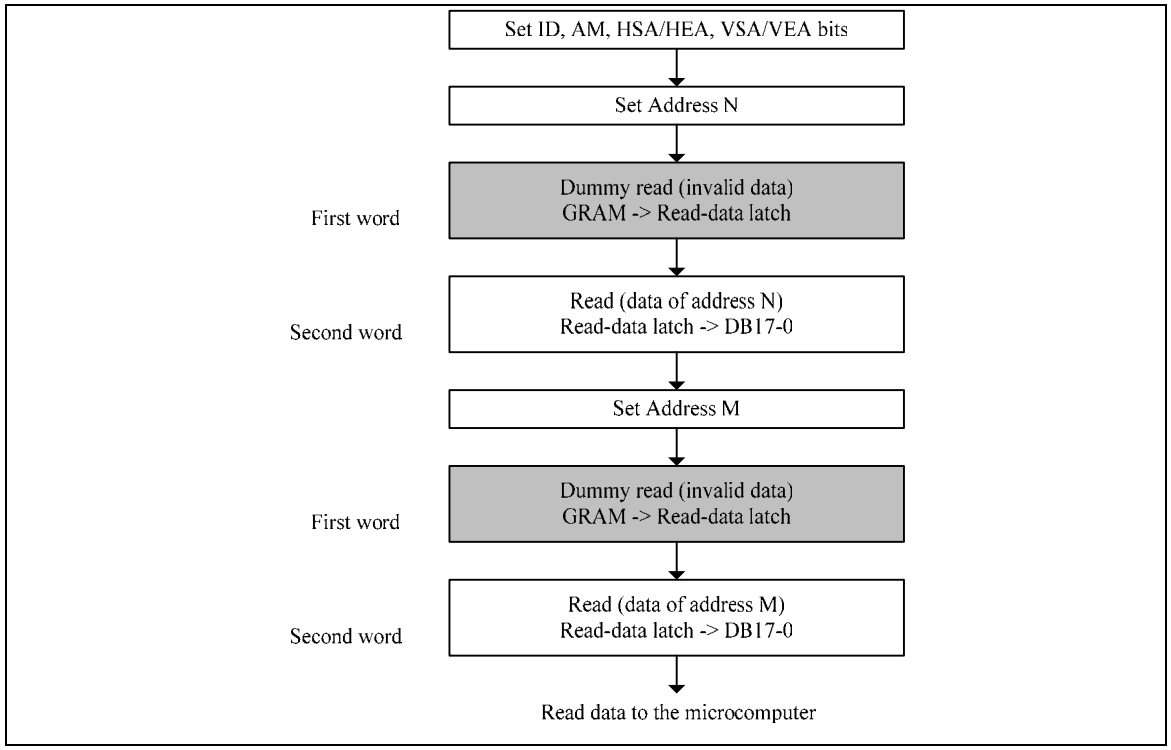


Figure 12

Red Gamma Control 1-16 (R30h to R3Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				
W	1						PFP1[2:0]								PFP0[2:0]		
W	1						PFP3[2:0]								PFP2[2:0]		
W	1						PFN1[2:0]								PFN0[2:0]		
W	1						PFN3[2:0]								PFN2[2:0]		
W	1														PMP[2:0]		
W	1														PMN[2:0]		

PKP5-0[2 :0] – γ fine-adjustment register for positive polarity
PRP1-0[2 :0] – γ gradient-adjustment register for positive polarity
VRP0[3:0], VRP1[4 :0] – γ amplitude-adjustment register for positive polarity

PKN5-0[2 :0] – γ fine-adjustment register for negative polarity
PRN1-0[2 :0] – γ gradient-adjustment register for negative polarity
VRN0[3:0], VRN1[4 :0] – γ amplitude-adjustment register for negative polarity

PFP3-0[2:0] – γ fine adjustment register bits for positive polarity
PFN3-0[2:0] – γ fine adjustment register bits for negative polarity
PMP[2:0] – γ fine adjustment register bits for positive polarity
PMN[2:0] – γ fine adjustment register bits for negative polarity

Note)
When BGR='1', these register setting vaules are for Blue Gamma Control.

For details see "γ-Correction Function" section

EPROM Control Register 1 (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	PTM[1:0]		POR	VPP	PPROG	PWE	PA[1:0]		PDIN[7:0]							

EPROM programming control. See "EPROM Control" section.

PDIN[7:0] – Data input. This corresponds to VCM[6:0] bits of R13h.

PA[1:0] – address input. This selects one of four banks of the EPROM.

Table 46

PA[1:0]	Write Data Input	Write OPT Cell
2'h0	PDIN[6:0]	Cell[6:0]
2'h1	PDIN[6:0]	Cell[14:8]
2'h2	PDIN[6:0]	Cell[22:16]
2'h3	PDIN[6:0]	Cell[30:24]

PWE – Write enable.

PPROG – Program mode enable.

VPP – Power switch control for the VPP pin of the embedded EPROM. When VPP = "1", the internal VPP is set to 7.2V; otherwise it is set to 1.8V.

POR – Pin for power-on rest.

PTM[1:0] – Pins for enabling test mode

EPROM Control Register 2 (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0										AUTOWR	RA[1:0]		VCMSEL[1:0]	

EPROM programming control. See "EPROM Control" section.

VCMSEL[1:0] – With VCMSEL pin, sets VcomH level from either the register R13h or the EPROM

Table 47

VCMSEL[1:0]	VCMSEL pin	VcomH Level adjustment
00	X	VCM[6:0] of the register R13h
01	X	EPROM data selected by RA[1:0]
1X	0	VCM[6:0] of the register R13h
1X	1	EPROM data selected by RA[1:0]

RA[1:0] – Read address input. This selects one of four banks of the EPROM.

AUTOWR – Select the methoe of write operation
If AUTOWR='1', write address is PA.
Else AUTOWR='0', write address is auto select address.

EPROM Control Register 3 (R42h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0								PDOUT[7:0]						

PDOUT[7:0] – EPROM Read Data output.

Window Horizontal RAM Address Start/End (R50h/R51h)

Window Vertical RAM Address Start/End (R52h/R53h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	HSA[7:0]							
W	1	0	0	0	0	0	0	0	0	HEA[7:0]							
W	1	0	0	0	0	0	0	0	VSA[8:0]								
W	1	0	0	0	0	0	0	0	VEA[8:0]								

HSA[7:0]/HEA[7:0] – HSA[7:0] and HEA[7:0] represent the addresses at the start and end of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the range on the GRAM to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HSA < HEA ≤ 8'hEF.

VSA[8:0]/VEA[8:0] – VSA[8:0] and VEA[8:0] represent the addresses at the start and end of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the range on the GRAM to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h13F.

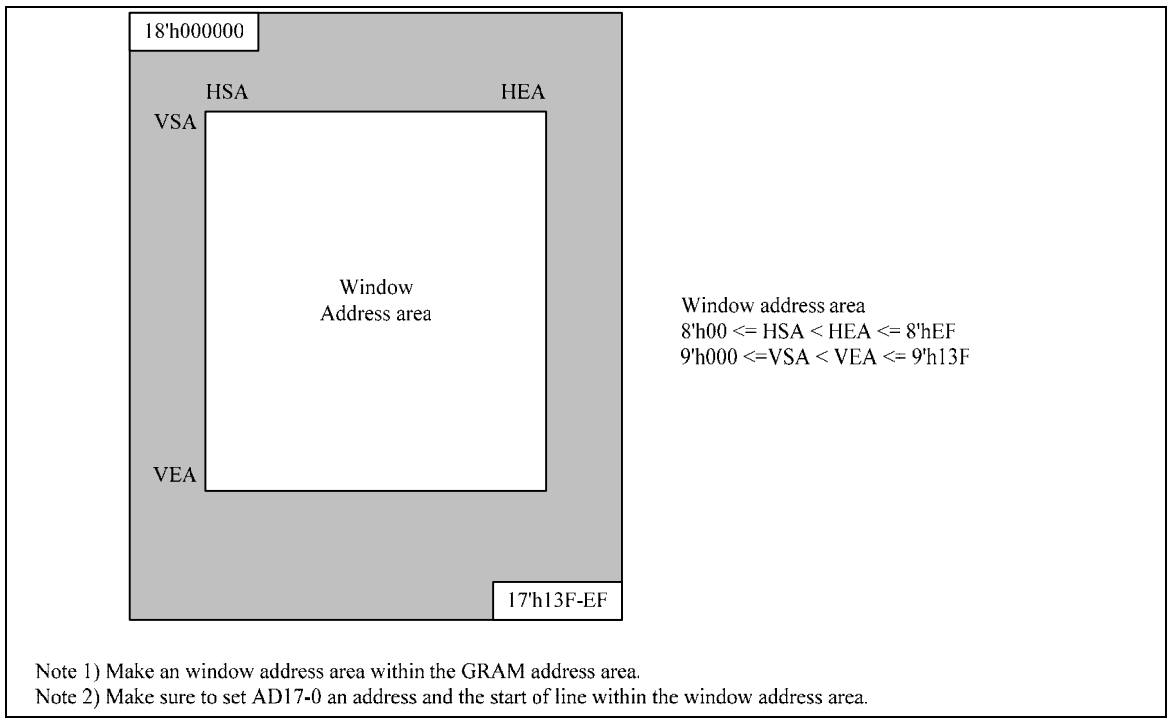


Figure 13

Driver Output Control (R60h)

Base Image Display Control (R61h)

Vertical Scroll Control (R6Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GS	0	NL[5:0]						0	0	SCN[5:0]					
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
W	1	0	0	0	0	0	0	0	VL[8:0]								

SCN[5:0] – Specifies the gate line where the gate driver starts scan.

NL[5:0] – Sets the number of lines to drive the LCD at an interval of 8lines. The GRAM address mapping is not affected by the number of lines set with NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 48

NL[5:0]	Number of Lines	NL[5:0]	Number of Lines
6'h00	8	6'h15	176
6'h01	16	6'h16	184
6'h02	24	6'h17	192
6'h03	32	6'h18	200
6'h04	40	6'h19	208
6'h05	48	6'h1A	216
6'h06	56	6'h1B	224
6'h07	64	6'h1C	232
6'h08	72	6'h1D	240
6'h09	80	6'h1E	248
6'h0A	88	6'h1F	256
6'h0B	96	6'h20	264
6'h0C	104	6'h21	272
6'h0D	112	6'h22	280
6'h0E	120	6'h23	288
6'h0F	128	6'h24	296
6'h10	136	6'h25	304
6'h11	144	6'h26	312
6'h12	152	6'h27	320
6'h13	160	6'h28 – 6'h3F	Setting disabled
6'h14	168		

GS – Set the direction of scan by the gate driver. Set the GS bit in combination with SM and SS bits to optimize scan method to the LCD module.

REV – The grayscale level corresponding to the GRAM data can be reversed by setting REV = 1. This enables the LGDP4532 to display the same image form a same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by resiger setting (PTS).

Table 49

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

VLE – Vertical scroll display enable bit. When VLE = 1, the LGDP4532 starts displaying the base image from the line (of the physical display) determined by setting the VL[8:0] bits. VL[8:0] represents the number of lines shifted from the first line of the physical display (the amount of scrolling). Note that the display position of partial image is not affected by the base image scrolling.

The vertical scrolling is not available in external display inteface opration. In this case, make sure to set VLE = 0.

NDL – Sets the source output level in non-display lit driving periods. By setting the NDL bit, the non-display area can be kept lit on.

Table 50

NDL	Non-display area	
	Positive	Negative
0	V63	V0
1	V0	V63

VL[8:0] – Sets the amount of scrolling the base image by the number of lines. The RAM data in the start line address is displayed on the line, which is shifted from the first line of the liquid crystal panel by the number of lines set with VL[8:0]. In setting VL[8:0], make sure VL ≤ 320.

Table 51

SCN[5:0]	Gate line No (Scan start position)			
	SM = 0		SM = 1	
	GS = 0	GS = 1	GS = 0	GS = 1
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G225	G96
6'h0F	G121	G200	G241	G80
6'h10	G129	G192	G257	G64
6'h11	G137	G184	G273	G48
6'h12	G145	G176	G289	G32
6'h13	G153	G168	G305	G16
6'h14	G161	G160	G2	G319
6'h15	G169	G152	G18	G303
6'h16	G177	G144	G34	G287
6'h17	G185	G136	G50	G271
6'h18	G193	G128	G66	G255
6'h19	G201	G120	G82	G239
6'h1A	G209	G112	G98	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28 – 6'h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Partial Image 1: Display Position (R80h)

RAM Address (Start/End Line Address) (R81h/R82h)

Partial Image 2: Display Position (R83h)

RAM Address (Start/End Line Address) (R84h/R85h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	PTDP0[8:0]								
W	1	0	0	0	0	0	0	0	PTSA0[8:0]								
W	1	0	0	0	0	0	0	0	PTEA0[8:0]								
W	1	0	0	0	0	0	0	0	PTDP1[8:0]								
W	1	0	0	0	0	0	0	0	PTSA1[8:0]								
W	1	0	0	0	0	0	0	0	PTEA1[8:0]								

PTDP0[8:0] – Sets the display position of partial image 1.
PTDP1[8:0] – Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting make sure that

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display position : (PTDP0, PTEA0)
Coordinates of partial image 2 display position : (PTDP1, PTEA1)

If PTDP0 = 9'h000, the partial image 1 is displayed from the first line of the base image.

PTSA0[8:0] – Sets the start line addresses of the RAM area, respectively for the partial image 1

PTEA0[8:0] – Sets the end display position of partial image 1.

PTSA1[8:0] – Sets the start line addresses of the RAM area, respectively for the partial image 2.

PTEA1[8:0] – Sets the end display position of partial image 2.

Panel Interface Control 1 (R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI[1:0]		RTNI[7:1]							0

RTNI[7:1] – Sets 1H (line) period. This setting is enabled while the LGDP4532's display operation is synchronized with internal clock. RTNI[7:0] should be greater than or equal to 120 (= 78h).

DIVI[1:0] – Sets the division ratio of the internal clock frequency. The LGDP4532's internal operation is synchronized with the frequency divided internal clock. When changing the DIVI[1:0] bits, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see "Frame-Frequency Adjustment Function". The setting in DIVI[1:0] is disabled in RGB interface operation.

Frame Frequency Calculation

Frame frequency = fosc/(clock cycles per line x division ratio x (active line + BP + FP))

Table 52 clocks per line (internal clock operation 1 clock = 1 OSC)

RTNI[7:0]	Clock per Line
8'h00 – 8'h76	Setting disabled
8'h78	120 clocks
8'h7A	122 clocks
8'h7C	124 clocks
8'h7E	126 clocks
…….	
8'hFC	252 clocks
8'hFE	254 clocks

Table 53 Division ratio of the internal clock

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

Panel Interface Control 2 (R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOWI[2:0]			0	0	0	0	EQI2[1:0]		EQI1[1:0]	

EQI1[1:0] – Sets equalization period.

Note : when VCOML >= 0V, EQI1,EQI2 setting is disabled.

Table 54

EQI1[1:0]	**Equalization period**
2'h0	0 (internal clock period see note)
2'h1	2
2'h2	4
2'h3	6

EQI2[1:0] – Sets equalization period.

Table 55

EQI2[1:0]	**Equalization period**
2'h0	0 (internal clock period see note)
2'h1	2
2'h2	4
2'h3	6

NOWI[2:0] – Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation in synchronization with internal clock.

Table 56

NOWI[2:0]	**Non-overlap period**
3'h0	0 (internal clock period see note)
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note : The internal clock is the frequency divided clock with the division ratio set with the DIVI[1:0] bits.

Panel Interface Control 3 (R93h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SEQI[2:0]			0	0	0	0	0	MCPI[2:0]		

MCPI[2:0] – Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation in synchronization with internal clock.

Table 57

MCPI[2:0]	Source output position
3'h0	0 (internal clock period [see note])
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note: The internal clock is the frequency divided clock with the division ratio set with the DIVI[[1:0] bits. The source output position is measured from a reference point by the number of internal clock cycle.

SEQI[2:0] – Sets Source equalization period.

Table 58

SEQI[2:0]	Source equalization periold
3'h0	0 (internal clock periold [see note])
3'h1	2
3'h2	4
3'h3	6
3'h4	8
3'h5	10
3'h6	12
3'h7	14

Panel Interface Control 4 (R95h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE[1:0]		RTNE[7:1]							0

RTNE[7:1] – Sets the number of internal clocks per 1H (line) period. Set the value that represents the number of DOTCLKs divided by the division ratio, which is input in a 1H period. RTNE[7:0] should be greater than or equal to 120 (= 78h).

DIVE[1:0] – Sets DIVE, the internal division ratio of DOTCLK. The internal operation is performed according to the clocks divided by the internal division ratio DIVE.

Table 59 Division ratio of DOTCLK

DIVE[1:0]	Division Ratio	Internal operation clock unit (DOTCLK)			
		18-bit, 1 transfer RGB interface	DOTCLK = 5 MHz	8-bit, 3 transfer RGB interface	DOTCLK = 15 MHz
2'h0	Setting disabled	Setting disabled	-	Setting disabled	-
2'h1	1/1	1 DOTCLKs	0.2 μs	3 DOTCLKs	0.2 μs
2'h2	1/2	2 DOTCLKs	0.4 μs	6 DOTCLKs	0.4 μs
2'h3	1/4	4 DOTCLKs	0.8 μs	12 DOTCLKs	0.8 μs

Table 60 DOTCLK per line (1H period)

RTNE[7:0]	DOTCLK per line (1H)
8'h00 – 8'h76	Setting disabled
8'h78	120 clocks
8'h7A	122 clocks
8'h7C	124 clocks
8'h7E	126 clocks
…….	
8'hFC	252 clocks
8'hFE	254 clocks

Panel Interface Control 5 (R97h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	NOWE[3:0]				0	0	0	0	EQE2[1:0]		EQE1[1:0]	

EQE1[1:0] – Sets equalization period.

Note : when VCOML >= 0V, EQE1,EQE2 setting is daiabled.

Table 61

EQE1[1:0]	Equalization period
2'h0	0 (internal clock period see note)
2'h1	2
2'h2	4
2'h3	6

EQE2[1:0] – Sets equalization period.

Table 62

EQE2[1:0]	Equalization period
2'h0	0 (internal clock period see note)
2'h1	2
2'h2	4
2'h3	6

NOWE[3:0] – Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

Table 63

NOWE[3:0]	Non-overlap period	NOWE[3:0]	Non-overlap period
4'h0	0 (internal clock period see note)	4'h8	32
4'h1	4	4'h9	36
4'h2	8	4'hA	40
4'h3	12	4'hB	44
4'h4	16	4'hC	48
4'h5	20	4'hD	52
4'h6	24	4'hE	56
4'h7	28	4'hF	60

Note : 1 clock = (Number of data transfers / pixel) x DIVE (division ratio) [DOTCLK].

Panel Interface Control 6 (R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2:0]		

MCPE[2:0] – Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation via RGB interface.

Table 64

MCPE[2:0]	Source output position
3'h0	0 (internal clock period see note)
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note : 1 clock = (Number of data transfers / pixel) x DIVE (division ratio) [DOTCLK].

SEQE[2:0] – Sets Source equalization period.

Table 65

SEQE[2:0]	Source equalization periold
3'h0	0 (internal clock periold see note)
3'h1	2
3'h2	4
3'h3	6
3'h4	8
3'h5	10
3'h6	12
3'h7	14

Test Register 1 (RA0h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	TDLY[1:0]		0	0	TMEM	TDFN	0	0	0	TOSC	0	0	TVCOM[1:0]	

TVCOM[1:0] – Sets the Vcom output level for test.

Table 66

TVCOM [1:0]	Vcom Level
2'h0	modulation
2'h1	modulation
2'h2	VCOML
2'h3	VCOMH

TOSC – Sets for the oscillator test.
TDFN – Sets for the function test.
TMEM – Sets for the memory test.
TDLY[1:0] – Sets for the delay time test.

Test Register 2 (RA1h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	REGULPD	0	0	0	TSAP	0	0	TSHZ	0	0	0	0	0

TSHZ – Sets
TSAP – Sets
REGULPD – Sets

Test Register 3 (RA2h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	T8CL	0	0	0	0	0	0	0	0	0	HaltVreg	MultiVci	

MultiVci – Used for Device Test.
HaltVreg – Used for Device Test.
T8CL – Used for 8 color mode test

Test Register 4 (RA3h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	RDSM[1:0]		0	0	WRPW[1:0]	

WRPW[1:0] – Used for memory write pulse width test.
RDSM[1:0] – Used for memory read sensing margin test.

Green Gamma Control 1-16 (RB0h to RBFh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				
W	1						PFP1[2:0]								PFP0[2:0]		
W	1						PFP3[2:0]								PFP2[2:0]		
W	1						PFN1[2:0]								PFN0[2:0]		
W	1						PFN3[2:0]								PFN2[2:0]		
W	1														PMP[2:0]		
W	1														PMN[2:0]		

PKP5-0[2 :0] – γ fine-adjustment register for positive polarity
PRP1-0[2 :0] – γ gradient-adjustment register for positive polarity
VRP0[3:0], R_VRP1[4 :0] – γ amplitude-adjustment register for positive polarity

PKN5-0[2 :0] – γ fine-adjustment register for negative polarity
PRN1-0[2 :0] – γ gradient-adjustment register for negative polarity
VRN0[3:0], VRN1[4 :0] – γ amplitude-adjustment register for negative polarity

PFP3-0[2:0] – γ fine adjustment register bits for positive polarity
PFN3-0[2:0] – γ fine adjustment register bits for negative polarity
PMP[2:0] – γ fine adjustment register bits for positive polarity
PMN[2:0] – γ fine adjustment register bits for negative polarity

Blue Gamma Control 1-16 (RC0h to RCFh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				
W	1						PFP1[2:0]								PFP0[2:0]		
W	1						PFP3[2:0]								PFP2[2:0]		
W	1						PFN1[2:0]								PFN0[2:0]		
W	1						PFN3[2:0]								PFN2[2:0]		
W	1														PMP[2:0]		
W	1														PMN[2:0]		

PKP5-0[2 :0] – γ fine-adjustment register for positive polarity
PRP1-0[2 :0] – γ gradient-adjustment register for positive polarity
VRP0[3:0], R_VRP1[4 :0] – γ amplitude-adjustment register for positive polarity

PKN5-0[2 :0] – γ fine-adjustment register for negative polarity
PRN1-0[2 :0] – γ gradient-adjustment register for negative polarity
VRN0[3:0], VRN1[4 :0] – γ amplitude-adjustment register for negative polarity

PFP3-0[2:0] – γ fine adjustment register bits for positive polarity
PFN3-0[2:0] – γ fine adjustment register bits for negative polarity
PMP[2:0] – γ fine adjustment register bits for positive polarity
PMN[2:0] – γ fine adjustment register bits for negative polarity

Note)
When BGR='1', these register setting vaules are for Red Gamma Control.

Instruction List

Index	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	Start oscillation																1
01h	Driver output control 1						SM (0)		SS (0)								
02h	LCD Driving Wave Control							BC0 (0)	EOR (0)			NW[5:0] (000000)					
03h	Entry mode	TRI (0)	DFM (0)		BGR (0)					ORG (0)		ID[1:0] (11)		AM (0)			
04h	Resizing Control							RCV[1:0] (00)				RCH[1:0] (00)				RSZ[1:0] (00)	
07h	Display Control 1			PTDE[1:0] (00)					BASEE (0)			GON (0)	DTE (0)	COL (0)		D[1:0] (00)	
08h	Display Control 2					FP[3:0] (1000)								BP[3:0] (1000)			
09h	Display Control 3						PTS[2:0] (000)					PTG[1:0] (00)		ISC[3:0] (0000)			
0Ah	Display Control 4													FMARKOE (0)	FMI[2:0] (000)		
0Ch	External display Interface Control 1			ENC[1:0] (000)					RM (0)			DM[1:0] (00)				RIM[1:0] (00)	
0Dh	Frame Marker Position								FMP[8:0] (000000000)								
0Fh	External display Interface Control 2												VSPL (0)	HSPL (0)		EPL (0)	DPL (0)
10h	Power Control 1		SAP[2:0] (000)				BT[2:0] (0000)				AP[2:0] (000)			DK (1)	DSTB (0)	SLP (0)	STBY (0)
11h	Power Control 2						DC1[2:0] (110)				DC0[2:0] (110)				VC[2:0] (000)		
12h	Power Control 3												PON (0)	VRH[3:0] (0000)			
13h	Power Control 4			VCOMG (0)	VDV[4:0] (00000)						VCM[6:0] (0000000)						
15h	Regulator Control		RSET[2:0] (000)				RI[2:0] (000)				RV[2:0] (011)				RCONT (000)		
16h	Gamma Select Control								SGE (0)				EN_MA (0)				PS (0)
20h	RAM Address Set (Horizontal Address)									AD[7:0] (00000000)							
21h	RAM Address Set (Vertical Address)								AD[16:8] (000000000)								
22h	RAM Data	WD[17:0] or RD[17:0]															
30h	Red Gamma Control 1						PKP1[2:0] (000)								PKP0[2:0] (000)		
31h	Red Gamma Control 2						PKP3[2:0] (000)								PKP2[2:0] (000)		
32h	Red Gamma Control 3						PKP5[2:0] (000)								PKP4[2:0] (000)		
33h	Red Gamma Control 4						PRP1[2:0] (000)								PRP0[2:0] (000)		
34h	Red Gamma Control 5						PKN1[2:0] (000)								PKN0[2:0] (000)		
35h	Red Gamma Control 6						PKN3[2:0] (000)								PKN2[2:0] (000)		
36h	Red Gamma Control 7						PKN5[2:0] (000)								PKN4[2:0] (000)		
37h	Red Gamma Control 8						PRN1[2:0] (000)								PRN0[2:0] (000)		
38h	Red Gamma Control 9				VRP1[4:0] (00000)								VRP0[4:0] (00000)				
39h	Red Gamma Control 10				VRN1[4:0] (00000)								VRN0[4:0] (00000)				
3Ah	Red Gamma Control 11						PFP1[2:0] (001)								PFP0[2:0] (001)		
3Bh	Red Gamma Control 12						PFP3[2:0] (001)								PFP2[2:0] (001)		
3Ch	Red Gamma Control 13						PFN1[2:0] (001)								PFN0[2:0] (001)		
3Dh	Red Gamma Control 14						PFN3[2:0] (001)								PFN2[2:0] (001)		
3Eh	Red Gamma Control 15														PMP[2:0] (001)		
3Fh	Red Gamma Control 16														PMN[2:0] (001)		

40h	EPROM Control 1	PTM[1:0] (00)		POR (0)	VPP (0)	PPROG (0)	PWE (0)	PA[1:0] (00)		PDIN[7:0] (00000000)									
41h	EPROM Control 2												AUTOWR (0)	RA[1:0] (00)		VCMSEL[1:0] (00)			
42h	EPROM Control 3									PDOUT[7:0] (11111111)									
50h	Window Horizontal RAM Start Address									HSA[7:0] (00000000)									
51h	Window Horizontal RAM End Address									HEA[7:0] (11101111)									
52h	Window Vertical RAM Start Address									VSA[8:0] (000000000)									
53h	Window Vertical RAM End Address									VEA[8:0] (100111111)									
60h	Driver Output Control 2	GS (0)		NL[5:0] (000000)								SCN[5:0] (000000)							
61h	Base Image Display Control														NDL (0)	VLE (0)	REV (0)		
6Ah	Vertical Scroll Control								VL[8:0] (000000000)										
80h	Partial Image 1 Display Position								PTDP0[8:0] (000000000)										
81h	Partial Image 1 RAM Start Line Address								PTSA0[8:0] (000000000)										
82h	Partial Image 1 RAM End Line Address								PTEA0[8:0] (000000000)										
83h	Partial Image 2 Display Position								PTDP1[8:0] (000000000)										
84h	Partial Image 2 RAM Start Line Address								PTSA1[8:0] (000000000)										
85h	Partial Image 2 RAM End Line Address								PTEA1[8:0] (000000000)										
90h	Panel Interface Control 1							DIVI[1:0] (00)		RTNI[7:0] (01111000)									
92h	Panel Interface Control 2						NOWI[2:0] (000)							EQI2[1:0] (00)		EQI1[1:0] (00)			
93h	Panel Interface Control 3						SEQI[2:0] (000)								MCPI[2:0] (000)				
95h	Panel Interface Control 4							DIVE[1:0] (00)		RTNE[7:0] (01111000)									
97h	Panel Interface Control 5					NOWE[3:0] (0000)								EQE2[1:0] (00)		EQE1[1:0] (00)			
98h	Panel Interface Control 6						SEQE[2:0] (000)								MCPE[2:0] (000)				
A0h	Test register 1			TDLY (00)				TMEM (0)	TDFN (0)				TOSC (0)			TVCOM[1:0] (00)			
A1h	Test register 2				REGULPD (0)				TSAP (0)			TSHZ (0)							
A2h	Test register 3				T8CL (0)										HaltVreg (0)	MultiVci (1)			
A3h	Test register 4											RDSM (00)				WRPW (00)			
B0h	Green Gamma Control 1						PKP1[2:0] (000)								PKP0[2:0] (000)				
B1h	Green Gamma Control 2						PKP3[2:0] (000)								PKP2[2:0] (000)				
B2h	Green Gamma Control 3						PKP5[2:0] (000)								PKP4[2:0] (000)				
B3h	Green Gamma Control 4						PRP1[2:0] (000)								PRP0[2:0] (000)				
B4h	Green Gamma Control 5						PKN1[2:0] (000)								PKN0[2:0] (000)				
B5h	Green Gamma Control 6						PKN3[2:0] (000)								PKN2[2:0] (000)				
B6h	Green Gamma Control 7						PKN5[2:0] (000)								PKN4[2:0] (000)				
B7h	Green Gamma Control 8						PRN1[2:0] (000)								PRN0[2:0] (000)				
B8h	Green Gamma Control 9				VRP1[4:0] (00000)								VRP0[4:0] (00000)						
B9h	Green Gamma Control 10				VRN1[4:0] (00000)								VRN0[4:0] (00000)						
BAh	Green Gamma Control 11						PFP1[2:0] (001)								PFP0[2:0] (001)				

BBh	Green Gamma Control 12						PFP3[2:0] (001)								PFP2[2:0] (001)
BCh	Green Gamma Control 13						PFN1[2:0] (001)								PFN0[2:0] (001)
BDh	Green Gamma Control 14						PFN3[2:0] (001)								PFN2[2:0] (001)
BEh	Green Gamma Control 15														PMP[2:0] (001)
BFh	Green Gamma Control 16														PMN[2:0] (001)
C0h	Blue Gamma Control 1						PKP1[2:0] (000)								PKP0[2:0] (000)
C1h	Blue Gamma Control 2						PKP3[2:0] (000)								PKP2[2:0] (000)
C2h	Blue Gamma Control 3						PKP5[2:0] (000)								PKP4[2:0] (000)
C3h	Blue Gamma Control 4						PRP1[2:0] (000)								PRP0[2:0] (000)
C4h	Blue Gamma Control 5						PKN1[2:0] (000)								PKN0[2:0] (000)
C5h	Blue Gamma Control 6						PKN3[2:0] (000)								PKN2[2:0] (000)
C6h	Blue Gamma Control 7						PKN5[2:0] (000)								PKN4[2:0] (000)
C7h	Blue Gamma Control 8						PRN1[2:0] (000)								PRN0[2:0] (000)
C8h	Blue Gamma Control 9				VRP1[4:0] (00000)								VRP0[4:0] (00000)		
C9h	Blue Gamma Control 10				VRN1[4:0] (00000)								VRN0[4:0] (00000)		
CAh	Blue Gamma Control 11						PFP1[2:0] (001)								PFP0[2:0] (001)
CBh	Blue Gamma Control 12						PFP3[2:0] (001)								PFP2[2:0] (001)
CCh	Blue Gamma Control 13						PFN1[2:0] (001)								PFN0[2:0] (001)
CDh	Blue Gamma Control 14						PFN3[2:0] (001)								PFN2[2:0] (001)
CEh	Blue Gamma Control 15														PMP[2:0] (001)
CFh	Blue Gamma Control 16														PMN[2:0] (001)

Reset Function

The LGDP4532 is initialized with a RESET input. During a reset period, the LGDP4532 is in a busy state and neither instruction nor access to the GRAM data from the MPU is accepted. The LGDP4532's internal power supply circuit unit is initialized also with a RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, neither access to the internal GRAM nor initial setting of instruction bits is accepted.

1. Initial state of instruction bits (default)
See the instruction list. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization
The RAM data is not automatically initialized with a RESET input and must be initialized by software in a display-off period (D1-0 = "00").

3. Output pin initial state *See note

1. LCD driver S1~S720	: GND
G1~G320 : VGL (= GND)	
2. Vcom	: GND
3. VcomDC	: GND
4. VRS	: GND
5. VCS	: GND
6. VREG1OUT	: VGS
7. VciOUT	: Hi-z
8. VLOUT1	: Vci
9. VLOUT2	: DDVDH (= Vci)
10. VLOUT3	: GND
11. FMARK	: GND
12. Oscillator	: Oscillate
13. SDO	: GND

4. Initial state of input/output pins*See note

1. C11+	: Hi-z
2. C11-	: Hi-z
3. C12+	: Hi-z
4. C12-	: Hi-z
5. C13+	: Vci1
6. C13-	: GND
7. C21+	: DDVDH (= Vci)
8. C21-	: GND
9. C22+	: DDVDH (= Vci)
10. C22-	: GND
11. C23+	: DDVDH (= Vci)
12. C23-	: GND
13. VDD	: VDD

Note: The above-mentioned initial states of output and input pins are the ones when the LGDP4532's power supply circuit is connected as exemplified in "Wiring example".

5. Note on Reset function

(1) When a RESET input is entered into the LGDP4532 while it is in deep standby mode, the LGDP4532 starts up the inside logic regulator and makes a transition to the initial state. During this period, the interface pins may be under an unstable condition. For this reason, do not enter a RESET input in deep standby mode.

(2) When transferring instruction using either two or three transfer mode via 8-/9-/16-bit interface, make sure to execute a data transfer synchronization after executing a reset operation.

Basic Mode operation of the LGDP4532

The basic operation modes of the LGDP4532 are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

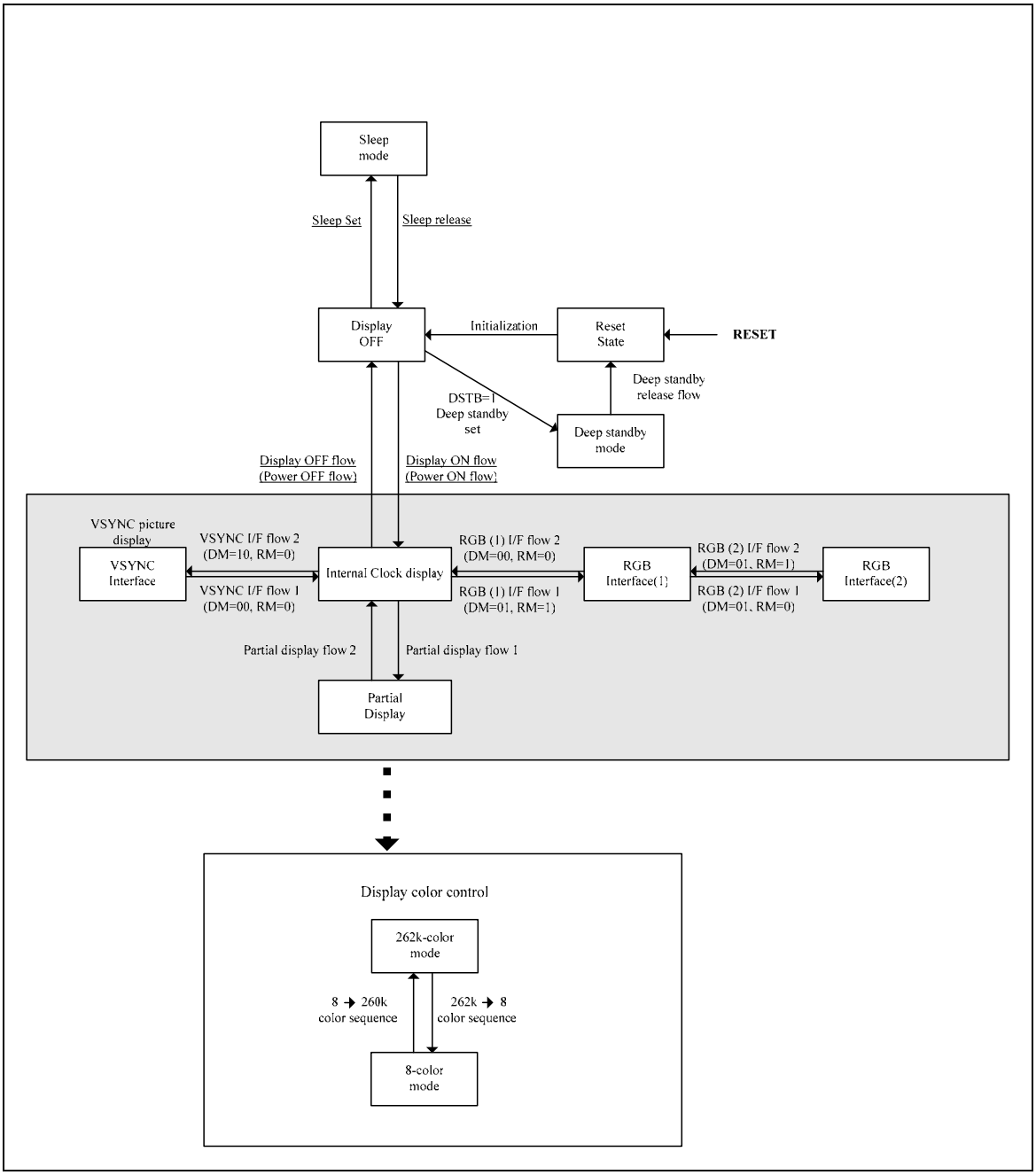


Figure 14

Interface and data format

The LGDP4532 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The LGDP4532 allows selecting an optimum interface according to the kind of display (moving or still picture) in order to transfer data efficiently.

As external display interface, the LGDP4532 supports RGB interface and VSYNC interface, both enabling data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the LGDP4532 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the LGDP4532's GRAM in order to minimize the data transfer by transferring data only when it is necessary to switch the moving picture frames. The window address function specifies the RAM area where data is rewritten for moving picture display and enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display using system interface by writing data to the GRAM at more than a certain speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in speed and methods of writing data to the internal RAM.

The LGDP4532 can operate in either one of the following four modes according to the state of display. The display operation mode is determined by setting the external interface control register. When switching between different modes, make sure to refer to mode switching sequence.

Table 67

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Notes:
1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM[1:0]) while RGB interface is in operation.
4. See the "External Display Interface" section for the mode transition sequence.

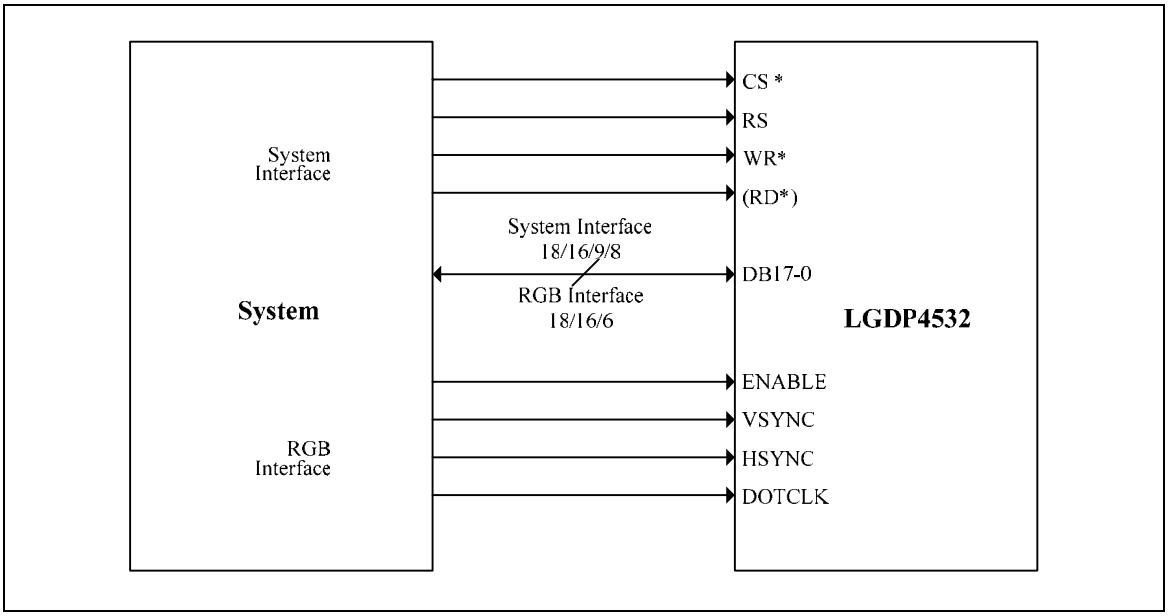


Figure 15 LGDP4532's Interface

Internal clock operation
The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. Any input via external display interface is invalid in this operation. The internal RAM is accessible only via system interface.

RGB interface operation (1)
The display operation is synchronized with the frame synchronous signal (VSYNC), the line synchronous signal (HSYNC), and the dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied throughout the display period using RGB interface.
The LGDP4532 transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function enables the LGDP4532 to display a moving picture and the data in other than the moving picture RAM area simultaneously and transferring only data to be overwritten in the moving picture RAM area when7 rewriting the moving picture RAM area. This structure can minimize the total number of data transfer.
The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the LGDP4532 by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with these settings.

RGB interface operation (2)
This mode enables the LGDP4532 to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first and then set a new address and the index register to R22h.

VSYNC interface operation
The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the LGDP4532 to display a moving picture using system interface by writing data to the internal RAM at more than a minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are constraints in speed and methods of writing RAM data. For details, see the "VSYNC Interface" section. As an external input, only VSYNC signal input is valid in this mode. Any other input via external display interface is invalid.
The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) according to the register settings inside the LGDP4532.

System Interface

The following are the kinds of system interfaces available with the LGDP4532. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 68

IM[3:0]	Interface Mode with MPU	DB pins	Colors
0000	Setting disabled	-	-
0001	Setting disabled	-	-
0010	80-system 16-bit interface	DB17-10, DB8-1	262,144 *see Note 1
0011	80-system 8-bit interface	DB17-10	262,144 *see Note 2
010*	Clock synchronous serial interface	SDI,SDO	65,536
0110	Setting disabled	-	-
0111	Setting disabled	-	-
1000	Setting disabled	-	-
1001	Setting disabled	-	-
1010	80-system 18-bit interface	DB17-0	262,144
1011	80-system 9-bit interface	DB17-9	262,144
1100	Setting disabled	-	-
1101	Setting disabled	-	-
1110	Setting disabled	-	-
1111	Setting disabled	-	-

Notes: 1. 65,536 colors in 16-bit signal transfer mode.
2. 65,536 colors in 8-bit 2-transfer mode.

80-system 18-bit Bus Interface

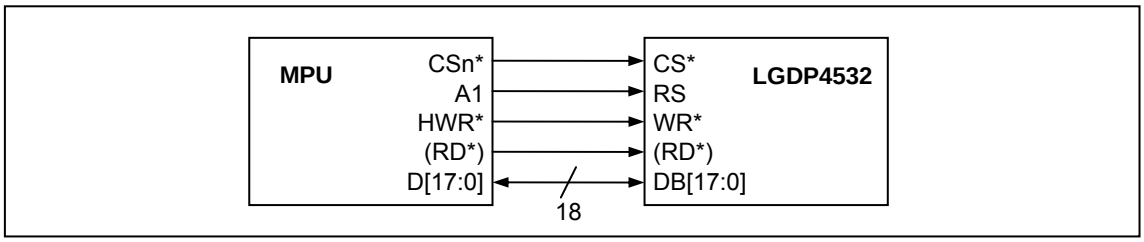


Figure 16 18-bit Interface

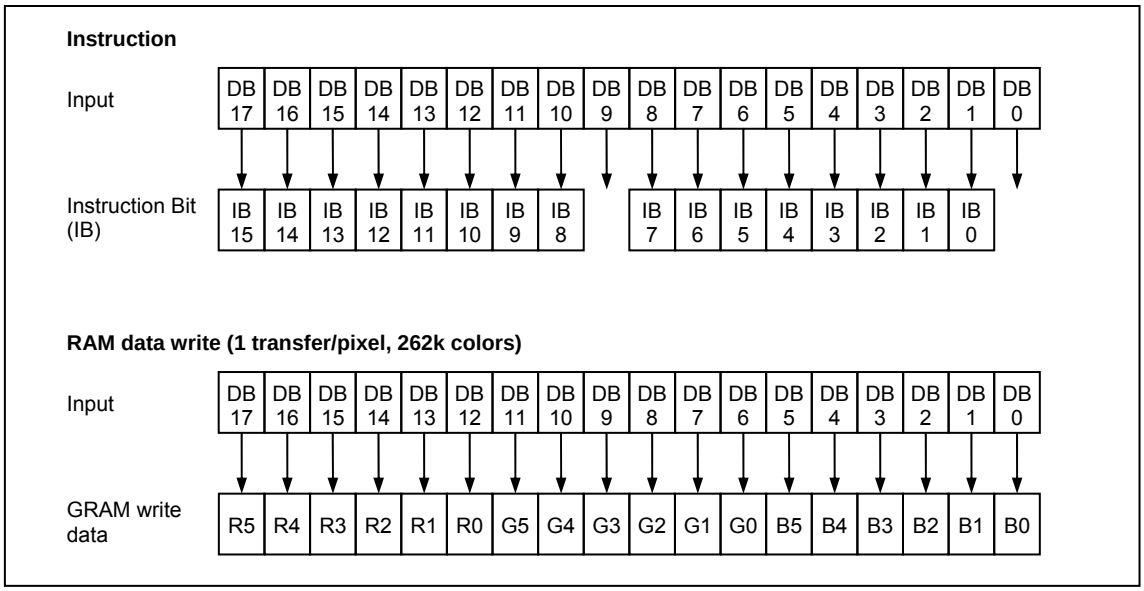


Figure 17 Data format for 18-bit interface

80-system 16-bit Bus Interface

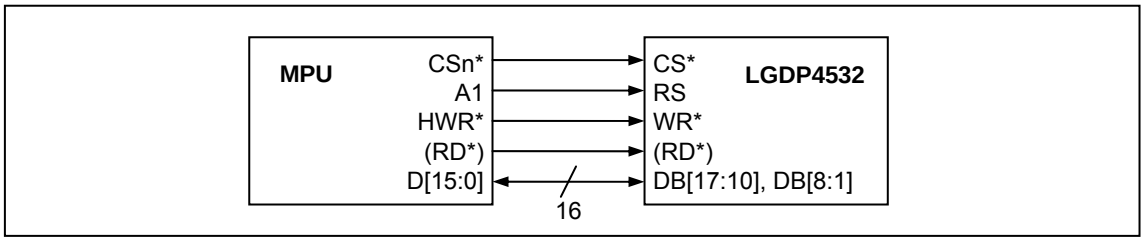


Figure 18 16-bit Interface

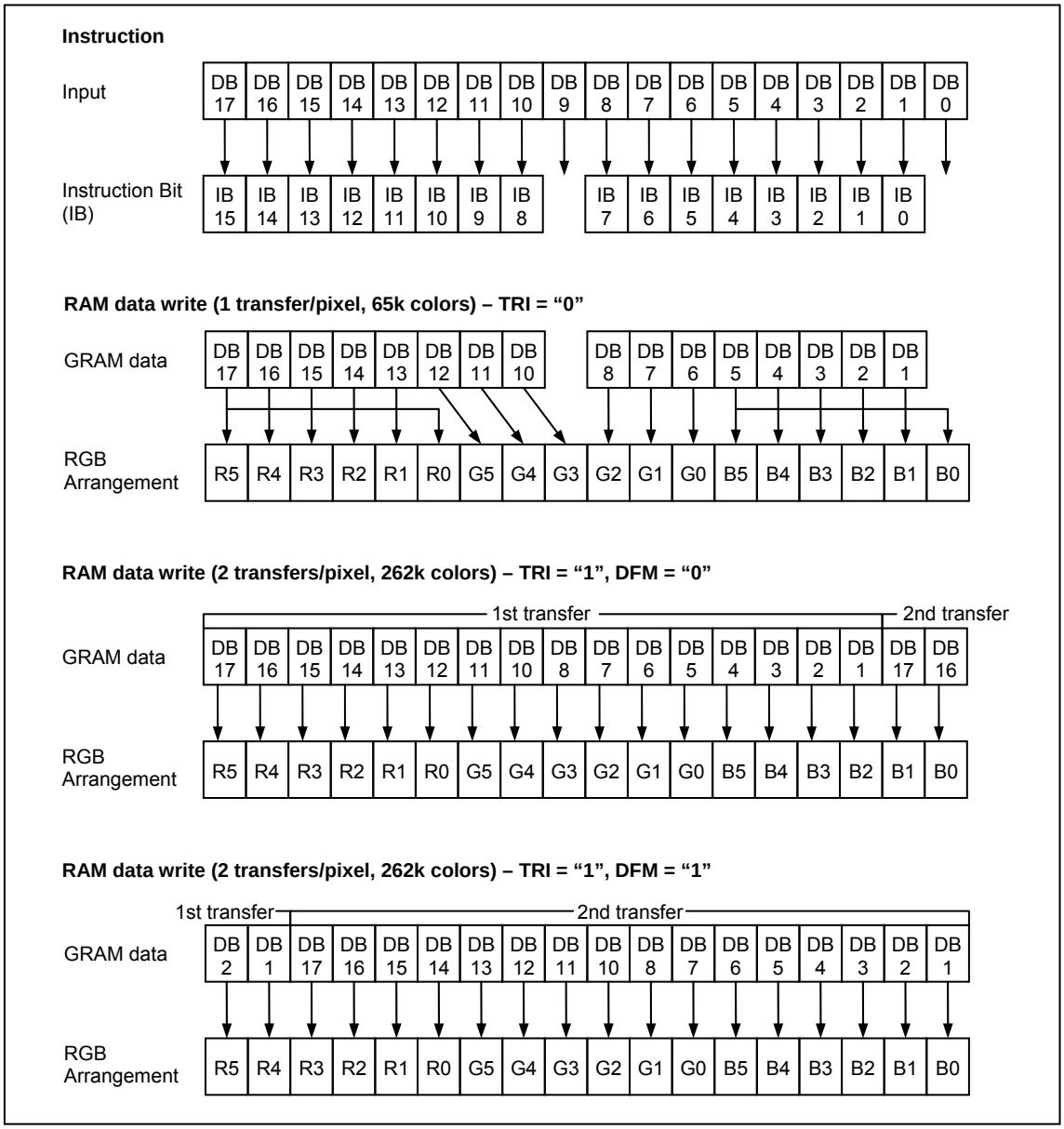


Figure 19 Data format for 16-bit interface

Data Transfer Synchronous in 16-bit Bus Interface operation

The LGDP4532 supports a data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 2/16 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

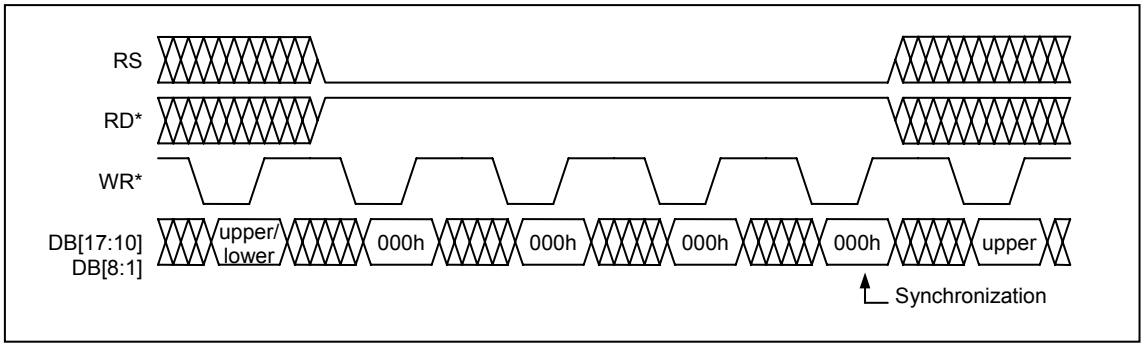


Figure 20 16-bit Data Transfer Synchronization

80-system 9-bit Bus Interface

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into the upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either the IOVcc or IOGND level. When writing to the index register, the upper byte (8 bits) must be written.

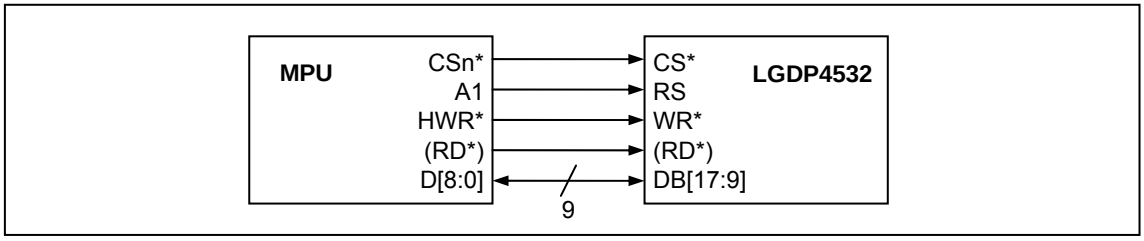


Figure 21 9-bit Intreface

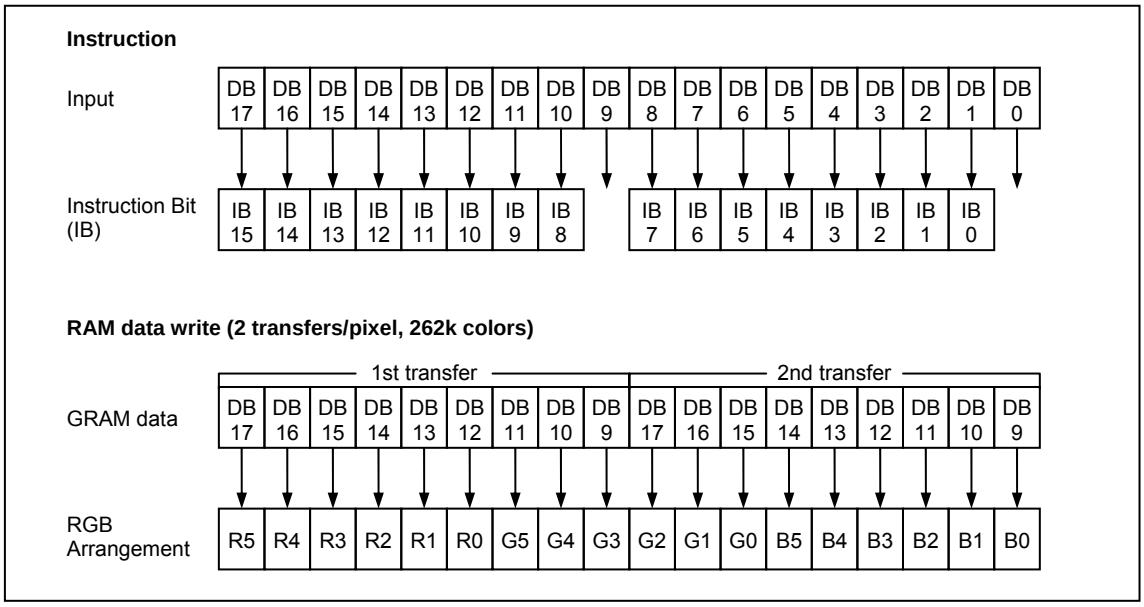


Figure 22 9-bit Intreface Data Format

Data Transfer Synchronous in 9-bit Bus Interface operation

The LGDP4532 supports a data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 9 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

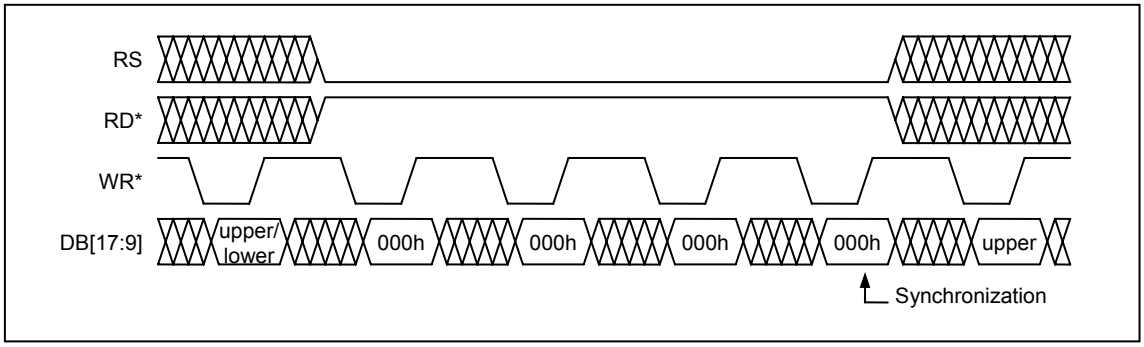


Figure 23 9-bit Data Transfer Synchronization

80-system 8-bit Bus Interface

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either the IOVcc or IOGND level. When writing the index register, the upper byte (8 bits) must be written.

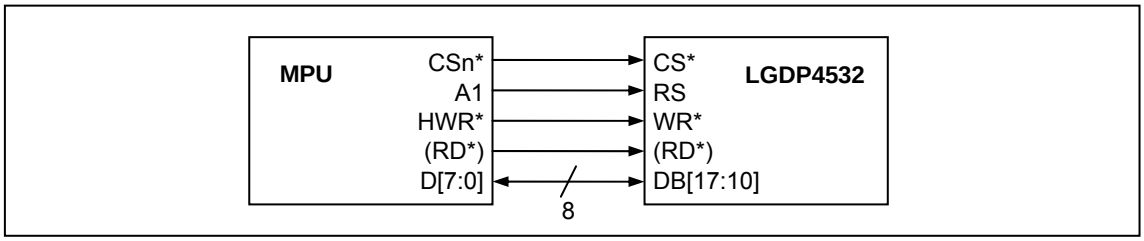


Figure 24 8-bit Interface

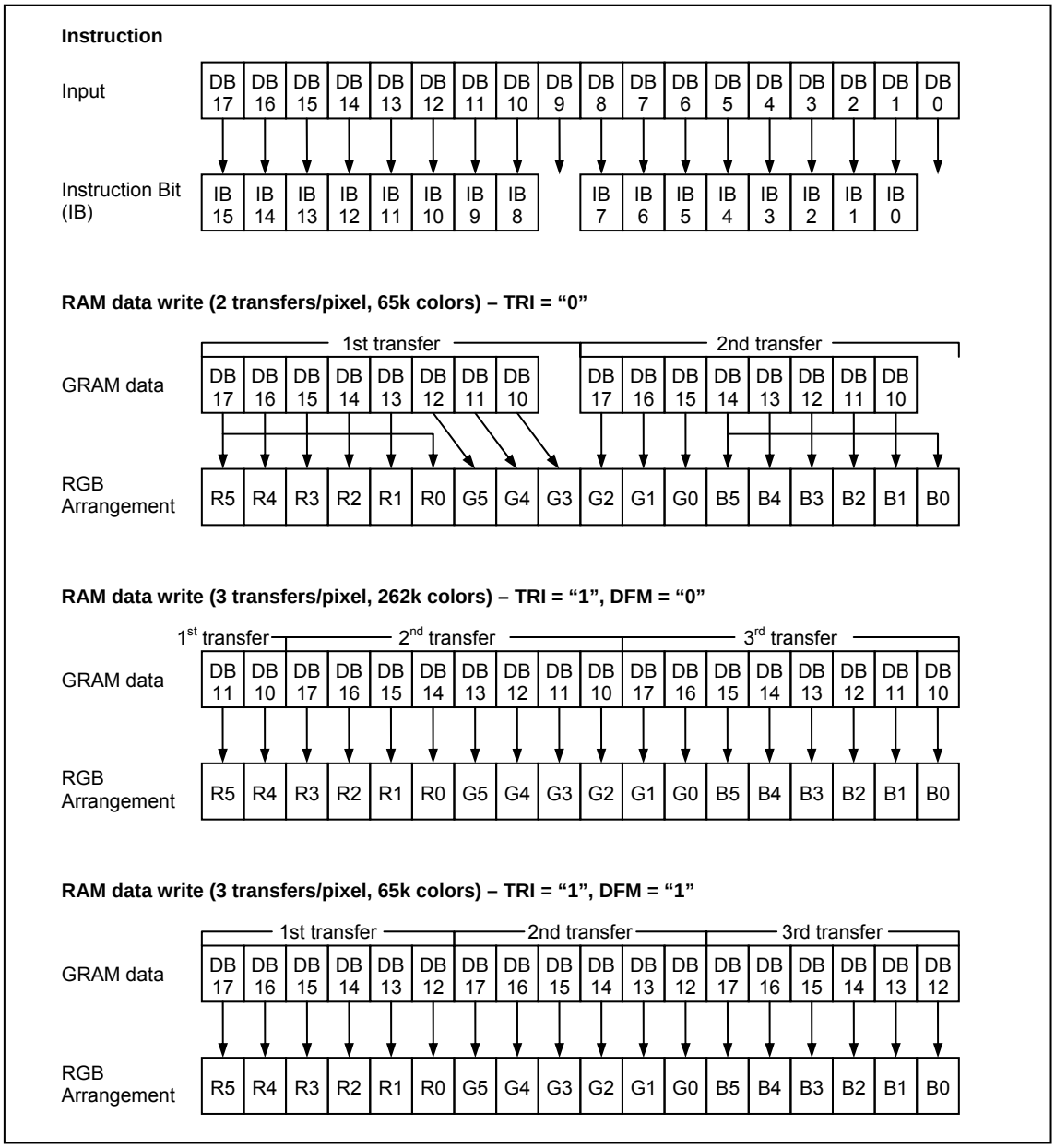


Figure 25 8-bit Intreface Data Format

Data Transfer Synchronous in 8-bit Bus Interface operation

The LGDP4532 supports a data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 8 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

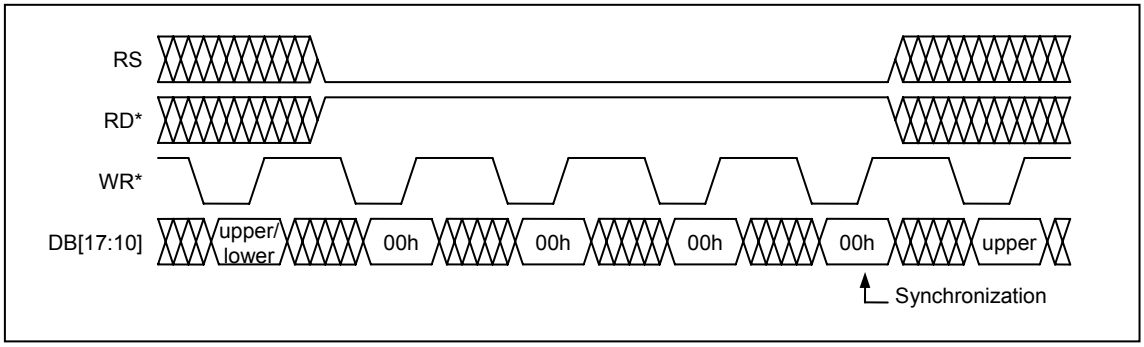


Figure 26 8-bit Data Transfer Synchronization

Serial Interface

The serial interface is selected by setting the IM3/2/1 pins to the IOGND/IOVcc/IOGND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The LGDP4532 recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The LGDP4532 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LGDP4532 are compared and both 6-bit data match, and then the LGDP4532 starts taking in data. The least significant bit of the device identification code is set with the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the LGDP4532 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, an index register write operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). The LGDP4532 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The LGDP4532 writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the LGDP4532 starts transferring or receiving data in units of bytes. The LGDP4532 executes data transfer from the MSB. The LGDP4532's instruction takes 16-bit format and they are executed inside after it is transferred in two bytes (16 bits: DB15-0) from the MSB (The LGDP4532 expands RAM write data into 18-bit format when writing them to the internal GRAM). The first byte received by the LGDP4532 following the start byte is always the upper eight bits of instruction and the second byte is the lower 8 bits of instruction.

In case of reading data from the GRAM, the LGDP4532 does not transfer valid data until first five bytes of data are read from the GRAM following the start byte. The LGDP4532 starts sending valid data as it reads the sixth and subsequent byte data.

Table 69 Start byte format

Transferred bits	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

Note: ID bit is selected by setting the IM0/ID pin.

Table 70

RS	**R/W**	**Function**
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

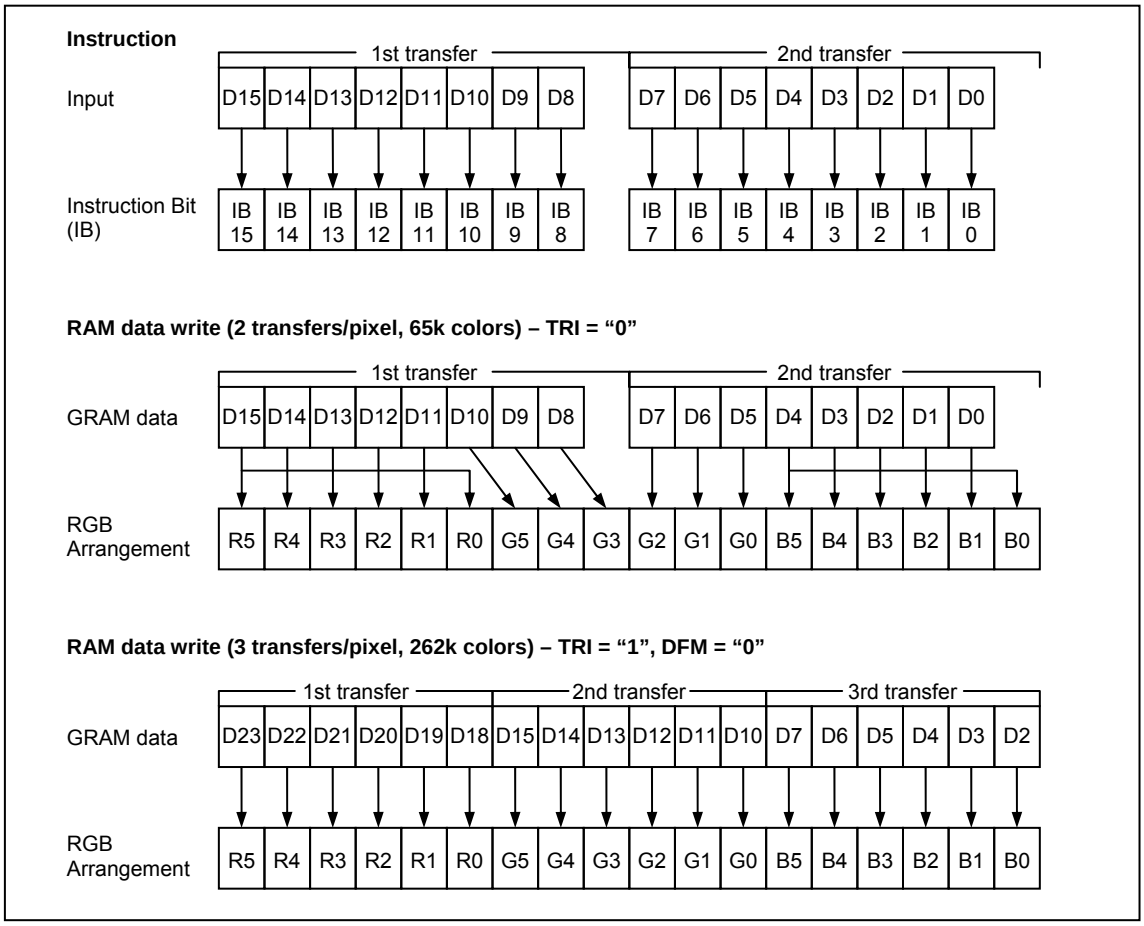


Figure 27 Data format for SPI

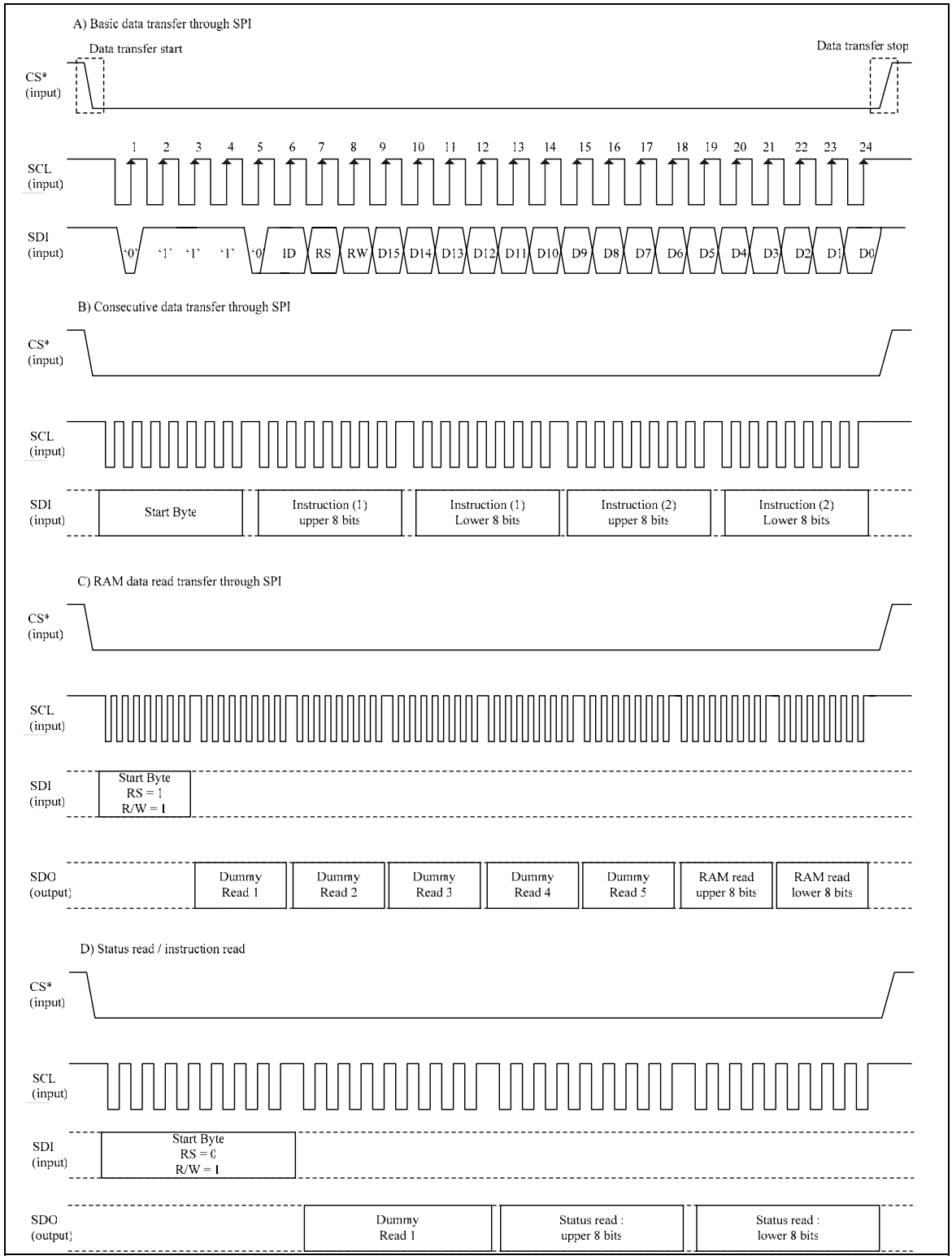


Figure 28 Data Transfer in Serial interface

VSYNC Interface

The LGDP4532 supports VSYNC interface, enabling the LGDP4532 to display a moving picture with minimum modifications to the existing system, using system interface and the frame synchronization signal (VSYNC).

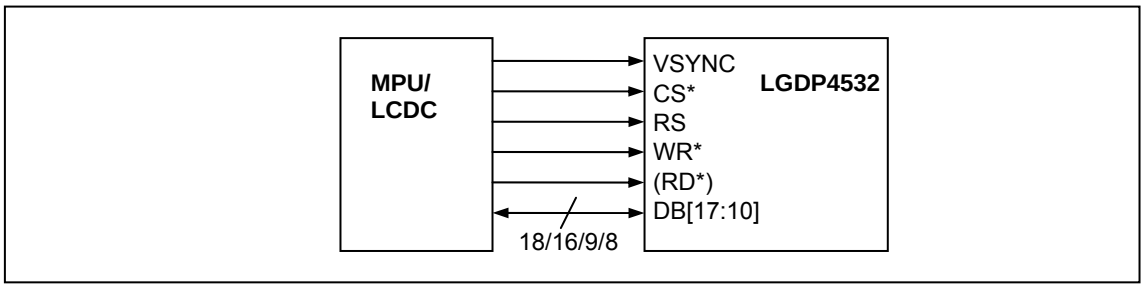


Figure 29 VSYNC Interface

The VSYNC interface is selected by setting DM[1:0] = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at a speed faster to a certain degree than the internal display operation speed, it becomes possible to rewrite data without flickering the moving picture on display and enables the LGDP4532 to display a moving picture using a system interface.

The LGDP4532 performs the display operation with the internal clock signal generated from the internal oscillator and the VSYNC signal in this mode. In VSYNC mode, the data displayed on the screen are written to the internal RAM in order to transfer only the data to be written over the moving picture RAM area and thereby minimize the total data transfer required for moving picture display.

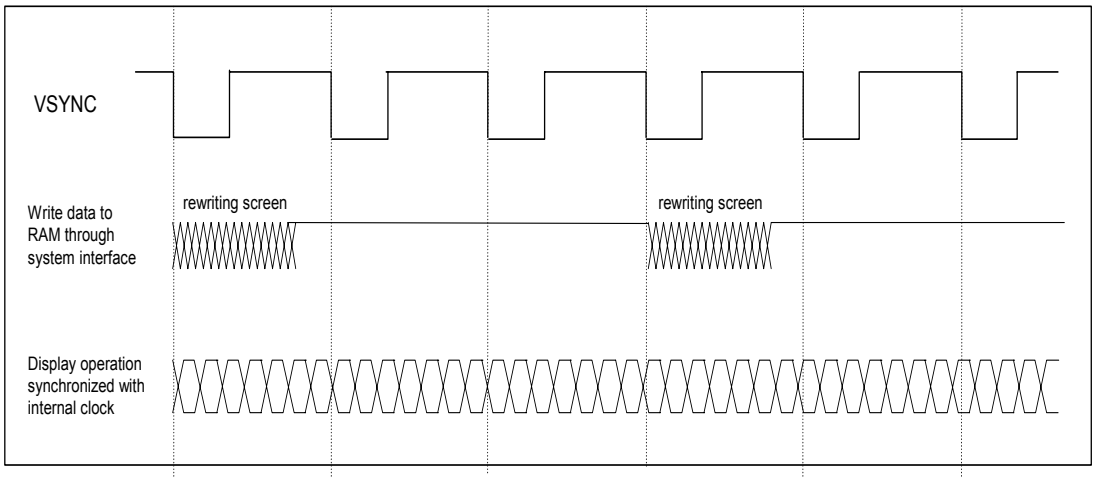


Figure 30 Moving Picture Data Transfers via VSYNC Interfce

The VSYNC interface has the minimum speed of writing data to the internal RAM via the system interface and the minimum internal clock frequency, which are calculated from the following formulae.

Internal clock frequency (fosc) [Hz]
= FrameFrequency × (DisplayLines (NL) + FrontPorch (FP) + BackPorch (BP)) × 64 clocks × variance

$$RAMWriteSpeed > \frac{240 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 64\ clocks \times \frac{1}{fosc}}$$

Note: When the RAM write operation does not start on the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum RAM writing speed and internal clock frequency in VSYNC interface mode is as follows.

[Example]

Display size	240 RGB × 320 lines
Lines	320 lines
Back/front porch	14/2 lines (BP = 1110/FP = 0010)
Frame frequency	60 Hz

Internal clock frequency (fosc)
= 60 Hz × (320 + 2 + 14) lines × 64 Clocks × 1.1 / 0.9 = 1.6 MHz

When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±10% for variances and ensures to complete the display operation within one VSYNC cycle.

In this example, variances attributed to the fabrication process of LSI and room temperature are counted in. Other possible causes of variances, such as differences in external resistors or voltage changes are not in consideration. It is necessary to allow for an enough margin if these factors must be incorporated.

Minimum speed for RAM writing
240 × 320 / {((14 + 320 - 2) lines × 64 clock) / 1.6 MHz} = 5.7 MHz

The above theoretical value is calculated on the premise that the LGDP4532 starts writing data to the internal RAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line where display operation is performed and the RAM line address where data write operation is performed.

The RAM write speed of 5.7MHz or more on the falling edge of VSYNC will guarantee the completion of RAM write operation before the LGDP4532 starts displaying the RAM data on the screen, enabling rewriting the entire screen without flicker.

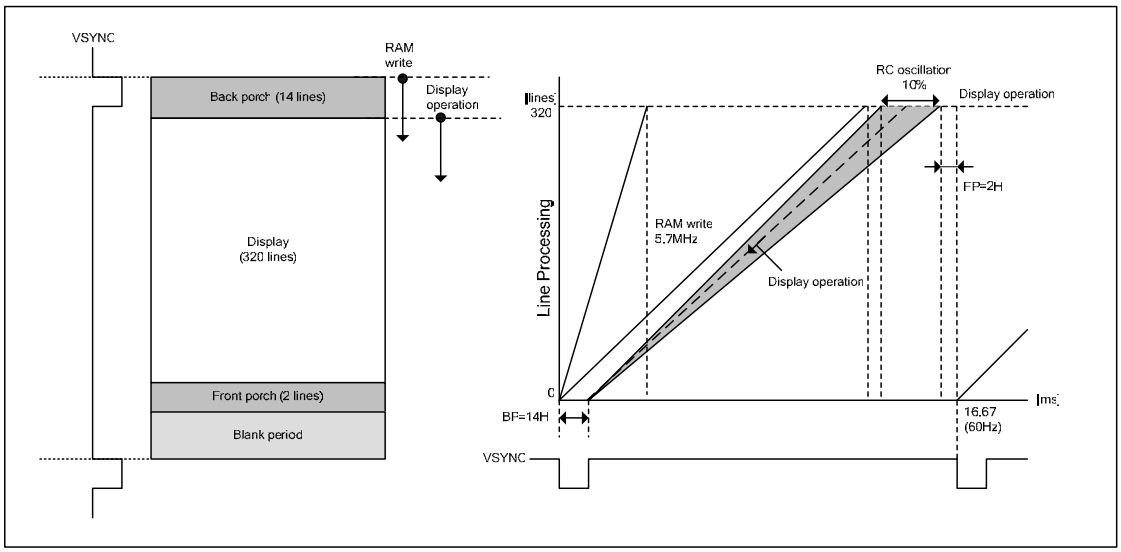


Figure 31 Write/Display Operation Timing via VSYNC Interface

Notes in using the VSYNC interface

1. The above example of calculation gives a theoretical value. In the actual setting, other possible causes of variances not counted in the above example such as differences in internal oscillators should also be taken into consideration. It is strongly recommended to allow for an enough margin in setting a RAM writing speed.

2. The above example of calculation gives a minimum value in case of rewriting the entire screen. If the moving picture display area is smaller than that, the range for setting a minimum RAM writing speed can have extra margins.

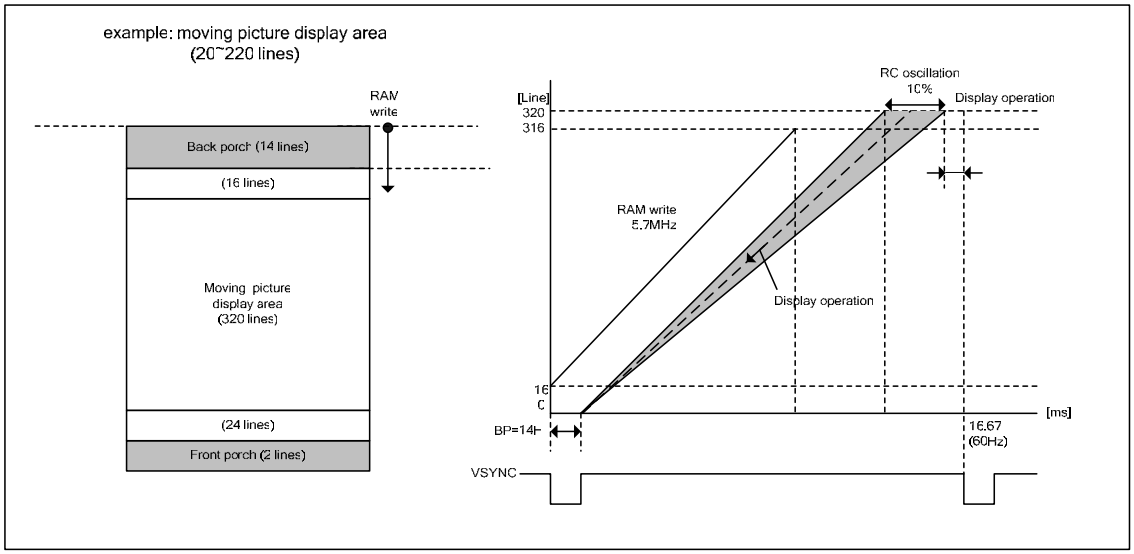


Figure 32 RAM write margin

3. After drawing 1 frame, a front porch period continues until the next input of VSYNC is detected.

4. When switching from the internal clock operation mode (DM1-0 = “00”) to the VSYNC interface mode, or the other way around, it is enabled from the next VSYNC cycle, i.e. after completing the display of the frame, which the LGDP4532 was internally processing when switching the modes.

5. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

6. In VSYNC interface mode, set the AM bit to “0” to transfer display data in the method mentioned above.

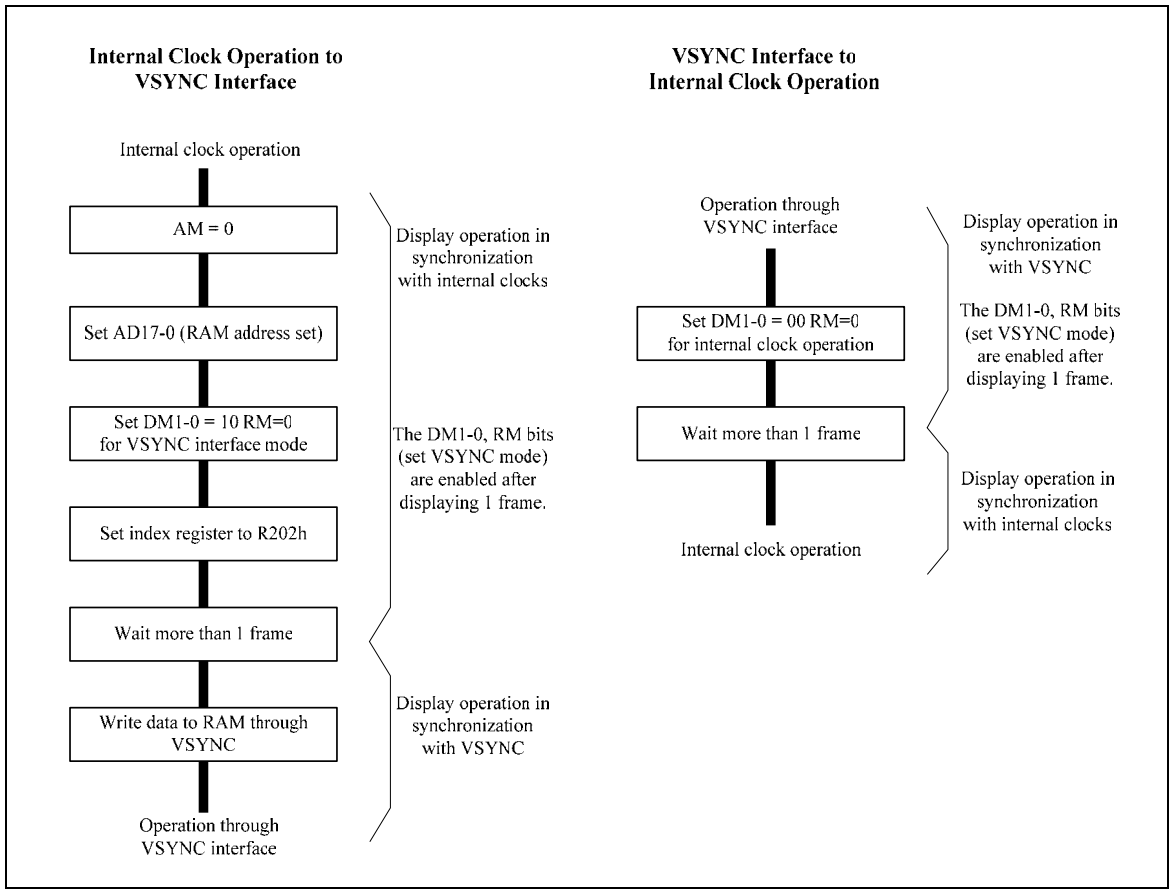


Figure 33 Sequences to Switch between VSYNC and Internal Clock Operation Modes

External Display Interface

The following RGB interfaces are available with the LGDP4532. The interface operation is set with the RIM[1:0] bits. The RGB interface is used for RAM access.

Table 71

RIM[1:0]	RGB Interface	DB Pin
00	18-bit RGB interface	DB[17:0]
01	16-bit RGB interface	DB[17:10], DB[8:1]
10	6-bit RGB interface	DB[17:12]
11	Setting disabled	-

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface in combination with the window address function enables minimizing data transfer by rewriting data in high-speed with low power consumption only within the RAM area where data must be updated. In RGB interface operation, it is necessary to set back and front porch periods before and after the display period, respectively.

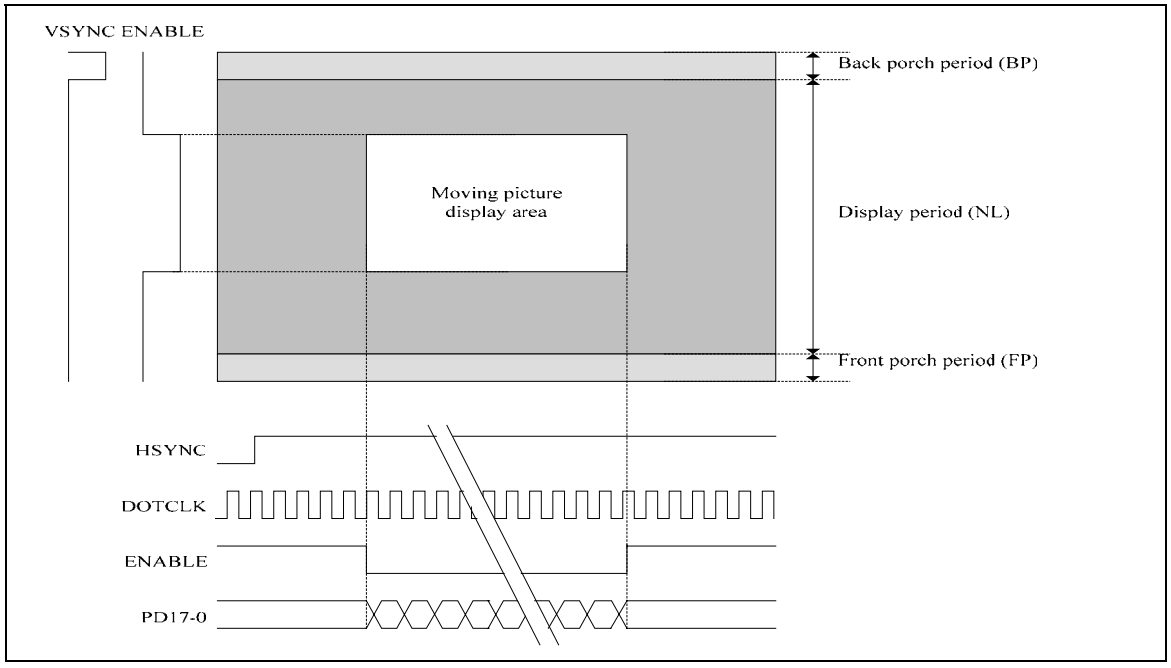


Figure 34 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals are changeable by setting the DPL, EPL, HSPL, and VSPL bits, respectively according to the system configuration.

RGB Interface Timing

The timing relationships of signals in RGB interface operation area as follows.

16-18-bit RGB Interface Timing

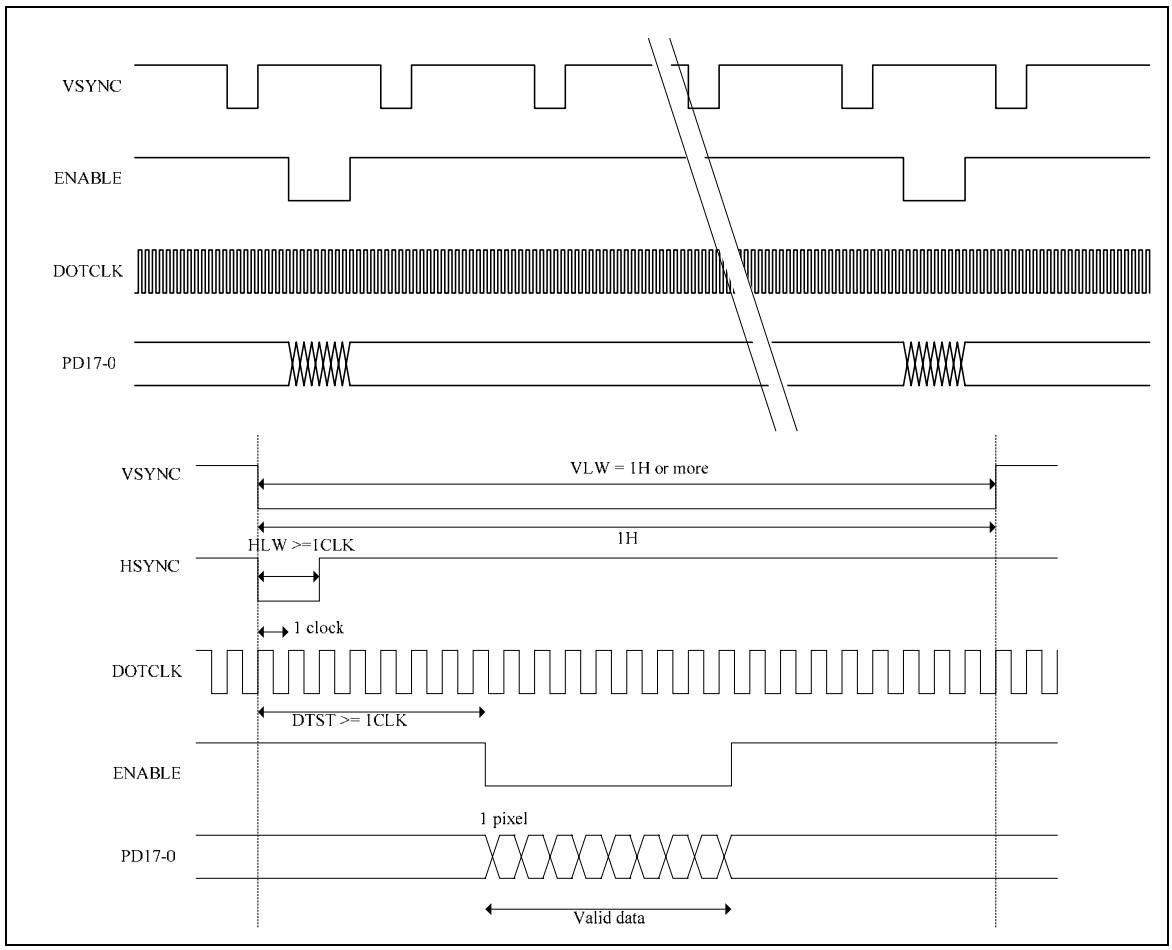


Figure 35

Notes: 1. VLW : VSYNC Low period
HLW : HSYNC Low period
DTST : data transfer setup time

6-bit RGB Interface Timing

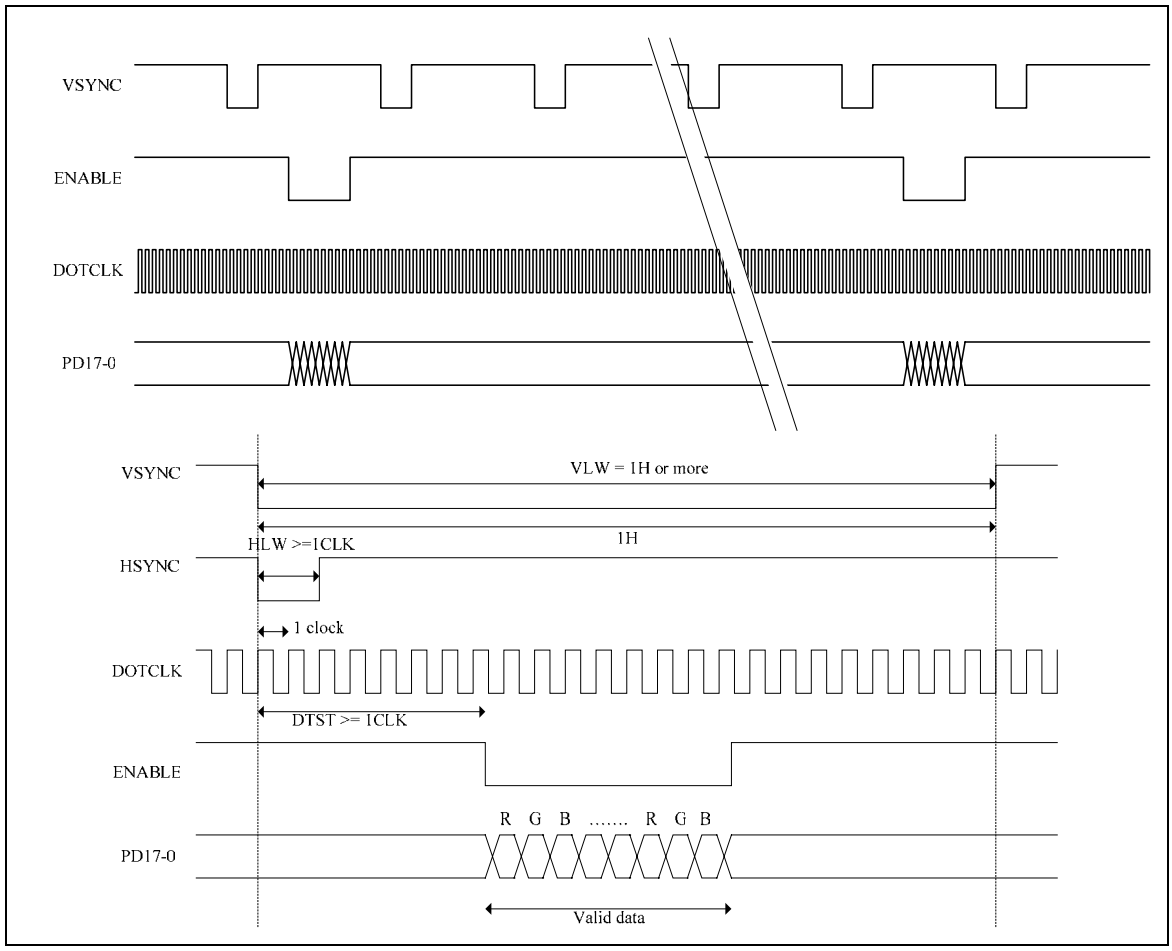


Figure 36

Notes: 1. VLW : VSYNC Low period
HLW : HSYNC Low period
DTST : Data transfer setup time
2. In 6-bit RGB interface operation, set the cycles of VSYNC, HSYNC, ENABLE, DOTCLK so that one pixel is transferred in units of three DOTCLKs via DB17-12 (DB5-0).

Moving Picture Display with the RGB Interface

The LGDP4532 supports RGB interfaces for displaying a moving picture and RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function can minimize data transfer by specifying a moving picture RAM area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. The data transfer is limited to a moving picture RAM area.
4. The reduction in data transfer contributes to the reduction in power consumption by the entire system
5. The combined use with system interface allows updating data in the still picture area, such as icons, while displaying a moving picture via RGB interface

RAM access via system interface in RGB interface operation

The LGDP4532 allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the RAM via system interface, set ENABLE "High" to stop writing data via RGB interface. Then set RM = "0" to enable RAM access via system interface. When reverting to the RGB interface operation, wait for a time for a read/write bus cycle. Then, set RM = "1" and the index register to R22h to start accessing RAM via RGB interface. A conflict between RAM accesses via two different interfaces will not guarantee write operation.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

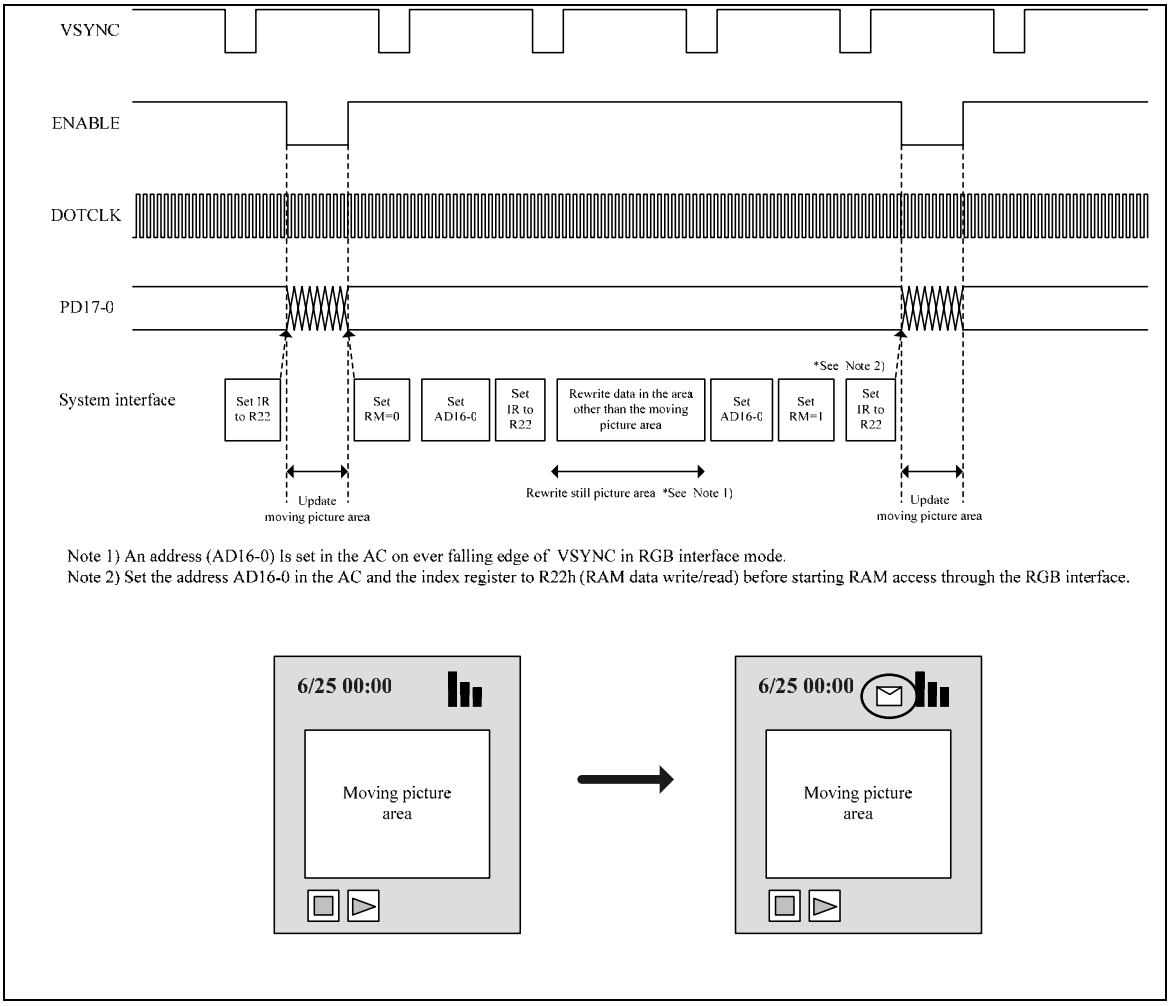


Figure 37 Updating the Still Picture Area while Displaying Moving Picture

6-bit RGB Interface

The 6-bit RGB interface is selected by setting RIM[1:0] = 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus according to data enable signal (ENABLE). Unused pins DB[11:0] must be fixed at either IOVcc or IOGND level.

The instructions are set only via system interface.

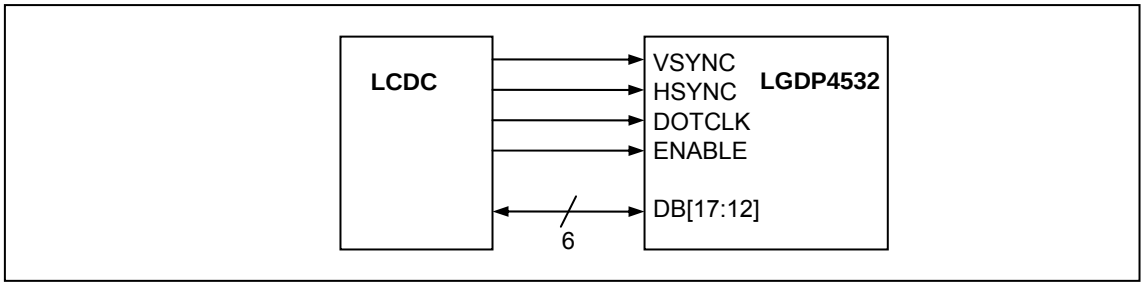


Figure 38 6-bit RGB interface

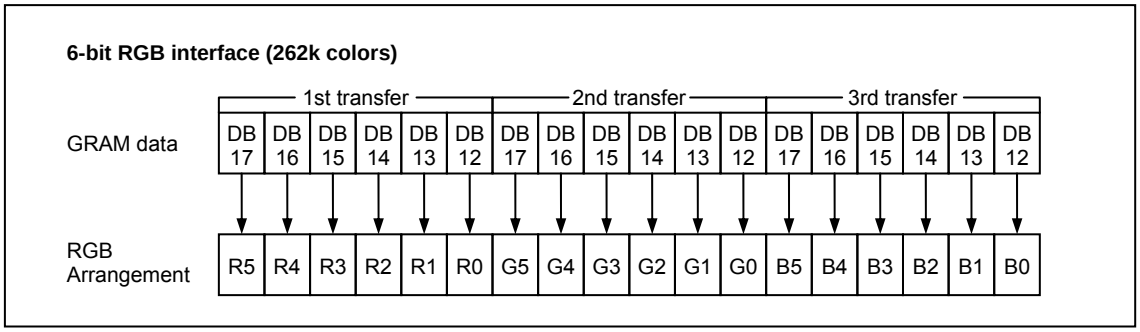


Figure 39 Data format for 6-bit interface

Data Transfer Synchronization in 6-bit Bus Interface operation

The LGDP4532 has data transfer counters to count the first, second, and third 6-bit data transfers in 6-bit RBG interface operation. The transfer counters are always reset to the first data transfer on the falling edge of VSYNC. If there is a mismatch in the number of data transfers, the counters are reset to the first data transfer at the start of each frame (on the falling edge of VSYNC) and data transfer can be restarted in correct order from the next frame. In case of displaying a moving picture, which requires consecutive data transfer, this function can minimize the effect from the data transfer mismatch and help recover the display system to a normal state.

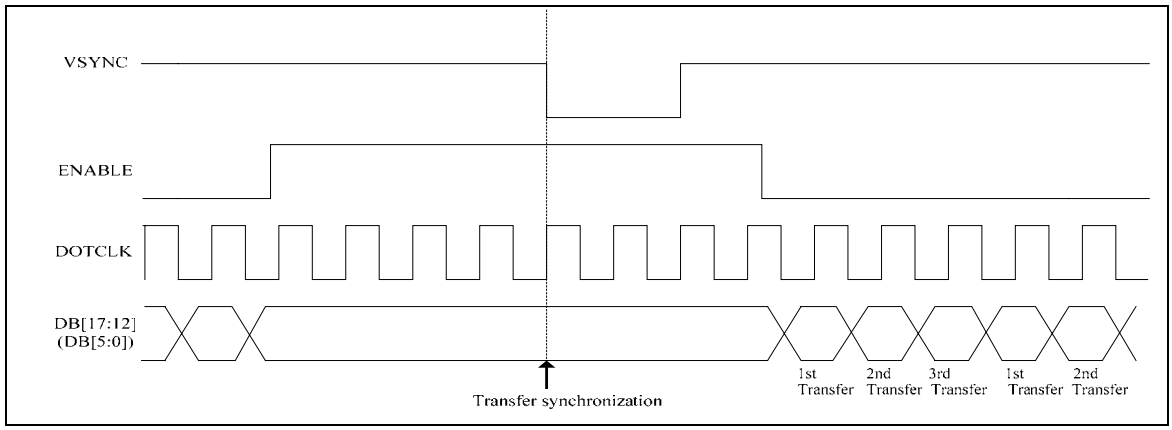


Figure 40 6-bit Transfer Synchronization

16-bit RGB Interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus according to data enable signal (ENABLE).

The instructions are set only via system interface.

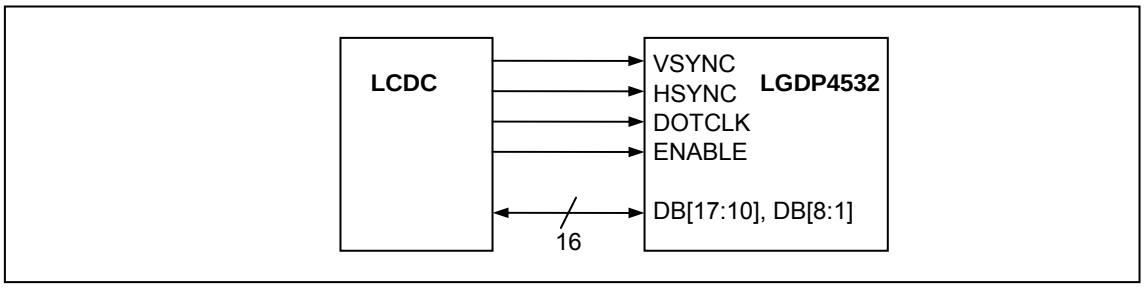


Figure 41 16-bit RGB interface

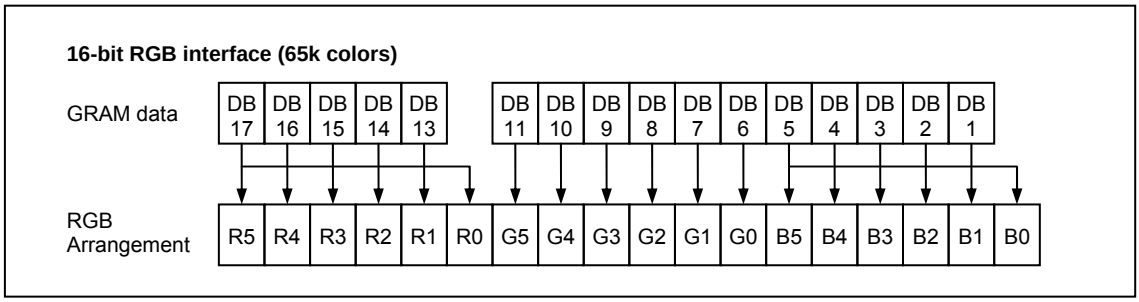


Figure 42 Data format for 16-bit interface

18-bit RGB Interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB17-0) according to data enable signal (ENABLE).

The instructions are set only via system interface.

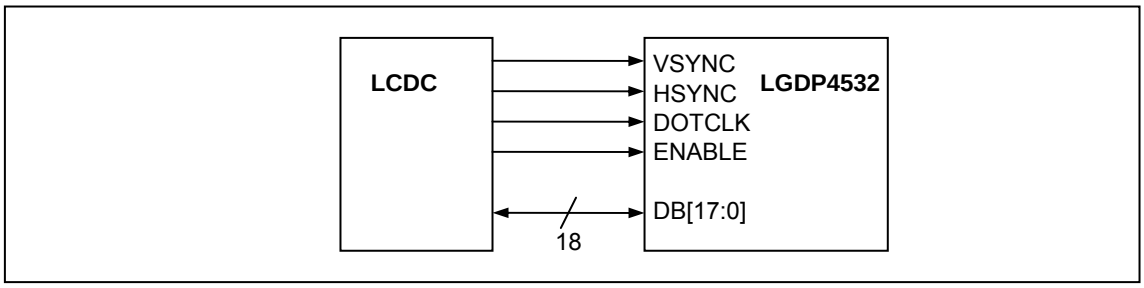


Figure 43 18-bit RGB interface

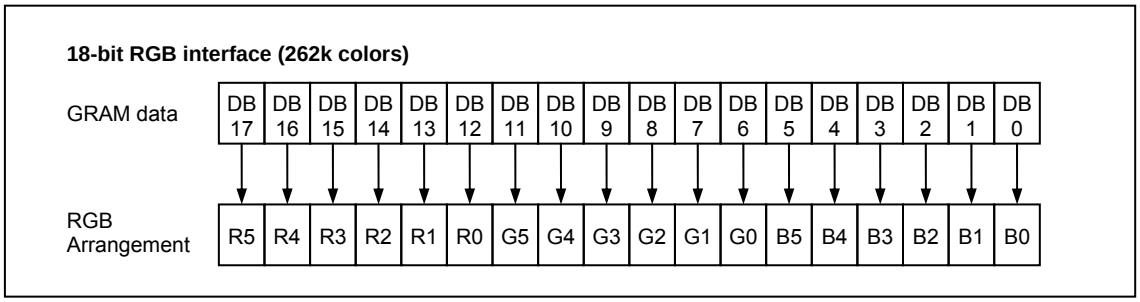


Figure 44 Data format for 18-bit interface

Notes on Using the External Display Interface

1. The following functions are not available in external display interface operation.

Table 72 Functions Not Available in External Display Interface operation

Fucntion	External Display Interface	Internal Display Interface
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied throughout the display operation.

3. The reference clock for generating liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.

4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel.

5. In 6-bit RGB interface operation, each 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. Take this into consideration and make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE, and data transfer via DB17-12 so that data transfer is completed in units of pixels.

6. When switching between the internal operation mode and the external display interface operation, follow the sequences in Figure 43 RGB and Internal Clock Operation Mode switching sequences.

7. In RGB interface operation, a front porch period continues until the next VSYNC input is detected after the end of each frame period.

8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to the internal RAM.

9. In RGB interface operation, RAM address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

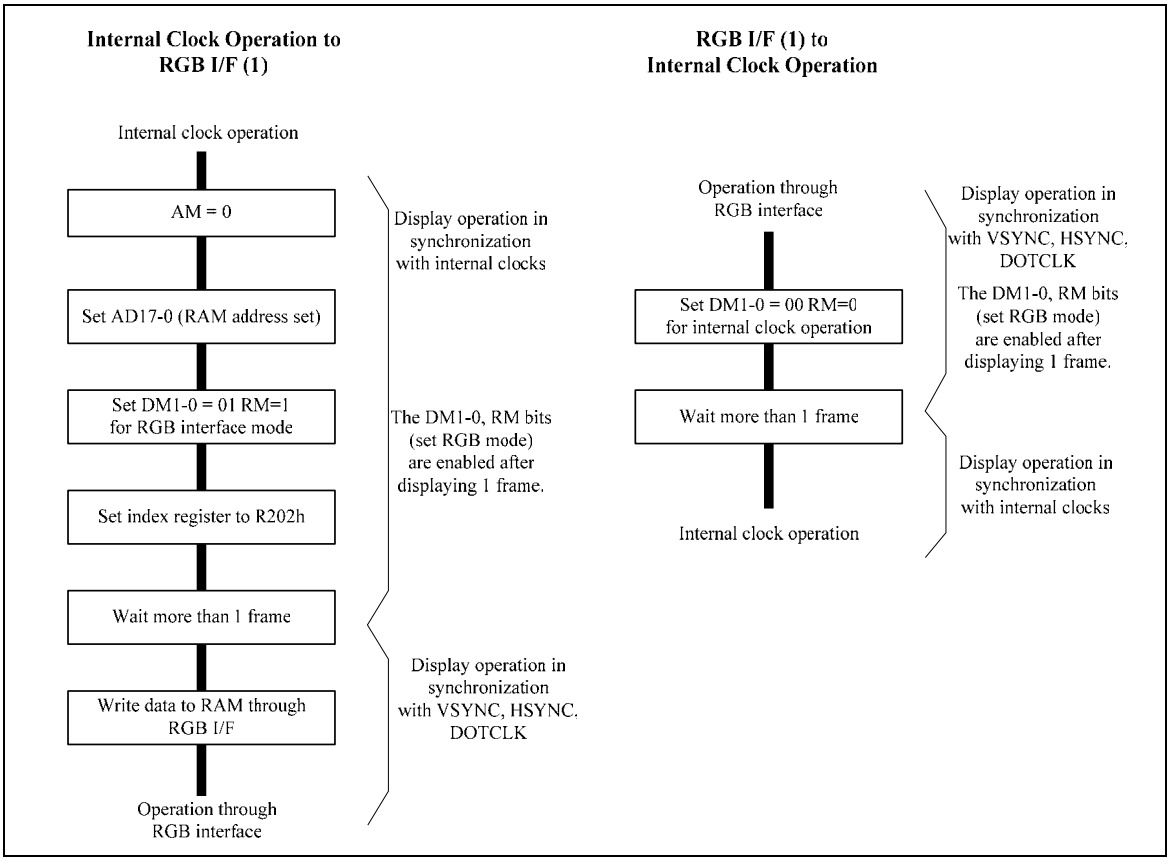


Figure 45 RGB and Internal Clock Operation Mode switching sequences

RAM Address and Display Position on the Panel

The LGDP4532 has memory to store display data of 240RGB x 320 lines. The LGDP4532 incorporates a circuit to control partial display, which enables switching driving methods for full-screen display and partial display.

The LGDP4532 allows separate settings for display control and driving position control and specifying a RAM area for each image displayed on the screen. This structure enables designing a display on the screen not constrained by the mounting position of the display panel.

The following is the sequence of settings for full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image with PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, the register setting in SS bit is required when writing RAM data.

Table 73

	Display ENABLE	**Numbers of Lines**	**RAM area**
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h13F)

Notes : 1: The base image is displayed from the first line of the screen.
2: Make sure NL ≤ 320 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h13F, respectively.

Table 74

	Display ENABLE	**Display position**	**RAM start position**
Partial image 1	PTDE0	(PTDP0, PTEA0)	PTSA0
Partial image 2	PTDE1	(PTDP1, PTEA1)	PTSA1

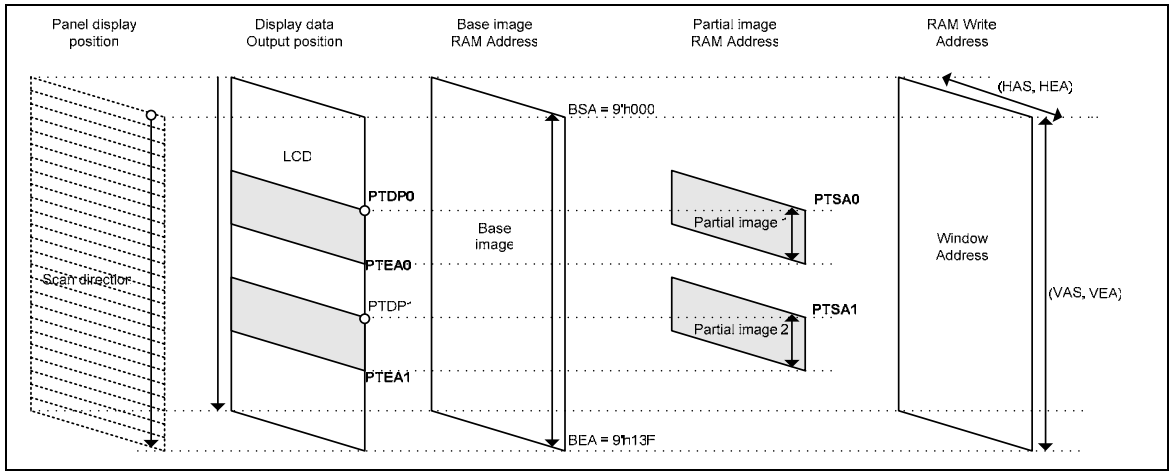


Figure 46 RAM Address, display position and drive position

Restrictions in setting display control instruction

The following are the constraints in setting coordinates of display data, display position, and partial image display.

Screen setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is within the limit: NL ≤ 320 lines

Base image display

1. The base image is displayed from the first line of the screen: BSA = 1st line (of the display panel)

2. The base image RAM area specified with BSA, BEA must include the same or more number of lines necessary to drive the liquid crystal panel (NL setting): BEA - BSA ≥ NL

Partial image display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partials do not overlap each other.

$0 \leq PTDP0 \leq PTEA0 <$
$PTDP1 \leq PTEA1 \leq NL$

The following figure shows the relationship among the RAM address, display position, and driving positions of the panel.

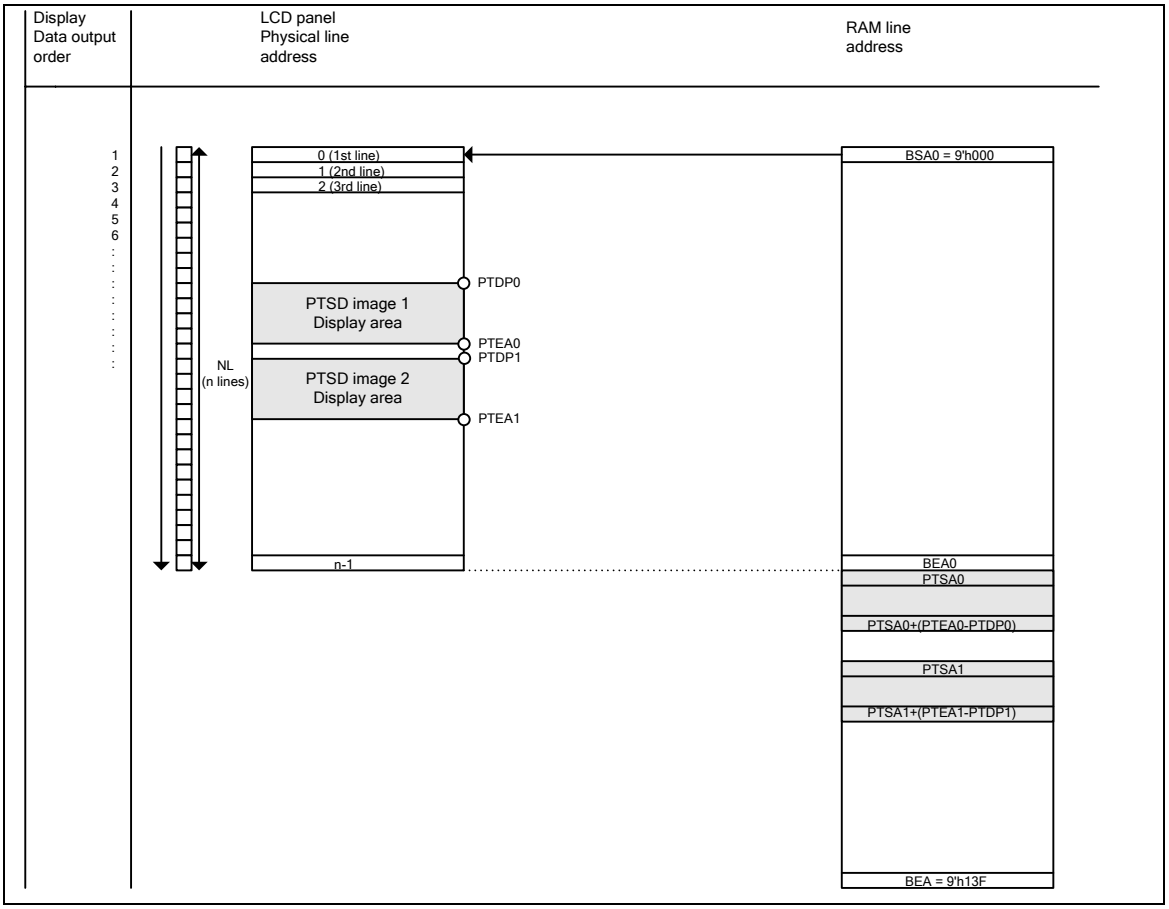


Figure 47 Display RAM Address and display position

Note: In this figure, the RAM address is defined in relation to the display position on the panel. Inside the LGDP4532, the RAM address area where the data is written is defined within a window address area on the GRAM address mapping.

Instruction setting example

The followings are the examples of settings for 240(RGB) x 320(lines) panels.

1. Full screen display (no partial)

The following is an example of setting for full screen display.

Table 75

Base image display insruction	
BASEE	1
NL[5:0]	6’h27
PTDE0	0
PTDE1	0

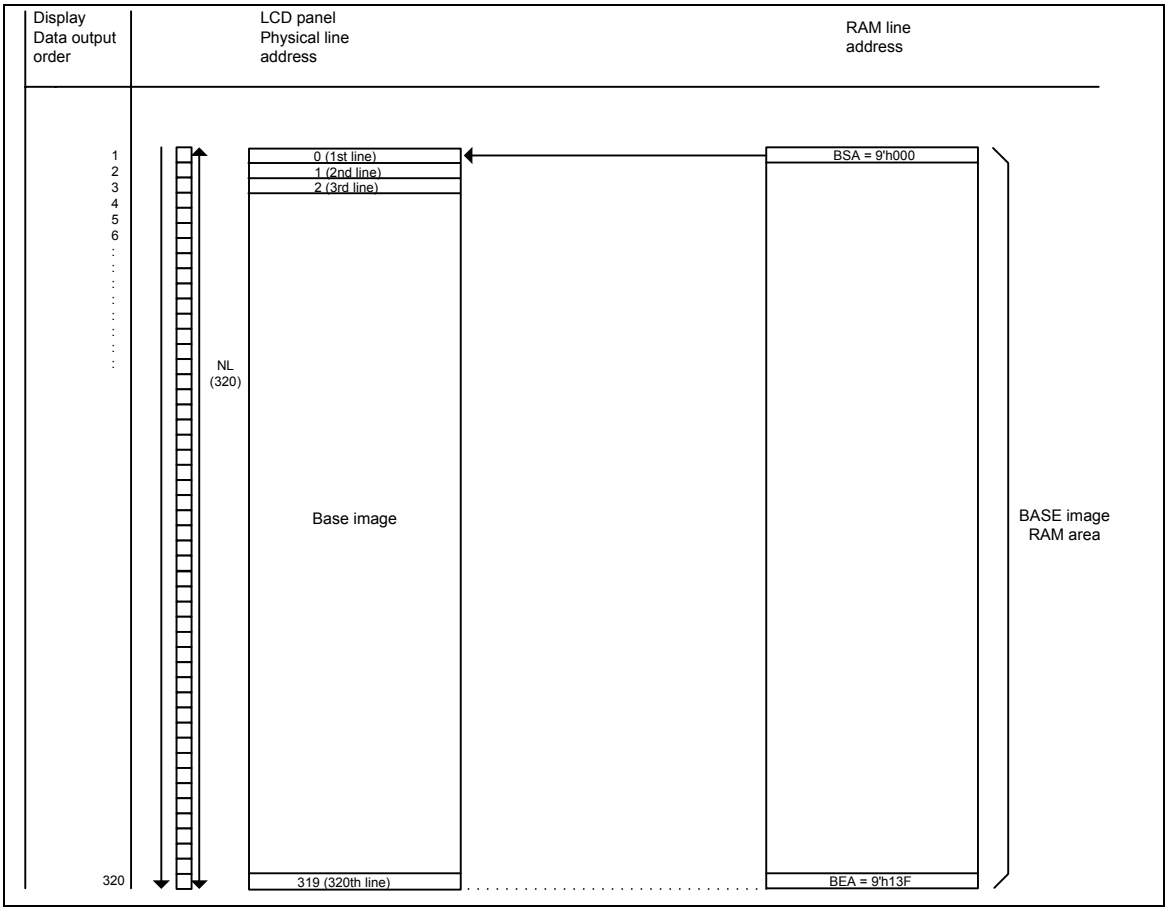


Figure 48 Full screen display (no partial)

2. Partial only

The following is an example of setting for displaying partial image 1 only and turning off the base image display. The partial image 1 is displayed at the position designated by users.

Table 76

Base image display insruction	
BASEE	0
NL[5:0]	6'h27

Partial image 1 display insruction	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h08F
PTDP0[8:0]	9'h080

Partial image 2 display insruction	
PTDE1	0
PTSA1[8:0]	9'h000
PTEA1[8:0]	9'h000
PTDP1[8:0]	9'h000

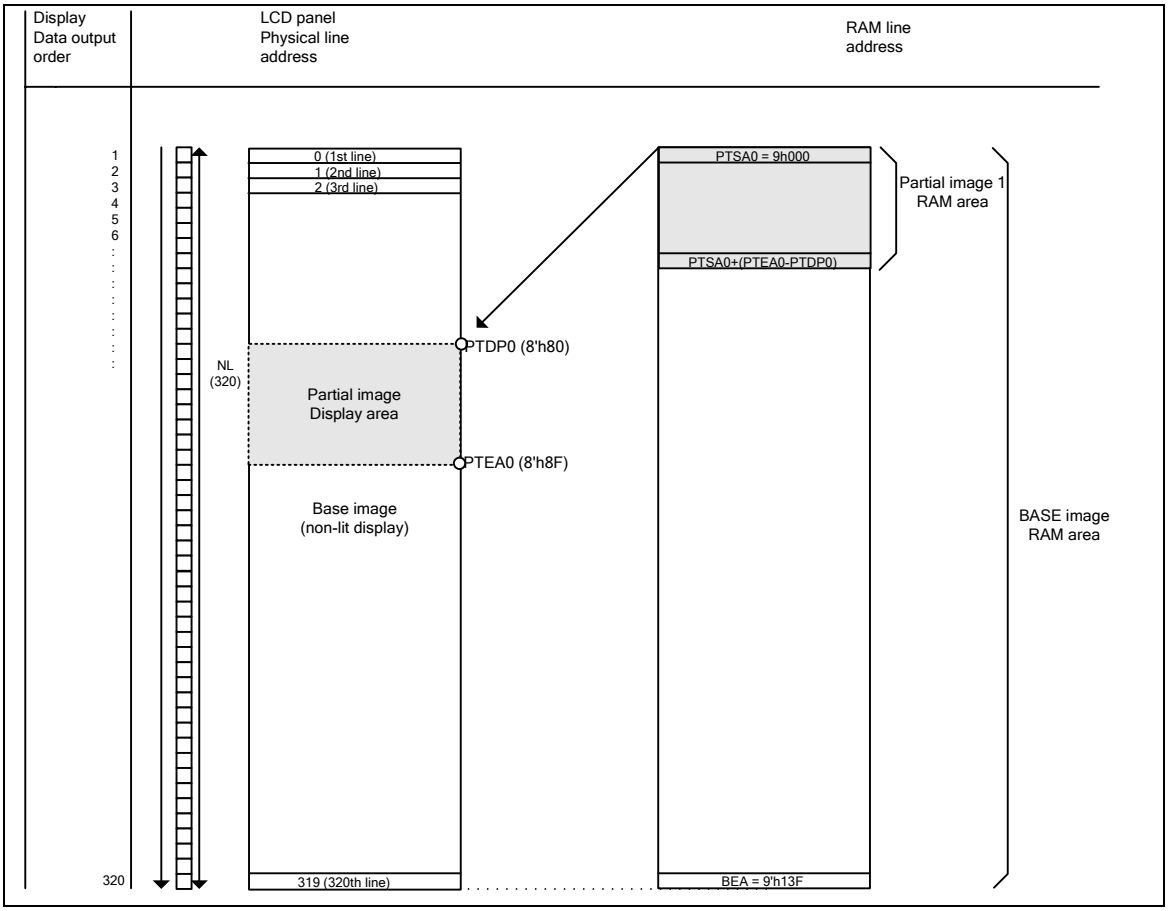


Figure 49 Partial display

Resizing function

The LGDP4532 supports resizing function (x 1/2, x 1/4), which is executed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit representing the contraction factor (x1/2 or x1/4) of the image. This function enables the LGDP4532 to write the resized image data directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system just to transfer data as usual even when resizing of the image is required. This feature makes a resized image easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The LGDP4532 processes the contraction of an image simply by selecting pixels. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.

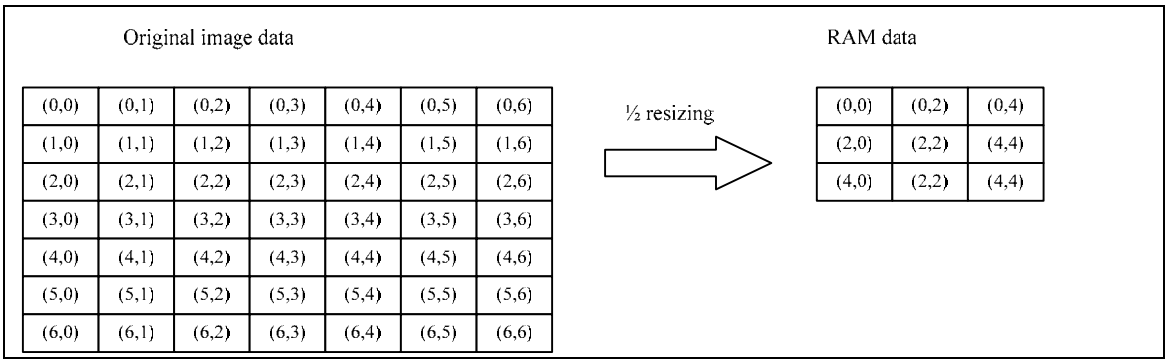


Figure 50 Data transfer in resizing

Table 77

Origianl image size (X x Y)	Resized image Size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
640x480(VGA)	320x240	160x120
352x288(CIF)	176x144	88x72
320x240(QVGA)	160x120	80x60
176x144(QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44

Resizing setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting the RAM area using the window address function, the window address area must be just the size of the resized picture. If resizing creates surplus pixels, which are calculated from the following equations, set them with the RCV, RCH bits before writing data to the internal RAM.

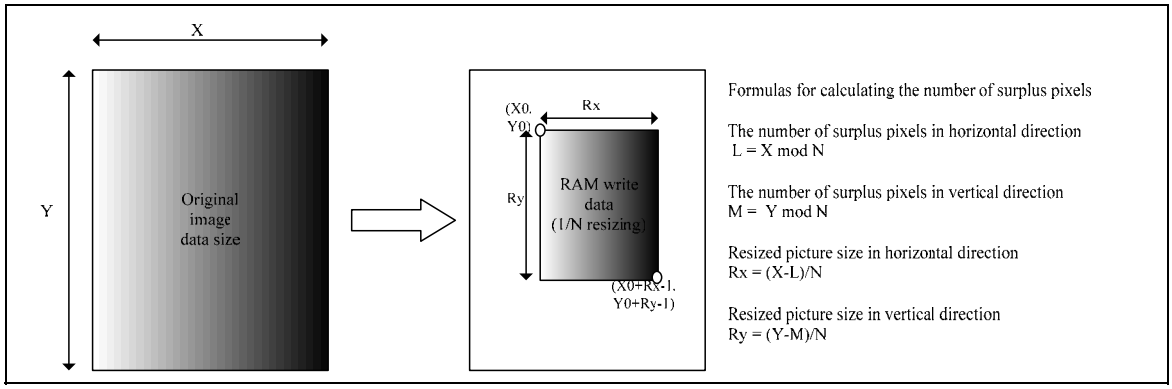


Figure 51 Resizing Setting, surplus pixel calculation

Table 78

Image (before resizing)		
Number of data in horizontal direction	X	
Numbef of data in vertical direction	Y	
Resizing ratio	1/N	

Resizing setting in the LGDP4532		
Resizing setting	RSZ	N-1
Numbef of data in horizontal direction	RCH	L
Numbef of data in vertical direction	RCV	M
RAM writing start address	AD	(X0,Y0)
RAM window address	HAS	X0
	HEA	X0+Rx-1
	VSA	Y0
	VEA	Y0+Ry-1

Notes to Resizing function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are remainder pixels. Otherwise (if RSZ = 2'h0), set RCH = RCV = 2'h0.

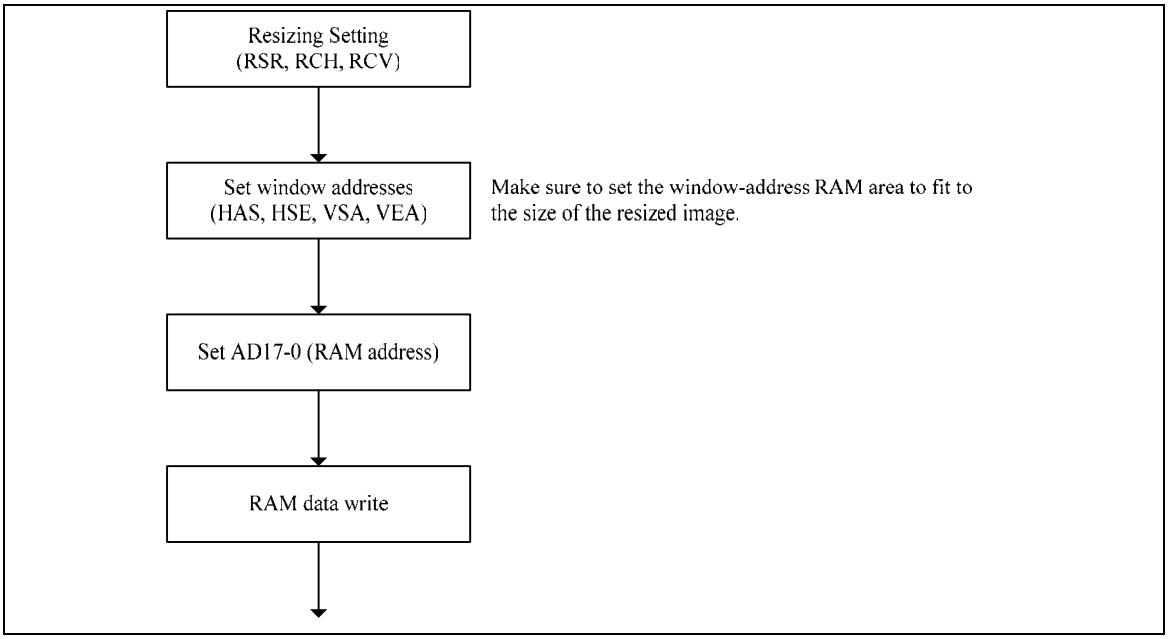


Figure 52 RAM write operation sequence in resizing

FMARK function

The LGDP4532 outputs an FMARK pulse in the timing when driving the line specified with FMP[8:0] bits. The FMARK signal can be used as a trigger signal in writing display data in synchronization with display operation by detecting the address where the RAM data is read out for display operation.

The output interval of FMARK pulse can be set with the FMI[2:0] bits. Set the FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. Sets FMARKOE = 1 when outputting FMARK pulse from the FMARK pin.

Table 79

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1
9'h002	2
:	:
9'h14D	333
9'h14E	334
9'h14F	335
9'h150 ~ 1FF	Setting disabled

Table 80

FMI[2:0]	FMARK output interval
3'h0	One frame period
3'h1	2 frame periods
3'h3	4 frame periods
3'h5	6 frame periods
Other setting	Setting disabled

FMP setting example

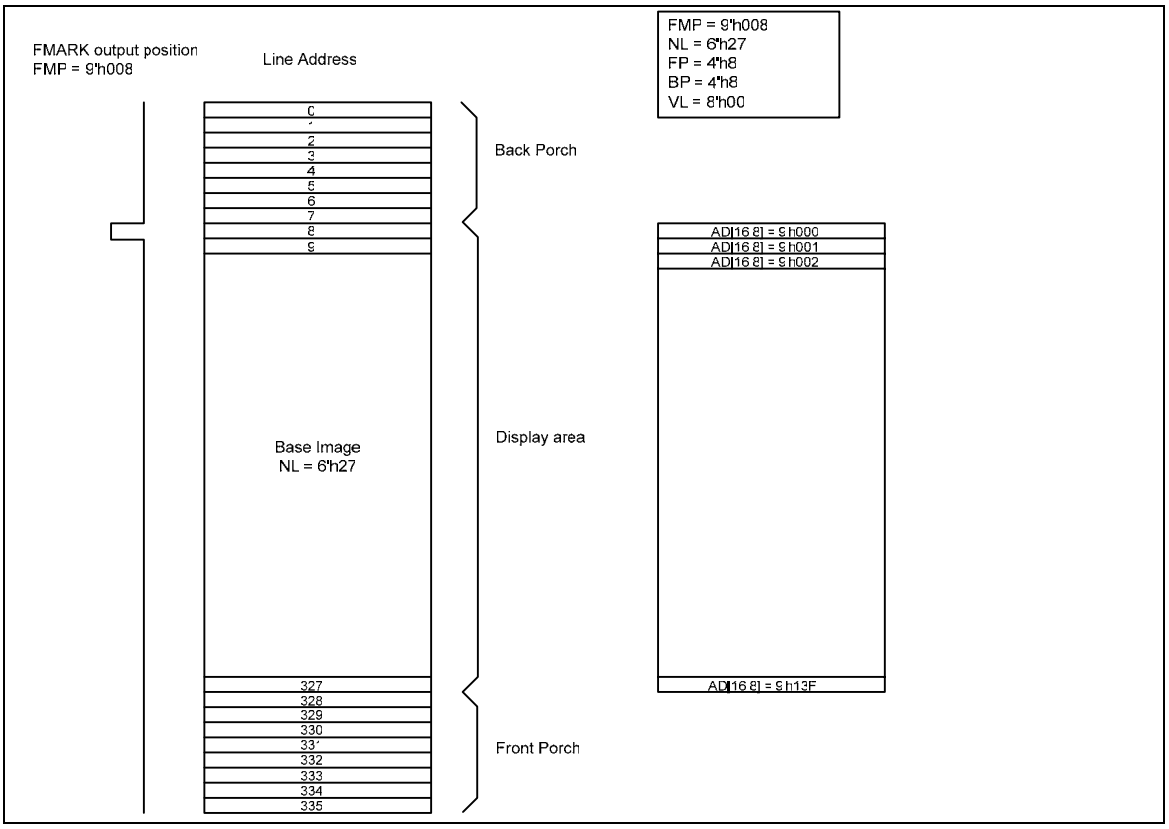


Figure 53

Display operation synchronous data transfer using FMARK

The LGDP4532 uses FMARK signal as a trigger signal to start writing data to the internal GRAM in synchronization with display scan operation.

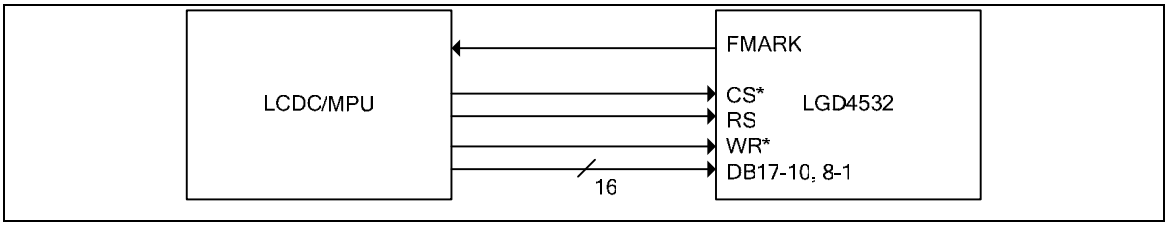


Figure 54 Display synchronous data transfer interface

The LGDP4532 writes display data to the internal GRAM at a speed faster to a certain degree than that of display operation in order to enable a moving picture display via the system interface without flicker. By writing all display data to the internal RAM, only the data tp be overwritten in the moving picture RAM area is transferred and the total data transfer for moving picture display can be minimized.

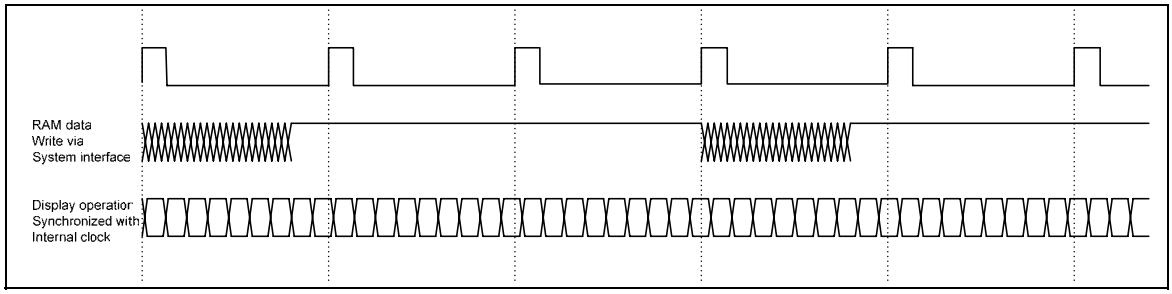


Figure 55 Moving Picture Data Transfers via FMARK function

The data transfer operation via FMARK function has a minimum RAM data rite speed an internal clock frequency, which must be more than the theoretical values chlculated from the following equations

Internal clock frequency (fosc) [Hz]
= FrameFrequency x (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) x 64(clocks) x variance

$$RAMWriteSpeed > \frac{240 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 64\ clocks \times \frac{1}{fosc}}$$

Note : When RAM write operation is not started right after the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of the RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the LGDP4532 to write data including image data consecutively without taking data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area setting range]
(Horizontal direction) 8'h00 ≤ HSA ≤ HEA ≤ 8'hEF
(Vertical direction) 9'h000 ≤ VSA ≤ VEA ≤ 9'h13F
[RAM Address setting range]
(RAM address) HSA ≤ AD7-0 ≤ HEA
VSA ≤ AD16-8 ≤ VEA

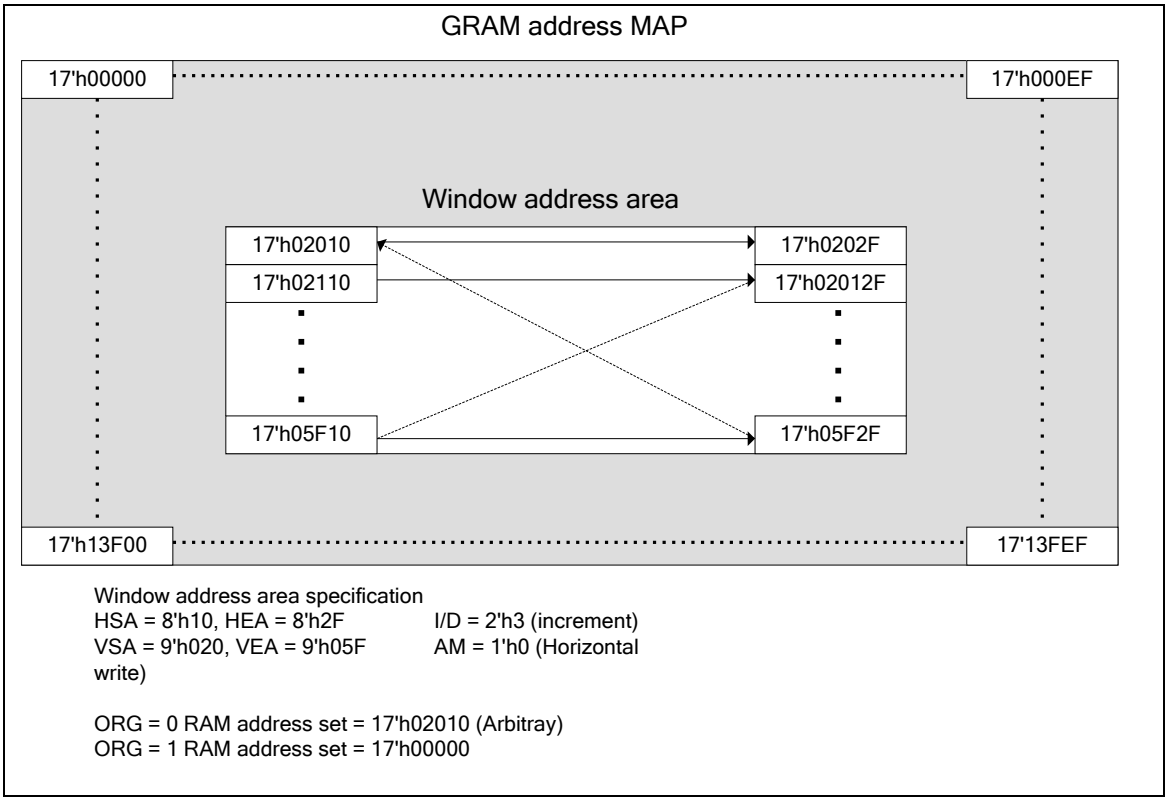


Figure 56 Automatic address update within a Window Address Area

EPROM Control

LGDP4532 has an embedded EPROM which is a 32-bit one-time programmable (OTP) IP from eMemory Technology Inc. (EO01X32KCV6).
EO01X32KCV6 is a CMOS, 1bit (1-bit) program OTP logic device. The main memory block is organized as 8-bits by 4 banks. See the data sheet of EO01X32KCV6.
The pins of the embedded EPROM can be controlled using the EPROM control 1 (R60h) register as shown below.

Table 81

EO01X32KCV6	Bit fields of register R40h
PTM = 0V/1.8V	PTM[1:0] = 00/11
POR = 0V/1.8V	POR = 0/1
VPP = 1.8V/7.2V	VPP = 0/1
PPROG = 0V/1.8V	PPROG = 0/1
PWE = 0V/1.8V	PWE = 0/1
PA[1:0] = 0V/1.8V	PA[1:0] = 0/1
PDIN[7:0] = 0V/1.8V	PDIN[7:0] = 0/1

The RA[1:0] of register R41h selects one of four EPROM bytes.
Accessing EPROM control registers, follow the timing requirements of read and program cycles.

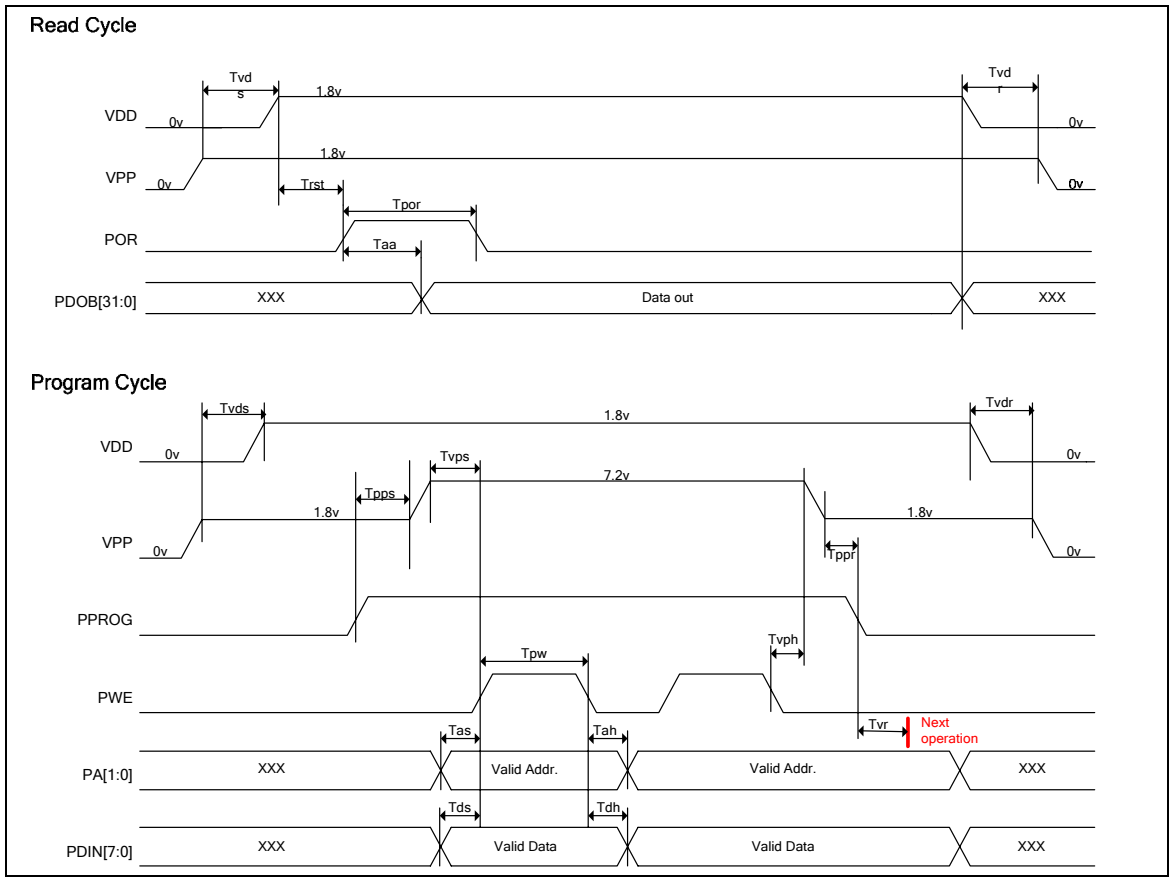


Figure 57 EPROM timings

Table 82

Parameter	Symbol	EO01X32KCV6		Unit
		Min	Max	
Risimg Time / Fallimg Time	T_r / T_f	-	1	ns
Data Access Time	T_{aa}	-	70	ns
Power-on Pulse Width Time	T_{por}	200	-	ns
Address / Data Setup Time	T_{as} / T_{ds}	4	-	ns
Address / Data Hold Time	T_{ah} / T_{dh}	9	-	ns
External VPP Setup Time	T_{vps}	0	-	ns
External VPP Hold Time	T_{vph}	0	-	ns
Program Recovery Time	T_{vr}	10	-	us
Program Pulse Width	T_{pw}	300	350	us
VDD Setup Time	T_{vds}	0	-	ms
VDD Recovery Time	T_{vdr}	0	-	ms
PPROG Setup Time	T_{pps}	10	-	ns
PPROG Recovery Time	T_{ppr}	10	-	ns
Power on Read Time	T_{rst}	20	-	ns

Notes
1. All electrical and timing parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.
2. All program signals that align together in the timing diagrams should be derived from the rising clock edge.
3. All timing measurements are from the 50% of the input to 50% of the output.
4. All input waveforms have rising time (t_r) and falling time (t_f) of 1ns from 10% to 90% of the input waveforms.
5. For capacitive loads greater than 1pF, access time will increase by 1ns per pF of additional loading.
6. Program time means one byte program time in user mode

Scan Mode Setting

The LGDP4532 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the LGDP4532 and the LCD panel.

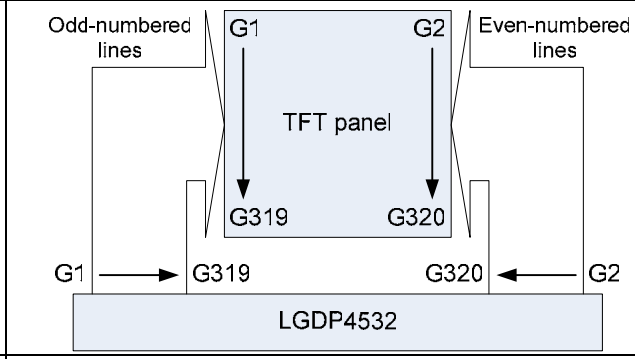
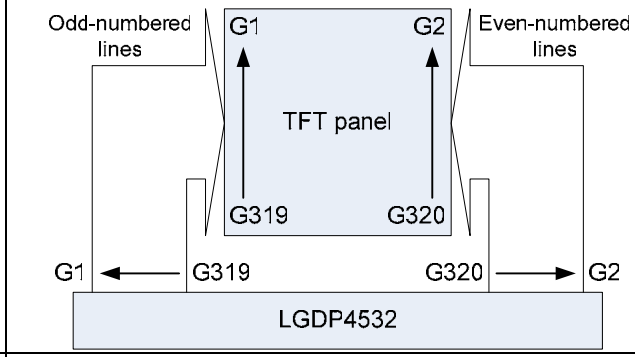
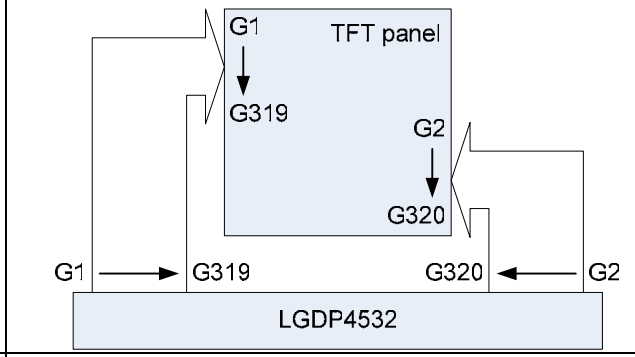
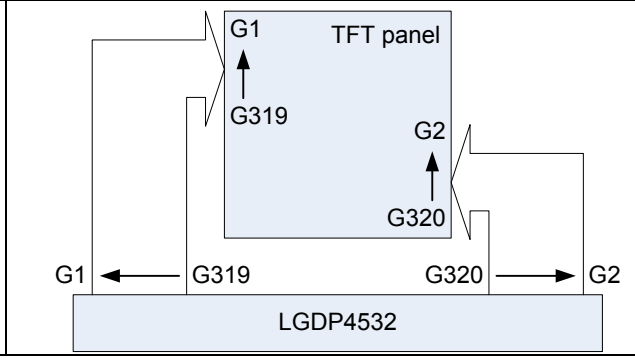
SM	GS	Scan direction	
0	0		G1, G2, G3, G4, …, G318, G319, G320
0	1		G320, G319, G318, …, G4, G3, G2, G1
1	0		G1, G3, G5, …, G317, G319, G2, G4, G6, …, G318, G320
1	1		G320, G318, G316, …, G6, G4, G2, G319, G317, G315, …, G5, G3, G1

Figure 58

Line Inversion AC Drive

The LGDP4532, in addition to the frame-inversion liquid crystal AC drive, supports the n-line inversion AC drive, in which the polarity of liquid crystal is inverted in units of n lines, where n takes a number from 1 to 64. The quality of display will be improved by using n-line inversion AC drive.
In determining n (the value set with the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells .

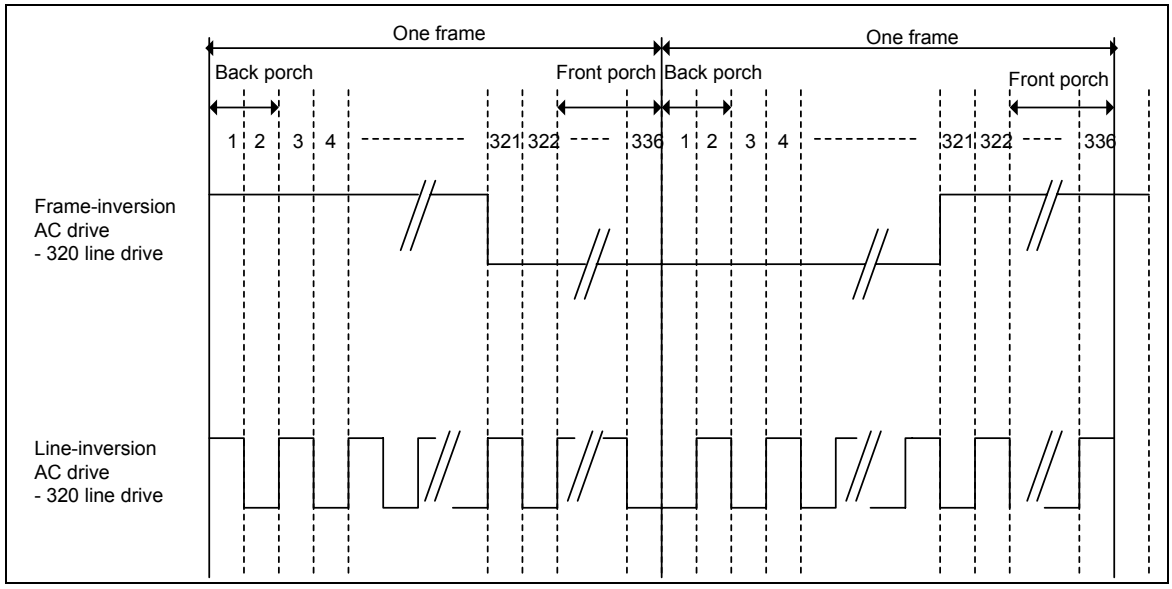


Figure 59 Example of Alternating Signals for n-line Inversion

Frame-Frequency Adjustment Function

The LGDP4532 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting the DIVI/E, RTNI/E bits without changing the oscillation frequency.

To switch frame frequencies according to whether displaying a moving picture or displaying a still picture, set a high oscillation frequency in advance. Then, set a low frame frequency to save power consumption when displaying a still picture. When displaying a moving picture, set the frequency high.

Relationship between the liquid crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frqme frequency is calaulated from the following equation. The frame frequency can be adjusted by setting the 1H period adjustment (RTNI/E) bit and the operation clock division (DIVI/E) bit.

Equlation for calculating frame frequency

$$Frame\ Frequency = \frac{Fosc}{Number\ Of\ Clocks\ Per\ Line \times Division\ Ratio \times (Line + FP + BP)}$$

Fosc	: RC oscillation frequency
Number of Clocks per line	: RTNI/E bit
Division Ratio	: DIVI/E bit
Line	: number of lines to drive the LCD (NL bit)
FP	: Number of lines for front porch
BP	: Number of lines for back porch

Example of Calculation : when maximum frame frequency = 60Hz

Number of lines : 320 lines
1H period : 64 Clock cycles (RTNI/E[4:0] = “10000”)
Division ratio of operating clock : 1/1
Front porch : 2 lines
Back porch : 14 lines

Fosc = 60 (Hz) x 64 (clocks) x 1/1 x (320 + 2 + 14) (Lines) = 1. 29(MHz)

In this case, the RC oscillation frequency is to set to 1.29MHz. Adjust the value of the external resistor coneected to the RC oscillator so that RC oscillation frequency becomes 1.29MHz.

Partial Display Function

The partial display function allows the LGDP4532 to drive linies selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven with non-display level to reduce power consumption.

The power saving effect can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

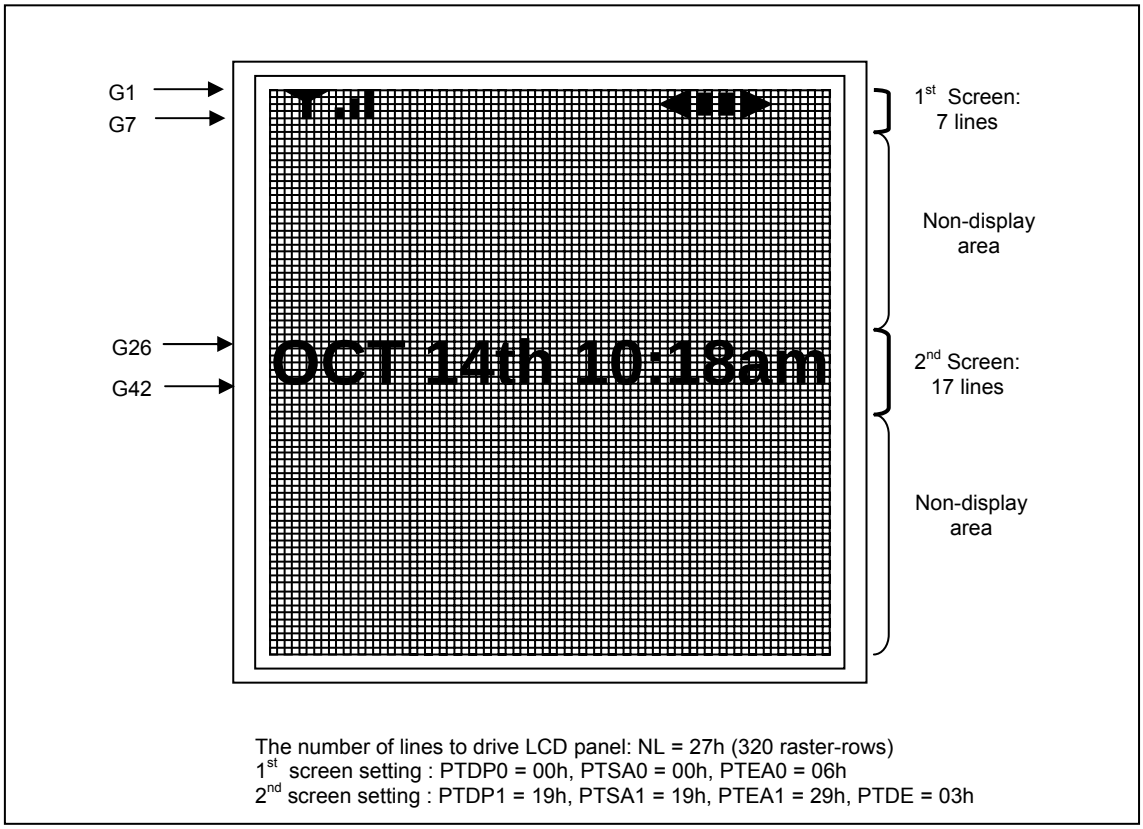


Figure 60

Liquid crystal pnael interface timing

The relationships between RGB interface signals and liquid crustal panel control signals in interhal operation and RGB interface operations are as follows.

Internal clock operation

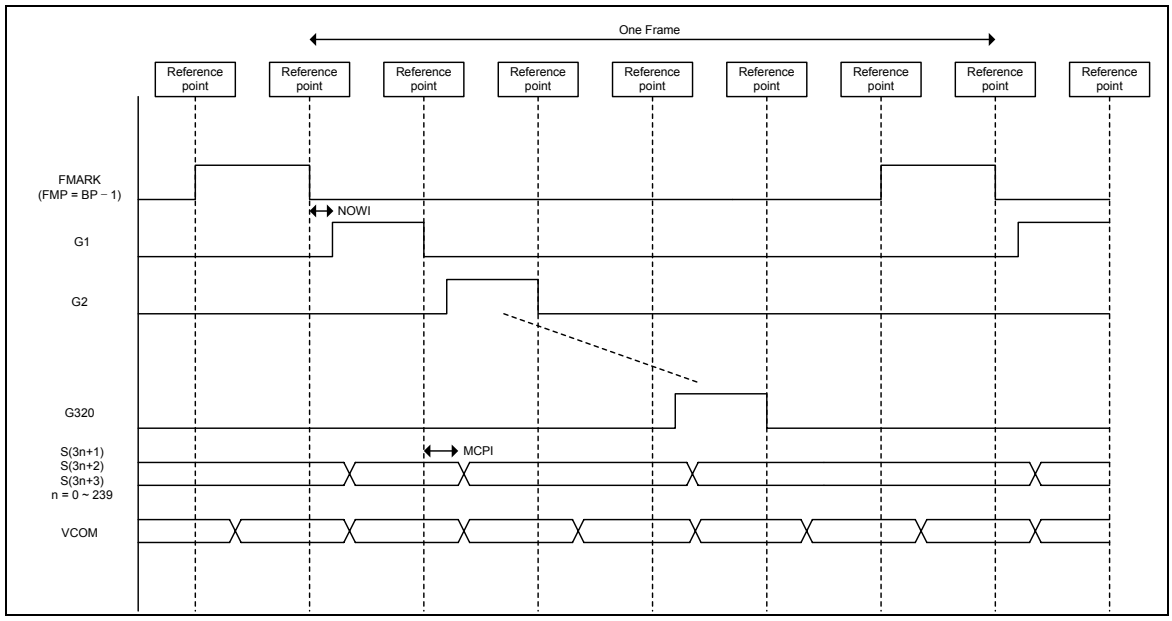


Figure 61

RGB Interface operation

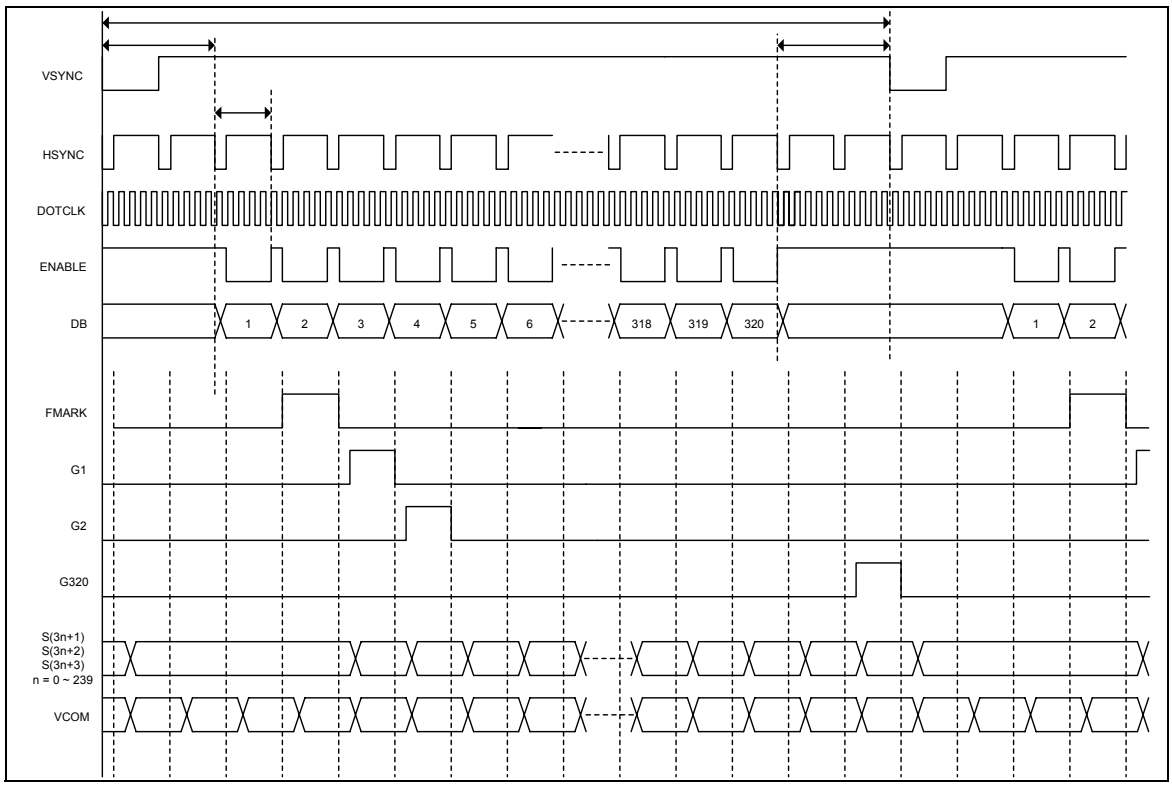


Figure 62

Oscillator

The LGDP4532 generates oscillation with the LGDP4532's internal RC oscillators by placing an external oscillation resistor between the OSC1 and OSC2 pins. The oscillation frequency varies due to resistance value of external resistor, wiring distance, and operating supply voltage. For example, placing an Rf resistor of a larger resistance value, or lowering the supply voltage level brings down the oscillation frequency. See the "Notes to Electrical Characteristics" section for the relationship between resistance value of Rf resistor and oscillation frequency.

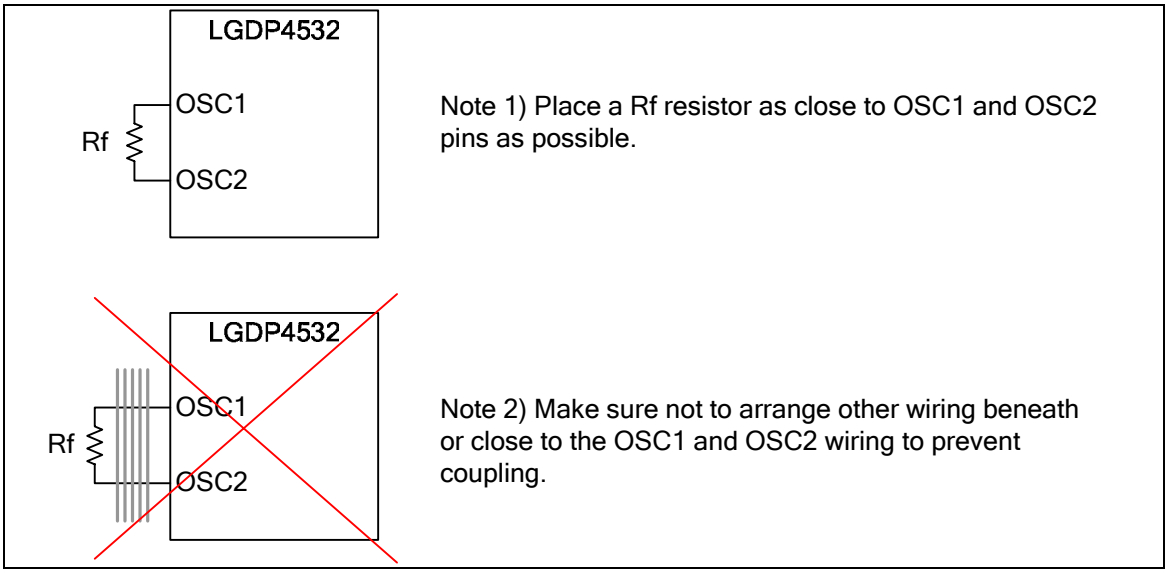


Figure 63

γ-Correction Function

The LGDP4532 has the γ-correction function to display in 262,144 colors simultaneously. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LGDP4532 available with liquid crystal panels of various characteristics.

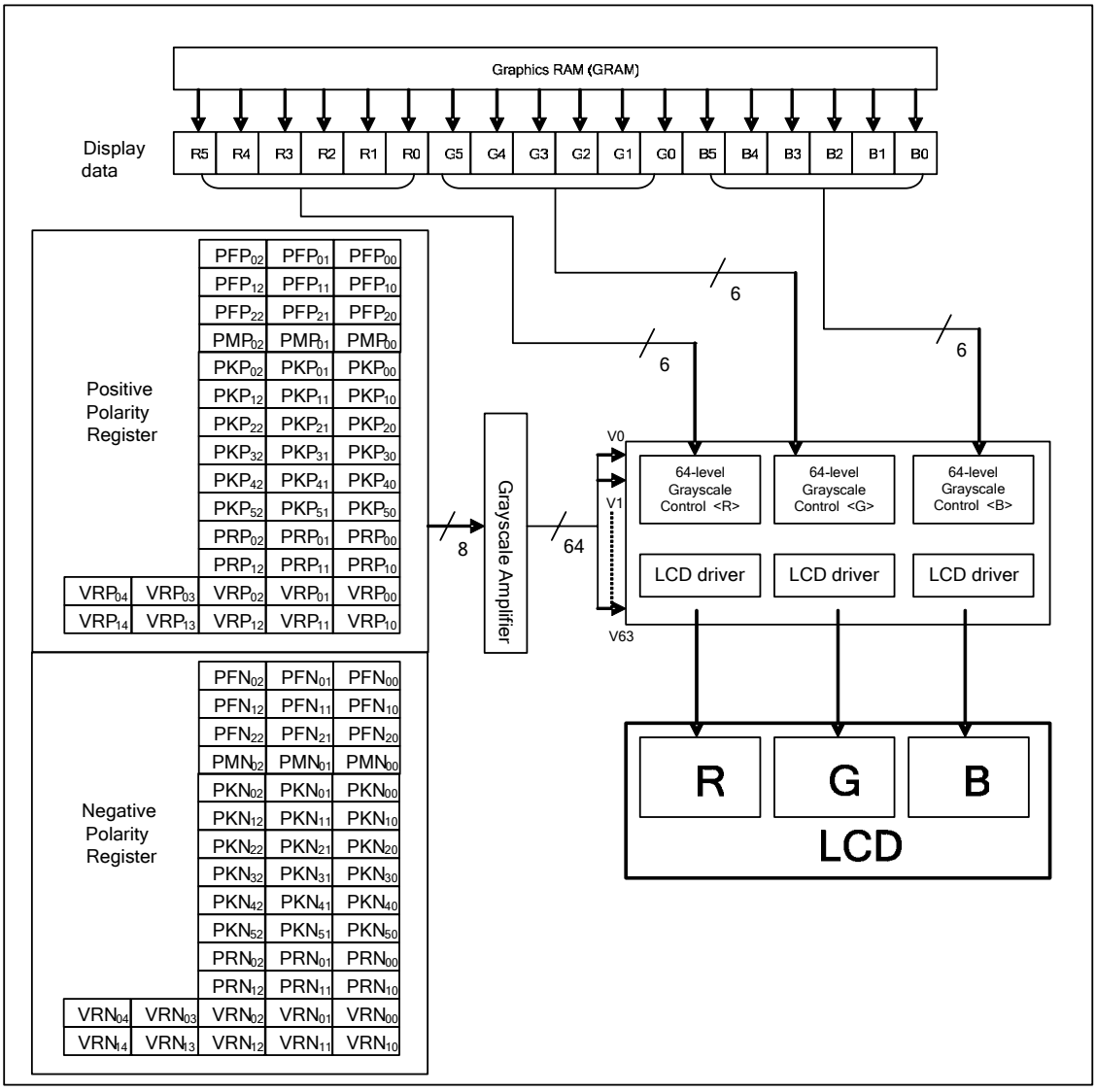


Figure 64 Grayscale control

Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the LGDP4532.

To generate 64 grayscale voltages (V0 to V63), the LGDP4532 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

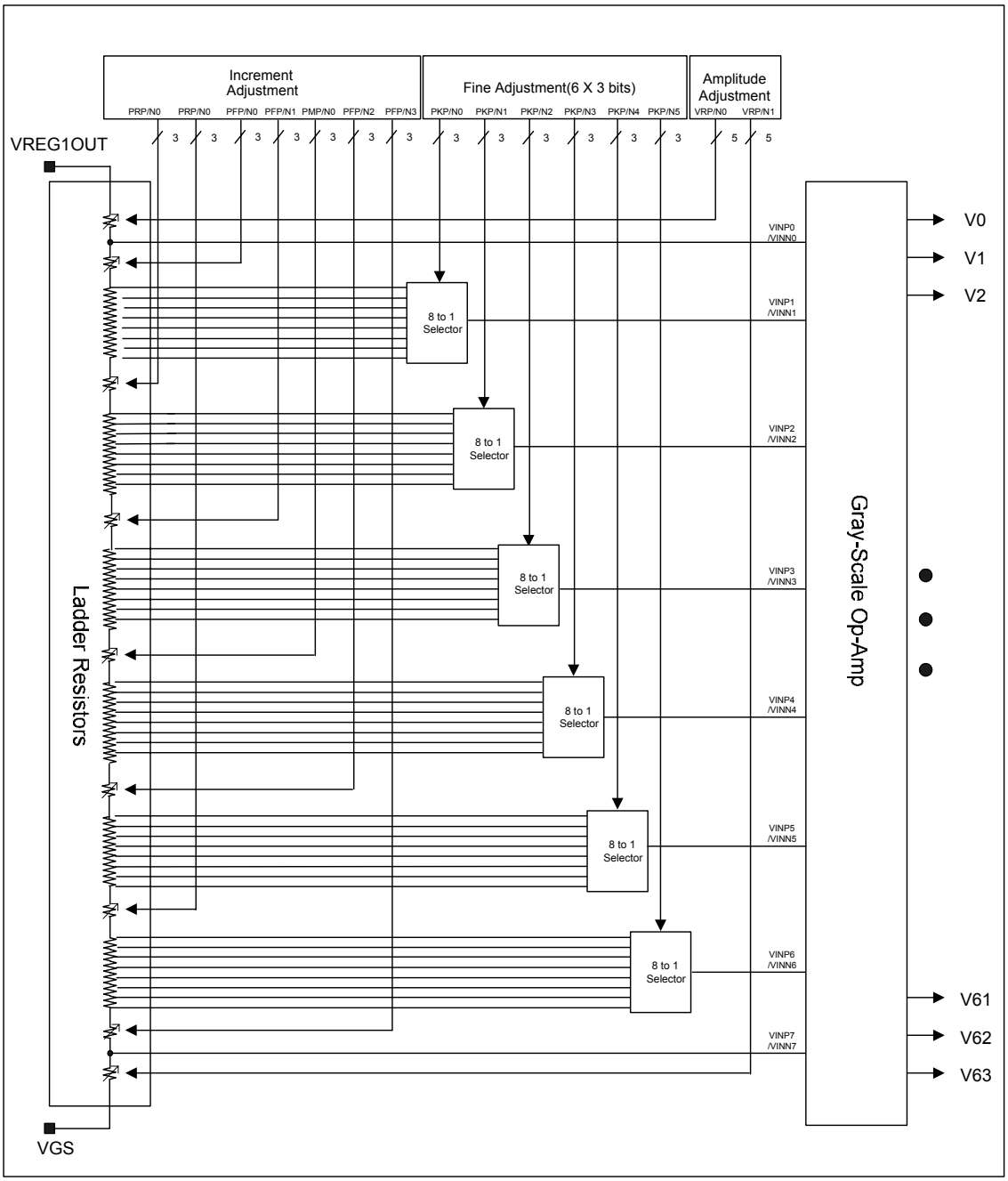


Figure 65 Grayscale amplifier unit

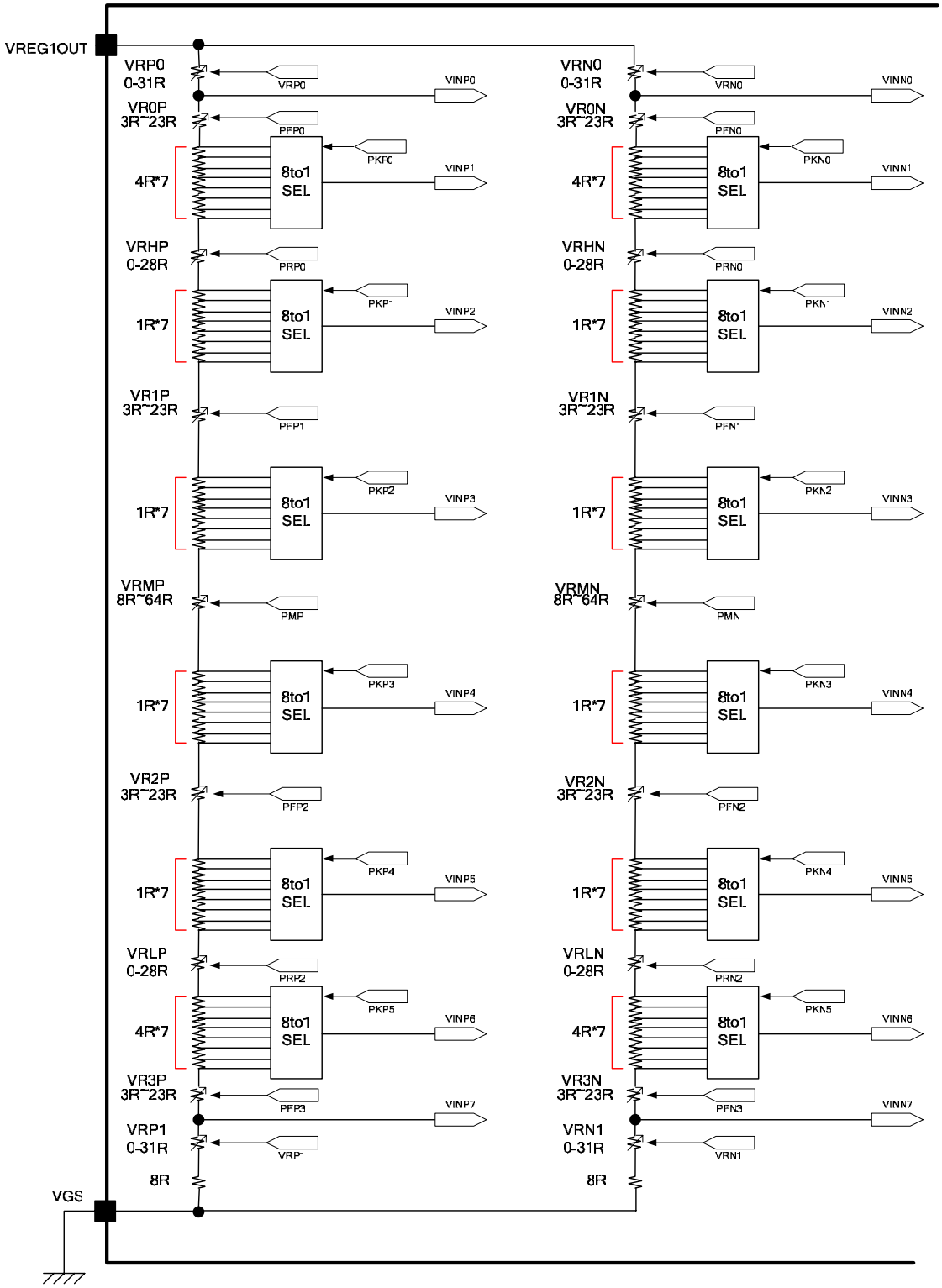


Figure 66 Ladder resistor units and 8-to-1 selectors

γ-Correction Register

The γ-correction registers of the LGDP4532 consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for γ-characteristics of a liquid crystal panel. These γ-correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.

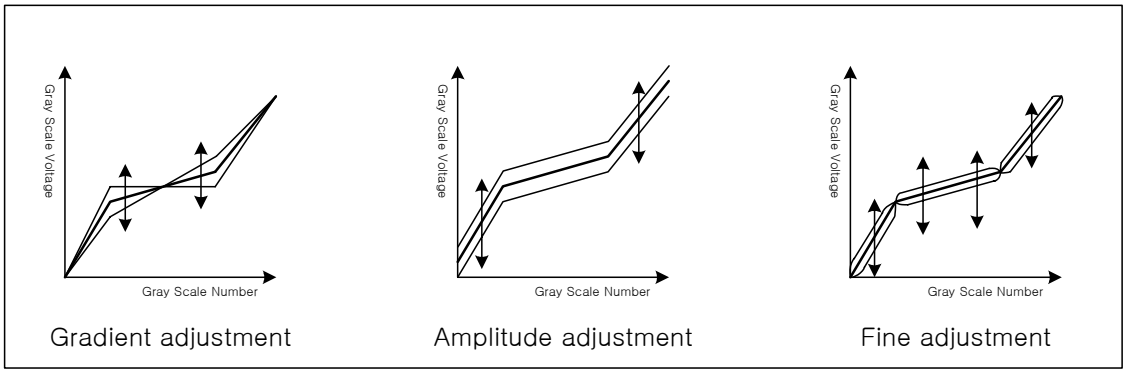


Figure 67

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 83 List of registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
	PFP0[2:0]	PFN0[2:0]	Variable resistor VR0P(N)
	PFP1[2:0]	PFN1[2:0]	Variable resistor VR1P(N)
	PFP2[2:0]	PFN2[2:0]	Variable resistor VR2P(N)
	PFP3[2:0]	PFN3[2:0]	Variable resistor VR3P(N)
	PMP[2:0]	PMN[2:0]	Variable resistor VRMP(N)
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder Resistors and 8-to-1 Selector

Block Configuration

The reference voltage generating unit as illustrated in figure 66 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LGDP4532 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)/VR0~4P(N)/VRMP(N)) and amplitude adjustment (VRP(N)0~1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 84 Gradient adjustment

Contents of register PRP(N)0/1[2:0]	Resistance VRHP(N) VRLP(N)	Contents of register PFP(N)0/1/2/3[2:0]	Resistance VR0/1P(N) VR2/3P(N)	Contents of register PMP(N)[2:0]	Resistance VRMP(N)
000	0R	000	3R	000	8R
001	4R	001	5R	001	16R
010	8R	010	9R	010	24R
011	12R	011	11R	011	32R
100	16R	100	15R	100	40R
101	20R	101	17R	101	48R
110	24R	110	21R	110	56R
111	28R	111	23R	111	64R

.

Table 85 Amplitude adjustment

Contents of register VRP(N)0[4:0]	Resistance VRP(N)0 VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages

Table 86 Fine adjustment registers and selected voltage

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
3'h0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
3'h1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
3'h2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3'h3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
3'h4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
3'h5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
3'h6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
3'h7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formula.

Table 87 Formula for calculating voltage (1)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VREG1OUT - ΔV*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV*(VRP0+VR0P+0R)/SUMRP	PKP0= 3'h0	VINP1
KVP2	VREG1OUT - ΔV*(VRP0+VR0P+4R)/SUMRP	PKP0= 3'h1	
KVP3	VREG1OUT - ΔV*(VRP0+VR0P+8R)/SUMRP	PKP0= 3'h2	
KVP4	VREG1OUT - ΔV*(VRP0+VR0P+12R)/SUMRP	PKP0= 3'h3	
KVP5	VREG1OUT - ΔV*(VRP0+VR0P+16R)/SUMRP	PKP0= 3'h4	
KVP6	VREG1OUT - ΔV*(VRP0+VR0P+20R)/SUMRP	PKP0= 3'h5	
KVP7	VREG1OUT - ΔV*(VRP0+VR0P+24R)/SUMRP	PKP0= 3'h6	
KVP8	VREG1OUT - ΔV*(VRP0+VR0P+28R)/SUMRP	PKP0= 3'h7	
KVP9	VREG1OUT - ΔV*(VRP0+VR0P+28R+VRHP)/SUMRP	PKP1= 3'h0	VINP2
KVP10	VREG1OUT - ΔV*(VRP0+VR0P+29R+VRHP)/SUMRP	PKP1= 3'h1	
KVP11	VREG1OUT - ΔV*(VRP0+VR0P+30R+VRHP)/SUMRP	PKP1= 3'h2	
KVP12	VREG1OUT - ΔV*(VRP0+VR0P+31R+VRHP)/SUMRP	PKP1= 3'h3	
KVP13	VREG1OUT - ΔV*(VRP0+VR0P+32R+VRHP)/SUMRP	PKP1= 3'h4	
KVP14	VREG1OUT - ΔV*(VRP0+VR0P+33R+VRHP)/SUMRP	PKP1= 3'h5	
KVP15	VREG1OUT - ΔV*(VRP0+VR0P+34R+VRHP)/SUMRP	PKP1= 3'h6	
KVP16	VREG1OUT - ΔV*(VRP0+VR0P+35R+VRHP)/SUMRP	PKP1= 3'h7	
KVP17	VREG1OUT - ΔV*(VRP0+VR0/1P+35R+VRHP)/SUMRP	PKP2= 3'h0	VINP3
KVP18	VREG1OUT - ΔV*(VRP0+VR0/1P+36R+VRHP)/SUMRP	PKP2= 3'h1	
KVP19	VREG1OUT - ΔV*(VRP0+VR0/1P+37R+VRHP)/SUMRP	PKP2= 3'h2	
KVP20	VREG1OUT - ΔV*(VRP0+VR0/1P+38R+VRHP)/SUMRP	PKP2= 3'h3	
KVP21	VREG1OUT - ΔV*(VRP0+VR0/1P+39R+VRHP)/SUMRP	PKP2= 3'h4	
KVP22	VREG1OUT - ΔV*(VRP0+VR0/1P+40R+VRHP)/SUMRP	PKP2= 3'h5	
KVP23	VREG1OUT - ΔV*(VRP0+VR0/1P+41R+VRHP)/SUMRP	PKP2= 3'h6	
KVP24	VREG1OUT - ΔV*(VRP0+VR0/1P+42R+VRHP)/SUMRP	PKP2= 3'h7	
KVP25	VREG1OUT - ΔV*(VRP0+VR0/1P+42R+VRHP +VRMP)/SUMRP	PKP3= 3'h0	VINP4
KVP26	VREG1OUT - ΔV*(VRP0+VR0/1P+43R+VRHP +VRMP)/SUMRP	PKP3= 3'h1	
KVP27	VREG1OUT - ΔV*(VRP0+VR0/1P+44R+VRHP +VRMP)/SUMRP	PKP3= 3'h2	
KVP28	VREG1OUT - ΔV*(VRP0+VR0/1P+45R+VRHP +VRMP)/SUMRP	PKP3= 3'h3	
KVP29	VREG1OUT - ΔV*(VRP0+VR0/1P+46R+VRHP +VRMP)/SUMRP	PKP3= 3'h4	
KVP30	VREG1OUT - ΔV*(VRP0+VR0/1P+47R+VRHP +VRMP)/SUMRP	PKP3= 3'h5	
KVP31	VREG1OUT - ΔV*(VRP0+VR0/1P+48R+VRHP +VRMP)/SUMRP	PKP3= 3'h6	
KVP32	VREG1OUT - ΔV*(VRP0+VR0/1P+49R+VRHP +VRMP)/SUMRP	PKP3= 3'h7	
KVP33	VREG1OUT - ΔV*(VRP0+VR0/1/2P+49R+VRHP +VRMP)/SUMRP	PKP4= 3'h0	VINP5
KVP34	VREG1OUT - ΔV*(VRP0+VR0/1/2P+50R+VRHP +VRMP)/SUMRP	PKP4= 3'h1	
KVP35	VREG1OUT - ΔV*(VRP0+VR0/1/2P+51R+VRHP +VRMP)/SUMRP	PKP4= 3'h2	
KVP36	VREG1OUT - ΔV*(VRP0+VR0/1/2P+52R+VRHP +VRMP)/SUMRP	PKP4= 3'h3	
KVP37	VREG1OUT - ΔV*(VRP0+VR0/1/2P+53R+VRHP +VRMP)/SUMRP	PKP4= 3'h4	
KVP38	VREG1OUT - ΔV*(VRP0+VR0/1/2P+54+VRHP +VRMP)/SUMRP	PKP4= 3'h5	
KVP39	VREG1OUT - ΔV*(VRP0+VR0/1/2P+55R+VRHP +VRMP)/SUMRP	PKP4= 3'h6	
KVP40	VREG1OUT - ΔV*(VRP0+VR0/1/2P+56R+VRHP +VRMP)/SUMRP	PKP4= 3'h7	
KVP41	VREG1OUT - ΔV*(VRP0+VR0/1/2P+56R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h0	VINP6
KVP42	VREG1OUT - ΔV*(VRP0+VR0/1/2P+60R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h1	
KVP43	VREG1OUT - ΔV*(VRP0+VR0/1/2P+64R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h2	
KVP44	VREG1OUT - ΔV*(VRP0+VR0/1/2P+68R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h3	
KVP45	VREG1OUT - ΔV*(VRP0+VR0/1/2P+72R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h4	

KVP46	VREG1OUT - ΔV*(VRP0+VR0/1/2P+76R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h5	
KVP47	VREG1OUT - ΔV*(VRP0+VR0/1/2P+80R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h6	
KVP48	VREG1OUT - ΔV*(VRP0+VR0/1/2P+84R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h7	
KVP49	VREG1OUT - ΔV*(VRP0+VR0/1/2/3P+84R+VRHP+VRMP +VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors = 92R+VRHP+VRLP+VRP0+VRP1+VR0P+VR1P+VR2P +VR3P+VRMP

ΔV : Difference in electrical potential between VDH and VGS

Table 88 Formula for calculating voltage (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	VINP2+(VINP1-VINP2)*(30/48)
V3	VINP2+(VINP1-VINP2)*(23/48)
V4	VINP2+(VINP1-VINP2)*(16/48)
V5	VINP2+(VINP1-VINP2)*(12/48)
V6	VINP2+(VINP1-VINP2)*(8/48)
V7	VINP2+(VINP1-VINP2)*(4/48)
V8	VINP2
V9	VINP3+(VINP2-VINP3)*(22/24)
V10	VINP3+(VINP2-VINP3)*(20/24)
V11	VINP3+(VINP2-VINP3)*(18/24)
V12	VINP3+(VINP2-VINP3)*(16/24)
V13	VINP3+(VINP2-VINP3)*(14/24)
V14	VINP3+(VINP2-VINP3)*(12/24)
V15	VINP3+(VINP2-VINP3)*(10/24)
V16	VINP3+(VINP2-VINP3)*(8/24)
V17	VINP3+(VINP2-VINP3)*(6/24)
V18	VINP3+(VINP2-VINP3)*(4/24)
V19	VINP3+(VINP2-VINP3)*(2/24)
V20	VINP3
V21	VINP4+(VINP3-VINP4)*(22/23)
V22	VINP4+(VINP3-VINP4)*(21/23)
V23	VINP4+(VINP3-VINP4)*(20/23)
V24	VINP4+(VINP3-VINP4)*(19/23)
V25	VINP4+(VINP3-VINP4)*(18/23)
V26	VINP4+(VINP3-VINP4)*(17/23)
V27	VINP4+(VINP3-VINP4)*(16/23)
V28	VINP4+(VINP3-VINP4)*(15/23)
V29	VINP4+(VINP3-VINP4)*(14/23)
V30	VINP4+(VINP3-VINP4)*(13/23)
V31	VINP4+(VINP3-VINP4)*(12/23)

Grayscale voltage	Formula
V32	VINP4+(VINP3-VINP4)*(11/23)
V33	VINP4+(VINP3-VINP4)*(10/23)
V34	VINP4+(VINP3-VINP4)*(9/23)
V35	VINP4+(VINP3-VINP4)*(8/23)
V36	VINP4+(VINP3-VINP4)*(7/23)
V37	VINP4+(VINP3-VINP4)*(6/23)
V38	VINP4+(VINP3-VINP4)*(5/23)
V39	VINP4+(VINP3-VINP4)*(4/23)
V40	VINP4+(VINP3-VINP4)*(3/23)
V41	VINP4+(VINP3-VINP4)*(2/23)
V42	VINP4+(VINP3-VINP4)*(1/23)
V43	VINP4
V44	VINP5+(VINP4-VINP5)*(22/24)
V45	VINP5+(VINP4-VINP5)*(20/24)
V46	VINP5+(VINP4-VINP5)*(18/24)
V47	VINP5+(VINP4-VINP5)*(16/24)
V48	VINP5+(VINP4-VINP5)*(14/24)
V49	VINP5+(VINP4-VINP5)*(12/24)
V50	VINP5+(VINP4-VINP5)*(10/24)
V51	VINP5+(VINP4-VINP5)*(8/24)
V52	VINP5+(VINP4-VINP5)*(6/24)
V53	VINP5+(VINP4-VINP5)*(4/24)
V54	VINP5+(VINP4-VINP5)*(2/24)
V55	VINP5
V56	VINP6+(VINP5-VINP6)*(44/48)
V57	VINP6+(VINP5-VINP6)*(40/48)
V58	VINP6+(VINP5-VINP6)*(36/48)
V59	VINP6+(VINP5-VINP6)*(32/48)
V60	VINP6+(VINP5-VINP6)*(25/48)
V61	VINP6+(VINP5-VINP6)*(18/48)
V62	VINP6
V63	VINP7

Note: Make sure DDVDH-V0 > 0.5V

Relationship between RAM Data and Voltage Output Levels

The relationship between RAM data and source output voltage levels is as follows..

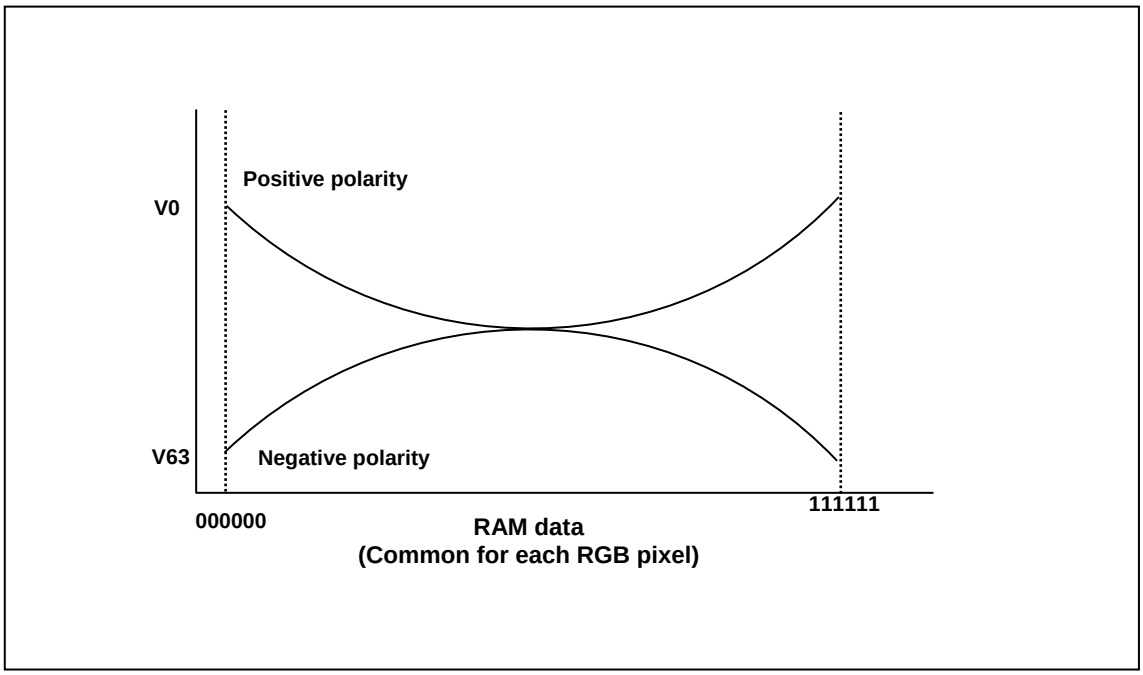


Figure 68 RAM data and the output voltage (REV = "1")

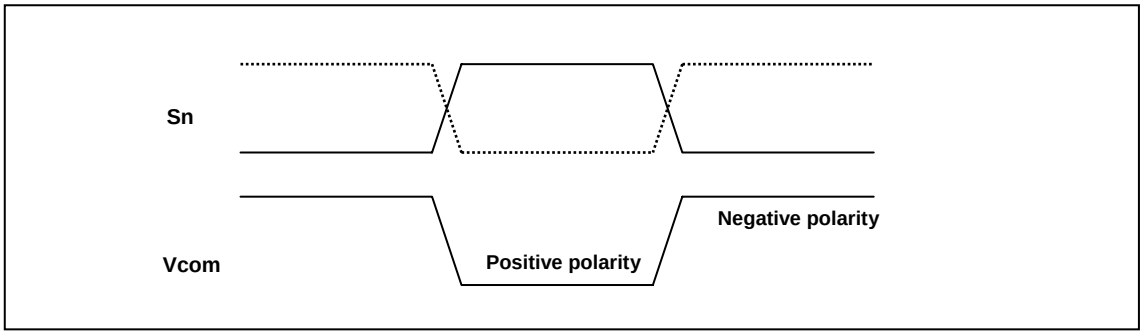


Figure 69 Source output and Vcom

8-Color Display Mode

The LGDP4532 has a function to display in 8colors. In 8-color mode, available grayscale levels are V0 and V63, and the power supplies of other grayscales (V1 to V62) are halted to reduce power consumption.

In 8-color display mode, the MSBs of the respective dot data (R5, G5, B5) are written to the rest of the dot data in order to display in 8 colors without rewriting the RAM data.

The γ- correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.

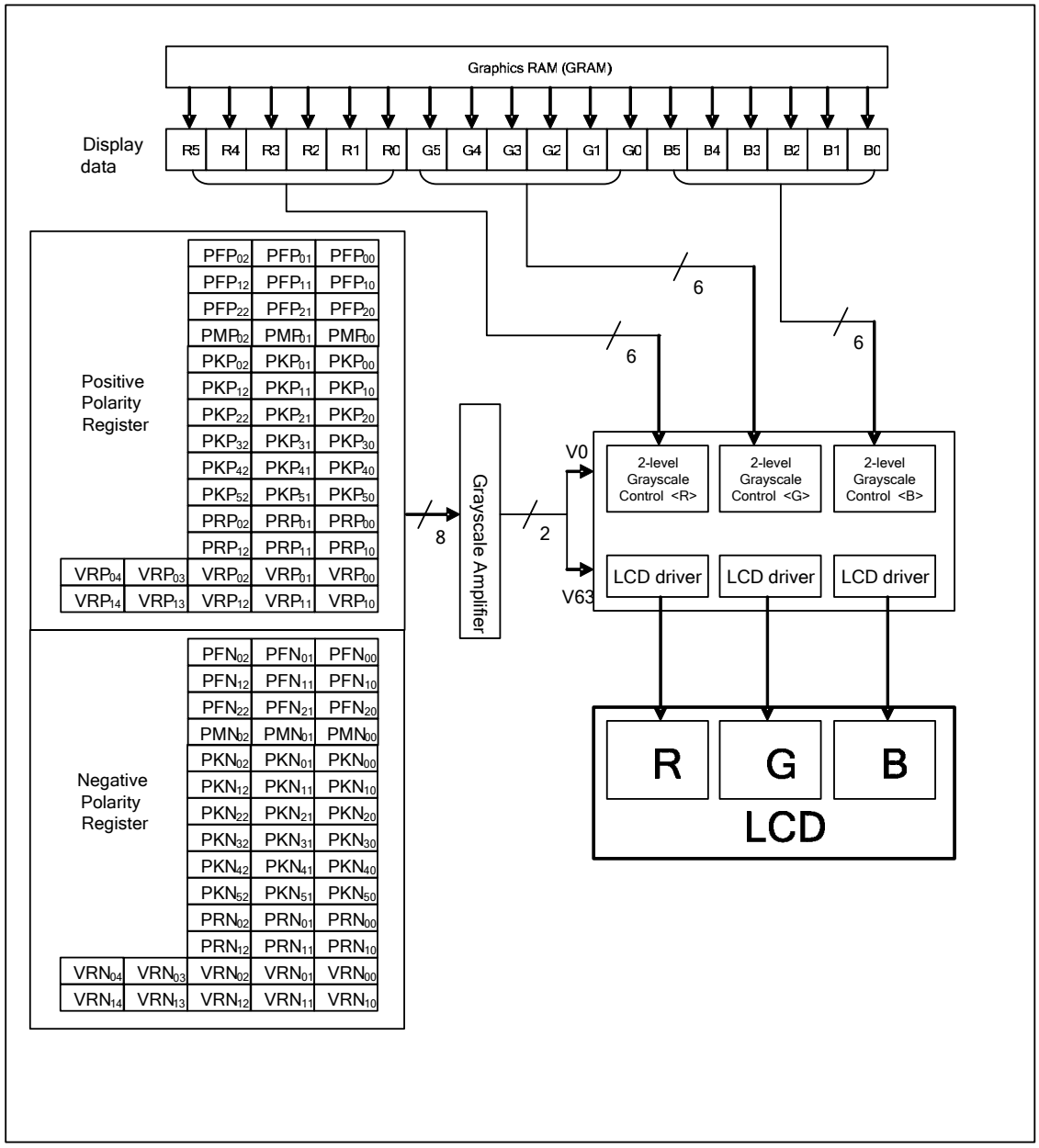


Figure 70 8-color display mode

To switch between the 262,144-color mode and 8-color mode, follow the sequence below.

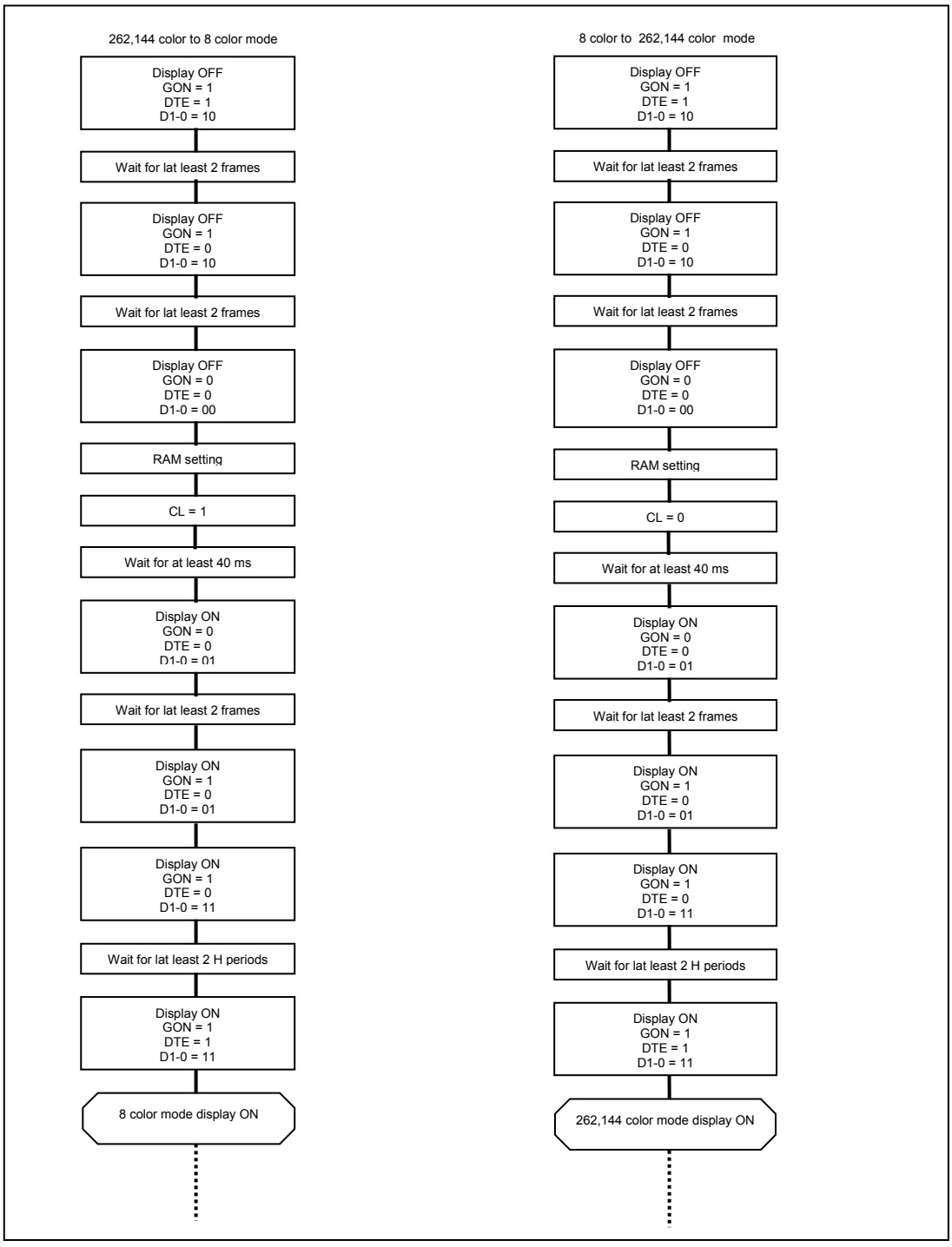


Figure 71

Power-supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the LGDP4532.

Power supply circuit connection example 1 (Vci1 = VciOUT)

In the following example, the VciOUT level is adjusted internally with the VciOUT output circuit.

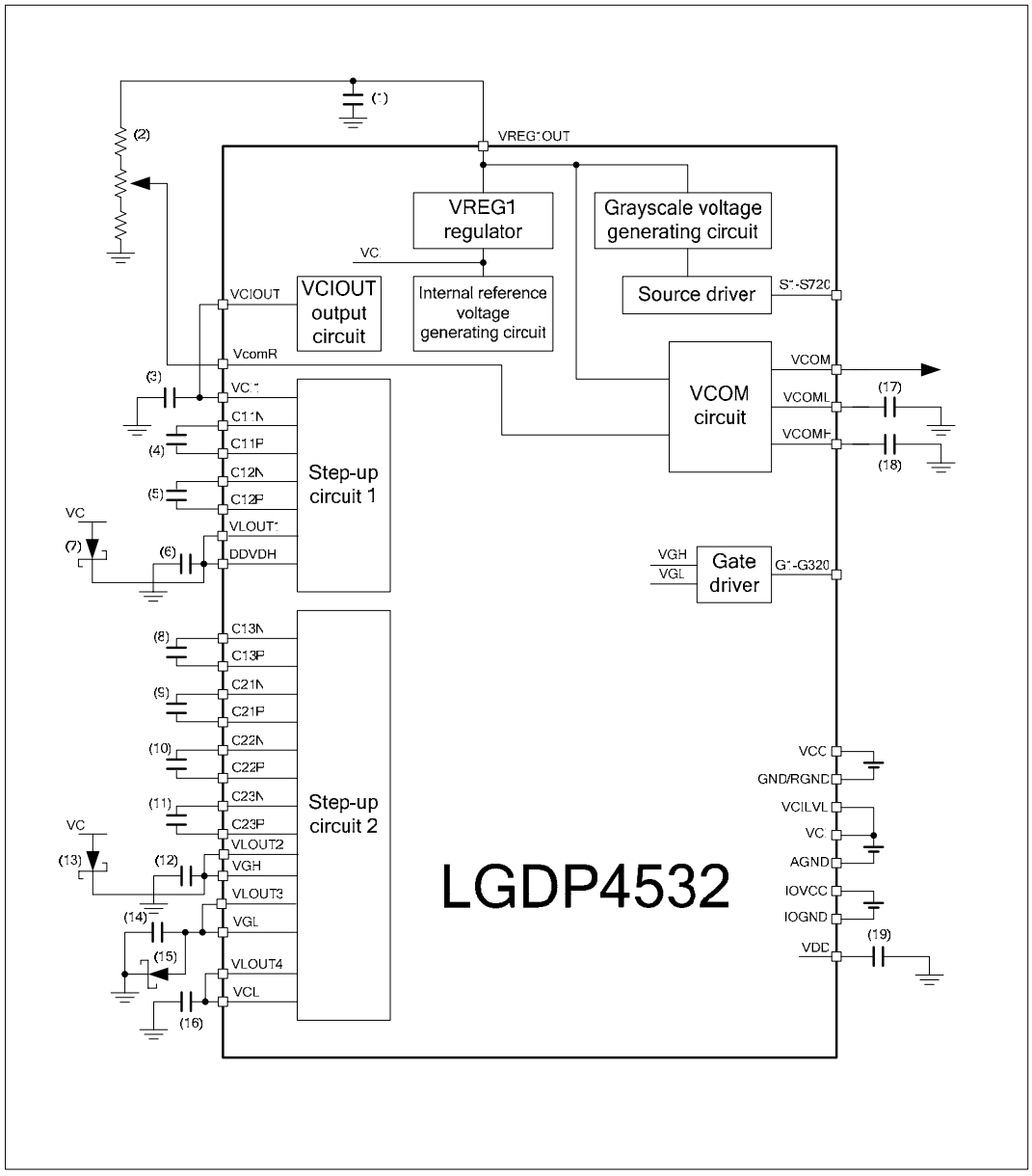


Figure 72

Note: The wiring resistance between the schottky diode and GND/VGL must be 10Ohm or less.

Power supply circuit connection example2 (Vci1 = Vci direct input)

In the following example, the electrical Vci is directly applied to Vci1. In this case, the VciOUT level cannot be adjusted internally but step-up operation becomes more effective

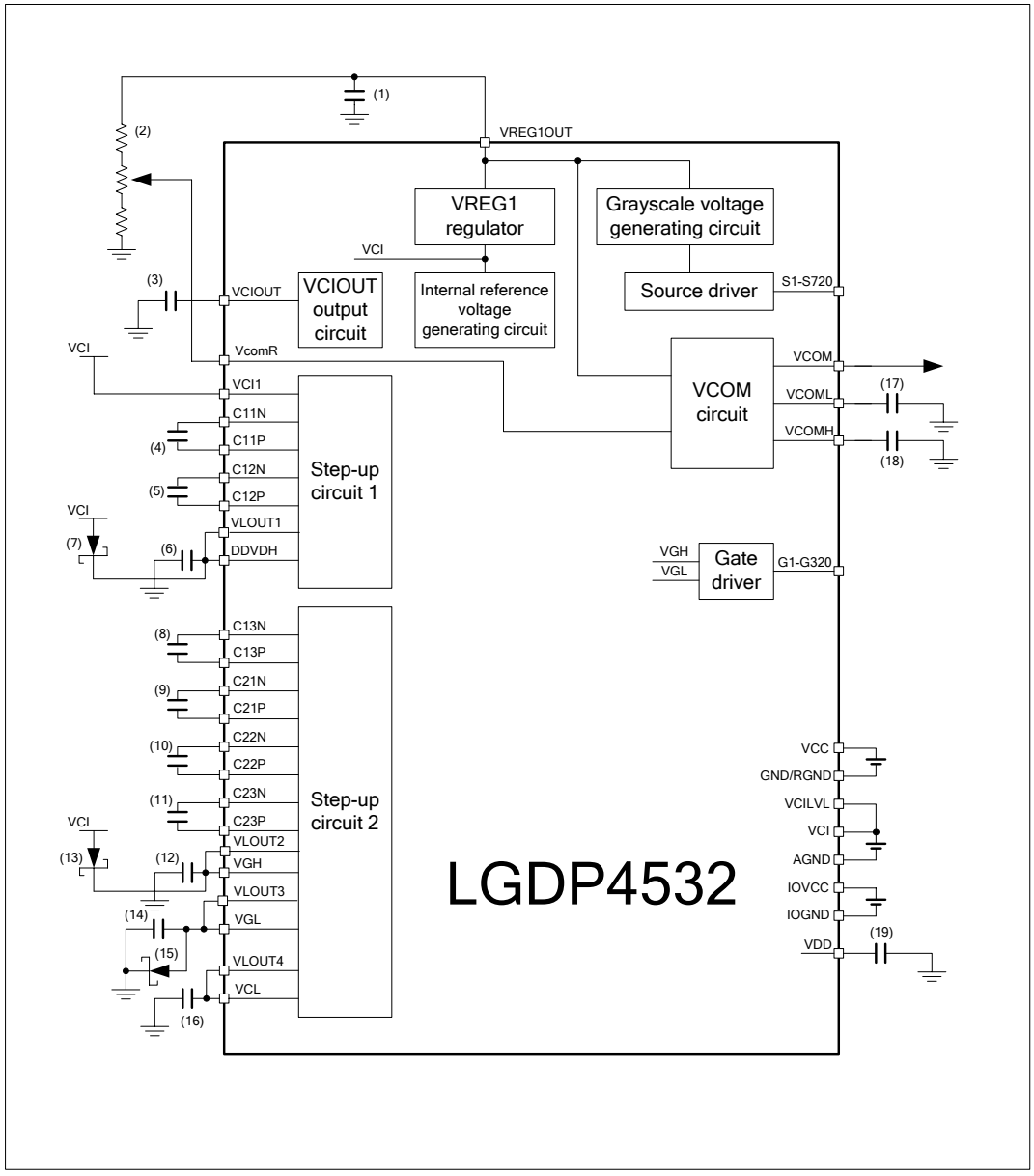


Figure 73

Note: 1. The wiring resistance between the schottky diode and GND/VGL must be 10Ohm or less.
2. When directly applying the Vci level to Vci1, set VC=3'h0.

Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the LGDP4532 are as follows.

Table 89 Capacitor

Capacitance	Voltage proof	Pin Connection
1uF (B characteristics)	6V	(1)VREG1OUT, (3)VciOUT, (4) C11N/P, (5) C12N/P, (8) C13N/P, (16) VLOUT4, (17) VCOML, (18) VCOMH, (19) VDD
	10V	(6) VLOUT1, (9) C21N/P, (10) C22N/P, (11) C23N/P
	25V	(12) VLOUT2, (14) VLOUT3

Notes: 1. Check with the LC module.
2. The numbers in the parentheses corresponds to the numbers of the elements in Figure 72, Figure 73.

Table 90 Schottky Diode

Specification	Pin Connection
VF<0.4 V/20 mA@25℃, VR ≥ 30V	(7) Vci-DDVDH (15) GND-VGL (13) Vci-VGH

Table 91 Variable Resistor

Specification	Pin Connection
>200kΩ	(2) VcomR

Voltage Setting Pattern Diagram

The pattern diabram of voltage setting and waveforms of the liquid crystal application voltages are as follows.

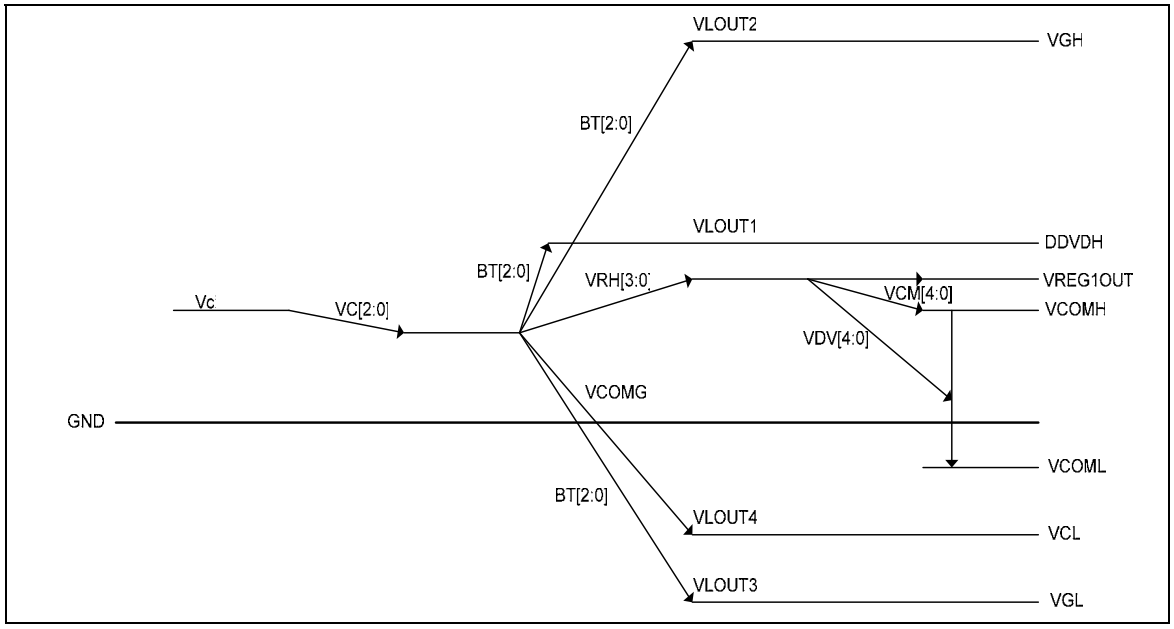


Figure 74 Pattern Diagram for Voltage Setting

Note Output voltages of DDVDH, VGH, VGL, and VCL drop from setting voltage(idea voltage) depending on the current consumption at output. (DDVDH – VREG1OUT) > 0.5V and (VCOML – VGL) > 0.5V are the relation to the actual voltage. When using the voltage in the large current consumption at the fast VCOM2 cycle(such as line-by-line inversion), check the voltage value

Power Supply Instruction Setting

The following are the sequences for setting power supply ON/OFF. Make power supply ON/OFF settings according to the following sequences in Display ON/OFF, Standby set/exit, Sleep set/exit sequences.

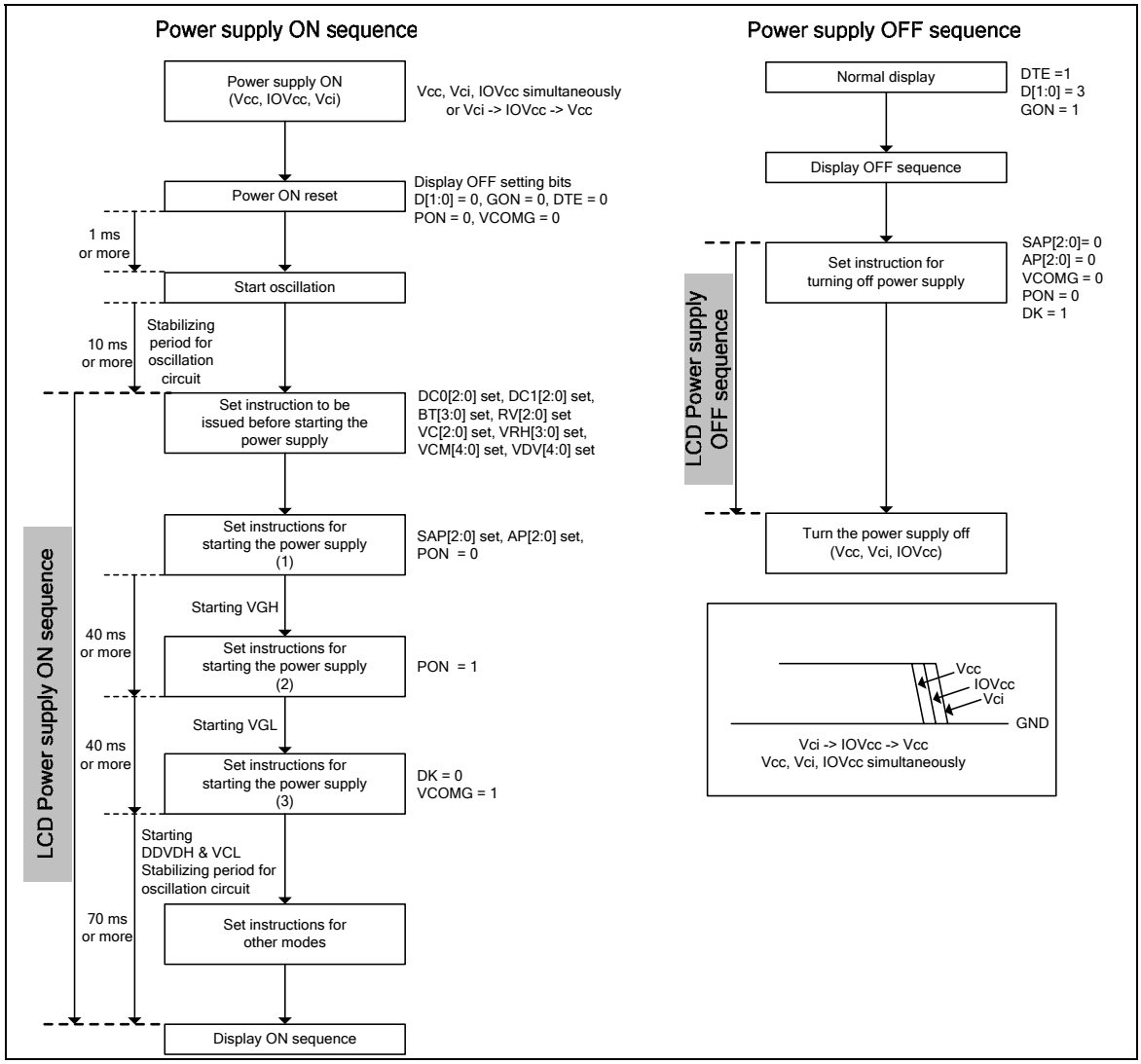


Figure 75

Instruction Setting

The following are the sequences for various instruction settings with the LGDP4532. When making the following instruction settings, follow the respective sequences below.

Display ON/OFF sequence

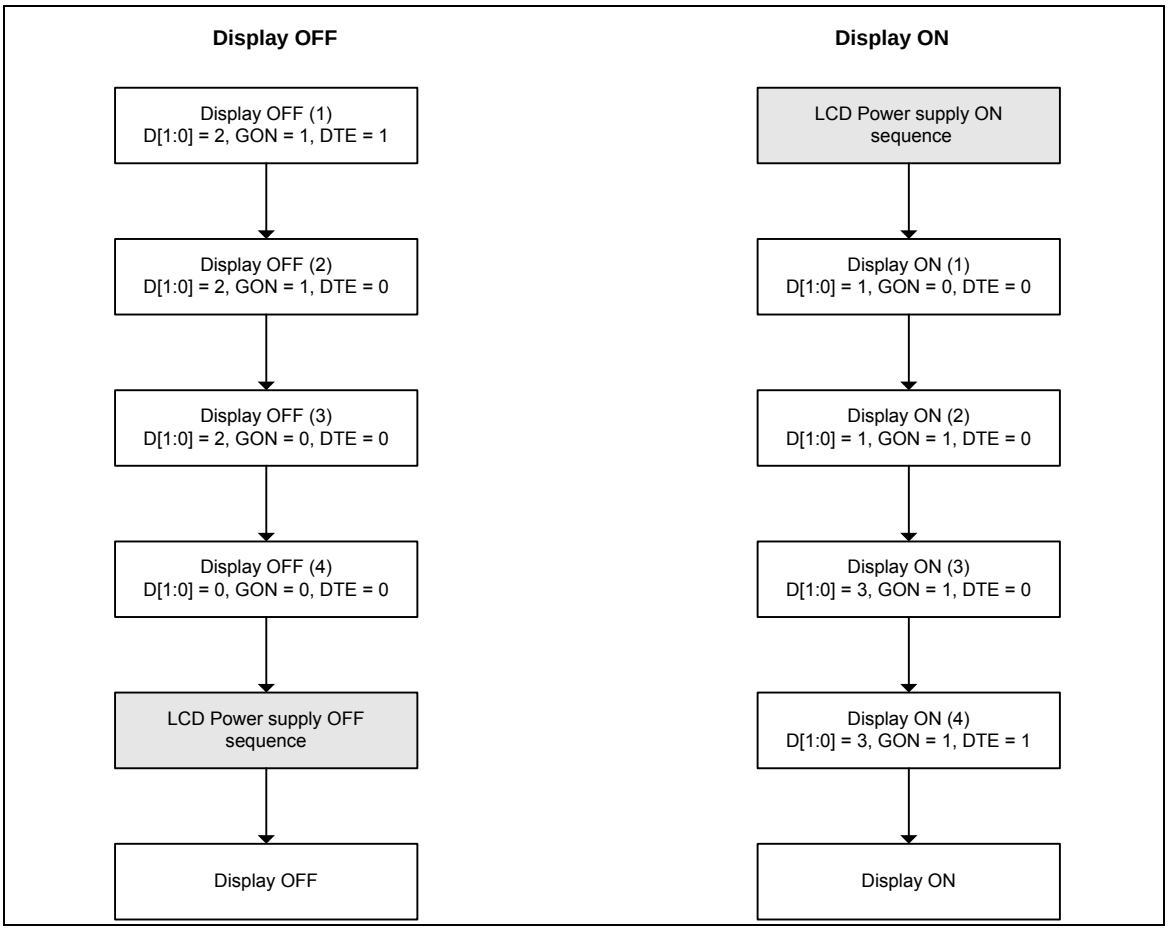


Figure 76

Standby / Sleep mode SET/EXIT sequences

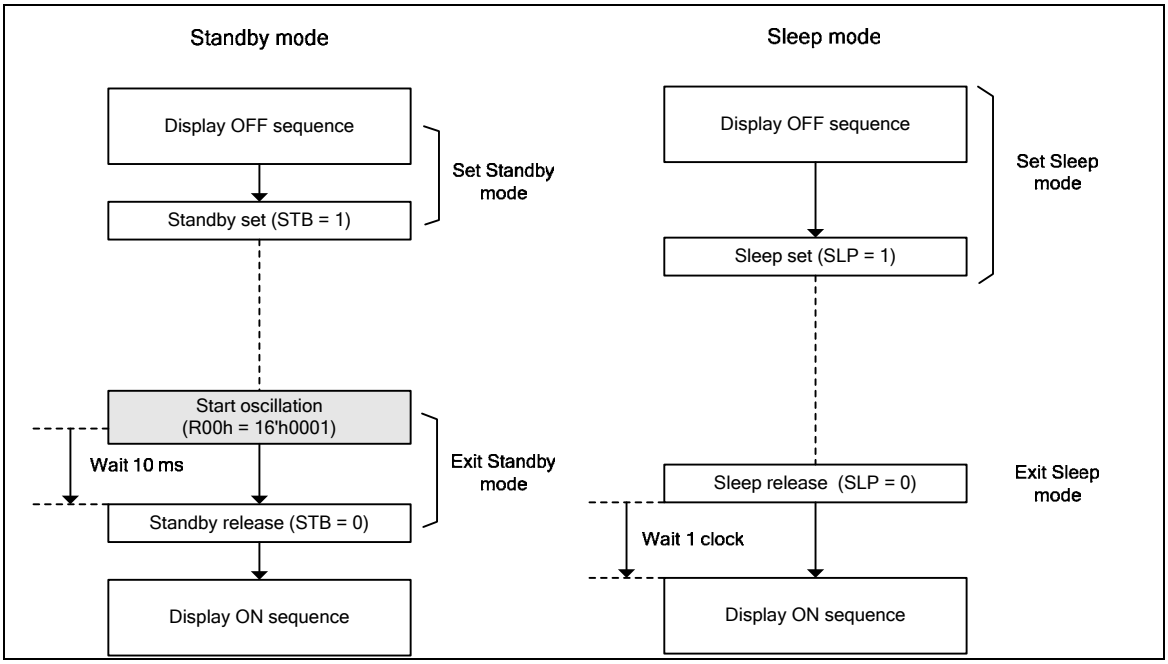


Figure 77

Note : “Display ON/OFF” sequences include “LCD Power Supply ON/OFF” sequences respectively. See “Display ON/OFF sequence” section.

Deep standby mode IN/EXIT sequences

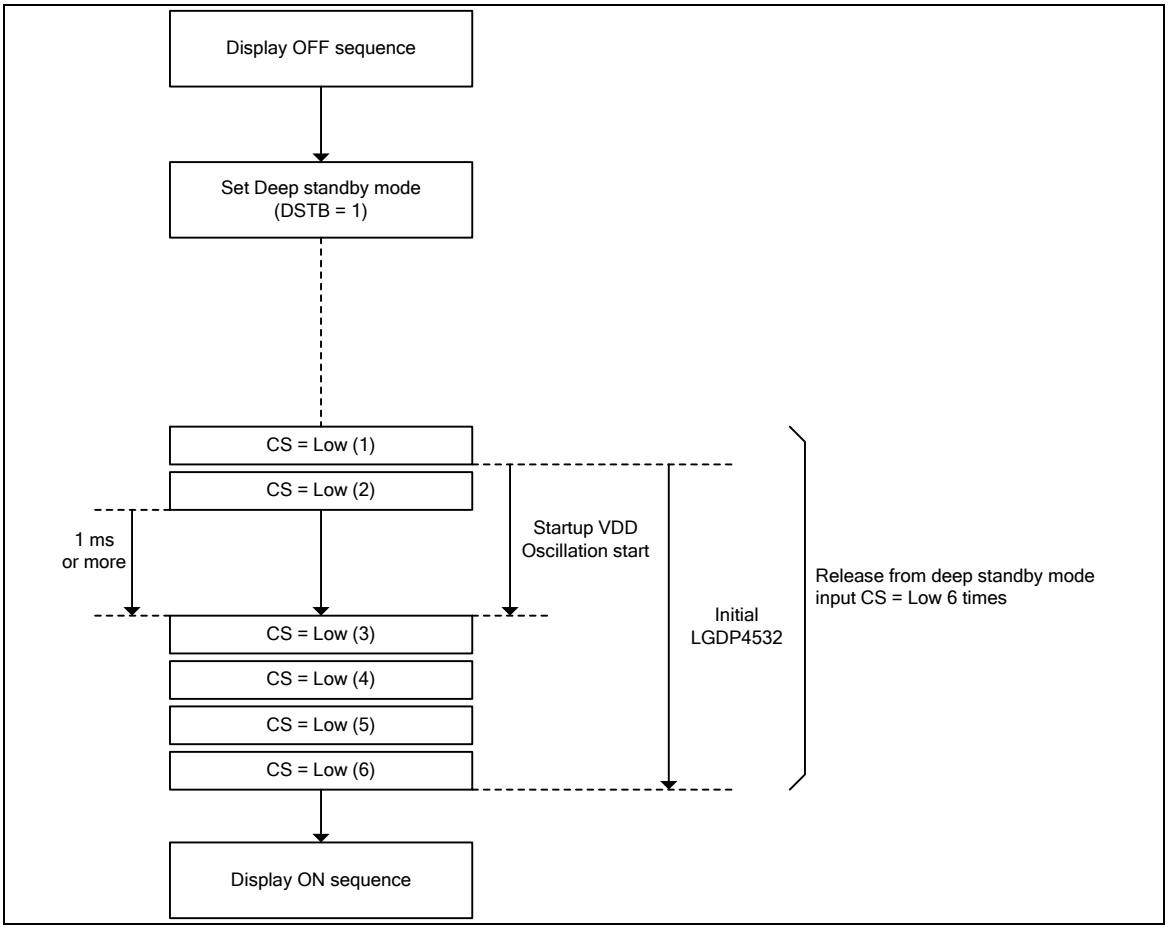


Figure 78

Note : “Display ON/OFF” sequences include “LCD Power Supply ON/OFF” sequences respectively.
See “Display ON/OFF sequence” section.

8-color mode setting

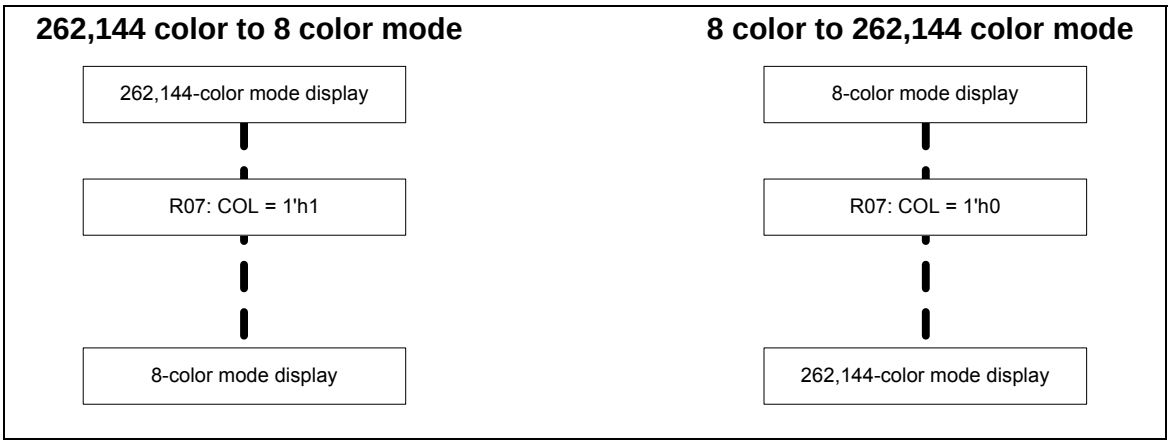


Figure 79

Parital Display setting

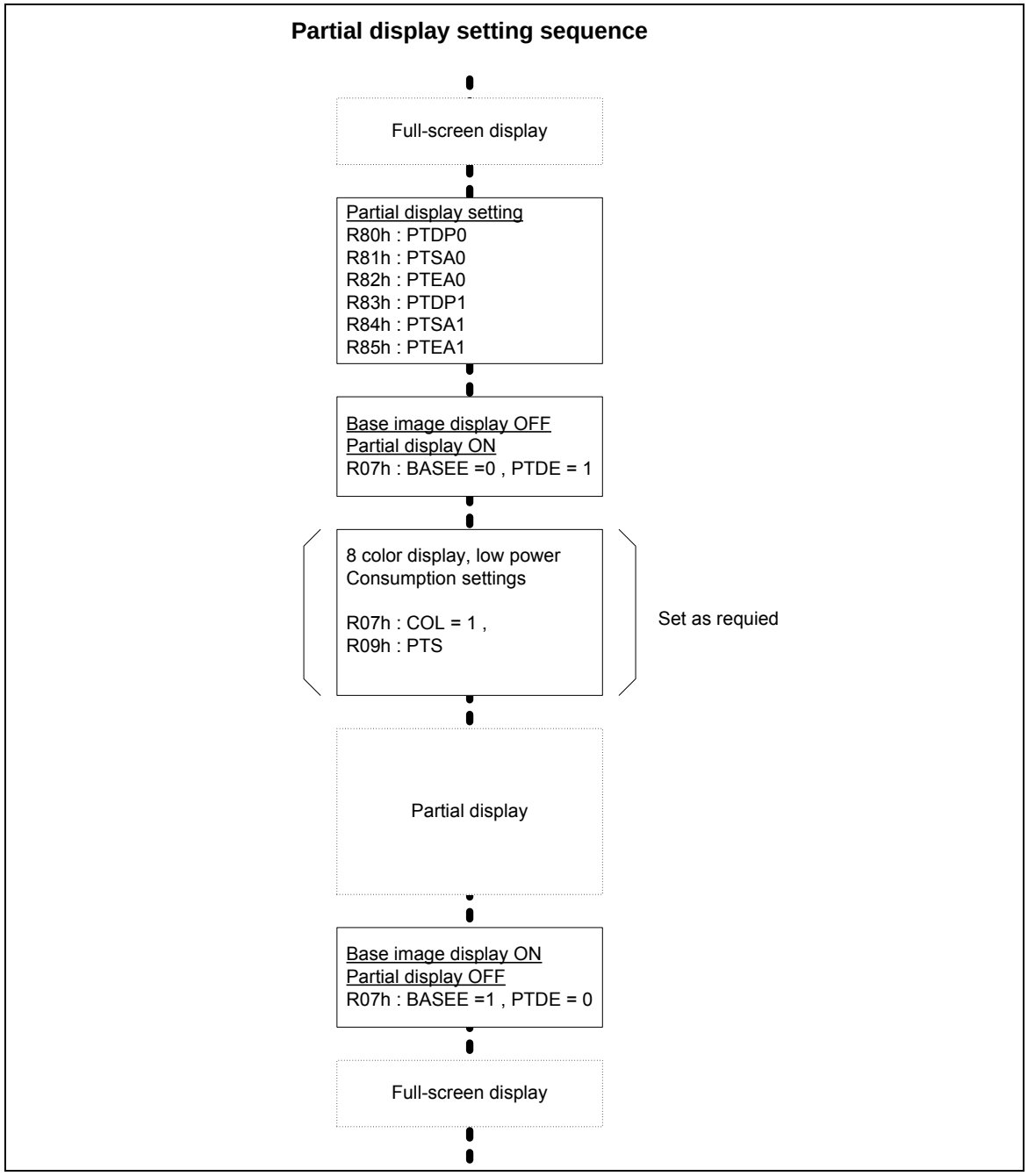


Figure 80

Absolute Maximum Ratings

Table 92

Item	Symbol	Unit	value	Notes
Power supply voltage (1)	Vcc, IOVcc	V	-0.3 ~ +4.5	1, 2
Power supply voltage (2)	Vci – AGND	V	-0.3 ~ +4.5	1, 3
Power supply voltage (3)	DDVDH – AGND	V	-0.3 ~ +8.0	1, 4
Power supply voltage (4)	AGND – VCL	V	-0.3 ~ +4.5	1
Power supply voltage (5)	DDVDH –VCL	V	-0.3 ~ +8.0	1, 5
Power supply voltage (6)	VGH – AGND	V	-0.3 ~ +18	1, 6
Power supply voltage (7)	AGND – VGL	V	-0.3 ~ +18	1, 7
Input voltage	Vt	V	-0.3~IOVcc+0.3	1
Operating temperature	Topr	˚C	-40 ~ +85	1, 8
Storage temperature	Tstg	˚C	-55 ~ +125	1

Note 1) If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.
Note 2) Make sure (High) Vcc ≥ GND (Low), (High) IOVcc ≥ GND (Low).
Note 3) Make sure (High) Vci ≥ GND (Low).
Note 4) Make sure (High) DDVDH ≥ AGND (Low).
Note 5) Make sure (High) DDVDH ≥ VCL (Low).
Note 6) Make sure (High) VGH ≥ AGND (Low).
Note 7) Make sure (High) AGND ≥ VGL (Low).
Note 8) The DC/AC characteristics of die and wafer products is guaranteed at 85 ℃.

Electrical Characteristics

DC Characteristics

Table 93

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Notes
Input high-level voltage	V_{IH}	V	IOVcc = 1.65 ~ 3.3V	0.8IOVcc		IOVcc	2,3
Input low-level voltage	V_{IL}	V	IOVcc = 1.65 ~ 3.3V	0		0.2IOVcc	2,3
Output high-level voltage (1) (DB17-0, SDO, FMARK)	V_{OH1}	V	IOVcc = 1.65 ~ 3.3V I_{OH} = 0.1mA	0.8IOVcc			2
Output lowlevel voltage (1) (DB17-0, SDO, FMARK)	V_{OL1}	V	IOVcc = 1.65~ 3.3V I_{OL} = 0.1mA			0.2IOVcc	2
I/O leakage current	I_{li}	µA	Vin = 0 ~ IOVcc	-1		1	4
Current consumption : Deep standby mode	I_{ST}	µA	IOVcc = Vcc = Vci = 2.8V , Ta ≈ 25°C		1	10	5

80-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 94 See Figure 83 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	t_{CYCW}	ns	T.B.D	T.B.D	T.B.D
		Read	t_{CYCW}	ns	T.B.D	T.B.D	T.B.D
Write “Low” level pulse width Read “Low” level pulse width		Write	PW_{LW}	ns	T.B.D	T.B.D	T.B.D
		Read	PW_{LR}	ns	T.B.D	T.B.D	T.B.D
Write “High” level pulse width Read “High” level pulse width		Write	PW_{HW}	ns	T.B.D	T.B.D	T.B.D
		Read	PW_{HR}	ns	T.B.D	T.B.D	T.B.D
Write/Read rise/fall time			t_{WRr} , t_{WRf}	ns	T.B.D	T.B.D	T.B.D
Setup time	Write (RS to CS*/ WR*)		t_{AS}	ns	T.B.D	T.B.D	T.B.D
	Read (RS to CS*/ RD*)				T.B.D	T.B.D	T.B.D
Address hold time			t_{AH}	ns	T.B.D	T.B.D	T.B.D
Write data setup time			t_{DSW}	ns	T.B.D	T.B.D	T.B.D
Write data hold time			t_{H}	ns	T.B.D	T.B.D	T.B.D
Read data delay time			t_{DDR}	ns	T.B.D	T.B.D	T.B.D
Read data hold time			t_{DHR}	ns	T.B.D	T.B.D	T.B.D

80-System Bus Interface Timing Characteristics (8/9-Bit Bus)

Table 95 See Figure 83 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	t_{CYCW}	ns	T.B.D	T.B.D	T.B.D
		Read	t_{CYCW}	ns	T.B.D	T.B.D	T.B.D
Write "Low" level pulse width Read "Low" level pulse width		Write	PW_{LW}	ns	T.B.D	T.B.D	T.B.D
		Read	PW_{LR}	ns	T.B.D	T.B.D	T.B.D
Write "High" level pulse width Read "High" level pulse width		Write	PW_{HW}	ns	T.B.D	T.B.D	T.B.D
		Read	PW_{HR}	ns	T.B.D	T.B.D	T.B.D
Write/Read rise/fall time			t_{WRr} , t_{WRf}	ns	T.B.D	T.B.D	T.B.D
Setup time	Write (RS to CS*/ WR*)		t_{AS}	ns	T.B.D	T.B.D	T.B.D
	Read (RS to CS*/ RD*)				T.B.D	T.B.D	T.B.D
Address hold time			t_{AH}	ns	T.B.D	T.B.D	T.B.D
Write data setup time			t_{DSW}	ns	T.B.D	T.B.D	T.B.D
Write data hold time			t_{H}	ns	T.B.D	T.B.D	T.B.D
Read data delay time			t_{DDR}	ns	T.B.D	T.B.D	T.B.D
Read data hold time			t_{DHR}	ns	T.B.D	T.B.D	T.B.D

Serial Peripheral Interface Timing Characteristics

Table 96 See Figure 84 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	T.B.D	T.B.D	T.B.D
	Read (transmitted)	t_{SCYC}	ns	T.B.D	T.B.D	T.B.D
Serial clock "High" level pulse width	Write (received)	t_{SCH}	ns	T.B.D	T.B.D	T.B.D
	Read (transmitted)	t_{SCH}	ns	T.B.D	T.B.D	T.B.D
Serial clock "Low" level pulse width	Write (received)	t_{SCL}	ns	T.B.D	T.B.D	T.B.D
	Read (transmitted)	t_{SCL}	ns	T.B.D	T.B.D	T.B.D
Serial clock rise/fall time		t_{scr} , t_{scf}	ns	T.B.D	T.B.D	T.B.D
Chip select setup time		t_{CSU}	ns	T.B.D	T.B.D	T.B.D
Chip select hold time		t_{CH}	ns	T.B.D	T.B.D	T.B.D
Serial input data setup time		t_{SISU}	ns	T.B.D	T.B.D	T.B.D
Serial input data hold time		t_{SIH}	ns	T.B.D	T.B.D	T.B.D
Serial output data delay time		t_{SOD}	ns	T.B.D	T.B.D	T.B.D
Serial output data hold time		t_{SOH}	ns	T.B.D	T.B.D	T.B.D

RGB Interface Timing Characteristics

Table 97 See Figure 85 (18/16-bit I/F, IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	ns	T.B.D	T.B.D	T.B.D
ENABLE setup time	tENS	ns	T.B.D	T.B.D	T.B.D
ENABLE hold time	tENH	ns	T.B.D	T.B.D	T.B.D
DOTCLK “Low” level pulse width	PWDL	ns	T.B.D	T.B.D	T.B.D
DOTCLK “High” level pulse width	PWDH	ns	T.B.D	T.B.D	T.B.D
DOTCLK cycle time	tCYCD	ns	T.B.D	T.B.D	T.B.D
Data setup time	tPDS	ns	T.B.D	T.B.D	T.B.D
Data hold time	tPDH	ns	T.B.D	T.B.D	T.B.D
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	T.B.D	T.B.D	T.B.D

Reset Timing Characteristics

Table 98 See Figure 86 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset “Low” level width	t_{RES}	ms	T.B.D	-	-
Reset rise time	t_{rRES}	us	-	-	T.B.D

LCD Driver Output Characteristics

Table 99 See Figure 87

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Driver output delay time	t_{DD}	us	Vcc=3.0V, DDVDH=5.5V, VREG1OUT=5.0V, RC oscillation: fosc =2.5MHz (driving 320 lines), Ta=25°C REV=0, SAP=010, AP=010, VRNx=5h’0, VRPx=5h’0, PKPx=3h’0, PKNx=3h’0, PRPx=3h’0, PRNx=3h’0, All pins undergo same changes from a same gray level. Time to reach ±35mV during VCOM polarity inversion. Load resistance R=10kΩ, Load capacitance C=20pF	-	T.B.D	-

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following are the configurations of I pin, I/O pin, and O pin.

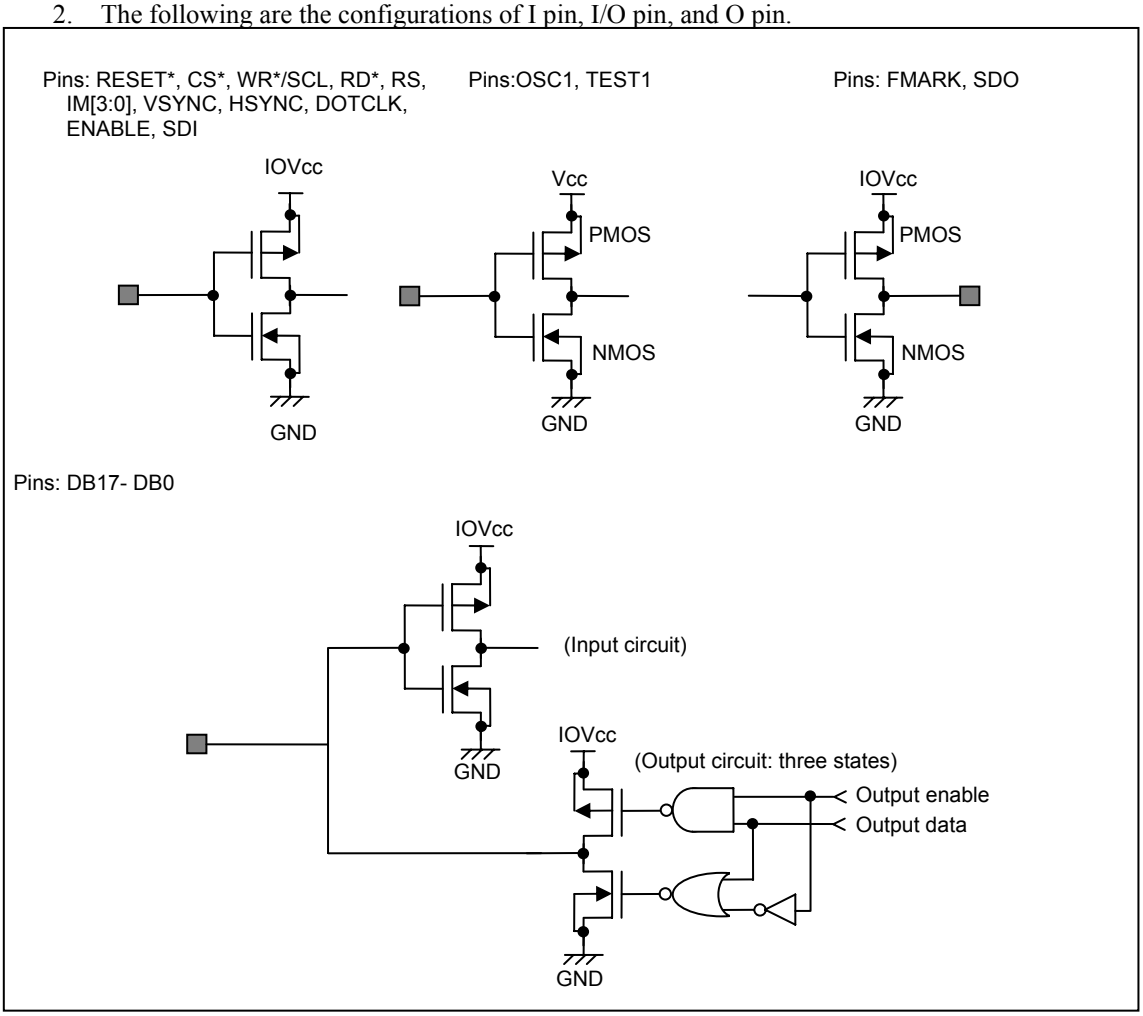


Figure 81

3. The TEST1 pin must be grounded (GND). The IM[3:0] pins must be fixed at either GND or the IOVcc level.
4. This excludes currents though the output drive MOS.
5. This excludes currents flowing through input/output units. Be sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CS* pin is set to “High” or “Low”.
6. This is the case when an external oscillation resistor Rf is used.

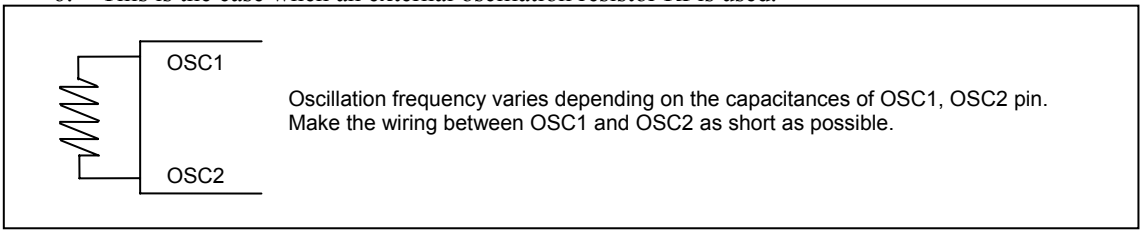
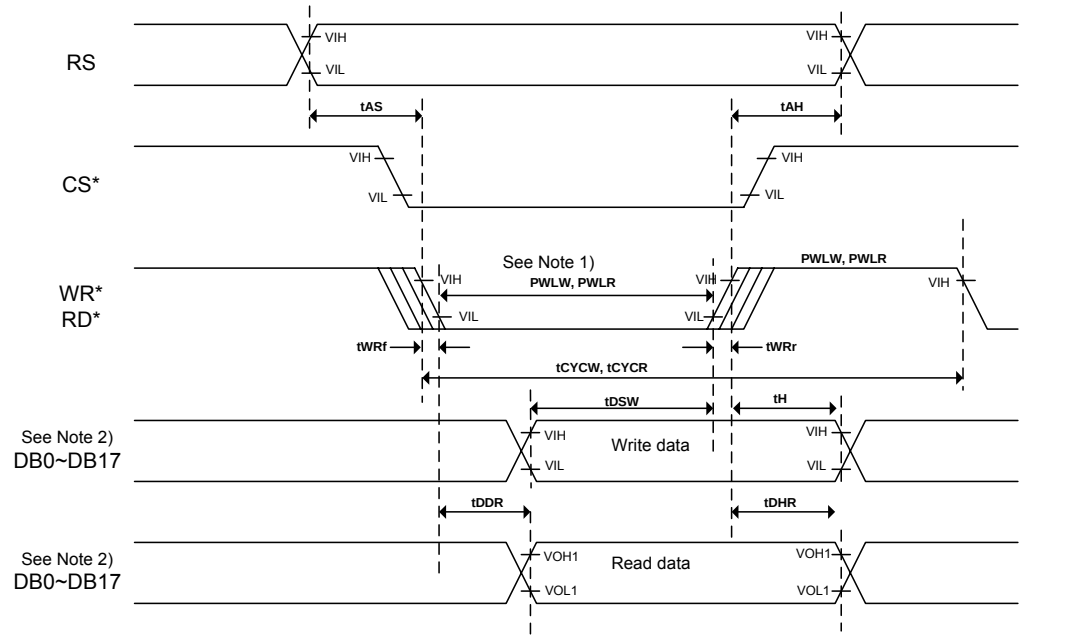


Figure 82

Table 100 Reference Data, Ta=25°C

Oscillation Resistance (kΩ)	RC Oscillation Frequency: fosc (MHz) @ VCC = 2.8V
13	T.B.D
15	T.B.D
16	T.B.D
18	T.B.D
20	T.B.D
22	T.B.D
24	T.B.D
27	T.B.D
30	T.B.D
33	T.B.D
39	T.B.D
47	T.B.D
51	T.B.D

Timing characteristic diagram



Note 1) PWLW and PWLR are defined by the overlap period when CS* is "Low" and WR* or RD* is "Low".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".

Figure 83 80-system bus interface operation

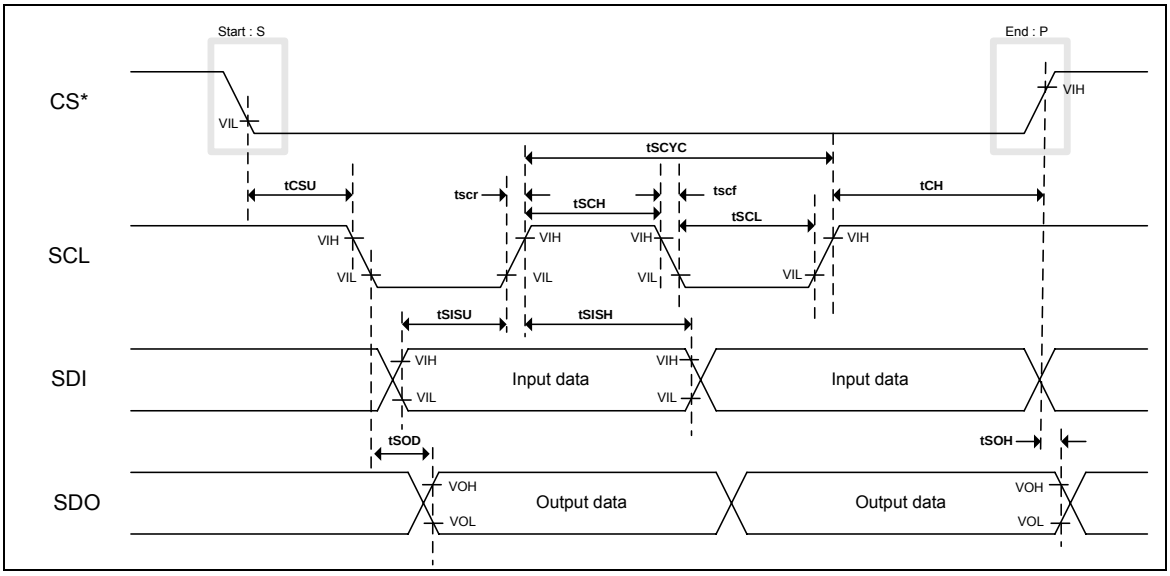


Figure 84 Serial Peripheral interface operation

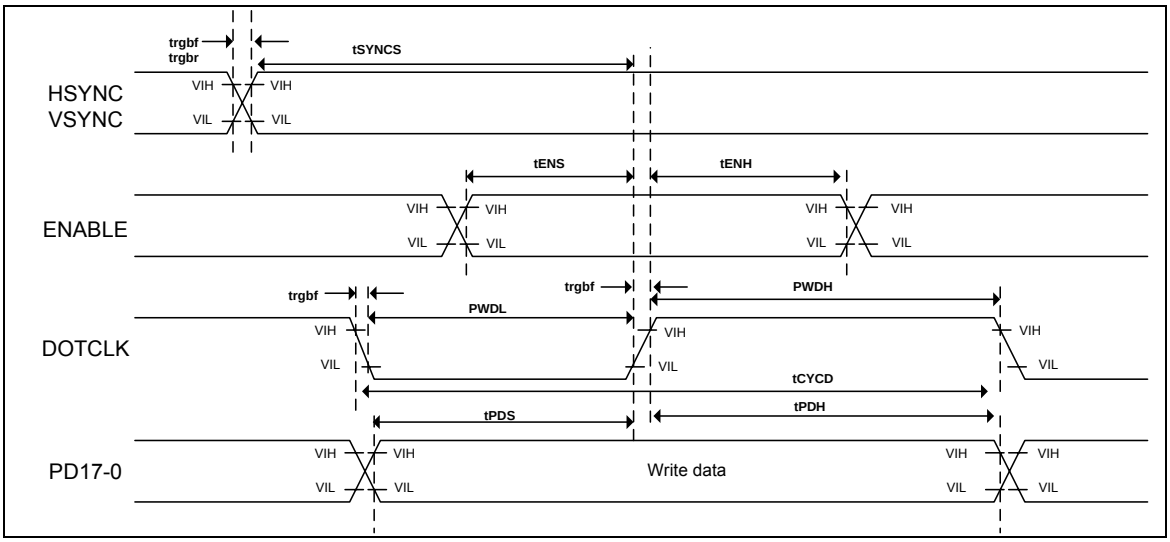


Figure 85 RGB interface operation

Figure 86 Reset operation

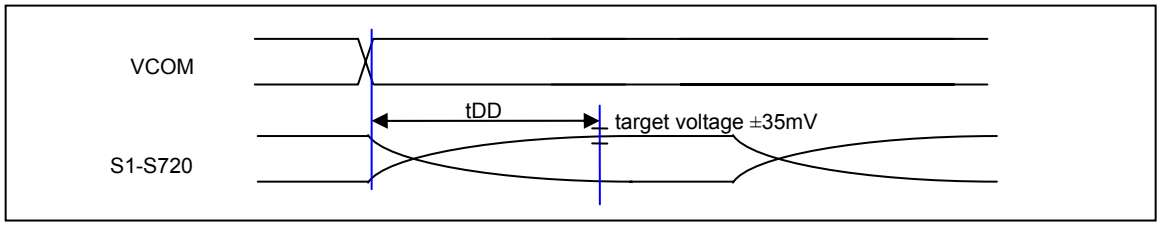


Figure 87 LCD driver outputs

Revision History

Rev.	Date	Revision Description	Revised by
0.1	2007.03.15	Preliminary release	S.H. Koh
0.11	2007.04.11	p.50 Register CMFPD, HSZ[2:0], LSZ[2:0] bits added p.141 Standby mode added : Figure 77	D.H. Kim
0.12	2007.04.19	p.58 Revised NL[5:0] : Table 48 p.145~147 Set the Interface Timing Characteristics T.B.D. : Table 94~98	D.H. Kim