ILITEK
Enrich visual experience

ILI9221

a-Si TFT LCD Single Chip Driver
176RGBx220 Resolution and 262K color

Datasheet
Preliminary

Version: V0.15
Document No.: ILI9221DS_V015.doc

ILI TECHNOLOGY CORP.
4F, No. 2, Tech. 5th Rd., Hsinchu Science Park,
Taiwan 300, R.O.C.
Tel.886-3-5670095; Fax.886-3-5670096

Table of Contents

Figures

1. Introduction

ILI9221 is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 176RGBx220 dots, comprising a 528-channel source driver, a 220-channel gate driver, 87120 bytes RAM for graphic data of 176RGBx220 dots, and power supply circuit.

ILI9221 has five kinds of system interfaces which are i80/M68-system MPU interface (8-/9-/16-/18-bit bus width), VSYNC interface (system interface + VSYNC, internal clock, DB[17:0]), serial data transfer interface (SPI) and RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

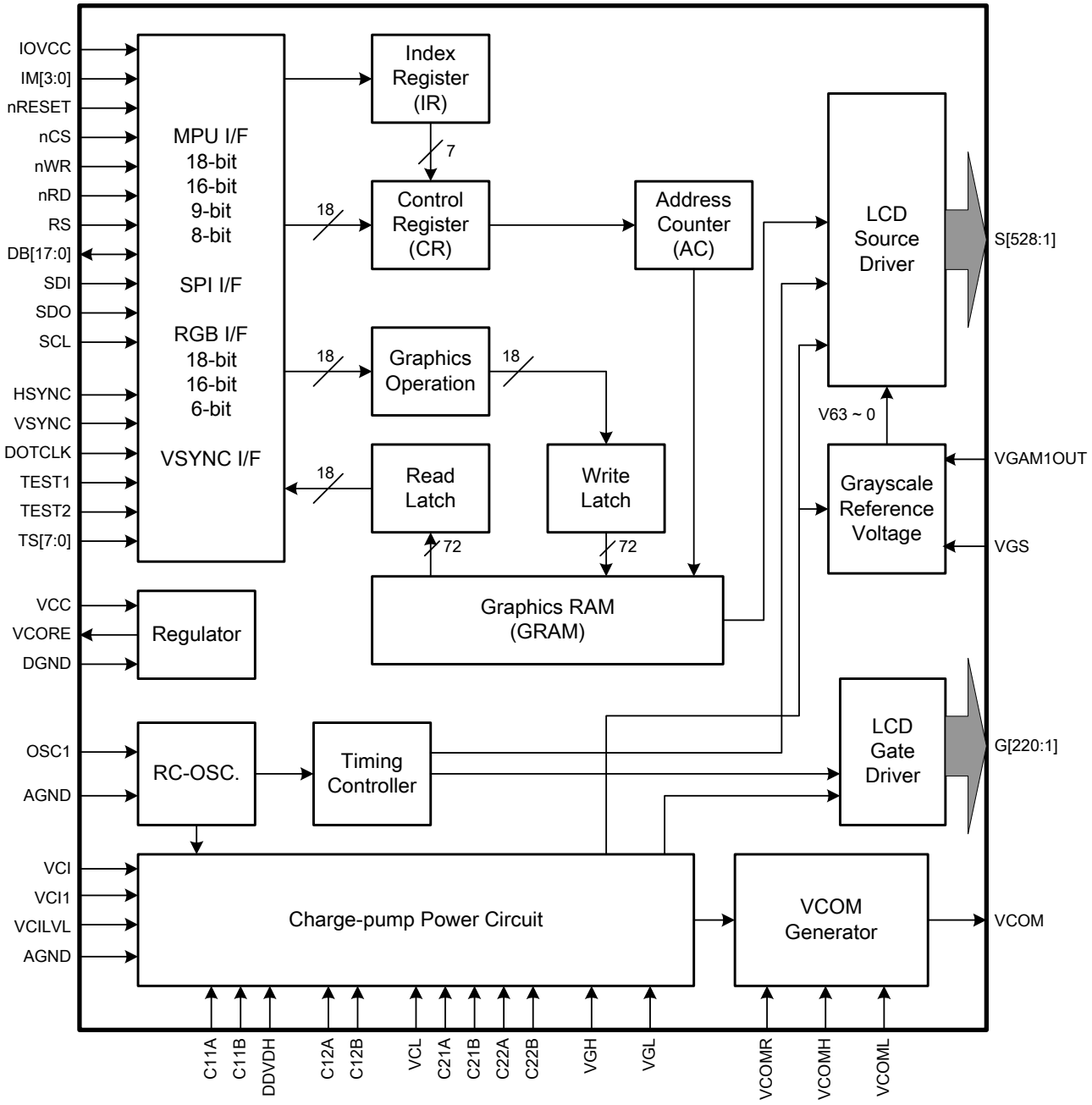
ILI9221 can operate with low I/O interface power supply up to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9221 also supports a function to display in 8 colors and a standby mode, allowing for precise power control by software. These features make the ILI9221 an ideal LCD driver for medium or small size portable products such as digital cellular phones or small PDA, where long battery life is a major concern.

2. Features

- Single chip solution for a liquid crystal QCIF+ TFT LCD display
- 176RGBx220-dot resolution capable of graphics display in 262,144 color
- Incorporate 528-channel source driver and 220-channel gate driver
- Internal 87,120 bytes graphic RAM
- High-speed RAM burst write function
- System interfaces
  - i80 system interface with 8-/ 9-/16-/18-bit bus width
  - M68 system interface with 8-/ 9-/16-/18-bit bus width
  - Serial Peripheral Interface (SPI)
  - RGB interface with 8-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - VSYNC interface (System interface + VSYNC)
- n-line liquid crystal AC drive: invert polarity at an interval of arbitrarily n lines (n: 1 ~ 64)
- Internal oscillator and hardware reset
- Reversible source/gate driver shift direction
- Window address function to specify a rectangular area for internal GRAM access
- Bit operation function for facilitating graphics data processing
  - Bit-unit write data mask function
  - Pixel-unit logical/conditional write function
- Abundant functions for color display control
  - γ-correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function

- Partial drive function, enabling partially driving an LCD panel at positions specified by user
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- Power saving functions
  - 8-color mode
  - standby mode
  - sleep mode
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVcc = 1.65 ~ 3.3 V (interface I/O)
    - Vcc = 2.4 ~ 3.3 V (internal logic)
    - Vci = 2.5 ~ 3.3 V (analog)
  - Low voltage drive: DDVDH = 4.5 ~ 5.5 V

3. Block Diagram



4. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td colspan="4">Input Interface</td></tr>
<tr><td>IM3,
IM2,
IM1,
IM0/ID</td><td>I</td><td>IOVcc</td><td>Select the MPU system interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>M68-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>M68-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>i80-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>i80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>Serial Peripheral Interface (SPI)</td><td>SDI, SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>Setting invalid</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>M68-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>M68-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i80-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i80-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting invalid</td><td></td></tr>
</table>
When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.</td></tr>
<tr><td>nCS</td><td>I</td><td>MPU
IOVcc</td><td>A chip select signal.
Low: the ILI9221 is selected and accessible
High: the ILI9221 is not selected and not accessible
Fix to the DGND level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU
IOVcc</td><td>A register select signal.
Low: select an index or status register
High: select a control register
Fix to either IOVcc or DGND level when not in use.</td></tr>
<tr><td>nWR/E/SCL</td><td>I</td><td>MPU
IOVcc</td><td>A write strobe signal and enables an operation to write data when the signal is low.
Fix to either IOVcc or DGND level when not in use.

SPI Mode:
A synchronizing clock signal in SPI mode.</td></tr>
<tr><td>nRD/RW</td><td>I</td><td>MPU
IOVcc</td><td>A read strobe signal and enables an operation to read out data when the signal is low.
Fix to either IOVcc or DGND level when not in use.</td></tr>
<tr><td>nRESET</td><td>I</td><td>MPU
IOVcc</td><td>A reset pin.
Initializes the ILI9221 with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>MPU
IOVcc</td><td>An 18-bit parallel bi-directional data bus for MPU system interface mode
8-bit I/F: DB[17:10] is used.
9-bit I/F: DB[17:9] is used.
16-bit I/F: DB[17:10] and DB[8:1] is used.
18-bit I/F: DB[17:0] is used.

Unused pins must be fixed either IOVcc or DGND level.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU
IOVcc</td><td>Serial data input (SDI) pin in serial interface operation. The data is latched on the rising edge of the SCL signal.

When the SPI interface is not used, the SDI shall be connected to either IOVcc or DGND level.</td></tr>
</table>

Pin Name	I/O	Type	Descriptions
SDO	O	MPU IOVcc	Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. When the SPI interface is not used, please let SDO as floating.
DOTCLK	I	MPU IOVcc	A dot clock signal. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK Fix to the IOVcc level when not in use
VSYNC	I	MPU IOVcc	A frame synchronizing signal. VSPL = "0": Active low. VSPL = "1": Active high. Fix to the IOVcc level when not in use.
HSYNC	I	MPU IOVcc	A line synchronizing signal. HSPL = "0": Active low. HSPL = "1": Active high. Fix to the IOVcc level when not in use
ENABLE	I	MPU IOVcc	A data ENEABLE signal in RGB interface mode. Low: Select (access enabled) High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVcc or DGND level when not in use.
FLM	O	MPU IOVcc	Output a frame head pulse signal. The FLM signal is used when writing RAM data in synchronization with frame. Leave the pin open when not in use.
LCD Driving signals			
S528~S1	O	LCD	Source output voltage signals applied to liquid crystal. To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "h00000" is output from S1. SS = "1", the data in the RAM address "h00000" is output from S528. S1, S4, S7, … display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G220~G1	O	LCD	Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines
VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.
Charge-pump and Regulator Circuit			
VCOMH	O	Stabilizing capacitor	The high level of VCOM AC voltage. Connect to a stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The low level of VCOM AC voltage. Adjust the VCOML level with the VDV bits. Connect to a stabilizing capacitor. To fix the VCOML level to AGND and set VCOMG = "0". In this case, capacitor connection is not necessary.
VCOMR	I	Variable resistor or open	A reference level to generate the VCOMH level either with an externally connected variable resistor or by setting the register of the ILI9221. When using a variable resistor, halt the internal VCOMH adjusting circuit by setting the register and place the resister between VGAM1OUT and AGND. When generating the VCOMH level by setting the register, leave this pin open.
C11A, C11B	-	Step-up capacitor	Pins to connect capacitors for the internal step-up circuit 1. Leave the pins open when not using the step-up circuit 1.
C12A, C12B C21A, C21B C22A, C22B	-	Step-up capacitor	Pins to connect capacitors for the internal step-up circuit 2. Connect a capacitor according to step-up rate. Leave the pins open when not using the step-up circuit 2.
OSC1	I	Oscillation resistor	Connect an external resistor for generating internal clock by internal R-C oscillation, or an external clock signal is supplied through OSC1.

Pin Name	I/O	Type	Descriptions
VciLVL	I	Power supply	A reference level to generate the VCI1/REGP level according to the step-up rate set with the VC[2:0] bits. Be sure to connect VciLVL with Vci on the FPC to prevent noise.
VCI1	O	Stabilizing capacitor Vci1	An internal reference voltage for the step-up circuit1. The amplitude between Vci and DGND is determined by the VC[2:0] bits. When not using an internal reference voltage, please connect this pin to a external voltage (less than 2.75V).
DDVDH	O	Stabilizing capacitor, DDVDH	An output voltage from the step-up circuit 1, twice the Vci1 level. Place a stabilizing capacitor between AGND. Place a shottkey diode between Vci and DDVDH. See "Configurations of Power supply circuit". DDVDH = 4.5 ~ 5.5V
VGH	O	Stabilizing capacitor, VGH	An output voltage from the step-up circuit 2, 4 ~ 6 times the Vci1 level. The step-up rate is set with the BT bits. Place a stabilizing capacitor between AGND. Place a shottkey diode between Vci. See "Configurations of Power supply circuit". VGH = max 16.5V
VGL	O	Stabilizing capacitor, VGL	An output voltage from the step-up circuit 2, -3 ~ -5 times the Vci1 level. The step-up rate is set with the BT bits. Place a stabilizing capacitor between AGND. Place a shottkey diode between Vci. See "Configurations of Power supply circuit". VGL = min –16.5V
VCL	O	Stabilizing capacitor, VCL	An output voltage from the step-up circuit 2, –1 time the Vci1 level. Connect to a stabilizing capacitor. VCLC = 0 ~ –3.3V
VGAM1OUT	I/O	Stabilizing capacitor or power supply	A voltage level of DDVDH-AGND, generated from the reference level of Vci-AGND according to the rate set with the VRH[3:0] bits. VGAM1OUT is (1) a source driver grayscale reference voltage VDH, (2) a VCOMH level reference voltage, and (3) a VCOM amplitude reference voltage. Connect to a stabilizing capacitor. VGAM1OUT = 3.0 ~ (DDVDH – 0.5)V
VGS	I	AGND or external resistor	A reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
Power Pads			
VCC	I	Power supply	A supply voltage to the internal logic: Vcc = 2.4~3.3V
IOVCC	I	Power supply	A supply voltage to the interface pins (IOVcc = 1.65 ~ 3.3V). IOVcc and the internal logic voltage Vcc must be supplied in the same condition. In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.
VCI	I	Power supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V.
VCORE	O	Power	Digital core power pad. Connect them with the 1uF capacitor.
DGND	I	Power supply	DGND for the logic side: DGND = 0V.
AGND	I	Power supply	AGND for the analog side: AGND = 0V. In case of COG, connect to DGND on the FPC to prevent noise.
IOVCCDUM1~2	O	P	Output the IOVcc voltage level. When adjacent pins are needed to pull high, tie these pins to IOVCCDUM1 and IOVCCDUM2.
IOVSSDDUM1~2	O	P	Output the DGND voltage level. When adjacent pins are needed to pull low, tie these pins to IOVSSDDUM1and IOVSSDDUM2.
Test Pads			
TEST1	I	Open	A test pin. This pin is internal pull down to DGND.
TEST2	I	Open	A test pin. This pin is internal pull down to DGND.
TS[7:0]	O	Open	Test pins, disconnect them.

Pin Name	I/O	Type	Descriptions
DUMMY1~ 40	O	Open	Dummy pads. Leave them open.
DUMMYR1~ 10	O	Open	Dummy pads. Leave them open.
NCPAD	-	Open	No connected pad. Leave them open.
POSC[2:0]	-	Open	Test pins. Leave them open.
TESTO[25:32]	-	Open	Test pins. Leave them open.
VGLDMY[4:1]	-	Open	Test pins. Leave them open.
TESTO[25:32]	-	Open	Test pins. Leave them open.

Liquid crystal power supply specifications Table 1

No.	Item		Description
1	TFT data lines		528 pins (176 x RGB)
2	TFT gate lines		220 pins
3	TFT display's capacitor structure		Cst structure only (Common VCOM)
4	Liquid crystal drive output	S1 ~ S528	V0 ~ V63 grayscales
		G1 ~ G220	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes VCOMH=VCOMR: Adjusted with an external resistor
5	Input voltage	IOVcc	1.65 ~ 3.30V
		Vcc	2.40 ~ 3.30V
		Vci	2.50 ~ 3.30V
6	Internal step-up circuits	DDVDH	Vci x 2
		VGH	Vci x 4, x 5, x 6
		VGL	Vci x -3, x -4, x -5
		VCL	Vci x -1

5. Pad Arrangement and Coordination

Chip Size: 17200um x 1250um

Chip thickness : 400 um (typ.)

Pad Location: Pad Center.

Coordinate Origin: Not chip center **(0, 65.5um)**

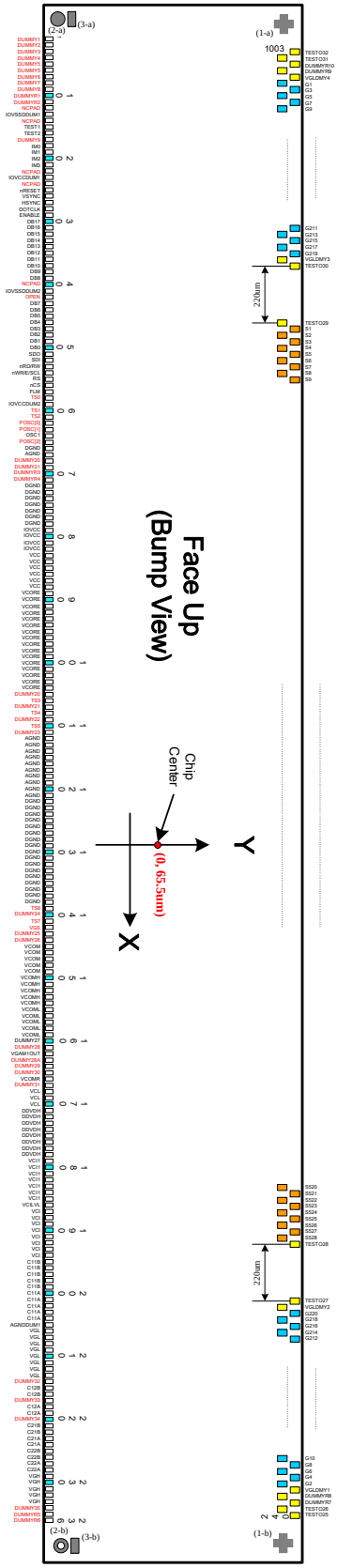
Au bump height: 15um (typ.)

Au Bump Size:

1. 19um x 120um (No. 240 ~ 1003)
   Gate: G1 ~ G220
   Source: S1 ~ S528

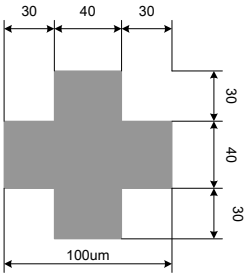
2. 50um x 80um (No. 1 ~ 236)
   Input Pads
   Pad 1 to 236.

3. 80um x 50um
   No: 237~ 241 and 1006~1010

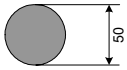


Alignment Marks

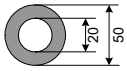
Alignment Mark: 1-a, 1-b.



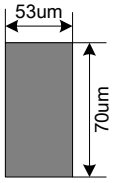
Alignment Mark: 2-a.



Alignment Mark: 2-b.



Alignment Mark: 3-a, 3-b.



No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY1	-8225	-454.5	61	TS2	-4025	-454.5	121	AGND	175	-454.5	181	VCI1	4375	-454.5	241	TESTO26	8189.5	411.5
2	DUMMY2	-8155	-454.5	62	POSC[0]	-3955	-454.5	122	DGND	245	-454.5	182	VCI1	4445	-454.5	242	DUMMYR7	8168.5	566.5
3	DUMMY3	-8085	-454.5	63	POSC[1]	-3885	-454.5	123	DGND	315	-454.5	183	VCI1	4515	-454.5	243	DUMMYR8	8147.5	411.5
4	DUMMY4	-8015	-454.5	64	OSC1	-3815	-454.5	124	DGND	385	-454.5	184	VCI1	4585	-454.5	244	VGLDMY1	8126.5	566.5
5	DUMMY5	-7945	-454.5	65	POSC[2]	-3745	-454.5	125	DGND	455	-454.5	185	VCI1	4655	-454.5	245	G2	8105.5	411.5
6	DUMMY5	-7875	-454.5	66	DGND	-3675	-454.5	126	DGND	525	-454.5	186	VCILVL	4725	-454.5	246	G4	8084.5	566.5
7	DUMMY6	-7805	-454.5	67	AGND	-3605	-454.5	127	DGND	595	-454.5	187	VCI	4795	-454.5	247	G6	8063.5	411.5
8	DUMMY7	-7735	-454.5	68	DUMMY20	-3535	-454.5	128	DGND	665	-454.5	188	VCI	4865	-454.5	248	G8	8042.5	566.5
9	DUMMY8	-7665	-454.5	69	DUMMY21	-3465	-454.5	129	DGND	735	-454.5	189	VCI	4935	-454.5	249	G10	8021.5	411.5
10	DUMMYR1	-7595	-454.5	70	DUMMYR3	-3395	-454.5	130	DGND	805	-454.5	190	VCI	5005	-454.5	250	G12	8000.5	566.5
11	DUMMYR2	-7525	-454.5	71	DUMMYR4	-3325	-454.5	131	DGND	875	-454.5	191	VCI	5075	-454.5	251	G14	7979.5	411.5
12	OPEN	-7455	-454.5	72	DGND	-3255	-454.5	132	DGND	945	-454.5	192	VCI	5145	-454.5	252	G16	7958.5	566.5
13	IOVSSDDUM1	-7385	-454.5	73	DGND	-3185	-454.5	133	DGND	1015	-454.5	193	VCI	5215	-454.5	253	G18	7937.5	411.5
14	OPEN	-7315	-454.5	74	DGND	-3115	-454.5	134	DGND	1085	-454.5	194	VCI	5285	-454.5	254	G20	7916.5	566.5
15	TEST1	-7245	-454.5	75	DGND	-3045	-454.5	135	DGND	1155	-454.5	195	C11B	5355	-454.5	255	G22	7895.5	411.5
16	TEST2	-7175	-454.5	76	DGND	-2975	-454.5	136	DGND	1225	-454.5	196	C11B	5425	-454.5	256	G24	7874.5	566.5
17	DUMMY9	-7105	-454.5	77	DGND	-2905	-454.5	137	DGND	1295	-454.5	197	C11B	5495	-454.5	257	G26	7853.5	411.5
18	IM0	-7035	-454.5	78	DGND	-2835	-454.5	138	DGND	1365	-454.5	198	C11B	5565	-454.5	258	G28	7832.5	566.5
19	IM1	-6965	-454.5	79	IOVCC	-2765	-454.5	139	TS6	1435	-454.5	199	C11B	5635	-454.5	259	G30	7811.5	411.5
20	IM2	-6895	-454.5	80	IOVCC	-2695	-454.5	140	DUMMY24	1505	-454.5	200	C11A	5705	-454.5	260	G32	7790.5	566.5
21	IM3	-6825	-454.5	81	IOVCC	-2625	-454.5	141	TS7	1575	-454.5	201	C11A	5775	-454.5	261	G34	7769.5	411.5
22	OPEN	-6755	-454.5	82	IOVCC	-2555	-454.5	142	VGS	1645	-454.5	202	C11A	5845	-454.5	262	G36	7748.5	566.5
23	IOVCCDUM1	-6685	-454.5	83	VCC	-2485	-454.5	143	DUMMY25	1715	-454.5	203	C11A	5915	-454.5	263	G38	7727.5	411.5
24	OPEN	-6615	-454.5	84	VCC	-2415	-454.5	144	DUMMY26	1785	-454.5	204	C11A	5985	-454.5	264	G40	7706.5	566.5
25	nRESET	-6545	-454.5	85	VCC	-2345	-454.5	145	VCOM	1855	-454.5	205	AGNDDUM1	6055	-454.5	265	G42	7685.5	411.5
26	VSYNC	-6475	-454.5	86	VCC	-2275	-454.5	146	VCOM	1925	-454.5	206	VGL	6125	-454.5	266	G44	7664.5	566.5
27	HSYNC	-6405	-454.5	87	VCC	-2205	-454.5	147	VCOM	1995	-454.5	207	VGL	6195	-454.5	267	G46	7643.5	411.5
28	DOTCLK	-6335	-454.5	88	VCC	-2135	-454.5	148	VCOM	2065	-454.5	208	VGL	6265	-454.5	268	G48	7622.5	566.5
29	ENABLE	-6265	-454.5	89	VCORE	-2065	-454.5	149	VCOM	2135	-454.5	209	VGL	6335	-454.5	269	G50	7601.5	411.5
30	DB17	-6195	-454.5	90	VCORE	-1995	-454.5	150	VCOMH	2205	-454.5	210	VGL	6405	-454.5	270	G52	7580.5	566.5
31	DB16	-6125	-454.5	91	VCORE	-1925	-454.5	151	VCOMH	2275	-454.5	211	VGL	6475	-454.5	271	G54	7559.5	411.5
32	DB15	-6055	-454.5	92	VCORE	-1855	-454.5	152	VCOMH	2345	-454.5	212	VGL	6545	-454.5	272	G56	7538.5	566.5
33	DB14	-5985	-454.5	93	VCORE	-1785	-454.5	153	VCOMH	2415	-454.5	213	VGL	6615	-454.5	273	G58	7517.5	411.5
34	DB13	-5915	-454.5	94	VCORE	-1715	-454.5	154	VCOMH	2485	-454.5	214	DUMMY32	6685	-454.5	274	G60	7496.5	566.5
35	DB12	-5845	-454.5	95	VCORE	-1645	-454.5	155	VCOML	2555	-454.5	215	C12B	6755	-454.5	275	G62	7475.5	411.5
36	DB11	-5775	-454.5	96	VCORE	-1575	-454.5	156	VCOML	2625	-454.5	216	C12B	6825	-454.5	276	G64	7454.5	566.5
37	DB10	-5705	-454.5	97	VCORE	-1505	-454.5	157	VCOML	2695	-454.5	217	DUMMY33	6895	-454.5	277	G66	7433.5	411.5
38	DB9	-5635	-454.5	98	VCORE	-1435	-454.5	158	VCOML	2765	-454.5	218	C12A	6965	-454.5	278	G68	7412.5	566.5
39	DB8	-5565	-454.5	99	VCORE	-1365	-454.5	159	VCOML	2835	-454.5	219	C12A	7035	-454.5	279	G70	7391.5	411.5
40	OPEN	-5495	-454.5	100	VCORE	-1295	-454.5	160	DUMMY27	2905	-454.5	220	DUMMY34	7105	-454.5	280	G72	7370.5	566.5
41	IOVSSDDUM2	-5425	-454.5	101	VCORE	-1225	-454.5	161	DUMMY28	2975	-454.5	221	C21B	7175	-454.5	281	G74	7349.5	411.5
42	OPEN	-5355	-454.5	102	VCORE	-1155	-454.5	162	VGAM1OUT	3045	-454.5	222	C21B	7245	-454.5	282	G76	7328.5	566.5
43	DB7	-5285	-454.5	103	VCORE	-1085	-454.5	163	DUMMY28A	3115	-454.5	223	C21A	7315	-454.5	283	G78	7307.5	411.5
44	DB6	-5215	-454.5	104	VCORE	-1015	-454.5	164	DUMMY29	3185	-454.5	224	C21A	7385	-454.5	284	G80	7286.5	566.5
45	DB5	-5145	-454.5	105	DUMMY20	-945	-454.5	165	DUMMY30	3255	-454.5	225	C22B	7455	-454.5	285	G82	7265.5	411.5
46	DB4	-5075	-454.5	106	TS3	-875	-454.5	166	VCOMR	3325	-454.5	226	C22B	7525	-454.5	286	G84	7244.5	566.5
47	DB3	-5005	-454.5	107	DUMMY21	-805	-454.5	167	DUMMY31	3395	-454.5	227	C22A	7595	-454.5	287	G86	7223.5	411.5
48	DB2	-4935	-454.5	108	TS4	-735	-454.5	168	VCL	3465	-454.5	228	C22A	7665	-454.5	288	G88	7202.5	566.5
49	DB1	-4865	-454.5	109	DUMMY22	-665	-454.5	169	VCL	3535	-454.5	229	VGH	7735	-454.5	289	G90	7181.5	411.5
50	DB0	-4795	-454.5	110	TS5	-595	-454.5	170	VCL	3605	-454.5	230	VGH	7805	-454.5	290	G92	7160.5	566.5
51	SDO	-4725	-454.5	111	DUMMY23	-525	-454.5	171	DDVDH	3675	-454.5	231	VGH	7875	-454.5	291	G94	7139.5	411.5
52	SDI	-4655	-454.5	112	AGND	-455	-454.5	172	DDVDH	3745	-454.5	232	VGH	7945	-454.5	292	G96	7118.5	566.5
53	nRD/RW	-4585	-454.5	113	AGND	-385	-454.5	173	DDVDH	3815	-454.5	233	VGH	8015	-454.5	293	G98	7097.5	411.5
54	nWR/E/SCL	-4515	-454.5	114	AGND	-315	-454.5	174	DDVDH	3885	-454.5	234	DUMMY35	8085	-454.5	294	G100	7076.5	566.5
55	RS	-4445	-454.5	115	AGND	-245	-454.5	175	DDVDH	3955	-454.5	235	DUMMYR5	8155	-454.5	295	G102	7055.5	411.5
56	NCS	-4375	-454.5	116	AGND	-175	-454.5	176	DDVDH	4025	-454.5	236	DUMMYR6	8225	-454.5	296	G104	7034.5	566.5
57	FLM	-4305	-454.5	117	AGND	-105	-454.5	177	DDVDH	4095	-454.5	237				297	G106	7013.5	411.5
58	TS0	-4235	-454.5	118	AGND	-35	-454.5	178	DDVDH	4165	-454.5	238				298	G108	6992.5	566.5
59	IOVCCDUM2	-4165	-454.5	119	AGND	35	-454.5	179	VCI1	4235	-454.5	239				299	G110	6971.5	411.5
60	TS1	-4095	-454.5	120	AGND	105	-454.5	180	VCI1	4305	-454.5	240	TESTO25	8210.5	566.5	300	G112	6950.5	566.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
301	G114	6929.5	411.5	361	S525	5470.5	566.5	421	S465	4210.5	566.5	481	S405	2950.5	566.5	541	S345	1690.5	566.5
302	G116	6908.5	566.5	362	S524	5449.5	411.5	422	S464	4189.5	411.5	482	S404	2929.5	411.5	542	S344	1669.5	411.5
303	G118	6887.5	411.5	363	S523	5428.5	566.5	423	S463	4168.5	566.5	483	S403	2908.5	566.5	543	S343	1648.5	566.5
304	G120	6866.5	566.5	364	S522	5407.5	411.5	424	S462	4147.5	411.5	484	S402	2887.5	411.5	544	S342	1627.5	411.5
305	G122	6845.5	411.5	365	S521	5386.5	566.5	425	S461	4126.5	566.5	485	S401	2866.5	566.5	545	S341	1606.5	566.5
306	G124	6824.5	566.5	366	S520	5365.5	411.5	426	S460	4105.5	411.5	486	S400	2845.5	411.5	546	S340	1585.5	411.5
307	G126	6803.5	411.5	367	S519	5344.5	566.5	427	S459	4084.5	566.5	487	S399	2824.5	566.5	547	S339	1564.5	566.5
308	G128	6782.5	566.5	368	S518	5323.5	411.5	428	S458	4063.5	411.5	488	S398	2803.5	411.5	548	S338	1543.5	411.5
309	G130	6761.5	411.5	369	S517	5302.5	566.5	429	S457	4042.5	566.5	489	S397	2782.5	566.5	549	S337	1522.5	566.5
310	G132	6740.5	566.5	370	S516	5281.5	411.5	430	S456	4021.5	411.5	490	S396	2761.5	411.5	550	S336	1501.5	411.5
311	G134	6719.5	411.5	371	S515	5260.5	566.5	431	S455	4000.5	566.5	491	S395	2740.5	566.5	551	S335	1480.5	566.5
312	G136	6698.5	566.5	372	S514	5239.5	411.5	432	S454	3979.5	411.5	492	S394	2719.5	411.5	552	S334	1459.5	411.5
313	G138	6677.5	411.5	373	S513	5218.5	566.5	433	S453	3958.5	566.5	493	S393	2698.5	566.5	553	S333	1438.5	566.5
314	G140	6656.5	566.5	374	S512	5197.5	411.5	434	S452	3937.5	411.5	494	S392	2677.5	411.5	554	S332	1417.5	411.5
315	G142	6635.5	411.5	375	S511	5176.5	566.5	435	S451	3916.5	566.5	495	S391	2656.5	566.5	555	S331	1396.5	566.5
316	G144	6614.5	566.5	376	S510	5155.5	411.5	436	S450	3895.5	411.5	496	S390	2635.5	411.5	556	S330	1375.5	411.5
317	G146	6593.5	411.5	377	S509	5134.5	566.5	437	S449	3874.5	566.5	497	S389	2614.5	566.5	557	S329	1354.5	566.5
318	G148	6572.5	566.5	378	S508	5113.5	411.5	438	S448	3853.5	411.5	498	S388	2593.5	411.5	558	S328	1333.5	411.5
319	G150	6551.5	411.5	379	S507	5092.5	566.5	439	S447	3832.5	566.5	499	S387	2572.5	566.5	559	S327	1312.5	566.5
320	G152	6530.5	566.5	380	S506	5071.5	411.5	440	S446	3811.5	411.5	500	S386	2551.5	411.5	560	S326	1291.5	411.5
321	G154	6509.5	411.5	381	S505	5050.5	566.5	441	S445	3790.5	566.5	501	S385	2530.5	566.5	561	S325	1270.5	566.5
322	G156	6488.5	566.5	382	S504	5029.5	411.5	442	S444	3769.5	411.5	502	S384	2509.5	411.5	562	S324	1249.5	411.5
323	G158	6467.5	411.5	383	S503	5008.5	566.5	443	S443	3748.5	566.5	503	S383	2488.5	566.5	563	S323	1228.5	566.5
324	G160	6446.5	566.5	384	S502	4987.5	411.5	444	S442	3727.5	411.5	504	S382	2467.5	411.5	564	S322	1207.5	411.5
325	G162	6425.5	411.5	385	S501	4966.5	566.5	445	S441	3706.5	566.5	505	S381	2446.5	566.5	565	S321	1186.5	566.5
326	G164	6404.5	566.5	386	S500	4945.5	411.5	446	S440	3685.5	411.5	506	S380	2425.5	411.5	566	S320	1165.5	411.5
327	G166	6383.5	411.5	387	S499	4924.5	566.5	447	S439	3664.5	566.5	507	S379	2404.5	566.5	567	S319	1144.5	566.5
328	G168	6362.5	566.5	388	S498	4903.5	411.5	448	S438	3643.5	411.5	508	S378	2383.5	411.5	568	S318	1123.5	411.5
329	G170	6341.5	411.5	389	S497	4882.5	566.5	449	S437	3622.5	566.5	509	S377	2362.5	566.5	569	S317	1102.5	566.5
330	G172	6320.5	566.5	390	S496	4861.5	411.5	450	S436	3601.5	411.5	510	S376	2341.5	411.5	570	S316	1081.5	411.5
331	G174	6299.5	411.5	391	S495	4840.5	566.5	451	S435	3580.5	566.5	511	S375	2320.5	566.5	571	S315	1060.5	566.5
332	G176	6278.5	566.5	392	S494	4819.5	411.5	452	S434	3559.5	411.5	512	S374	2299.5	411.5	572	S314	1039.5	411.5
333	G178	6257.5	411.5	393	S493	4798.5	566.5	453	S433	3538.5	566.5	513	S373	2278.5	566.5	573	S313	1018.5	566.5
334	G180	6236.5	566.5	394	S492	4777.5	411.5	454	S432	3517.5	411.5	514	S372	2257.5	411.5	574	S312	997.5	411.5
335	G182	6215.5	411.5	395	S491	4756.5	566.5	455	S431	3496.5	566.5	515	S371	2236.5	566.5	575	S311	976.5	566.5
336	G184	6194.5	566.5	396	S490	4735.5	411.5	456	S430	3475.5	411.5	516	S370	2215.5	411.5	576	S310	955.5	411.5
337	G186	6173.5	411.5	397	S489	4714.5	566.5	457	S429	3454.5	566.5	517	S369	2194.5	566.5	577	S309	934.5	566.5
338	G188	6152.5	566.5	398	S488	4693.5	411.5	458	S428	3433.5	411.5	518	S368	2173.5	411.5	578	S308	913.5	411.5
339	G190	6131.5	411.5	399	S487	4672.5	566.5	459	S427	3412.5	566.5	519	S367	2152.5	566.5	579	S307	892.5	566.5
340	G192	6110.5	566.5	400	S486	4651.5	411.5	460	S426	3391.5	411.5	520	S366	2131.5	411.5	580	S306	871.5	411.5
341	G194	6089.5	411.5	401	S485	4630.5	566.5	461	S425	3370.5	566.5	521	S365	2110.5	566.5	581	S305	850.5	566.5
342	G196	6068.5	566.5	402	S484	4609.5	411.5	462	S424	3349.5	411.5	522	S364	2089.5	411.5	582	S304	829.5	411.5
343	G198	6047.5	411.5	403	S483	4588.5	566.5	463	S423	3328.5	566.5	523	S363	2068.5	566.5	583	S303	808.5	566.5
344	G200	6026.5	566.5	404	S482	4567.5	411.5	464	S422	3307.5	411.5	524	S362	2047.5	411.5	584	S302	787.5	411.5
345	G202	6005.5	411.5	405	S481	4546.5	566.5	465	S421	3286.5	566.5	525	S361	2026.5	566.5	585	S301	766.5	566.5
346	G204	5984.5	566.5	406	S480	4525.5	411.5	466	S420	3265.5	411.5	526	S360	2005.5	411.5	586	S300	745.5	411.5
347	G206	5963.5	411.5	407	S479	4504.5	566.5	467	S419	3244.5	566.5	527	S359	1984.5	566.5	587	S299	724.5	566.5
348	G208	5942.5	566.5	408	S478	4483.5	411.5	468	S418	3223.5	411.5	528	S358	1963.5	411.5	588	S298	703.5	411.5
349	G210	5921.5	411.5	409	S477	4462.5	566.5	469	S417	3202.5	566.5	529	S357	1942.5	566.5	589	S297	682.5	566.5
350	G212	5900.5	566.5	410	S476	4441.5	411.5	470	S416	3181.5	411.5	530	S356	1921.5	411.5	590	S296	661.5	411.5
351	G214	5879.5	411.5	411	S475	4420.5	566.5	471	S415	3160.5	566.5	531	S355	1900.5	566.5	591	S295	640.5	566.5
352	G216	5858.5	566.5	412	S474	4399.5	411.5	472	S414	3139.5	411.5	532	S354	1879.5	411.5	592	S294	619.5	411.5
353	G218	5837.5	411.5	413	S473	4378.5	566.5	473	S413	3118.5	566.5	533	S353	1858.5	566.5	593	S293	598.5	566.5
354	G220	5816.5	566.5	414	S472	4357.5	411.5	474	S412	3097.5	411.5	534	S352	1837.5	411.5	594	S292	577.5	411.5
355	VGLDMY2	5795.5	411.5	415	S471	4336.5	566.5	475	S411	3076.5	566.5	535	S351	1816.5	566.5	595	S291	556.5	566.5
356	TESTO27	5774.5	566.5	416	S470	4315.5	411.5	476	S410	3055.5	411.5	536	S350	1795.5	411.5	596	S290	535.5	411.5
357	TESTO28	5554.5	566.5	417	S469	4294.5	566.5	477	S409	3034.5	566.5	537	S349	1774.5	566.5	597	S289	514.5	566.5
358	S528	5533.5	411.5	418	S468	4273.5	411.5	478	S408	3013.5	411.5	538	S348	1753.5	411.5	598	S288	493.5	411.5
359	S527	5512.5	566.5	419	S467	4252.5	566.5	479	S407	2992.5	566.5	539	S347	1732.5	566.5	599	S287	472.5	566.5
360	S526	5491.5	411.5	420	S466	4231.5	411.5	480	S406	2971.5	411.5	540	S346	1711.5	411.5	600	S286	451.5	411.5

No.	Name	X	Y
601	S285	430.5	566.5
602	S284	409.5	411.5
603	S283	388.5	566.5
604	S282	367.5	411.5
605	S281	346.5	566.5
606	S280	325.5	411.5
607	S279	304.5	566.5
608	S278	283.5	411.5
609	S277	262.5	566.5
610	S276	241.5	411.5
611	S275	220.5	566.5
612	S274	199.5	411.5
613	S273	178.5	566.5
614	S272	157.5	411.5
615	S271	136.5	566.5
616	S270	115.5	411.5
617	S269	94.5	566.5
618	S268	73.5	411.5
619	S267	52.5	566.5
620	S266	31.5	411.5
621	S265	10.5	566.5
622	S264	-10.5	411.5
623	S263	-31.5	566.5
624	S262	-52.5	411.5
625	S261	-73.5	566.5
626	S260	-94.5	411.5
627	S259	-115.5	566.5
628	S258	-136.5	411.5
629	S257	-157.5	566.5
630	S256	-178.5	411.5
631	S255	-199.5	566.5
632	S254	-220.5	411.5
633	S253	-241.5	566.5
634	S252	-262.5	411.5
635	S251	-283.5	566.5
636	S250	-304.5	411.5
637	S249	-325.5	566.5
638	S248	-346.5	411.5
639	S247	-367.5	566.5
640	S246	-388.5	411.5
641	S245	-409.5	566.5
642	S244	-430.5	411.5
643	S243	-451.5	566.5
644	S242	-472.5	411.5
645	S241	-493.5	566.5
646	S240	-514.5	411.5
647	S239	-535.5	566.5
648	S238	-556.5	411.5
649	S237	-577.5	566.5
650	S236	-598.5	411.5
651	S235	-619.5	566.5
652	S234	-640.5	411.5
653	S233	-661.5	566.5
654	S232	-682.5	411.5
655	S231	-703.5	566.5
656	S230	-724.5	411.5
657	S229	-745.5	566.5
658	S228	-766.5	411.5
659	S227	-787.5	566.5
660	S226	-808.5	411.5

No.	Name	X	Y
661	S225	-829.5	566.5
662	S224	-850.5	411.5
663	S223	-871.5	566.5
664	S222	-892.5	411.5
665	S221	-913.5	566.5
666	S220	-934.5	411.5
667	S219	-955.5	566.5
668	S218	-976.5	411.5
669	S217	-997.5	566.5
670	S216	-1018.5	411.5
671	S215	-1039.5	566.5
672	S214	-1060.5	411.5
673	S213	-1081.5	566.5
674	S212	-1102.5	411.5
675	S211	-1123.5	566.5
676	S210	-1144.5	411.5
677	S209	-1165.5	566.5
678	S208	-1186.5	411.5
679	S207	-1207.5	566.5
680	S206	-1228.5	411.5
681	S205	-1249.5	566.5
682	S204	-1270.5	411.5
683	S203	-1291.5	566.5
684	S202	-1312.5	411.5
685	S201	-1333.5	566.5
686	S200	-1354.5	411.5
687	S199	-1375.5	566.5
688	S198	-1396.5	411.5
689	S197	-1417.5	566.5
690	S196	-1438.5	411.5
691	S195	-1459.5	566.5
692	S194	-1480.5	411.5
693	S193	-1501.5	566.5
694	S192	-1522.5	411.5
695	S191	-1543.5	566.5
696	S190	-1564.5	411.5
697	S189	-1585.5	566.5
698	S188	-1606.5	411.5
699	S187	-1627.5	566.5
700	S186	-1648.5	411.5
701	S185	-1669.5	566.5
702	S184	-1690.5	411.5
703	S183	-1711.5	566.5
704	S182	-1732.5	411.5
705	S181	-1753.5	566.5
706	S180	-1774.5	411.5
707	S179	-1795.5	566.5
708	S178	-1816.5	411.5
709	S177	-1837.5	566.5
710	S176	-1858.5	411.5
711	S175	-1879.5	566.5
712	S174	-1900.5	411.5
713	S173	-1921.5	566.5
714	S172	-1942.5	411.5
715	S171	-1963.5	566.5
716	S170	-1984.5	411.5
717	S169	-2005.5	566.5
718	S168	-2026.5	411.5
719	S167	-2047.5	566.5
720	S166	-2068.5	411.5

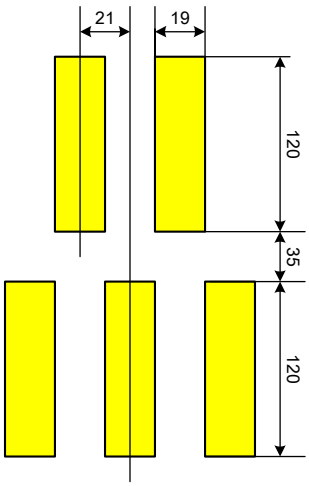
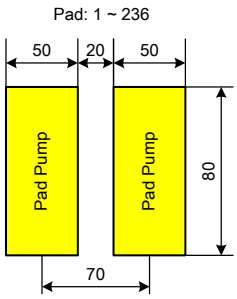
No.	Name	X	Y
721	S165	-2089.5	566.5
722	S164	-2110.5	411.5
723	S163	-2131.5	566.5
724	S162	-2152.5	411.5
725	S161	-2173.5	566.5
726	S160	-2194.5	411.5
727	S159	-2215.5	566.5
728	S158	-2236.5	411.5
729	S157	-2257.5	566.5
730	S156	-2278.5	411.5
731	S155	-2299.5	566.5
732	S154	-2320.5	411.5
733	S153	-2341.5	566.5
734	S152	-2362.5	411.5
735	S151	-2383.5	566.5
736	S150	-2404.5	411.5
737	S149	-2425.5	566.5
738	S148	-2446.5	411.5
739	S147	-2467.5	566.5
740	S146	-2488.5	411.5
741	S145	-2509.5	566.5
742	S144	-2530.5	411.5
743	S143	-2551.5	566.5
744	S142	-2572.5	411.5
745	S141	-2593.5	566.5
746	S140	-2614.5	411.5
747	S139	-2635.5	566.5
748	S138	-2656.5	411.5
749	S137	-2677.5	566.5
750	S136	-2698.5	411.5
751	S135	-2719.5	566.5
752	S134	-2740.5	411.5
753	S133	-2761.5	566.5
754	S132	-2782.5	411.5
755	S131	-2803.5	566.5
756	S130	-2824.5	411.5
757	S129	-2845.5	566.5
758	S128	-2866.5	411.5
759	S127	-2887.5	566.5
760	S126	-2908.5	411.5
761	S125	-2929.5	566.5
762	S124	-2950.5	411.5
763	S123	-2971.5	566.5
764	S122	-2992.5	411.5
765	S121	-3013.5	566.5
766	S120	-3034.5	411.5
767	S119	-3055.5	566.5
768	S118	-3076.5	411.5
769	S117	-3097.5	566.5
770	S116	-3118.5	411.5
771	S115	-3139.5	566.5
772	S114	-3160.5	411.5
773	S113	-3181.5	566.5
774	S112	-3202.5	411.5
775	S111	-3223.5	566.5
776	S110	-3244.5	411.5
777	S109	-3265.5	566.5
778	S108	-3286.5	411.5
779	S107	-3307.5	566.5
780	S106	-3328.5	411.5

No.	Name	X	Y
781	S105	-3349.5	566.5
782	S104	-3370.5	411.5
783	S103	-3391.5	566.5
784	S102	-3412.5	411.5
785	S101	-3433.5	566.5
786	S100	-3454.5	411.5
787	S99	-3475.5	566.5
788	S98	-3496.5	411.5
789	S97	-3517.5	566.5
790	S96	-3538.5	411.5
791	S95	-3559.5	566.5
792	S94	-3580.5	411.5
793	S93	-3601.5	566.5
794	S92	-3622.5	411.5
795	S91	-3643.5	566.5
796	S90	-3664.5	411.5
797	S89	-3685.5	566.5
798	S88	-3706.5	411.5
799	S87	-3727.5	566.5
800	S86	-3748.5	411.5
801	S85	-3769.5	566.5
802	S84	-3790.5	411.5
803	S83	-3811.5	566.5
804	S82	-3832.5	411.5
805	S81	-3853.5	566.5
806	S80	-3874.5	411.5
807	S79	-3895.5	566.5
808	S78	-3916.5	411.5
809	S77	-3937.5	566.5
810	S76	-3958.5	411.5
811	S75	-3979.5	566.5
812	S74	-4000.5	411.5
813	S73	-4021.5	566.5
814	S72	-4042.5	411.5
815	S71	-4063.5	566.5
816	S70	-4084.5	411.5
817	S69	-4105.5	566.5
818	S68	-4126.5	411.5
819	S67	-4147.5	566.5
820	S66	-4168.5	411.5
821	S65	-4189.5	566.5
822	S64	-4210.5	411.5
823	S63	-4231.5	566.5
824	S62	-4252.5	411.5
825	S61	-4273.5	566.5
826	S60	-4294.5	411.5
827	S59	-4315.5	566.5
828	S58	-4336.5	411.5
829	S57	-4357.5	566.5
830	S56	-4378.5	411.5
831	S55	-4399.5	566.5
832	S54	-4420.5	411.5
833	S53	-4441.5	566.5
834	S52	-4462.5	411.5
835	S51	-4483.5	566.5
836	S50	-4504.5	411.5
837	S49	-4525.5	566.5
838	S48	-4546.5	411.5
839	S47	-4567.5	566.5
840	S46	-4588.5	411.5

No.	Name	X	Y
841	S45	-4609.5	566.5
842	S44	-4630.5	411.5
843	S43	-4651.5	566.5
844	S42	-4672.5	411.5
845	S41	-4693.5	566.5
846	S40	-4714.5	411.5
847	S39	-4735.5	566.5
848	S38	-4756.5	411.5
849	S37	-4777.5	566.5
850	S36	-4798.5	411.5
851	S35	-4819.5	566.5
852	S34	-4840.5	411.5
853	S33	-4861.5	566.5
854	S32	-4882.5	411.5
855	S31	-4903.5	566.5
856	S30	-4924.5	411.5
857	S29	-4945.5	566.5
858	S28	-4966.5	411.5
859	S27	-4987.5	566.5
860	S26	-5008.5	411.5
861	S25	-5029.5	566.5
862	S24	-5050.5	411.5
863	S23	-5071.5	566.5
864	S22	-5092.5	411.5
865	S21	-5113.5	566.5
866	S20	-5134.5	411.5
867	S19	-5155.5	566.5
868	S18	-5176.5	411.5
869	S17	-5197.5	566.5
870	S16	-5218.5	411.5
871	S15	-5239.5	566.5
872	S14	-5260.5	411.5
873	S13	-5281.5	566.5
874	S12	-5302.5	411.5
875	S11	-5323.5	566.5
876	S10	-5344.5	411.5
877	S9	-5365.5	566.5
878	S8	-5386.5	411.5
879	S7	-5407.5	566.5
880	S6	-5428.5	411.5
881	S5	-5449.5	566.5
882	S4	-5470.5	411.5
883	S3	-5491.5	566.5
884	S2	-5512.5	411.5
885	S1	-5533.5	566.5
886	TESTO29	-5554.5	411.5
887	TESTO30	-5774.5	566.5
888	VGLDMY3	-5795.5	411.5
889	G219	-5816.5	566.5
890	G217	-5837.5	411.5
891	G215	-5858.5	566.5
892	G213	-5879.5	411.5
893	G211	-5900.5	566.5
894	G209	-5921.5	411.5
895	G207	-5942.5	566.5
896	G205	-5963.5	411.5
897	G203	-5984.5	566.5
898	G201	-6005.5	411.5
899	G199	-6026.5	566.5
900	G197	-6047.5	411.5

No.	Name	X	Y
901	G195	-6068.5	566.5
902	G193	-6089.5	411.5
903	G191	-6110.5	566.5
904	G189	-6131.5	411.5
905	G187	-6152.5	566.5
906	G185	-6173.5	411.5
907	G183	-6194.5	566.5
908	G181	-6215.5	411.5
909	G179	-6236.5	566.5
910	G177	-6257.5	411.5
911	G175	-6278.5	566.5
912	G173	-6299.5	411.5
913	G171	-6320.5	566.5
914	G169	-6341.5	411.5
915	G167	-6362.5	566.5
916	G165	-6383.5	411.5
917	G163	-6404.5	566.5
918	G161	-6425.5	411.5
919	G159	-6446.5	566.5
920	G157	-6467.5	411.5
921	G155	-6488.5	566.5
922	G153	-6509.5	411.5
923	G151	-6530.5	566.5
924	G149	-6551.5	411.5
925	G147	-6572.5	566.5
926	G145	-6593.5	411.5
927	G143	-6614.5	566.5
928	G141	-6635.5	411.5
929	G139	-6656.5	566.5
930	G137	-6677.5	411.5
931	G135	-6698.5	566.5
932	G133	-6719.5	411.5
933	G131	-6740.5	566.5
934	G129	-6761.5	411.5
935	G127	-6782.5	566.5
936	G125	-6803.5	411.5
937	G123	-6824.5	566.5
938	G121	-6845.5	411.5
939	G119	-6866.5	566.5
940	G117	-6887.5	411.5
941	G115	-6908.5	566.5
942	G113	-6929.5	411.5
943	G111	-6950.5	566.5
944	G109	-6971.5	411.5
945	G107	-6992.5	566.5
946	G105	-7013.5	411.5
947	G103	-7034.5	566.5
948	G101	-7055.5	411.5
949	G99	-7076.5	566.5
950	G97	-7097.5	411.5
951	G95	-7118.5	566.5
952	G93	-7139.5	411.5
953	G91	-7160.5	566.5
954	G89	-7181.5	411.5
955	G87	-7202.5	566.5
956	G85	-7223.5	411.5
957	G83	-7244.5	566.5
958	G81	-7265.5	411.5
959	G79	-7286.5	566.5
960	G77	-7307.5	411.5

No.	Name	X	Y
961	G75	-7328.5	566.5
962	G73	-7349.5	411.5
963	G71	-7370.5	566.5
964	G69	-7391.5	411.5
965	G67	-7412.5	566.5
966	G65	-7433.5	411.5
967	G63	-7454.5	566.5
968	G61	-7475.5	411.5
969	G59	-7496.5	566.5
970	G57	-7517.5	411.5
971	G55	-7538.5	566.5
972	G53	-7559.5	411.5
973	G51	-7580.5	566.5
974	G49	-7601.5	411.5
975	G47	-7622.5	566.5
976	G45	-7643.5	411.5
977	G43	-7664.5	566.5
978	G41	-7685.5	411.5
979	G39	-7706.5	566.5
980	G37	-7727.5	411.5
981	G35	-7748.5	566.5
982	G33	-7769.5	411.5
983	G31	-7790.5	566.5
984	G29	-7811.5	411.5
985	G27	-7832.5	566.5
986	G25	-7853.5	411.5
987	G23	-7874.5	566.5
988	G21	-7895.5	411.5
989	G19	-7916.5	566.5
990	G17	-7937.5	411.5
991	G15	-7958.5	566.5
992	G13	-7979.5	411.5
993	G11	-8000.5	566.5
994	G9	-8021.5	411.5
995	G7	-8042.5	566.5
996	G5	-8063.5	411.5
997	G3	-8084.5	566.5
998	G1	-8105.5	411.5
999	VGLDMY4	-8126.5	566.5
1000	DUMMYR9	-8147.5	411.5
1001	DUMMYR10	-8168.5	566.5
1002	TESTO31	-8189.5	411.5
1003	TESTO32	-8210.5	566.5
	1-a	-8422	536.9
	1-b	8422	536.9
	2-a	-8508	-474.5
	2-b	8508	-474.5
	3-a	-8505	-398
	3-b	8505	-398

S1 ~ S528 G1 ~ G220 VGLDMY1~4 TESTO25~32 DUMMYR7~R10	 Unit: um
I/O Pads	

6. Block Description

MPU System Interface

ILI9221 supports three system high-speed interfaces: i80/M68-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9221 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9221 read the first data from the internal GRAM. Valid data are read out after the ILI9221 performs the second read operation.

Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

Registers selection by system interface (8-/9-/16-/18-bit bus width)	I80			M68	
Function	**RS**	**nWR**	**nRD**	**E**	**RW**
Write an index to IR register	0	0	1	1	0
Read an internal status	0	1	0	1	1
Write to control registers or the internal GRAM by WDR register.	1	0	1	1	0
Read from the internal GRAM by RDR register.	1	1	0	1	1

Registers selection by the SPI system interface		
Function	**R/W**	**RS**
Write an index to IR register	0	0
Read an internal status	1	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

ILI9221 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section. The ILI9221 allows for switching

between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Bit Operation

The ILI9221 supports a write data mask function for selectively writing data to the internal RAM in units of bits and a logical/compare operation to write data to the GRAM only when a condition is met as a result of comparing the data and the compare register bits. For details, see “Graphics Operation Functions”.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 87,120 (176 x 220x 18/8) bytes, using 18 bits for each pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the “γ-Correction Register” section.

Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC.)

ILI9221 generates RC oscillation with an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency is changed according to the value of an external resistor. Adjust the oscillation frequency in accordance to the operating voltage or the frame frequency. An operating clock can be input externally. During standby mode, RC oscillation is halted to reduce power consumption. For details, see “Oscillator”.

LCD Driver Circuit

The LCD driver circuit of ILI9221 consists of a 528-output source driver (S1 ~ S528) and a 220-output gate driver (G1~G220). Display pattern data are latched when the 528th bit data are input. The latched data control

the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

7. System Interface

7.1. Interface Specifications

ILI9221 has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9221 also has the RGB interface and VSYNC interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

ILI9221 operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM[1:0] = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available simultaneously.

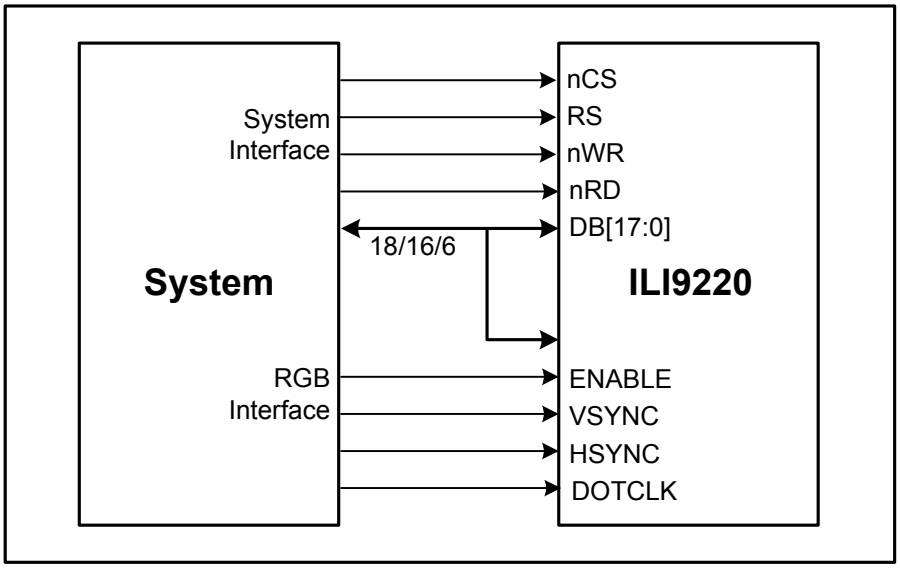


Figure1 System Interface and RGB Interface connection

7.2. Input Interfaces

The following are the system interfaces available with the ILI9221. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting instructions and RAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	M68-system 16-bit interface	DB[17:10], DB[8:1]
0	0	0	1	M68-system 8-bit interface	DB[17:10]
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO (DB[1:0])
0	1	1	*	Setting invalid	
1	0	0	0	M68-system18-bit interface	DB[17:0]
1	0	0	1	M68-system 9-bit interface	DB[17:9]
1	0	1	0	i80-system18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

7.2.1. i80/18-bit System Interface

The i80/18-bit system interface is selected by setting the IM[3:0] as “1010” levels.

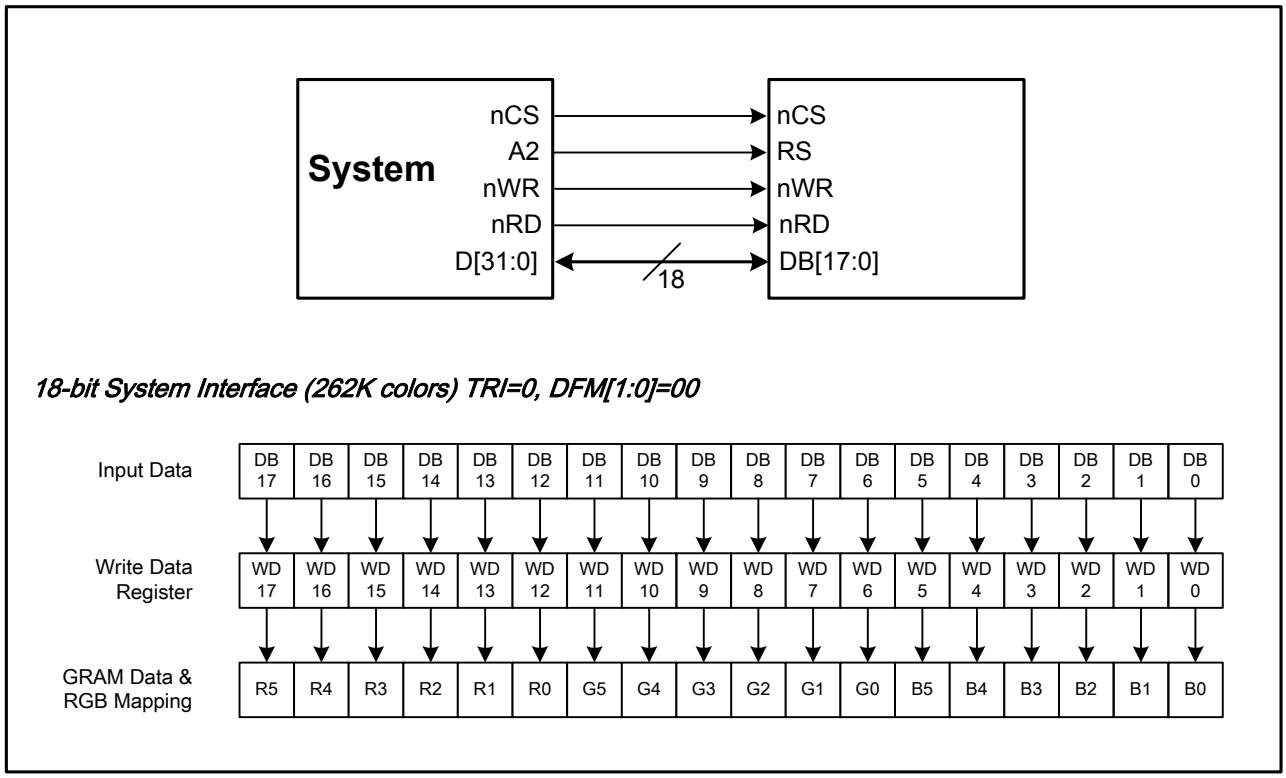


Figure2 18-bit System Interface Data Format

7.2.2. i80/16-bit System Interface

The i80/16-bit system interface is selected by setting the IM[3:0] as “0010” levels.

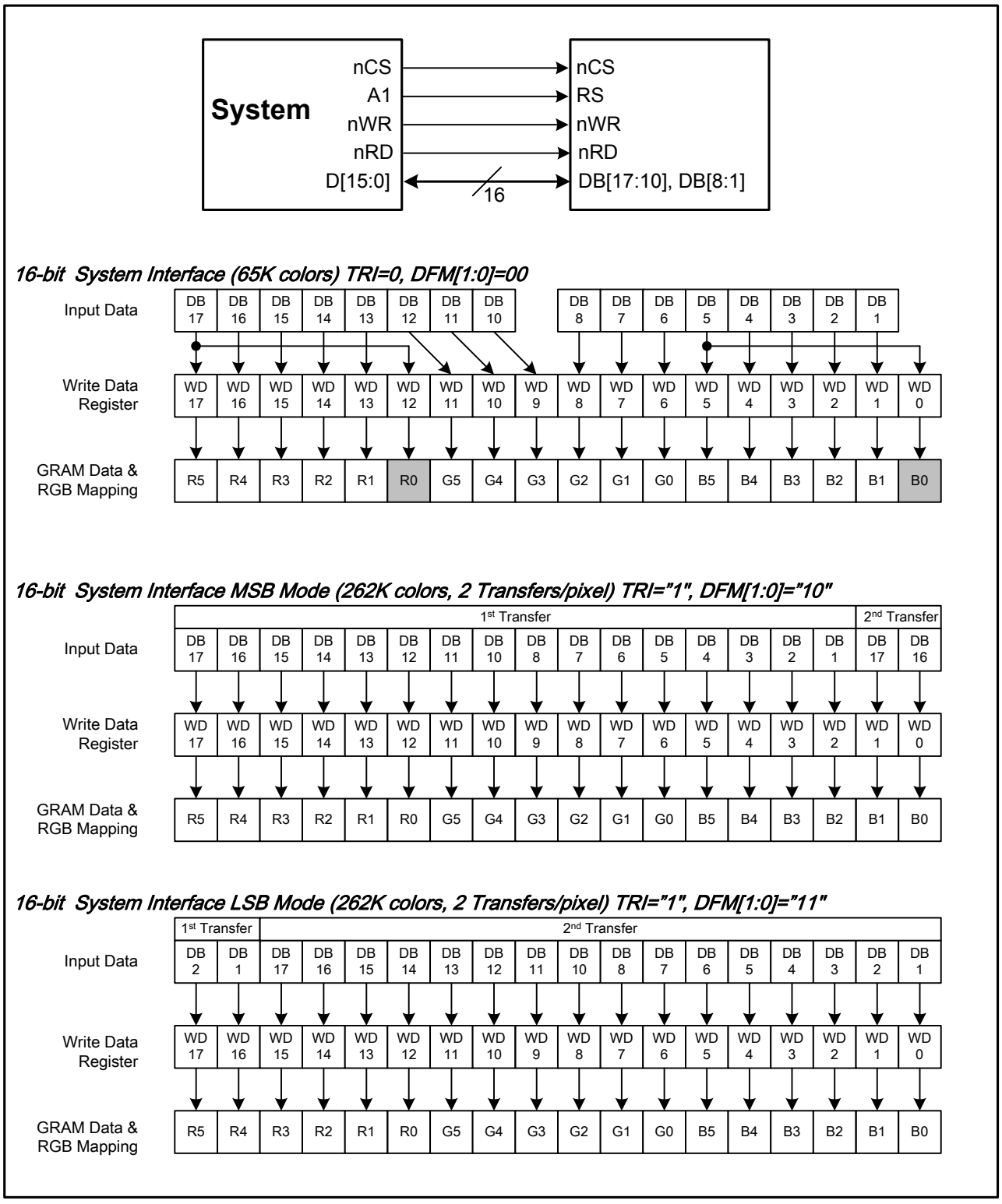


Figure3 16-bit System Interface Data Format

7.2.3. i80/9-bit System Interface

The i80/9-bit system interface is selected by setting the IM[3:0] as “1011” and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to either Vcc or AGND.

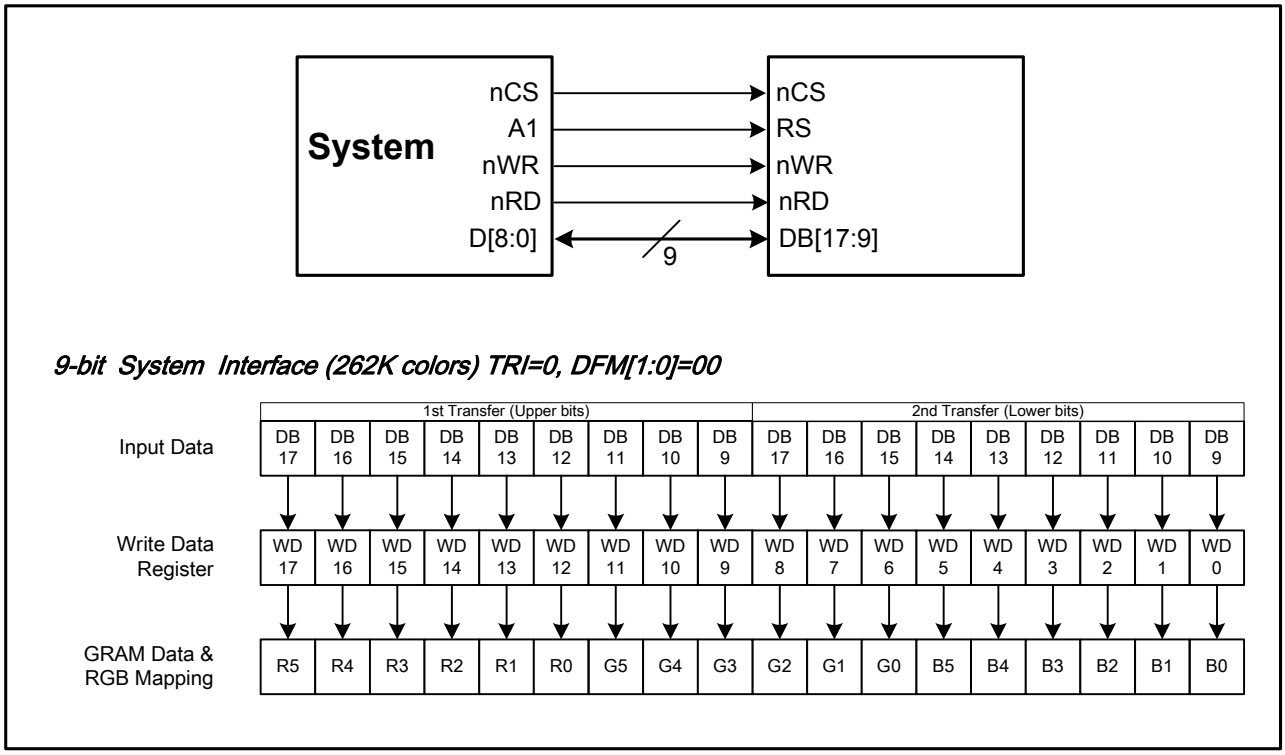
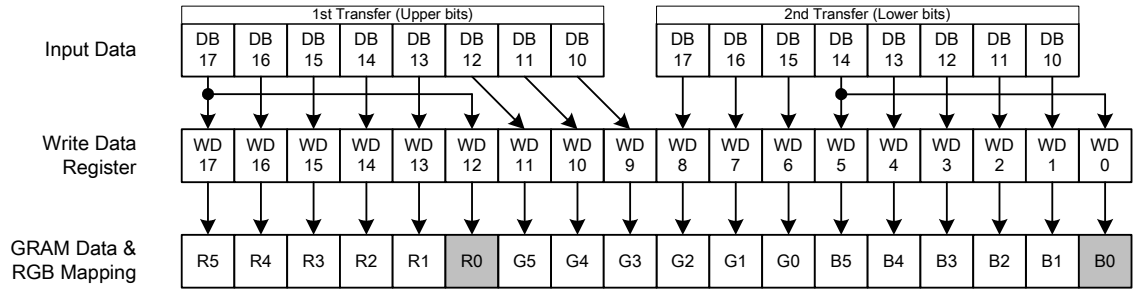


Figure4 9-bit System Interface Data Format

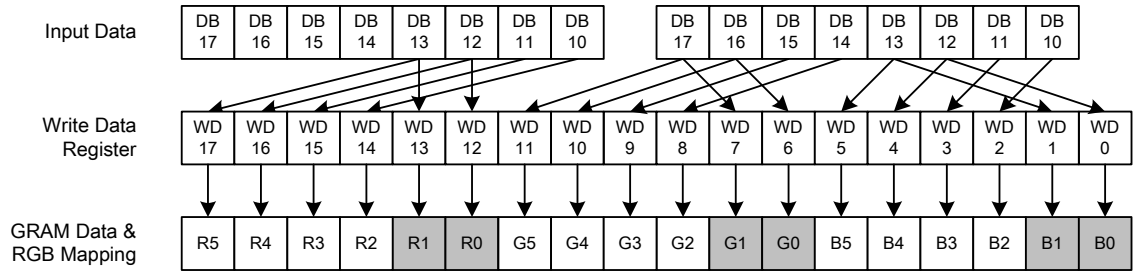
7.2.4. i80/8-bit System Interface

The i80/8-bit system interface is selected by setting the IM[3:0] as “0011” and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to either Vcc or AGND.

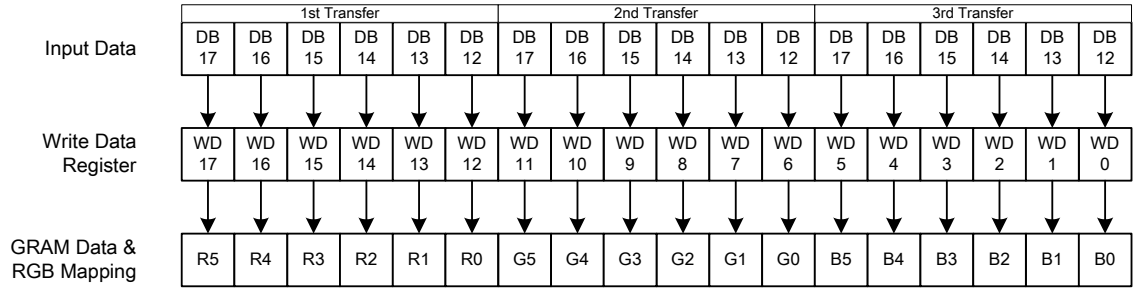
8-bit System Interface (65K colors) TRI=0, DFM[1:0]=00



8-bit System Interface (4096 colors) TRI=0, DFM[1:0]=01



8-bit System Interface (262K colors) TRI=1, DFM[1:0]=10



8-bit System Interface (65K colors) TRI=1, DFM[1:0]=11

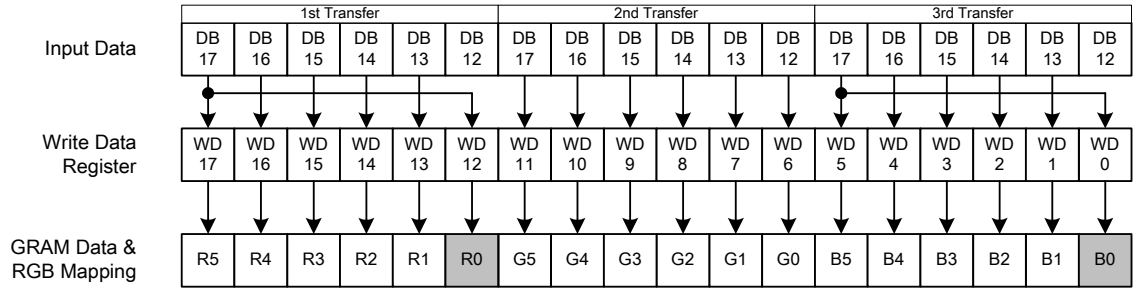


Figure5 8-bit System Interface Data Format

Data transfer synchronization in 8/9-bit bus interface mode

ILI9221 supports a data transfer synchronization function to reset upper and lower counters which count the transfers number of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in the numbers of transfers between the upper and lower byte counters due to noise and so on, the “00”h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.

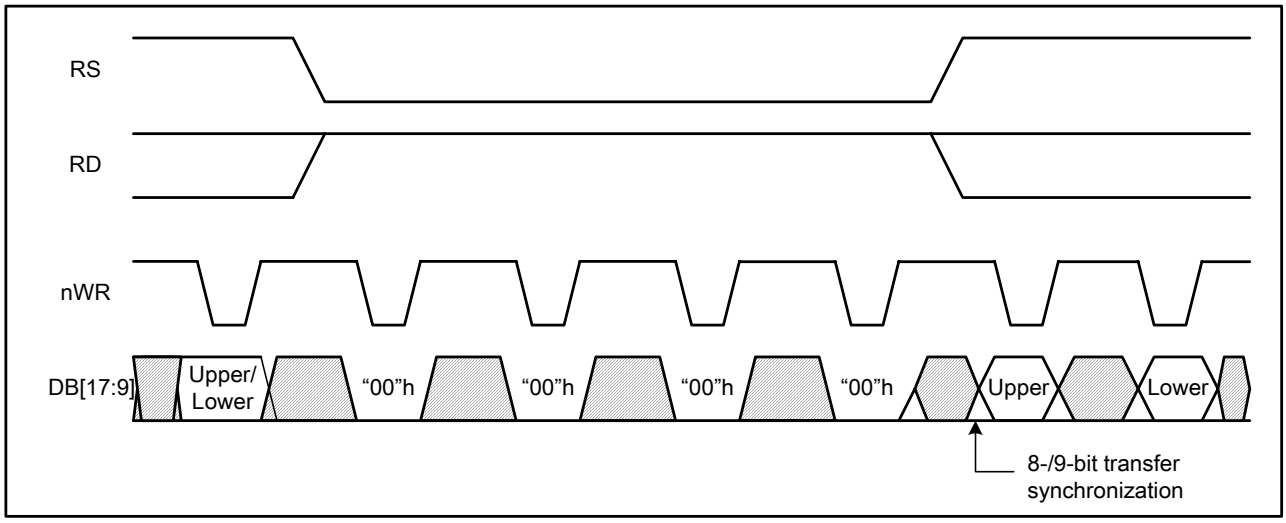


Figure6 Data Transfer Synchronization in 8/9-bit System Interface

7.3. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “010x” level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code.The DB[17:0] pins, which are not used, must be tied to either IOVcc or DGND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9221.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, ILI9221 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9221 are 16-bit format and receive the first and the second

byte datat as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin.

RS and R/W Bit Function

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

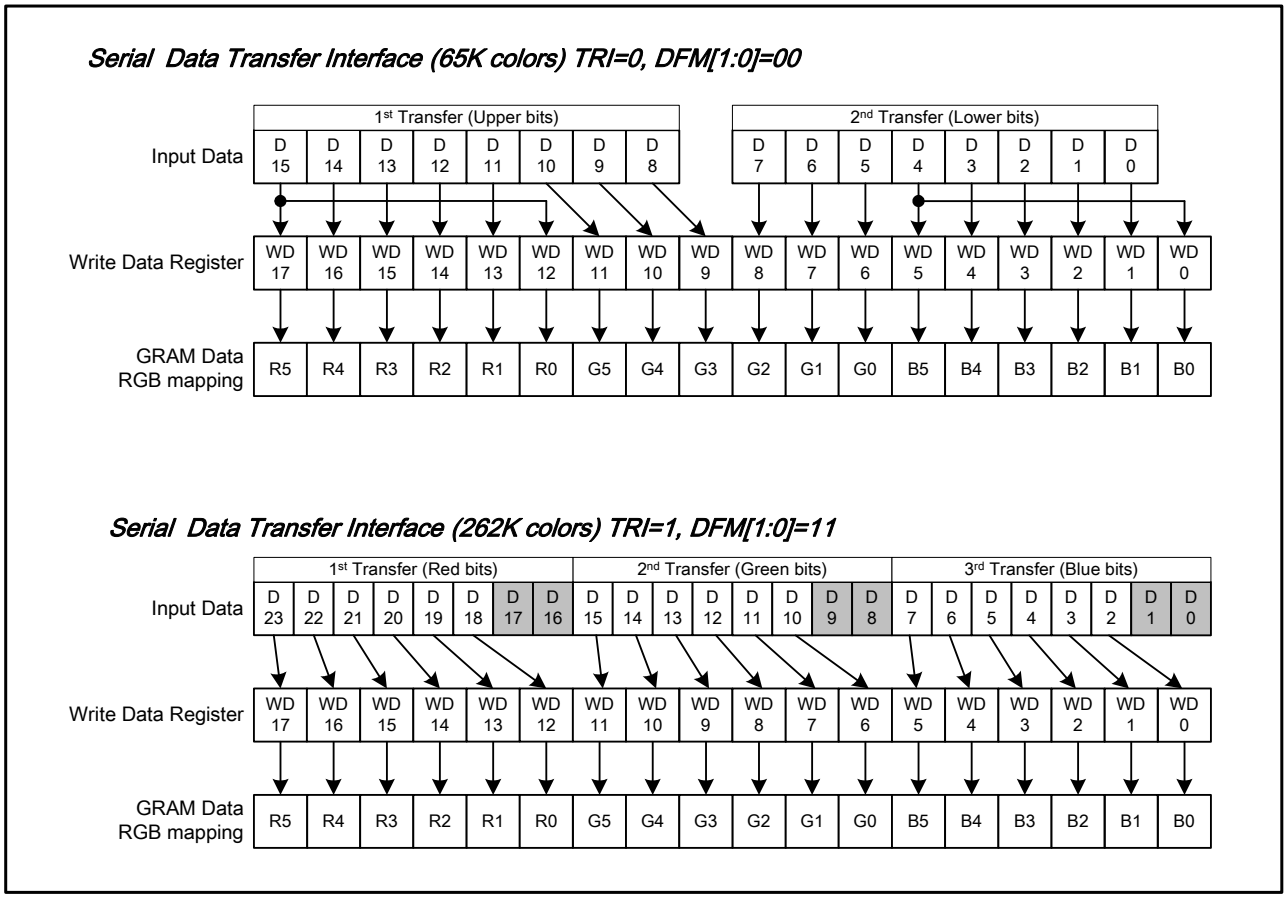


Figure 7 Data Format of SPI Interface

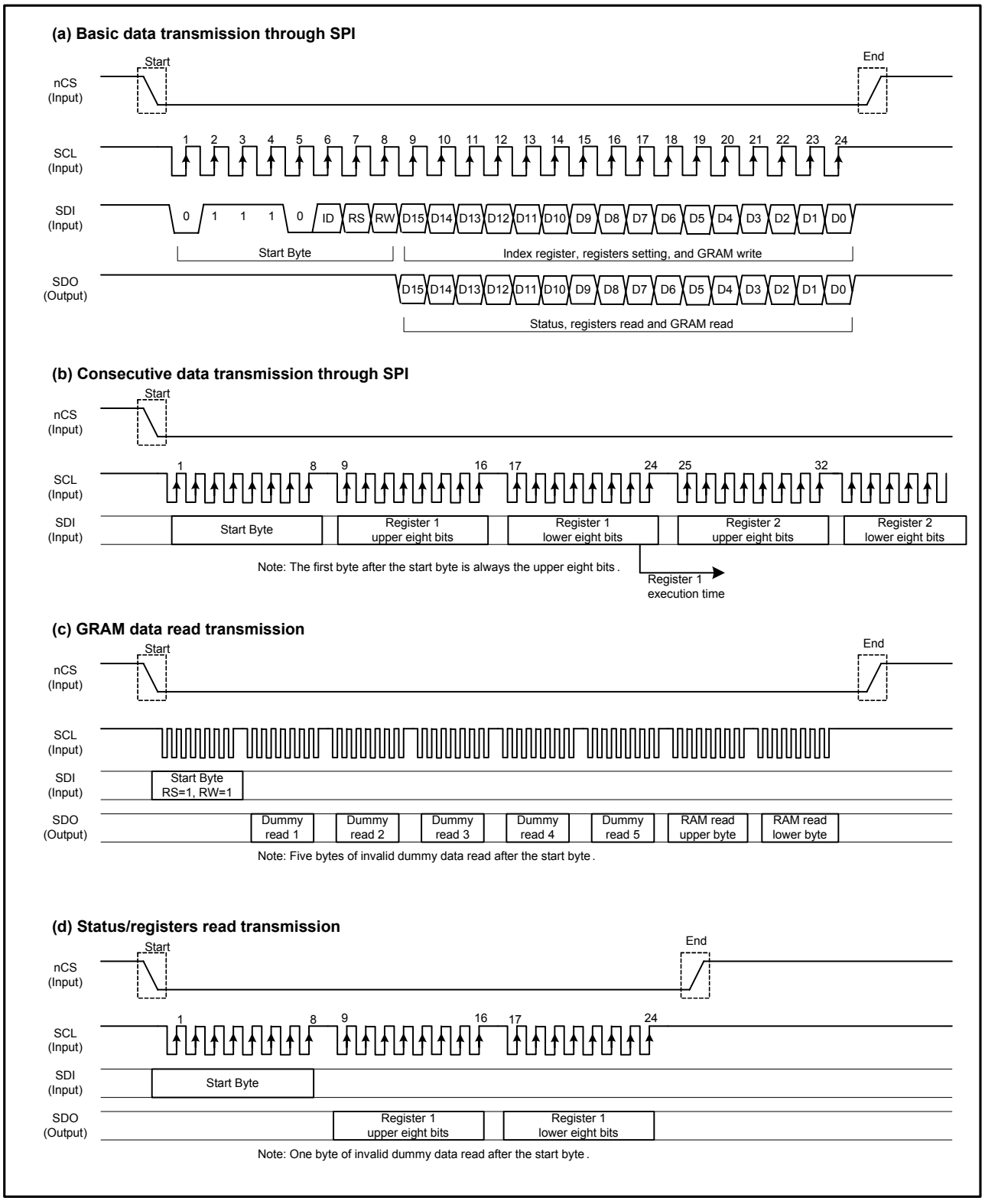
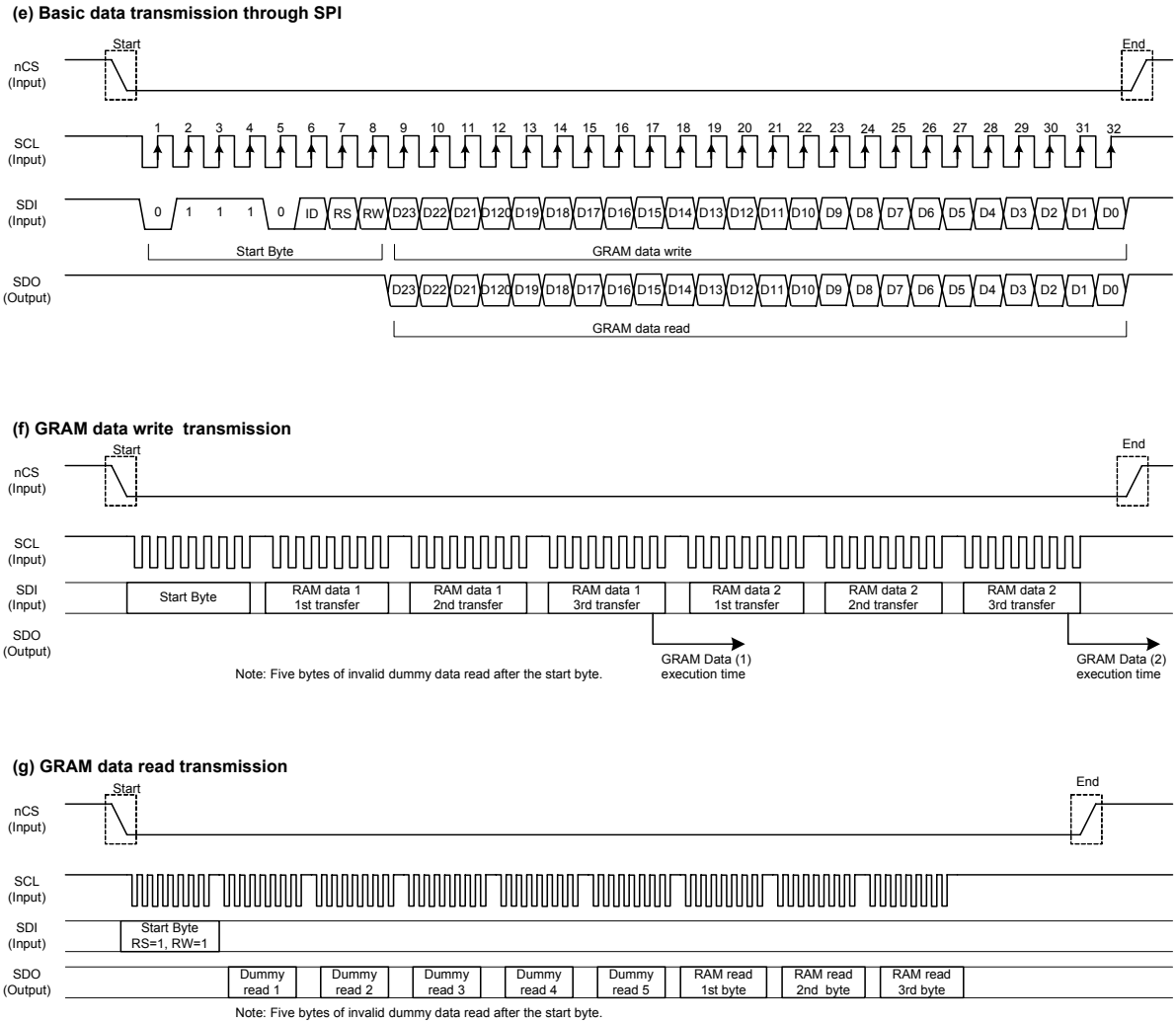


Figure8 Data transmission through serial peripheral interface (SPI)



RAM data transfer in SPI mode when TRI=1 and DFM[1:0]=10.

Figure9 Data transmission through serial peripheral interface (SPI), TRI=”1” and DFM=”10”)

7.4. VSYNC Interface

ILI9221 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the i80/M68 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.

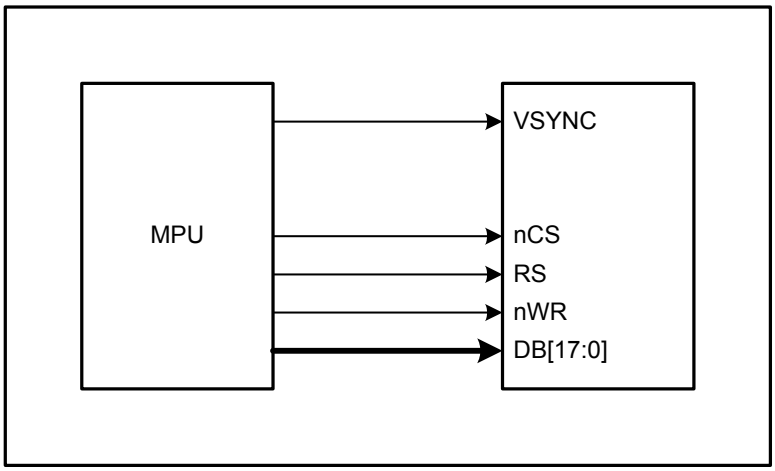


Figure10 Data transmission through VSYNC interface)

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

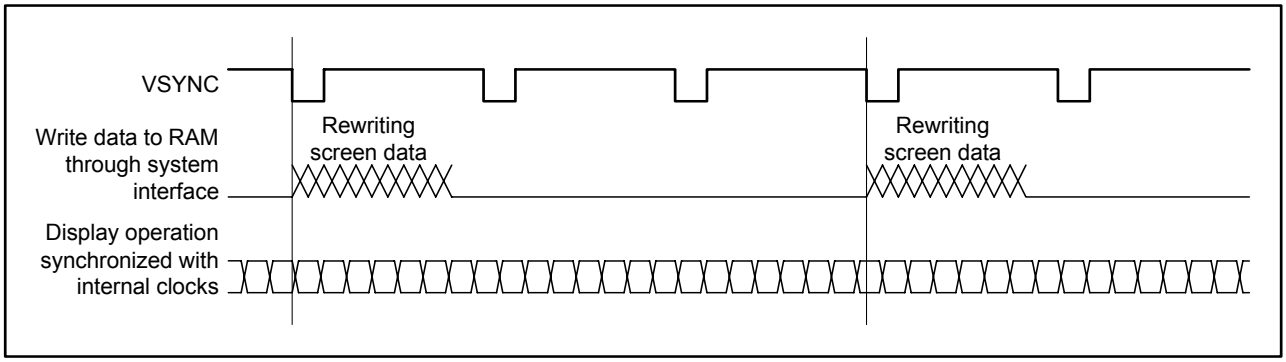


Figure11 Moving picture data transmission through VSYNC interface

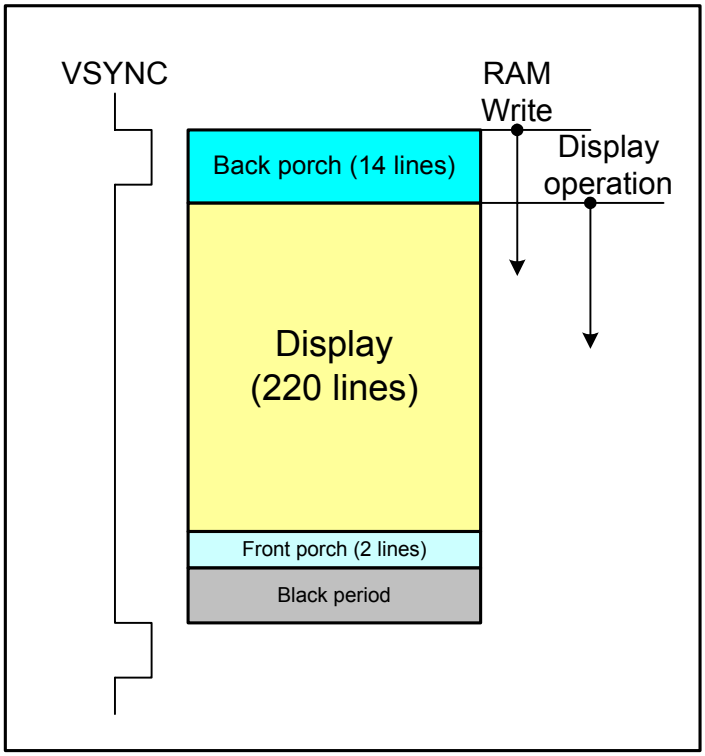


Figure12 Operation through VSYNC Interface

The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (FP) + BackPorch (BP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed (HZ)} > \frac{\textit{176 x DisplayLines (NL)}}{\textit{[(BackPorch(BP)+DisplayLines(NL) - margins] x 16 (clocks) x 1/fosc}}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 176 RGB × 220 lines

Lines: 220 lines (NL = 110011)

Back porch: 14 lines (BP = 1110)

Front porch: 2 lines (FP = 0010)

Frame frequency: 60 Hz

Frequency fluctuation: 5%

Internal oscillator clock (fosc.) [Hz] = 60 x [220 + 2 + 14] x 16 x (1.05/0.95) ≒ 251KHz

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±5% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 176 x 220 x 251K / [(14 + 220 – 2) x16] ≒ 2.62 MHz

The above theoretical value is calculated based on the premise that the ILI9221 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 2.62MHz or more will guarantee the completion of GRAM write operation before the ILI9221 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to “0” to transfer display data.

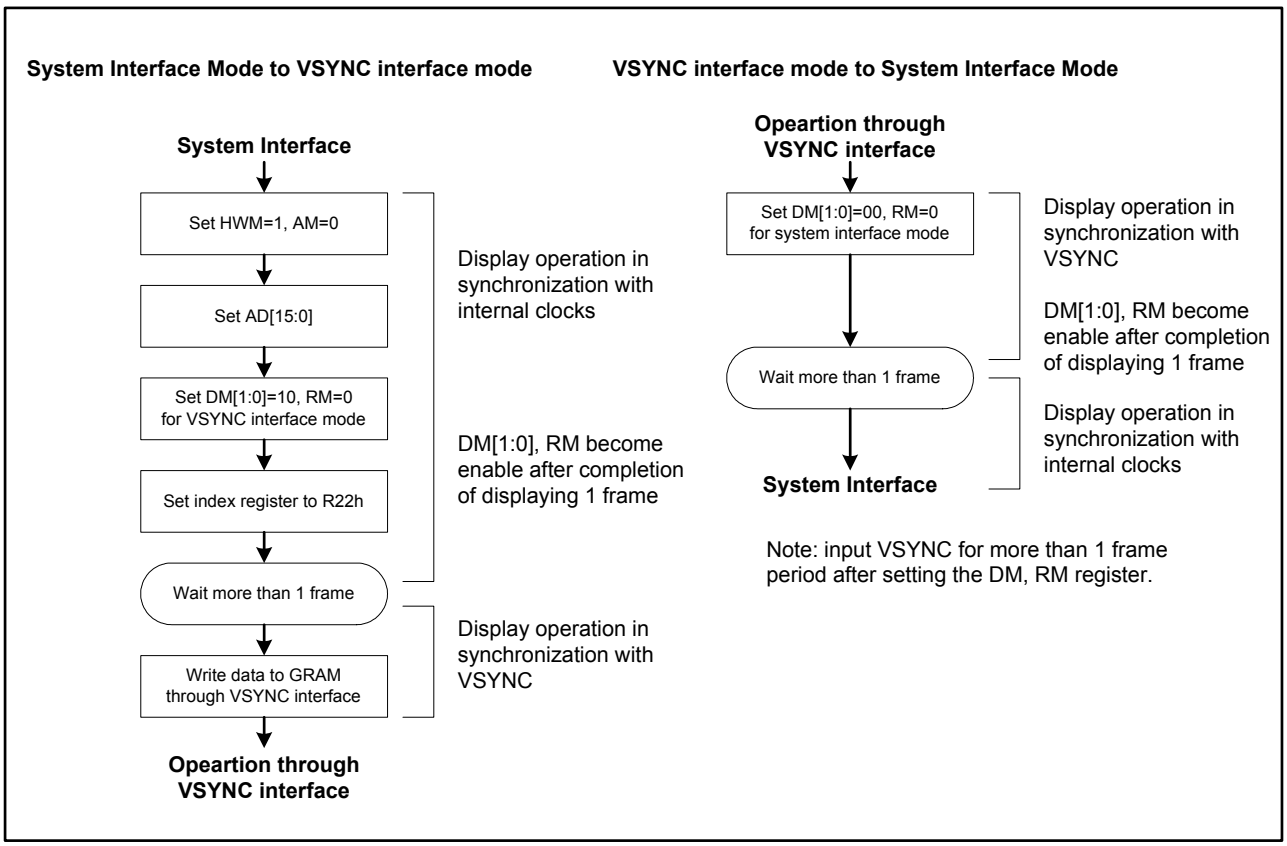


Figure13 Transition flow between VSYNC and internal clock operation modes

7.5. RGB Input Interface

The RGB Interface mode is available for ILI9221 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

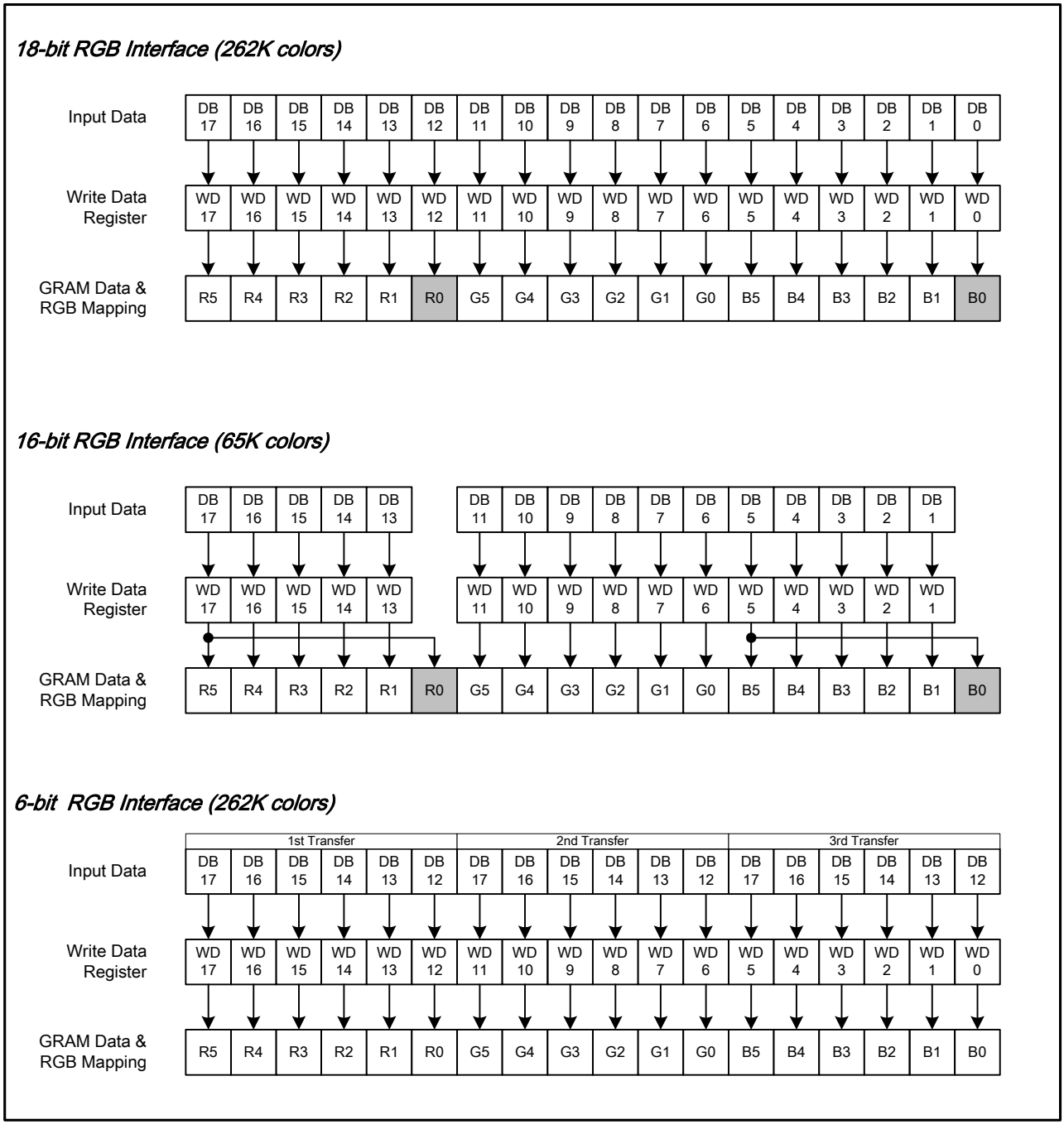


Figure14 RGB Interface Data Format

7.5.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM with the high-speed write function and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

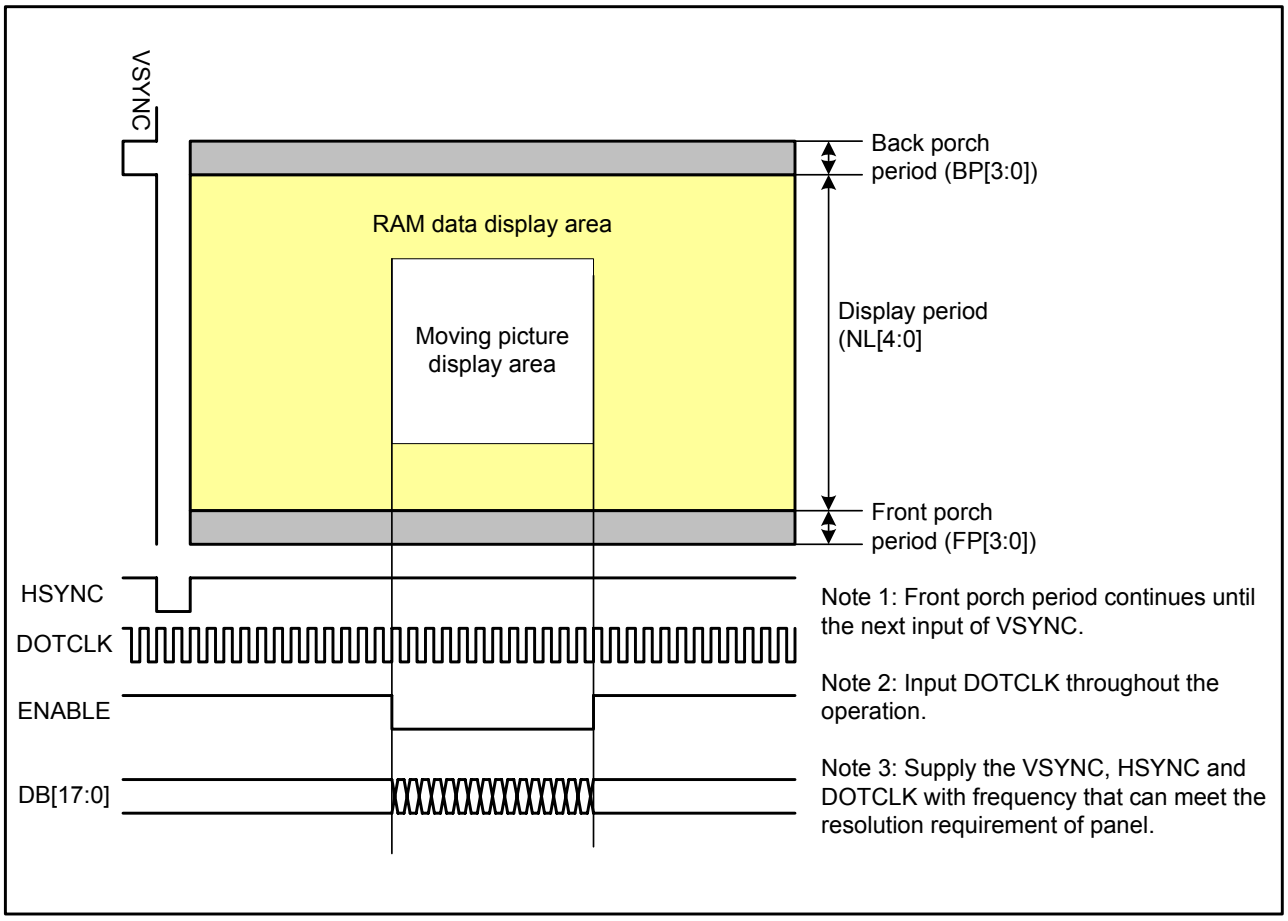


Figure15 GRAM Access Area by RGB Interface

7.5.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.

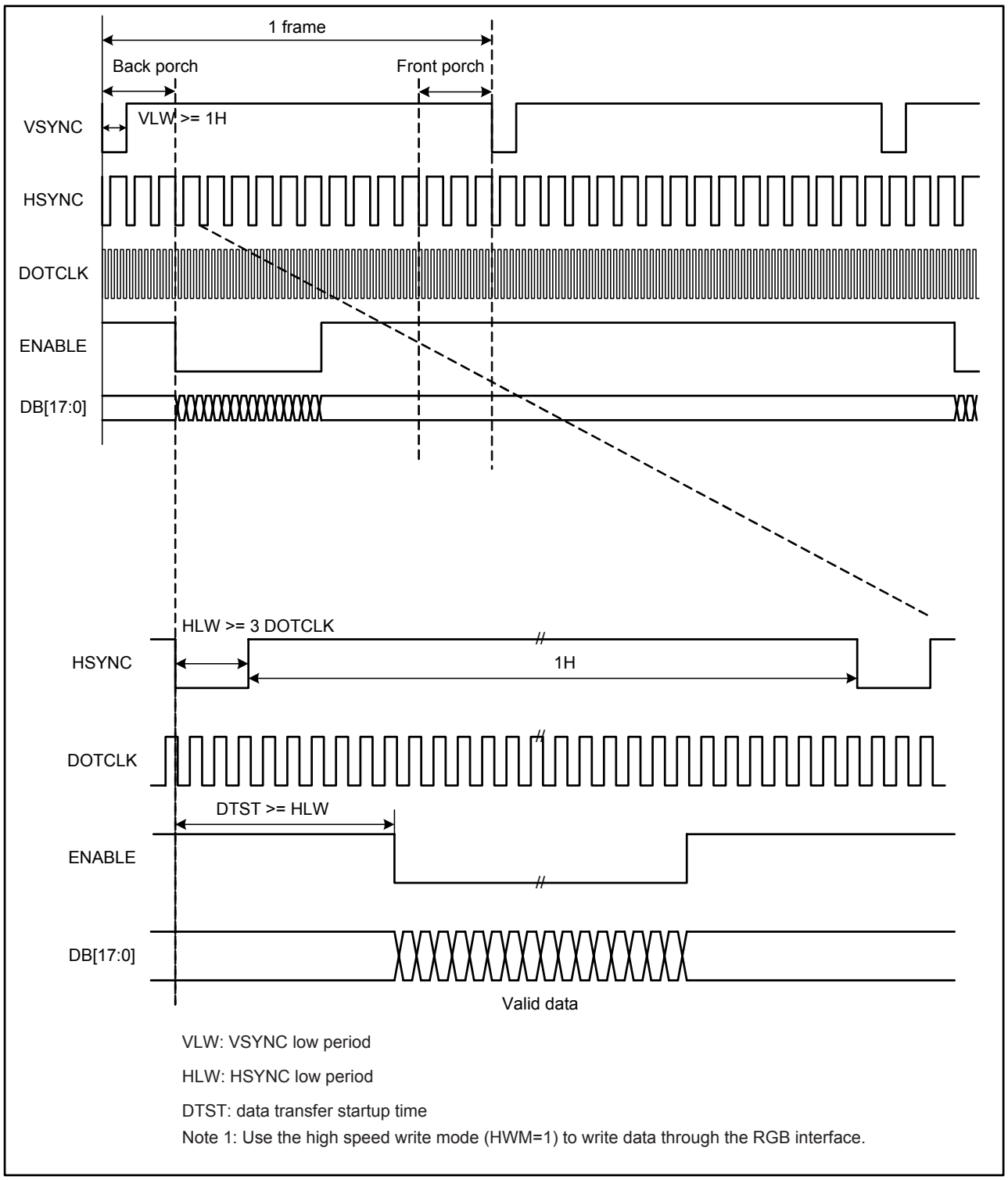
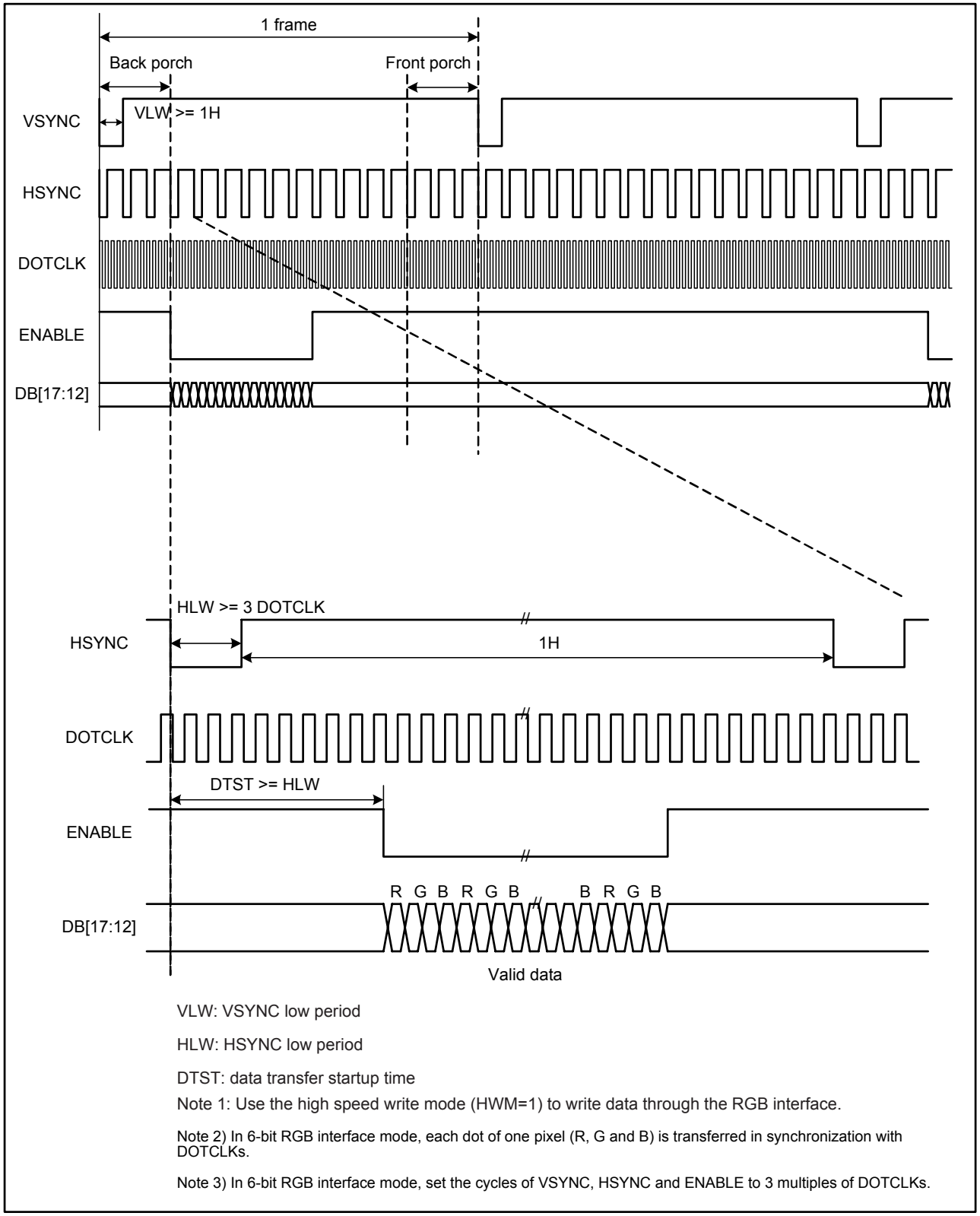


Figure16 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as follows.



VLW: VSYNC low period

HLW: HSYNC low period

DTST: data transfer startup time

Note 1: Use the high speed write mode (HWM=1) to write data through the RGB interface.

Note 2) In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLKs.

Note 3) In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and ENABLE to 3 multiples of DOTCLKs.

Figure17 Timing chart of signals in 6-bit RGB interface mode

7.5.3. Moving Picture Mode

ILI9221 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

ILI9221 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = “0”) and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = “1” and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the ILI9221 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

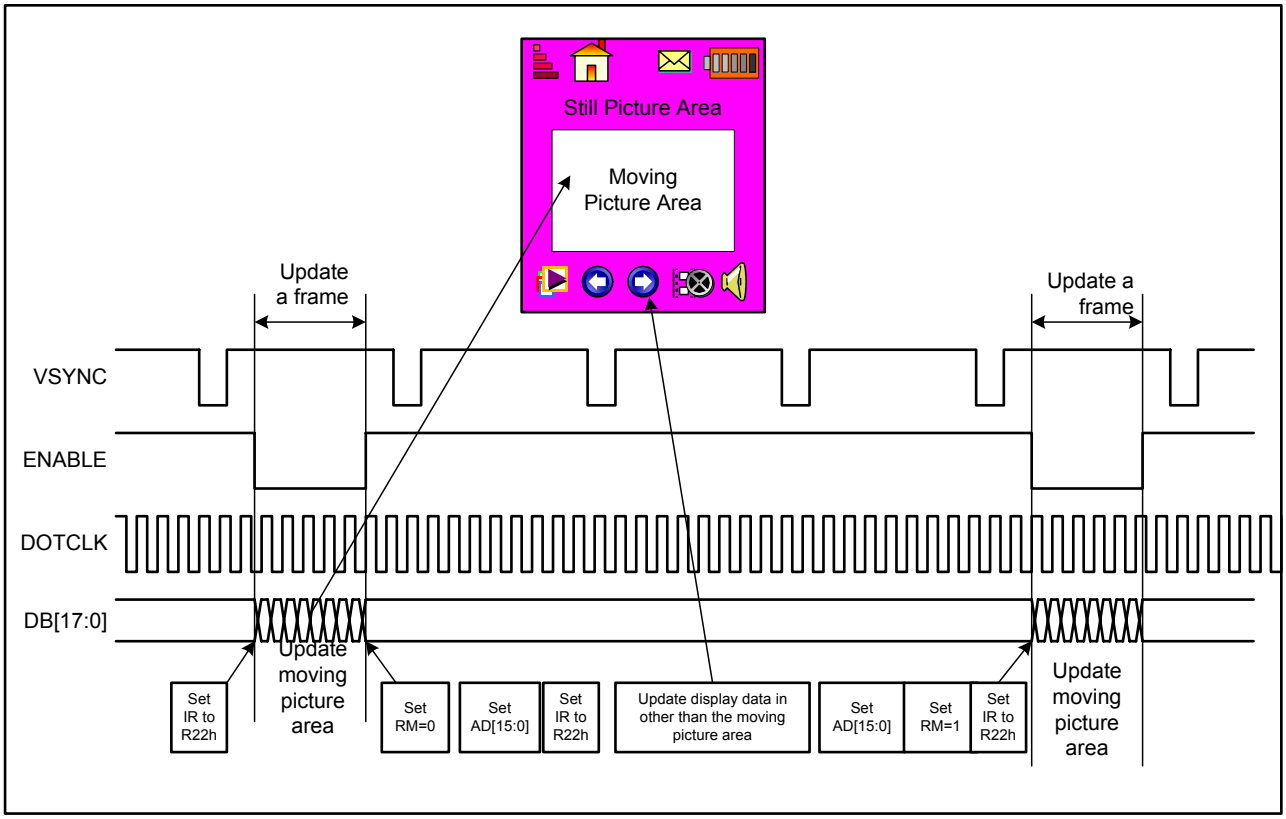


Figure18 Example of update the still and moving picture

7.5.4. 6-bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to "10". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at either IOVcc or DGND level. Registers can be set by the system interface (i80/M68/SPI).

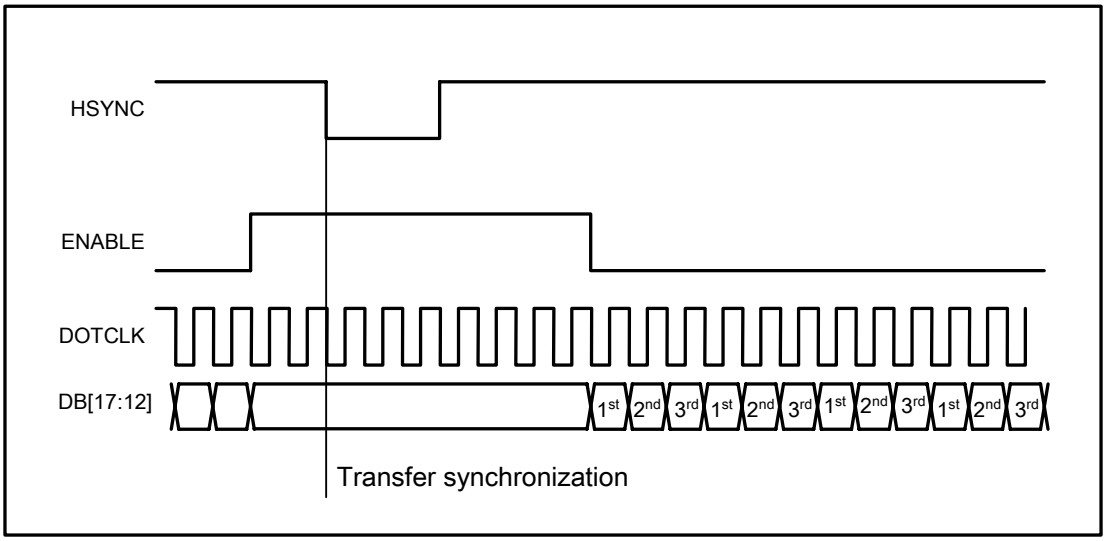
RGB interface with 6-bit data bus

	1st Transfer						2nd Transfer						3rd Transfer					
Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Data transfer synchronization in 6-bit RGB interface mode

ILI9221 has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

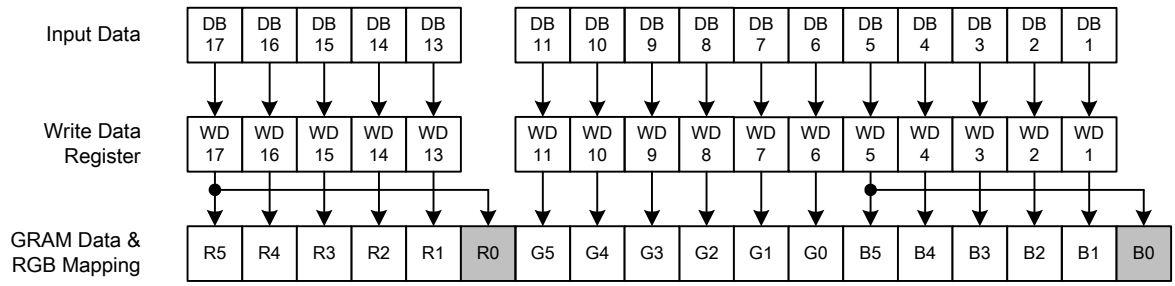
Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



7.5.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.

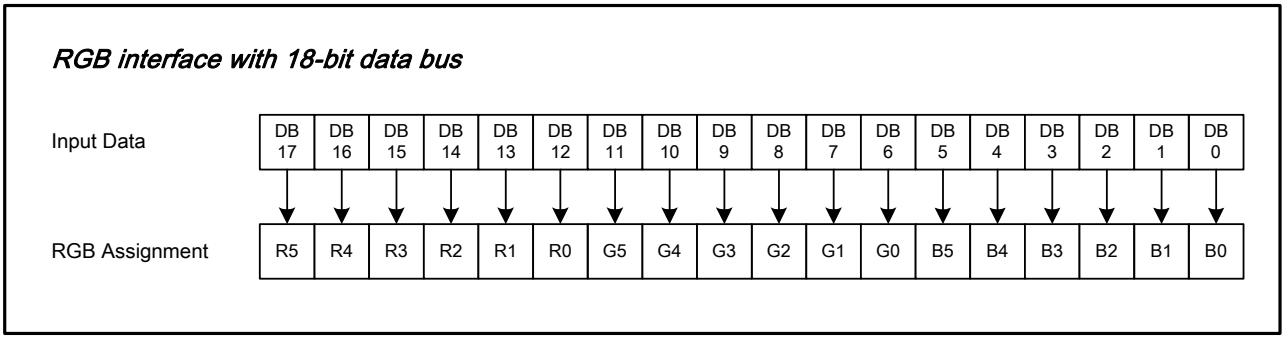
16-bit RGB Interface (65K colors)



7.5.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.

RGB interface with 18-bit data bus



Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB interface	I80/M68 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in

RGB interface mode.

4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

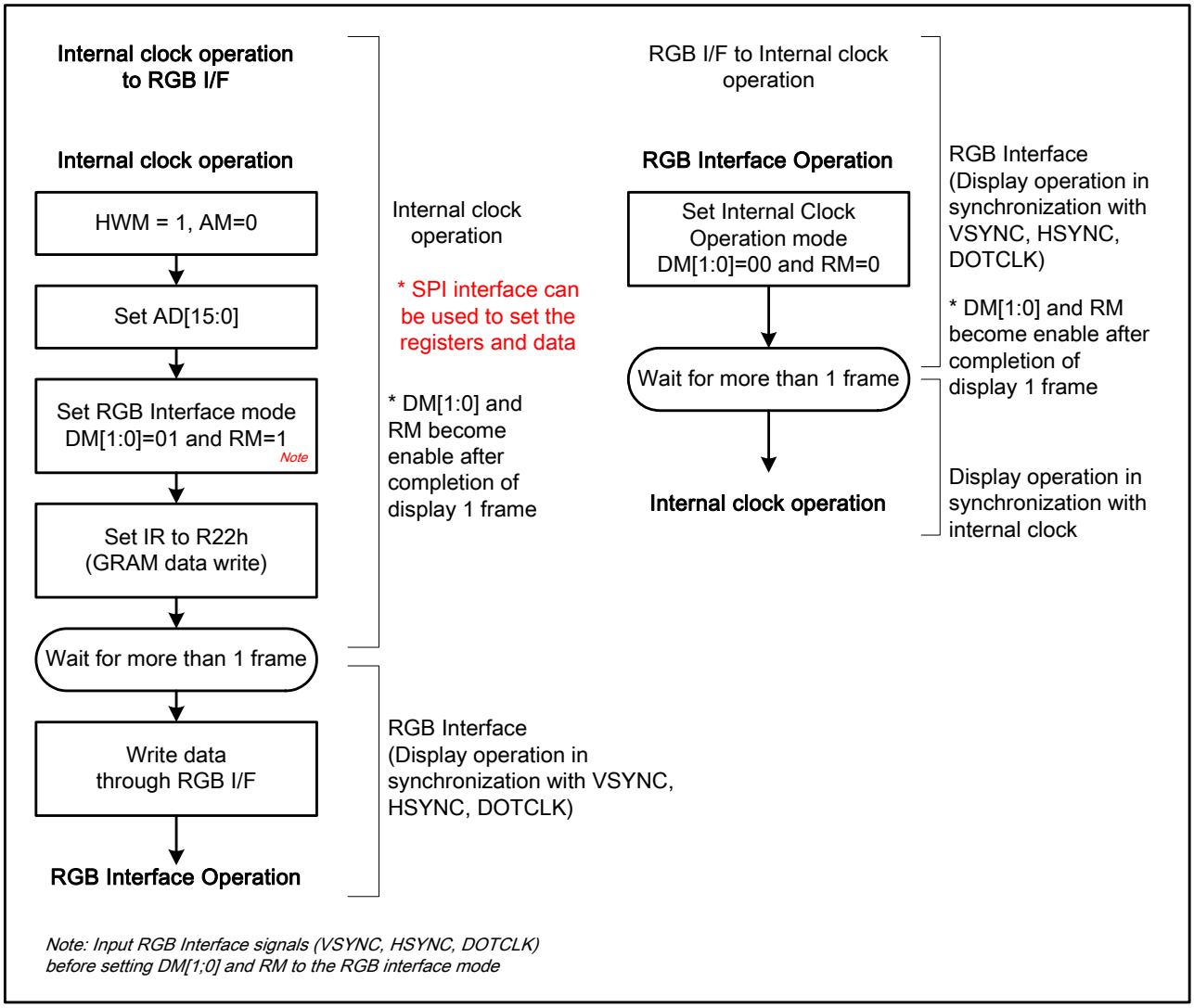


Figure19 Internal clock operation/RGB interface mode switching

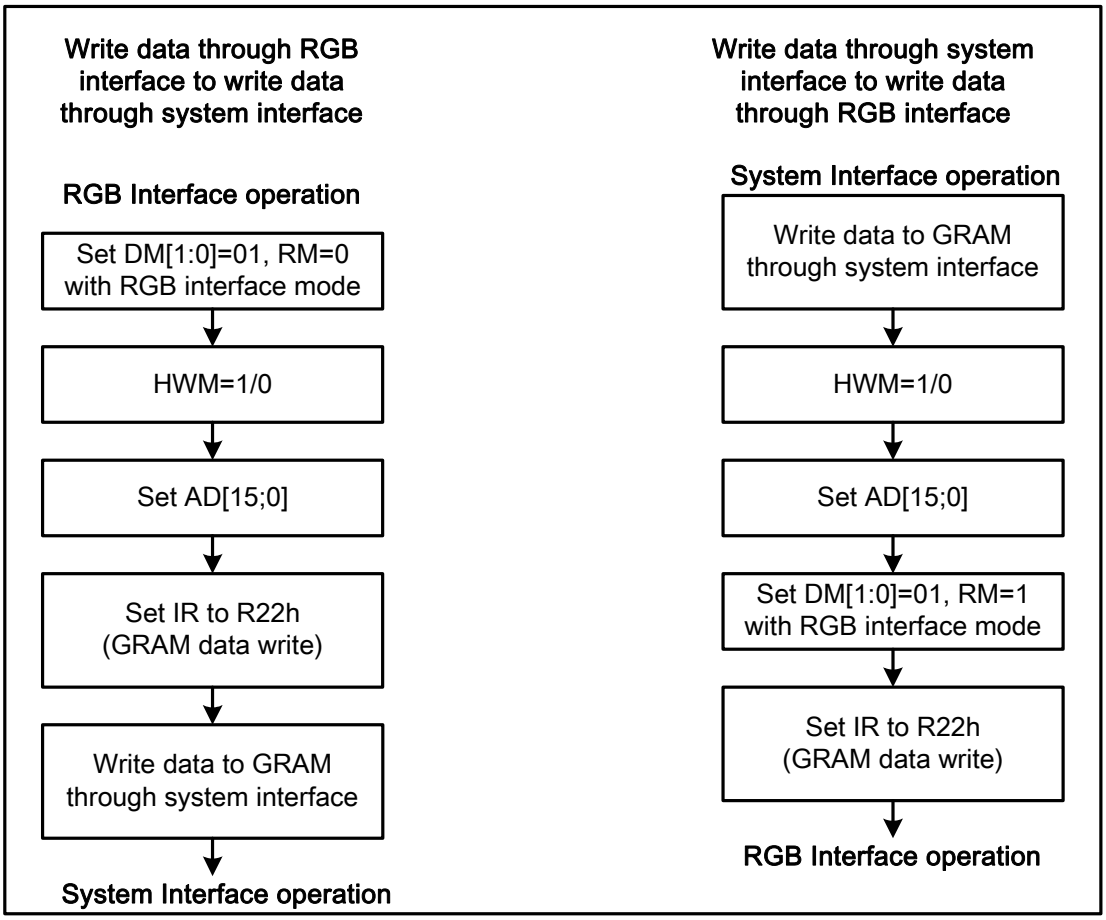


Figure20 GRAM access between system interface and RGB interface

7.6. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

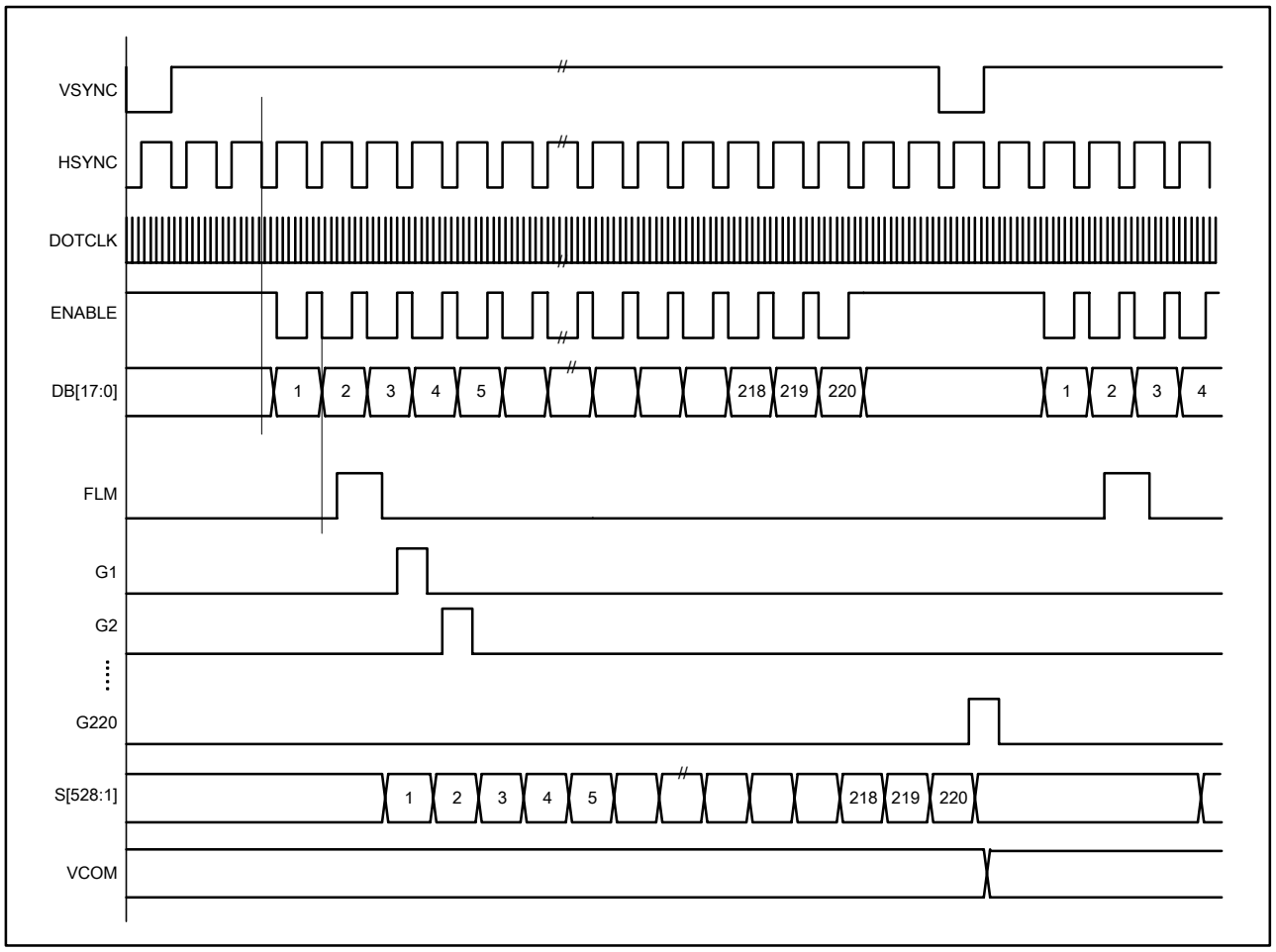


Figure21 Relationship between RGB I/F signals and LCD Driving Signals for Panel

8. Register Descriptions

8.1. Registers Access

ILI9221 adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9221 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9221. The registers of the ILI9221 are categorized into the following groups.

1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale γ-correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9221 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

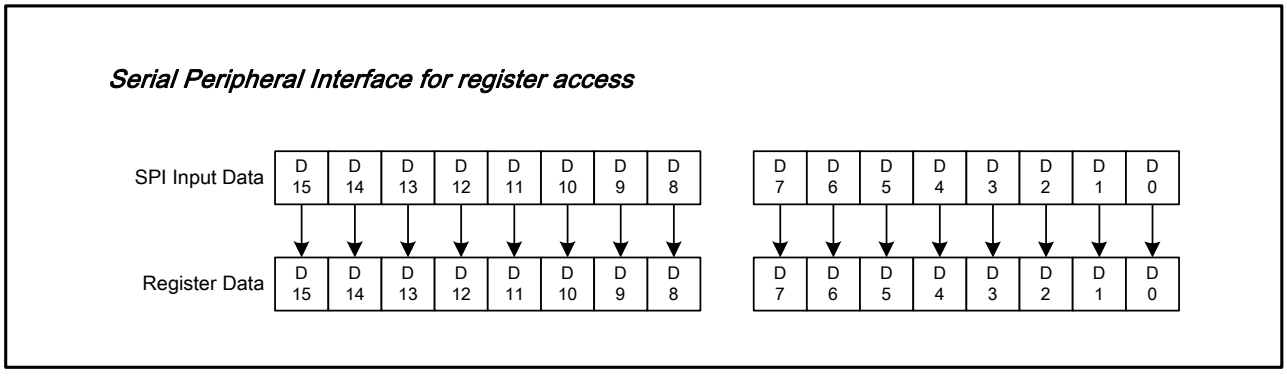
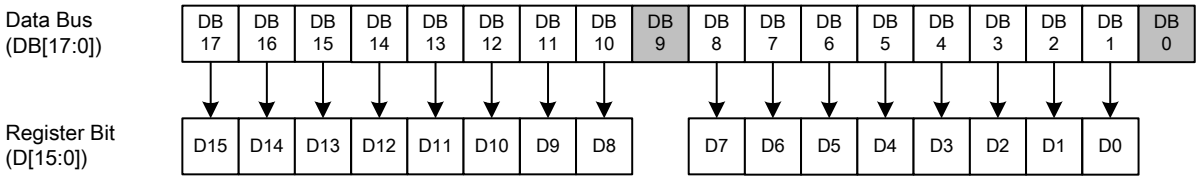
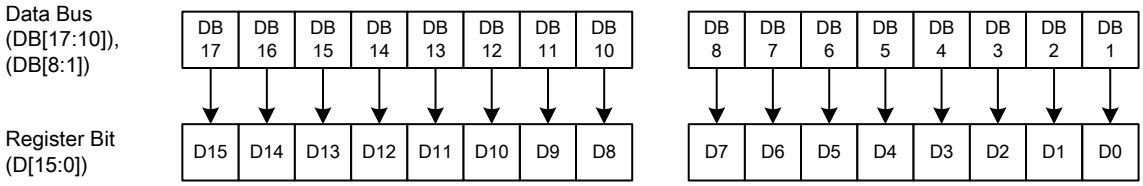


Figure22 Register Setting with Serial Peripheral Interface (SPI)

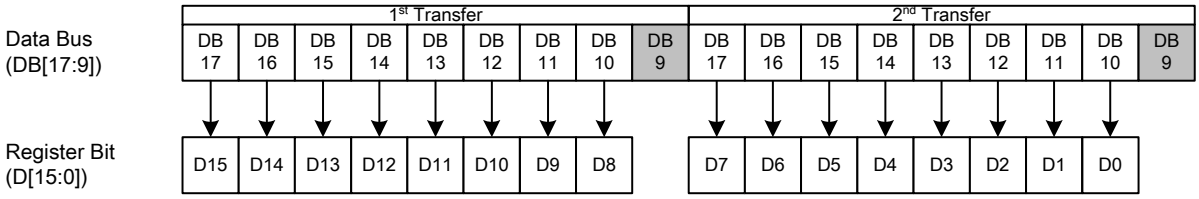
i80/M68 system 18-bit data bus interface



i80/M68 system 16-bit data bus interface



i80/M68 system 9-bit data bus interface



i80/M68 system 8-bit data bus interface/Serial peripheral interface (2/3 transmission)

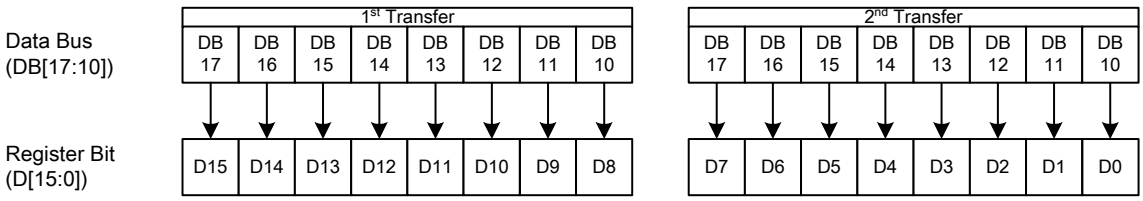


Figure23 Register setting with i80/M68 System Interface

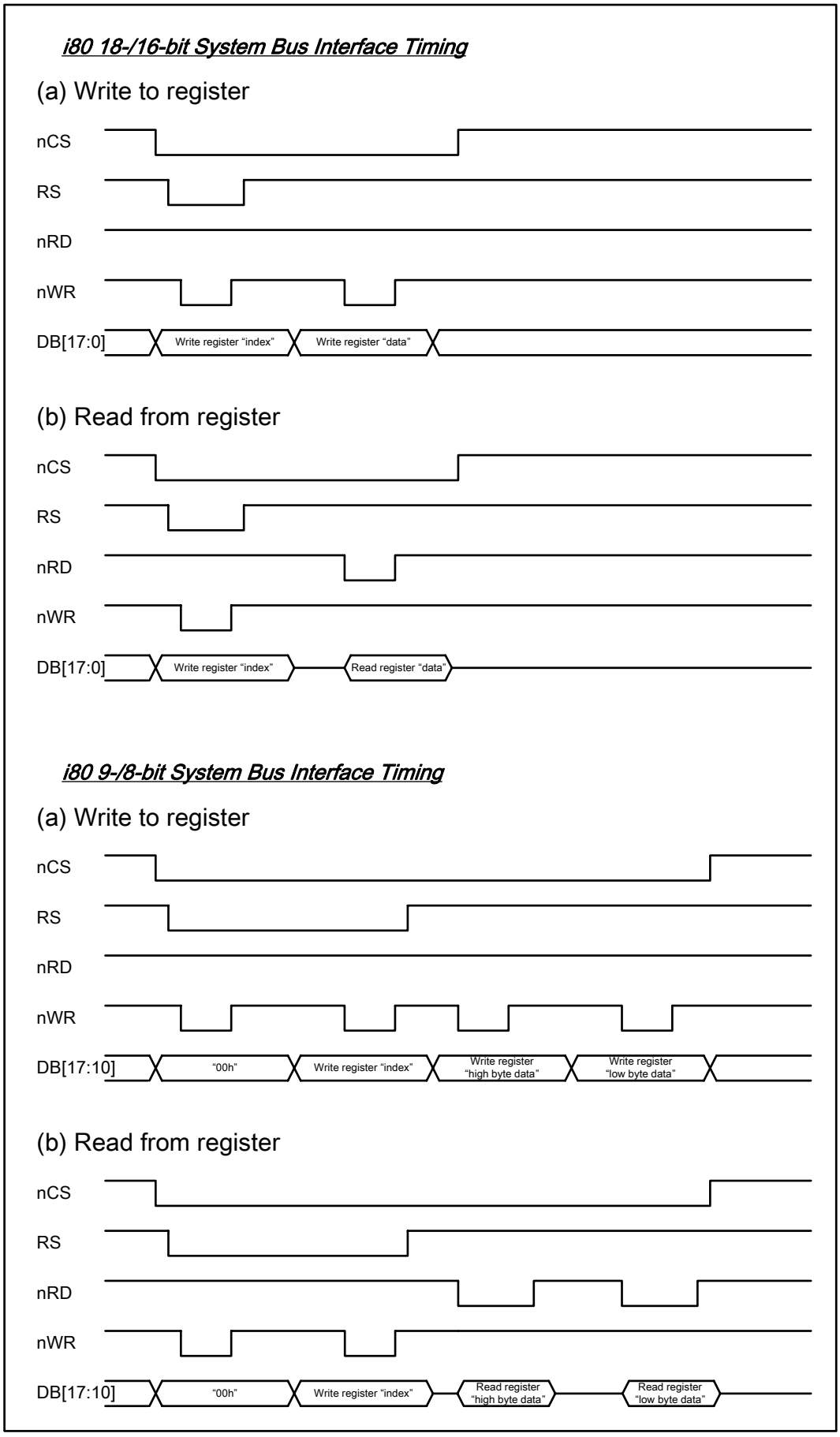


Figure 24 Register Read/Write Timing of i80 System Interface

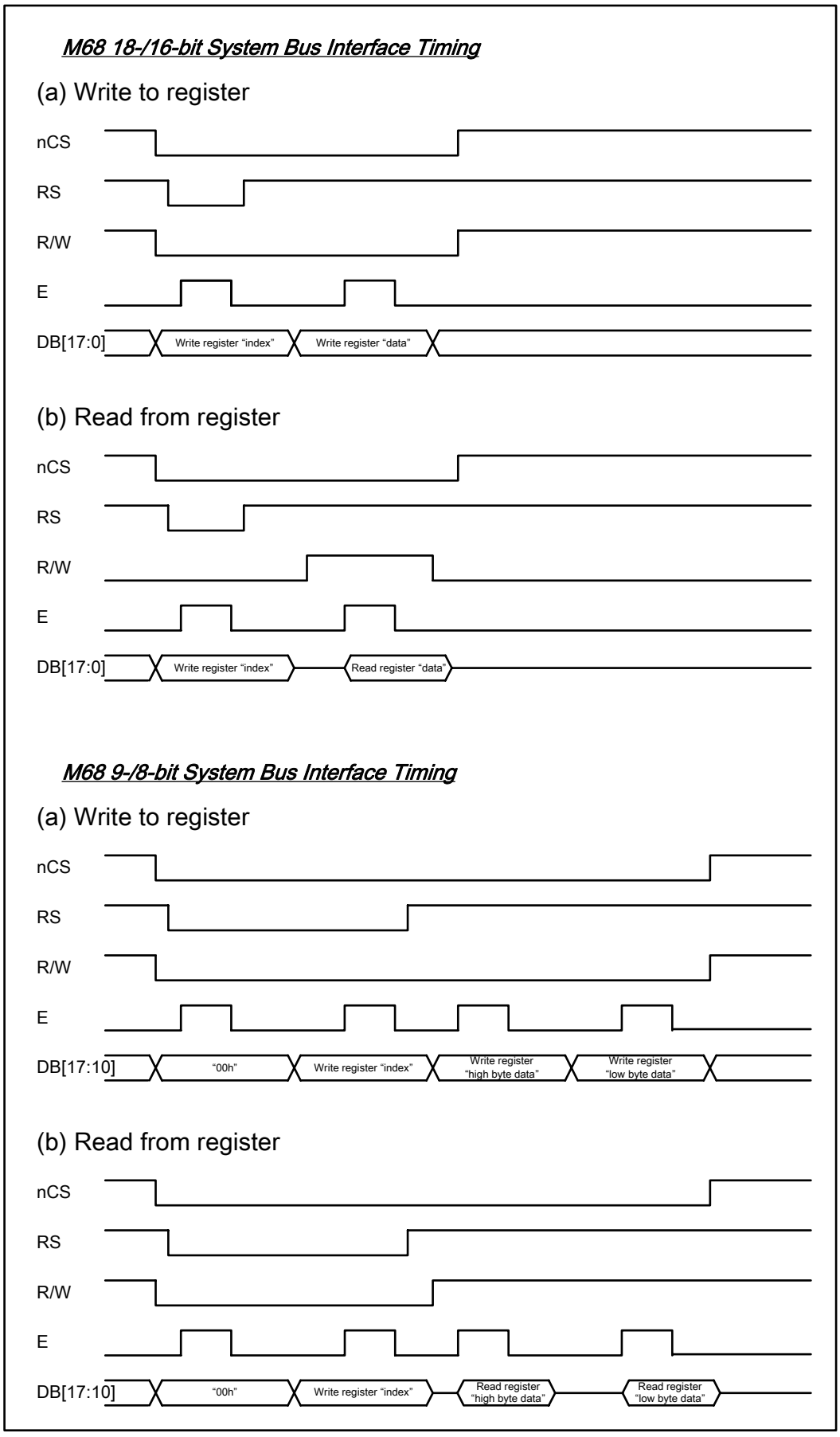


Figure 25 Register Read/Write Timing of M68 System Interface

8.2. Instruction Descriptions

No.	Registers Name	R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0		-	-	-	-	-	-	-	-	-	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	R	0		L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
00h	Start Oscillation	W	1		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	OSC
00h	Driver Code Read	R	1		1	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0
01h	Driver Output Control	W	1		0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0
02h	LCD AC Driving Control	W	1		0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0
03h	Entry Mode	W	1		TRI	DFM1	DFM0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
04h	Compare Register 1	W	1		0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0
05h	Compare Register 2	W	1		0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12
07h	Display Control 1	W	1		0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0
08h	Display Control 2	W	1		0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1		0	0	0	0	0	0	0	0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Bh	Frame Cycle Control	W	1		GD1	GD0	SDT1	SDT0	CE1	CE0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0
0Ch	External Display Interface Control	W	1		0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
10h	Power Control 1	W	1		0	SAP2	SAP	SAP0	0	BT2	BT1	BT0	0	AP2	AP1	AP0	0	DK	SLP	STB
11h	Power Control 2	W	1		0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1		0	0	0	0	0	0	0	0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1		0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
21h	RAM Address Set	W	1		AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
22h	Write Data to GRAM	W	1																	
23h	18-bit RAM Write Mask 1	W	1		0	0	WM11	WM10	WM9	WM8	WM7	WM6	0	0	WM5	WM4	WM3	WM2	WM1	WM0
24h	18-bit RAM Write Mask 2	W	1		0	0	0	0	0	0	0	0	0	0	WM17	WM16	WM15	WM14	WM13	WM12
30h	Gamma Control 1	W	1		0	0	0	0	0	MP1[2]	MP1[1]	MP1[0]	0	0	0	0	0	MP0[2]	MP0[1]	MP0[0]
31h	Gamma Control 2	W	1		0	0	0	0	0	MP3[2]	MP3[1]	MP3[0]	0	0	0	0	0	MP2[2]	MP2[1]	MP2[0]
32h	Gamma Control 3	W	1		0	0	0	0	0	MP5[2]	MP5[1]	MP5[0]	0	0	0	0	0	MP4[2]	MP4[1]	MP4[0]
33h	Gamma Control 4	W	1		0	0	0	0	0	CP1[2]	CP1[1]	CP1[0]	0	0	0	0	0	CP0[2]	CP0[1]	CP0[0]
34h	Gamma Control 5	W	1		0	0	0	0	0	MN1[2]	MN1[1]	MN1[0]	0	0	0	0	0	MN0[2]	MN0[1]	MN0[0]
35h	Gamma Control 6	W	1		0	0	0	0	0	MN3[2]	MN3[1]	MN3[0]	0	0	0	0	0	MN2[2]	MN2[1]	MN2[0]
36h	Gamma Control 7	W	1		0	0	0	0	0	MN5[2]	MN5[1]	MN5[0]	0	0	0	0	0	MN4[2]	MN4[1]	MN4[0]
37h	Gamma Control 8	W	1		0	0	0	0	0	CN1[2]	CN1[1]	CN1[0]	0	0	0	0	0	CN0[2]	CN0[1]	CN0[0]
38h	Gamma Control 9	W	1		0	0	0	OP1[4]	OP1[3]	OP1[2]	OP1[1]	OP1[0]	0	0	0	0	OP0[3]	OP0[2]	OP0[1]	OP0[0]
39h	Gamma Control 10	W	1		0	0	0	ON1[4]	ON1[3]	ON1[2]	ON1[1]	ON1[0]	0	0	0	0	ON0[3]	ON0[2]	ON0[1]	ON0[0]
40h	Gate Scan Control	W	1		0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

No.	Registers Name	R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
41h	Vertical Scroll Control	W	1		0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
42h	1st Screen Drive Position	W	1		SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
43h	2nd Screen Drive Position	W	1		SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
44h	Horizontal RAM Address Position	W	1		HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
45h	Vertical RAM Address Position	W	1		VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Means the initial value is “1"

Means the initial value is “0"

8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	-	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ R4Fh) or RAM which will be accessed.

8.2.2. Status Read (RS)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The SR bits represent the internal status of the ILI9221.

L[7:0] Indicates the position of driving line which is driving the TFT panel currently.

8.2.3. Start Oscillation (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
R	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	0	1

Set the OSC bit as ‘1’ to start the internal oscillator and as ‘0’ to stop the oscillator. Wait at least 10ms to let the frequency of oscillator stable and then do the other function setting. The device code “9221”h is read out when read this register.

8.2.4. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

VSPL: Inverts the polarity of signals from the VSYNC pin.

VSPL = ”0” : Low active.

VSPL = ”1” : High active.

HSPL: Inverts the polarity of signals from the HSYNC pin.

HSPL = ”0” : Low active.

HSPL = ”1” : High active.

DPL: Inverts the polarity of signals from the DOTCLK pin.

DPL = ”0” : Data are read on the rising edge of the DOTCLK.

DPL = ”1” : Data are read on the falling edge of the DOTCLK.

EPL: Set the polarity of the signal from the ENABLE pin in RGB interface mode. .

EPL = “0”:

ENABLE = “Low” / Write data to DB[17:0]

ENABLE = “High” / Inhibit data write operation

EPL =”1”:

ENABLE = “High” / Write data to DB[17:0]

ENABLE = “Low” / Inhibit data write operation

The following table shows the relationship between the EPL, ENABLE bits, and RAM access.

EPL	ENABLE	RAM write	RAM address
0	0	Enabled	Updated
0	1	Inhibited	Retained
1	0	Inhibited	Retained
1	1	Enabled	Updated

SS: Select the shift direction of outputs from the source driver.

When SS = 0, the shift direction of outputs is from S1 to S528

When SS = 1, the shift direction of outputs is from S528 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

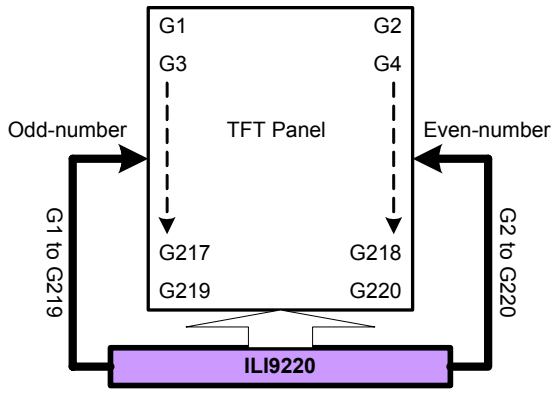
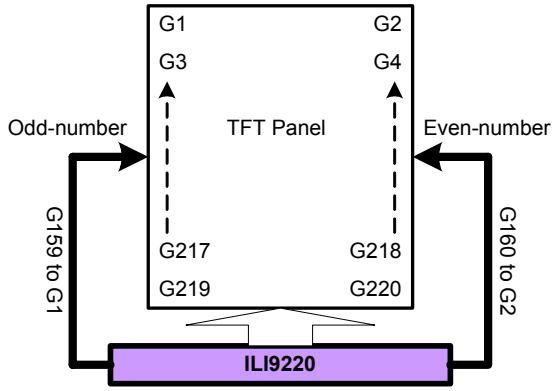
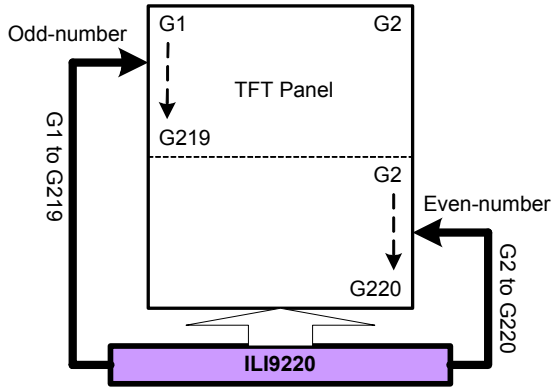
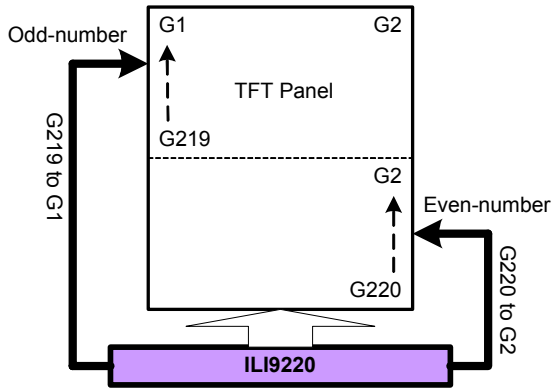
To assign R, G, B dots to the source driver pins interchangeably from S1, set SS = 0, BGR = 0.

To assign R, G, B dots to the source driver pins interchangeably from S528, set SS = 1, BGR = 1.

When changing SS or BGR bits, RAM data must be rewritten.

GS: Select the shift direction of outputs from the gate driver. The scan order is changeable in accordance to the scan mode by the gate driver. Select an optimum shift direction for the assembly.

SM: Set the scan order by the gate driver. Select an optimum scan order for the assembly.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4, …,G216 G217, G218, G219, G220
0	1		G220, G219, G218, …, G6, G5, G4, G3, G2, G1
1	0		G1, G3, G5, G7, …,G211 G213, G215, G217, G219 G2, G4, G6, G8, …,G212 G214, G216, G218, G220
1	1		G220, G218, G216, …, G10, G8, G6, G4, G2 G219, G217, G215, …, G9, G78, G5, G3, G1

NL[4:0] Set the active gate driver line to drive the liquid crystal display panel with 8 multiples as the following table. The GRAM address mapping is independent from the number of gate lines set with the NL[4:0] bits.

NL4	NL3	NL2	NL1	NL0	Display Size	Number of LCD Driver Lines	Gate Driver Used
0	0	0	0	0	528 * 8 dots	8	G1~G8
0	0	0	0	1	528 * 16 dots	16	G1~G16
0	0	0	1	0	528 * 24 dots	24	G1~G24
0	0	0	1	1	528 * 32 dots	32	G1~G32
0	0	1	0	0	528 * 40 dots	40	G1~G40
0	0	1	0	1	528 * 48 dots	48	G1~G48
0	0	1	1	0	528 * 56 dots	56	G1~G56
0	0	1	1	1	528 * 64 dots	64	G1~G64
0	1	0	0	0	528 * 72 dots	72	G1~G72
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	0	0	0	528 * 200 dots	200	G1~G200
1	1	0	0	1	528 * 208 dots	208	G1~G208
1	1	0	1	0	528 * 216 dots	216	G1~G216
1	***1***	***0***	***1***	***1***	528 * 220 dots	220	G1~G220
1	1	1	0	0	528 * 220 dots	220	G1~G220
1	1	1	0	1	528 * 220 dots	220	G1~G220
1	1	1	1	0	528 * 220 dots	220	G1~G220
1	1	1	1	1	528 * 220 dots	220	G1~G220

8.2.5. LCD Driving Waveform Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

NW[5:0] Specify the n-line inversion number. When the ILI9221 is set to generate n-line inversion waveform (B/C = “1”). The polarity is inverted for every n+1 display lines.

.**B/C** 0 : Frame/Field inversion

1 : n-line inversion

When ILI9221 is set to generate a field-inversion waveform (B/C = “0”), the polarity is inverted every field. ILI9221 inverts the driving polarity every n-line in accordance to NW and EOR bits when an n-line inversion mode is selected (B/C = “1”).

EOR: By setting EOR = “1”, the polarity of C pattern waveform (one-line inversion waveform) is inverted according to the result of EOR (exclusive OR) between the odd/even-number frame select signal and the one-line inversion signal. Set EOR = 1 when the number of lines to drive liquid crystal is not compatible with one-line inversion waveform.

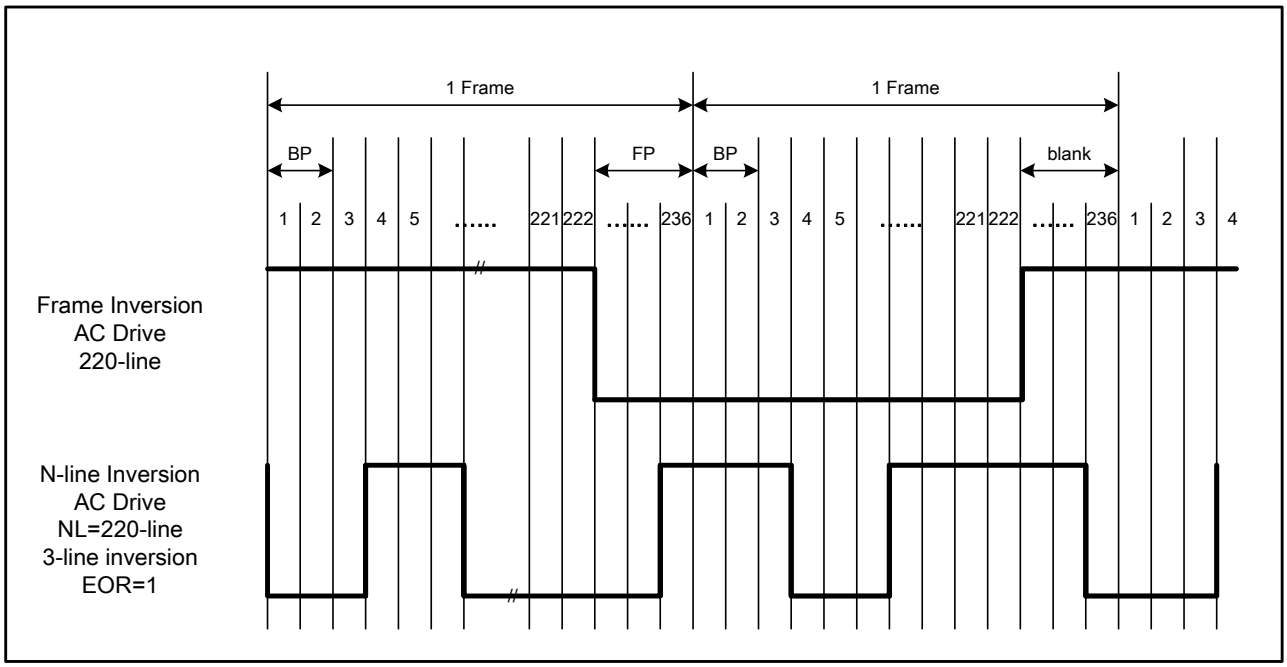


Figure 26 n-line Inversion AC Drive

FLD[1:0] Set the field number for the AC driving. The FLD bits shall be disabled in RGB Input Interface mode, when using the RGB Input Interface, set FLD[1:0]= “01”.

FLD1	FLD0	Number of fields
0	0	Setting disabled
0	1	1 field (=1 frame)
1	0	Setting disabled
1	1	3 field

GS = “0”						
FLD[1:0]	“01"	“11"				
Field / Gate	-	1	2	3	4	
G1	*	*			*	
G2	*		*			
G3	*			*		
G4	*	*			*	
G5	*		*			
G6	*			*		
G7	*	*			*	
G8	*		*			
G9	*			*		
G10	*	*			*	
	⋮	⋮	⋮	⋮	⋮	
G217	*	*		*		
G218	*		*		*	
G219	*			*		
G220	*	*			*	

GS = “1”						
FLD[1:0]	“01"	“11"				
Field / Gate	-	1	2	3	4	
G220	*	*			*	
G219	*		*			
G218	*			*		
G217	*	*			*	
G216	*		*			
G215	*			*		
G214	*	*			*	
G213	*		*			
G212	*			*		
G211	*	*			*	
	⋮	⋮	⋮	⋮	⋮	
G4	*	*		*		
G3	*		*		*	
G2	*			*		
G1	*	*			*	

Figure27 Interlace Scan of AC Drive

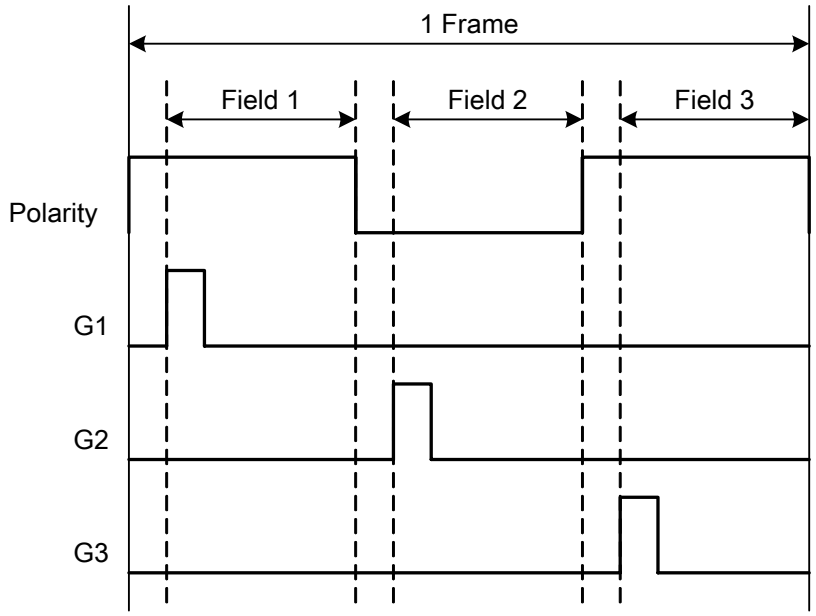


Figure28 Output Timing of Interlace Gate Signals (Three-field is selected)

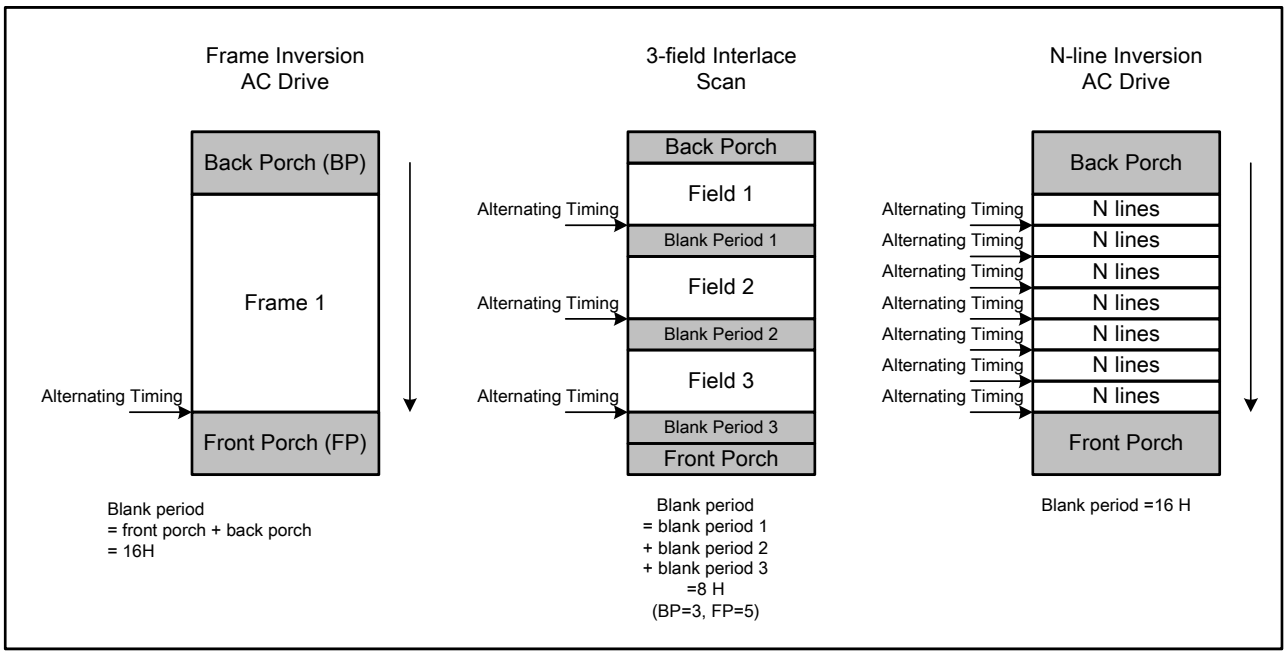


Figure29 AC Driving Alternating Timing

8.2.6. Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM1	DFM0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0

LG[2:0] Compare the data read from the GRAM or write data written from the microprocessor with the compare registers (CP[15:0] or CP[17:0]) by a compare/logical operation and write the results into GRAM. The R10h register can set the 18-/16-bit mask/compare operation. For details, see the "Graphic Operation function".

AM Control the GRAM update direction. When AM = "0", the address is updated in horizontal writing direction. When AM = "1", the address is updated in vertical writing direction. When a window area is set by registers R16h and R17h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.

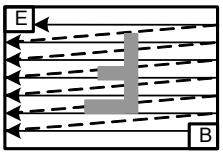
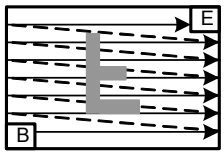
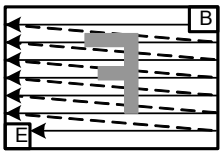
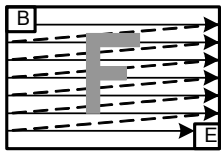
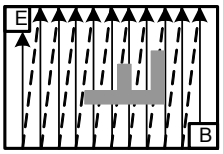
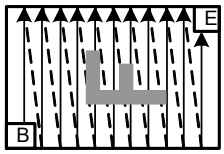
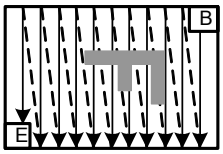
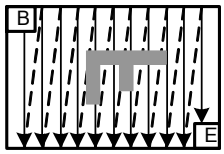
	I/D[1:0] = 00 Horizontal : decrement Vertical : decrement	I/D[1:0] = 01 Horizontal : increment Vertical : decrement	I/D[1:0] = 10 Horizontal : decrement Vertical : increment	I/D[1:0] = 11 Horizontal : increment Vertical : increment
AM = 0 Horizontal				
AM = 1 Vertical				

Figure30 GRAM Access Direction Setting

AM	I/D[1:0]	Register R21 Start Address
0/1	00	DBAFh
	01	DB00h
	10	00AFh
	11	0000h

BGR Swap the R and B order of written data. Note that the order of RGB dots in both WM[17:0] and CP[17:0] registers are automatically changed on BGR= “1”. When the BGR=1, the B and R order is swapped.

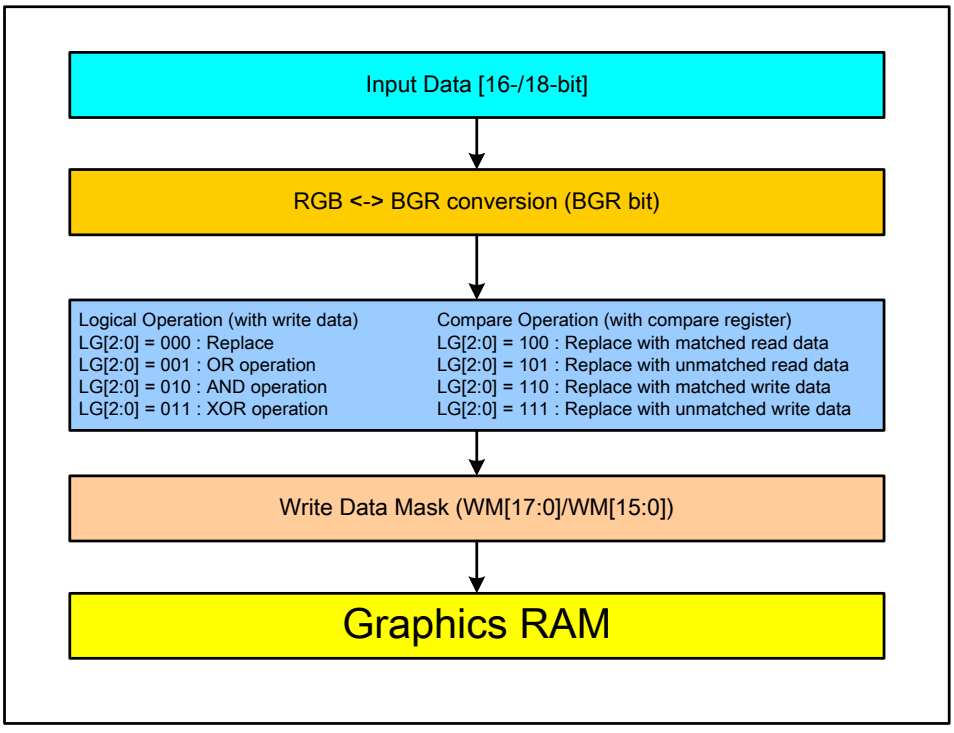


Figure31 Data Operation with Mask and Compare Function

TRI When TRI = “1”, data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = “0”.

DFM[1:0] Set the mode of transferring data to the internal RAM when TRI = “1”. See the following figures for details.

<table>
<tr><th>TRI</th><th>DFM1</th><th>DFM0</th><th>16-bit MPU System Interface Data Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MPU System Interface (1 Transfer/pixel) 65K colors available
1st Transfer: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10
2nd Transfer: DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MPU System Interface MSB Mode (2 Transfers/pixel) 262K colors available
1st Transfer: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
2nd Transfer: DB17 DB16
R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>MPU System Interface LSB Mode (2 Transfers/pixel) 262K colors available
1st Transfer: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
2nd Transfer: DB17 DB16
R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0</td></tr>
<tr><td colspan="3">others</td><td>ignored</td></tr>
</table>

Figure32 16-bit MPU System Interface Data Format

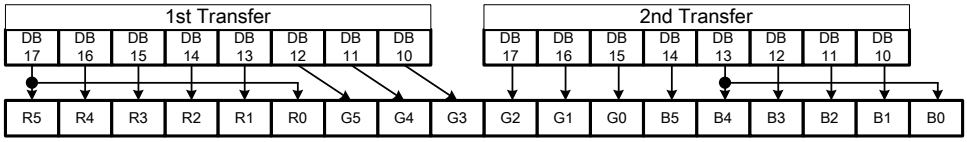
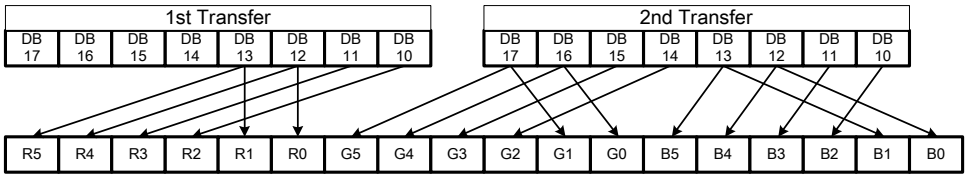
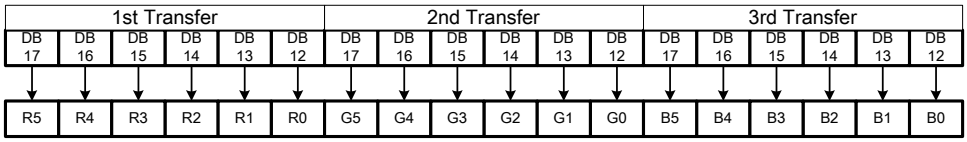
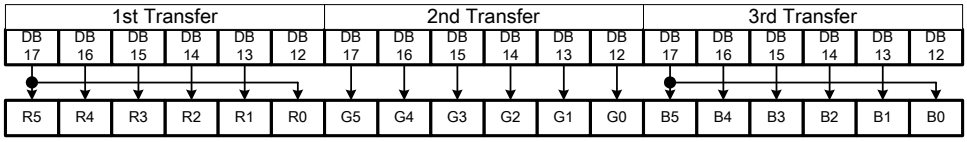
TRI	DFM1	DFM0	8-bit MPU System Interface Data Format
0	0	0	
0	0	1	
1	1	0	
1	1	1	
others			ignored

Figure33 8-bit MPU System Interface Data Format

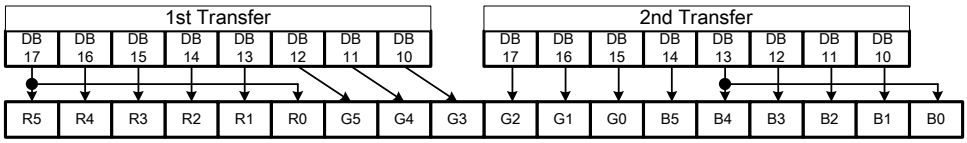
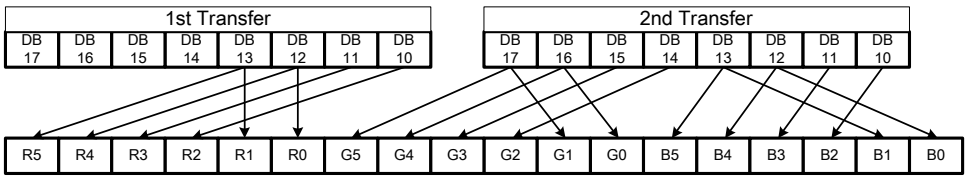
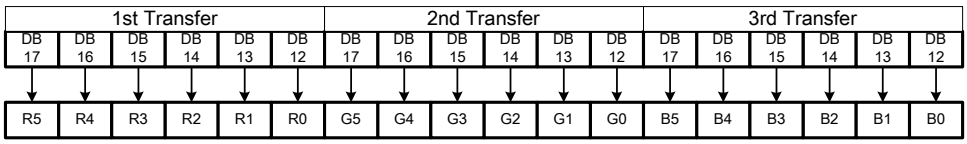
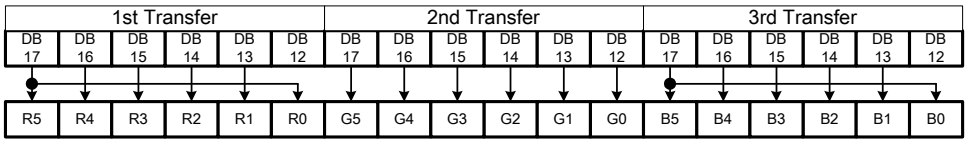
TRI	DFM1	DFM0	Serial Peripheral Interface (SPI) Data Format
0	0	0	
0	0	1	
1	1	0	
1	1	1	
others			ignored

Figure34 SPI System Interface Data Format

8.2.7. Compare Registers (R04h, R05h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0
W	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12

CP[17:0] Compare register for GRAM update. For details, see the “Graphics Operation Function” section. Note that the write mask function is always performed on 18-bit GRAM write data, but this function is not available for the RGB interface.

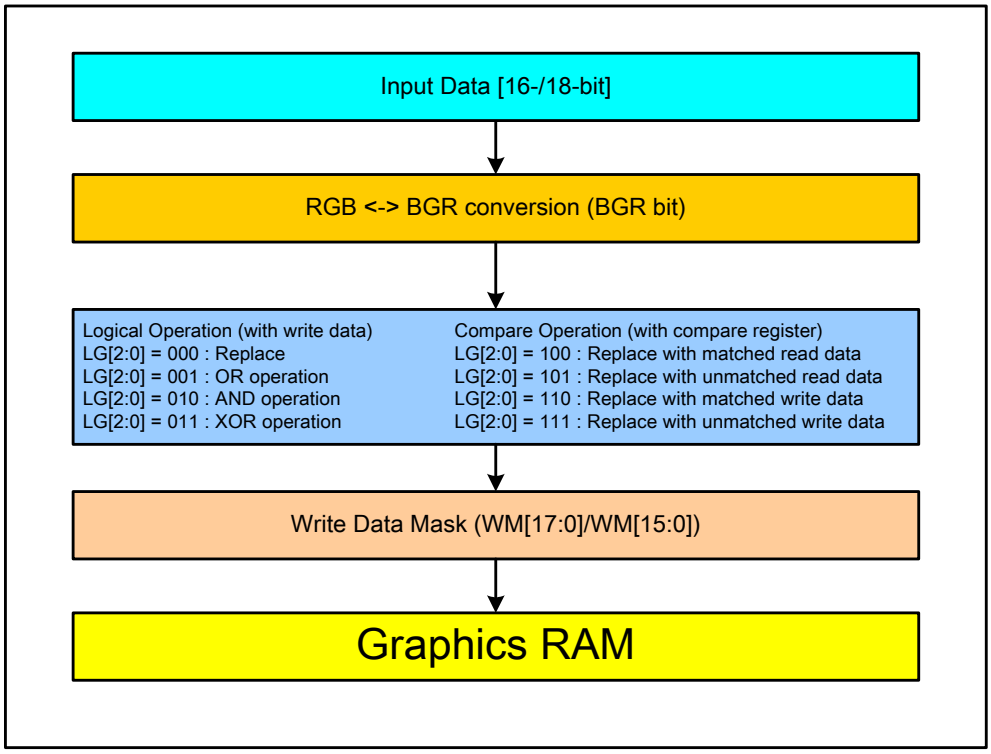


Figure35 Data Operation with Mask and Compare Function

8.2.8. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

PT[1:0] Set the source driver output in non-display area of partial display. For details, see the “Partial Display Function” section.

PT1	PT0	Source Output in Non-display Area		Gate Output in Non-display
		Positive polarity	negative polarity	
0	0	V63	V0	Refer to PTG[1:0]
0	1	disabled	disabled	-
1	0	GND	GND	Refer to PTG[1:0]
1	1	Hi-Z	Hi-Z	Refer to PTG[1:0]

VLE[2:1] When VLE1 = “1”, the first partial display window is scrolled in vertical direction. When VLE2 = “1”, the second partial display window is scrolled in vertical direction. The first and second display

windows cannot be scrolled simultaneously. This scroll function is not available for the RGB Input Interface and please set VLE[2:1]= "00".

VLE2	VLE1	1st Display window	2nd Display window
0	0	Fixed display	Fixed display
0	1	**Scrolled display**	Fixed display
1	0	Fixed display	**Scrolled display**
1	1	Setting prohibited	Setting prohibited

SPT Set SPT = "1" to display two separate partial display windows in the LCD panel. For details, see the "Partial Display Function" section. This function is not available with the RGB Input Interface. In this case, set SPT = "0".

GON and DTE Set the output level of gate driverG1 ~ G220 as follows

GON	DTE	G1 ~G220 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	**Normal Display**

CL When CL = "1", the 8-color display mode is selected. For details, see the "8-color Display Mode" section.

CL	Colors
0	262,144
1	8

REV When REV = "1", the grayscale levels can be inverted. The source output level of front and back porch periods and a blank period in partial display mode is set with the PT[1:0] bits.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V63	V0

D[1:0] Set D[1:0="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

D1	D0	Source, VCOM Output	ILI9221 internal operation	Gate drive control signal
0	0	VSS	Halt	Halt
0	1	VSS	Operate	Operate
1	0	Display	Operate	Operate
1	**1**	**Display**	**Operate**	**Operate**

Note: data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

8.2.9. Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP[3:0]/BP[3:0]

The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively.

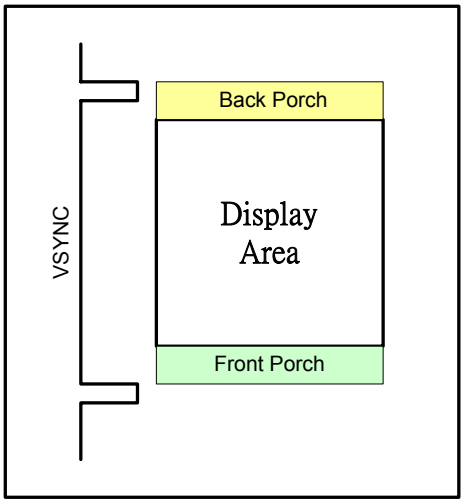
When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

FP[3:0] / BP[3:0]	Number of lines for Front Porch / Number of lines for Back Porch
0000	Setting Prohibited
0001	Setting Prohibited
0010	2 lines
0011	3 lines
0100	4 lines
0101	5 lines
0110	6 lines
0111	7 lines
1000	8 lines
1001	9 lines
1010	10 lines
1011	11 lines
1100	12 lines
1101	13 lines
1110	14 lines
1111	Setting Prohibited



Note: The output timing to the LCD is delayed by 2 lines period from the input of synchronizing signal.

Set the BP[3:0] and FP[3:0] bits as below for each operation mode

Operation Mode	Number of Interlace Scan Field	BP	FP	BP+FP
I80/M68 System Interface	**FLD[1:0] = "01"**	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
	FLD[1:0] = "11"	BP = 3 lines	FP = 5 lines	-
RGB interface		BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface		BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

8.2.10. Display Control 3 (R09h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

PTG1-0: Set the scan mode by the gate driver in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	**0**	**Normal scan**	**Set with the PT[1:0] bits**	**VcomH/VcomL**
0	1	VGL (Fixed)	Set with the PT[1:0] bits	VcomH/VcomL
1	0	Interval scan	Set with the PT[1:0] bits	VcomH/VcomL
1	1	Setting Disabled	-	-

ISC[3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG[1:0]=”10”. Then scan cycle is set as odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC3	ISC3	ISC3	Scan Cycle	f_{FLM}=70 Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frame	50ms
0	0	1	0	5 frame	84ms
0	0	1	1	7 frame	117ms
0	1	0	0	9 frame	150ms
0	1	0	1	11 frame	184ms
0	1	1	0	13 frame	217ms
0	1	1	1	15 frame	251ms
1	0	0	0	17 frame	284ms
1	0	0	1	19 frame	317ms
1	0	1	0	21 frame	351ms
1	0	1	1	23 frame	384ms
1	1	0	0	25 frame	418ms
1	1	0	1	27 frame	451ms
1	1	1	0	29 frame	484ms
1	1	1	1	31 frame	518ms

8.2.11. Frame Cycle Control (R0Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	GD1	GD0	SDT1	SDT0	CE1	CE0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

RTN[3:0] Set the clock cycle number of one display line.

RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
0	0	0	0	16 clocks
0	0	0	1	17 clocks
0	0	1	0	18 clocks
0	0	1	1	19 clocks
0	1	0	0	20 clocks
0	1	0	1	21 clocks
0	1	1	0	22 clocks
0	1	1	1	23 clocks
1	0	0	0	24 clocks
1	0	0	1	25 clocks
1	0	1	0	26 clocks
1	0	1	1	27 clocks
1	1	0	0	28 clocks
1	1	0	1	29 clocks
1	1	1	0	30 clocks
1	1	1	1	31 clocks

DIV[1:0] The internal operation is synchronized with the clock, which is divided with the division ratio setting by the DIV[1:0] bits.

Set the RTN and DIV bits to adjust frame frequency. If the number of lines for driving liquid crystal is

changed, the frame frequency must also be changed. In RGB interface mode, the DIV[1:0] bits are disabled.

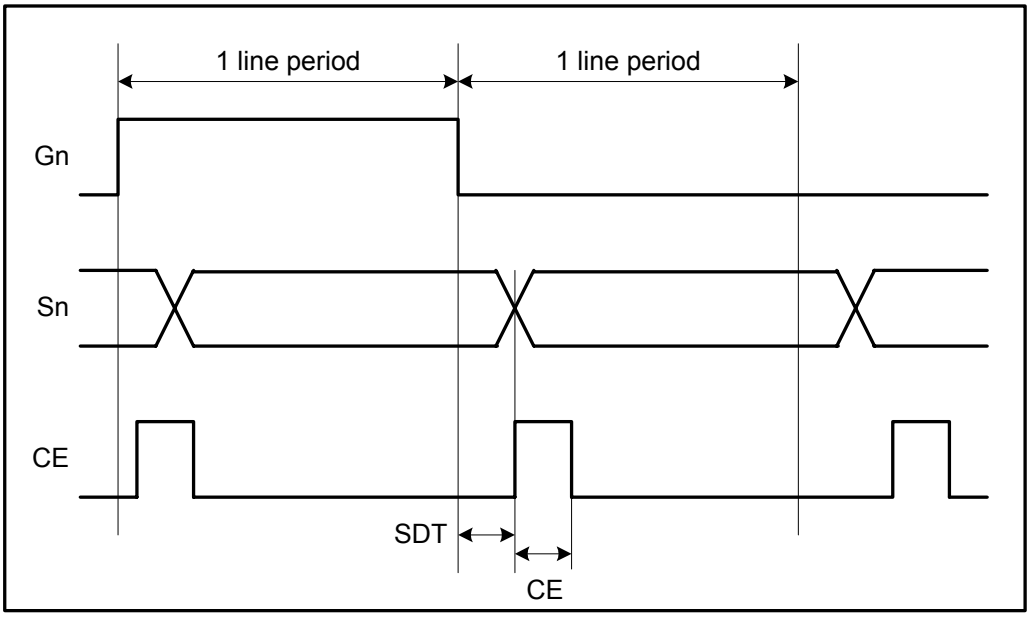
DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Formula to calculate frame frequency

$$Frame\ Rate = \frac{f_{osc.}}{Clock\ cycles\ per\ line \times division\ ratio \times (Lines + BP + FP)}$$

$f_{osc.}$: frequency if RC oscillation.
Clock cycles per line : RTN bits
Division ratio : DIV bits
Lines : number of lines for driving the LCD panel.
FP: Front porch lines
BP; Back porch lines

CE[1:0]: CE period can be set with CE[1:0].



CE1	CE0	System Interface Mode (Clock source: R-C Oscillator)	RGB Interface Mode (Clock source: DOTCLK)
0	0	Not CE	Not CE
0	1	1 clock cycle	8 clock cycle
1	0	2 clock cycle	16 clock cycle
1	1	3 clock cycle	24 clock cycle

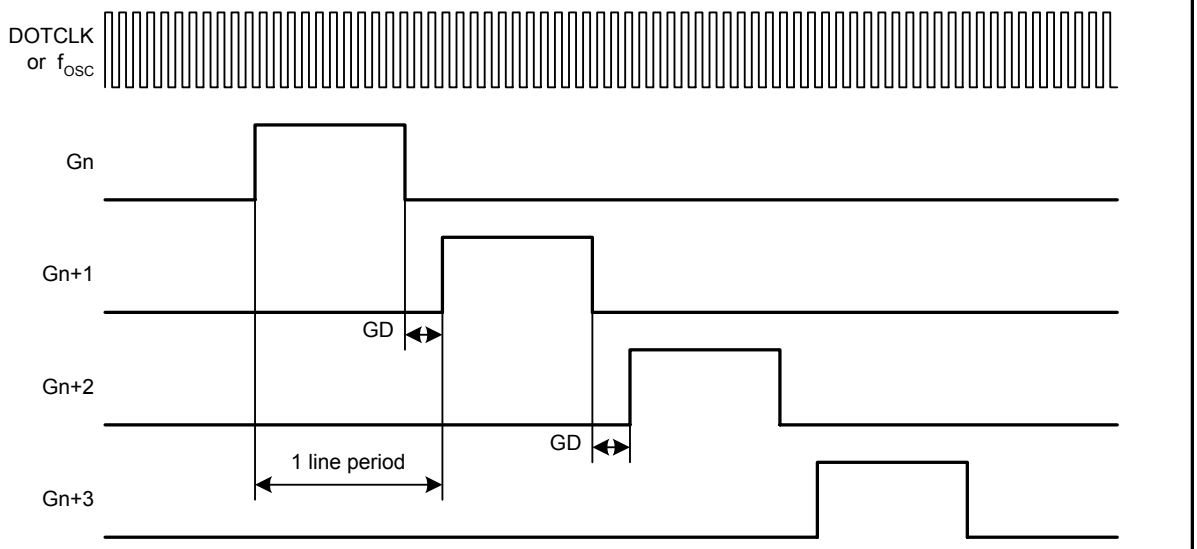
SDT[1:0] Set the delay time for the source output timing from the falling edge of gate output signal by the number of following clocks.

Source output delay period			
SDT1	**SDT0**	**System Interface Mode (Clock source: R-C Oscillator)**	**RGB Interface Mode (Clock source: DOTCLK)**
0	0	1 clock	8 clocks
0	1	2 clocks	16 clocks
1	0	3 clocks	24 clocks
1	1	4 clocks	32 clocks

Note1: The source output delay time is measured from the falling edge of the CL1.

GD[1:0] Set the non-overlap period between adjacent gate drivers.

Gate output non-overlap period setting			
GD1	**GD0**	**System Interface Mode (Clock source: R-C Oscillator)**	**RGB Interface Mode (Clock source: DOTCLK)**
0	0	1 clock	8 clock
0	1	4 clocks	32 clocks
1	0	6 clocks	48 clocks
1	1	8 clocks	64 clocks



Non-overlap time between two adjacent gate driver output

8.2.12. RGB Input Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RIM[1:0] Select the data bus width of RGB interface modes.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)

0	1	16-bit RGB interface (one transfer/pixel)
1	0	6-bit RGB interface (three transfers/pixel)
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

DM[1:0] Select the display operation mode.

DM1	DM0	Display Interface
0	0	Internal system clock
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	Internal system clock interface/VSYNC interface
1	RGB interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0]
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
Rewrite still picture area while Displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1) Registers are set only via the system interface or SPI interface.

Note 2) Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

8.2.13. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	SAP2	SAP	SAP0	0	BT2	BT1	BT0	0	AP2	AP1	AP0	0	DK	SLP	STB

SAP[2:0] Set the driving capability of source driver.

Set a larger driving capability to obtain better display quality, but the power consumption also increases.

SAP[2:0]	Constant current in operational amplifier
000	Halt
001	Setting disabled
010	0.62
011	0.71
100	1
101	1.25
110	1.43
111	Setting disabled

Note: The constant current in the table is shown as the ratio to the constant current when SAP[2:0] = "100".

BT[2:0] The output factor of step-up circuit is selected. Adjust scale factor of the step-up circuit by the voltage used. Lower amplification of the step-up circuit consumes less current.

BT2	BT1	BT0	Circuit1 DDVDH	Circuit4 VCL	Circuit2 VGH	Circuit3 VGL	Capacitor Connection Pins
0	0	0	2 x VCI1	-1 x VCI1	6 x VCI1	-5 x VCI1	DDVDH, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	0	1	2 x VCI1	-1 x VCI1	6 x VCI1	-4 x VCI1	DDVDH, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	0	2 x VCI1	-1 x VCI1	6 x VCI1	-3 x VCI1	DDVDH, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	1	2 x VCI1	-1 x VCI1	5 x VCI1	-5 x VCI1	DDVDH, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	0	2 x VCI1	-1 x VCI1	5 x VCI1	-4 x VCI1	DDVDH, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	1	2 x VCI1	-1 x VCI1	5 x VCI1	-3 x VCI1	DDVDH, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	0	2 x VCI1	-1 x VCI1	4 x VCI1	-4 x VCI1	DDVDH, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	1	2 x VCI1	-1 x VCI1	4 x VCI1	-3 x VCI1	DDVDH, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B

Note: The step-up factors of VGH are derived from VCI1 when DDVDH and VCI2 are shorted. The conditions of DDVDH≦ 5.5V and VGH ≦16.5V must be satisfied.

AP[2:0] Adjust the driving capability of step-up circuit 1. When the driving capability is set to larger, the step-up voltage will be more stable and the display quality will also be better. When the AP[2:0] is set “000” and the display is turned off, the current consumption can be reduced by turn off the operational amplifier and step-up circuit operation.

AP2	AP1	AP0	Amount of current operational amplifier
0	0	0	Stop
0	0	1	ignore
0	1	0	0.50 * Iout
0	1	1	0.75 * Iout
1	0	0	**1.00 * Iout**
1	0	1	1.25 * Iout
1	1	0	1.50 * Iout
1	1	1	ignore

DK: Control the ON/OFF operation of step-up circuit 1 (for Source Driver/VCOM voltage).

DK	Operation of step-up circuit 1
0	ON
1	OFF

SLP: When SLP = 1, ILI9221 enters the sleep mode and the display operation stops except the R-C oscillator to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following two instructions.

a. Sleep mode cancel (SLP = “0”)

b. Start oscillation

STB: When STB = 1, ILI9221 enters the standby mode and the display operation completely stops and all the internal operations halt including the internal R-C oscillator. Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = “0”)

b. Start oscillation

In the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

8.2.14. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

VC[2:0] Set the rate applied to Vci to generate the reference voltage **REGP** for the VGAM1OUT and VCI1 levels.

VC2	VC1	VC0	Internal reference voltage REGP of VGAM1OUT and Vci1
0	0	0	Vci
0	0	1	0.92 x Vci
0	1	0	0.87 x Vci
0	1	1	0.83 x Vci
1	0	0	0.76 x Vci
1	0	1	0.73 x Vci
1	1	0	Setting disabled
1	1	1	Setting disabled

DC02	DC01	DC00	Step-up circuit1 step-up frequency (f_{DCDC1})
0	0	0	Oscillation clock / 8
0	0	1	Oscillation clock / 16
0	1	0	Oscillation clock / 32
0	1	1	Oscillation clock / 64
1	0	0	Oscillation clock / 128
1	0	1	Setting disabled
1	1	0	Setting disabled
1	1	1	Setting disabled

DC12	DC11	DC10	Step-up circuit2 step-up frequency (f_{DCDC2})
0	0	0	Oscillation clock / 16
0	0	1	Oscillation clock / 32
0	1	0	Oscillation clock / 64
0	1	1	Oscillation clock / 128
1	0	0	Oscillation clock / 256
1	0	1	Setting disabled
1	1	0	Setting disabled
1	1	1	Setting disabled

Note: Be sure fDCDC1≥fDCDC2 when setting DC02-00, DC12-10.

8.2.15. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0

PON: Control ON/OFF of circuit3 (VGL) output.

Set PON = “0” to disable VGL output

Set PON = “1” to enable VGL output

VRH[3:0] Set the amplifying rate (1.33 ~ **2.775**) of REGP applied to output the VGAM1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VRH3	VRH2	VRH1	VRH0	VGAM1OUT
0	0	0	0	REGP x 1.33
0	0	0	1	REGP x 1.45
0	0	1	0	REGP x 1.55
0	0	1	1	REGP x 1.65
0	1	0	0	REGP x 1.75
0	1	0	1	REGP x 1.80
0	1	1	0	REGP x 1.85
0	1	1	1	Halt

VRH3	VRH2	VRH1	VRH0	VGAM1OUT
1	0	0	0	REGP x 1.90
1	0	0	1	REGP x 2.175
1	0	1	0	REGP x 2.325
1	0	1	1	REGP x 2.475
1	1	0	0	REGP x 2.625
1	1	0	1	REGP x 2.700
1	1	1	0	REGP x 2.775
1	1	1	1	Halt

8.2.16. Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

VCOMG When VCOMG = “1”, ILI9221 can output a negative voltage for VCOML (1.0V~ –Vci+0.5V Max.). When VCOMG = “0”, ILI9221 halts the negative voltage output to save power and the VCOML voltage is connected to AGND. When VCOMG = “0”, the VDV[4:0] setting function is disabled and the amplitude of VCOM is adjusted by the VCM[4:0]. Please set PON = “1” before setting VCOMG =“1”.

VDV[4:0] Set the amplitude of VCOM AC voltage. If VCOMG = “0”, the VDV[4:0] bits are disabled.

VCM[4:0] Set the VCOMH level.

If the VCOMH is adjusted by an external resistor from VCOMR, please set VCM[4:0] = “11111” to disable the internal VCOMH setting.

VCM[4:0]						VDV[4:0]					
VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	VGAM1OUT x 0.40	0	0	0	0	0	VGAM1OUT x 0.60
0	0	0	0	1	VGAM1OUT x 0.42	0	0	0	0	1	VGAM1OUT x 0.63
0	0	0	1	0	VGAM1OUT x 0.44	0	0	0	1	0	VGAM1OUT x 0.66
0	0	0	1	1	VGAM1OUT x 0.46	0	0	0	1	1	VGAM1OUT x 0.69
0	0	1	0	0	VGAM1OUT x 0.48	0	0	1	0	0	VGAM1OUT x 0.72
0	0	1	0	1	VGAM1OUT x 0.50	0	0	1	0	1	VGAM1OUT x 0.75
0	0	1	1	0	VGAM1OUT x 0.52	0	0	1	1	0	VGAM1OUT x 0.78
0	0	1	1	1	VGAM1OUT x 0.54	0	0	1	1	1	VGAM1OUT x 0.81
0	1	0	0	0	VGAM1OUT x 0.56	0	1	0	0	0	VGAM1OUT x 0.84
0	1	0	0	1	VGAM1OUT x 0.58	0	1	0	0	1	VGAM1OUT x 0.87
0	1	0	1	0	VGAM1OUT x 0.60	0	1	0	1	0	VGAM1OUT x 0.90
0	1	1	1	1	VGAM1OUT x 0.62	0	1	1	1	1	VGAM1OUT x 0.93
0	1	1	0	0	VGAM1OUT x 0.64	0	1	1	0	0	VGAM1OUT x 0.96
0	1	1	0	1	VGAM1OUT x 0.66	0	1	1	0	1	VGAM1OUT x 0.99
0	1	1	1	0	VGAM1OUT x 0.68	0	1	1	1	0	VGAM1OUT x 1.02
0	1	1	1	1	Halt internal volume adjustment. Adjust with a external variable resistor (VR) from VCOMR	0	1	1	1	1	Setting disabled
1	0	0	0	0	VGAM1OUT x 0.70	1	0	0	0	0	VGAM1OUT x 1.05
1	0	0	0	1	VGAM1OUT x 0.72	1	0	0	0	1	VGAM1OUT x 1.08
1	0	0	1	0	VGAM1OUT x 0.74	1	0	0	1	0	VGAM1OUT x 1.11
1	0	0	1	1	VGAM1OUT x 0.76	1	0	0	1	1	VGAM1OUT x 1.14
1	0	1	0	0	VGAM1OUT x 0.78	1	0	1	0	0	VGAM1OUT x 1.17
1	0	1	0	1	VGAM1OUT x 0.80	1	0	1	0	1	VGAM1OUT x 1.20
1	0	1	1	0	VGAM1OUT x 0.82	1	0	1	1	0	VGAM1OUT x 1.23
1	0	1	1	1	VGAM1OUT x 0.84	1	0	1	1	1	Setting disabled
1	1	0	0	0	VGAM1OUT x 0.86	1	1	0	0	0	Setting disabled
1	1	0	0	1	VGAM1OUT x 0.88	1	1	0	0	1	Setting disabled
1	1	0	1	0	VGAM1OUT x 0.90	1	1	0	1	0	Setting disabled
1	1	0	1	1	VGAM1OUT x 0.92	1	1	0	1	1	Setting disabled
1	1	1	0	0	VGAM1OUT x 0.94	1	1	1	0	0	Setting disabled
1	1	1	0	1	VGAM1OUT x 0.96	1	1	1	0	1	Setting disabled

1	1	1	1	0	VGAM1OUT x 0.98	1	1	1	1	0	Setting disabled
1	1	1	1	1	Halt internal volume adjustment. Adjust with a external variable resistor (VR) from VCOMR	1	1	1	1	1	Setting disabled

Note1: Adjust VGAM1OUT and VCM[4:0] so that VCOMH are set within the range 3.0 ~ (VGH – 0.5)V
Note2: Adjust VGAM1OUT and VDV[4:0] so that the amplitude of VCOM are set to 6.0V or less.

8.2.17. RAM Address Set (R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD[15:0] Set the initial value of address counter (AC).

The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

Note1: When the RGB interface is selected (RM = "1"), the address AD[15:0] is set to the address counter every frame on the falling edge of VSYNC.

Note2: When the internal clock operation or the VSYNC interface mode is selected (RM = "0"), the address AD[15:0] is set to address counter when update register R21.

Note3: The R21 register value shall be set based on the GRAM written direction (R03 register) and the reference start address setting is as the following table.

AM	I/D[1:0]	Register R21 Start Address
0/1	00	DBAFh
	01	DB00h
	10	00AFh
	11	0000h

8.2.18. Write Data to GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																	

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

8.2.19. Read Data from GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																	

RD[17:0] Read 18-bit data from GRAM through the read data register (RDR).

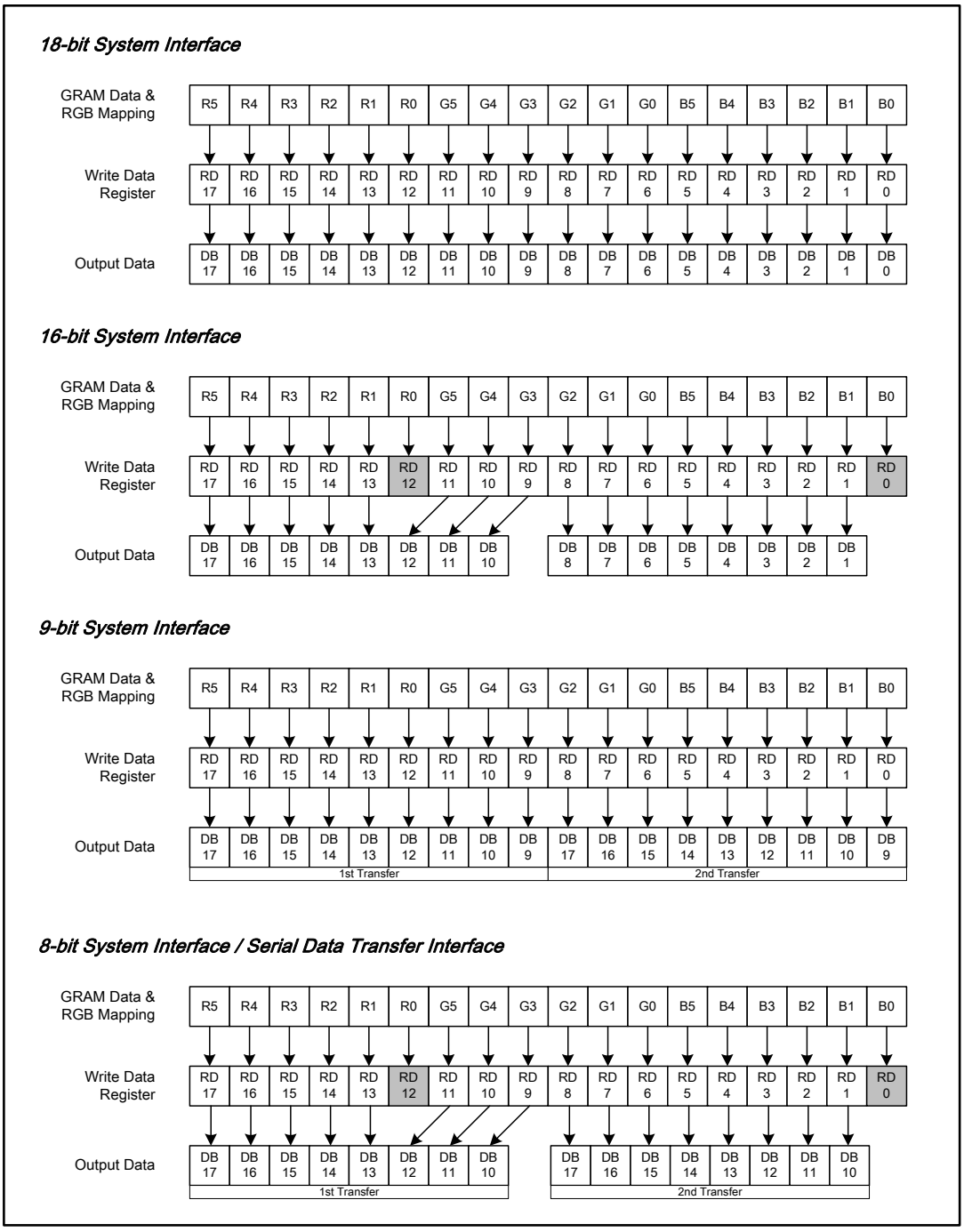


Figure 36 Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit Interface Mode

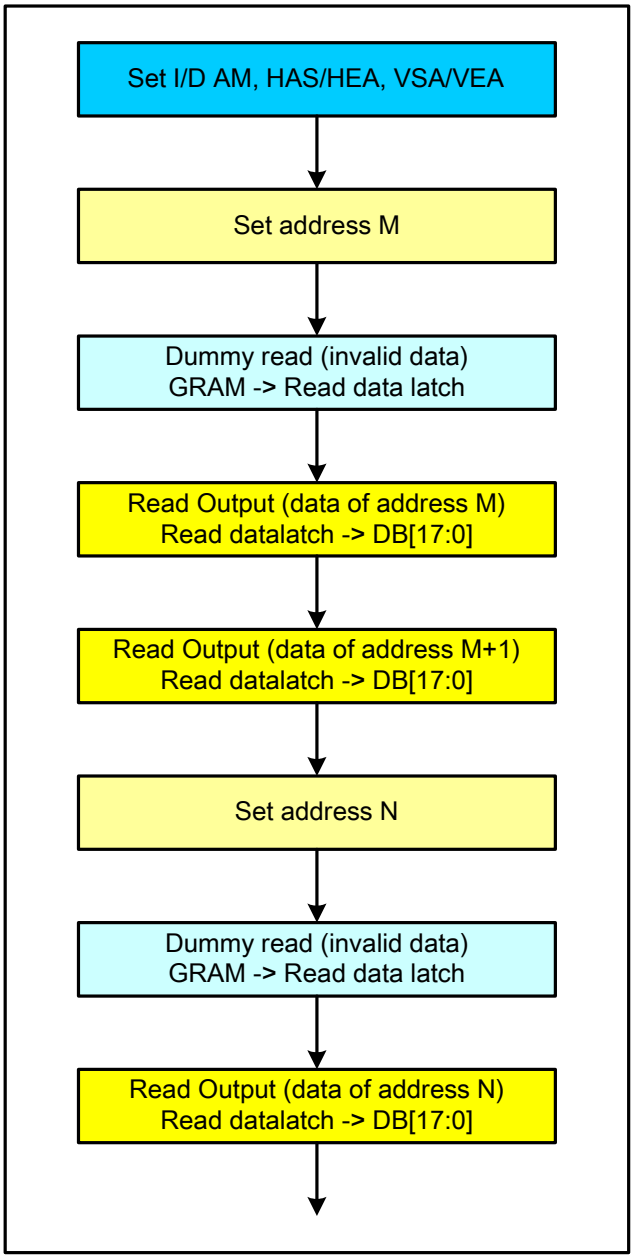


Figure 37 GRAM Data Read Back Flow Chart

8.2.20. RAM Write Mask (R23h, R24h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	WM11	WM10	WM9	WM8	WM7	WM6	0	0	WM5	WM4	WM3	WM2	WM1	WM0
W	1	0	0	0	0	0	0	0	0	0	0	WM17	WM16	WM15	WM14	WM13	WM12

WM[17:0] Write-mask data in units of bits before writing data to the GRAM. For example, if WM17 = “1”, the MSB of the write data is masked so that the MSB is not written over to the GRAM data. In the same manner, when the WM16~WM0 bits are set to “1”, the corresponding bits of the write data are masked and not written over to the GRAM data. For details, see the “Graphics Operation Function” section.

Note that the write mask function is always performed on 18-bit GRAM write data. This function is not available with the RGB interface.

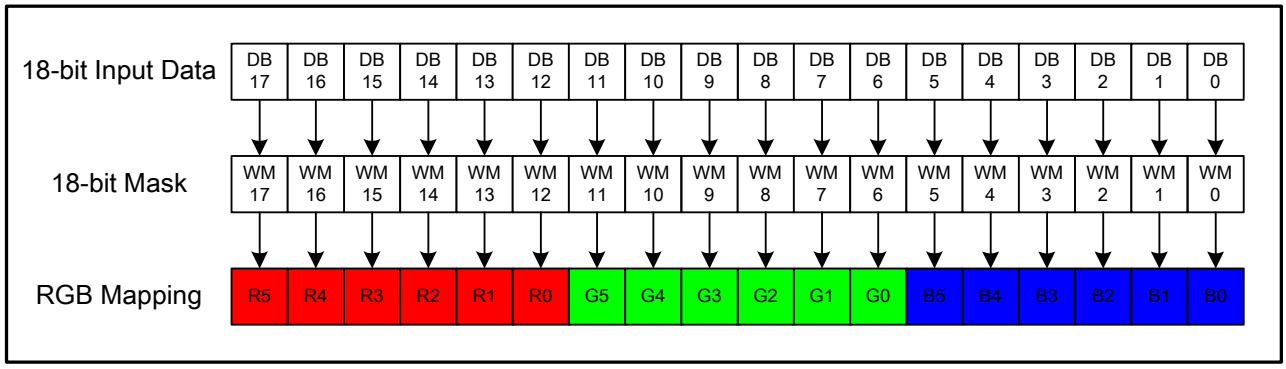


Figure 38 GRAM write with 18-bit data mask

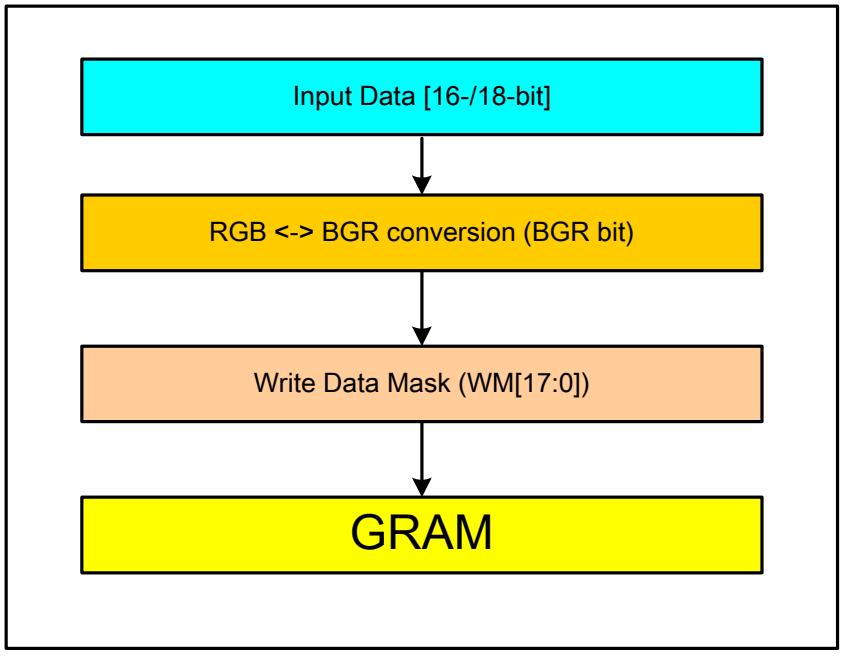


Figure 39 GRAM data map with mask and BGR conversion

8.2.21. Gamma Control (R30h ~ R39h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R30h	W	1	0	0	0	0	0	MP1[2]	MP1[1]	MP1[0]	0	0	0	0	0	MP0[2]	MP0[1]	MP0[0]
R31h	W	1	0	0	0	0	0	MP3[2]	MP3[1]	MP3[0]	0	0	0	0	0	MP2[2]	MP2[1]	MP2[0]
R32h	W	1	0	0	0	0	0	MP5[2]	MP5[1]	MP5[0]	0	0	0	0	0	MP4[2]	MP4[1]	MP4[0]
R33h	W	1	0	0	0	0	0	CP1[2]	CP1[1]	CP1[0]	0	0	0	0	0	CP0[2]	CP0[1]	CP0[0]
R34h	W	1	0	0	0	0	0	MN1[2]	MN1[1]	MN1[0]	0	0	0	0	0	MN0[2]	MN0[1]	MN0[0]
R35h	W	1	0	0	0	0	0	MN3[2]	MN3[1]	MN3[0]	0	0	0	0	0	MN2[2]	MN2[1]	MN2[0]
R36h	W	1	0	0	0	0	0	MN5[2]	MN5[1]	MN5[0]	0	0	0	0	0	MN4[2]	MN4[1]	MN4[0]
R37h	W	1	0	0	0	0	0	CN1[2]	CN1[1]	CN1[0]	0	0	0	0	0	CN0[2]	CN0[1]	CN0[0]
R38h	W	1	0	0	0	OP1[4]	OP1[3]	OP1[2]	OP1[1]	OP1[0]	0	0	0	0	OP0[3]	OP0[2]	OP0[1]	OP1[0]
R39h	W	1	0	0	0	ON1[4]	ON1[3]	ON1[2]	ON1[1]	ON1[0]	0	0	0	0	ON0[3]	ON0[2]	ON0[1]	ON1[0]

MP5-0[2:0] : γ fine adjustment register bits for positive polarity

CP1-0[2:0] : γ gradient adjustment register bits for positive polarity

MN5-0[2:0] : γ fine adjustment register bits for negative polarity

CN1-0[2:0] : γ gradient adjustment register bits for negative polarity

OP0[3:0]/OP1[4:0] : amplitude adjustment register bits for positive polarity

ON0[3:0]/ON1[4:0] : amplitude average adjustment register bits for negative polarity

For details "γ -Correction Function" section.

8.2.22. Gate Scan Control (R40h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

SCN[4:0] The ILI9221 allows specifying the gate line from which the gate driver starts scan by setting the SCN[4:0] bits.

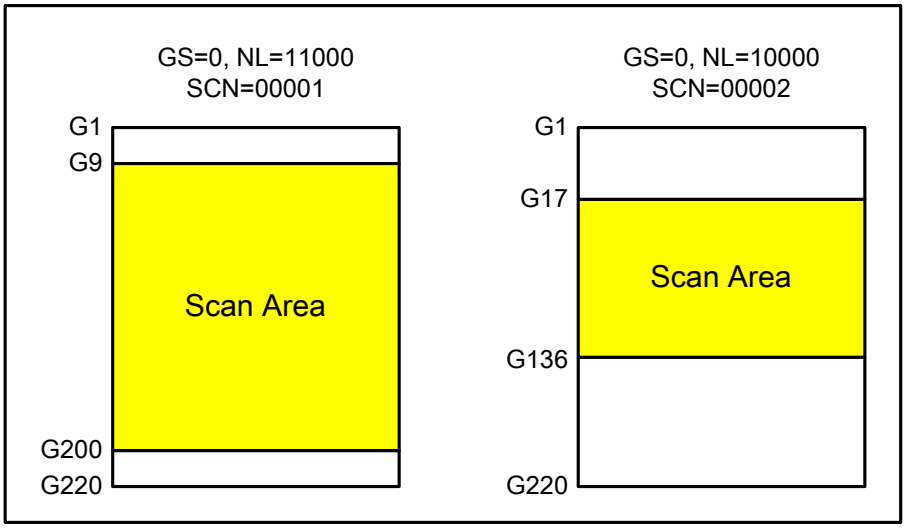


Figure 40 Scanning Start Position for Gate Driver

Note: Don't set NL[4:0], SCN[4:0] over the end position of gate line (G220)

Note: Set NL[4:0] and SCN[4:0] to let the number for the end position of the gate line scans will not exceed 220.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G220	G1	G220
0	0	0	0	1	G9	G212	G17	G204
0	0	0	1	0	G17	G204	G33	G188
0	0	0	1	1	G25	G196	G49	G172
0	0	1	0	0	G33	G188	G65	G156
0	0	1	0	1	G41	G180	G81	G140
0	0	1	1	0	G49	G172	G97	G124
0	0	1	1	1	G57	G164	G113	G108
0	1	0	0	0	G65	G156	G129	G92
0	1	0	0	1	G73	G148	G145	G76
0	1	0	1	0	G81	G140	G161	G60
0	1	0	1	1	G89	G132	G177	G44
0	1	1	0	0	G97	G124	G193	G28
0	1	1	0	1	G105	G116	G209	G12
0	1	1	1	0	G113	G108	G2	G219
0	1	1	1	1	G121	G100	G18	G203
1	0	0	0	0	G129	G92	G34	G187
1	0	0	0	1	G137	G84	G50	G171
1	0	0	1	0	G145	G76	G66	G155
1	0	0	1	1	G153	G68	G82	G139
1	0	1	0	0	G161	G60	G98	G123
1	0	1	0	1	G169	G52	G114	G107
1	0	1	1	0	G177	G44	G130	G91
1	0	1	1	1	G185	G36	G146	G75
1	1	0	0	0	G193	G28	G162	G59
1	1	0	0	1	G201	G20	G178	G43
1	1	0	1	0	G209	G12	G194	G27
1	1	0	1	1	G217	G4	G210	G11

8.2.23. Vertical Scroll Control (R41h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL[7:0] Set the scrolling amount of an image on the screen in vertical direction. The scrolling amount can be set from 0 line to 220 lines. The start position for displaying the image is shifted vertically by the number of lines set with the VL[7:0] bits. The part of the image, which is scrolled out from the end line (the 220th line) as a result of scrolling, is displayed from the 1st line of the physical display. The VL[7:0] bits are enabled when either first display vertical scroll enable bit VLE1 or the second display vertical scroll enable bit VLE2 is set to "1". When VLE[2:1] = "00", the image on the screen is displayed at the position set with the SS and SE bits. The vertical scrolling function is not available with the external display interface.

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling Lines

0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

8.2.24. 1st Screen Drive Position (R42h) and 2nd Screen Drive Position (R43h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS1[7:0] Set the position of the start line from which the first display window starts. The gate driver starts scan from the line of the number set with the SS1[7:0] bits + 1.

SE1[7:0] Set the position of the end line at which the first display ends. The gate driver ends scan at the line of the number set with the SE1[7:0] bits + 1. For instance, when SS1[7:0] = “07”h and SE1[7:0] =“10”h, the first display is shown on the gate lines from G8 to G17, and gate lines G1 to G7 and G18 thereafter are driven to show a blank screen. Be sure that SS1[7:0] ≤ SE1[7:0] ≤ “DB”H. For details, see the “Partial Display Function” section.

SS2[7:0] Set the position of the start line from which the second display starts. The gate driver starts scan from the line of the number set with the SS2[7:0] bits + 1. The second display is shown when SPT = “1”.

SE2[7:0] Set the position of the end line at which the second display ends. The gate driver ends scan at the line of the number set with the SE2[7:0] bits + 1. For instance, when SPT = “1”, and SS2[7:0] = “20”h, SE2[7:0] = “4F”h, the second display is shown on the gate lines from G33 to G80.

Be sure that SS1[7:0] ≤ SE1[7:0] < SS2[7:0] ≤ SE2[7:0] ≤ “DB”h. For details, see the “Partial Display Function” section.

8.2.25. Horizontal and Vertical RAM Address Position (R44h, R45h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

HSA[7:0]/HEA[7:0] HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00”h ≤ HSA[7:0]< HEA[7:0] ≤ “AF”h.

VSA[7:0]/VEA[7:0] VSA[7:0] and VEA[7:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure “00”h ≤ VSA[7:0]< VEA[7:0] ≤ “DB”h.

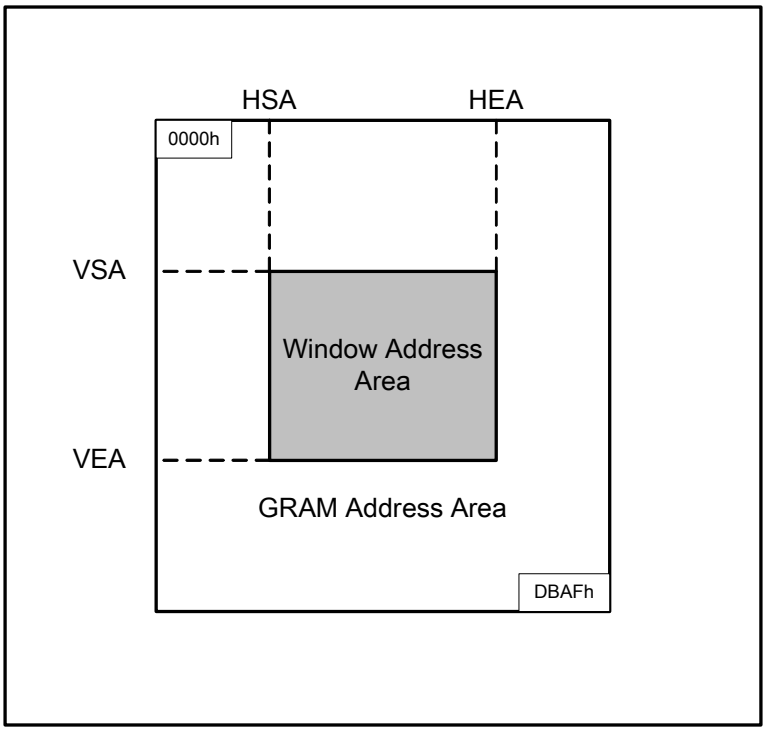


Figure 41 GRAM Access Range configuration

“00”h ≤HAS[7:0] ≤HEA[7:0] ≤”AF”h
“00”h ≤VSA[7:0] ≤VEA[7:0] ≤”DB”h

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

9. Reset Function

The ILI9221 is internally initialized with RESET input. During the reset period, the ILI9221 is in busy state, and neither access to instructions nor to GRAM data from the MPU is accepted. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the frequency of RC oscillation stabilizes (for 10 ms). During this period, neither access to the internal GRAM nor initial instruction setting is allowed.

Initial state of GRAM data

GRAM data are not automatically initialized with a RESET input. Initialize the internal GRAM by software during a display-off period (D1-0 = “00”).

Initial state of output pins

1. LCD driver (source outputs): All pins output the GND level (Halt)
2. Vcom1/2/11/21: Output the GND level (Halt)
3. LCD driver (gate outputs): All pins output the GND level (Halt)
4. FLM: Output the GND level (Halt)
5. Oscillator: Oscillate

10. GRAM Address Map & Read/Write

ILI9221 has an internal graphics RAM (GRAM) of 87,120 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80/M68 system, SPI and RGB interfaces.

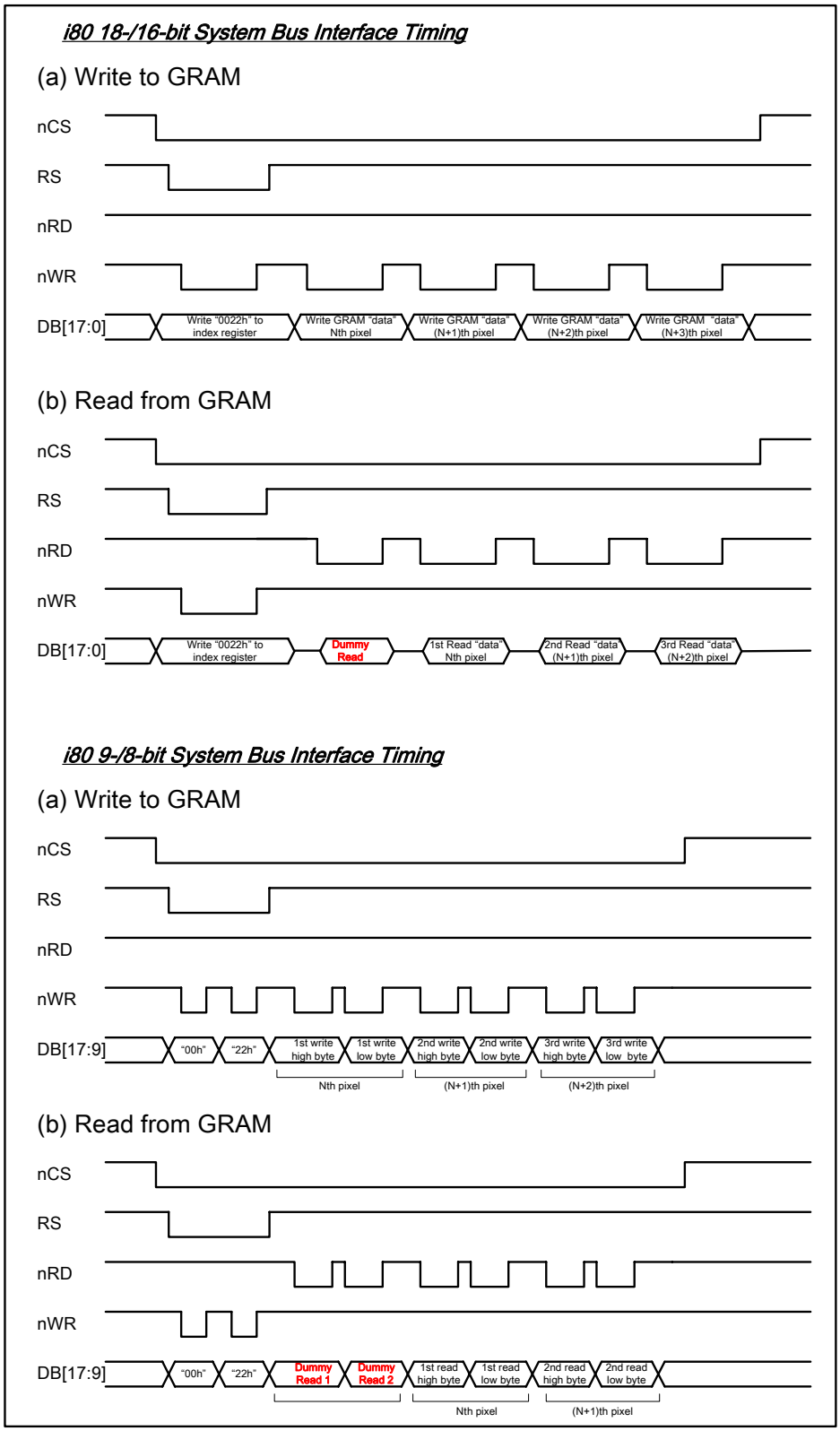


Figure42 GRAM Read/Write Timing of i80-System Interface

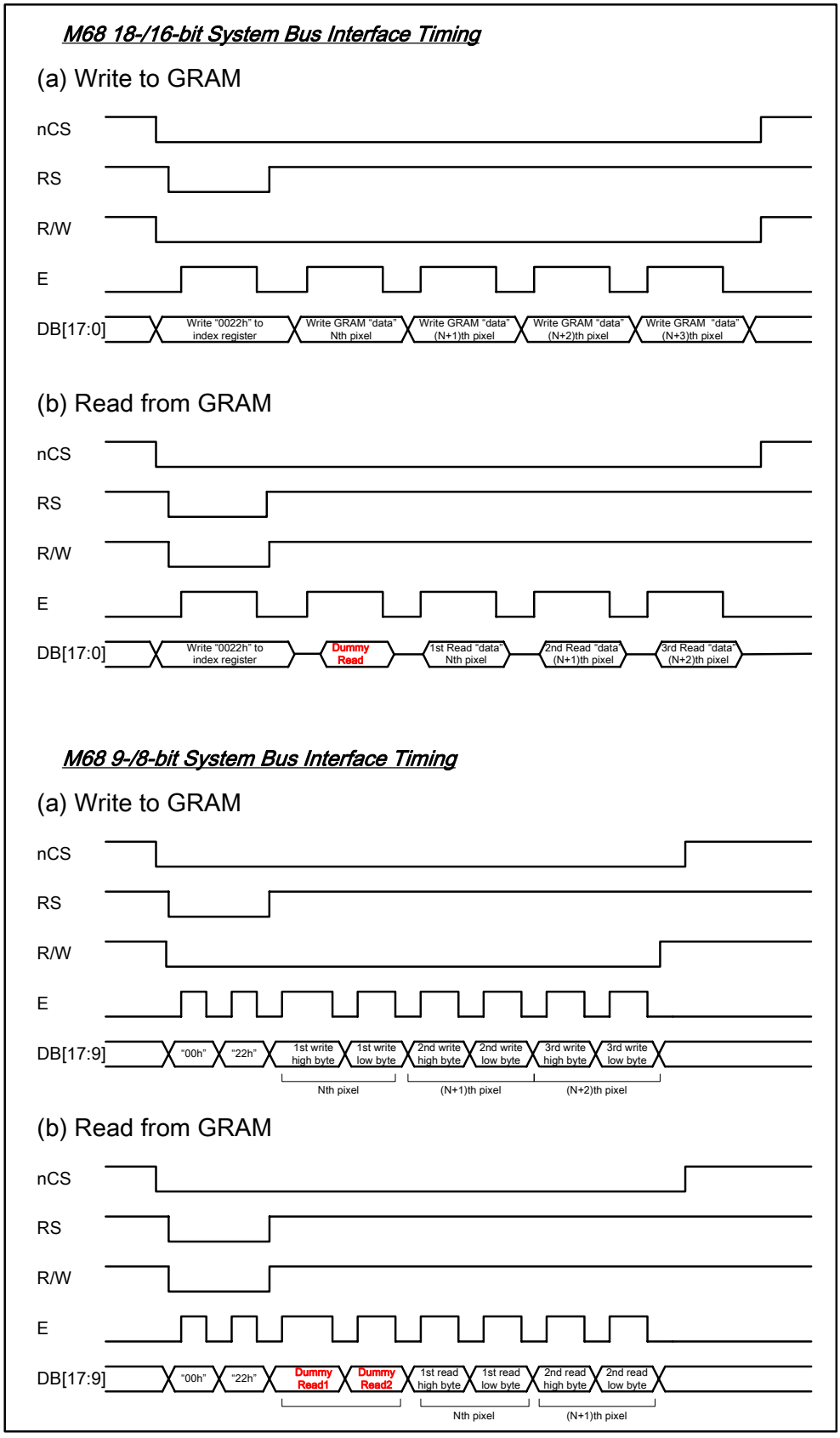
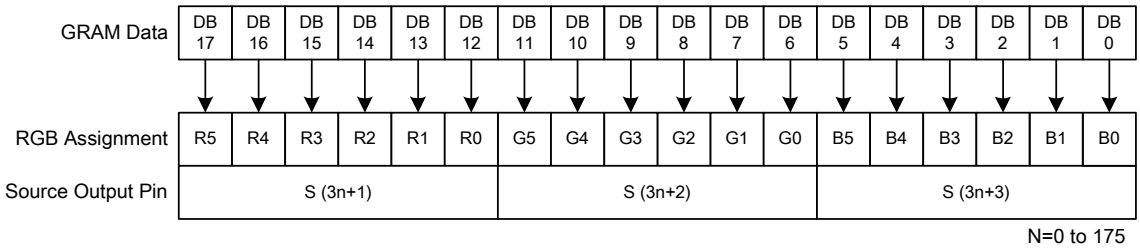


Figure 43 GRAM Read/Write Timing of M68-System Interface

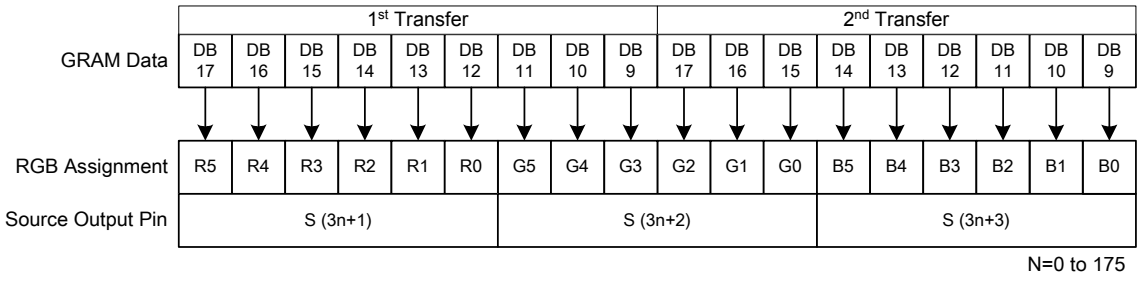
GRAM address map table of SS=0, BGR=0

SS=0, BGR=0		S1…S3	S4…S6	S7…S9	S10…S12	…	S517…S519	S520…S522	S523…S525	S526…S528
GS=0	GS=1	DB17…0	DB17…0	DB17…0	DB17…0	…	DB17…0	DB17…0	DB17…0	DB17…0
G1	G220	“0000h”	“0001h”	“0002h”	“0003h”	…	“00ACh”	“00ADh”	“00AEh”	“00AFh”
G2	G219	“0100h”	“0101h”	“0102h”	“0103h”	…	“01ACh”	“01ADh”	“01AEh”	“01AFh”
G3	G218	“0200h”	“0201h”	“0202h”	“0203h”	…	“02ACh”	“02ADh”	“02AEh”	“02AFh”
G4	G217	“0300h”	“0301h”	“0302h”	“0303h”	…	“03ACh”	“03ADh”	“03AEh”	“03AFh”
G5	G216	“0400h”	“0401h”	“0402h”	“0403h”	…	“04ACh”	“04ADh”	“04AEh”	“04AFh”
G6	G215	“0500h”	“0501h”	“0502h”	“0503h”	…	“05ACh”	“05ADh”	“05AEh”	“05AFh”
G7	G214	“0600h”	“0601h”	“0602h”	“0603h”	…	“06ACh”	“06ADh”	“06AEh”	“06AFh”
G8	G213	“0700h”	“0701h”	“0702h”	“0703h”	…	“07ACh”	“07ADh”	“07AEh”	“07AFh”
G9	G212	“0800h”	“0801h”	“0802h”	“0803h”	…	“08ACh”	“08ADh”	“08AEh”	“08AFh”
G10	G211	“0900h”	“0901h”	“0902h”	“0903h”	…	“09ACh”	“09ADh”	“09AEh”	“09AFh”
. . .	. . .	. . .	. . .	. . .	. . .	…	. . .	. . .	. . .	. . .
G211	G10	“D200h”	“D201h”	“D202h”	“D203h”	…	“D2ACh”	“D2ADh”	“D2AEh”	“D2AFh”
G212	G9	“D300h”	“D301h”	“D302h”	“D303h”	…	“D3ACh”	“D3ADh”	“D3AEh”	“D3AFh”
G213	G8	“D400h”	“D401h”	“D402h”	“D403h”	…	“D4ACh”	“D4ADh”	“D4AEh”	“D4AFh”
G214	G7	“D500h”	“D501h”	“D502h”	“D503h”	…	“D5ACh”	“D5ADh”	“D5AEh”	“D5AFh”
G215	G6	“D600h”	“D601h”	“D602h”	“D603h”	…	“D6ACh”	“D6ADh”	“D6AEh”	“D6AFh”
G216	G5	“D700h”	“D701h”	“D702h”	“D703h”	…	“D7ACh”	“D7ADh”	“D7AEh”	“D7AFh”
G217	G4	“D800h”	“D801h”	“D802h”	“D803h”	…	“D8ACh”	“D8ADh”	“D8AEh”	“D8AFh”
G218	G3	“D900h”	“D901h”	“D902h”	“D903h”	…	“D9ACh”	“D9ADh”	“D9AEh”	“D9AFh”
G219	G2	“DA00h”	“DA01h”	“DA02h”	“DA03h”	…	“DAACh”	“DAADh”	“DAAEh”	“DAAFh”
G220	G1	“DB00h”	“DB01h”	“DB02h”	“DB03h”	…	“DBACh”	“DBADh”	“DBAEh”	“DBAFh”

i80/M68 system 18-bit data bus interface



i80/M68 system 9-bit data bus interface

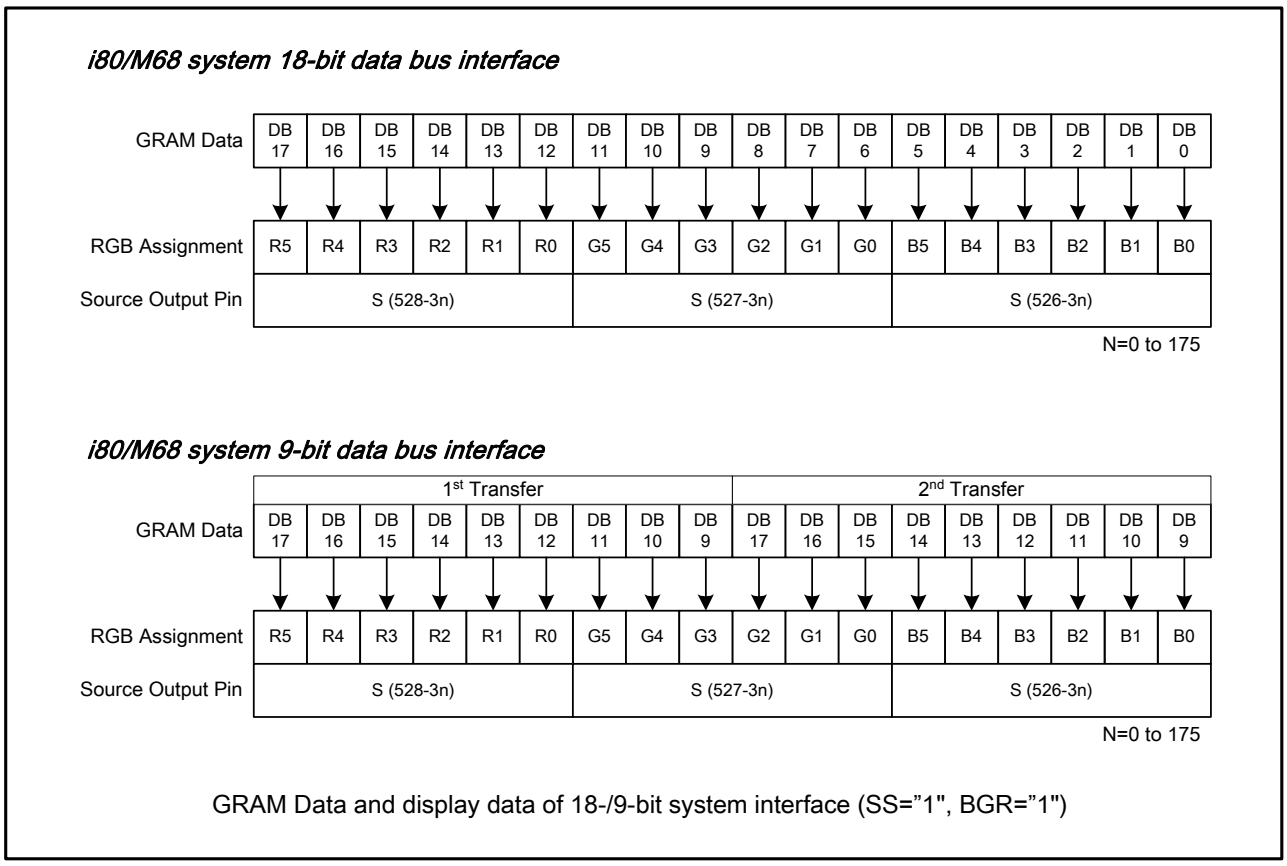


GRAM Data and display data of 18-/9-bit system interface (SS=”0", BGR=”0")

Figure44 i80-System Interface with 18-/9-bit Data Bus (SS=”0”, BGR=”0”)

GRAM address map table of SS=1, BGR=1

SS=1, BGR=1		S1…S3	S4…S6	S7…S9	S10…S12	…	S517…S519	S520…S522	S523…S525	S526…S528
GS=0	GS=1	DB17…0	DB17…0	DB17…0	DB17…0	…	DB17…0	DB17…0	DB17…0	DB17…0
G1	G220	“00AFh”	“00AEh”	“00ADh”	“00ACh”	…	“0003h”	“0002h”	“0001h”	“0000h”
G2	G219	“01AFh”	“01AEh”	“01ADh”	“01ACh”	…	“0103h”	“0102h”	“0101h”	“0100h”
G3	G218	“02AFh”	“02AEh”	“02ADh”	“02ACh”	…	“0203h”	“0202h”	“0201h”	“0200h”
G4	G217	“03AFh”	“03AEh”	“03ADh”	“03ACh”	…	“0303h”	“0302h”	“0301h”	“0300h”
G5	G216	“04AFh”	“04AEh”	“04ADh”	“04ACh”	…	“0403h”	“0402h”	“0401h”	“0400h”
G6	G215	“05AFh”	“05AEh”	“05ADh”	“05ACh”	…	“0503h”	“0502h”	“0501h”	“0500h”
G7	G214	“06AFh”	“06AEh”	“06ADh”	“06ACh”	…	“0603h”	“0602h”	“0601h”	“0600h”
G8	G213	“07AFh”	“07AEh”	“07ADh”	“07ACh”	…	“0703h”	“0702h”	“0701h”	“0700h”
G9	G212	“08AFh”	“08AEh”	“08ADh”	“08ACh”	…	“0803h”	“0802h”	“0801h”	“0800h”
G10	G211	“09AFh”	“09AEh”	“09ADh”	“09ACh”	…	“0903h”	“0902h”	“0901h”	“0900h”
. . .	. . .	. . .	. . .	. . .	. . .	…	. . .	. . .	. . .	. . .
G211	G10	“D2AFh”	“D2AEh”	“D2ADh”	“D2ACh”	…	“D203h”	“D202h”	“D201h”	“D200h”
G212	G9	“D3AFh”	“D3AEh”	“D3ADh”	“D3ACh”	…	“D303h”	“D302h”	“D301h”	“D300h”
G213	G8	“D4AFh”	“D4AEh”	“D4ADh”	“D4ACh”	…	“D403h”	“D402h”	“D401h”	“D400h”
G214	G7	“D5AFh”	“D5AEh”	“D5ADh”	“D5ACh”	…	“D503h”	“D502h”	“D501h”	“D500h”
G215	G6	“D6AFh”	“D6AEh”	“D6ADh”	“D6ACh”	…	“D603h”	“D602h”	“D601h”	“D600h”
G216	G5	“D7AFh”	“D7AEh”	“D7ADh”	“D7ACh”	…	“D703h”	“D702h”	“D701h”	“D700h”
G217	G4	“D8AFh”	“D8AEh”	“D8ADh”	“D8ACh”	…	“D803h”	“D802h”	“D801h”	“D800h”
G218	G3	“D9AFh”	“D9AEh”	“D9ADh”	“D9ACh”	…	“D903h”	“D902h”	“D901h”	“D900h”
G219	G2	“DAAFh”	“DAAEh”	“DAADh”	“DAACh”	…	“DA03h”	“DA02h”	“DA01h”	“DA00h”
G220	G1	“DBAFh”	“DBAEh”	“DBADh”	“DBACh”	…	“DB03h”	“DB02h”	“DB01h”	“DB00h”



GRAM Data and display data of 18-/9-bit system interface (SS=”1", BGR=”1")

Figure 45 i80-System Interface with 18-/9-bit Data Bus (SS=”1”, BGR=”1”)

11. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[7:0], end: VEA[7:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9221 to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the AD[15:0] bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

(Horizontal direction) 00H ≤ HSA[7:0] ≤ HEA[7:0] ≤ "AF"H

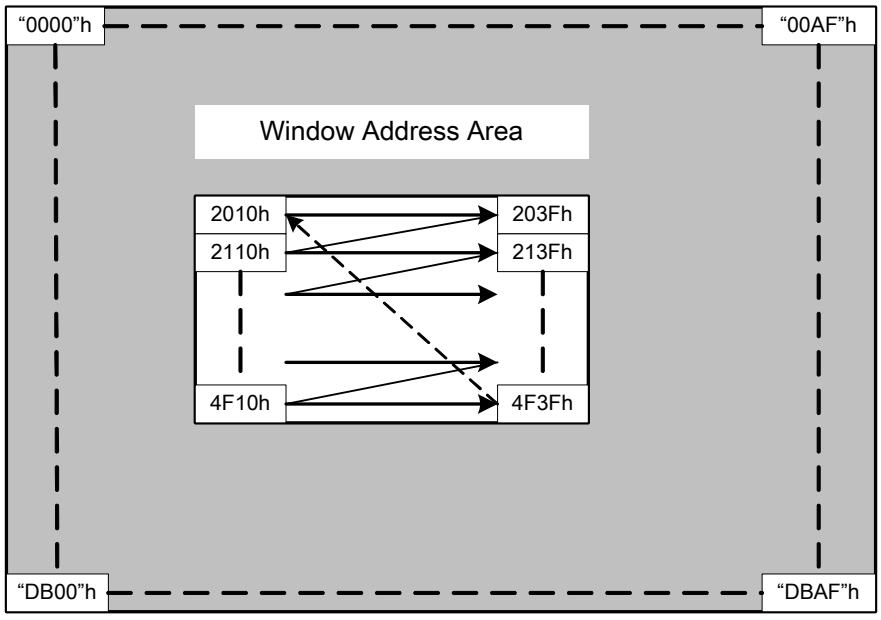
(Vertical direction) 00H ≤ VSA[7:0] ≤ VEA[7:0]≤ "DB"H

[RAM address, AD[15:0] (an address within a window address area)]]

(RAM address) HSA[7:0] ≤ AD[7:0] ≤ HEA[7:0]

VSA[7:0] ≤ AD[15:8] ≤ VEA[7:0]

GRAM Address Map



Window address setting area

HSA[7:0] = 10h, HSA[7:0] = 3Fh, I/D = 1 (increment)
VSA[7:0] = 20h, VSA[7:0] = 4Fh, AM = 0 (horizontal writing)

Figure 46 GRAM Access Window Map

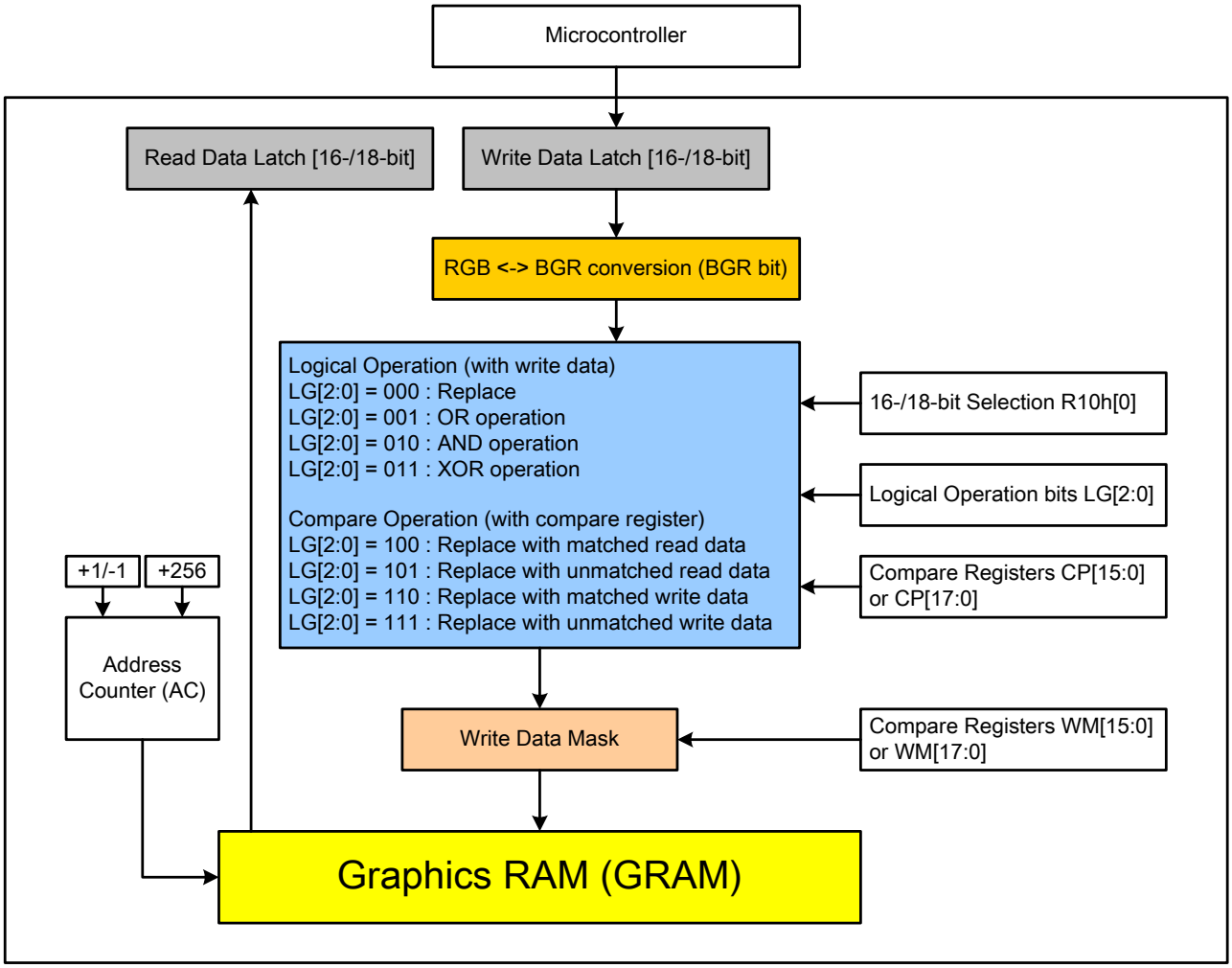
12. Graphics Operation Function

ILI9221 can significantly reduce the load on software in the microcomputer when processing graphics data with 18-bit architecture and graphics operation functions. The graphics operation functions of the ILI9221 include:

1. Write data mask function for writing only selected bits in the 18-bit write data over the RAM data.
2. A logical operation writes function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
3. Conditional rewrite function for writing data sent from the microcomputer only when a certain condition is met as a result of comparing the data and the bits in the compare register These graphics operation functions control the write operation of data sent from the microcomputer, according to the setting in the entry mode register or the write data mask register.

Graphics operation and related register (bits) setting

Operation Mode	Bit Setting			Operation and Usage
	I/D	AM	LG[2:0]	
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing



12.1. Write Data Mask Function

The write data mask function controls the operation of writing 18-bit data to the internal GRAM in units of bits. The ILI9221 expands 16-bit data sent from the microcomputer into 18-bit data internally. In case of 18-bit interface mode, data are not expanded.

The write data mask function enables the write operation of bits when the corresponding bits in the write data mask resister (WM[17:0]) are given “0” and inhibits the write operation of bits when the corresponding bits in the write data mask register (WM[17:0]) are given “1”. In the letter case, the GRAM data are not overwritten but retained. This function is useful when only data of one specific pixel are rewritten or a particular display color is selectively changed.

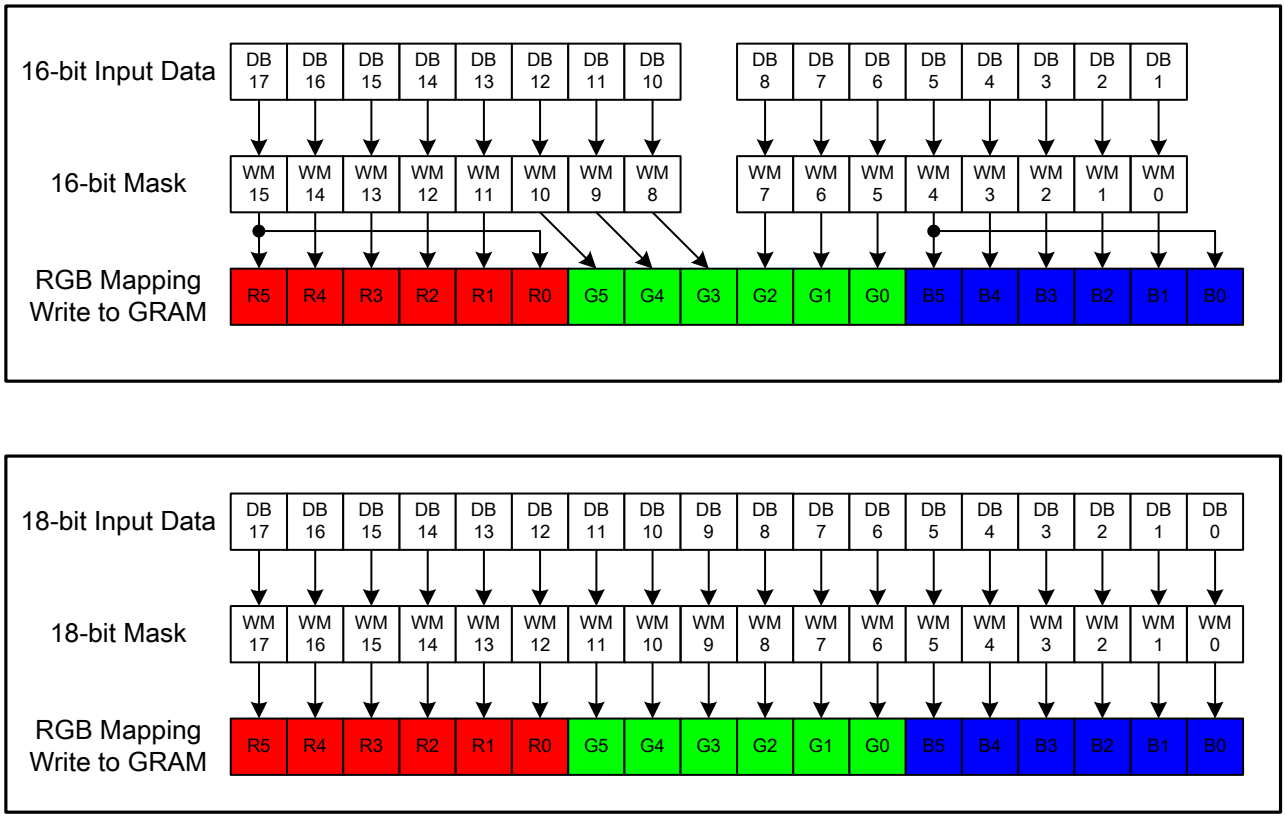


Figure 47 16-/18-bit Data Mask Function

12.2. Graphics Operation Processing

1. Write mode 1: AM = "0", LG[2:0] = "000"

This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM[17:0] or WM[15:0]) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = "1") or decrements by 1 (I/D = "0"), and automatically jumps to the counter edge one-raster row below after it has reached the left or right edge of the GRAM.

Operation Examples:

1) I/D="1", AM="0", LG[2:0]="000"
2) WM[17:0]= "00FFF"h
3) AC= "0000"h

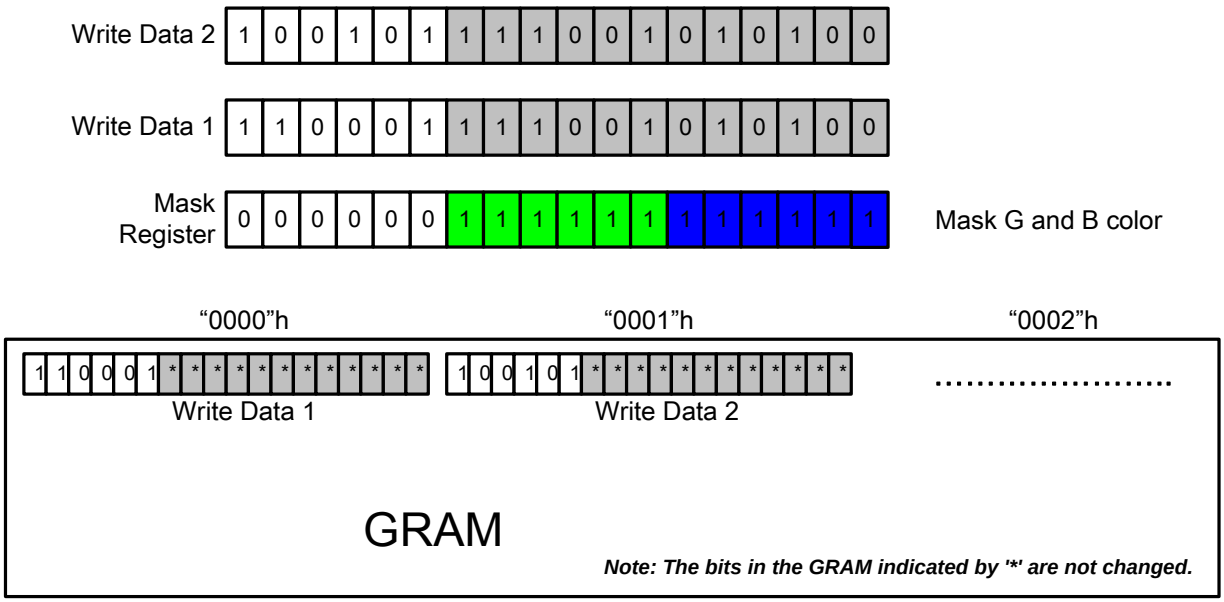


Figure 48 Write Operation of Write Mode 1

2. Write mode 2: AM = “1”, LG[2:0] = “000”

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM[17:0] or WM[15:0]) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 160, and automatically jumps to the upper-right edge (I/D = “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I/D=”1", AM=”1", LG[2:0]=”000"
2) WM[17:0]= “00FFF”h
3) AC= “0000”h

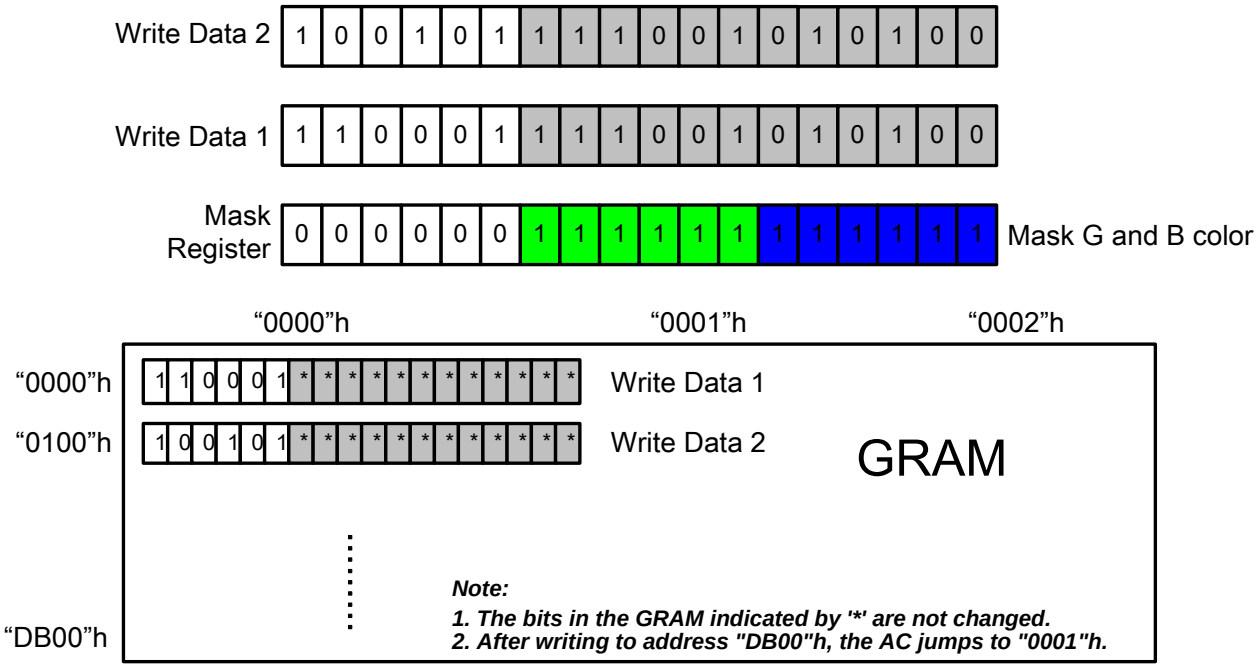


Figure 49 Write Operation of Write Mode 2

3. Write mode 3: AM = “0”, LG[2:0] = “110”/”111”

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP[17:0] or CP[15:0]). When the result of the comparison in a word unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM[17:0] or WM[15:0]) is also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = “1”) or decrements by 1 (I/D = “0”), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

Operation Examples:

1) I/D=”1", AM=”0", LG[2:0]=”110" (matched write)
2) CP[17:0]= “12860”h
3) WM[17:0]= “00000”h
4) AC= “0000”h

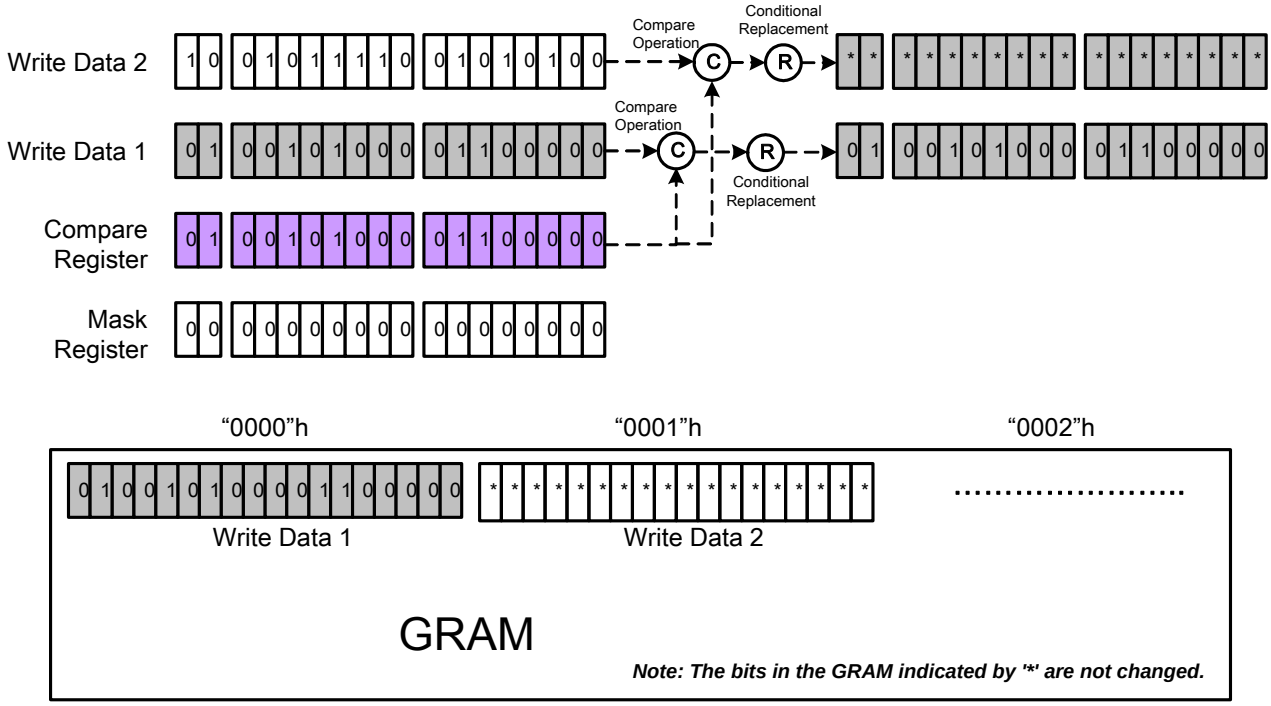


Figure 50 Write Operation of Write Mode 3

4. Write mode 4: AM = “1”, LG[2:0] = “110”/ “111”

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP[17:0] or CP[15:0]) to write the data. When the result by the comparison in a word unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM[17:0] or WM[15:0]) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D= “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I/D=”1", AM=”1", LG[2:0]=”111" (unmatched write)
2) CP[17:0]= “12860”h
3) WM[17:0]= “00000”h
4) AC= “0000”h

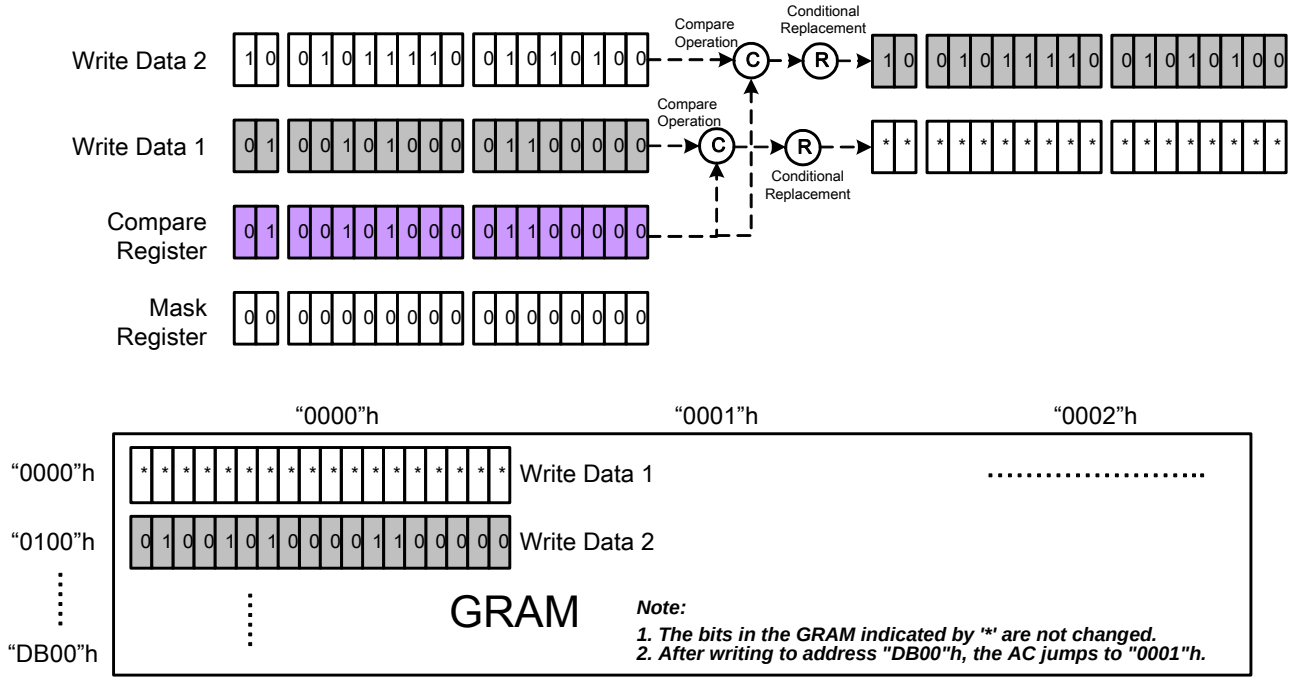


Figure 51 Write Operation of Write Mode 4

5. Read/Write mode 1: AM = "0", LG[2:0] = "001"/ "010" / "011"

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (i80-system: nRD low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the readdata latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM[17:0] or WM[15:0]) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = "1") or decrements by 1 (I/D = "0"), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

Operation Examples:

1) I/D="1", AM="0", LG[2:0]="001" (OR)
2) WM[17:1]= "0000"h
3) AC= "0000"h

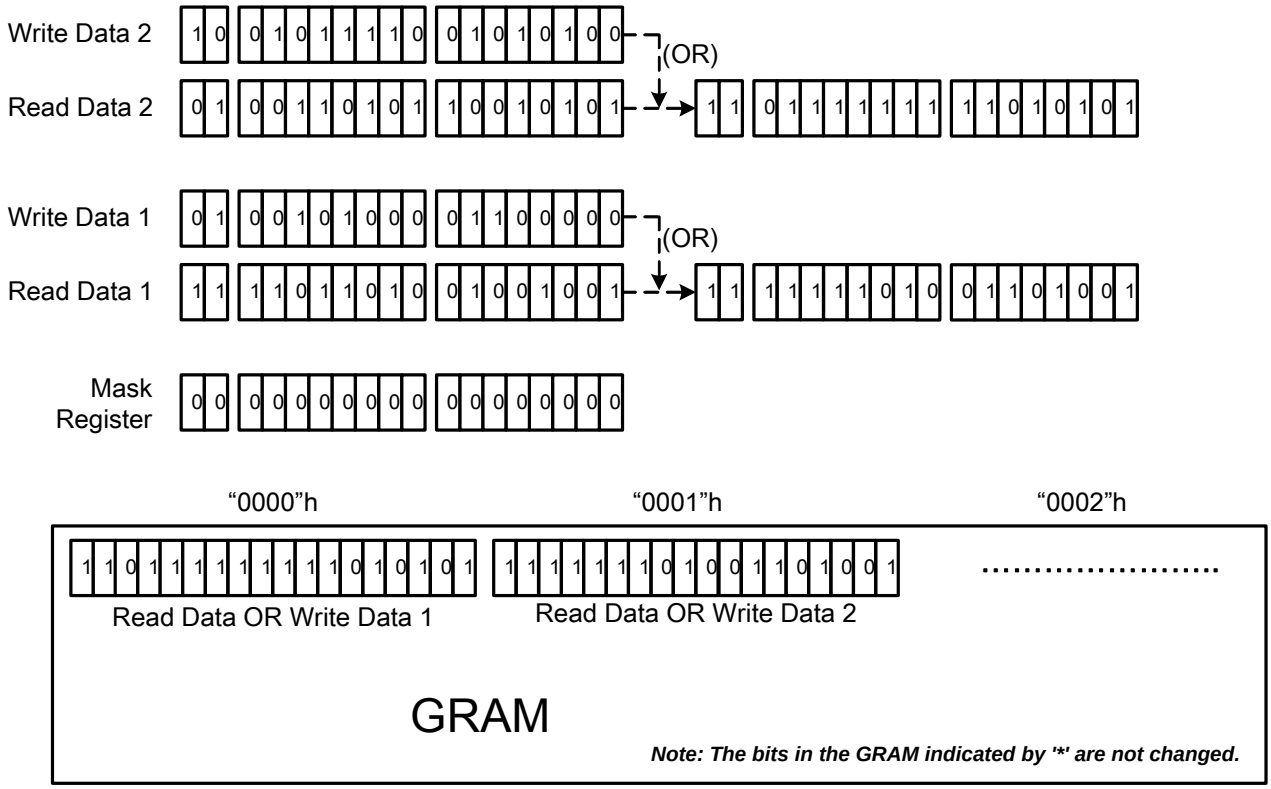


Figure 52 Write Operation of Read/Write Mode 1

6. Read/Write mode 2: AM = “1”, LG[2:0] = “001”/ “010” / “011”

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (i80-system: nRD low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write data mask function (WM[17:0] or WM[15:0]) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I/D=”1", AM=”1", LG[2:0]=”001" (OR)
2) WM[17:1]= “3FFE0”h
3) AC= “0000”h

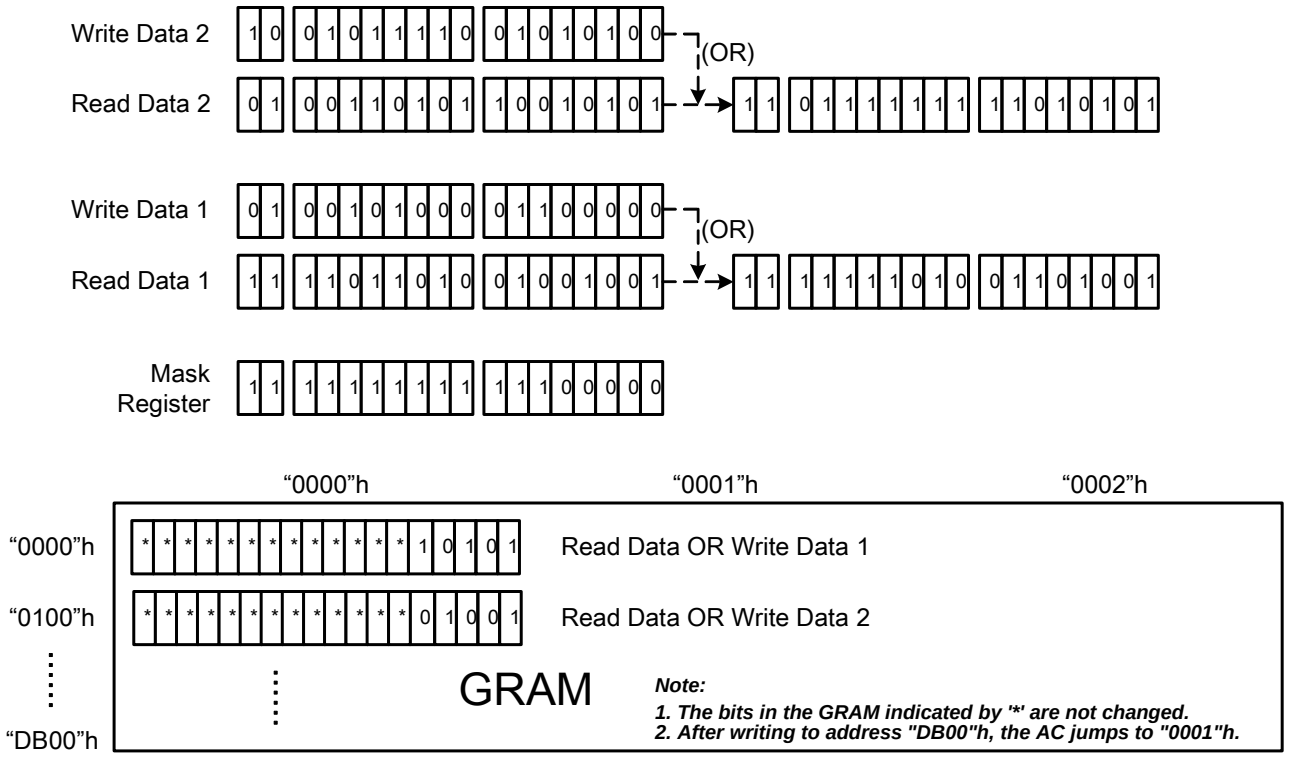


Figure 53 Write Operation of Read/Write Mode 2

7. Read/Write mode 3: AM = 0, LG[2:0] = “100”/”101”

This mode is used when the data is horizontally written by comparing the original data and the set value of the latched data in the RDR register. It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (i80-system: nRD low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the readdata latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM[17:0] or WM[15:0]) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = “1”) or decrements by 1 (I/D = “0”), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

Operation Examples:

1) I/D=”1", AM=”0", LG[2:0]=”100" (matched write)
2) CP[17:0]= “12860”h
3) WM[17:0]= “00000”h
4) AC= “0000”h

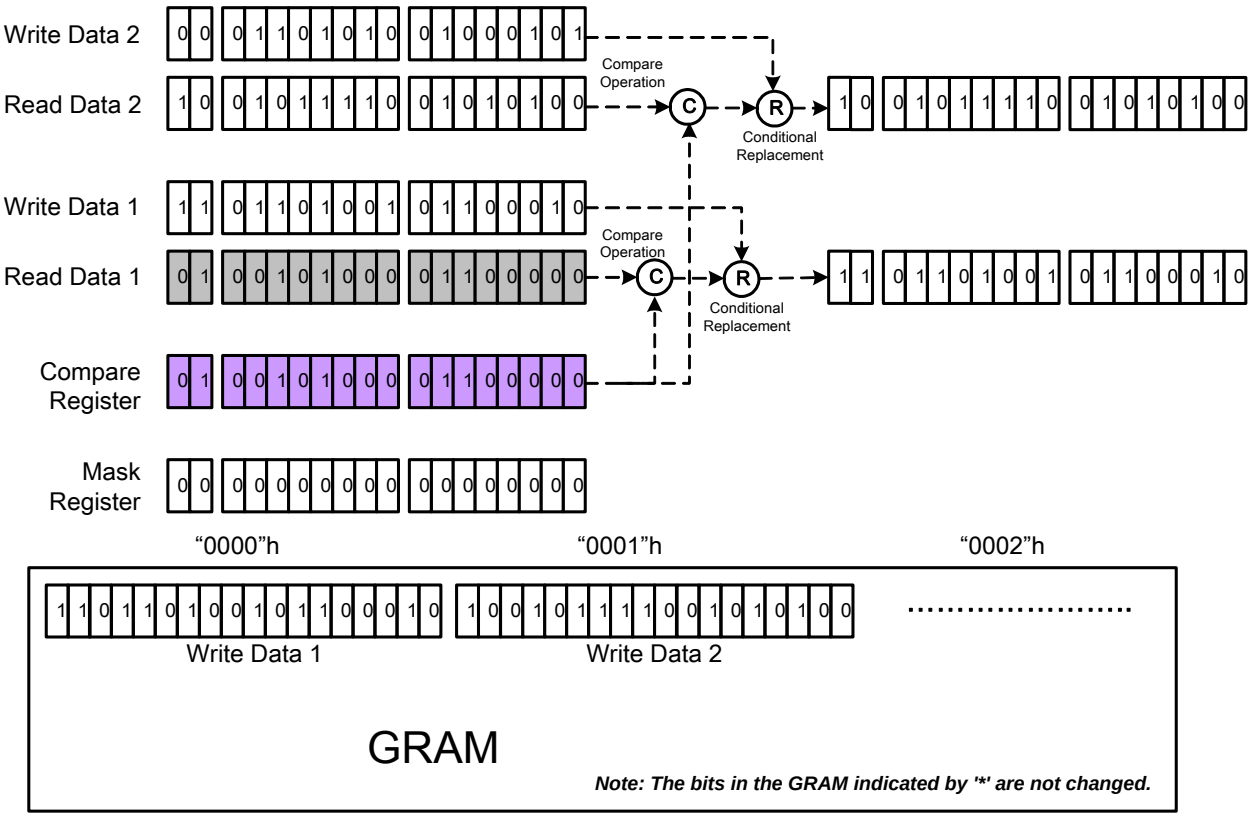


Figure 54 Write Operation of Read/Write Mode 3

8. Read/Write mode 4: AM = “1”, LG[2:0] = “100” / “101”

This mode is used when the data is vertically written by comparing the original data and the set value of the latched data in the RDR register. It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the compare operation satisfies the condition. This mode reads the data during the same access-pulse width (i80-system: nRD low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write data mask function (WM[17:0] or WM[15:0]) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I/D=”1", AM=”1", LG[2:0]=”101" (unmatched write)
2) CP[17:0]= “12860”h
3) WM[17:0]= “00000”h
4) AC= “0000”h

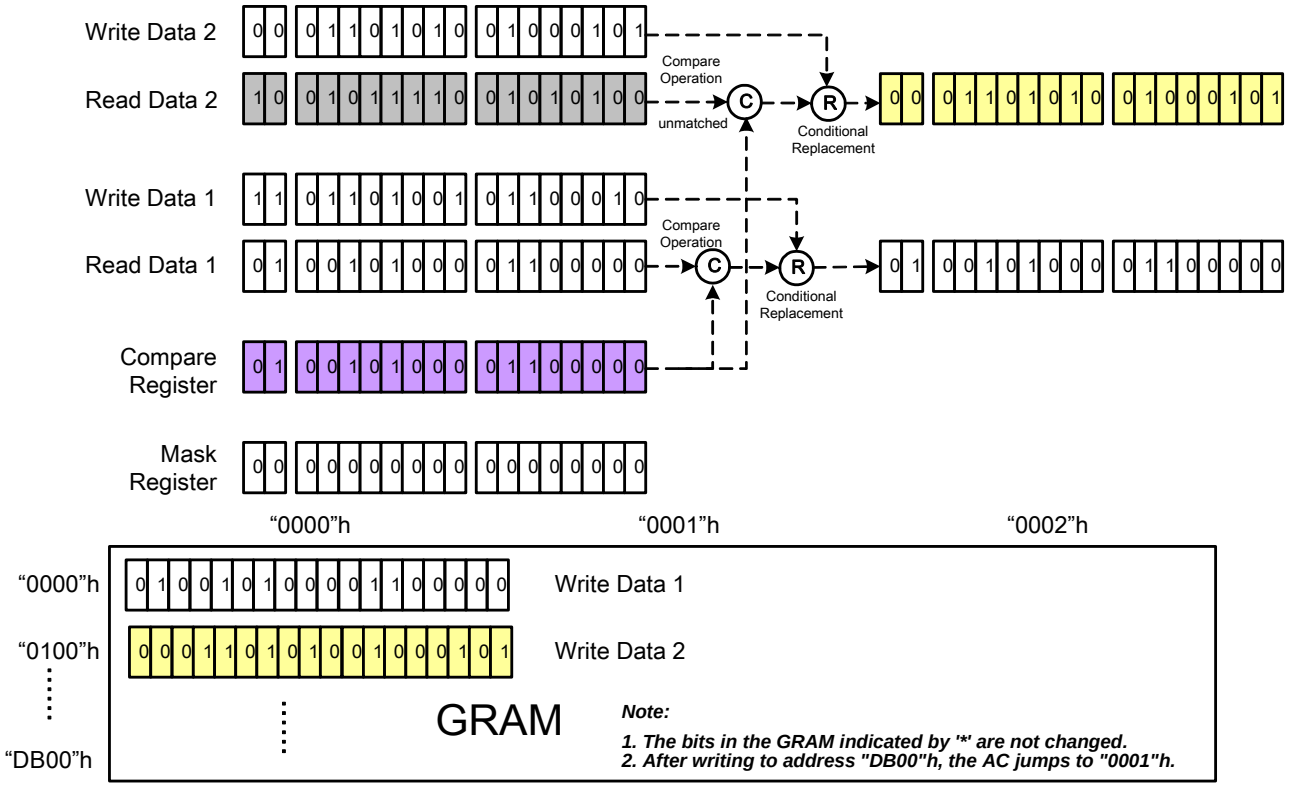


Figure 55 Write Operation of Read/Write Mode 4

13. Gamma Correction

ILI9221 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9221 available with liquid crystal panels of various characteristics.

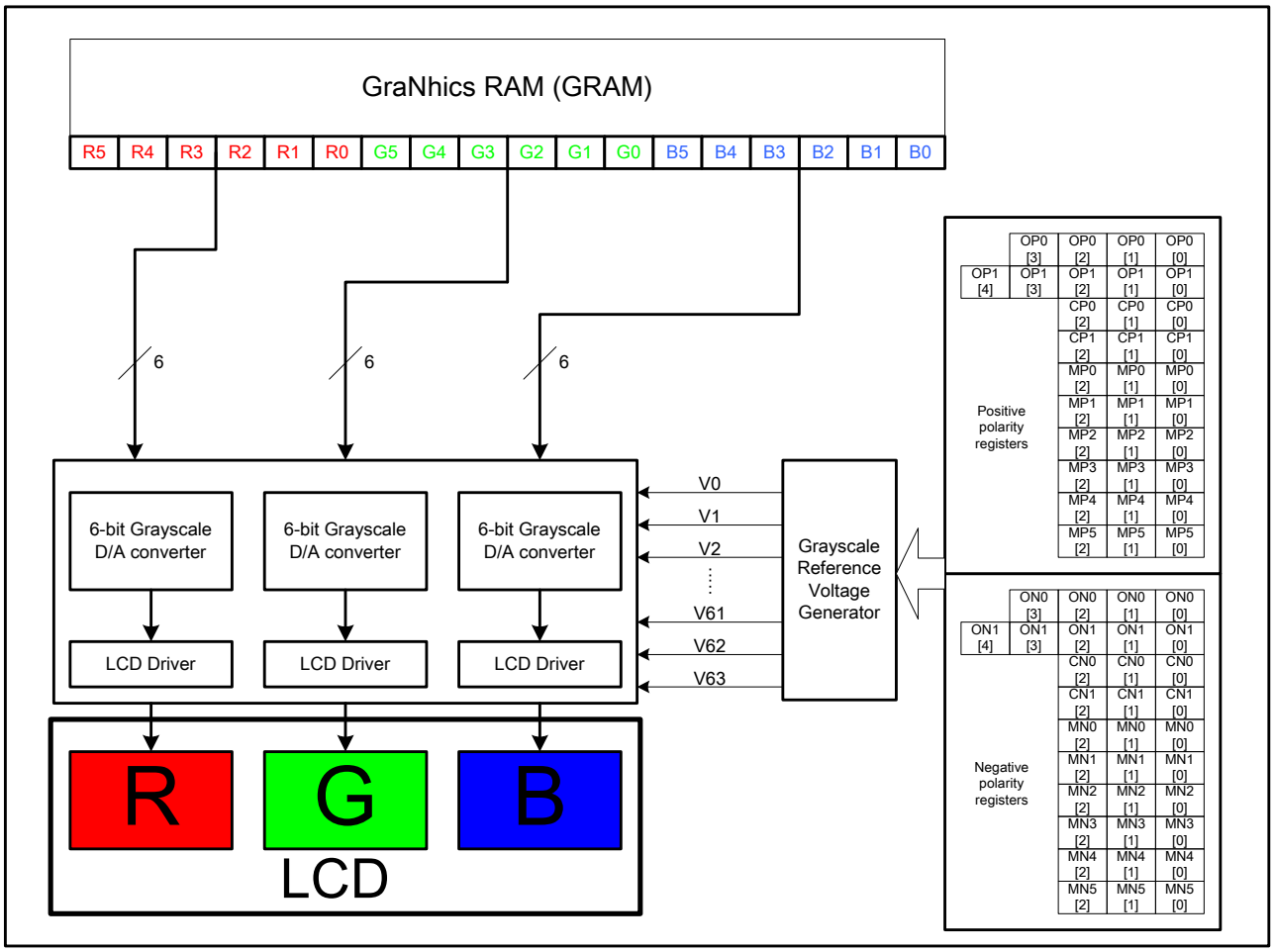


Figure 56 Grayscale Mapping

Grayscale Voltage Generator Configuration

The following figure illustrates the grayscale voltage generator function of the ILI9221. To generate 64 grayscale voltages (V0~V63), ILI9221 first generates eight reference grayscale voltages (VgP/N0, VgP/N1, VgP/N8, VgP/N20, VgP/N43, VgP/N55, VgP/N62, VgP/N63) and the grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein. Total 64 grayscale levels are generated from the γ-correction function and used for the LCD source driver.

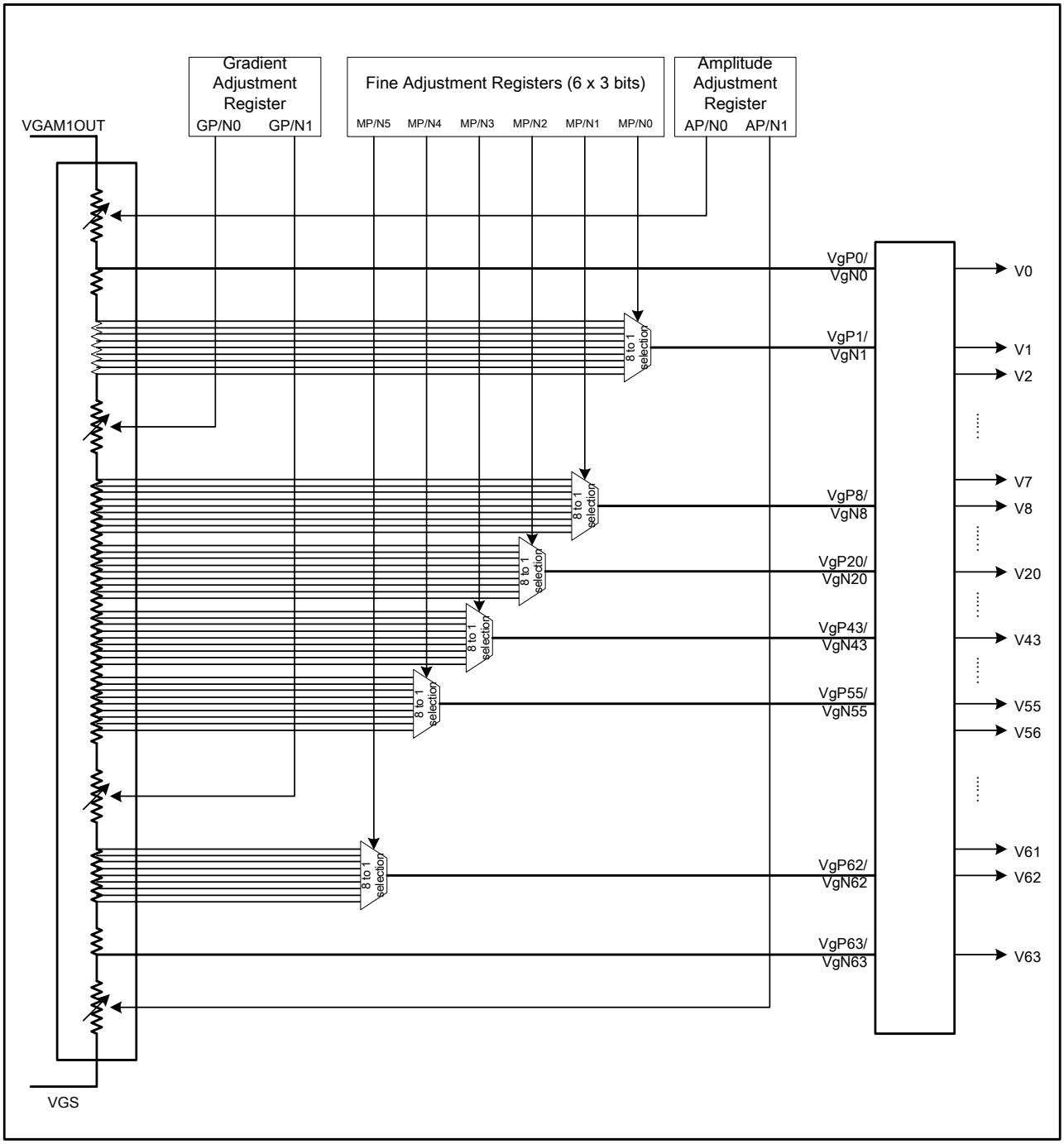


Figure 57 Grayscale Voltage Generation

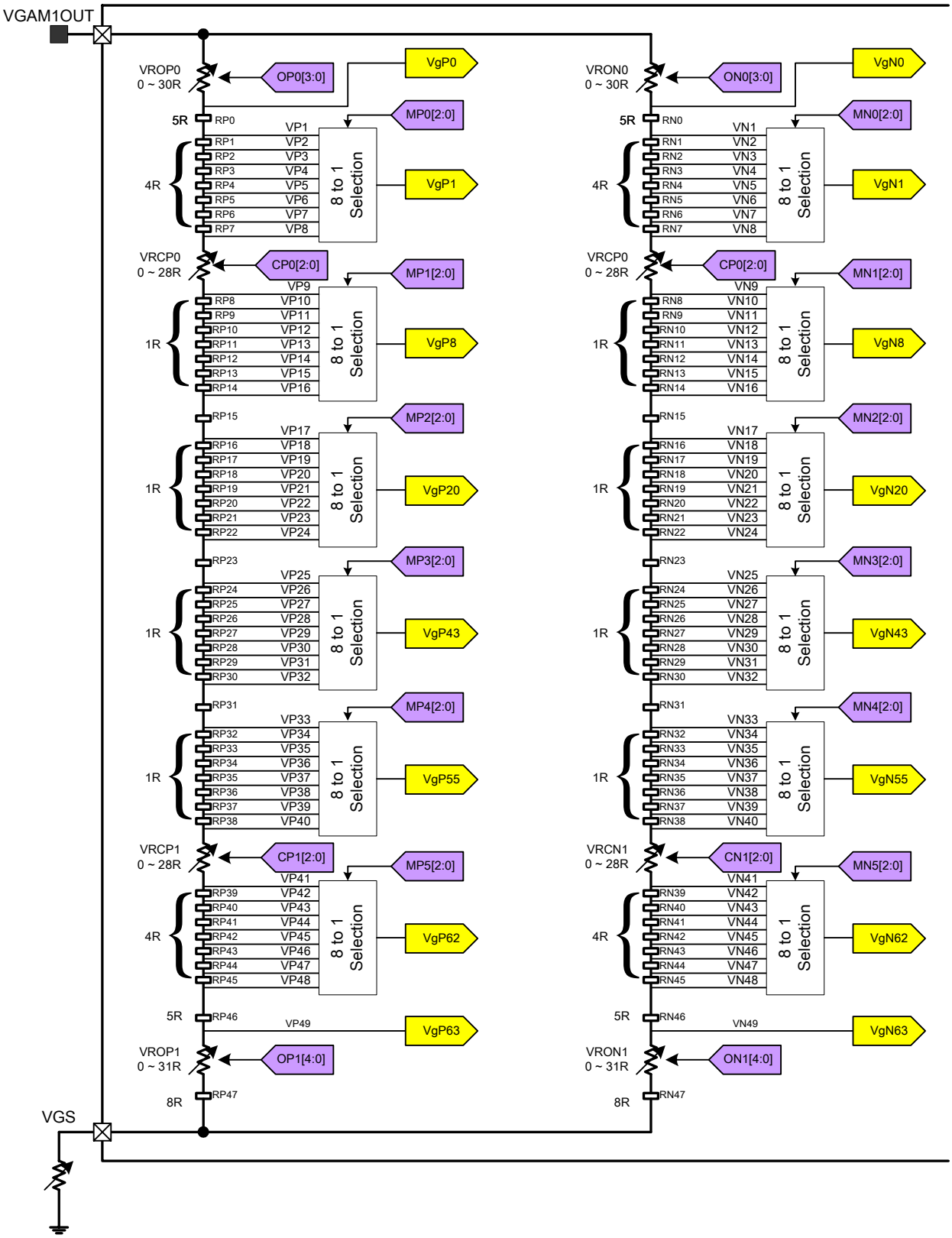


Figure 58 Grayscale Voltage Adjustment

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers CP0[2:0]/CN0[2:0], CP1[2:0]/CN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, OP0[3:0]/ON0[3:0], OP1[4:0]/ON1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

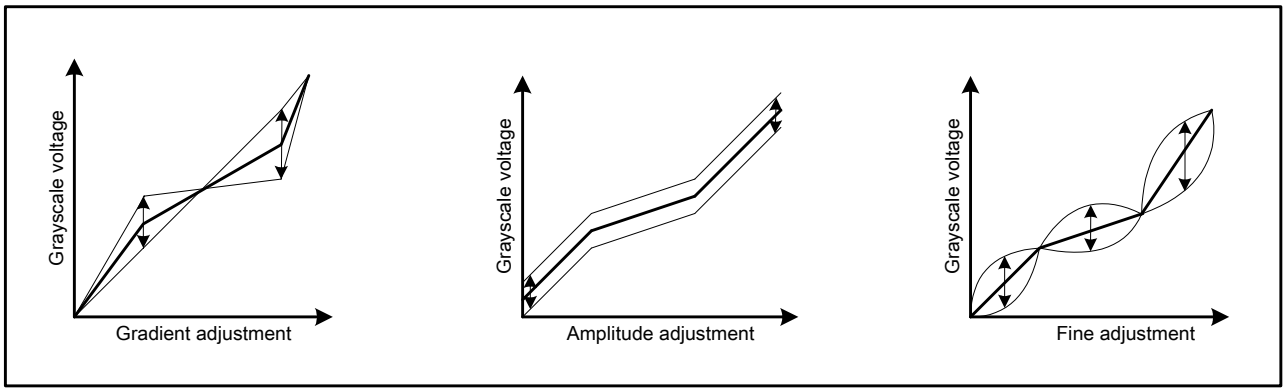


Figure 59 Gamma Curve Adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	CP0 [2:0]	CN0 [2:0]	Variable resistor VRCP0, VRCN0
	CP1 [2:0]	CN1 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	OP0 [3:0]	ON0 [3:0]	Variable resistor VROP0, VRON0
	OP1 [4:0]	ON1 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	MP0 [2:0]	MN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	MP1 [2:0]	MN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	MP2 [2:0]	MN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	MP3 [2:0]	MN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	MP4 [2:0]	MN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	MP5 [2:0]	MN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the **γ-**correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable resistors

ILI9221 uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment		Amplitude adjustment (1)		Amplitude adjustment (2)	
CP(N)0/1[2:0] Register	VRCP(N)0 Resistance	OP(N)0[3:0] Register	VROP(N)0 Resistance	OP(N)1[4:0] Register	VROP(N)1 Resistance
000	0R	0000	0R	00000	0R
001	4R	0001	2R	00001	1R
010	8R	0010	4R	00010	2R
011	12R	:	:	:	:
100	16R	:	:	:	:
101	20R	1101	26R	11101	29R
110	24R	1111	28R	11110	30R
111	28R	1111	30R	11111	31R

8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	Selected Voltage					
MP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formulae.

Formulae for calculating voltage (Positive polarity)

Reference Voltage	Fine Adjustment Value	Formula	Vout
VgP0	———	VGAM1OUT–VD*VROP0/sumRP	VP0
VgP1	MP0[2:0]=000	VGAM1OUT–VD*(VROP0+5R)/sumRP	VP1
	MP0[2:0]=001	VGAM1OUT–VD*(VROP0+9R)/sumRP	VP2
	MP0[2:0]=010	VGAM1OUT–VD*(VROP0+13R)/sumRP	VP3
	MP0[2:0]=011	VGAM1OUT–VD*(VROP0+17R)/sumRP	VP4
	MP0[2:0]=100	VGAM1OUT–VD*(VROP0+21R)/sumRP	VP5
	MP0[2:0]=101	VGAM1OUT–VD*(VROP0+25R)/sumRP	VP6
	MP0[2:0]=110	VGAM1OUT–VD*(VROP0+29R)/sumRP	VP7
	MP0[2:0]=111	VGAM1OUT–VD*(VROP0+33R)/sumRP	VP8
VgP8	MP1[2:0]=000	VGAM1OUT–VD*(VROP0+33R+VRCP0)/sumRP	VP9
	MP1[2:0]=001	VGAM1OUT–VD*(VROP0+34R+VRCP0)/sumRP	VP10
	MP1[2:0]=010	VGAM1OUT–VD*(VROP0+35R+VRCP0)/sumRP	VP11
	MP1[2:0]=011	VGAM1OUT–VD*(VROP0+36R+VRCP0)/sumRP	VP12
	MP1[2:0]=100	VGAM1OUT–VD*(VROP0+37R+VRCP0)/sumRP	VP13
	MP1[2:0]=101	VGAM1OUT–VD*(VROP0+38R+VRCP0)/sumRP	VP14
	MP1[2:0]=110	VGAM1OUT–VD*(VROP0+39R+VRCP0)/sumRP	VP15
	MP1[2:0]=111	VGAM1OUT–VD*(VROP0+40R+VRCP0)/sumRP	VP16
VgP20	MP2[2:0]=000	VGAM1OUT–VD*(VROP0+45R+VRCP0)/sumRP	VP17
	MP2[2:0]=001	VGAM1OUT–VD*(VROP0+46R+VRCP0)/sumRP	VP18
	MP2[2:0]=010	VGAM1OUT–VD*(VROP0+47R+VRCP0)/sumRP	VP19
	MP2[2:0]=011	VGAM1OUT–VD*(VROP0+48R+VRCP0)/sumRP	VP20
	MP2[2:0]=100	VGAM1OUT–VD*(VROP0+49R+VRCP0)/sumRP	VP21
	MP2[2:0]=101	VGAM1OUT–VD*(VROP0+50R+VRCP0)/sumRP	VP22
	MP2[2:0]=110	VGAM1OUT–VD*(VROP0+51R+VRCP0)/sumRP	VP23
	MP2[2:0]=111	VGAM1OUT–VD*(VROP0+52R+VRCP0)/sumRP	VP24
VgP43	MP3[2:0]=000	VGAM1OUT–VD*(VROP0+68R+VRCP0)/sumRP	VP25
	MP3[2:0]=001	VGAM1OUT–VD*(VROP0+69R+VRCP0)/sumRP	VP26
	MP3[2:0]=010	VGAM1OUT–VD*(VROP0+70R+VRCP0)/sumRP	VP27
	MP3[2:0]=011	VGAM1OUT–VD*(VROP0+71R+VRCP0)/sumRP	VP28
	MP3[2:0]=100	VGAM1OUT–VD*(VROP0+72R+VRCP0)/sumRP	VP29
	MP3[2:0]=101	VGAM1OUT–VD*(VROP0+73R+VRCP0)/sumRP	VP30
	MP3[2:0]=110	VGAM1OUT–VD*(VROP0+74R+VRCP0)/sumRP	VP31
	MP3[2:0]=111	VGAM1OUT–VD*(VROP0+75R+VRCP0)/sumRP	VP32
VgP55	MP4[2:0]=000	VGAM1OUT–VD*(VROP0+80R+VRCP0)/sumRP	VP33
	MP4[2:0]=001	VGAM1OUT–VD*(VROP0+81R+VRCP0)/sumRP	VP34
	MP4[2:0]=010	VGAM1OUT–VD*(VROP0+82R+VRCP0)/sumRP	VP35
	MP4[2:0]=011	VGAM1OUT–VD*(VROP0+83R+VRCP0)/sumRP	VP36
	MP4[2:0]=100	VGAM1OUT–VD*(VROP0+84R+VRCP0)/sumRP	VP37
	MP4[2:0]=101	VGAM1OUT–VD*(VROP0+85R+VRCP0)/sumRP	VP38
	MP4[2:0]=110	VGAM1OUT–VD*(VROP0+86R+VRCP0)/sumRP	VP39
	MP4[2:0]=111	VGAM1OUT–VD*(VROP0+87R+VRCP0)/sumRP	VP40
VgP62	MP5[2:0]=000	VGAM1OUT–VD*(VROP0+87R+VRCP0+VRCP1)/sumRP	VP41
	MP5[2:0]=001	VGAM1OUT–VD*(VROP0+91R+VRCP0+VRCP1)/sumRP	VP42
	MP5[2:0]=010	VGAM1OUT–VD*(VROP0+95R+VRCP0+VRCP1)/sumRP	VP43
	MP5[2:0]=011	VGAM1OUT–VD*(VROP0+99R+VRCP0+VRCP1)/sumRP	VP44
	MP5[2:0]=100	VGAM1OUT–VD*(VROP0+103R+VRCP0+VRCP1)/sumRP	VP45
	MP5[2:0]=101	VGAM1OUT–VD*(VROP0+107R+VRCP0+VRCP1)/sumRP	VP46
	MP5[2:0]=110	VGAM1OUT–VD*(VROP0+111R+VRCP0+VRCP1)/sumRP	VP47
	MP5[2:0]=111	VGAM1OUT–VD*(VROP0+115R+VRCP0+VRCP1)/sumRP	VP48
VgP63	———	VGAM1OUT–VD*(VROP0+120R+VRCP0+VRCP1)/sumRP	VP49

Sum of positive resistor sumRP = 128R + VROP0 + VROP1 + VRCP0 + VRCP1

Sum of negative resistor sumRN = 128R + VRON0 + VRON1 + VRCN0 + VRCN1

Voltage difference VD = (VGAM1OUT – VGS)

Formulae for calculating voltage (Positive polarity)

Grayscale Voltage	Formula
V0	VgP0
V1	VgP1
V2	V3+(V1–V3)*(8/24)
V3	V8+(V1–V8)*(450/800)
V4	V8+(V3–V8)*(16/24)
V5	V8+(V3–V8)*(12/24)
V6	V8+(V3–V8)*(8/24)
V7	V8+(V3–V8)*(4/24)
V8	VgP8
V9	V20+(V8–V20)*(22/24)
V10	V20+(V8–V20)*(20/24)
V11	V20+(V8–V20)*(18/24)
V12	V20+(V8–V20)*(16/24)
V13	V20+(V8–V20)*(14/24)
V14	V20+(V8–V20)*(12/24)
V15	V20+(V8–V20)*(10/24)
V16	V20+(V8–V20)*(8/24)
V17	V20+(V8–V20)*(6/24)
V18	V20+(V8–V20)*(4/24)
V19	V20+(V8–V20)*(2/24)
V20	VgP20
V21	V43+(V20–V43)*(22/23)
V22	V43+(V20–V43)*(21/23)
V23	V43+(V20–V43)*(20/23)
V24	V43+(V20–V43)*(19/23)
V25	V43+(V20–V43)*(18/23)
V26	V43+(V20–V43)*(17/23)
V27	V43+(V20–V43)*(16/23)
V28	V43+(V20–V43)*(15/23)
V29	V43+(V20–V43)*(14/23)
V30	V43+(V20–V43)*(13/23)
V31	V43+(V20–V43)*(12/23)

Grayscale Voltage	Formula
V32	V43+(V20–V43)*(11/23)
V33	V43+(V20–V43)*(10/23)
V34	V43+(V20–V43)*(9/23)
V35	V43+(V20–V43)*(8/23)
V36	V43+(V20–V43)*(7/23)
V37	V43+(V20–V43)*(6/23)
V38	V43+(V20–V43)*(5/23)
V39	V43+(V20–V43)*(4/23)
V40	V43+(V20–V43)*(3/23)
V41	V43+(V20–V43)*(2/23)
V42	V43+(V20–V43)*(1/23)
V43	VgP43
V44	V55+(V43–V55)*(22/24)
V45	V55+(V43–V55)*(20/24)
V46	V55+(V43–V55)*(18/24)
V47	V55+(V43–V55)*(16/24)
V48	V55+(V43–V55)*(14/24)
V49	V55+(V43–V55)*(12/24)
V50	V55+(V43–V55)*(10/24)
V51	V55+(V43–V55)*(8/24)
V52	V55+(V43–V55)*(6/24)
V53	V55+(V43–V55)*(4/24)
V54	V55+(V43–V55)*(2/24)
V55	VgP55
V56	V60+(V55–V60)*(20/24)
V57	V60+(V55–V60)*(16/24)
V58	V60+(V55–V60)*(12/24)
V59	V60+(V55–V60)*(8/24)
V60	V62+(V55–V62)*(350/800)
V61	V62+(V60–V62)*(16/24)
V62	VgP62
V63	VgP63

Note: The following condition shall be always retained.

DDVDH – V0 > 0.5V

DDVDH – V8 > 1.1V

V55 – AGND > 1.1V

Formulae for calculating voltage (Negative polarity)

Reference Voltage	Fine Adjustment Value	Formula	Vout
VgN0	———	VGAM1OUT–VD*VRON0/sumRN	VN0
VgN1	MN0[2:0]=000	VGAM1OUT–VD*(VRON0+5R)/sumRN	VN1
	MN0[2:0]=001	VGAM1OUT–VD*(VRON0+9R)/sumRN	VN2
	MN0[2:0]=010	VGAM1OUT–VD*(VRON0+13R)/sumRN	VN3
	MN0[2:0]=011	VGAM1OUT–VD*(VRON0+17R)/sumRN	VN4
	MN0[2:0]=100	VGAM1OUT–VD*(VRON0+21R)/sumRN	VN5
	MN0[2:0]=101	VGAM1OUT–VD*(VRON0+25R)/sumRN	VN6
	MN0[2:0]=110	VGAM1OUT–VD*(VRON0+29R)/sumRN	VN7
	MN0[2:0]=111	VGAM1OUT–VD*(VRON0+33R)/sumRN	VN8
VgN8	MN1[2:0]=000	VGAM1OUT–VD*(VRON0+33R+VRCN0)/sumRN	VN9
	MN1[2:0]=001	VGAM1OUT–VD*(VRON0+34R+VRCN0)/sumRN	VN10
	MN1[2:0]=010	VGAM1OUT–VD*(VRON0+35R+VRCN0)/sumRN	VN11
	MN1[2:0]=011	VGAM1OUT–VD*(VRON0+36R+VRCN0)/sumRN	VN12
	MN1[2:0]=100	VGAM1OUT–VD*(VRON0+37R+VRCN0)/sumRN	VN13
	MN1[2:0]=101	VGAM1OUT–VD*(VRON0+38R+VRCN0)/sumRN	VN14
	MN1[2:0]=110	VGAM1OUT–VD*(VRON0+39R+VRCN0)/sumRN	VN15
	MN1[2:0]=111	VGAM1OUT–VD*(VRON0+40R+VRCN0)/sumRN	VN16
VgN20	MN2[2:0]=000	VGAM1OUT–VD*(VRON0+45R+VRCN0)/sumRN	VN17
	MN2[2:0]=001	VGAM1OUT–VD*(VRON0+46R+VRCN0)/sumRN	VN18
	MN2[2:0]=010	VGAM1OUT–VD*(VRON0+47R+VRCN0)/sumRN	VN19
	MN2[2:0]=011	VGAM1OUT–VD*(VRON0+48R+VRCN0)/sumRN	VN20
	MN2[2:0]=100	VGAM1OUT–VD*(VRON0+49R+VRCN0)/sumRN	VN21
	MN2[2:0]=101	VGAM1OUT–VD*(VRON0+50R+VRCN0)/sumRN	VN22
	MN2[2:0]=110	VGAM1OUT–VD*(VRON0+51R+VRCN0)/sumRN	VN23
	MN2[2:0]=111	VGAM1OUT–VD*(VRON0+52R+VRCN0)/sumRN	VN24
VgN43	MN3[2:0]=000	VGAM1OUT–VD*(VRON0+68R+VRCN0)/sumRN	VN25
	MN3[2:0]=001	VGAM1OUT–VD*(VRON0+69R+VRCN0)/sumRN	VN26
	MN3[2:0]=010	VGAM1OUT–VD*(VRON0+70R+VRCN0)/sumRN	VN27
	MN3[2:0]=011	VGAM1OUT–VD*(VRON0+71R+VRCN0)/sumRN	VN28
	MN3[2:0]=100	VGAM1OUT–VD*(VRON0+72R+VRCN0)/sumRN	VN29
	MN3[2:0]=101	VGAM1OUT–VD*(VRON0+73R+VRCN0)/sumRN	VN30
	MN3[2:0]=110	VGAM1OUT–VD*(VRON0+74R+VRCN0)/sumRN	VN31
	MN3[2:0]=111	VGAM1OUT–VD*(VRON0+75R+VRCN0)/sumRN	VN32
VgN55	MN4[2:0]=000	VGAM1OUT–VD*(VRON0+80R+VRCN0)/sumRN	VN33
	MN4[2:0]=001	VGAM1OUT–VD*(VRON0+81R+VRCN0)/sumRN	VN34
	MN4[2:0]=010	VGAM1OUT–VD*(VRON0+82R+VRCN0)/sumRN	VN35
	MN4[2:0]=011	VGAM1OUT–VD*(VRON0+83R+VRCN0)/sumRN	VN36
	MN4[2:0]=100	VGAM1OUT–VD*(VRON0+84R+VRCN0)/sumRN	VN37
	MN4[2:0]=101	VGAM1OUT–VD*(VRON0+85R+VRCN0)/sumRN	VN38
	MN4[2:0]=110	VGAM1OUT–VD*(VRON0+86R+VRCN0)/sumRN	VN39
	MN4[2:0]=111	VGAM1OUT–VD*(VRON0+87R+VRCN0)/sumRN	VN40
VgN62	MN5[2:0]=000	VGAM1OUT–VD*(VRON0+87R+VRCN0+VRCN1)/sumRN	VN41
	MN5[2:0]=001	VGAM1OUT–VD*(VRON0+91R+VRCN0+VRCN1)/sumRN	VN42
	MN5[2:0]=010	VGAM1OUT–VD*(VRON0+95R+VRCN0+VRCN1)/sumRN	VN43
	MN5[2:0]=011	VGAM1OUT–VD*(VRON0+99R+VRCN0+VRCN1)/sumRN	VN44
	MN5[2:0]=100	VGAM1OUT–VD*(VRON0+103R+VRCN0+VRCN1)/sumRN	VN45
	MN5[2:0]=101	VGAM1OUT–VD*(VRON0+107R+VRCN0+VRCN1)/sumRN	VN46
	MN5[2:0]=110	VGAM1OUT–VD*(VRON0+111R+VRCN0+VRCN1)/sumRN	VN47
	MN5[2:0]=111	VGAM1OUT–VD*(VRON0+115R+VRCN0+VRCN1)/sumRN	VN48
VgN63	———	VGAM1OUT–VD*(VRON0+120R+VRCN0+VRCN1)/sumRN	VN49

Sum of positive resistor sumRP = 128R + VROP0 + VROP1 + VRCP0 + VRCP1

Sum of negative resistor sumRN = 128R + VRON0 + VRON1 + VRCN0 + VRCN1

Voltage difference VD = (VGAM1OUT – VGS)

Grayscale Voltage	Formula
V0	VgN0
V1	VgN1
V2	V3+(V1–V3)*(8/24)
V3	V8+(V1–V8)*(450/800)
V4	V8+(V3–V8)*(16/24)
V5	V8+(V3–V8)*(12/24)
V6	V8+(V3–V8)*(8/24)
V7	V8+(V3–V8)*(4/24)
V8	VgN8
V9	V20+(V8–V20)*(22/24)
V10	V20+(V8–V20)*(20/24)
V11	V20+(V8–V20)*(18/24)
V12	V20+(V8–V20)*(16/24)
V13	V20+(V8–V20)*(14/24)
V14	V20+(V8–V20)*(12/24)
V15	V20+(V8–V20)*(10/24)
V16	V20+(V8–V20)*(8/24)
V17	V20+(V8–V20)*(6/24)
V18	V20+(V8–V20)*(4/24)
V19	V20+(V8–V20)*(2/24)
V20	VgN20
V21	V43+(V20–V43)*(22/23)
V22	V43+(V20–V43)*(21/23)
V23	V43+(V20–V43)*(20/23)
V24	V43+(V20–V43)*(19/23)
V25	V43+(V20–V43)*(18/23)
V26	V43+(V20–V43)*(17/23)
V27	V43+(V20–V43)*(16/23)
V28	V43+(V20–V43)*(15/23)
V29	V43+(V20–V43)*(14/23)
V30	V43+(V20–V43)*(13/23)
V31	V43+(V20–V43)*(12/23)

Grayscale Voltage	Formula
V32	V43+(V20–V43)*(11/23)
V33	V43+(V20–V43)*(10/23)
V34	V43+(V20–V43)*(9/23)
V35	V43+(V20–V43)*(8/23)
V36	V43+(V20–V43)*(7/23)
V37	V43+(V20–V43)*(6/23)
V38	V43+(V20–V43)*(5/23)
V39	V43+(V20–V43)*(4/23)
V40	V43+(V20–V43)*(3/23)
V41	V43+(V20–V43)*(2/23)
V42	V43+(V20–V43)*(1/23)
V43	VgN43
V44	V55+(V43–V55)*(22/24)
V45	V55+(V43–V55)*(20/24)
V46	V55+(V43–V55)*(18/24)
V47	V55+(V43–V55)*(16/24)
V48	V55+(V43–V55)*(14/24)
V49	V55+(V43–V55)*(12/24)
V50	V55+(V43–V55)*(10/24)
V51	V55+(V43–V55)*(8/24)
V52	V55+(V43–V55)*(6/24)
V53	V55+(V43–V55)*(4/24)
V54	V55+(V43–V55)*(2/24)
V55	VgN55
V56	V60+(V55–V60)*(20/24)
V57	V60+(V55–V60)*(16/24)
V58	V60+(V55–V60)*(12/24)
V59	V60+(V55–V60)*(8/24)
V60	V62+(V55–V62)*(350/800)
V61	V62+(V60–V62)*(16/24)
V62	VgN62
V63	VgN63

Relationship between RAM data and voltage output levels (REV = “0”)

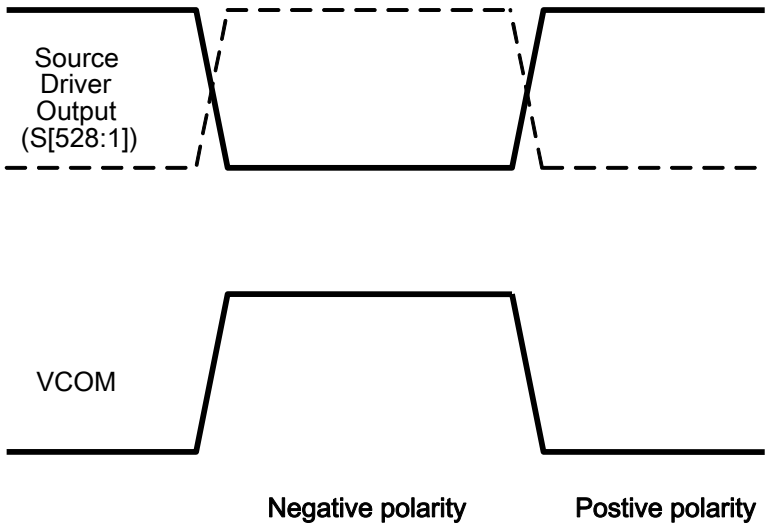


Figure 60 Relationship between Source Output and VCOM

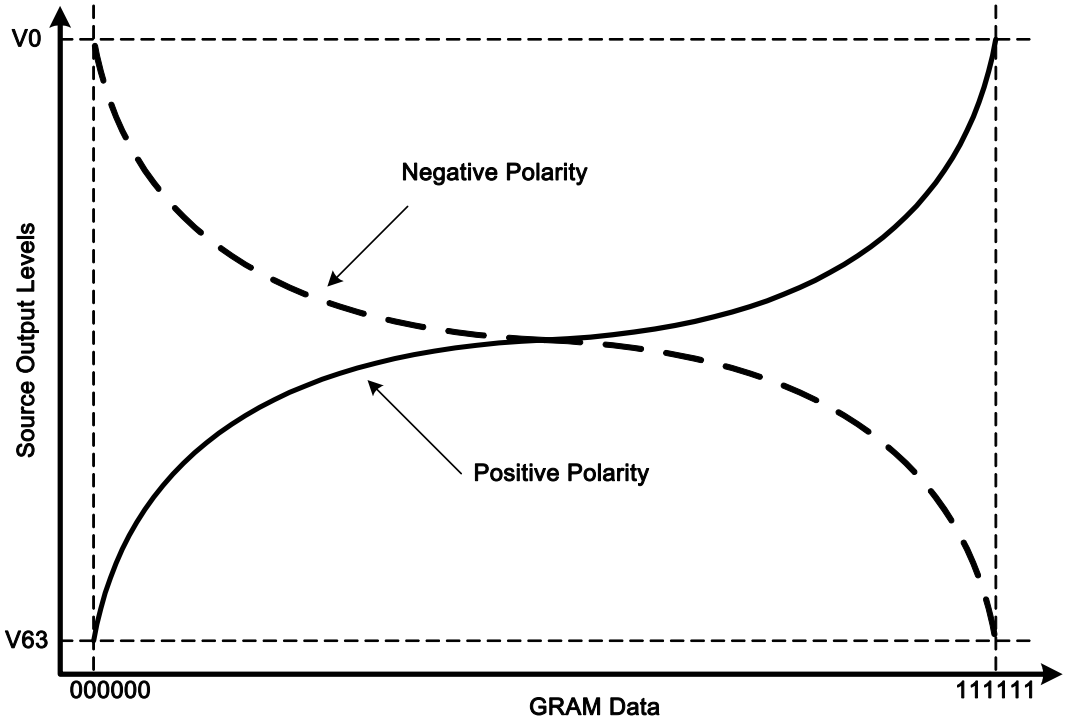


Figure 61 Relationship between GRAM Data and Output Level

14. Application

14.1. Configuration of Power Supply Circuit

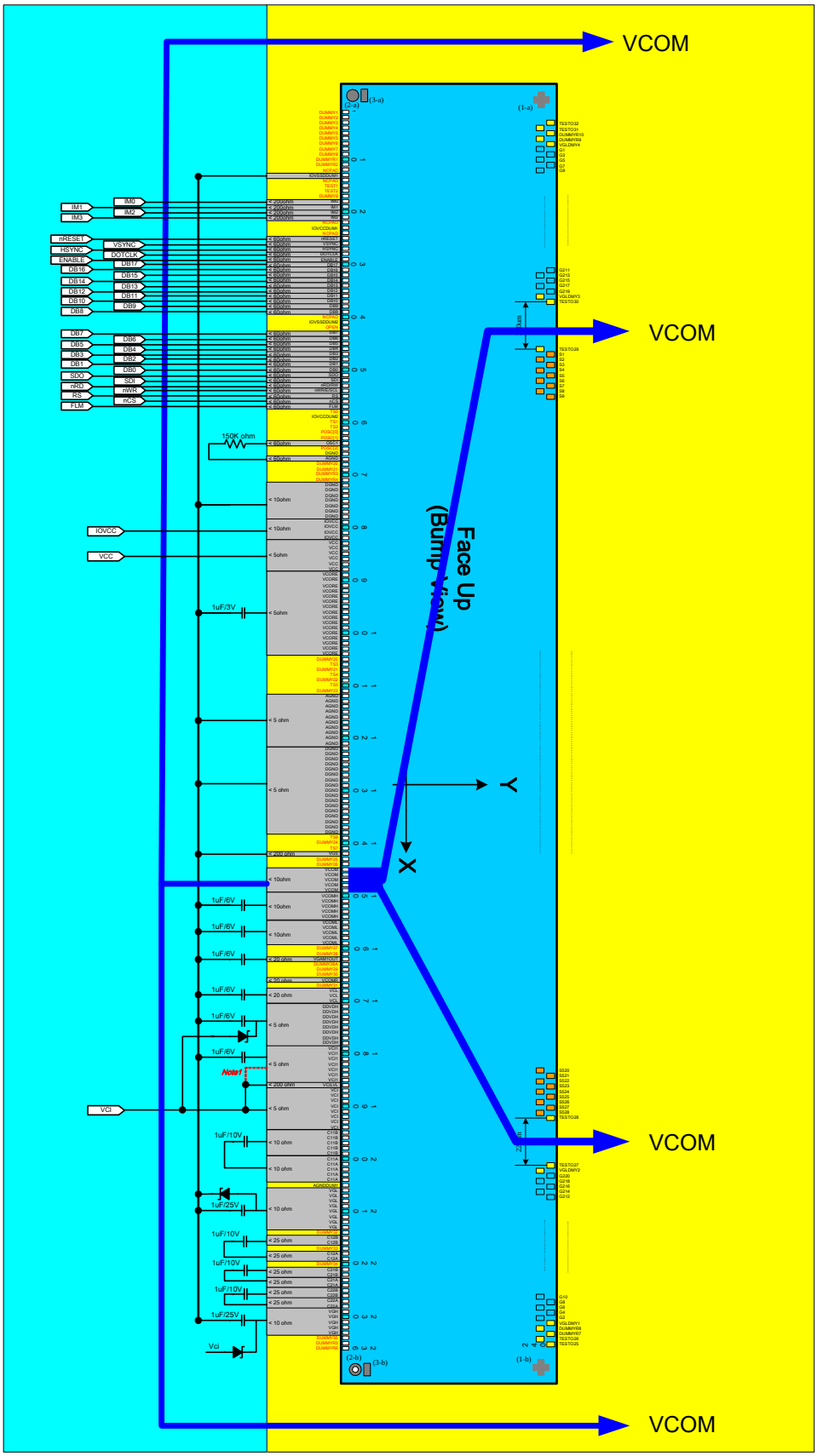


Figure 62 Power Supply Circuit Block

The following table shows specifications of external elements connected to the ILI9221's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 μF (B characteristics)	6.3V	VGAM1OUT, VCI1, VDDD, VCL, VCOMH, VCOML, C11A/B, C12A/B
	10V	DDVDH, C21A/B, C22A/B
	25V	VGH, VGL
Schottky diode	VF<0.4V/20mA at 25°C, VR ≥30V (Recommended diode: HSC226)	(AGND – VGL), (Vci – VGH), (Vci – DDVDH)
Variable resistor	> 200 kΩ	VCOMR

14.2. Display ON/OFF Sequence

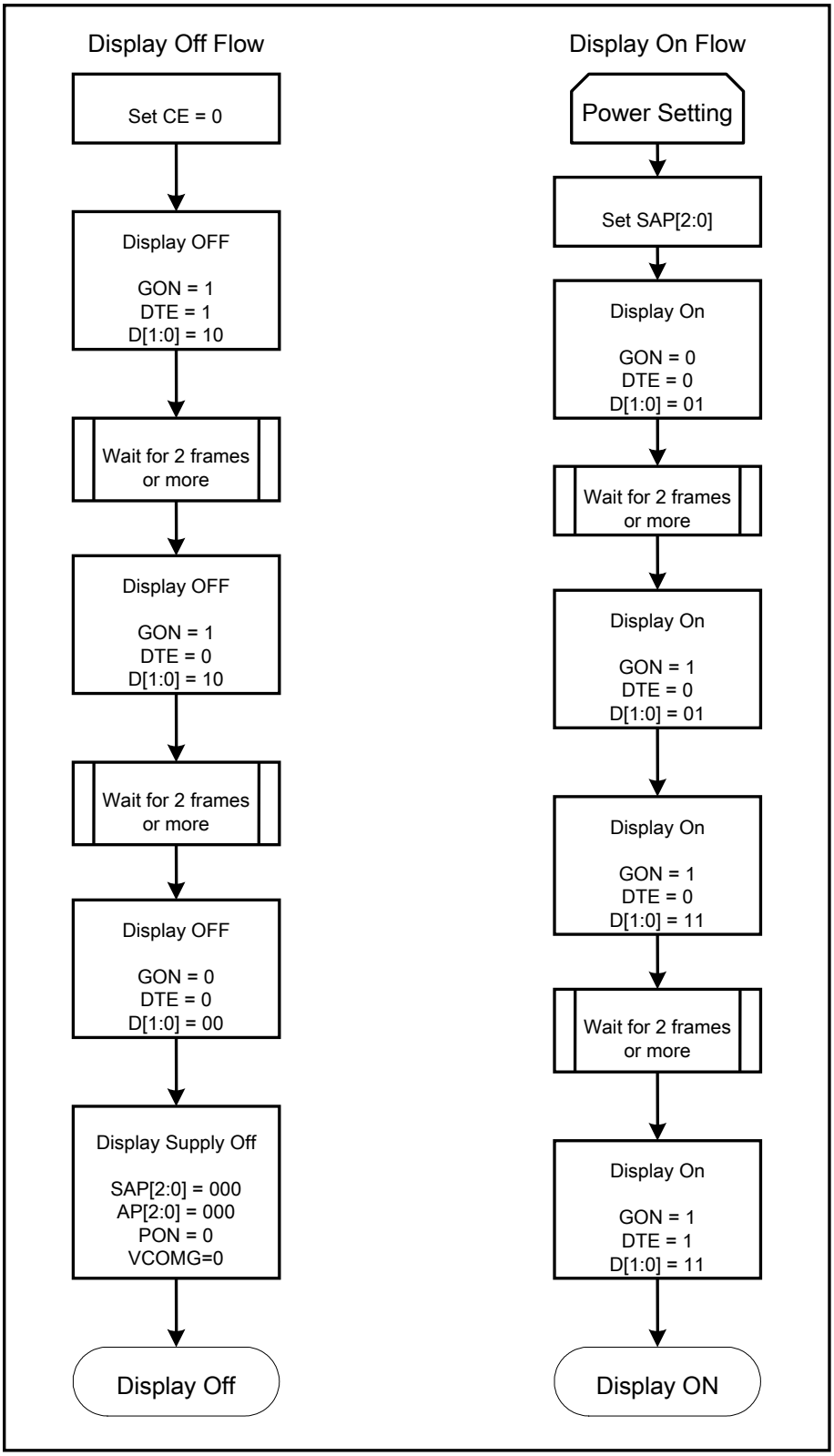


Figure 63 Display On/Off Register Setting Sequence

14.3. Standby and Sleep Mode

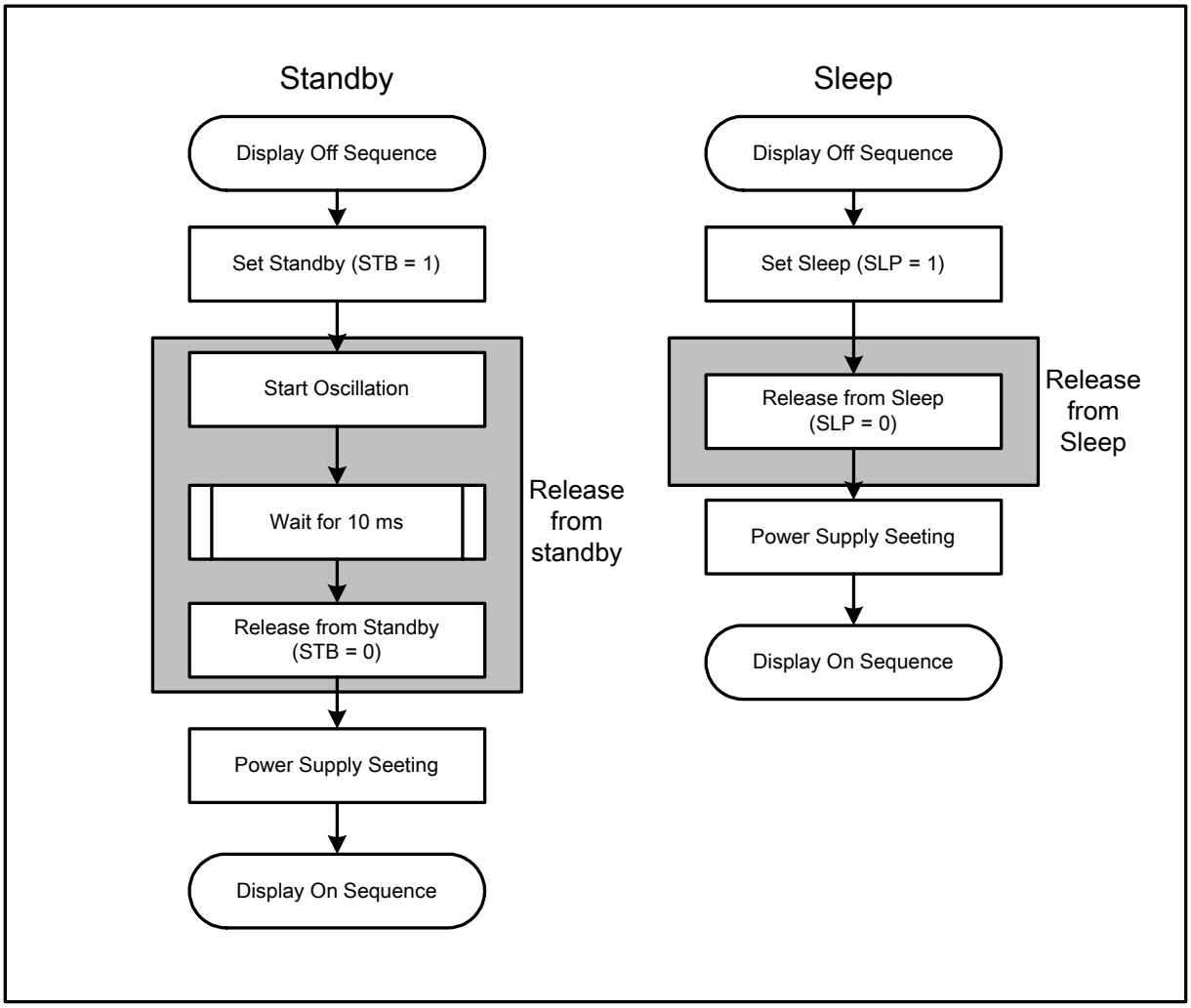


Figure 64 Standby/Sleep Mode Register Setting Sequence

14.4. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.

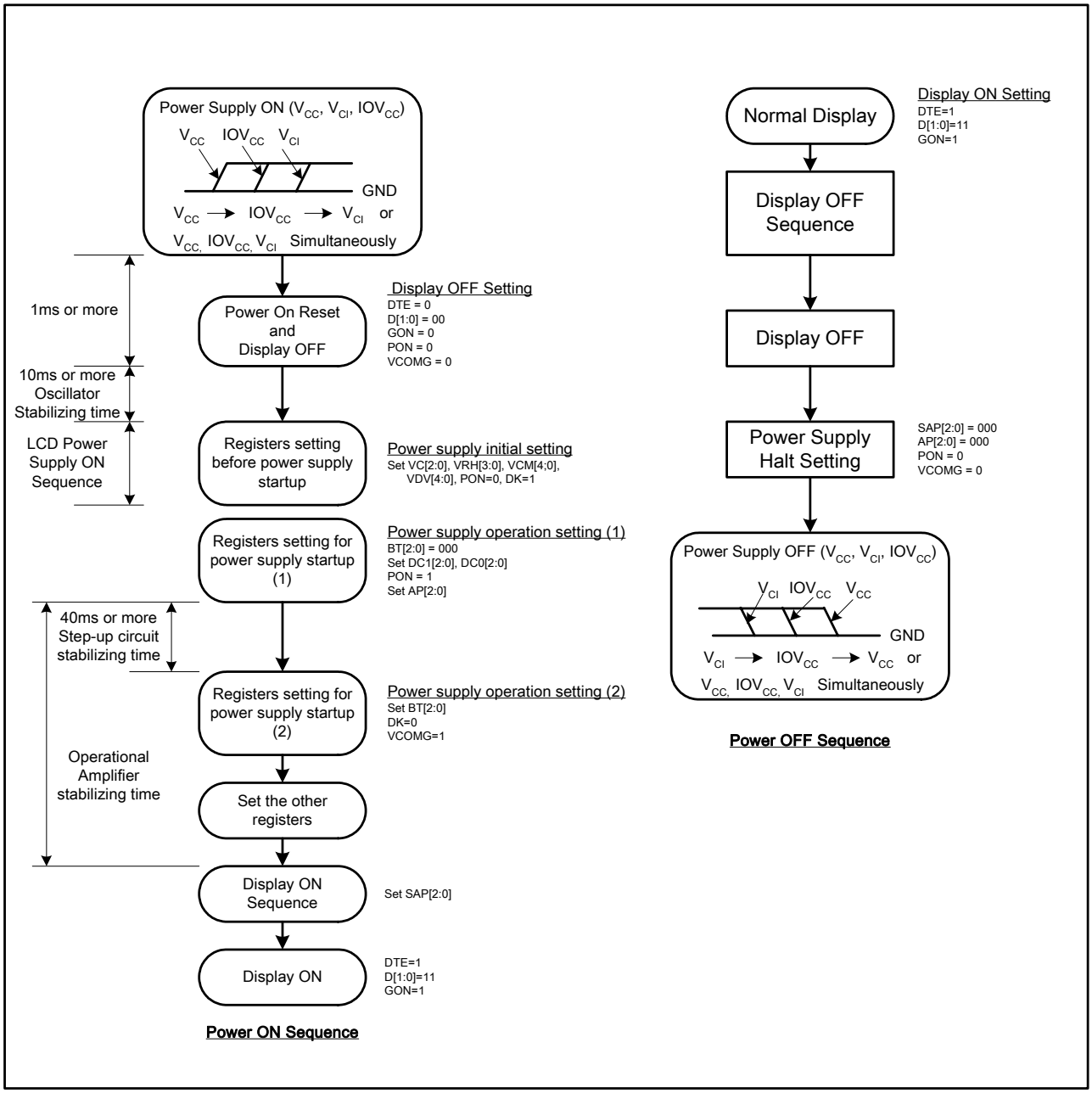


Figure 65 Power Supply ON/OFF Sequence

14.5. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9221 are as follows.

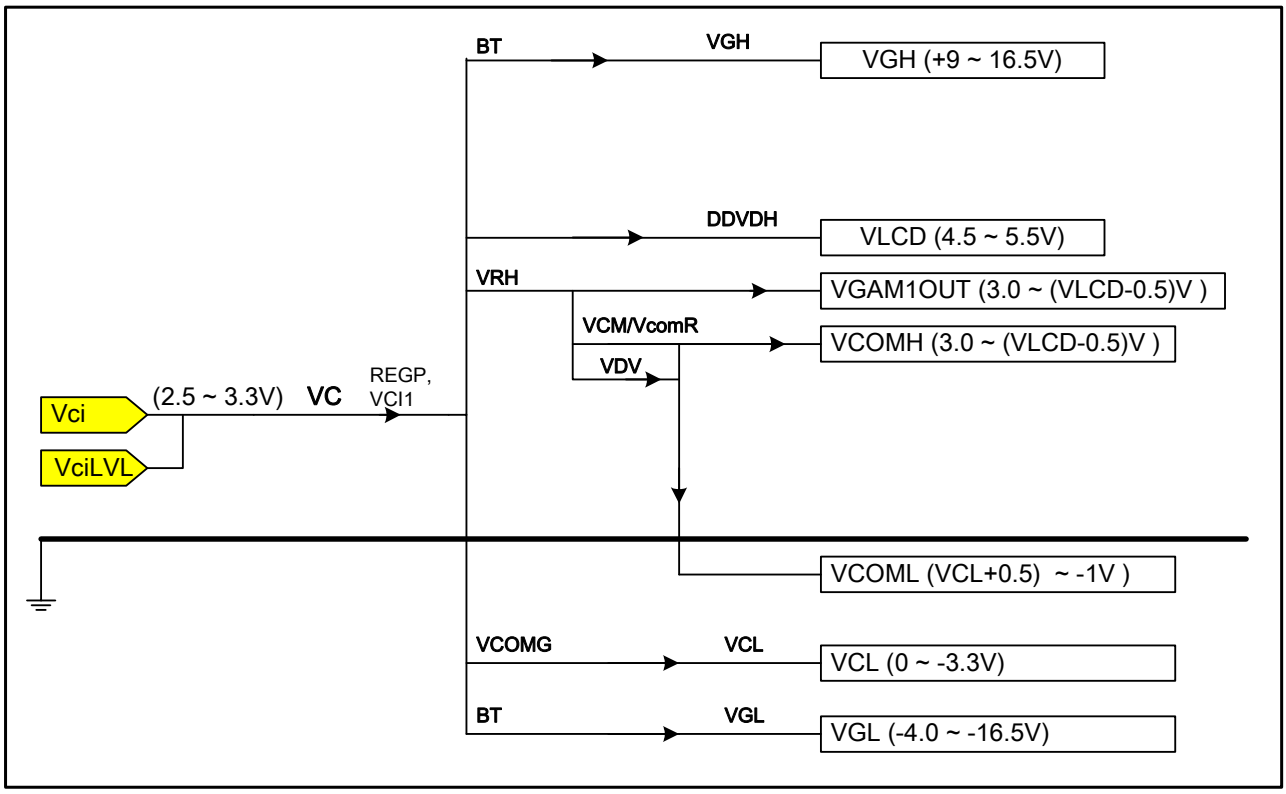


Figure 66 Voltage Configuration Diagram

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships (DDVDH – VGAM1OUT) > 0.5V, (VCOML1 – VCL) > 0.5V, (VCOML2 – VCL) > 0.5V are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

14.6. Applied Voltage to the TFT panel

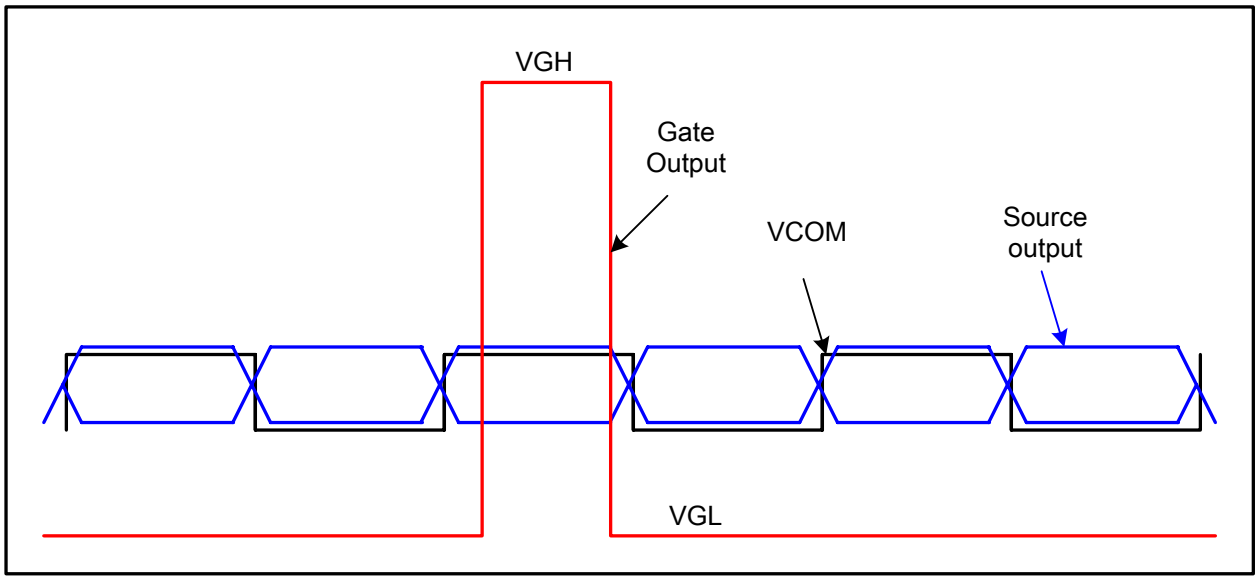


Figure 67 Voltage Output to TFT LCD Panel

14.7. Oscillator

ILI9221 generates oscillation with the ILI9221's internal RC oscillators by placing an external resistor between the OSC1 and OSC2 pins. The oscillation frequency varies with resistance value of external resistor, wiring distance, and operating supply voltage. For example, placing a Rosc resistor of larger resistance value or lower the supply voltage level will generate a lower oscillation frequency. See the "Notes to Electrical Characteristics" section for the relationship between resistance value of Rosc resistor and oscillation frequency.

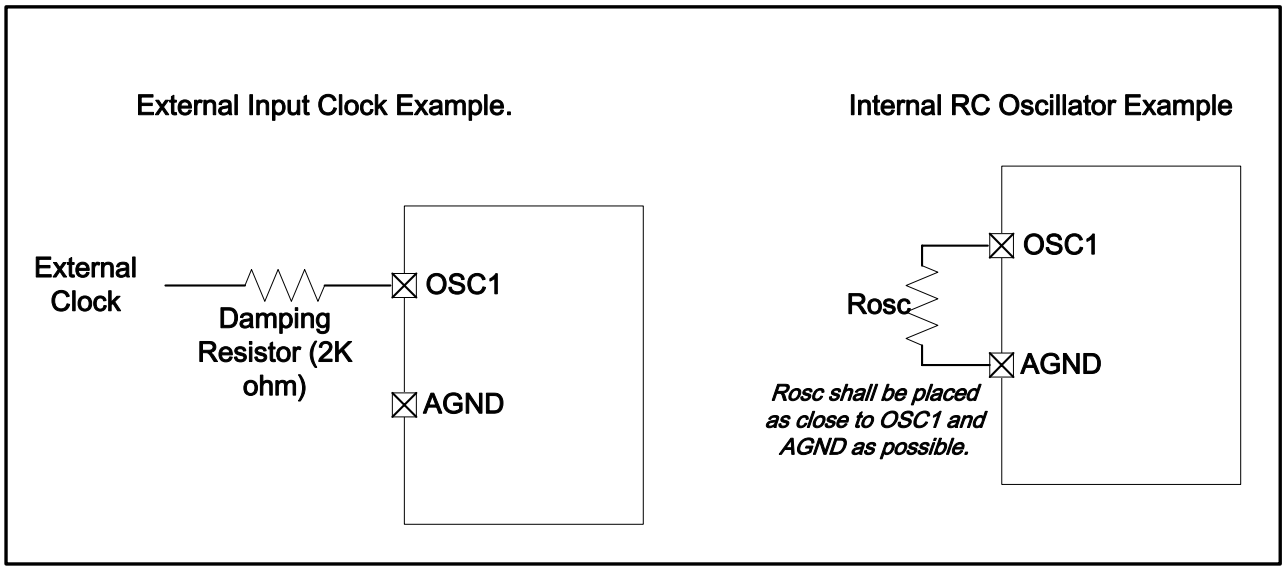


Figure 68 Oscillation Connection

14.8. Frame Rate Adjustment

The ILI9221 has a frame frequency adjustment function. The frame frequency for driving LCDs can be adjusted by registers (using the DIV, RTN bits) without changing the oscillation frequency.

To switch frame frequencies between when displaying a moving picture and when displaying a still picture, set a high oscillation frequency in advance. By doing so, it becomes possible to set a low frame frequency when displaying a still picture for saving power consumption and to set a high frame frequency when displaying a moving picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following formula. The frame frequency is adjusted by register using the 1H period adjustment bits (RTN bits) and the operation clock division bits (DIV bits).

Formula to calculate frame frequency

$$Formula\ rate = \frac{f_{osc.}}{Clock\ cycles\ per\ line \times division\ ratio \times (Lines + BP + FP)}$$

$f_{osc.}$: frequency if RC oscillation.
Clock cycles per line : RTN bits
Division ratio : DIV bits
Lines : number of lines for driving the LCD panel.
FP: Front porch lines
BP; Back porch lines

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive the LCD: 160 lines

1H period: 16 clock cycle (RTN[3:0] = “0000”)

Operational clock division ratio: 1/1

fosc = 60 Hz × (0 + 16) clock × 1/1 × (160 + 16) lines = 246 (kHz)

In this case, the RC oscillation frequency is 246 kHz. Adjust the external resistor of the RC oscillator to 246 kHz.

14.9. Partial Display Function

The ILI9221 allows selectively driving two images on the screen at arbitrary positions set in the screen drive position registers (R42h and R43h). Only the lines for displaying two images are selectively driven in order to reduce current consumption.

The first display drive position register (R42h) includes the start line setting bits (SS1[7:0]) and the end line setting bits (SE1[7:0]) for displaying the first image. The second display drive position register (R43h) includes the start line setting bits (SS2[7:0]) and the end line setting bits (SE2[7:0]) for displaying the second image. The second display control is effective when the SPT bit is set to “1”. The total number of lines driven for displaying the first and second display must be less than the number of lines set with the NL[4:0] bits.

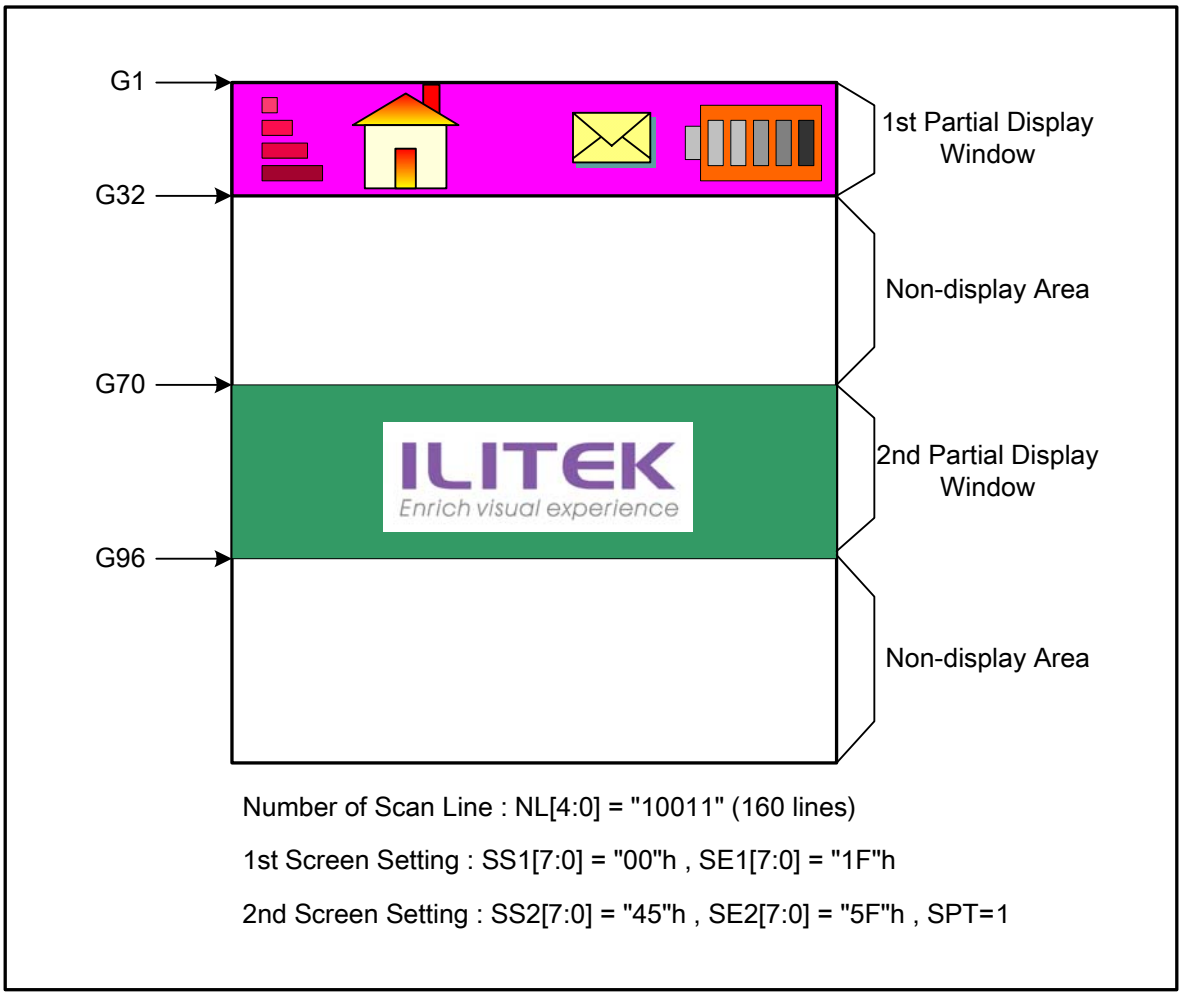


Figure 69 Partial Display Example

Constraints in Setting the 1st/2nd Screen Drive Position Register

When setting the start line setting bits (SS1[7:0]) and the end line setting bits (SE1[7:0]) of the first display drive position register (R42h), and the start line setting bits (SS2[7:0]) and the end line setting bits (SE2[7:0]) of the second display drive position register (R43h), it is necessary to satisfy the following conditions to display screens correctly.

One Screen Drive (SPT = "0")

Register Settings	Display Operation
(SE1[7:0] - SS1[7:0]) = NL	Full screen display The area of (SE1[7:0] - SS1[7:0]) is normally displayed.
(SE1[7:0] - SS1[7:0]) < NL	Partial screen display The area of (SE1[7:0] - SS1[7:0]) is normally displayed. The rest of the area is a white display irrespective of data in RAM.
(SE1[7:0] - SS1[7:0]) > NL	Setting disabled

Two Screens Drive (SPT = "1")

Register Settings	Display Operation
((SE1[7:0] - SS1[7:0]) + (SE2[7:0] - SS2[7:0]))= NL	Full screen display The area of (SE2[7:0] - SS1[7:0]) is normally displayed.
((SE1[7:0] - SS1[7:0]) + (SE2[7:0] - SS2[7:0])) < NL	Partial screen display The area of (SE2[7:0] - SS1[7:0]) is normally displayed. The rest of the area is a white display irrespective of data in RAM.
((SE1[7:0] – SS1[7:0]) + (SE2[7:0] - SS2[7:0])) > NL	Setting disabled

Note 1) Be sure that SS1[7:0] ≤ SE1[7:0] < SS2[7:0] ≤ SE2[7:0] ≤ "DB"H.

Note 2) Be sure that (SE2[7:0] - SS1[7:0]) ≤ NL.

Source outputs in non-display areas

		Source Output in Non-display Area		Operating amplifier in non-display area
PT1	PT0	Positive Polarity	Negative Polarity	
0	0	V63	V0	V0 ~ V63
0	1	V63	V0	V0 ~ V63
1	0	DGND	DGND	V0 ~ V63
1	1	Hi-Z	Hi-Z	V0 ~ V63

Gate outputs in non-display areas

PTG	PTG	Gate output in non-display area	Source output in non-display area	Vcom Output
0	0	Normal scan	Set with the PT[1:0] bits	VCOMH-VCOML amplitude
0	1	VGL (fixed)	Set with the PT[1:0] bits	VCOMH-VCOML amplitude
1	0	Interval scan	Set with the PT[1:0] bits	VCOMH-VCOML amplitude
1	1	Setting disabled	-	-

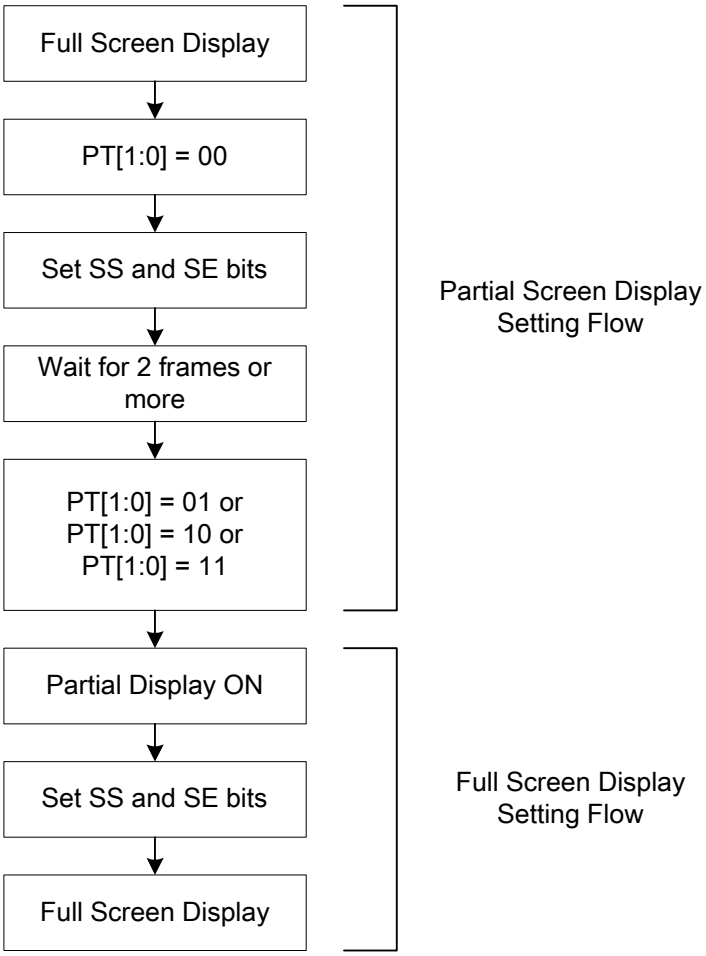


Figure 70 Partial Display Setting Flow

14.10. 8-color Display

ILI9221 supports an 8-color display mode. The grayscale level to be used is V0 and V63 with R5, G5, B5 decoding, and the other levels (V1-V62) are halted to reduce power consumption. In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

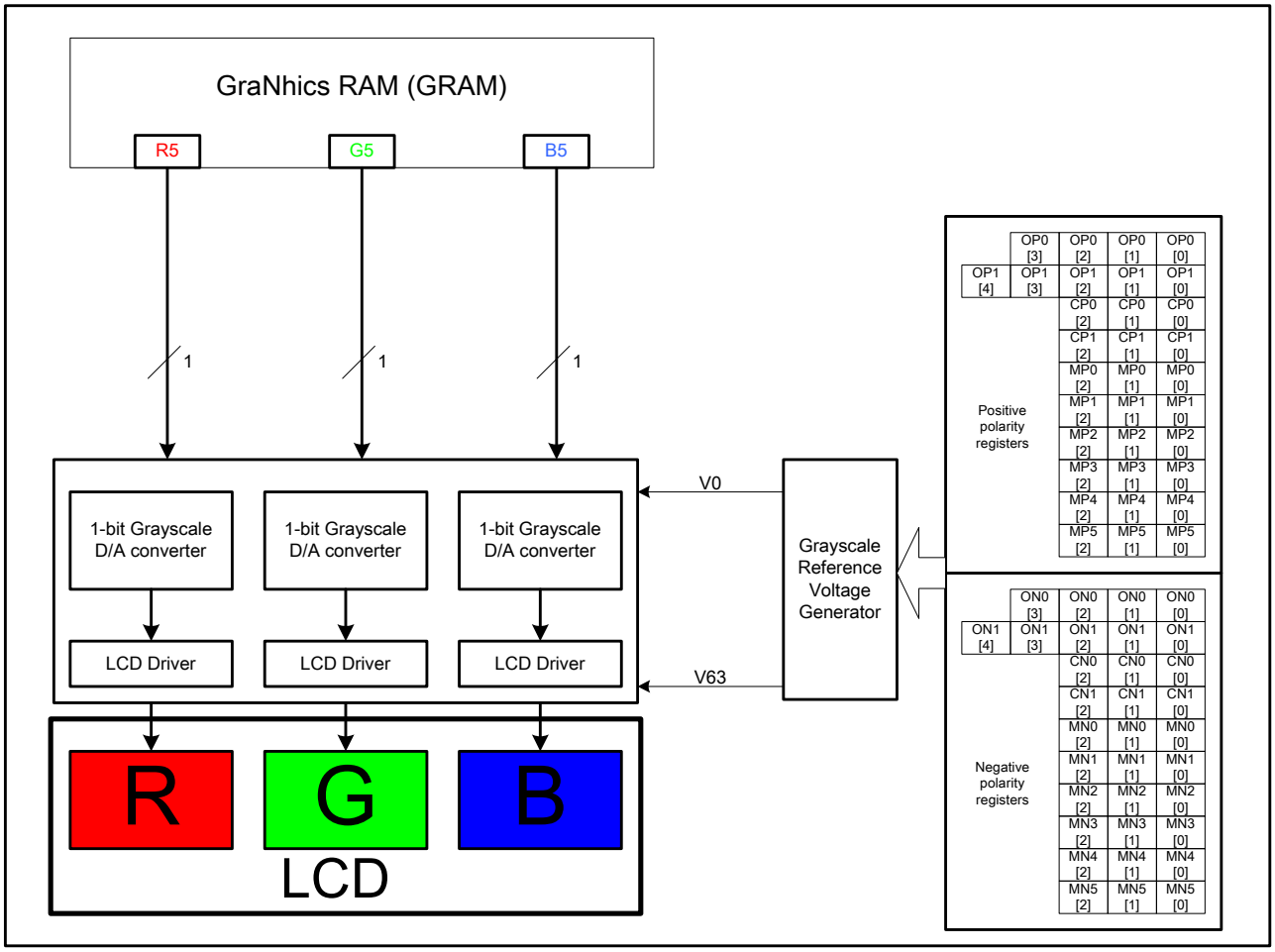


Figure71 8-color Display Mode

The follow figure is the switch sequence between the 262,144-color mode and 8-color mode:

15. Electrical Characteristics

15.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9221 is used out of the absolute maximum ratings, the ILI9221 may be permanently damaged. To use the ILI9221 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9221 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	VCC, IOVCC	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI - AGND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	DDVDH - AGND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	AGND -VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	DDVDH - VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH - AGND	V	-0.3 ~ + 18.5	1, 5
Power supply voltage (1)	AGND - VGL	V	-0.3 ~ + 18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:
1. VCC,DGND must be maintained
2. (High) (VCC = VCC) ≥ DGND (Low), (High) IOVCC ≥ DGND (Low).
3. Make sure (High) VCI ≥ DGND (Low).
4. Make sure (High) DDVDH ≥ ASSD (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. For die and wafer products, specified up to 85°C.
9. This temperature specifications apply to the TCP package

15.2. DC Characteristics

(VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V, Ta= -40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VCC= 1.8 ~ 3.3V	0.8*IOVCC	-	IOVCC	-
Input low voltage	V_{IL}	V	VCC= 1.8 ~ 3.3V	-0.3	-	0.2*IOVCC	-
Output high voltage(1) (DB0-17 Pins)	V_{OH1}	V	IOH = -0.1 mA	0.8*IOVCC	-	-	-
Output low voltage (DB0-17 Pins)	V_{OL1}	V	IOVCC=1.65~3.3V VCC= 2.4 ~ 3.3V IOL = 0.1mA	-	-	0.2*IOVCC	-
I/O leakage current	I_{LI}	µA	Vin = 0 ~ VCC	-0.1	-	0.1	-
Current consumption during normal operation (V_{CC} – DGND)	I_{OP}	µA	VCC=3.0V , Ta=25°C , fOSC = 177KHz (176 Line) GRAM data = 0000h	-	100 (VCC)	-	-
Current consumption during standby mode (V_{CC} – DGND)	I_{ST}	µA	VCC=3V , Ta=25 °C	-	5	10	-
LCD Drive Power Supply Current (DDVDH-DGND)	ILCD	mA	VCC=3V , VGAM1OUT=5.0V DDVDH=5.5V , fOSC = 177KHz (160 line) , Ta=25 °C, GRAM data = 0000h, REV="0", SAP="001", ON4-0="0", OP4-0="0", MP52-00="0", MN52-00="0", CP12-00="0" CN12-00="0	-	3.0	-	-
LCD Driving Voltage (DDVDH-DGND)	DDVDH	V	-	4.5	-	6	-
Output voltage deviation		mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-10	-	10	-

15.3. Clock Characteristics

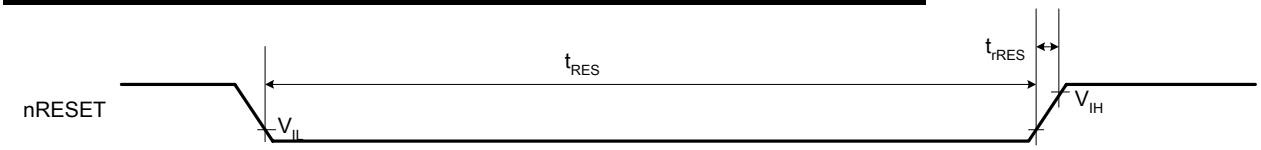
VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
External Clock Frequency	fcp	VCC = 2.4 ~ 3.3V	275	335	395	KHz
External Clock Duty	f_{Duty}	VCC = 2.4 ~ 3.3V	45	50	55	
External Clock Rising Time	Trcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
External Clock Falling Time	Tfcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
RC oscillation clock	f_{OSC}	Rf = 130KΩ, VCC = 2.8V	275	335	395	KHz

15.4. Reset Timing Characteristics

Reset Timing Characteristics (VCC = 1.8 ~ 3.3 V, IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	µs	-	-	10



15.5. LCD Driver Output Characteristics

Item	Symbol	Timing diagram	Min.	Typ.	Max.	Unit
Driver output delay time	tdd	VCC=2.8V, DDVDH=5.5V, VGAM1OUT=5.0V, RC oscillation: fosc =315kHz (220 lines), Ta=25°C REV=0, SAP=010, AP=010, 0N14-00=0, 0P14-00=0, MP52-00=0, MN52-00=0, CP12-00=0, CN12-00=0, Load resistance R=10kΩ, Load capacitance C=20pF • when the level changes from a same grayscale level on all pins • Time to reach +/-35mV when VCOM polarity inverts	-	35	-	µs

15.6. AC Characteristics

15.6.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	100	-	-	-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	50	-	500	-
Write high-level pulse width		PW_{HW}	ns	50	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_{H}	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	

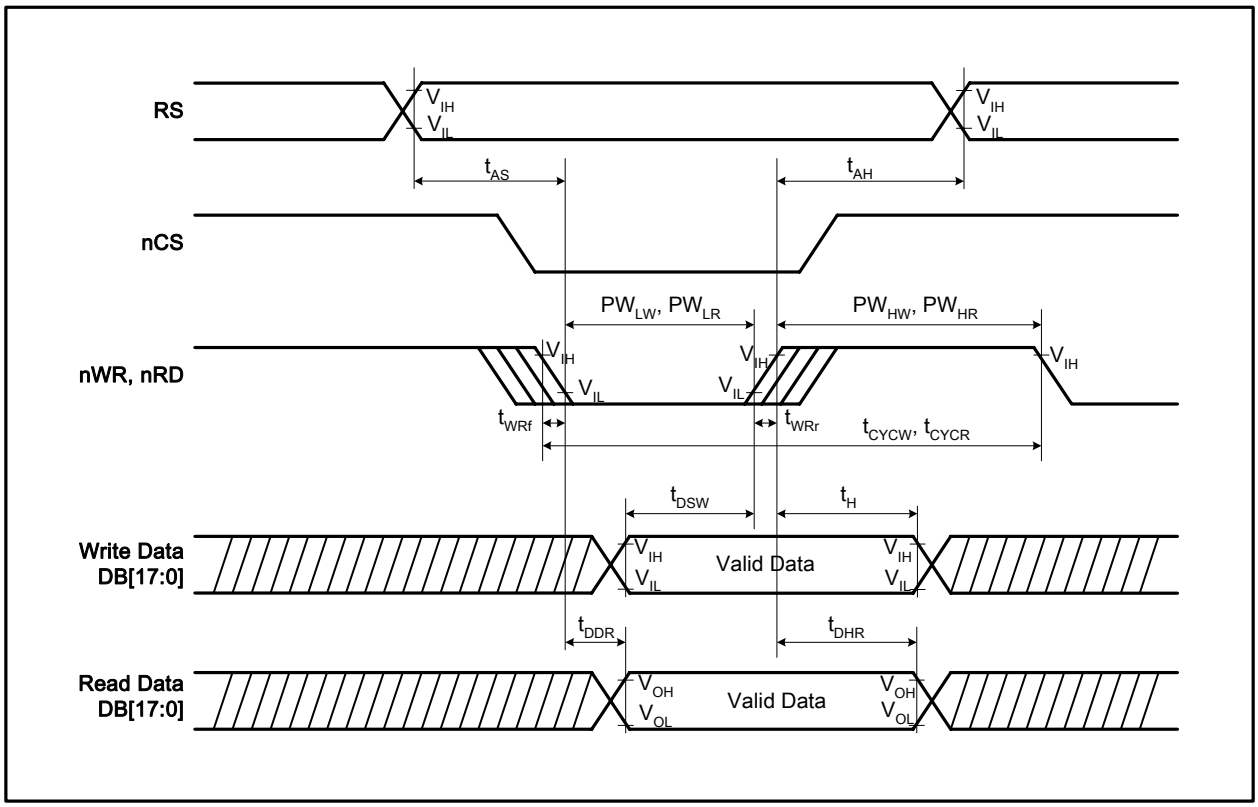


Figure 72 i80-System Bus Timing

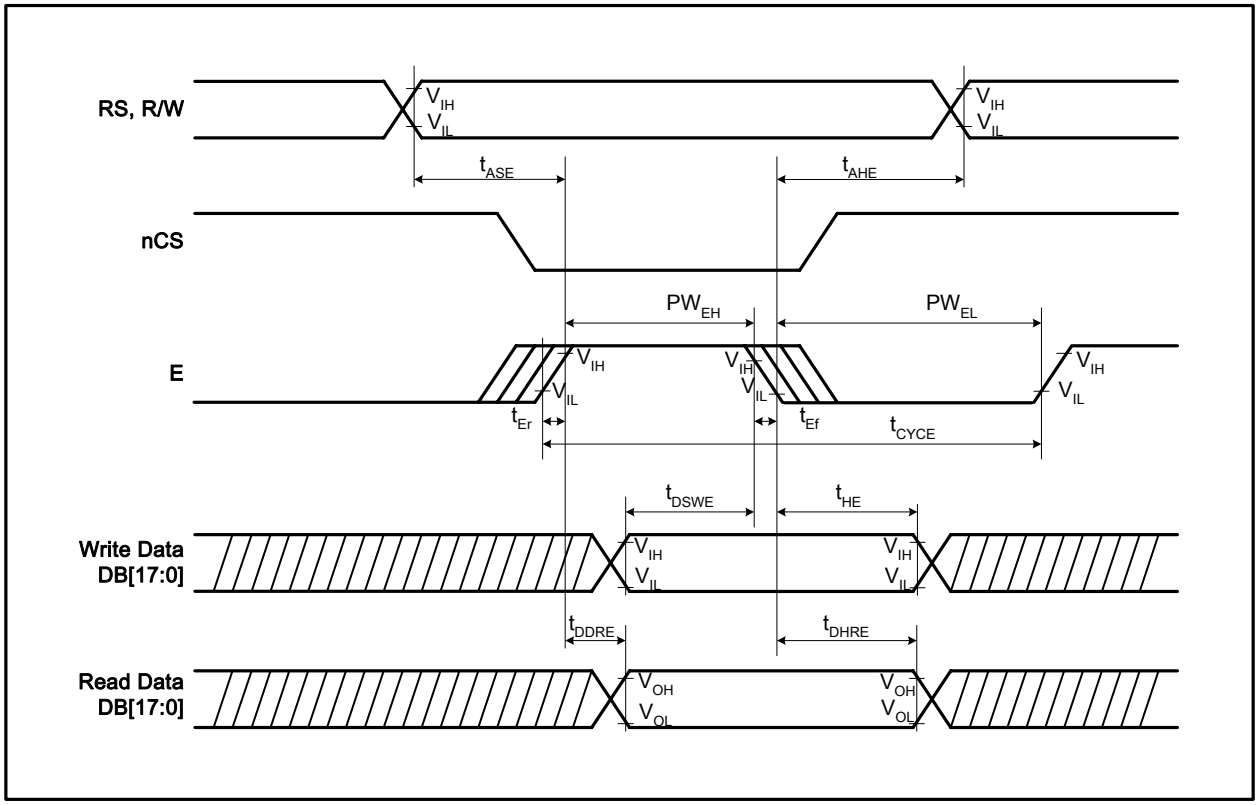


Figure 73 M68-System Bus Timing

15.6.2. M68-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCEW}	ns	100	-	-	-
	Read	t_{CYCER}	ns	300	-	-	-
Write low-level pulse width		PW_{ELW}	ns	50	-	500	-
Write high-level pulse width		PW_{EHW}	ns	50	-	-	-
Read low-level pulse width		PW_{ELR}	ns	150	-	-	-
Read high-level pulse width		PW_{EHR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{ASE}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			10	-	-	
Address hold time		t_{AHE}	ns	5	-	-	
Write data set up time		t_{DSWE}	ns	10	-	-	
Write data hold time		t_{HE}	ns	15	-	-	
Read data delay time		t_{DDRE}	ns	-	-	100	
Read data hold time		t_{DHRE}	ns	5	-	-	

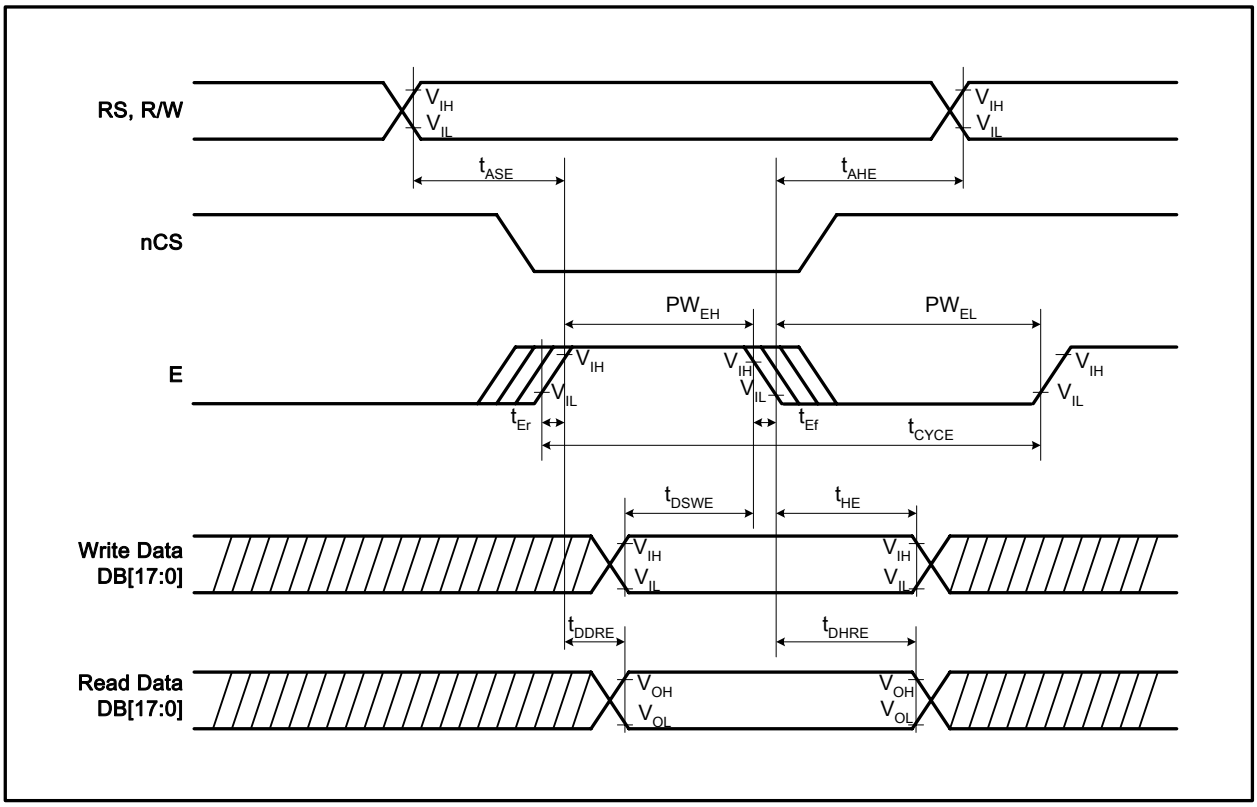


Figure74 M68-System Interface Timing

15.6.3. Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.653.3V and VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	μs	100	-	-	
	Read (transmitted)	t_{SCYC}	μs	200	-	-	
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	
	Read (transmitted)	t_{SCH}	ns	100	-	-	
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	
	Read (transmitted)	t_{SCL}	ns	100	-	-	
Serial clock rise / fall time		t_{SCr}, t_{SCf}	ns	-	-	5	
Chip select set up time		t_{CSU}	ns	10	-	-	
Chip select hold time		t_{CH}	ns	50	-	-	
Serial input data set up time		t_{SISU}	ns	20	-	-	
Serial input data hold time		t_{SIH}	ns	20	-	-	
Serial output data set up time		t_{SOD}	ns	-	-	100	
Serial output data hold time		t_{SOH}	ns	5	-	-	

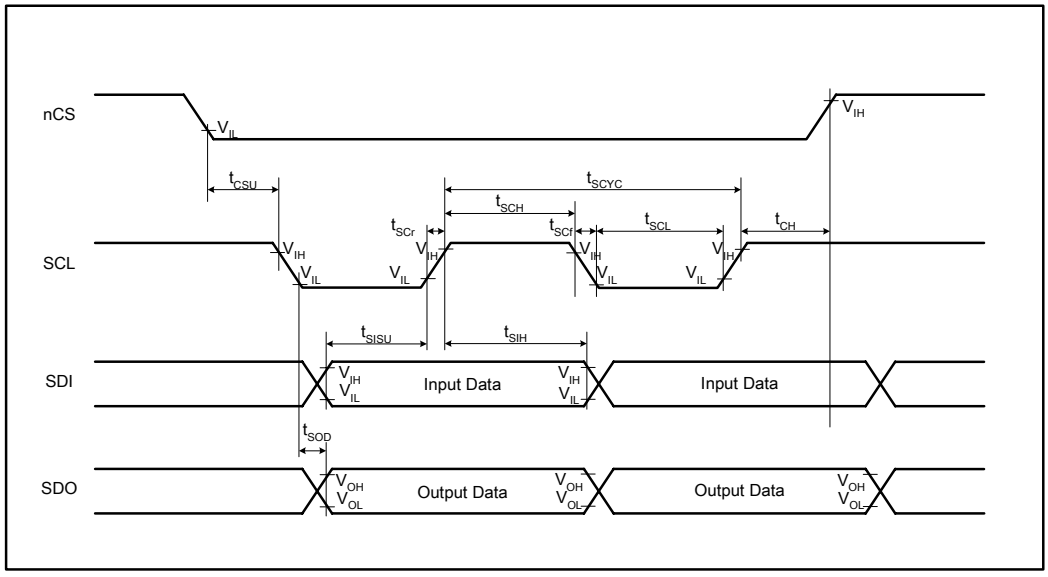


Figure 75 SPI System Bus Timing

15.6.4. RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

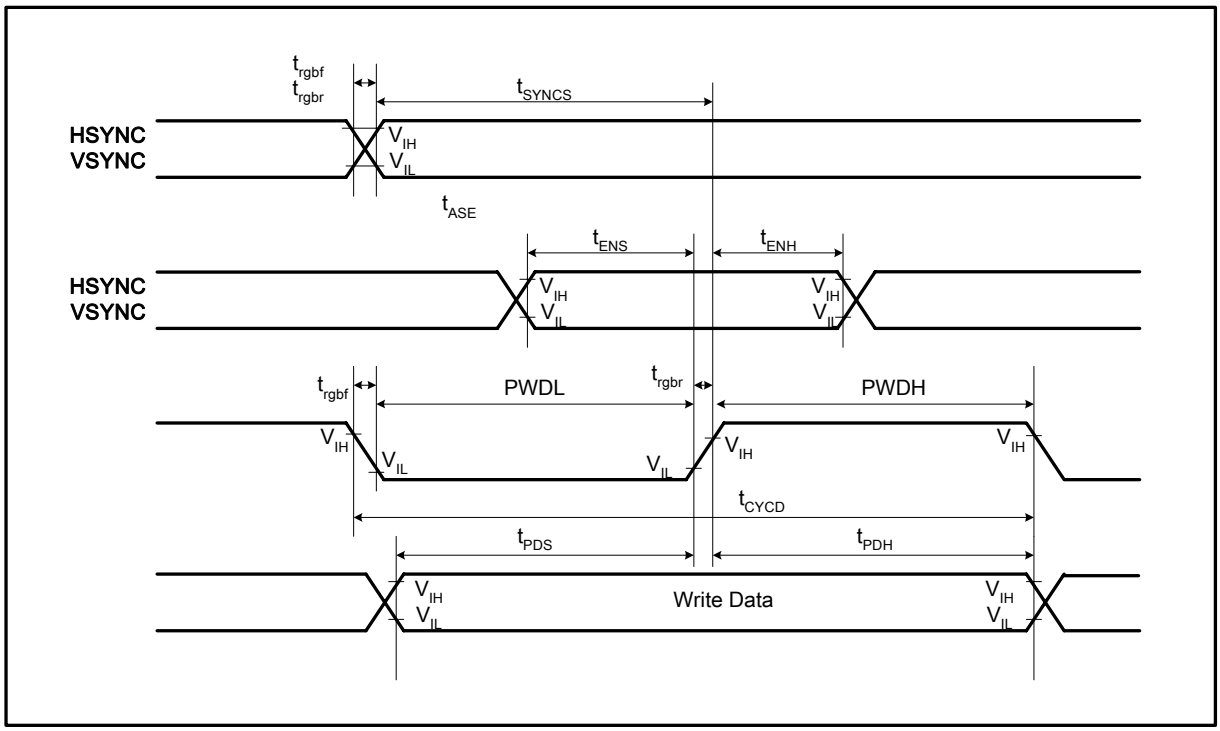


Figure76 RGB Interface Timing

16. Revision History

Version No.	Date	Page	Description
V.01	2006/4/17		New Created
V.011	2006/5/9	14 -18	Pads location diagram and coordinate
V.012	2006/5/10	14	Update the height of ILI9221, (1250um → 1280um)
V.013	2006/5/24	14 ~ 19 110	Update the height of ILI9221, (1280um → 1250um) Remove pin 237 ~ 239, pin 1004~1006
V.014	2006/6/12	10, 11	Add the SDI/SDO description
V.015	2006/8/10		Let VCOMR as floating in Application Circuit