DATA SHEET

(DOC No. HX8357-D00/D01-DS)

HX8357-D00/D01

320RGB x 480 dot, 16M color,
with internal GRAM,
TFT Mobile Single Chip Driver

Temporary Version 00 April, 2012

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1. General Description

This document describes Himax's HX8357-D00/D01 supports HVGA resolution driving controller. The HX8357-D00/D01 is designed to provide a single-chip solution that combines a source driver, power supply circuit to drive a TFT-LCD panel with 320RGBx480 dots at maximum.

The HX8357-D00/D01 can be operated in low-voltage condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8357-D00/D01 also supports various functions to reduce the power consumption of a TFT-LCD panel via software control.

The HX8357-D00/D01 supports several interface modes, including MPU MIPI DBI Type B interface mode and MIPI DPI/DBI Type C interface mode. The HX8357-D01 also supports MIPI DSI (Display Serial Interface) interface mode. The interface mode is selected by the external hardware pins IM2~0.

The HX8357-D00/D01 is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

2.1Display

- Resolution:
  - 320(H) x RGB(H) x 480(V)

- Display Color modes
  - Normal Display Mode On
    1. DBI Interface
       a. 65k colors (R(5),G(6),B(5))
       b. 262k colors (R(6),G(6),B(6))
       c. Virtual 24 bits colors (R(8),G(8),B(8))
    2. DPI Interface
       a. 65k colors (R(5),G(6),B(5))
       b. 262k colors (R(6),G(6),B(6))
       c. 16M colors (R(8),G(8),B(8))
    3. MIPI Interface (For HX8357-D01 only)
       a. 65k colors (R(5),G(6),B(5))
       b. 262k colors (R(6),G(6),B(6))
       c. Virtual 24 bits colors (R(8),G(8),B(8))
  - Idle Mode On
    - 8 (R(1),G(1),B(1)) colors

2.2Display module

- Frame Memory area 320 (H) x 480 (V) x 18 bits
- On module DC/DC converter
- VSP = 5.2 V for two time pump (Power supply for driver circuit range)
- VSP = 6.2 V for three time pump (Power supply for driver circuit range)
- VSN = -5.2 V for two time pump (Power supply for driver circuit range)
- VSN = -6.2 V for three time pump (Power supply for driver circuit range)
- VSPR =3.3V to 5.8V (Positive Source output voltage range)
- VSNR= -3.3V to -5.8V (Negative Source output voltage range)
- VGH = +10.0 to +15.3V (Positive Gate output voltage range)
- VGL = -7.5 to -12.8V (Negative Gate output voltage range)
- VCOM=-2.5V to 0V

2.3Display control interface

- MIPI-DBI 8-/9-/16-/18-/24-bit MPU parallel interface.
- MIPI-DBI Serial data transfer interface.
- MIPI-DPI 8-/16-/18-/24-data lines parallel video (RGB) interface.
- MIPI-DSI interface.(for Display Serial Interface Version 1.01 and D-PHY Version 1.00)

2.4Input power

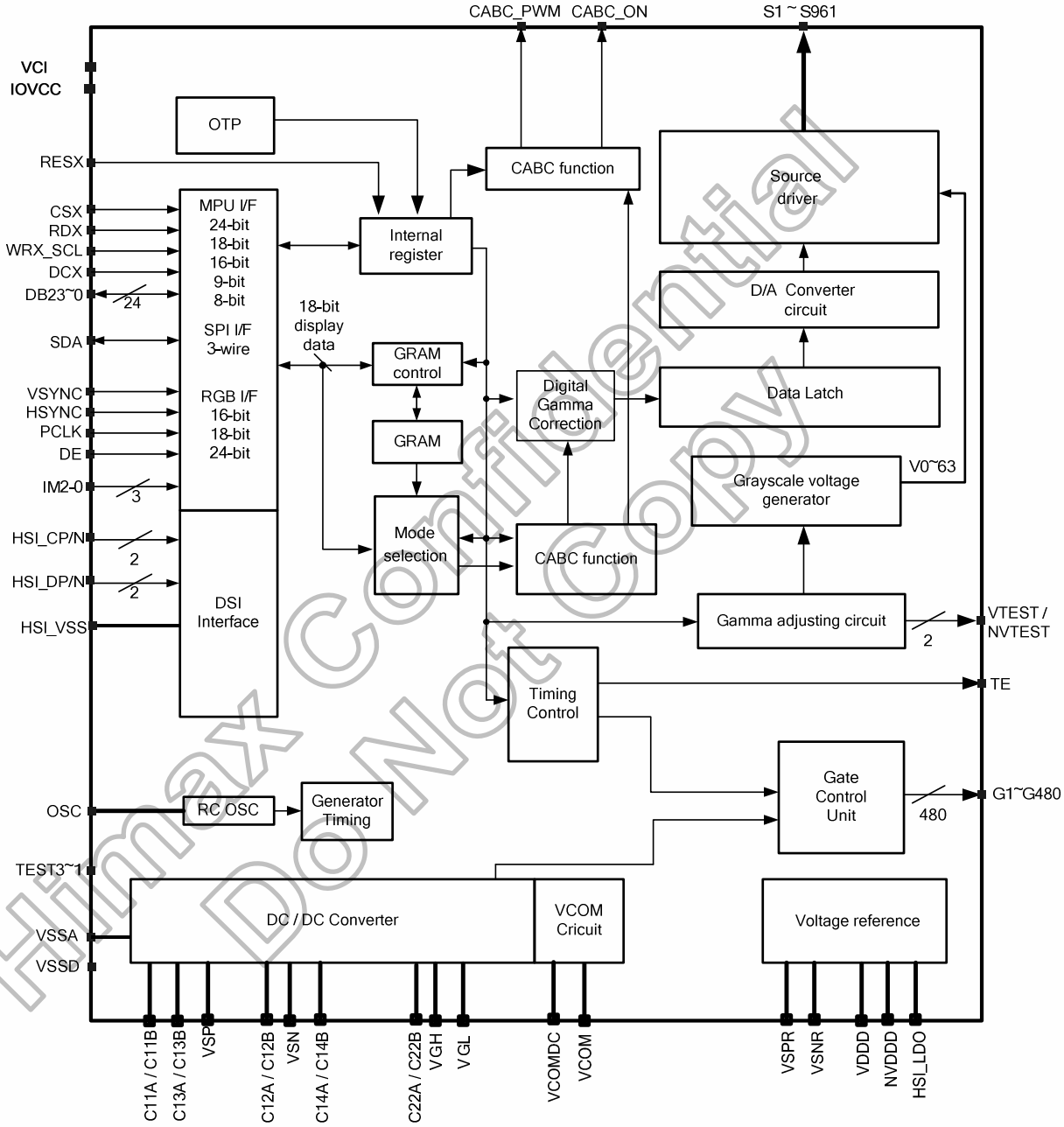
- Logic power supply (IOVCC): 1.65V ~ 3.3V
- Analog power supply (VCI): 2.5V ~ 3.3V

2.5Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- One chip solution for COG assembly
- Support 24-bits Input Image function
- Support 1-dot/2-dot/4-dot/column inversion/Zig-Zag inversion
- Support Area scrolling
- Support Partial display mode
- Support Deep standby mode
- Support normal black/normal white LCD
- Support wide view angle display
- On-chip OTP (One-time-programming) and MTP(four-time-programming for ID and VCOM register)
- Built-in internal OTP power
- Support Content Adaptive Brightness Control(CABC) function
- Support Color enhancement function
- Support Digital 3-Gamma function
- Operating temperature range : -40℃~ 85℃

3. Block Diagram

3.1Block diagram



3.2Pin description

<table>
<tr><th colspan="5">Interface Logic Pin</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IM2,IM1,IM0</td><td>I</td><td>3</td><td>VSSD/ IOVCC</td><td>System interface select.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI TYPE-B 18-bit/24-bit</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI TYPE-B 9-bit</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI TYPE-B 16-bit</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI TYPE-B 8-bit</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Not use</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DBI TYPE-C Option 1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI DSI (For HX8357-D01 only)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DBI TYPE-C Option 3</td></tr>
</table>
If not used, please fix this pin to IOVCC or VSSD level.</td></tr>
<tr><td>CSX</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
Fix it to IOVCC when not used.</td></tr>
<tr><td>WRX_SCL</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-B mode: Serves as a write signal and write data at the low level.
DBI Type-C mode: it servers as SCL (Serial Clock)
Fix it to IOVCC or VSSD level when not used.</td></tr>
<tr><td>RDX</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-B: Serves as a read signal and read data at the low level.
If not used, please fix this pin at IOVCC or GND level</td></tr>
<tr><td>DCX</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-B, Type-C Option 3: Data / Command Selection pin
If not used, please fix this pin at IOVCC or GND level.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Vertical synchronizing signal in DPI interface.
Let to open or connected to VSSD.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Horizontal synchronizing signal in DPI interface.
Let to open or connected to VSSD.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal in DPI I/F mode.
Let to open or connected to VSSD.</td></tr>
<tr><td>PCLK</td><td>I</td><td>1</td><td>MPU</td><td>Data enable signal in DPI interface.
Let to open or connected to VSSD.</td></tr>
<tr><td>RESX</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.</td></tr>
<tr><td>DIN_SDA</td><td>I/O</td><td>1</td><td>MCU</td><td>Serial data input pin and output pin in serial bus system interface.
The data is inputted on the rising edge of the SCL signal.
If not used, please let it open</td></tr>
<tr><td>DOUT</td><td>O</td><td>1</td><td>MPU</td><td>Serial data output.
If SDO_EN=0, DOUT is not use.
If SDO_EN=1, DOUT is serial data output.
Let it to open in MPU interface mode.</td></tr>
<tr><td>DB17~0
DB18
TS0_DB19
TS1_DB20
TS2_DB21
TS3_DB22
TS4_DB23</td><td>I/O</td><td>24</td><td>MPU</td><td>24-bit bi-directional data bus.
The unused pins let to open or connected to VSSD.</td></tr>
</table>

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S961	O	961	LCD	Output voltages applied to the liquid crystal.
G1~G480	O	480	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open).
VCOM	O	13	TFT common electrode	The power supply of common voltage in TFT driving. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. If not used, please open this pin.
CABC_PWM1	O	1	Backlight Circuit/MPU	CABC backlight control PWM signal output.
CABC_PWM2	O	1	Backlight Circuit	CABC backlight control PWM signal output.
CABC_ON	O	1	Backlight Circuit	LED Driver Enable Signal. If not used, please open this pin.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B C13A, C13B	I/O	11,11 10,10	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation (VSP).
C12A,C12B C14A,C14B	I/O	6,6 13,14	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation (VSN).
C22A,C22B	I/O	12,13	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation (VGH/VGL).

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	7	Power Supply	Digital IO Pad power supply.
VCI	P	22	Power Supply	Analog power supply.
VSSD	P	13	Ground	Digital ground.
VSSA	P	8	Ground	Analog ground.
VDDD	O	11	Stabilizing capacitor	For internal logic voltage. Connect to a stabilizing capacitor.
NVDDDOUT	O	10	Open	For internal logic voltage
VSPROUT	O	4	Open	Internal generated stable power for source driver unit.
VSNROUT	O	7	Open	Internal generated stable power for source driver unit.
VSP	O	9	Stabilizing capacitor	An output from the step-up circuit1. Connect a stabilizing capacitor between VSSA and VSP.
VSN	O	11	Stabilizing capacitor	An output from the step-up circuit3. Connect a stabilizing capacitor between VSSA and VSN.
VGH	O	8	Stabilizing capacitor	A positive power output from the step-up circuit 2 for the gate line drive circuit.
VGL	O	10	Schottkey barrier diode	A negative power output from the step-up circuit 2 for the gate line drive circuit. Connect a schottkey barrier diode between VSSA and VGL.
VCOMDC	O	3	Open	An output of VCOM level.

High speed interface parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
HSI_DP, HSI_DN	I/O	2/2	DSI Host	High speed interface data differential signal input/output pins. If not used, please open or connect it to VSSA
HSI_CP, HSI_CN	I	2/2	DSI Host	High speed interface CLOCK differential signal input pins. If not used, please open or connect it to VSSA
HSI_VSS	P	4	Ground	High speed interface analogy ground. HSI_VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
HSI_LDO	O	3	Capacitor	High speed interface regulator output pin. Connect to a stabilizing capacitor between HSI_VSS and HSI_LDO If not used, please open these pins.

Test pin and others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST1	I	1	Open	Test pin input (Internal pull low). If not used, please open or connect it to VSSA
TEST2	I	1	Open	Test pin input (Internal pull low). If not used, please open or connect it to VSSA
TEST3	I	1	Open	Test pin input (Internal pull low). If not used, please open or connect it to VSSA
OSC	I	1	Open	A test pin. Please let it open
TESTDP	O	1	Open	A test pin. Please let it open
VTEST	O	1	Open	A test pin. Please let it open
NVTEST	O	1	Open	Gamma voltage of Panel test pin output. Must be left open.
DUMMY1~30 DUMMY31~69	-	69	Open	Dummy pads. Please let it open Dummy1 can be used as COG bonding resistance measurement
DUMMY_VCL	-	9	Open	Dummy pads. Please let it open

3.3Pin assignment

TBD

4. Interface

The HX8357-D supports MIPI interfaces: DBI (Display Bus Interface), DPI (Display Pixel Interface), DSI (Display Serial Interface). Where DBI supports (24-/18-/16-/9-/8-bit interface) Parallel Interface (Type B) and Serial interface (Type C Option 1/ Option 3). The interface mode can be selected by IM2-0 pins setting as show in Table 4.1.

IM2	IM1	IM0	Interface	WRX_SCL	Data Bus use	
					Command/ Parament	GRAM
0	0	0	DBI TYPE-B 18-bit (DB_EN='0')	WRX	DB7-DB0	DB17-DB0: 18-bits Data
0	0	0	DBI TYPE-B 24-bit(DB_EN='1')	WRX	DB7-DB0	DB23-DB0: 24-bits Data
0	0	1	DBI TYPE-B 9-bit	WRX	DB7-DB0	DB8-DB0: 9-bits Data
0	1	0	DBI TYPE-B 16-bit	WRX	DB7-DB0	DB15-DB0: 16-bits Data
0	1	1	DBI TYPE-B 8-bit	WRX	DB7-DB0	DB7-DB0: 8-bit Data
1	0	0	Not use	-	-	
1	0	1	DBI TYPE-C Option 1	SCL	SDA	
1	1	0	MIPI DSI (For HX8357-D01 only)	-	HSI_CP/N , HSI_D0P/N	
1	1	1	DBI TYPE-C Option 3	SCL	SDA	

Table 4.1: Interface selection

The HX8357-D includes an index register (IR), which is stored the index data of internal control register and GRAM. When DCX="L", the command via DBI interface write into register. When DCX="H", GRAM data via R2Ch register can be written through data bus. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM.

When data is read from the GRAM to the MPU, it is first read from GRAM to the read-data latch and then data is read to MPU through the read-data latch in next read operation. Therefore, the read data in data bus in first read operation is invalid, and the read data is valid from second read in data bus.

4.1MIPI DBI-B interface

The selection of DBI interface IM2~IM0 pin to select DBI interface mode. The parallel interface timing diagram is described in Figure 4.1 and Figure 4.2.

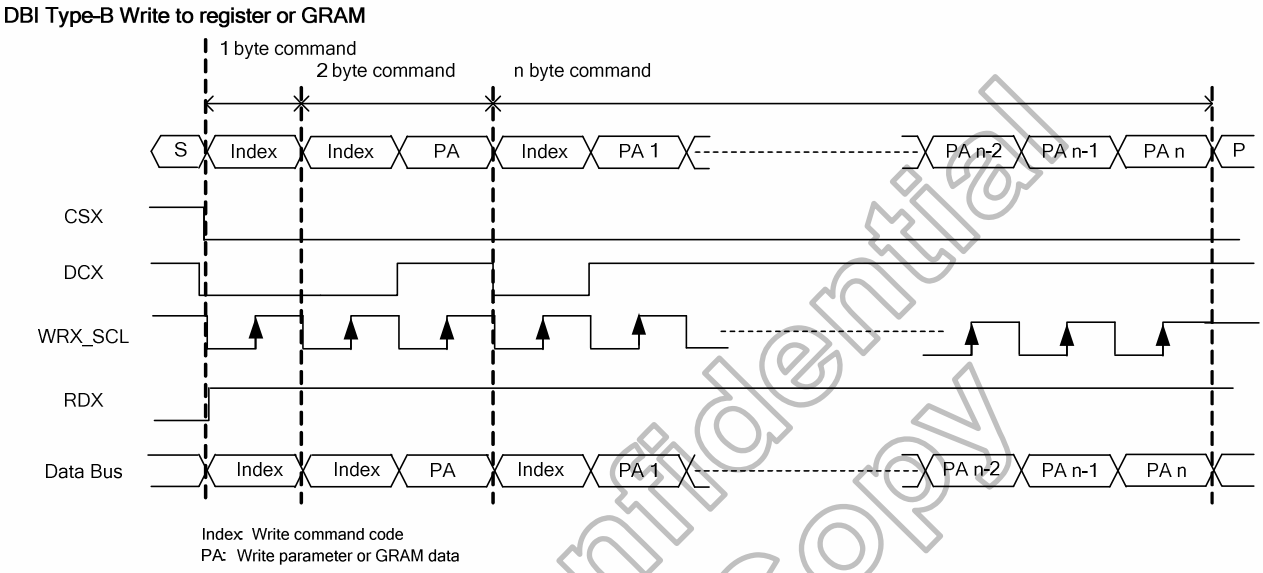


Figure 4.1: DBI-B system interface protocol, write to register or GRAM

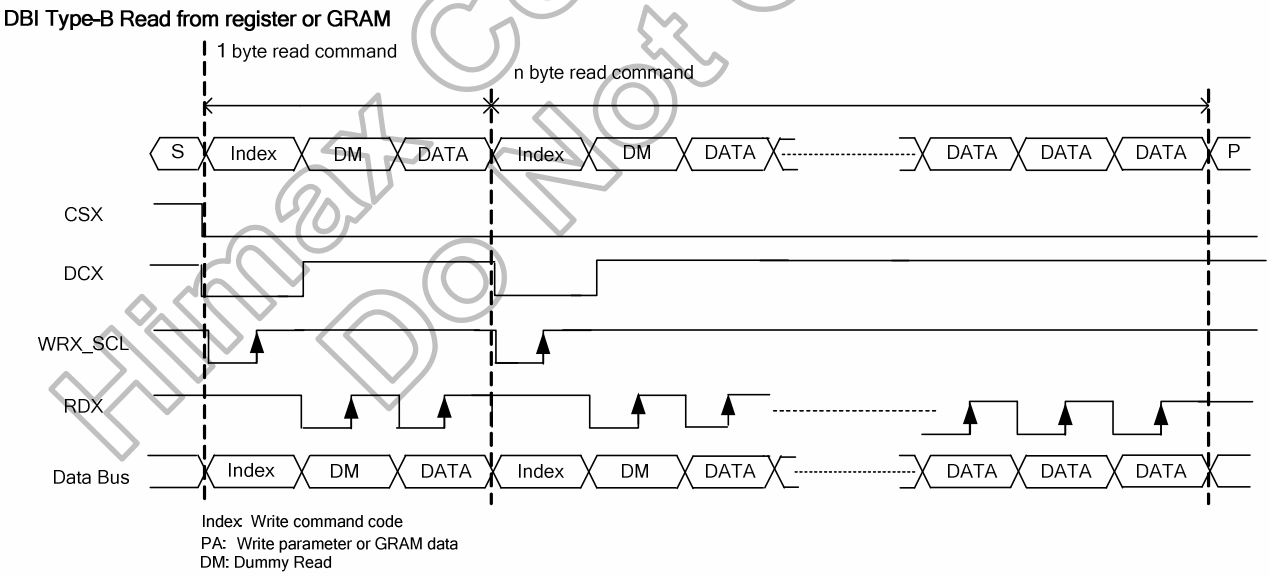


Figure 4.2: DBI-B system interface protocol, read from register or GRAM

DBI TYPE-B 8-bit Parallel Bus System Interface

The DBI-B system 8-bit bus parallel data transfer can be used by setting “IM2-0” pins to “011”. The Figure4.3 is the example of interface with 8-bit DBI-B microcomputer system interface.

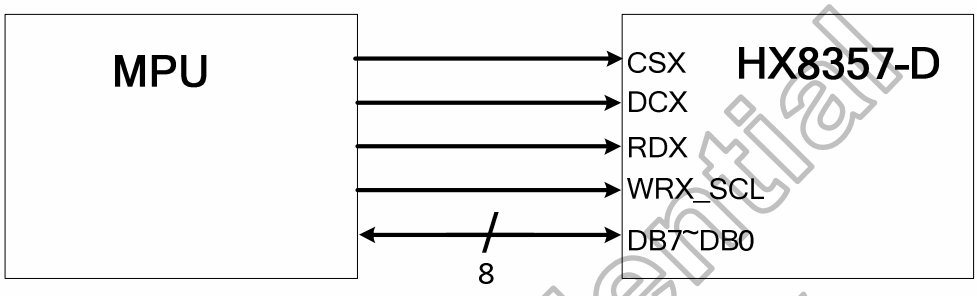


Figure 4.3: Example of DBI-B System 8-bit bus Interface

8-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 3AH=”05h”
There is 1-pixel (3 sub-pixels) per 2-bytes.

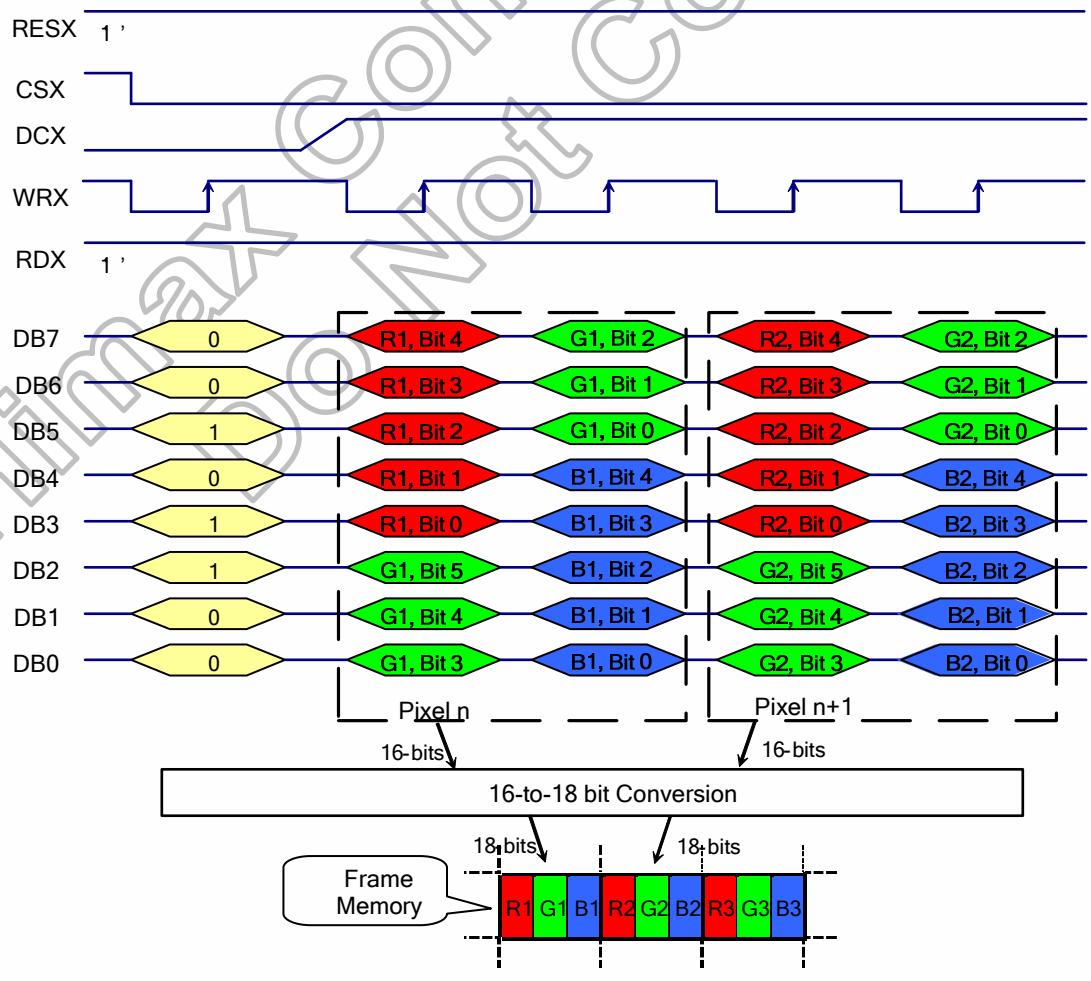


Figure 4.4: Write data for RGB 5-6-5 (65k colors) bits input in 8-bit parallel interface

8-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (3 sub-pixels) per 3-bytes.

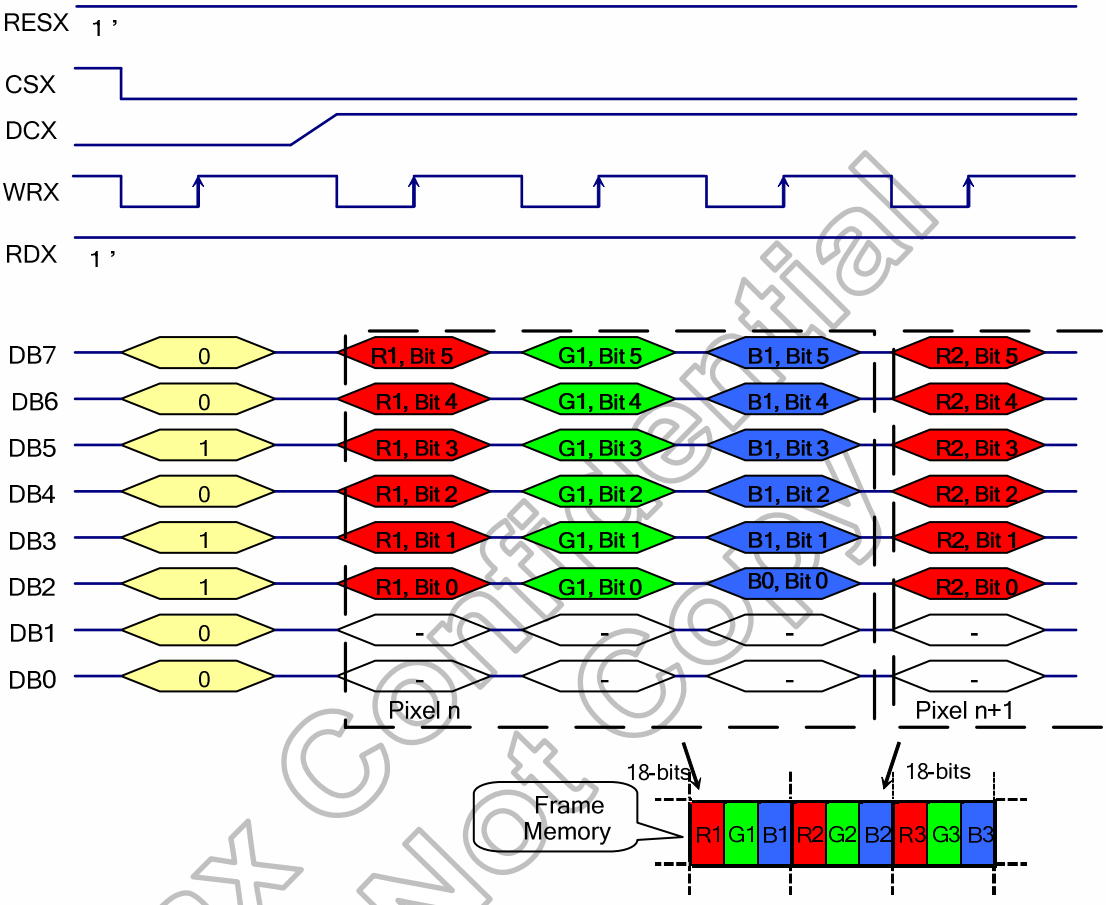


Figure 4.5: Write data for RGB 6-6-6-bits(262k colors) input in 8-bit parallel interface

8-bits data bus for 24-bits/pixel (RGB 8-8-8-bits input), 16M-colors, 3AH="07h"
There is 1-pixel (3 sub-pixels) per 3-bytes.

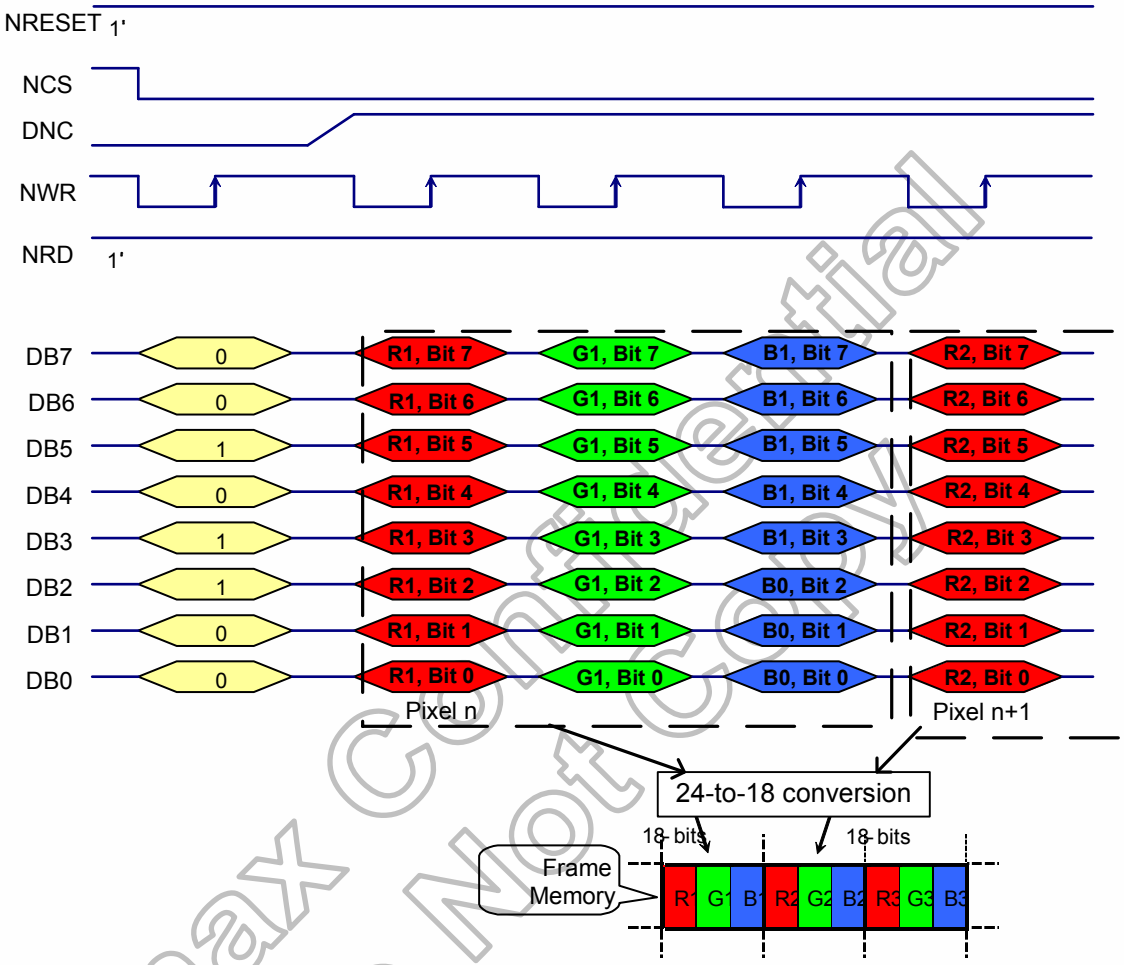


Figure 4.6: Write data for RGB 8-8-8-bits(16M colors) input in 8-bit parallel interface

DBI TYPE-B 9-bit Parallel Bus System Interface

The DBI-B system 9-bit bus parallel data transfer can be used by setting “IM2-0” pins to “001”. The Figure4.7 is the example of interface with 9-bit DBI-B microcomputer system interface.

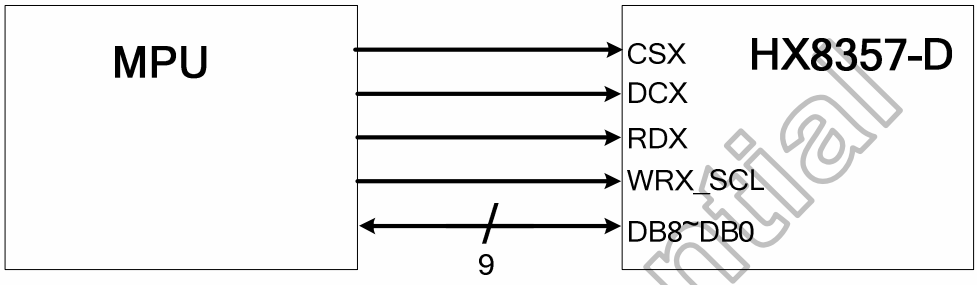


Figure 4.7: Example of DBI-B system 9-bit bus interface

9-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 3AH=”05h”
There is 1-pixel (3 sub-pixels) per 2-bytes.

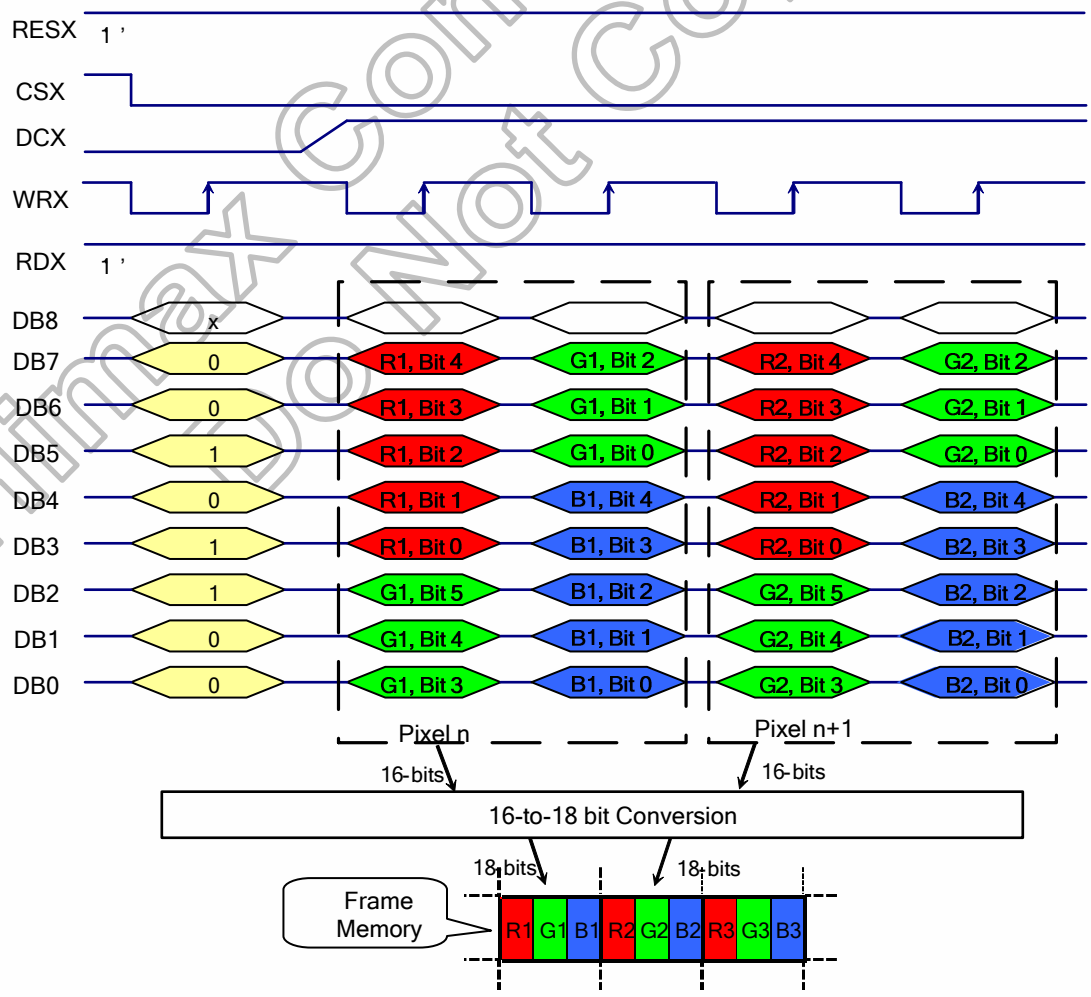


Figure 4.8: Write data for RGB 5-6-5 (65k colors) bits input in 9-bit parallel interface

9-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (3 sub-pixels) per 2-bytes

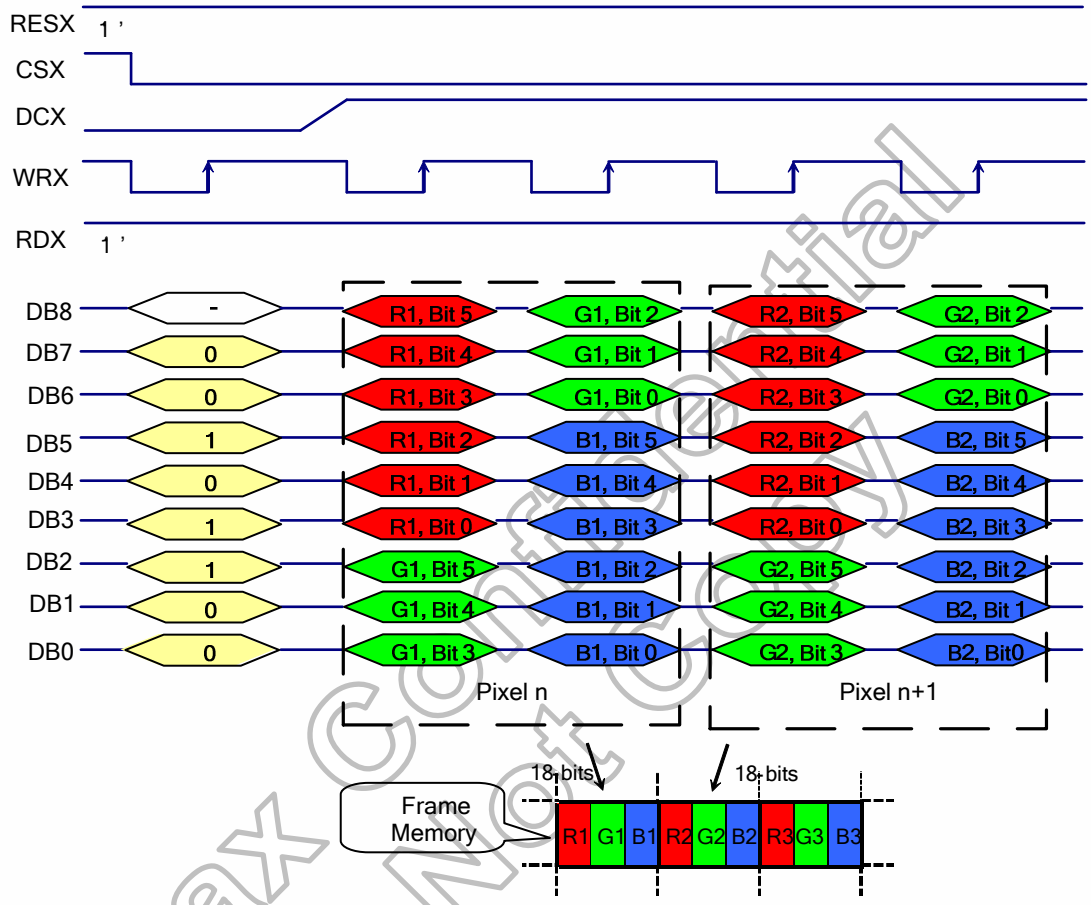


Figure 4.9: Write data for RGB 6-6-6 (262k colors) bits input in 9-bit parallel interface

DBI TYPE-B 16-bit Parallel Bus System Interface

The DBI-B system 16-bit bus parallel data transfer can be used by setting “IM2-0”pins to “010”. The Figure4.10 is the example of interface with 16-bit DBI-B microcomputer system interface.

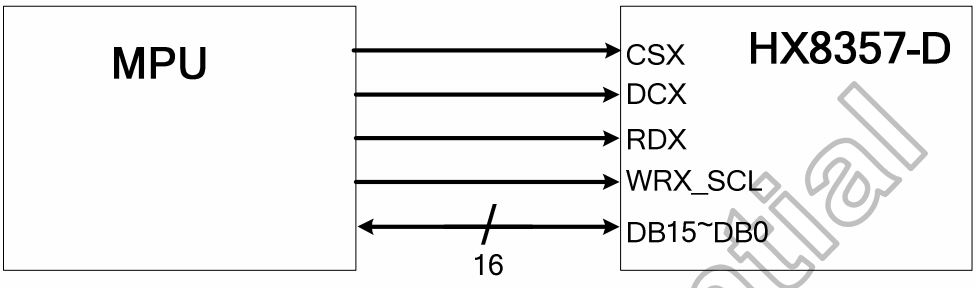


Figure 4.10: Example of DBI-B System 16-bit bus interface

16-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 3AH="05h"
There is 1-pixel (3 sub-pixels) per 1-byte

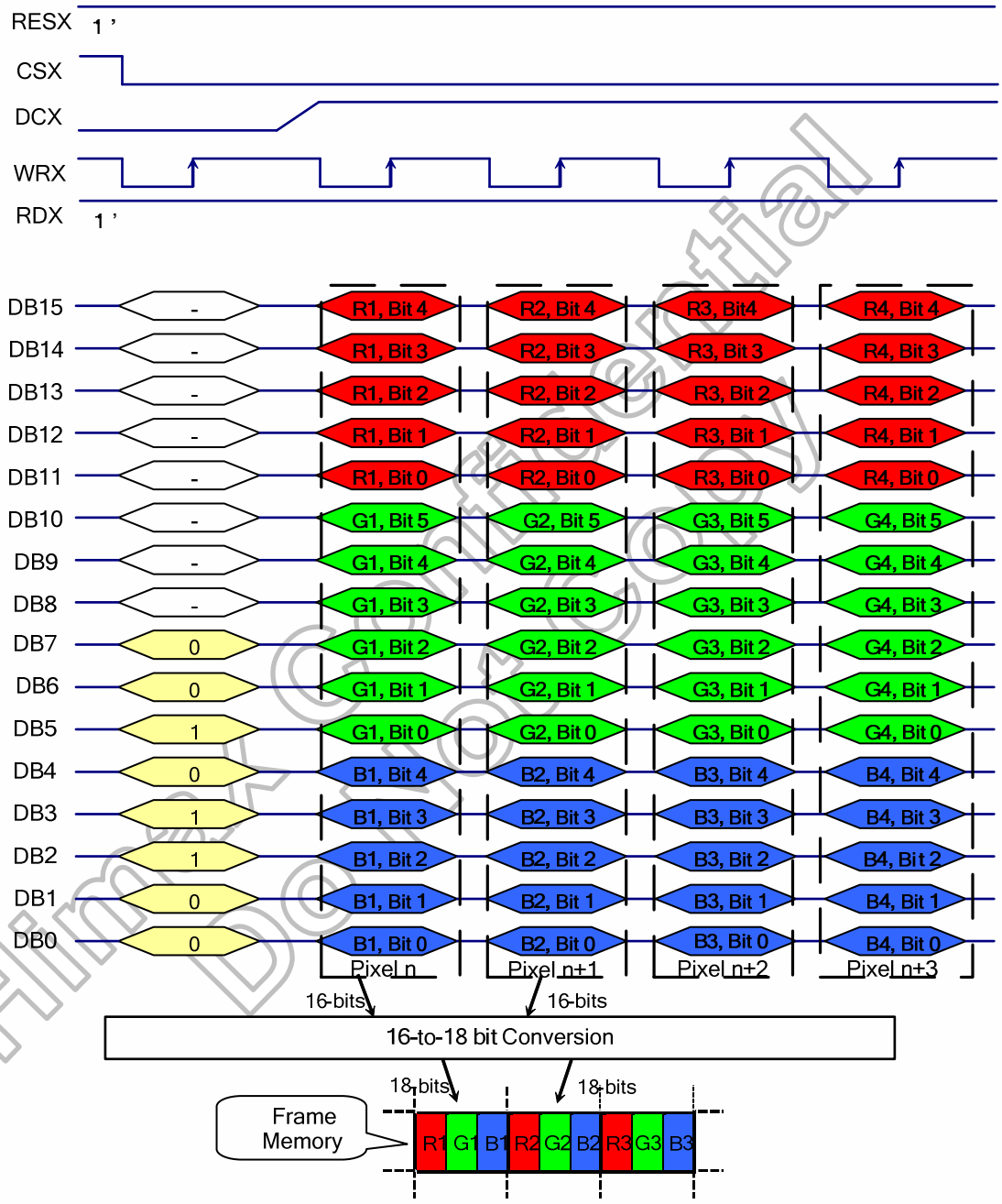


Figure 4.11: Write data for RGB 5-6-5 (65k colors) bits input in 16-bit parallel interface

16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There are 2-pixels (6 sub-pixels) per 3-bytes

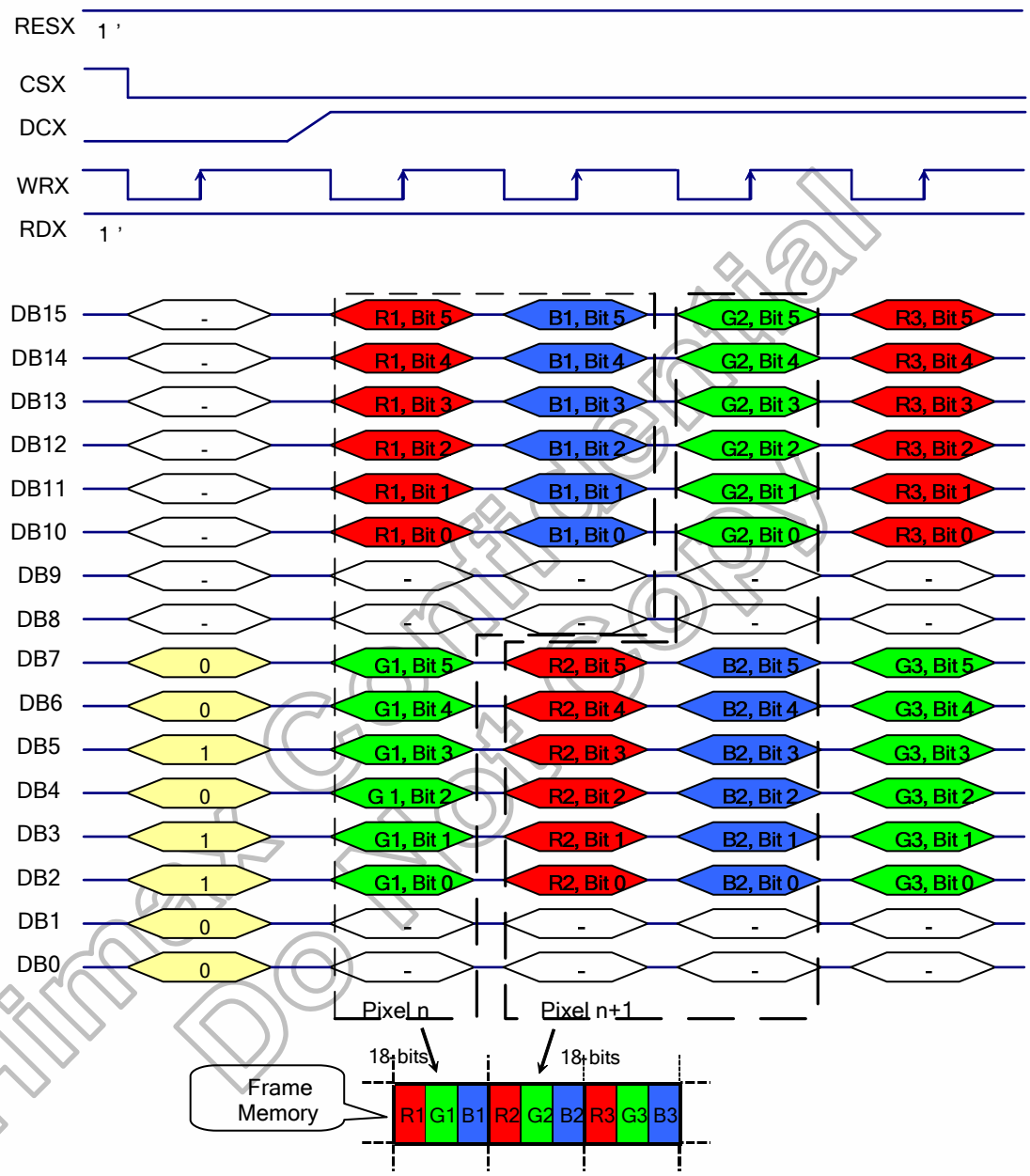


Figure 4.12: Write data for RGB 6-6-6 (262k colors) bits input in 16-bit parallel interface

16-bits data bus for 18-bits/pixel (RGB 8-8-8-bits input), 16M-colors, 3AH="07h"
There are 2-pixels (6 sub-pixels) per 3-bytes

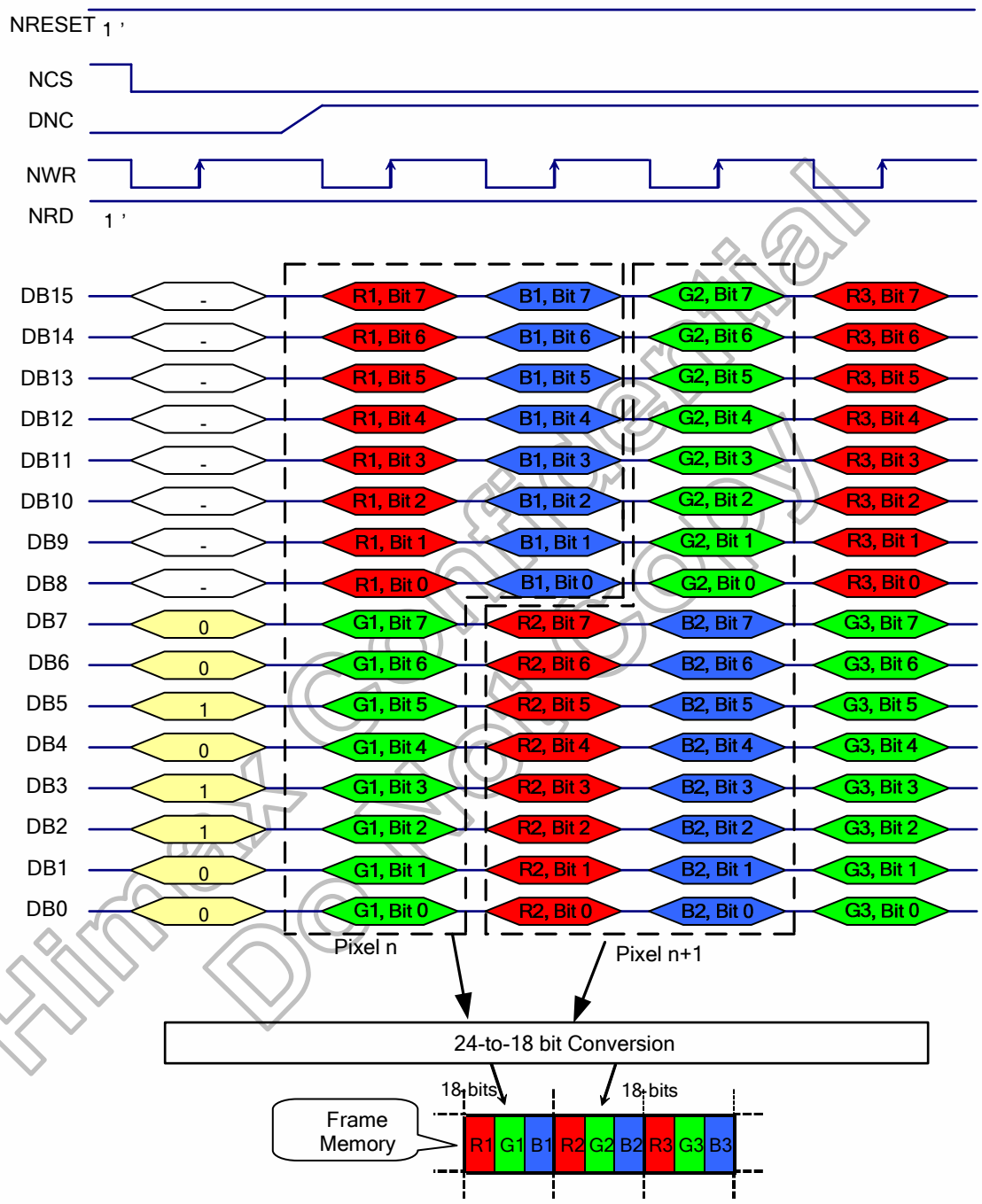


Figure 4.13: Write data for RGB 8-8-8 (16M colors) bits input in 16-bit parallel interface

DBI TYPE-B 18-bit Parallel Bus System Interface

The DBI-B system 18-bit bus parallel data transfer can be used by setting “IM2-0”pins to “000” and register setting DB_EN=’0’. The Figure 4.14 is the example of interface with 18-bit DBI-B microcomputer system interface.

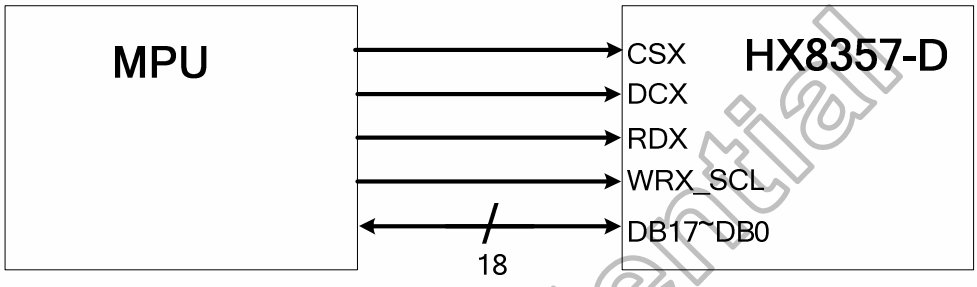


Figure 4.14: Example of DBI-B system 18-bit parallel bus interface

18-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 3AH="06h"
There is 1-pixel (6 sub-pixels) per 1-byte

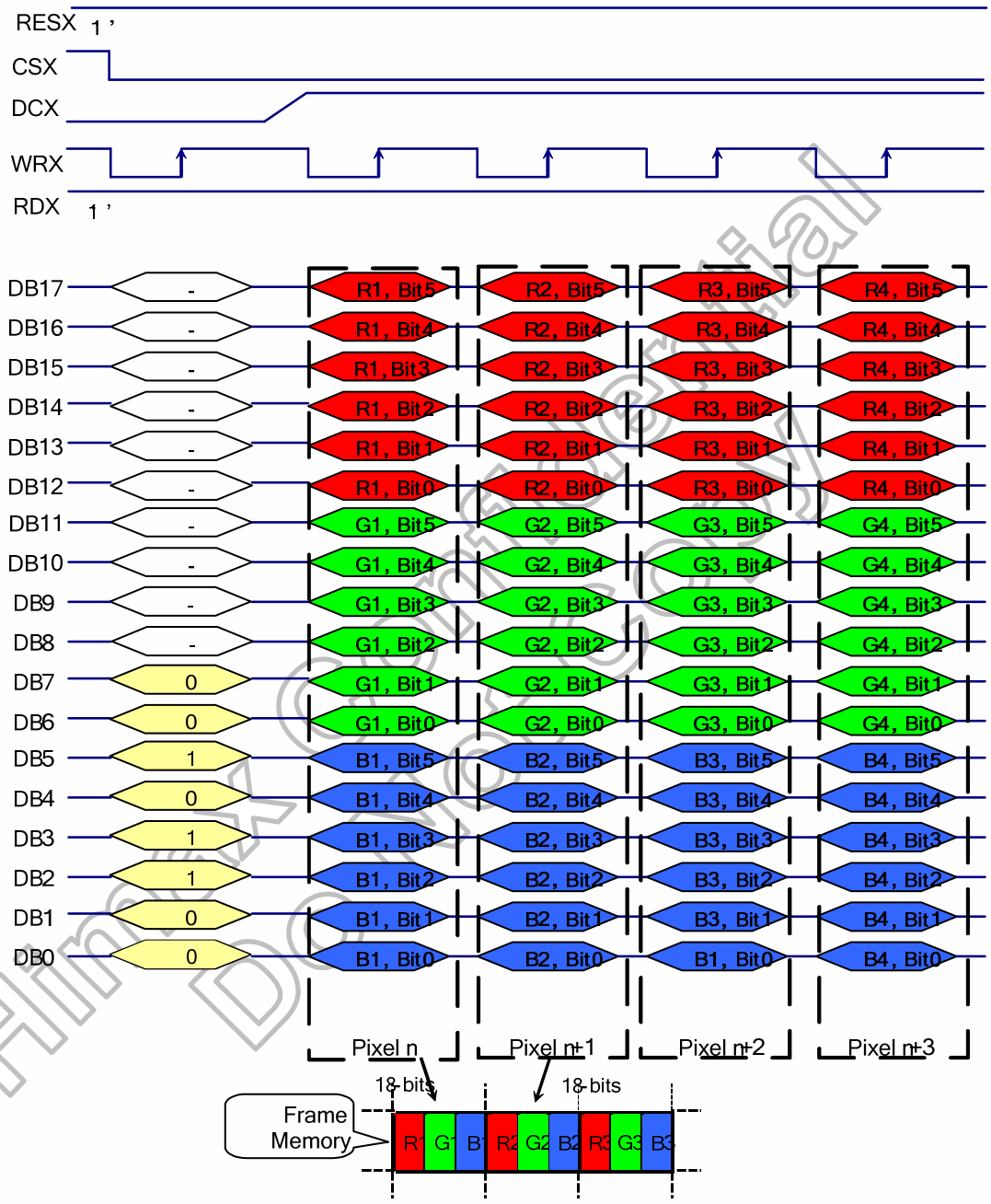


Figure 4.15 Write data for RGB 6-6-6 (262k colors) bits input in 18-bit parallel interface

DBI TYPE-B 24-bit Parallel Bus System Interface

The DBI-B system 24-bit bus parallel data transfer can be used by setting “IM2-0”pins to “000” and register setting DB_EN=’1’. The Figure 4.16 is the example of interface with 24-bit DBI-B microcomputer system interface.

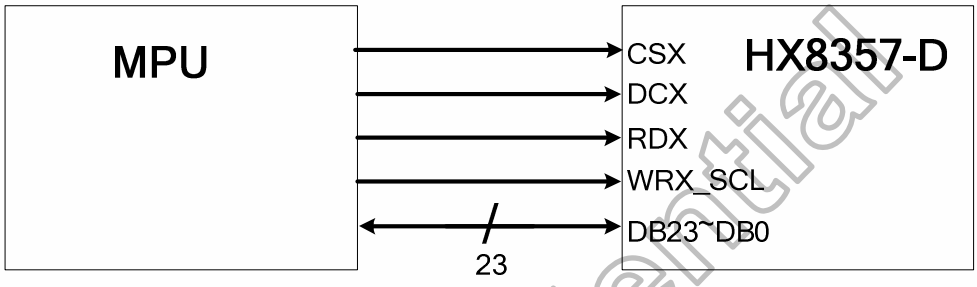


Figure 4.16: Example of DBI-B system 24-bit parallel bus interface

24-bits data bus for 24-bits/pixel (RGB 8-8-8-bits input), 16M-colors, 3AH="07h"
There is 1-pixel (8 sub-pixels) per 1-byte

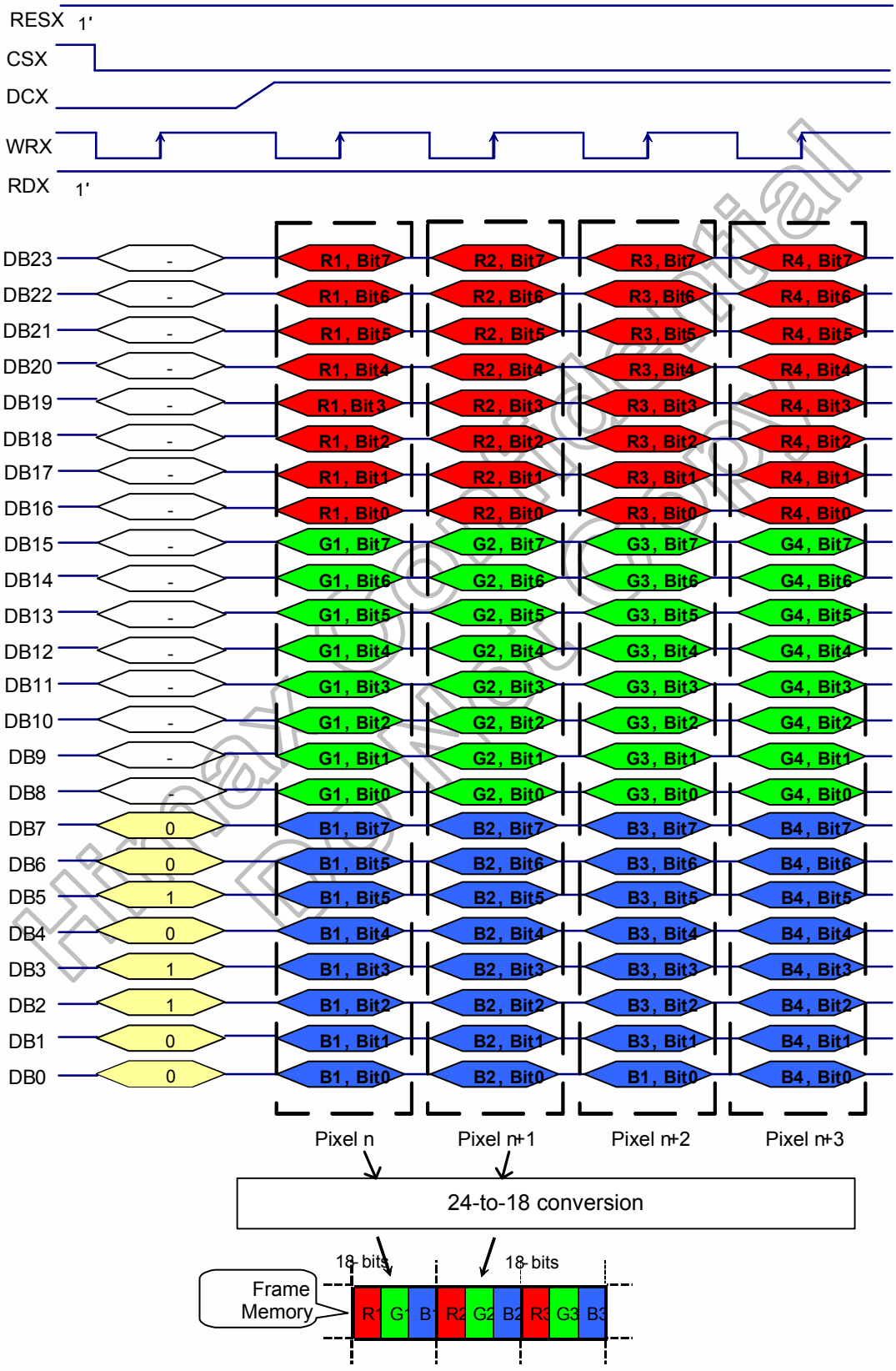


Figure 4.17 Write data for RGB 8-8-8 (16M colors) bits input in 24-bit parallel interface

Parallel Interface Data Color Coding

Data Color Coding for GRAM data ***Write***

- Parallel 8-Bits Bus Interface (IM2,IM1,IM0="011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
05h	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-bytes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	
07h	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	16M-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	
	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	

Table 4.2: 8-bit interface GRAM write table

- Parallel 9-Bits Bus Interface (IM2,IM1,IM0="001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
05h	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-bytes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4.3: 9-bit interface GRAM write table

- Parallel 16-Bits Bus Interface (IM2,IM1,IM0="010")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
06h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
07h	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16M-Color (2-pixels/ 3bytes)
	x	x	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0	
	x	x	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	

Table 4.4: 16-bit interface GRAM write table

- Parallel 18-Bits Bus Interface (IM2,IM1,IM0="000"and DB_EN='0')

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 4.5: 18-bit interface GRAM write table

- Parallel 24-Bits Bus Interface (IM2,IM1,IM0="000" and DB_EN='1')

Register Command	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2Ch**
3Ah	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
07h	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	16M-Color

Table 4.6: 24-bit interface GRAM write table

Data Color Coding for RAM data ***Read***

- Parallel 8-Bits Bus Interface (IM2,IM1,IM0="011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4.7: 8-bit parallel interface GRAM read table

- Parallel 16-Bits Bus Interface (IM2,IM1,IM0="010")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4.8: 16-bit parallel interface GRAM read table

- Parallel 9-Bits Bus Interface (IM2,IM1,IM0="001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4.9: 9-bit parallel interface GRAM read table

- Parallel 18-Bits Bus Interface (IM2,IM1,IM0="000" and DB_EN='0')

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 4.10: 18-bit parallel interface GRAM read table

- Parallel 24-Bits Bus Interface (IM2,IM1,IM0="000" and DB_EN='1')

Register Command	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2Eh**
Read Data Format	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R7	R6	R5	R4	R3	R2			G7	G6	G5	G4	G3	G2			B7	B6	B5	B4	B3	B2			262K-Color

Table 4.11: 24-bit parallel interface GRAM read table

4.2Serial data transfer interface (MIPI DBI TYPE-C)

The HX8357-D00/D01 supports DBI Type C option 1(3-wire) and option 3(4-wire) serial data transfer interface, the interface selection by setting IM2-0 pins, The IM2-0 set “101” is select option1 3 wire serial bus. The IM2-0 set “111” is select option3 4 wire serial bus.

The 3 wire serial bus is use: chip select line (CSX), serial input/output data (SDA) and the serial transfer clock line (WRX_SCL).

The 4 wire serial bus is use: chip select line (CSX), data/command select (DCX), serial input/output data (SDA/SDO) and the serial transfer clock line (WRX_SCL).

4.2.1 Serial data write mode

The 3-Pin serial data packet contains a control bit D/CX and a transmission byte If D/CX is low, the transmission byte is command byte. If D/CX is high, the transmission byte is stored in to command register or GRAM. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (SDA/SDO) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

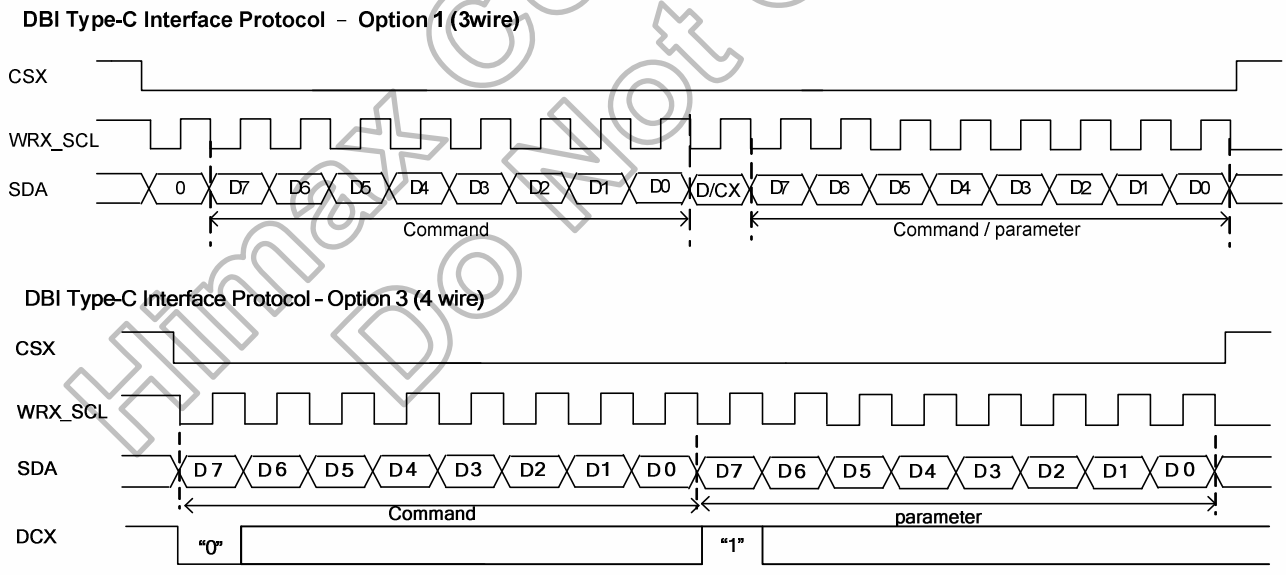


Figure 4.18: DBI type C – serial interface protocol 3 wire/ 4 wire, write mode

4.2.2 Read operation in serial peripheral interface

In serial peripheral interface read operation, the host controller first has to send a command and then the following byte is transmitted to host controller in the SDA. The read mode has two type command data read (8-/Over 8-bit) and one type GRAM data read.

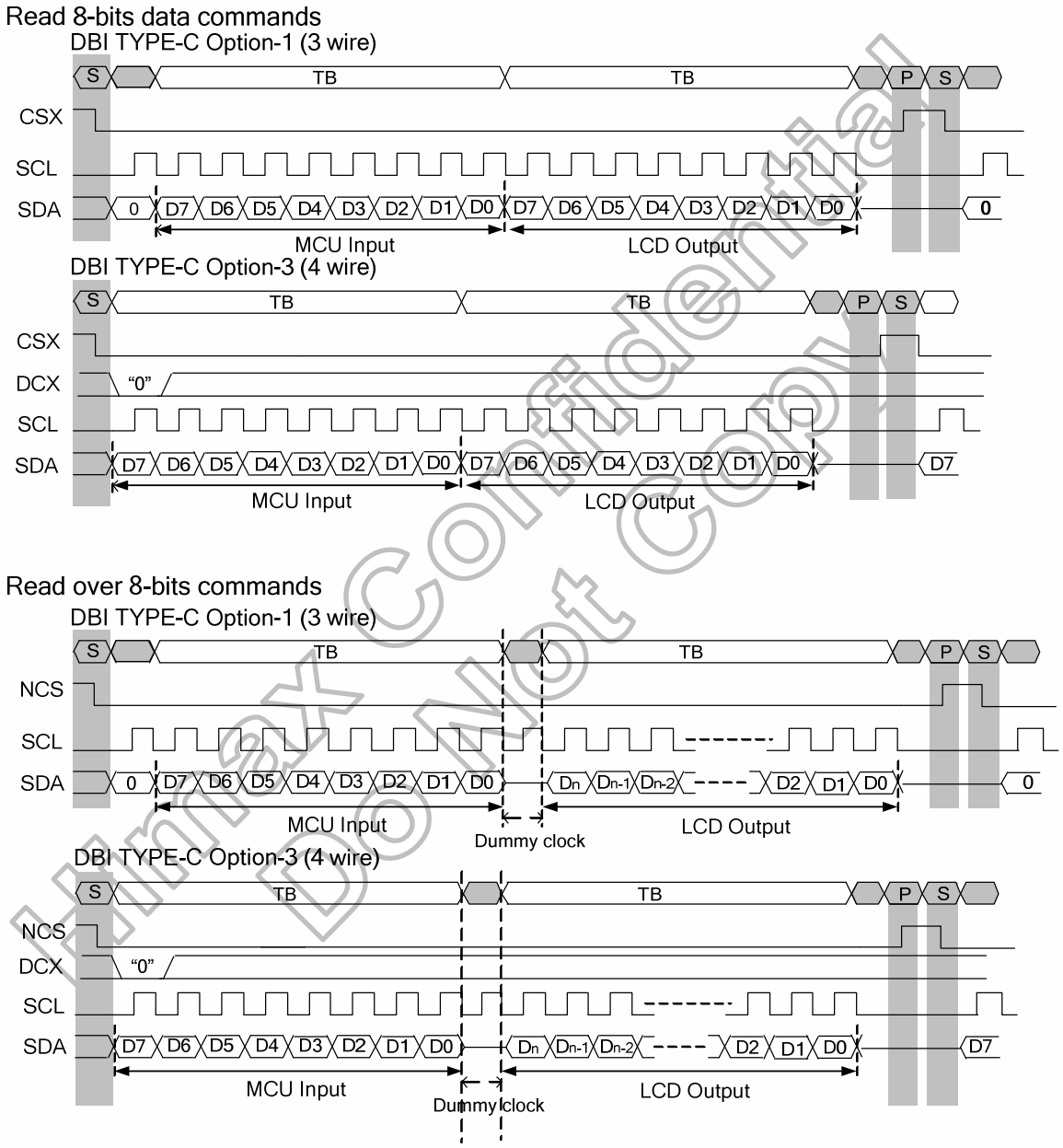


Figure 4.19: Command read operation in serial peripheral interface

4.2.3 DBI TYPE-C interface data color coding

There are two types data format to write display data at Serial data bus Interface and it is as same as 8-bit bus Interface.

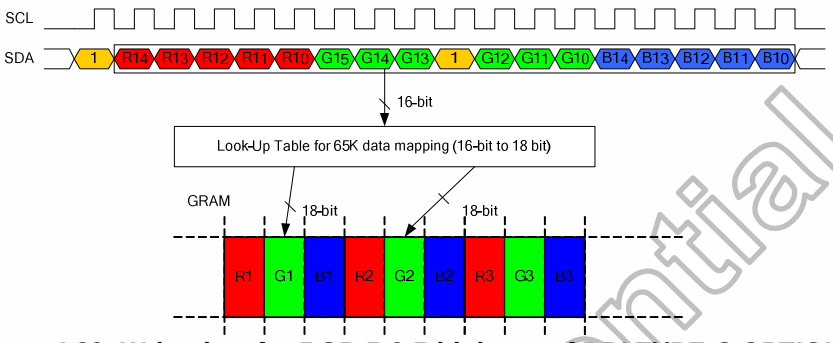


Figure 4.20: Write data for RGB 5-6-5-bit input of DBI TYPE-C OPTION 1

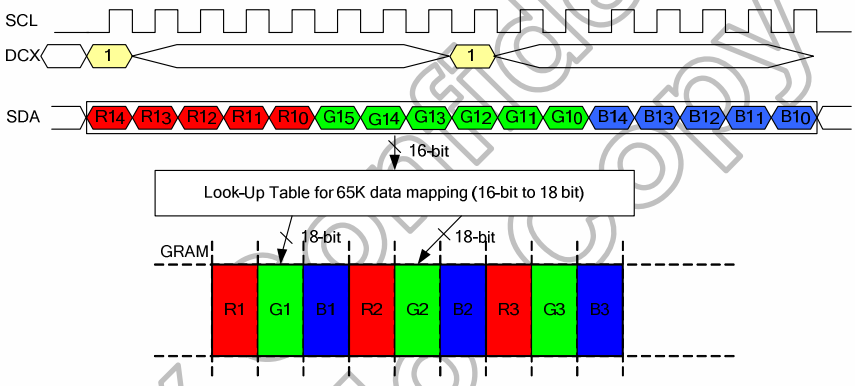


Figure 4.21: Write data for RGB 5-6-5-bit input of DBI TYPE-C OPTION 3

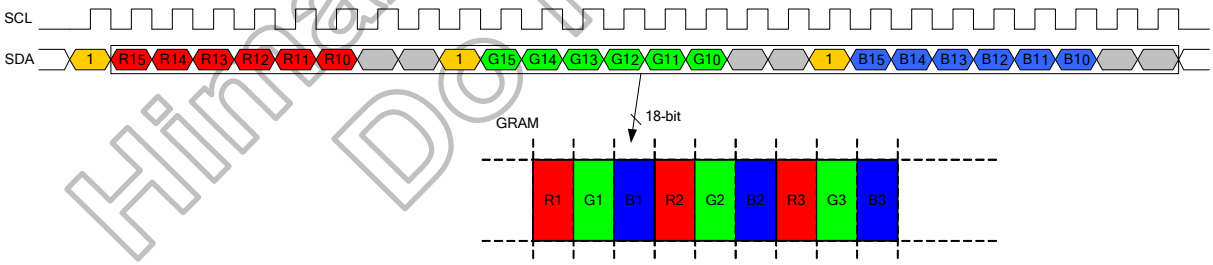


Figure 4.22: Write data for RGB 6-6-6-bit input of DBI TYPE-C OPTION 1

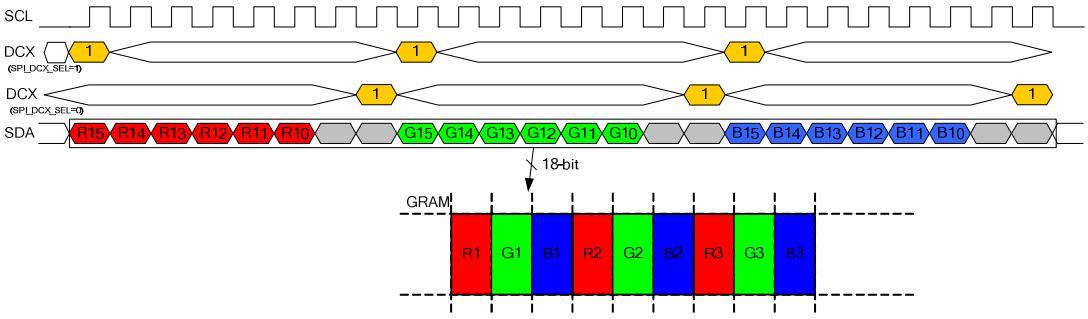


Figure 4.23: Write data for RGB 6-6-6-bit input of DBI TYPE-C OPTION 3

Register Command	D7	D6	D5	D4	D3	D2	D1	D0	Command
3Ah	0	0	1	0	1	1	0	0	**2CH**
05h	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-transfer)
	G2	G1	G0	B4	B3	B2	B1	B0	
06h	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3-transfer)
	G5	G4	G3	G2	G1	G0	x	x	
	B5	B4	B3	B2	B1	B0	x	x	

Table 4.12: DBI TYPE-C interface GRAM write table

4.2.4 Break and pause sequences

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

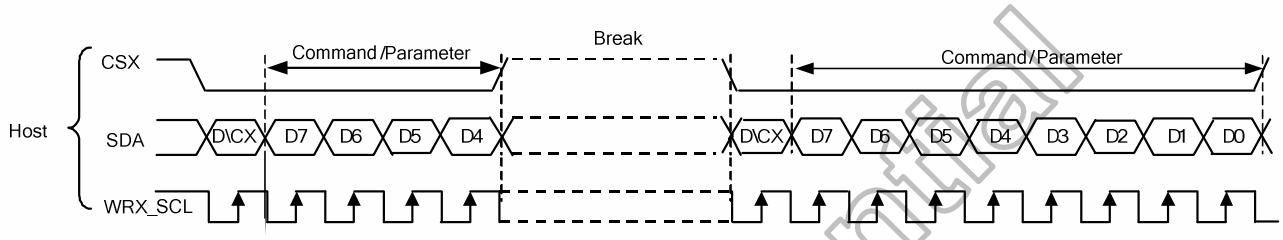


Figure 4.24: Display module data transfer recovery

If a one or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

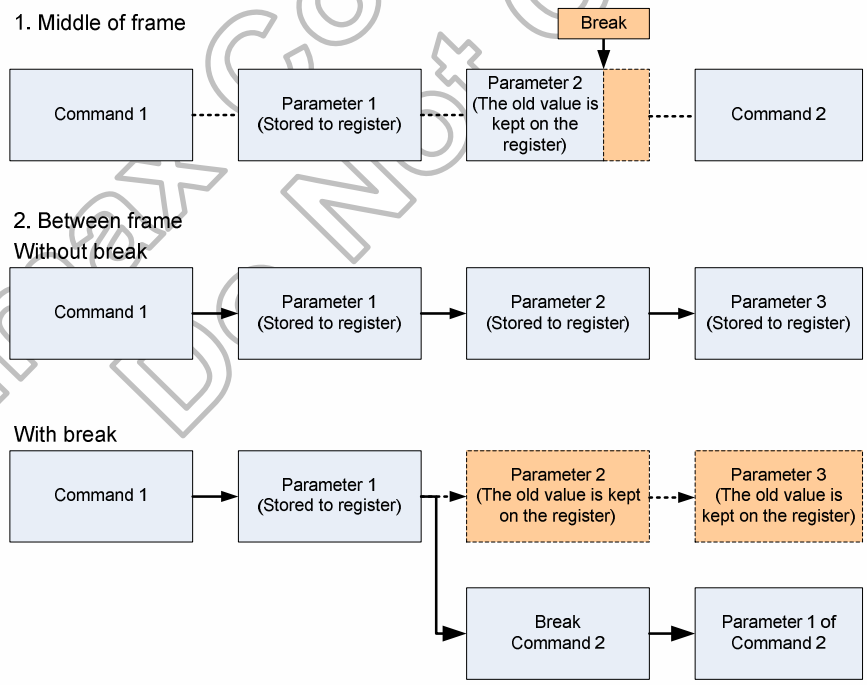


Figure 4.25: Break during parameter

The host processor can pause a write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the write sequence at the point where the sequence was paused.

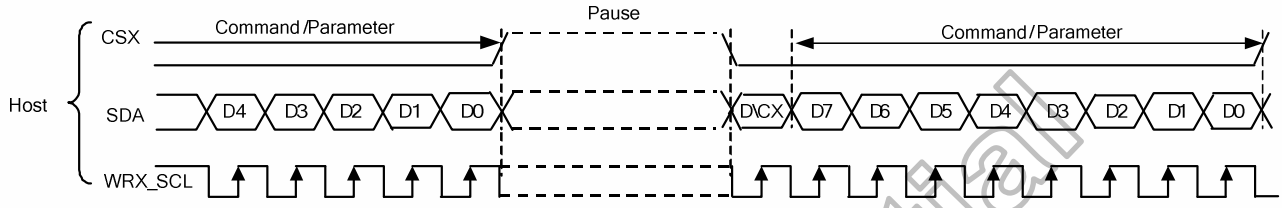


Figure 4.26: Display module data transfer pause

There are 4 cases where there is possible to see this kind of pause:

1. Command – Pause – Command
2. Command – Pause – Parameter
3. Parameter – Pause – Command
4. Parameter – Pause – Parameter

4.3MIPI DPI interface (display pixel interface)

The HX8357-D00/D01 uses 16, 18, 24-bit parallel DPI interface which includes: HSYNC, VSYNC, DE, PCLK, DB23~DB0. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HSYNC, VSYNC, DE and DB17~DB0 –lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In –mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative (‘-‘, ‘0’, low) active and its state is read to the display module by a rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is negative (‘-‘, ‘0’, low) active and its state is read to the display module by a rising edge of the PCLK-line. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is positive (‘+’, ‘1’, high) active and its state is read to the display module by a rising edge of the PCLK-line. DB pin 24 bit: DB23-DB16(R7-R0), DB15-DB8(G7-G0) and DB7-DB0(B7-B0);18 bit: DB17-DB12(R5-R0), DB11-DB6(G5-G0) and DB5-DB0(B5-B0); 16 bit: DB17-DB13(R4-R0), DB11-DB6(G5-G0) and DB5-DB1(B4-B0); are used to tell what is the information of the image that is transferred on the display (when DE =1 and there is a rising edge of PCLK). DB17~DB0 – lines can be set to “0” (low) or “1” (high). These lines are read by a rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.

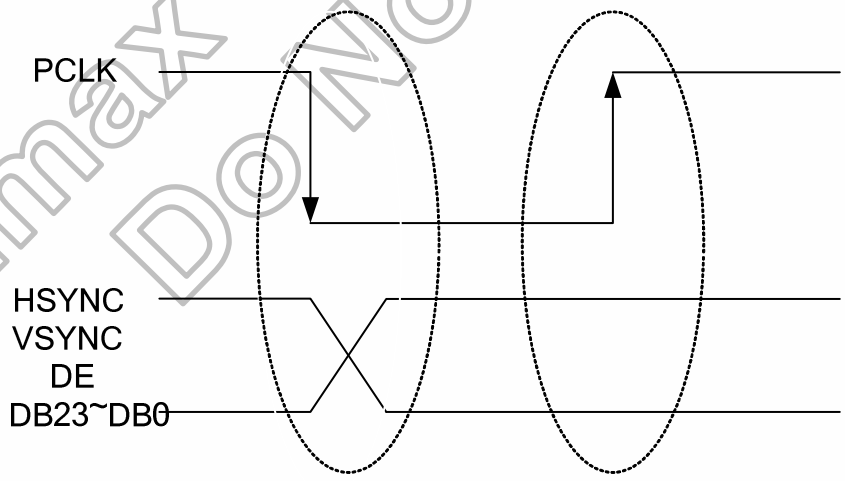


Figure 4.27: PCLK cycle

General timing diagram

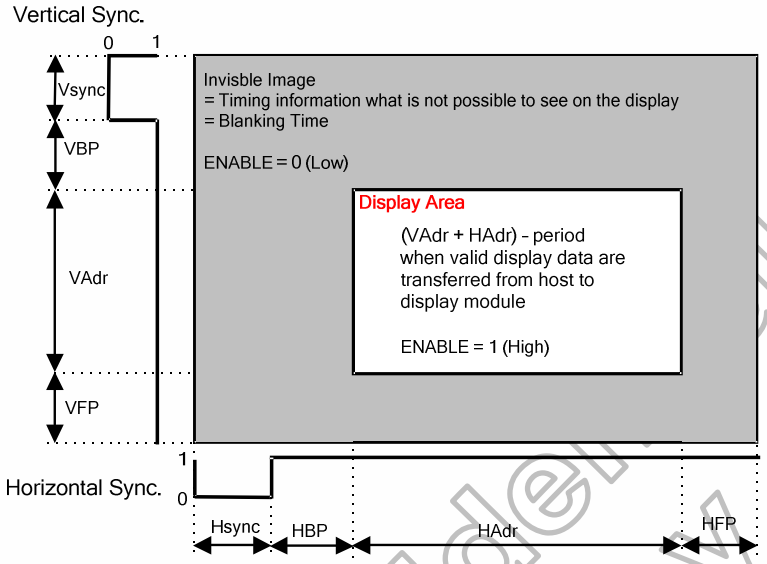


Figure 4.28: General timing diagram

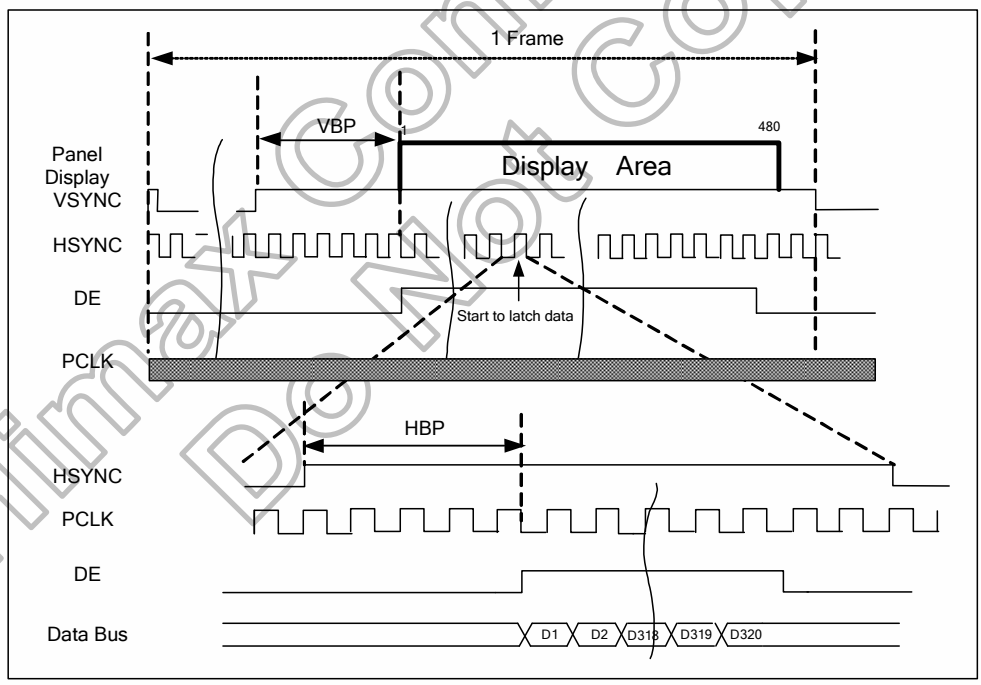


Figure 4.29: DPI timing diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

DPI interface data color coding

The MIPI DPI interface includes three types which are 16-/ 18-bit data format by register 3Ah (set_pixel_format) to select.

Register 3Ah	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DPI Interface mode
50h	R4	R3	R2	R1	R0		G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0		16-bit 65K-Color
60h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit 262K-Color

Table 4.13: 16-/18- DPI color mapping

Register 3Ah	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DPI Interface mode
70h	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bit 16M-Color

Table 4.14: 24-DPI color mapping

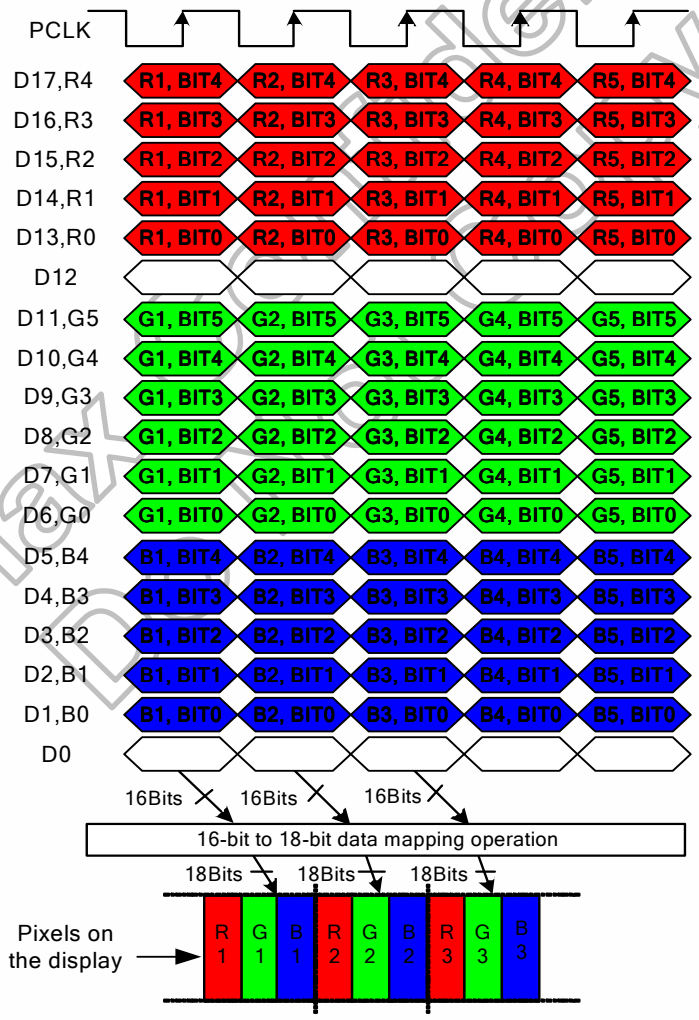


Figure 4.30: 16-bit data bus color order on DPI interface

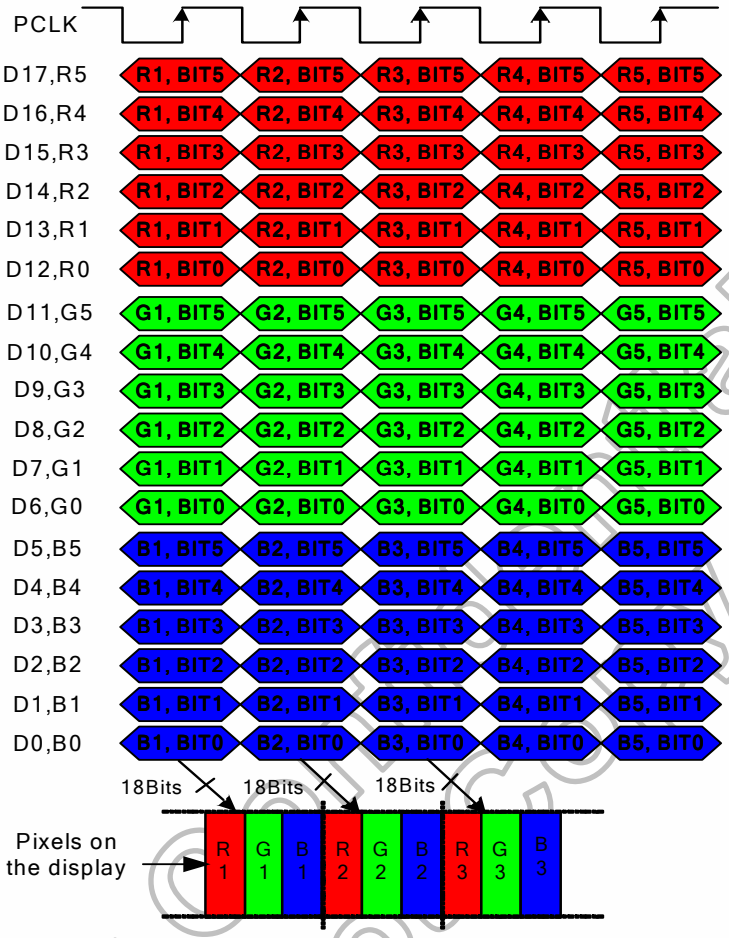


Figure 4.31: 18-bit data bus color order on DPI interface

DPI interface displaying moving pictures can be selected to by register **DM** and **RM.**

RM The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation.

RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting.

RM	Interface for RAM access
0	DBI Interface (MPU)
1	DPI Interface (RGB)

DM bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DPI signal.

DM	Display Mode
0	Internal oscillation clock
1	DPI interface

Operation Mode	Frame Memory Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	MPU interface (RM=0)	Internal clock operation (DM=0)
DPI interface (displaying moving pictures)	DPI interface (RM=1)	DPI interface (DM=1)

4.4 DSI system interface (For HX8357-D01 only)

The selection of interface is by IM(2-0) =”110 “, the DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.30 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that. DSI-compliant peripherals support Command Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display.

Command Mode refers to operation in which transactions primarily take the form of sending Commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

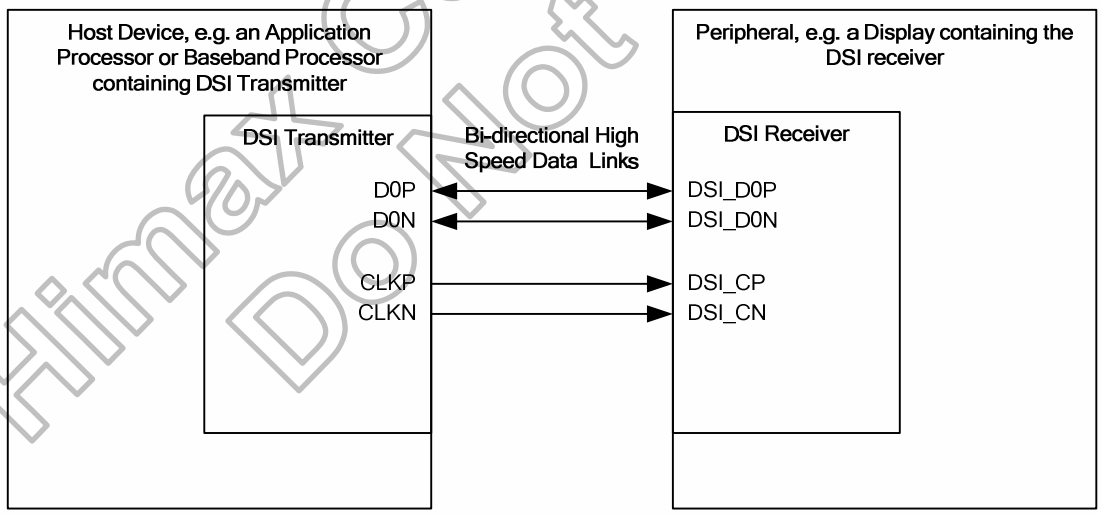


Figure 4.32: DSI transmitter and receiver interface

Please refer to “**MIPI Alliance Standard for DSI”** for DSI detailed specifications.

4.4.1 DSI layer definitions

According Figure 4.31 DSI transmitter and Receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four types: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.

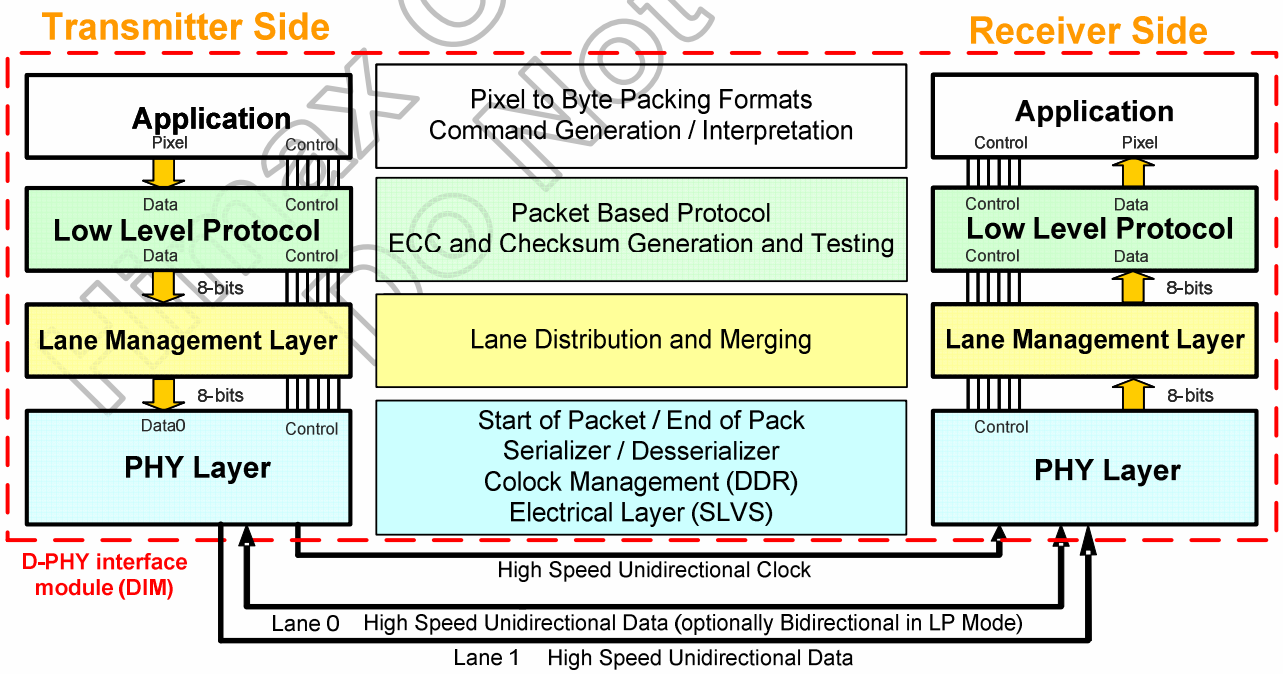
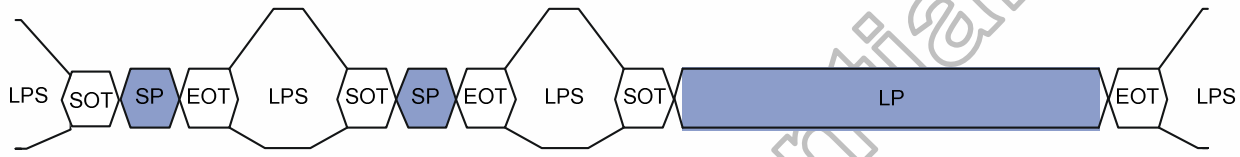


Figure 4.33: Transmitter and receiver interface

4.4.2 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 4.34 illustrates multiple HS Transmission packets.

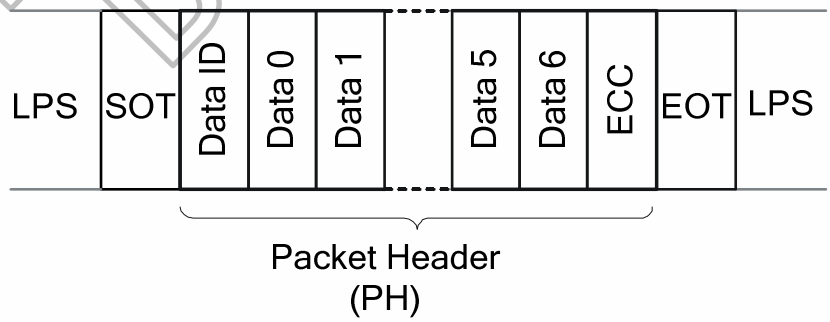


LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

Figure 4.34: DSI multiple HS transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Short packets specify the payload length using the Data Type field and are from two to nine bytes in length. Short packet is used for most Command Mode commands and associated parameters. Where short packets format include an 8-bit Data ID followed by zero to seven bytes and an 8-bit ECC. Figure 4.33 shows the structure of the Short packet.

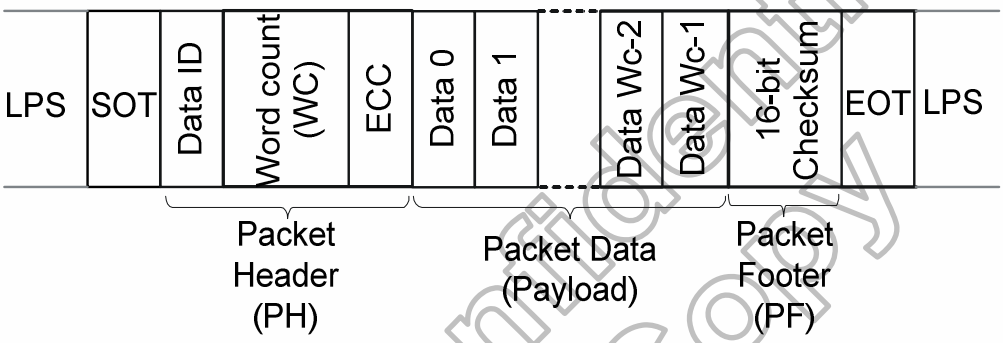


DI(Data ID): Contain Virtual Channel Identifier and Data Type.
ECC(Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 4.35: Structure of the short packet

Long packets specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.. Figure 4.43 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where 65,541 bytes = (216-1) + 4 bytes PH + 2 bytes PF



DI (Data ID)：Contain Virtual Channel Identifier and Data Type.
WC (Word Count)：The receiver use WC to define packet end.
ECC (Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF(Packet Footer)：Mean 16-bit Checksum.

Figure 4.36: Structure of the long packet

According to packet form, basic elements include DI and ECC. Figure 4.44 the shows format of Data ID.

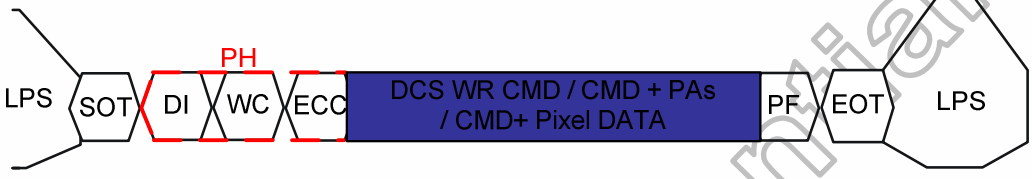
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

DI[7:6] ➔ These two bits identify the data as directed to one of four virtual channels.
DI[5:0]: These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

Figure 4.37: Format of data ID

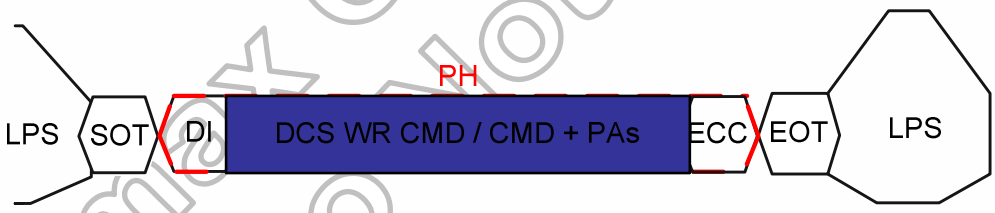
Due to Data Type (DT) mean format of transmission type, Figure 4.36 show Short- / Long-packet transmission command sequence.

Long packet write Command / Parameters / Pixel Datas



DI ➔ Write suitable Data type.
WC ➔ Write number of Payload Data.
Ex: One CMD write, WC setting as 1.
CMD + PAs write, WC setting as number of (CMD+PAs).
CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Short packet write Command / Parameters



DI ➔ Write suitable Data type.
Ex: One CMD write, DI + DCS WR CMD
CMD + PAs write, DI + DCS WR CMD + PAs

Figure 4.38: Show short- / long-packet transmission command sequence

4.4.2.1 Processor to peripheral direction packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.12 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 4.15: Data types for processor-sourced packets

Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	**Function description**	**Number of bytes**
01h	V Sync start, Start of VSA pulse.	2 bytes (DI + ECC)
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of HSA pulse.	
31h	H Sync End, End of HSA pulse.	
Note: V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively.		

Color mode status (Color Mode On, Color Mode Off)		
Data type, hex	**Function description**	**Number of bytes**
02h	Color Mode On that switches a Video Mode display module to a low-color mode for power saving.	2 bytes (DI + ECC)
12h	Color Mode Off that switches a Video Mode display module from low-color display to normal display.	

Display status (shutdown command, turn-on command)		
Data type, hex	**Function description**	**Number of bytes**
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	2 bytes (DI + ECC)
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	
Note: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.		

DCS command setting		
Data type, hex	**Function description**	**Number of bytes**
06h	DCS Read command, the returned data may be of Short or Long packet format.	3 bytes (DI + DCS CMD. + ECC)
39h	DCS Long Write/ Write_LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

Note: (1) For write part, If DCS Short Write command, followed by BTA, the peripheral shall respond with **ACK** when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with **Acknowledge with Error Report**.

(2) When use DCS Read Command, the **Set Max Return Packet Size** command will limit the size of returning packets.

(3) The peripheral shall respond to DCS Read Command Request in one of the following ways:

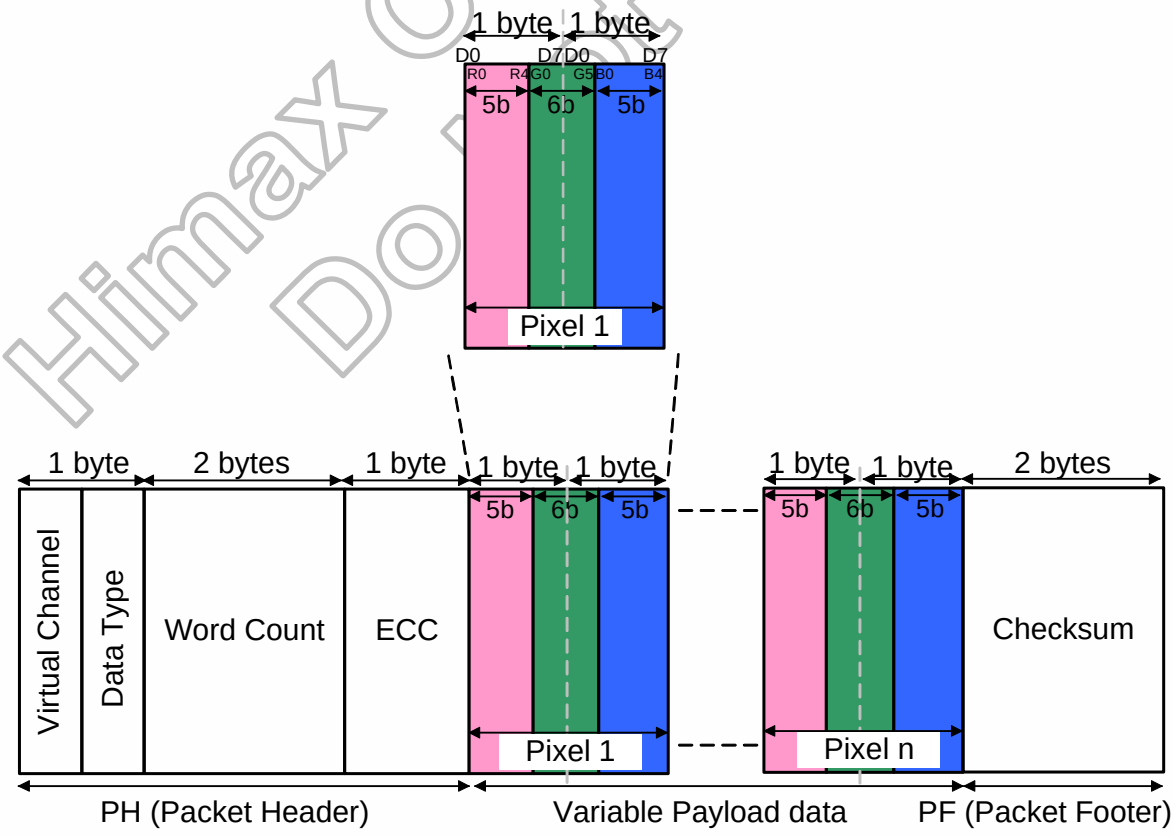
- If an error was detected by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.

(4) **One byte <= Length of payload DATA <= 2^{WC}-1**

Return packet size setting		
Data type, hex	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes (DI + WC + ECC)
Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.		

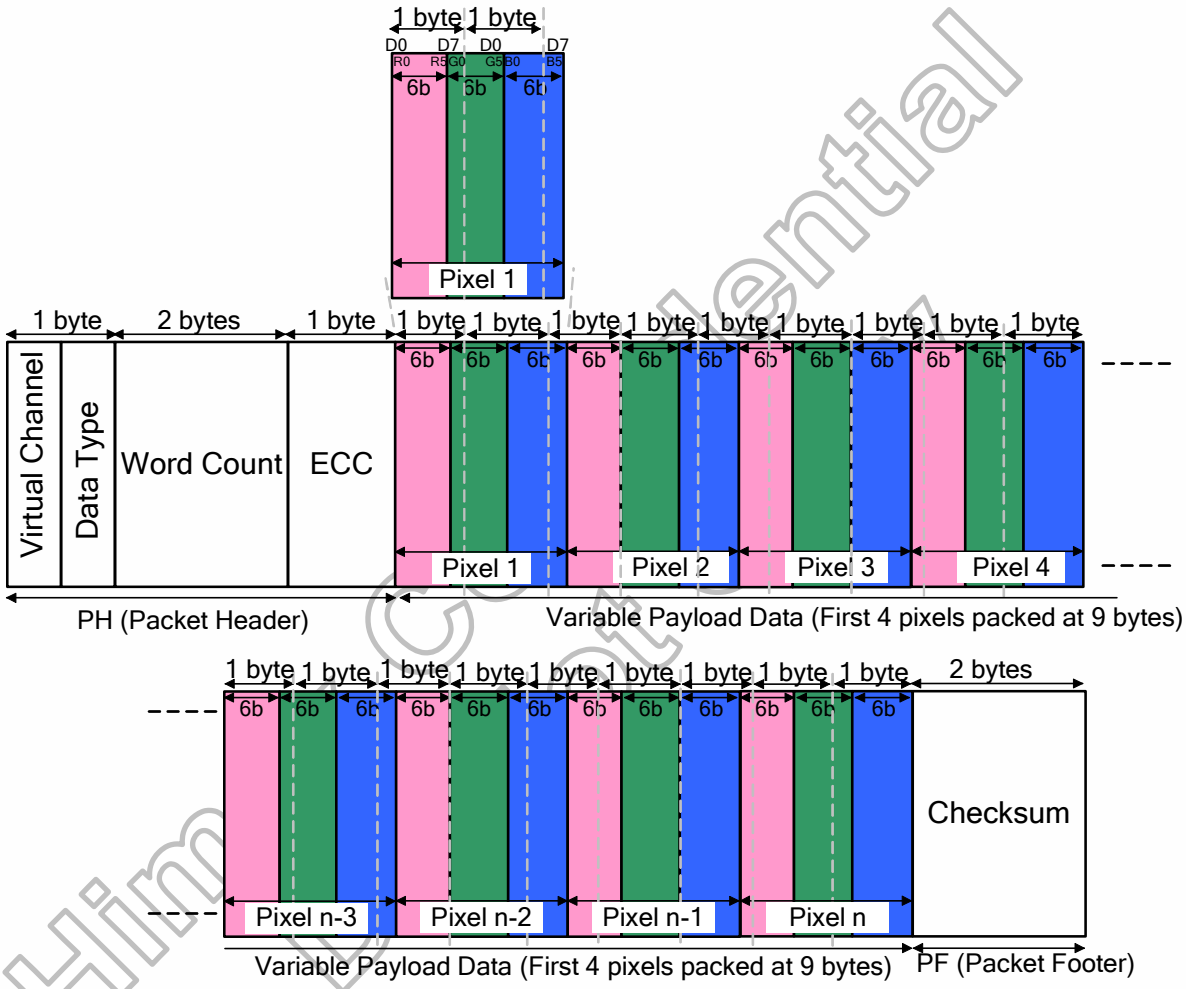
Variable data packet		
Data type, hex	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
19h	Blanking packet is used to convey blanking timing information in a Long packet.	
Note: (1) When **Null Packet**, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data. (2) When **Blanking packet**, the packet represents a period between active scan lines of a Video Mode display,		

Data stream format – 16bit Format		
Data type, hex	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "(5 bits) red, (6 bits) green and (5 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



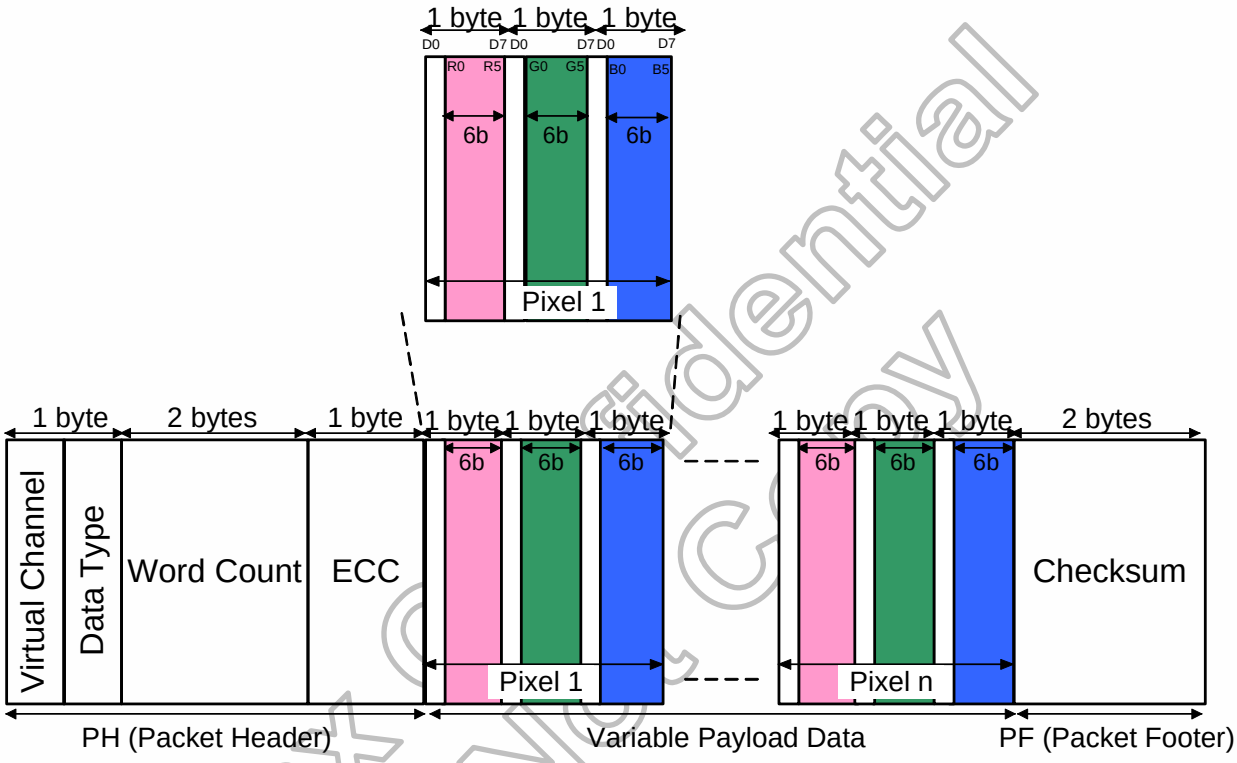
Note: Within a color component, the "LSB is sent first, the MSB last ".

Data stream format – 18bit Format		
Data type, hex	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



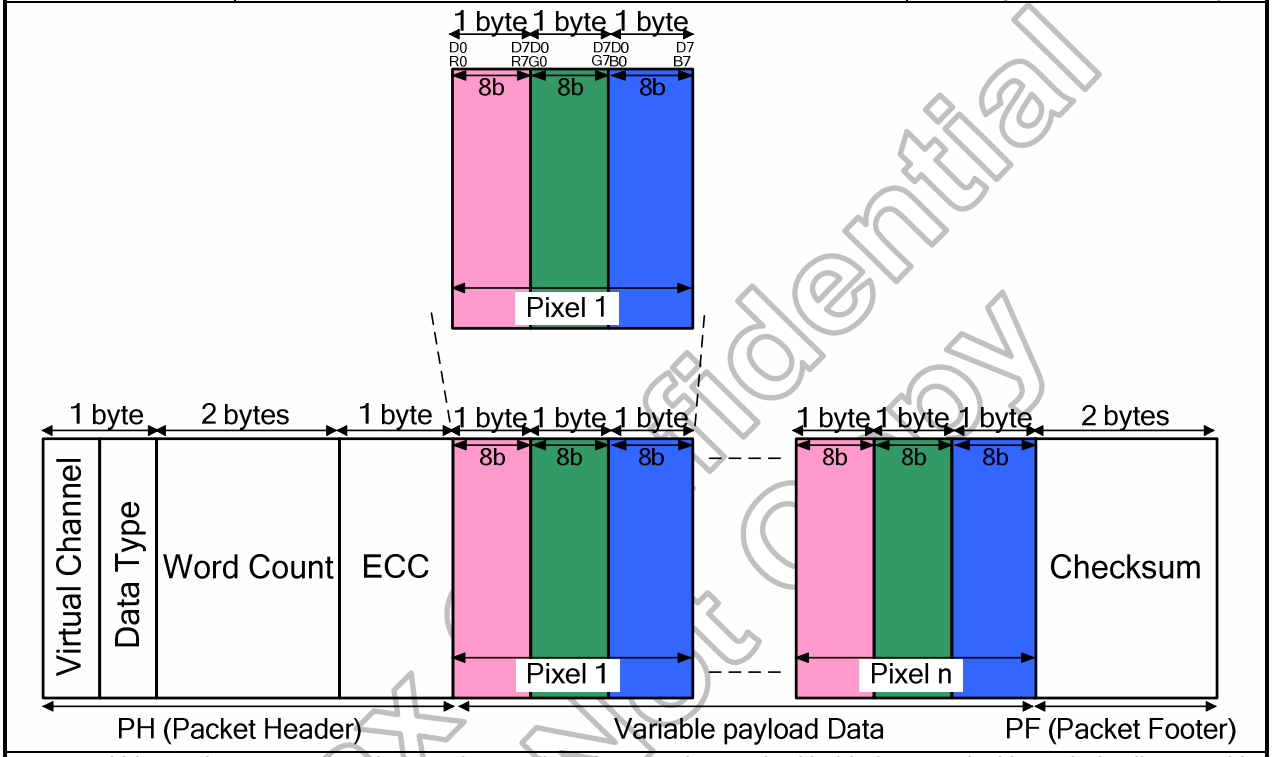
Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.

Data stream format – 18bit Format		
Data type, hex	**Function description**	**Number of bytes**
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is “(6 bits) red, (6 bits) green and (6 bits) blue”.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Data stream forma – 24bit Format		
Data Type, Hex	**Function Description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

4.4.2.2 Peripheral to processor (reverse direction)

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets may use ECC and Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

Peripheral-to-processor transactions are of four basic types:

A. Tearing Effect is a Trigger message sent to convey display timing information to the host processor. Trigger messages ate signal byte packets sent by a peripheral's PHY layer in response to a signal form the DSI protocol layer.
B. *Acknowledge* is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
C. Acknowledge and Error Report is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
D. Response to Read Request may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with BTA asserted, can contain under form.

A. Following a **non-Read command** in which no error was detected, the peripheral shall respond with Acknowledge.
B. Following a **Read request** in which no error was detected, the peripheral shall send the requested READ data.
C. Following a **Read request in which the ECC error** was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
D. Following a **non-Read command in which the ECC error** was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
E. Following any command in which **SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid** was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

Which,

A. “Acknowledge” includes 2 bytes which are DI (VC + Acknowledge Data Type) and ECC.
B. “Acknowledge with Error Report” include 4 bytes which are DI, 2 bytes Error report and ECC.
C. “Response to Read Request” contains 2 types which are Short packet and long packet.

An error report is comprised of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.16 shows the Error Report Bit Definitions. And Table 4.16 list complete set of peripheral-to-processor Data Types.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	reserved
7	reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

Table 4.16: Shows the error report bit definitions

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
08h	00 1000	End of Transmission (EoT) packet	Short
1Ch	01 1100	DCS Long READ Response	Long
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short
Others (00h→3Fh)		Reserved	-

Table 4.17: Complete set of peripheral-to-processor data types

Acknowledge types		
Data type, hex	**Function description**	**Number of bytes**
02	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error➔Acknowledge with error report, Without error➔ Acknowledge.		

DCS Read types		
Data type, hex	**Function description**	**Number of bytes**
21h, 22h	This is the DCS Short Read Response, 1 or 2 bytes, respectively.	4 bytes
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		

5. Functional Description

5.1Display data GRAM mapping

The display data RAM stores display dots and consists of 2,764,800 bits (320x18x480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **CASET's SC, EC** and **PASET's SP, EP**, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

5.1.1 Address counter (AC)

The HX8357-D00/D01 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range:

MV	X range	Y range	Panel resolution
0	0~319d.	0~479d.	320 RGBX480 dot
1	0~479d.	0~319d.	

Table 5.1: Addresses counter range

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the Column address register (start: SC, end: EC) or the Row address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

5.1.2 System interface to GRAM write direction

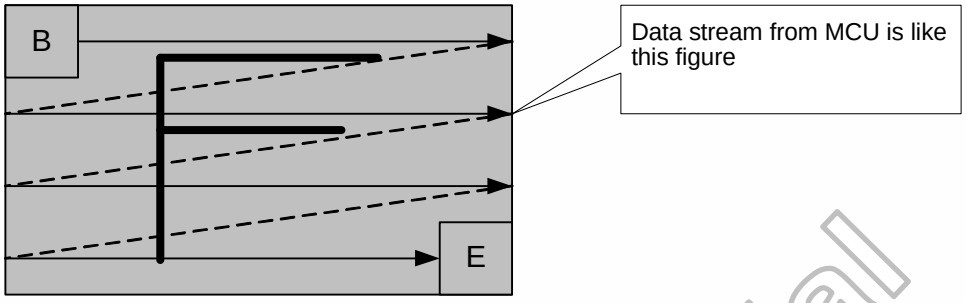


Figure 5.1: Image data sending order from host

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by MADTCL's MV(B5), MX(B6) and MY(B7) bits setting

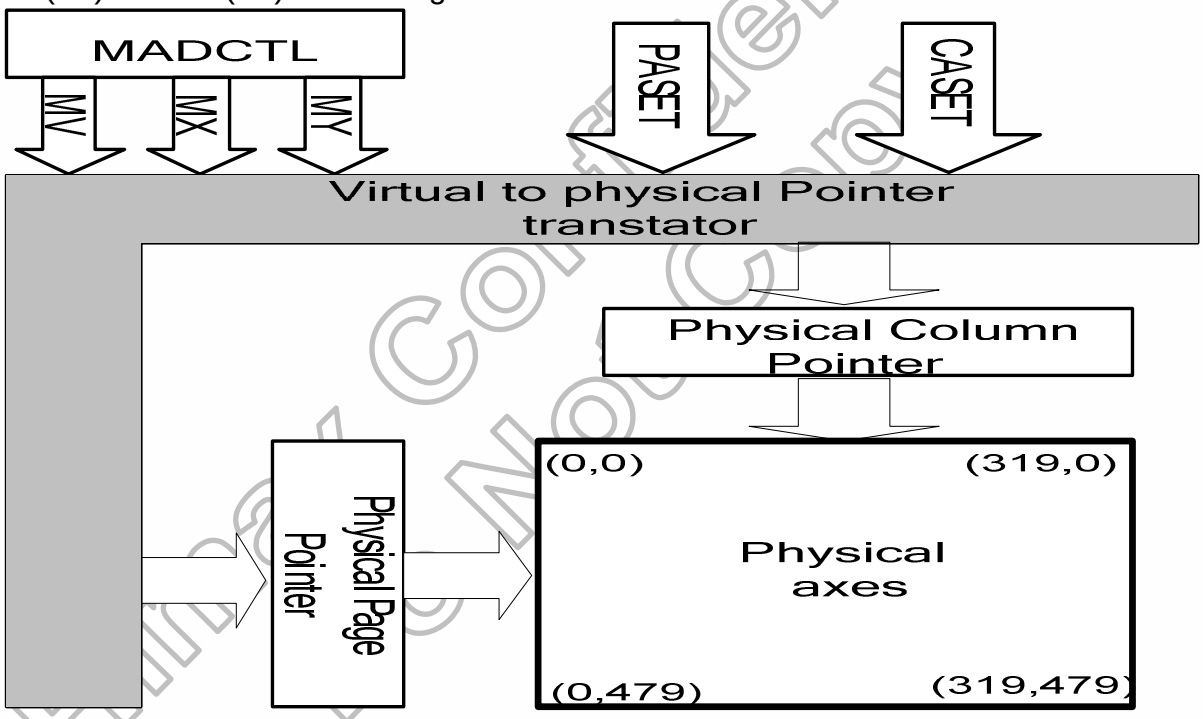


Figure 5.2: MY,MX,MV Setting of GRAM control

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

Table 5.2: MY.MX.MV Setting of GRAM address mapping

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

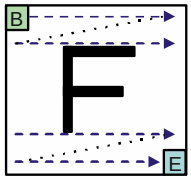
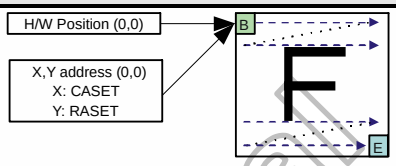
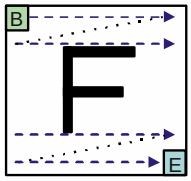
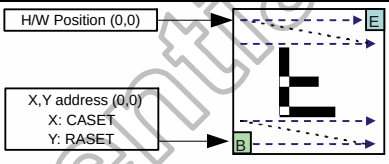
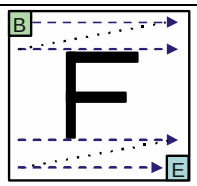
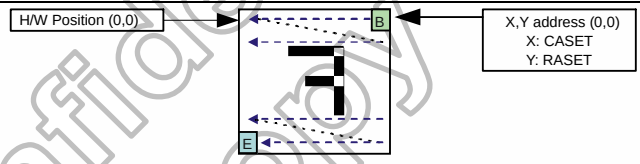
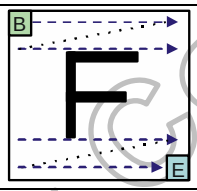
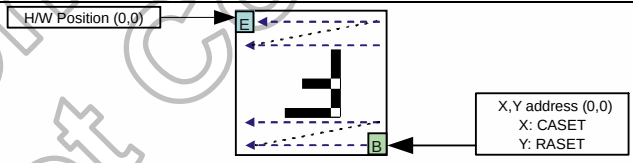
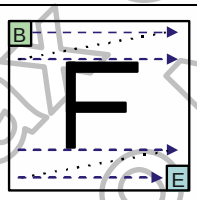
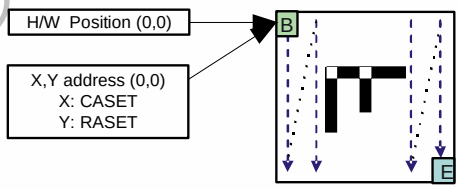
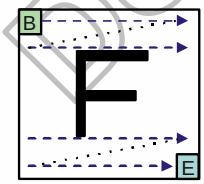
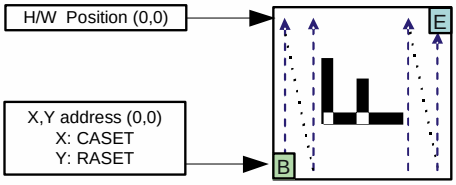
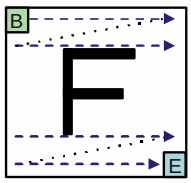
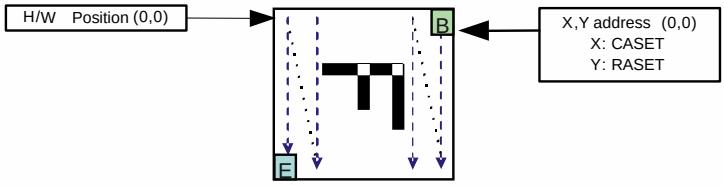
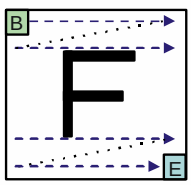
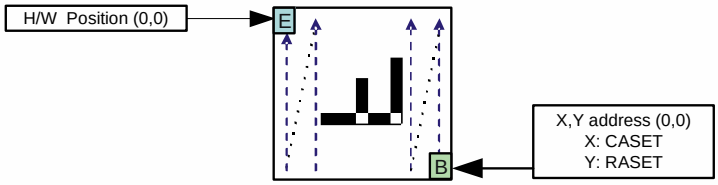
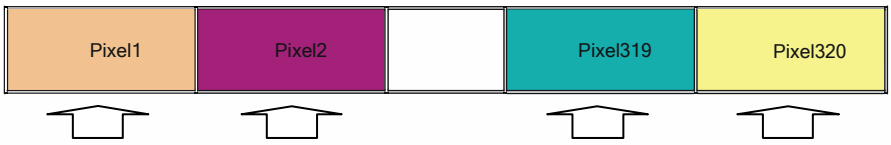
Display Data Direction	MADCTR parameter MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange X-invert	1	0	1		
X-Y Exchange Y-invert	1	1	0		
X-Y Exchange X-invert Y-invert	1	1	1		

Table 5.3: Address direction settings

5.1.3 Source, gate and memory map



Source Out		S1	S2	S3	S4	S5	S6	RGB Order ——— :BGR=0 ----- :BGR=1	S955	S956	S957	S958	S959	S960	SA	
RA																
MY=0	MY=1														ML=0	ML=1
0	479	R0 5-0	G0 5-0	B0 5-0	R1 5-0	G1 5-0	B1 5-0	–	R318 5-0	G318 5-0	B318 5-0	R319 5-0	G319 5-0	B319 5-0	0	479
1	478							–							1	478
2	477							–							2	477
3	476							–							3	476
4	475							–							4	475
5	474							–							5	474
6	473							–							6	473
7	472							–							7	472
8	471							–							8	471
9	470							–							9	470
10	469							–							10	469
11	468							–							11	468
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
472	7							–							472	7
473	6							–							473	6
474	5							–							474	5
475	4							–							475	4
476	3							–							476	3
477	2							–							477	2
478	1							–							478	1
479	0							–				RN 5-0	GN 5-0	BN 5-0	479	0
CA	MX=0	0			1				318			319				
	MX=1	319			318				1			0				

Note: RA = Row Address.
CA = Column Address.
SA = Scan Address.
MX = Mirror X-axis (Column address direction parameter), D6 parameter of Memory Access Control (R36h) command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of Memory Access Control (R36h) command
ML = Scan direction parameter, D4 parameter of Memory Access Control (R36h) command
BGR = Red, Green and Blue pixel position change, D3 parameter of Memory Access Control (R36h) command

Figure 5.3: Memory map 320RGBx480 dot

5.1.4 Fully display, partial display, vertical scrolling display

5.1.4.1 Full display

Example: (1) 320RGBx480 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x13Fh (R2Ah) and SP=0x000h, EP=0x1DFh (R2Bh), ML=0.

GRAM	00h DB---DB 17 --- 0	01h DB---DB 17 --- 0	--------- ---------	13Eh DB---DB 17 --- 0	13Fh DB---DB 17 --- 0
000h	000000H	000001H	---------	00013EH	00013FH
001h	001000H	001001H	---------	00113EH	00113FH
002h	002000H	002001H	---------	00213EH	00213FH
003h	003000H	003001H	---------	00313EH	00313FH
004h	004000H	004001H	---------	00413EH	00413FH
005h	005000H	005001H	---------	00513EH	00513FH
⋮	⋮	⋮	---------	⋮	⋮
1DAh	1DA000H	1DA001H	---------	1DA13EH	1DA13FH
1DBh	1DB000H	1DB001H	---------	1DB13EH	1DB13FH
1DCh	1DC000H	1DC001H	---------	1DC13EH	1DC13FH
1DDh	1DD000H	1DD001H	---------	1DD13EH	1DD13FH
1DEh	1DE000H	1DE001H	---------	1DE13EH	1DE13FH
1DFh	1DF000H	1DF001H	---------	1DF13EH	1DF13FH

Table 5.4: Memory map of full display

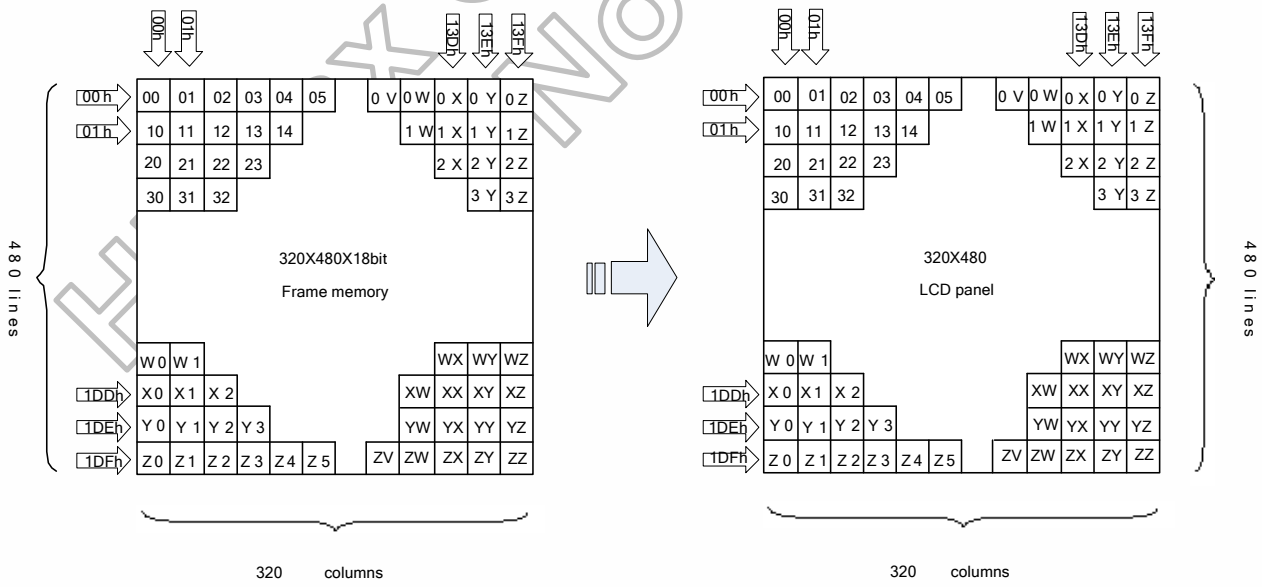


Figure 5.4: Memory map of full display

5.1.4.2 Partial display

Example: (1) 320RGBx480 dot display mode.
(2) PLTON instruction (R12h).
(3) SR[15:0]=0002h, ER[15:0]=01DBh, ML=0.

GRAM	00h DB---DB 17 --- 0	01h DB---DB 17 --- 0	--------- ---------	13Eh DB---DB 17 --- 0	13Fh DB---DB 17 --- 0
000h	000000H	000001H	---------	00013EH	00013FH
001h	001000H	001001H	---------	00113EH	00113FH
002h	002000H	002001H	---------	00213EH	00213FH
003h	003000H	003001H	---------	00313EH	00313FH
004h	004000H	004001H	---------	00413EH	00413FH
005h	005000H	005001H	---------	00513EH	00513FH
⋮	⋮	⋮	---------	⋮	⋮
1DAh	1DA000H	1DA001H	---------	1DA13EH	1DA13FH
1DBh	1DB000H	1DB001H	---------	1DB13EH	1DB13FH
1DCh	1DC000H	1DC001H	---------	1DC13EH	1DC13FH
1DDh	1DD000H	1DD001H	---------	1DD13EH	1DD13FH
1DEh	1DE000H	1DE001H	---------	1DE13EH	1DE13FH
1DFh	1DF000H	1DF001H	---------	1DF13EH	1DF13FH

LCD panel S/G pins	Pixel 1	Pixel 2	---------	Pixel319	Pixel320
G1	000000H	000001H	---------	00013EH	00013FH
G2	001000H	001001H	---------	00113EH	00113FH
G3	002000H	002001H	---------	00213EH	00213FH
G4	003000H	003001H	---------	00313EH	00313FH
G5	004000H	004001H	---------	00413EH	00413FH
G6	005000H	005001H	---------	00513EH	00513FH
⋮	⋮	⋮	---------	⋮	⋮
G475	1DA000H	1DA001H	---------	1DA13EH	1DA13FH
G476	1DB000H	1DB001H	---------	1DB13EH	1DB13FH
G477	1DC000H	1DC001H	---------	1DC13EH	1DC13FH
G478	1DD000H	1DD001H	---------	1DD13EH	1DD13FH
G479	1DE000H	1DE001H	---------	1DE13EH	1DE13FH
G480	1DF000H	1DF001H	---------	1DF13EH	1DF13FH

Table 5.5: Memory map of partial display

5.1.4.3 Vertical scrolling display

The vertical scrolling display is specified by VSCRDEF instruction (R33h) and VSCRSADD instruction (R37h).

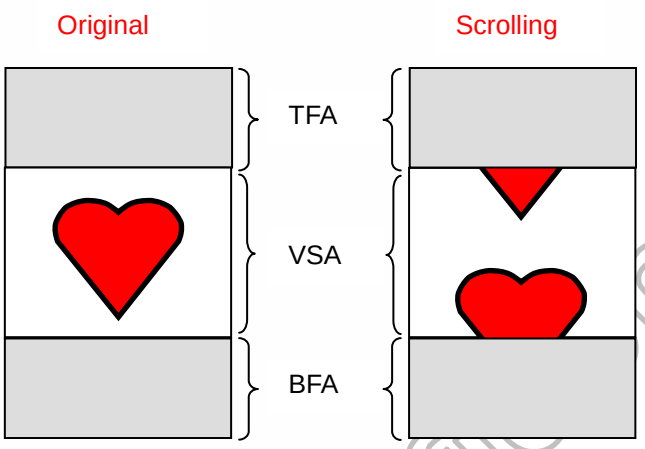


Figure 5.5: Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=Panel total scan lines. In this case, scrolling is applied as shown below.

Example 1 : (1) 320RGBx480 dot display mode.
(2) TFA=2,VSA=478,BFA=0 when MADCTL B4=0
(3) VSCRSADD=03h

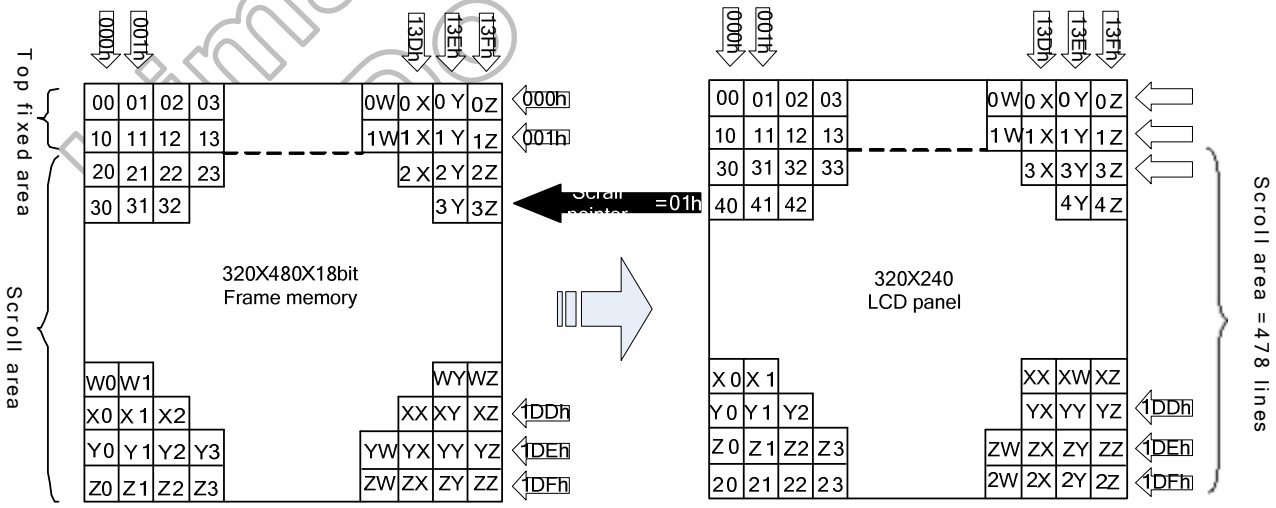


Figure 5.6: Memory map of vertical scrolling example 1

Example 2 : (1) 320RGBx480 dot display mode.
(2) TFA=2,VSA=476,BFA=2 when MADCTL B4=0
(3) VSCRSADD=03h

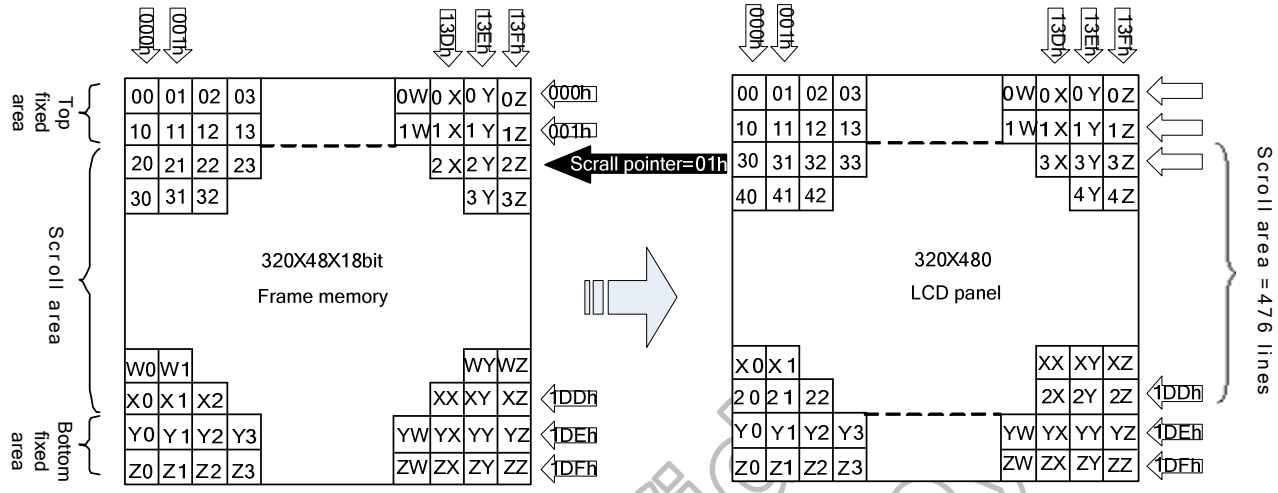


Figure 5.7: Memory map of vertical scrolling example 2

Example 3 : (1) 320RGBx480 dot display mode.
(2) TFA=2,VSA=476,BFA=2 when MADCTL B4=0
(3) VSCRSADD=04h

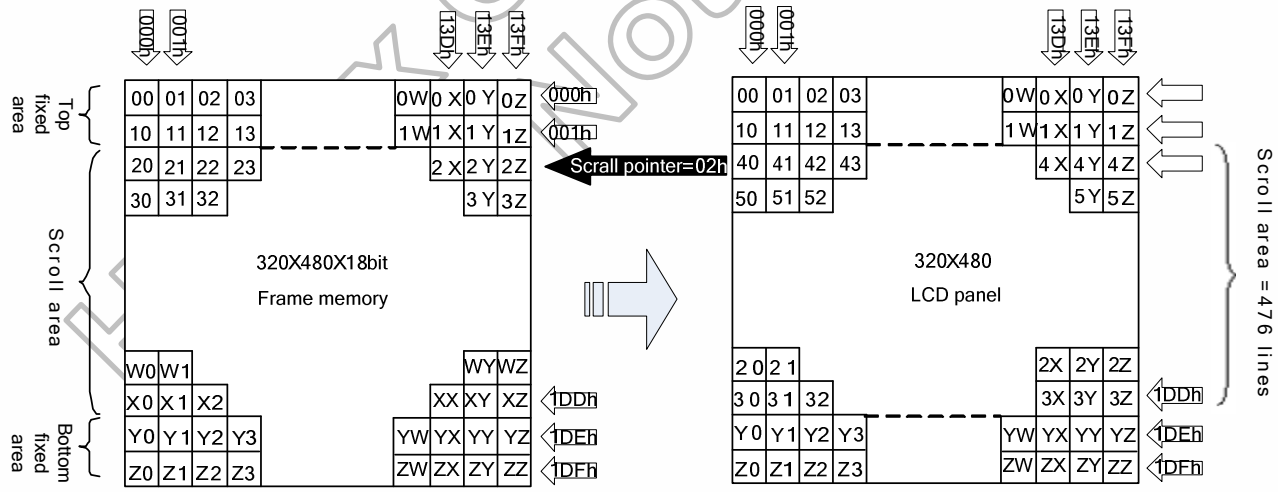


Figure 5.8: Memory map of vertical scrolling example 3

Vertical **Scroll Example**

There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA ≠ Panel scan lines
N/A. Do not set TFA + VSA + BFA≠Panel scan lines. In that case, unexpected picture will be shown.
Case 2: TFA + VSA + BFA = Panel scan lines (Scrolling)

Example 1 : (1) 320RGBx480 dot display mode.
(2) When TFA=0, VSA=480, BFA=0 and VSCRSADD=40. MADCTL parameter B4="0"

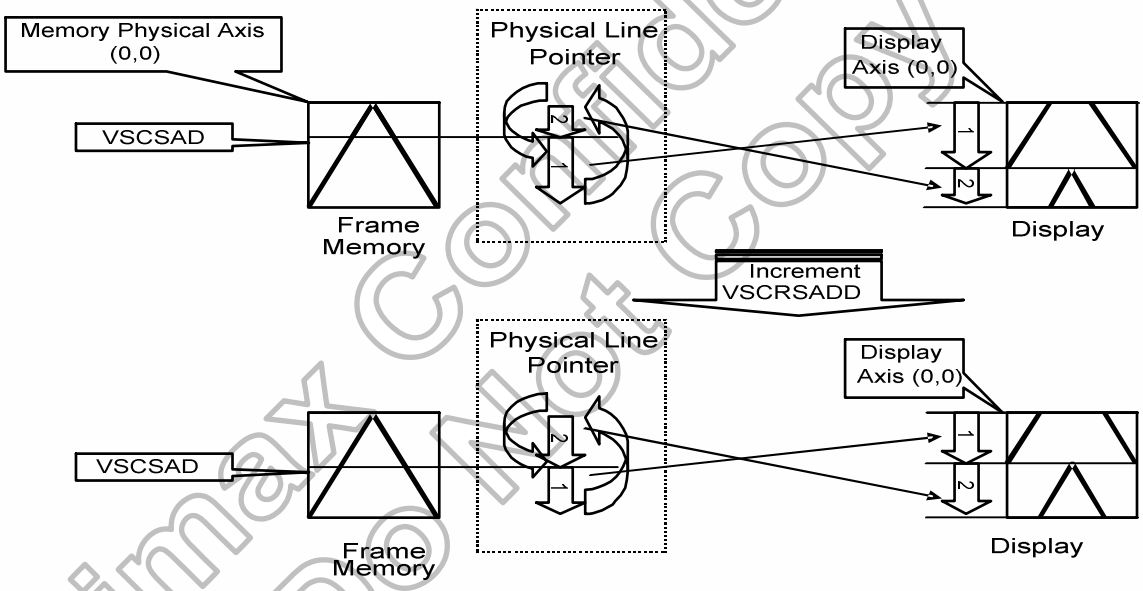


Figure 5.9: Display of vertical scroll example 1

Example 2 : (1) 320RGBx480 dot display mode.
(2) TFA=60, VSA=420, BFA=0 and VSCRSADD =160. MADCTRL parameter B4=”1”

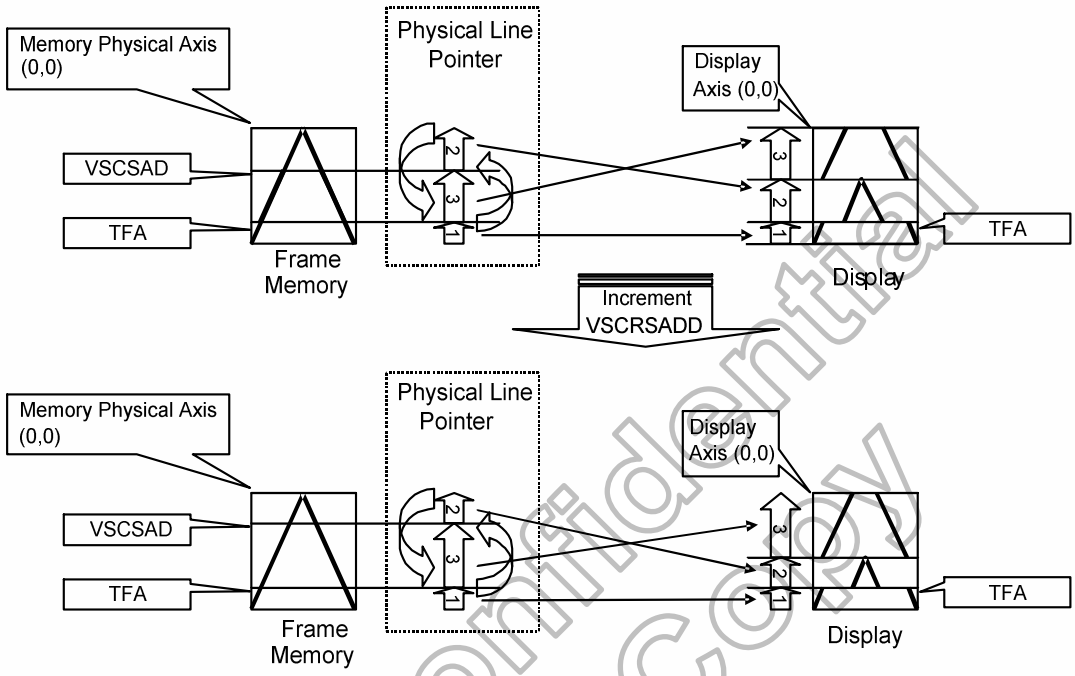


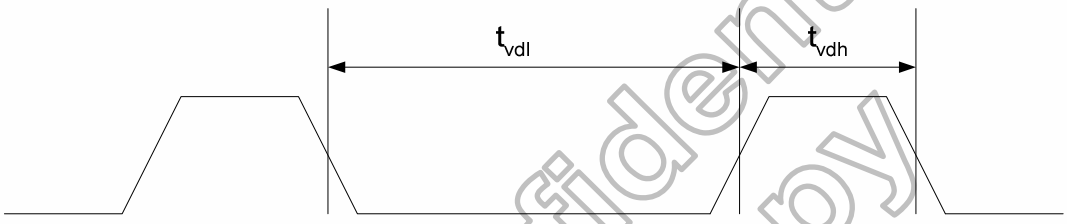
Figure 5.10: Display of vertical scroll example 2

5.2Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.2.1 Tearing effect line modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Figure 5.11: TE mode 1 output

Under Mode1, the TE output timing will be defined by TSEL[15:0] setting.
Ex:
1. TSEL[15:0]=0, then TE signal will output after last Line finished.
2. TSEL[15:0]=2, then TE signal will output at second Line start.

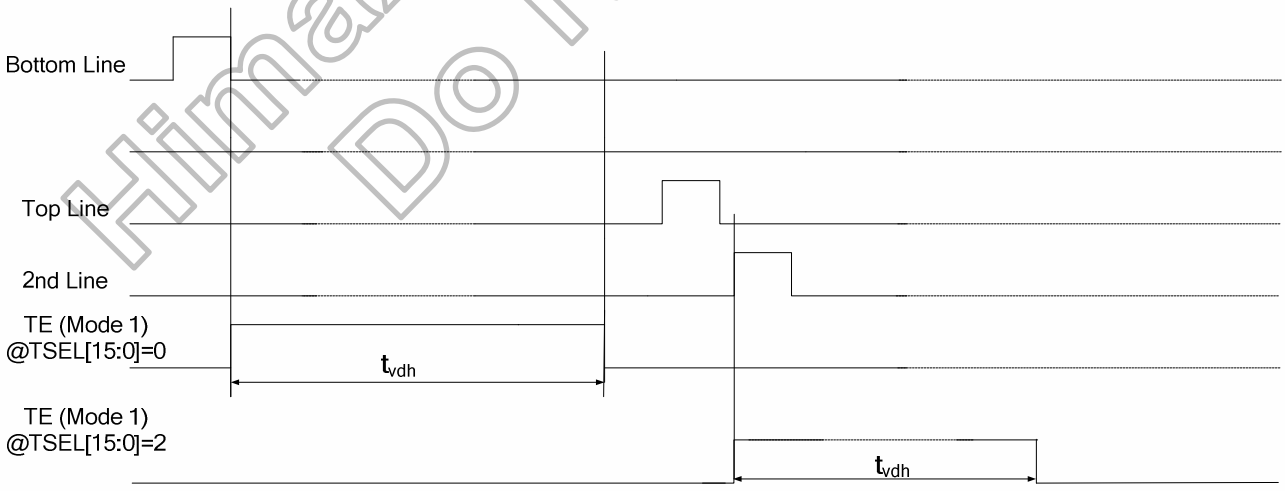
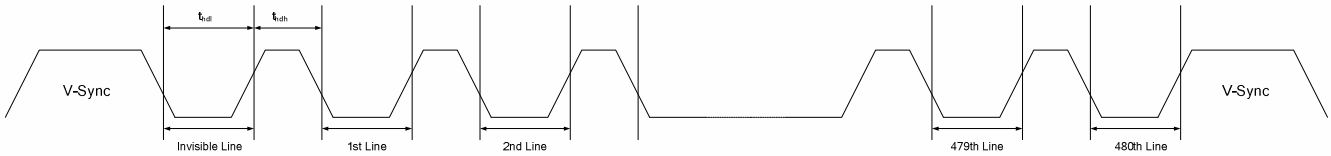


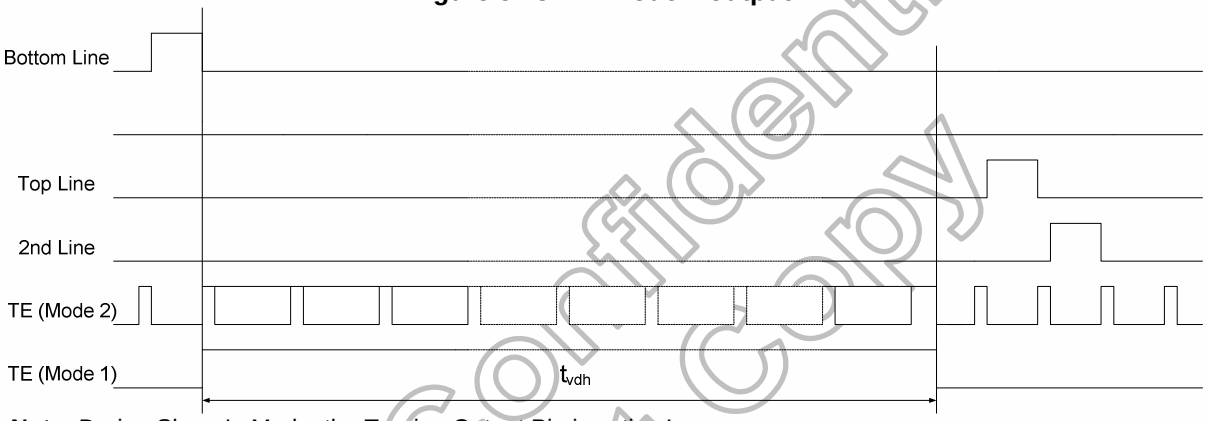
Figure 5.12: TE delay output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Figure 5.13: TE mode 2 output



Note: During Sleep In Mode, the Tearing Output Pin is active Low

Figure 5.14: TE output waveform

5.2.2 Tearing effect line timing

The Tearing Effect signal is described below.

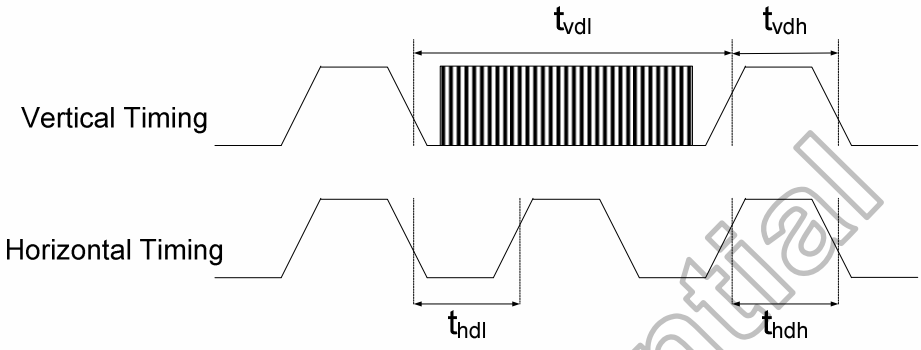


Figure 5.15: Waveform of tearing effect signal

Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Spec.			Unit	Description
		Min.	Typ.	Max.		
tvdl	Vertical Timing Low Duration	-		-	ms	-
tvdh	Vertical Timing High Duration	1000		-	µs	-
thdl	Horizontal Timing Low Duration	-		-	µs	-
thdh	Horizontal Timing High Duration	-		500	µs	-

Table 5.6: AC characteristics of tearing effect signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

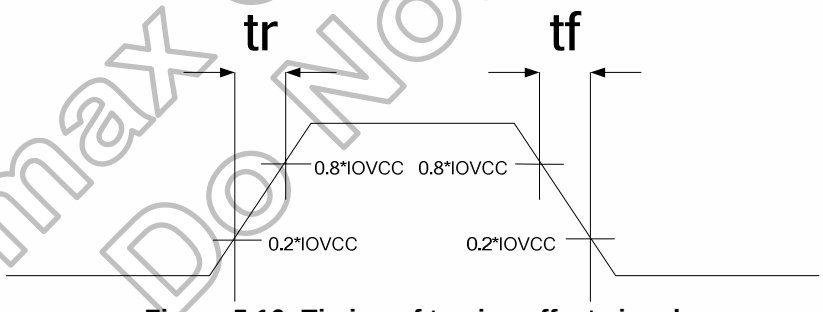


Figure 5.16: Timing of tearing effect signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

5.2.3 Example 1: MPU write is faster than panel read

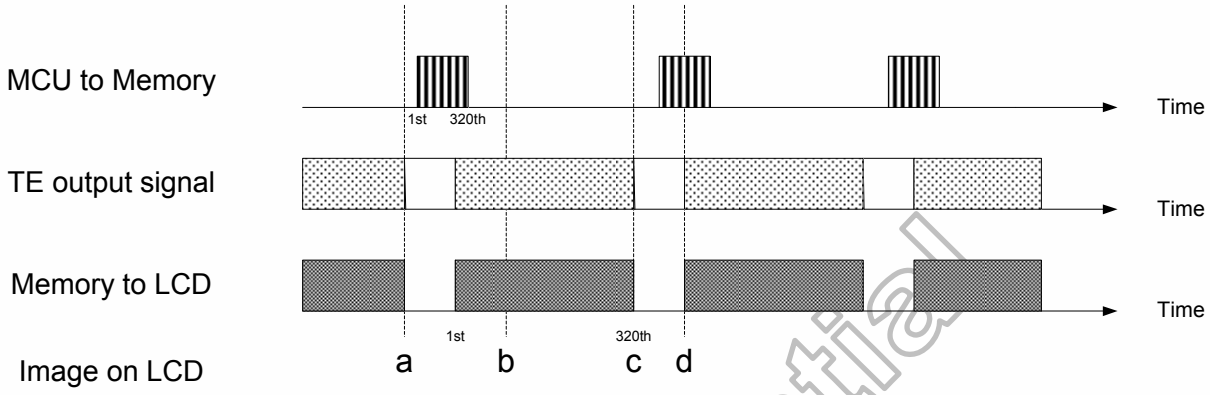


Figure 5.17: Timing of MPU write is faster than panel read

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

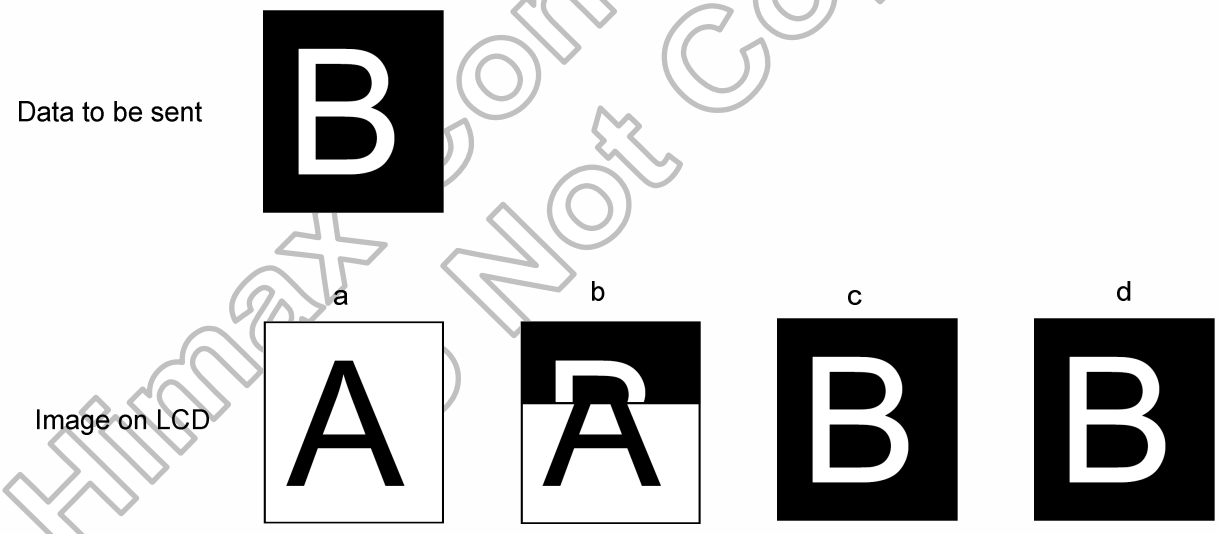


Figure 5.18: Display of MPU write is faster than panel read

5.2.4 Example 2: MPU write is slower than panel read

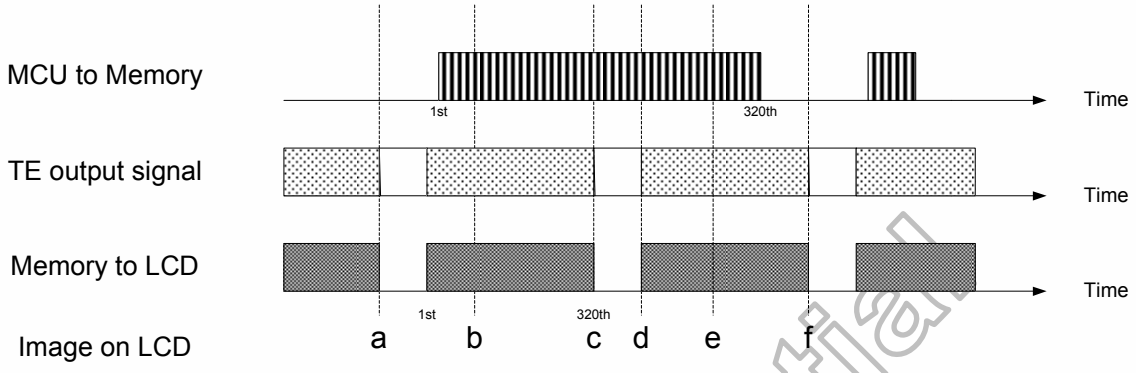


Figure 5.19: Timing of MPU write is slower than panel read

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

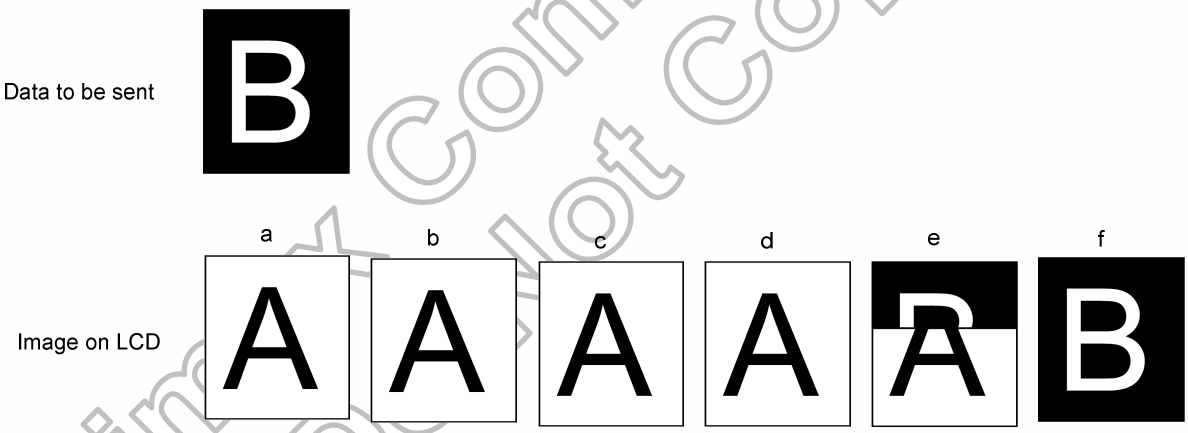


Figure 5.20: Display of MPU write is slower than panel read

5.3Checksums

The display module consists of two 8-bit checksum registers, which are used checksum calculations for area registers (includes the frame memory), on the display module. Command area registers are registers which values users can change a command directly.

One of the checksum registers is “First Checksum” (FCS) and another is “Continue Checksum” (CCS).

These register values are set to 00h as an initial value when there is started to calculate a new checksum.

The display module is starting to calculate the new checksum after there is a write access on command area registers. This means that read commands are not used as a calculation starting trigger in this case.
The checksum calculation is always interrupted, when there is a new write access on command area registers.
The checksum calculation is also started from the beginning.

The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on area registers and the new checksum value is calculated in the first time again.
The maximum time, when the FCS is readable, is 150ms after there is the last write access on area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last command area register has been calculated to the checksum.
The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on command area registers.

There is always updated a checksum comparison bit (See section: “Read Display Self-Diagnostic Result (0Fh)” and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time).

Users can read FCS, CCS and Comparison bit D0 values. See section: “Read First Checksum (AAh)”,
“Read Continue Checksum (AFh)” and ”Read Display Self-Diagnostic Result (0Fh)”.
There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:

- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in “Sleep Out” mode and it is stopped in “Sleep In” mode.

Step Note 1	Time Note 2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on area registers => FCS and CCS registers are initialized.
2	0 – 150ms	Counting Sum of command Area Registers	Counting	-	-	The first register counting is running
3	150ms	Stores Sum of Registers on FCS Register	Set to 00h after Value is Moved to FCS Register	Stores Sum of Area Registers on FCS Register	-	The result of the first register counting is stored on the FCS register. The result of the FCS is available to the MCU.
4	150 – 300ms	Counting Sum of command Area Registers	Counting	-	-	The second register counting is running
5	300ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of command Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MCU.
6	300 – 450ms	Counting Sum of command Area Registers	Counting	-	-	The third register counting is running
7	450ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of command Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU.
8	450 – 600ms	Counting Sum of command Area Registers	Counting	-	-	The fourth register counting is running
9	600ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of command Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU.
10	etc	-	-	-	-	Same Sequence Countinue e.g. steps 4 and 5

Note: (1) This function is restarted at Step 1 if there is any write action on command area registers.
(2) These time can be shorter on the display module.

5.4Oscillator

The HX8357-D00/D01 can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±5%, it can be adjusted by the **UADJ [3:0]** bits for initial 10MHz internal clock generation. With other dividers setting, the 10MHz internal clock can be used to generate clock for other part of the chip using.

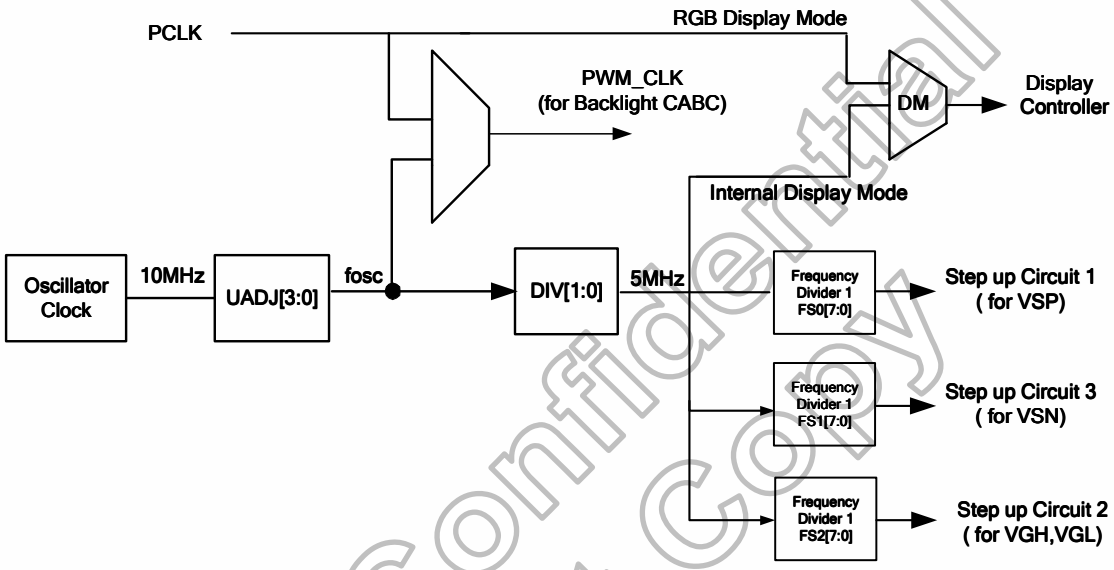


Figure 5.21: HX8357-D00/D01 internal clock circuit

5.5Source driver

The HX8357-D00/D01 contains a 481 channels of source driver (normal S1~S480; Zig-zag S1~S481) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 481 channels and generates corresponding gray scale voltage output, which can realize a 262k colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

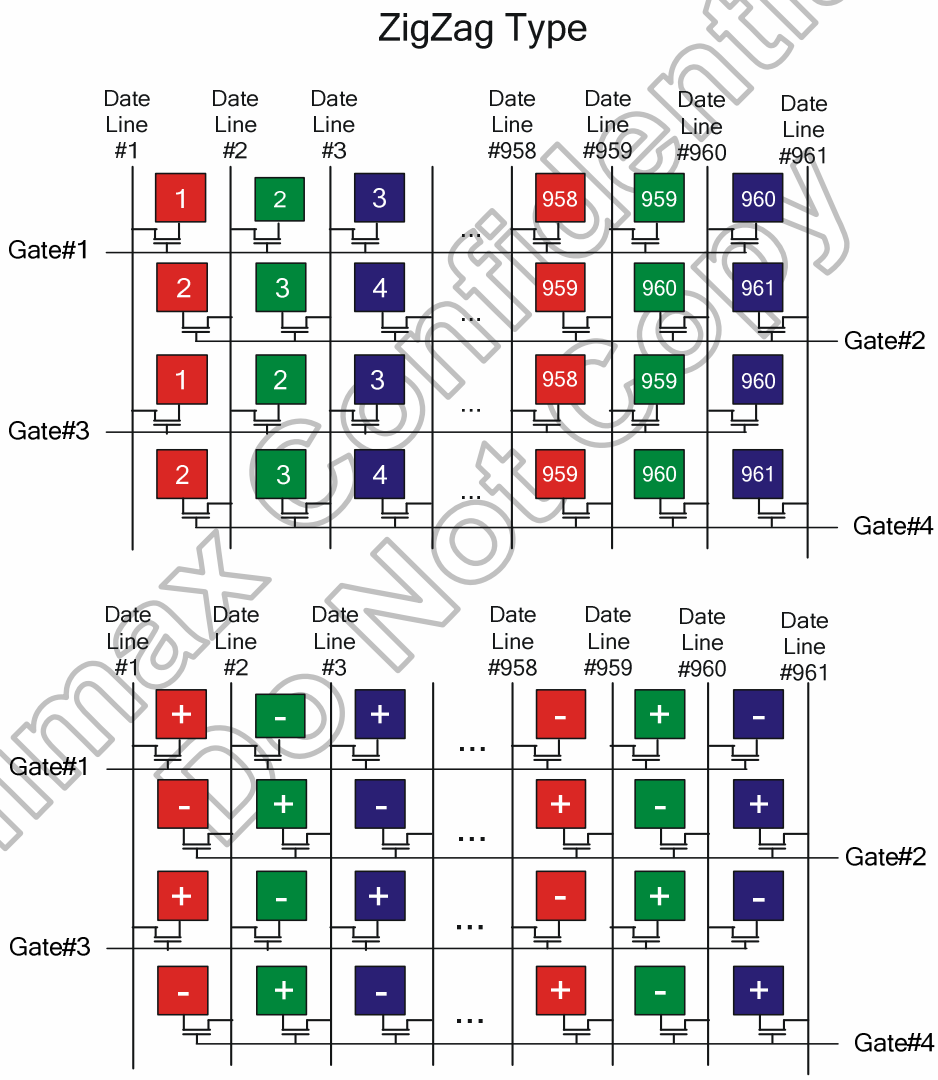


Figure 5.22: Source channels of ZigZag inversion mode

5.6Gate driver

The HX8357-D00/D01 contains a 480 gate channels of gate driver (G1~G480) which is used for driving the gate. The gate driver level is VGH in scan line, the other lines is VGL.

The HX8357-D00/D01 can set internal register SM_PANEL and GS_PANEL bit to determine the pin assignment of gate. The SM_PANEL and GS_PANEL setting allows changing the shift direction of gate outputs by connecting LCD panel with the HX8357-D00/D01.

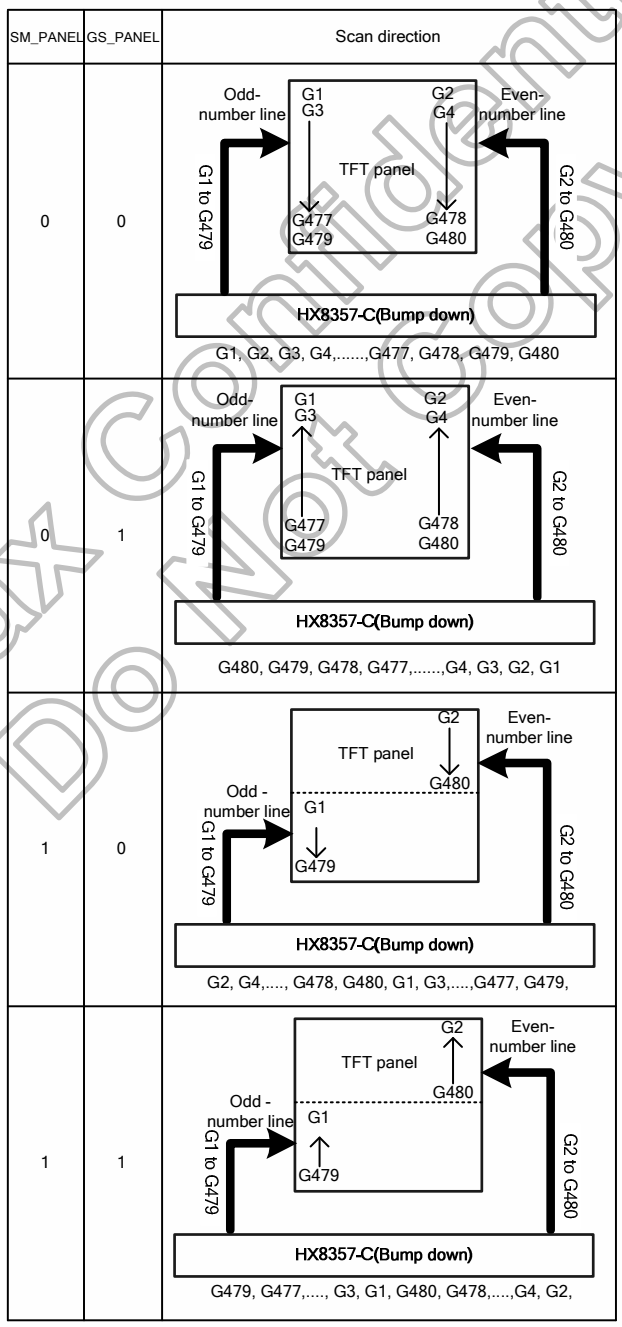


Figure 5.23: Scan direction of Gate Driver

5.7LCD power generation circuit

5.7.1 Power supply circuit

The power circuit of HX8357-D00/D01 is used to generate supply voltages for LCD panel driving.

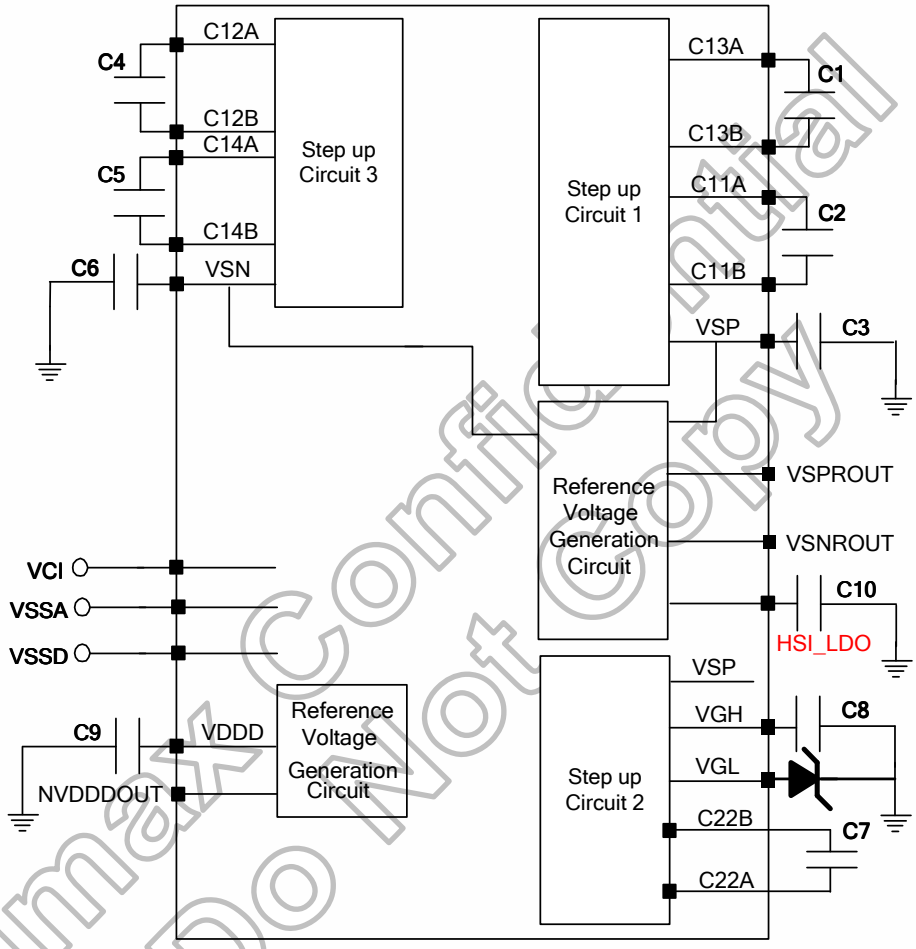


Figure 5.24: Block diagram of HX8357-D00/D01 power circuit

Specification of connected passive component

Capacitor	Recommended voltage	Capacity
C1 (C13A/B)	10V	1 µF (B characteristics)
C2 (C11A/B)	10V	1 µF (B characteristics)
C3 (VSP)	10V	1 µF ~ 2.2uF (B characteristics)
C4 (C14A/B)	10V	1 µF (B characteristics)
C5 (C12A/B)	10V	1 µF (B characteristics)
C6 (VSN)	10V	1 µF~2.2uF (B characteristics)
C7 (C22A/B)	16V	1 µF (B characteristics)
C8 (VGH)	25V	1 µF (B characteristics)
C9(VDDD)	6V	1 µF (B characteristics)
C10(HSI_LDO)	6V	1 µF (B characteristics)
D1 (VGL-VSSA)	Schottky Diode	VF < 0.4V / 20mA at 25℃, VR ≥30V (Recommended diode: RB521S-30)

Note: If not use High speed interface (DSI), the capacitor of HSI_LDO can be removed.

Table 5.7 Adoptability of capacitor

5.7.2 LCD power generation scheme

The boost voltage generated is shown as below.

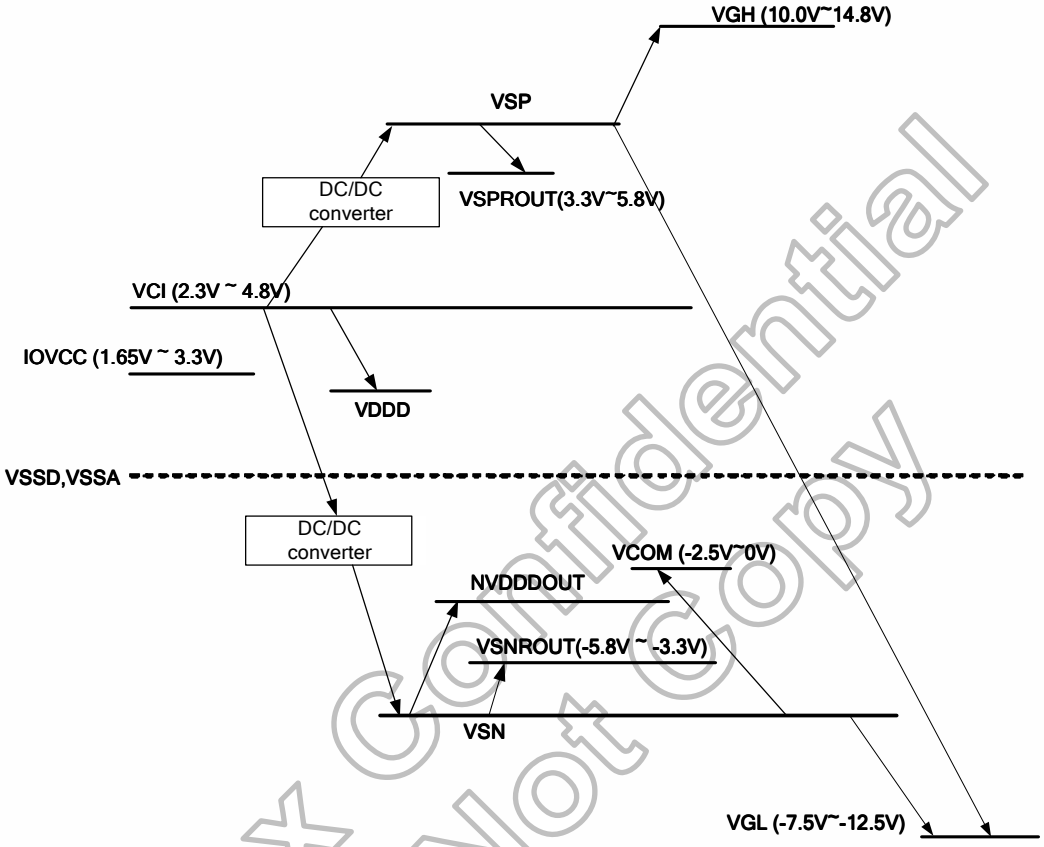
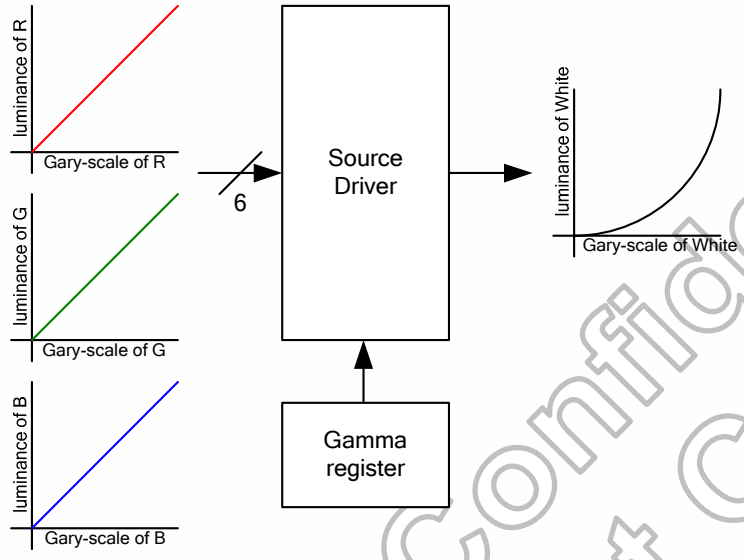


Figure 5.25: LCD power generation scheme

5.8Gamma characteristic correction function

The HX8357-D00/D01 offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction

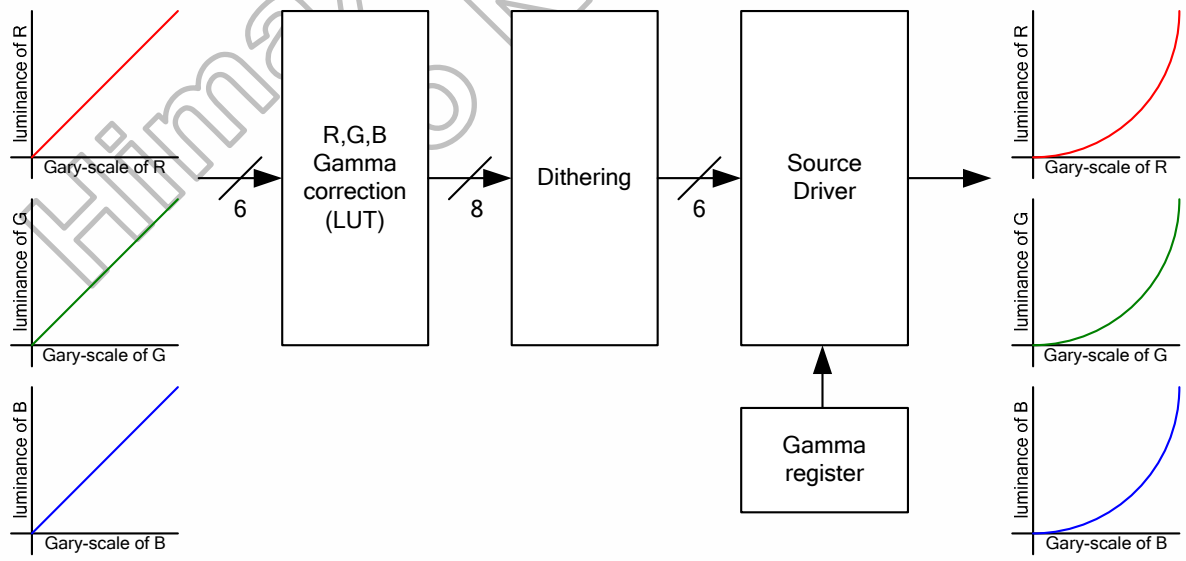


Figure 5.26: Gamma adjustments different of source driver with digital gamma correction

5.8.1 Gamma characteristic correction function

The HX8357-D00/D01 incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment operation is implemented by deciding the 16 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

Gamma resister stream

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including 16 gamma reference voltages. VgP/N (0, 1, 2, 4, 6, 13, 20, 27, 36, 43, 50, 57, 59, 61, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.

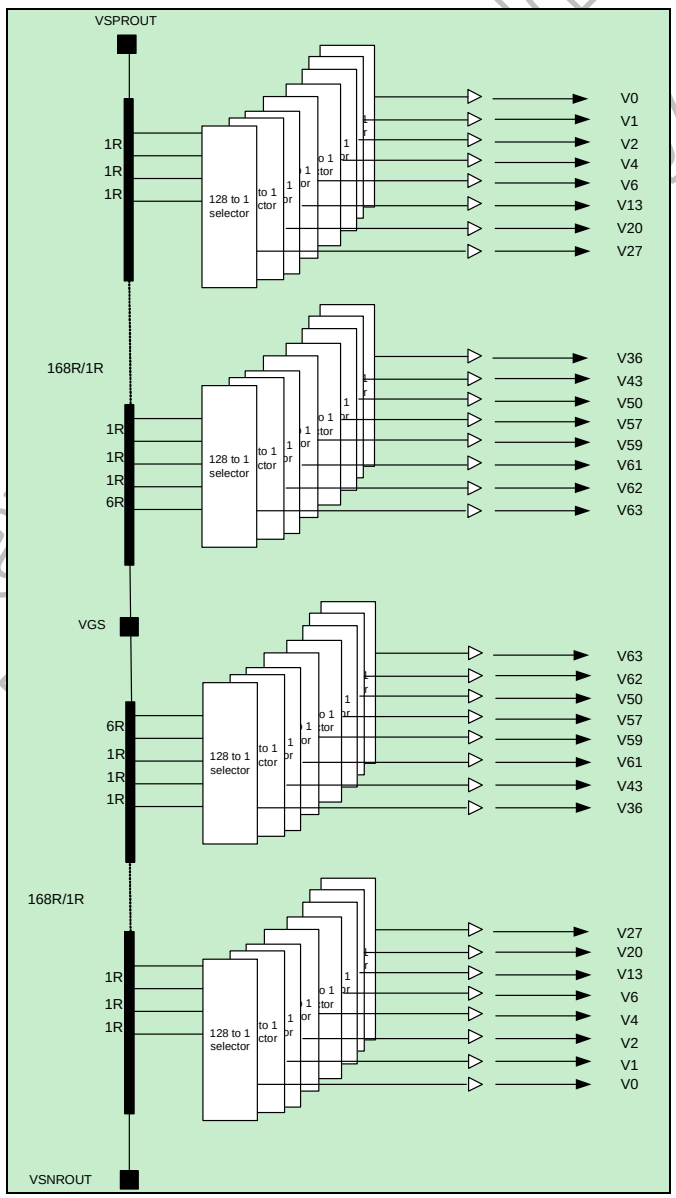


Figure 5.27: Gamma resister stream and gamma reference voltage

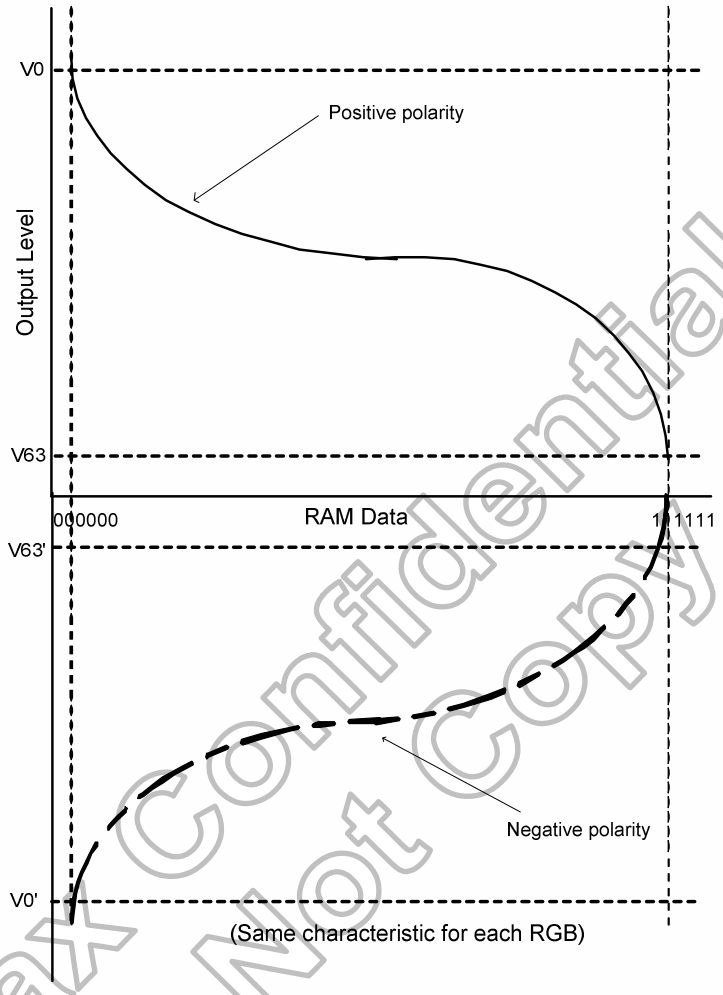


Figure 5.28: Relationship between GRAM data and output level (normal white panel REV_Panel="0")

Four-characteristic gamma curve selection

There are four kinds of Gamma Curve which can be selected by GAMSET command. The parameter GC[7:0] is stored in internal register and used to select one set of gamma correction register.

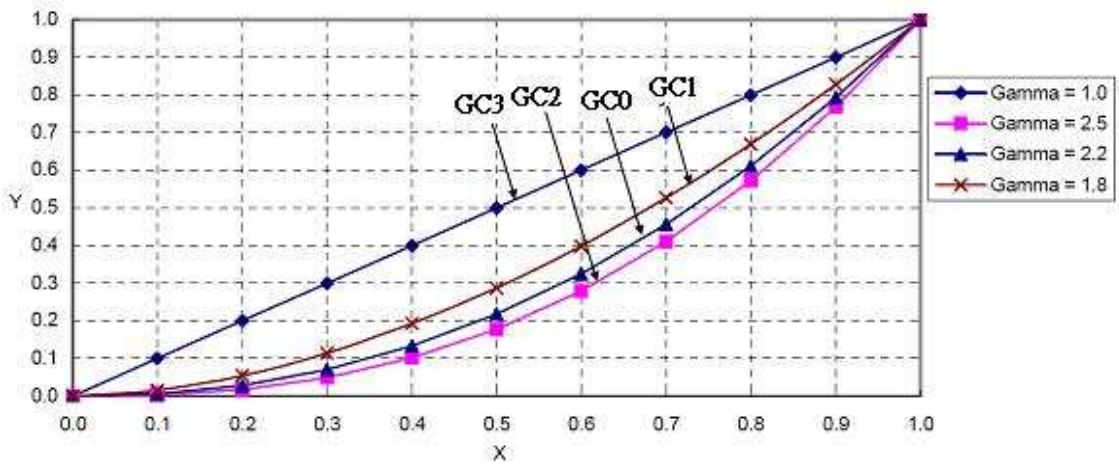


Figure 5.29: Gamma curve according to GC0 to GC3 bit

5.8.2 Gray voltage generator for digital gamma correction

The HX8357-D00/D01 digital gamma correction can reach the independent GAMMA curve of RGB. The HX8357-D00/D01 utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 6-bit into 8-bit and sends 8-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

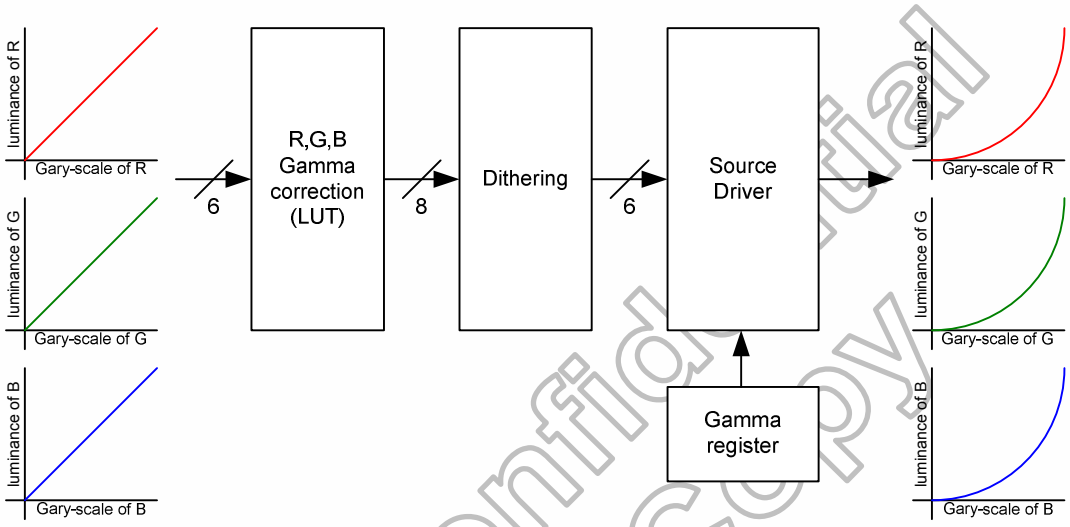


Figure 5.30: Block diagram of digital gamma correction

There are 99 bytes DGC LUT to set R, G, B gamma independently. When DGC_EN=1, R, G, B gamma will mapping V0, V2, V4, ..., V60, V62, V63 voltage to the LUT register setting gray level voltage. V(2N+1) = (V(2N) + V(2N+2))/2 (N=0~30).

Parameter	Input (6 bit)	D7	D6	D5	D4	D3	D2	D1	D0	Default	Gray Mapping
1st	R00h	R007	R006	R005	R004	R003	R002	R001	R000	00h	R_V0
2nd	R02h	R017	R016	R015	R014	R013	R012	R011	R010	08h	R_V2
3rd	R04h	R027	R026	R025	R024	R023	R022	R021	R020	10h	R_V4
	:	:	:	:	:	:	:	:	:	:	:
32nd	R62h	R317	R316	R315	R314	R313	R312	R311	R310	F8h	R_V62
33rd	R63h	R327	R326	R325	R324	R323	R322	R321	R320	FCh	R_V63
34th	G00h	G007	G006	G005	G004	G003	G002	G001	G000	00h	G_V0
35th	G02h	G017	G016	G015	G014	G013	G012	G011	G010	08h	G_V2
36th	G04h	G027	G026	G025	G024	G023	G022	G021	G020	10h	G_V4
	:	:	:	:	:	:	:	:	:	:	:
65th	G62h	G317	G316	G315	G314	G313	G312	G311	G310	F8h	G_V62
66th	G63h	G327	R326	G325	G324	G323	G322	G321	G320	FCh	G_V63
67th	B00h	B007	B006	B005	B004	B003	B002	B001	B000	00h	B_V0
68th	B02h	B017	B016	B015	B014	B013	B012	B011	B010	08h	B_V2
69th	B04h	B027	B026	B025	B024	B023	B022	B021	B020	10h	B_V4
	:	:	:	:	:	:	:	:	:	:	:
98th	B62h	B317	B316	B315	B314	B313	B312	B311	B310	F8h	B_V62
99th	B63h	B327	B326	B325	B324	B323	B322	B321	B320	FCh	B_V63

5.9Power function

5.9.1 Power on/off sequence

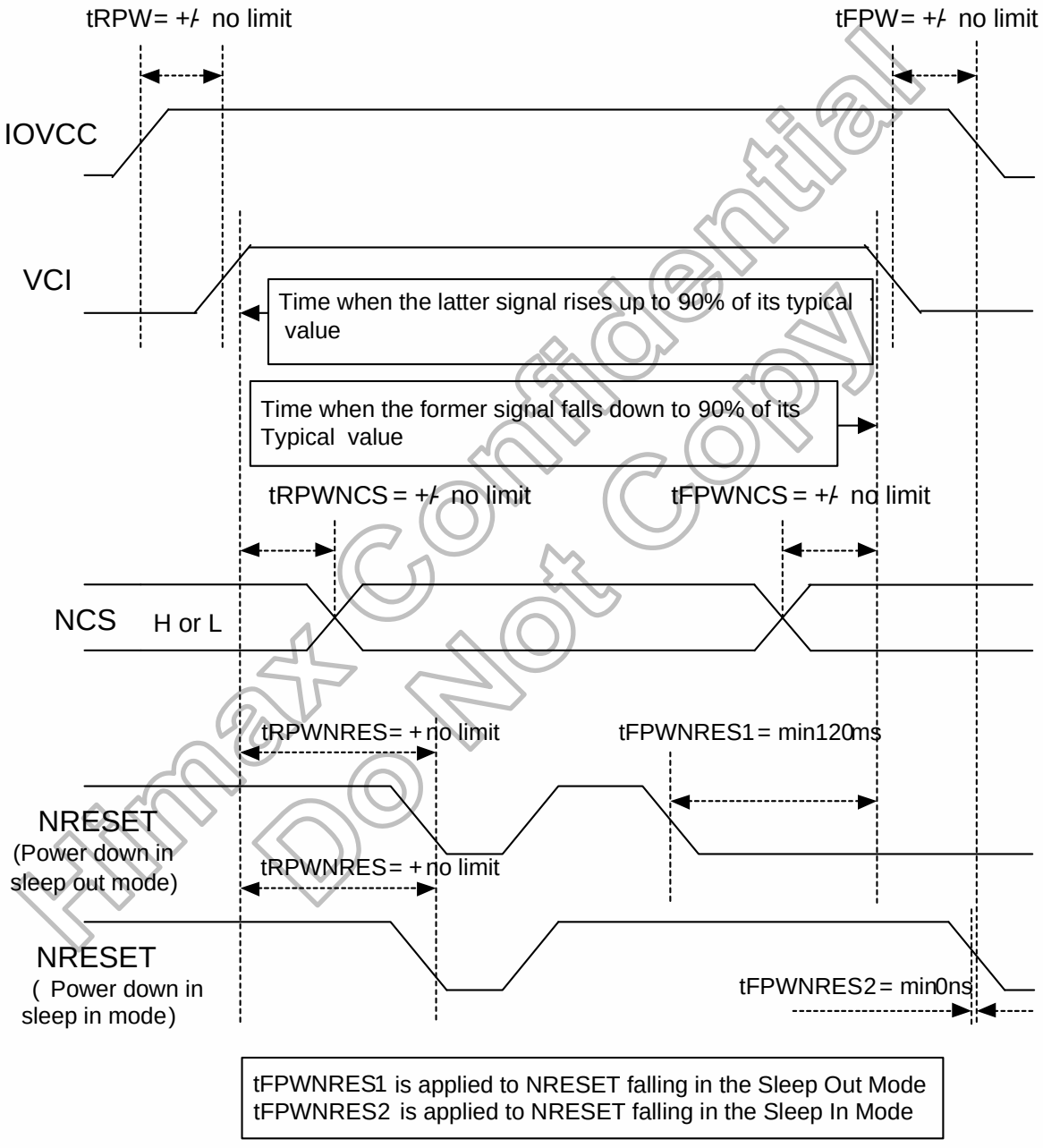
Power source IOVCC, VCI can be applied and powered down in any order.
IOVCC, VCI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.
During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.
NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

Note: (1) There will be no damage to the display module if the power sequences are not met.
(2) There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
(3) There will be no abnormal visible effects on the display between end of Power on Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
(4) If NRESET line is not held stable by host during Power on Sequence as defined in Sections 5.11.1.1 and 5.11.1.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence to ensure correct operation. Otherwise correct function is not guaranteed.

If NRESET line is not held stable by host during Power on Sequence as defined in Sections 5.9.1.1 and 5.9.1.2 then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence is complete to ensure correct operation, otherwise correct functionality is not guaranteed. The power on/off sequence is illustrated as below

5.9.1.1 Case 1 – NRESET line is held high or unstable by host at power on

If NRESET line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC, VCI have been applied, otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

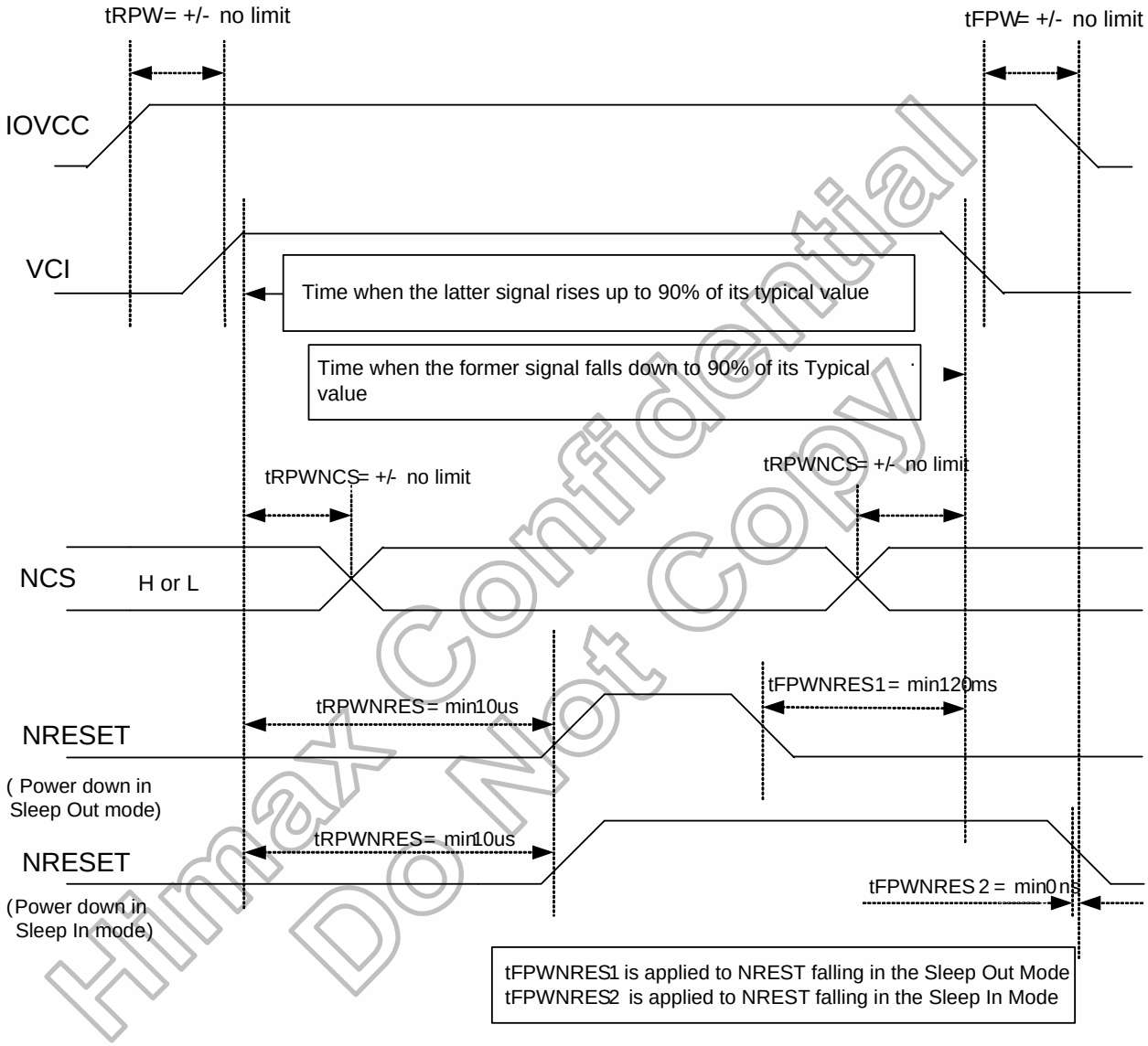


Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5.31: Case 1 – NRESET line is held high or unstable by host at power on

5.9.1.2 Case 2 – NRESET line is held low by host at power on

If NRESET line is held Low (and stable) by the host during Power On, then the NRESET must be held low for minimum 10µsec after VCI have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5.32: NRESET line is held low by host at power on

5.9.2 Power levels definition

5.9.2.1 General definition for power levels

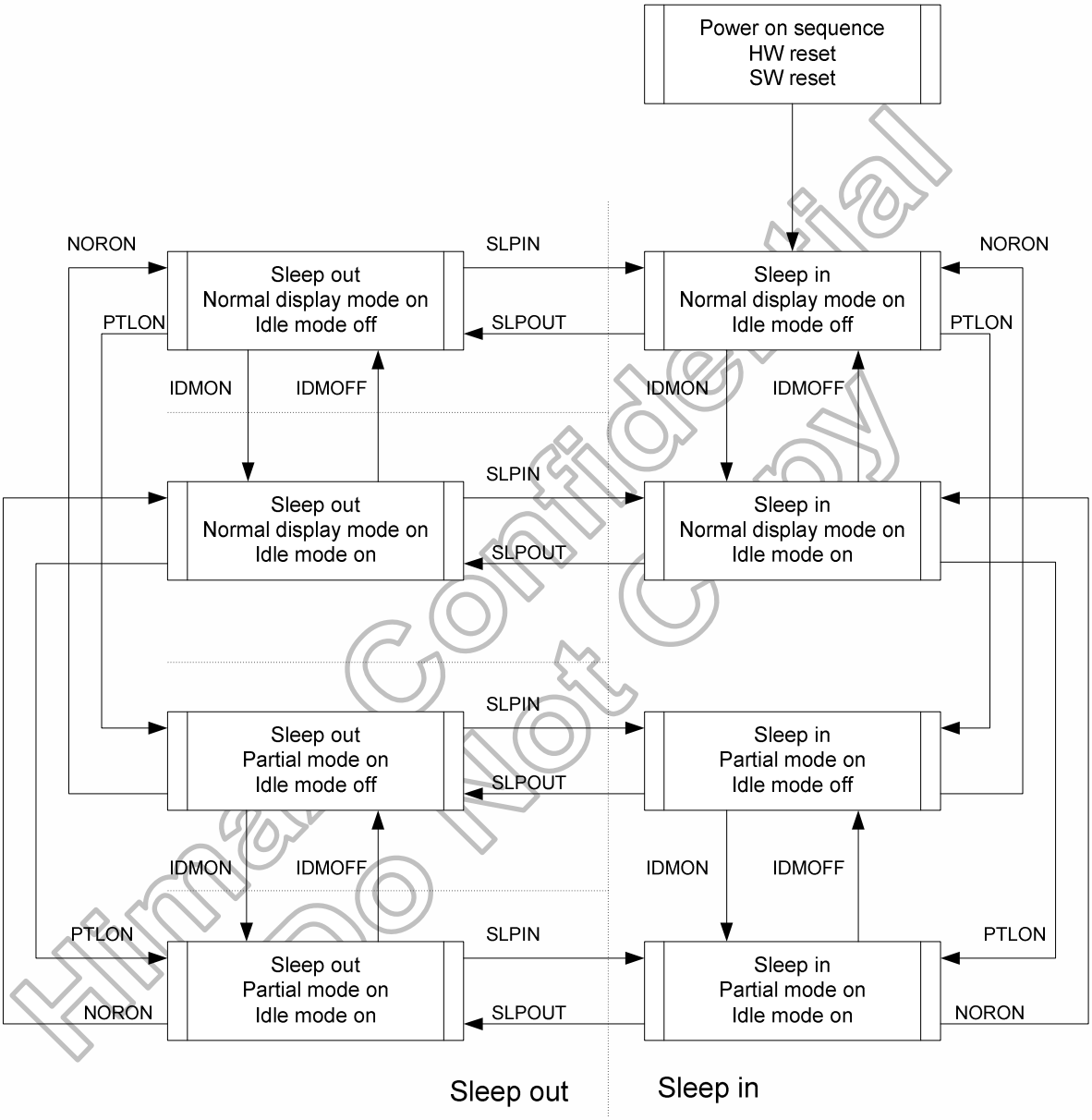


Figure 5.33: Power flow chart for different power modes

5.9.3 Deep standby mode set up flow

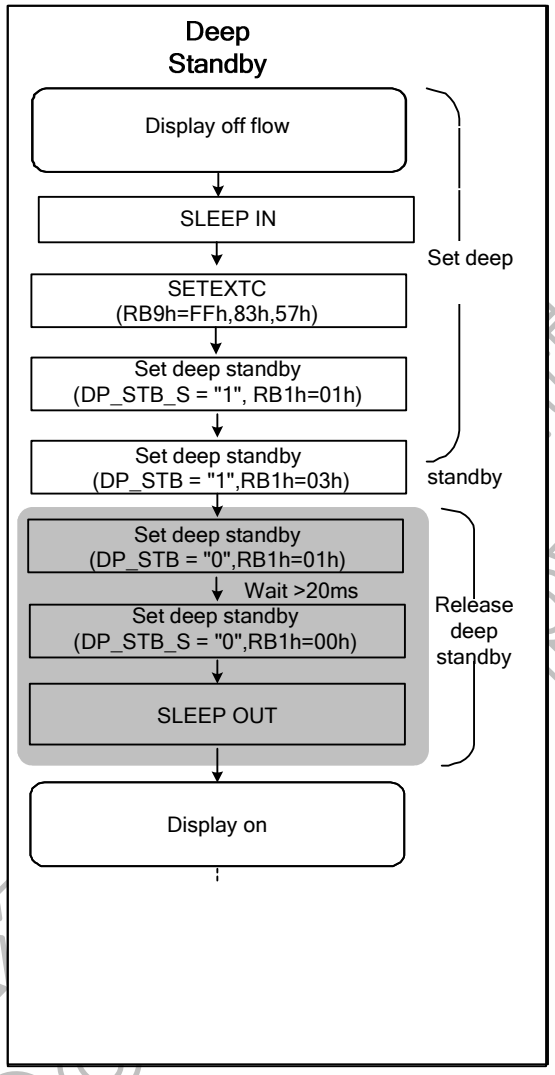


Figure 5.34: Deep standby mode setting flow

5.10Input / output pin state

5.10.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB23 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
CABC_ON	Low	Low
CABC_PWM	Low	Low

Table 5.8: Characteristics of output pins

5.10.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX_SCL	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
DCX	Input invalid	Input valid	Input valid	Input invalid
DIN_SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
PCLK	Input invalid	Input valid	Input valid	Input invalid
D[23:0]	Input invalid	Input valid	Input valid	Input invalid
OSC, IM2, IM1,IM0	Input invalid	Input valid	Input valid	Input invalid
TEST3-1	Input invalid	Input valid	Input valid	Input invalid

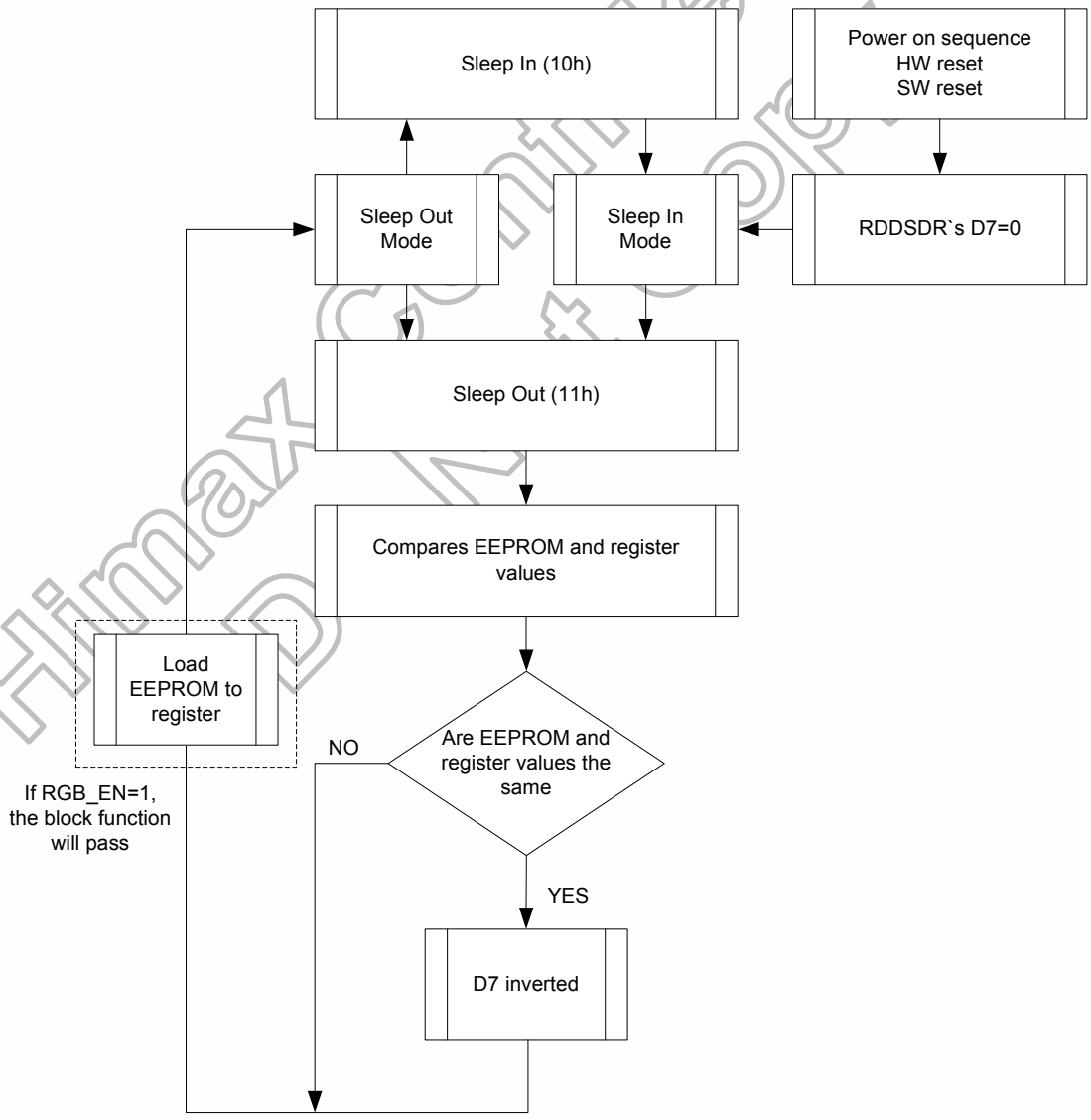
Table 5.9: Characteristics of input pins

5.11Sleep out – command and self-diagnostic functions of display module

5.11.1 Register loading detection

Sleep Out-command (See section “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are the same, there is an inverted (=increased by 1) bit, which is defined in section “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The bit used for this command is D7). If those both values are not the same, this bit (D7) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



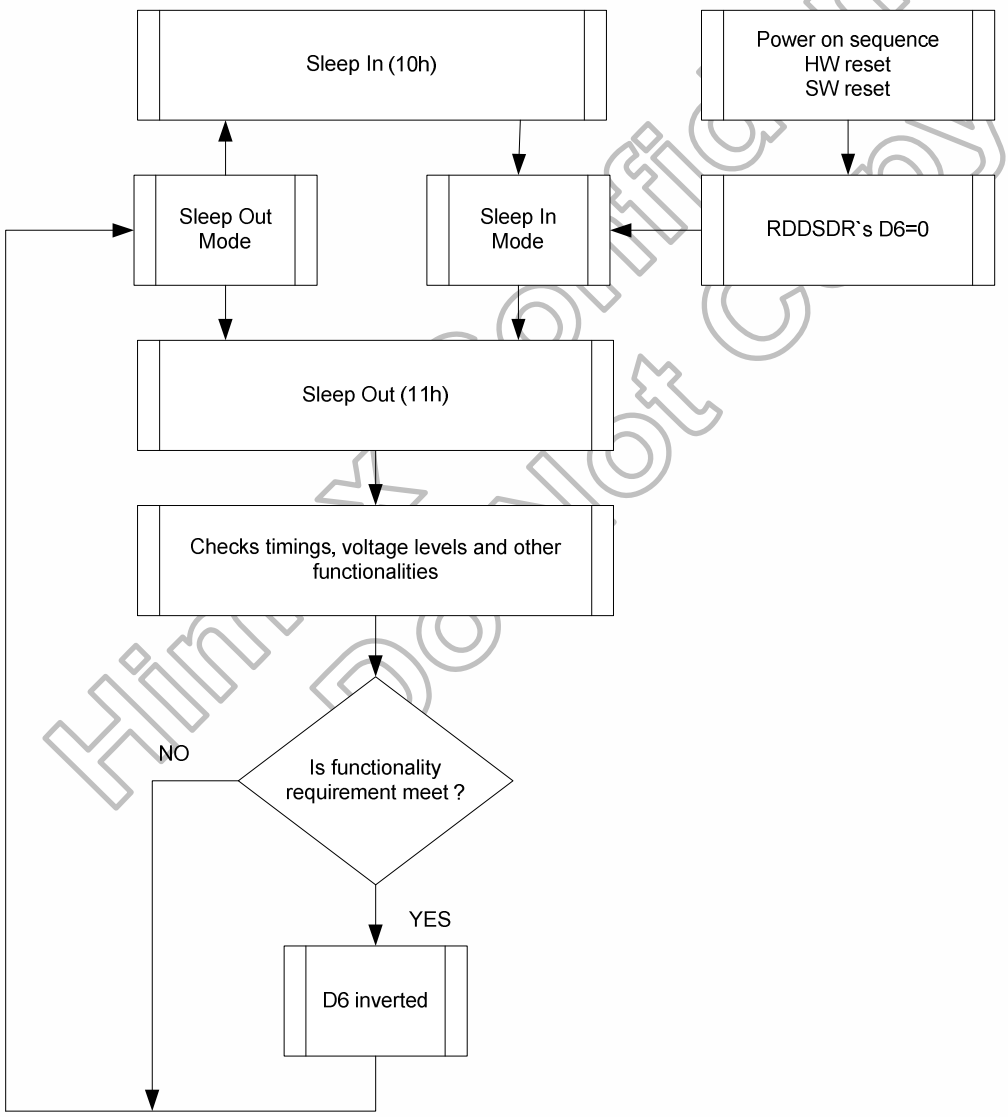
Note: There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module.

Figure 5.35: RDDSDR register loading detection flow

5.11.2 Functionality detection

Sleep Out-command (“Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in section 6.2.13 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5.36: Functionality detection flow

5.12Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

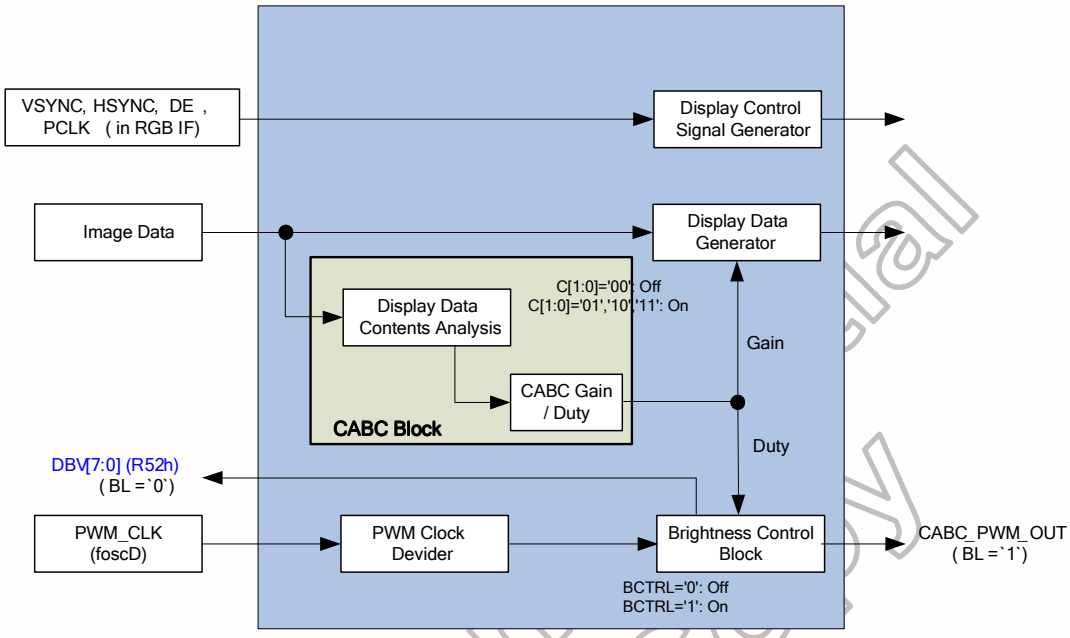
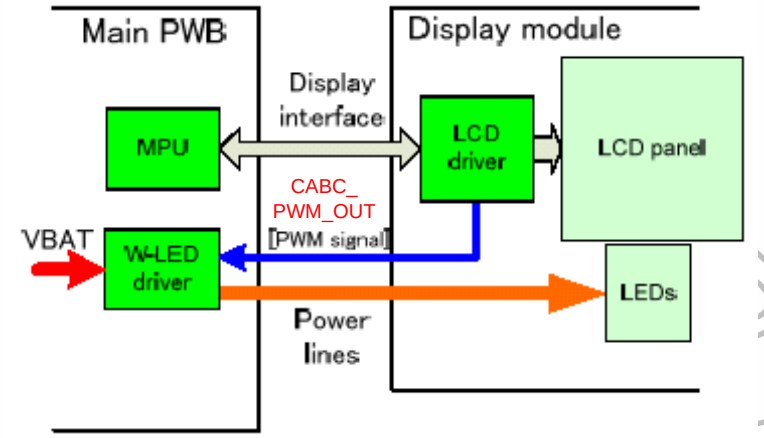


Figure 5.37: CABC block diagram

5.12.1 Module architectures

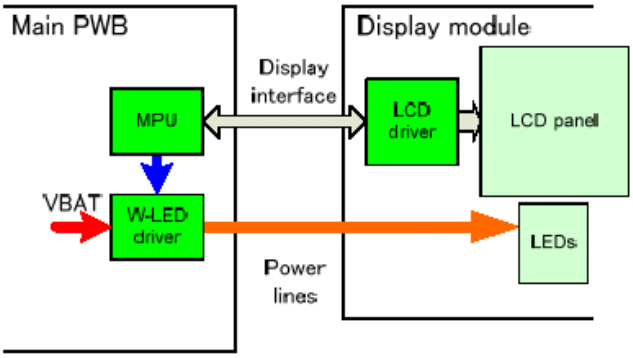
The HX8357-D00/D01 can support two module architectures for CABC operation. The **BL** bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- **Architecture I**



1. **BL** =`1` of R53h
2. LED backlight brightness for the display is controlled by external output "CABC_PWM_OUT".

- **Architecture II**



1. **BL** =`0` of R53h
2. LED backlight brightness data for the display is read with DBV[7:0] bits of R52h.
3. Read commands R52h should be synchronized with V-sync.

5.12.2 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness. The CABC_PWM_OUT output active polarity is defined by **INVPULS** bit of RC9h.

The CABC_PWM_OUT output period is controlled by **PWMDIV[2:0]** and **PWM_PERIOD[7:0]** bits of RC9h setting.

Ex: PWM CLK is 5.5MHz (period 180ns), PWMDIV=110(divide by 64),
and PWM_PERIOD=00h (the value is 0+1).
➔ CABC_PWM_OUT period = 180ns x 64 x (1x256) = 2.95 ms

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as DBV[7:0]/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period = 2.95 ms, and DBV[7:0](R51h) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM_OUT duty = 228 / 255 x 74% ≡ 66.16%. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.95ms, and the low-level of CABC_PWM_OUT = 1.00ms.

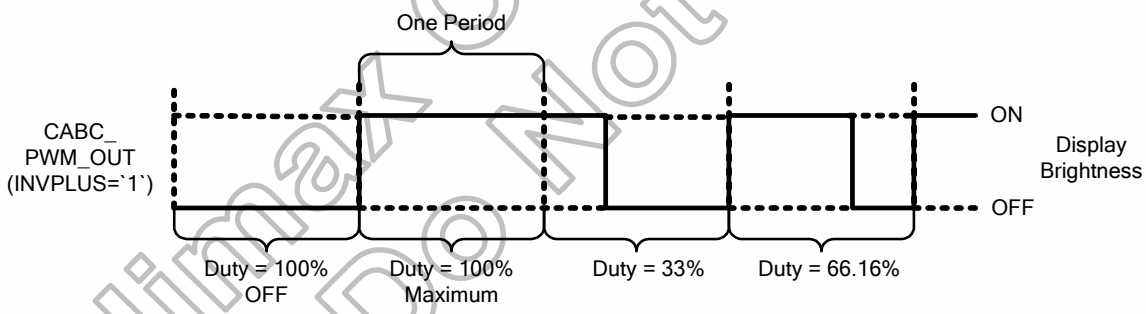


Figure 5.38: CABC_PWM_OUT output duty

When Architecture II module is used (**BL**='0') with the example below, the CABC_PWM_OUT is always output low (**INVPULS='1'**) and the DBV[7:0](R52h) will be read a value as 169_{DEC} (169/255≡ 66.27%).

5.12.3 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

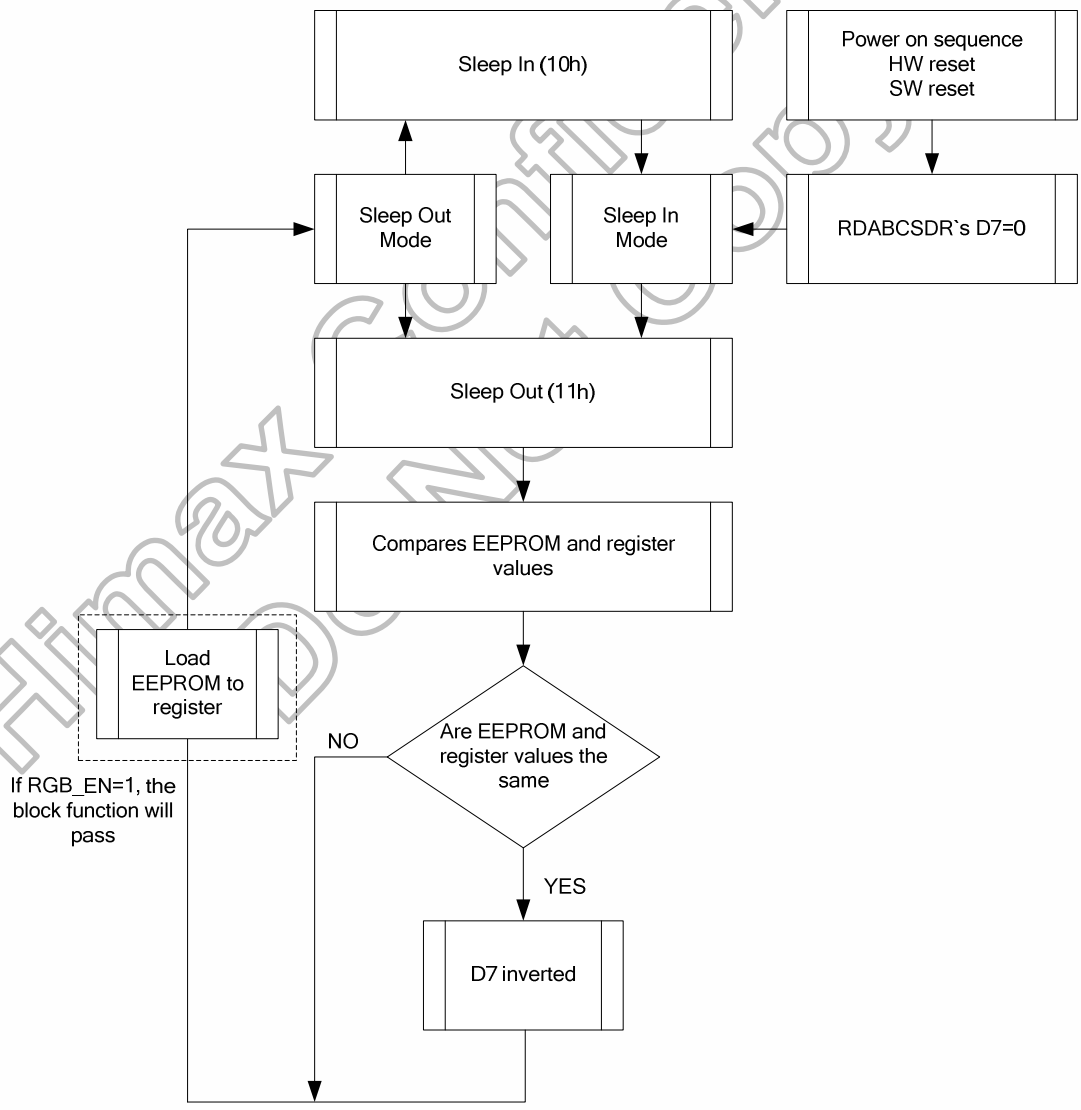
This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (**BCTRL='0'** of R53h), CABC minimum brightness setting is ignored. "**CMB[7:0],** Read CABC minimum brightness (R5Fh) "always read the setting value of "**CMB[7:0],** Write CABC minimum brightness (R5Eh)".

5.12.3.1 Register loading detection

Sleep Out command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: compares register and EEPROM values, 2nd step: loads EEPROM values to registers). If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command "Read Automatic Brightness Control Self-Diagnostic Result (68h)" (=RDABCSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).
The flow chart for this internal function is following:



Note: There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module

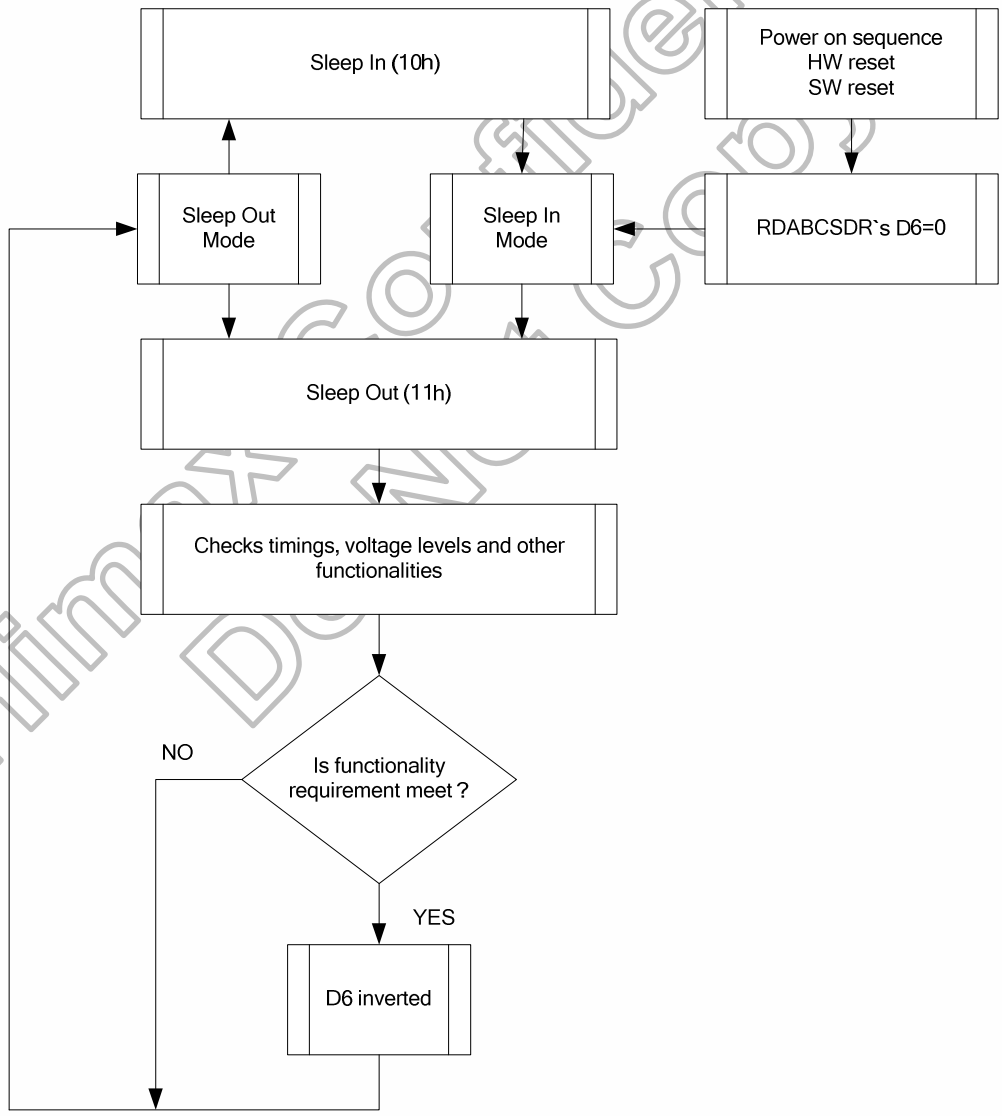
Figure 5.39: RDABCSDR register loading detection flow

5.12.3.2 Functionality detection

Sleep Out command (See section 6.2.15, Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If the functionality requirement is met, there is inverted (increased by 1) a bit, which defined in command “Read Automatic Brightness Control Self-Diagnostic Result (68h)” (=RDABCSDR) (The used bit of this command is D6). If the functionality requirement is not same, this bit (D6) is not inverted (=not increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDABCSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5.40: RDABCSDR functionality detection flow

5.12.4 Display dimming

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another to avoid flicker in the actual display module. This dimming function curve is the same in increment and decrement directions.

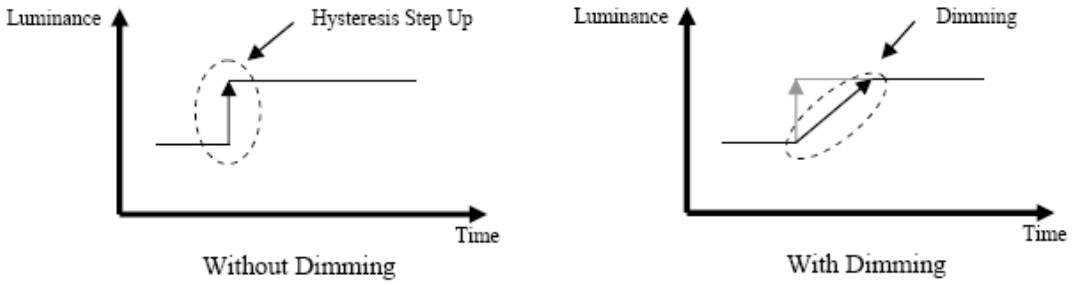


Figure 5.41: Dimming function

5.13OTP programing

5.13.1 OTP table

OTP_Index	Table_ Index	D7	D6	D5	D4	D3	D2	D1	D0
01	01	ID1[7:0]							
	02	ID2[7:0]							
	03	ID3[7:0]							
	04	ID1[7:0]							
	05	ID2[7:0]							
	06	ID3[7:0]							
	07	ID1[7:0]							
	08	ID2[7:0]							
	09	ID3[7:0]							
	0A	ID1[7:0]							
	0B	ID2[7:0]							
	0C	ID3[7:0]							
0D	0D	*	VCOM[6:0]						
	0E	*	VCOM[6:0]						
	0F	*	VCOM[6:0]						
	10	*	VCOM[6:0]						
12	12	*	*	*	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL
13	13	*	*	TRI	XDK		BT[2:0]		
	14	*	*	VRH[5:0]					
	15	*	*	NVRH[5:0]					
16	16	FS1[3:0]				FS0[3:0]			
18	18	SDO_EN	BYPASS	EPF[1:0]	*	*	*	RM	DM
	19	*	*	*	*	DPL	HSPL	VSPL	EPL
1A	1A	ZINV		I_NW[1:0]		*	*	N_NW[1:0]	
7F	7F	DDB1[7:0]							
	80	DDB2[7:0]							
	81	DDB3[7:0]							
	82	DDB4[7:0]							
83	83		VRP0[6:0]						
	84		VRP1[6:0]						
	85		VRP2[6:0]						
	:								
	A1		VRN14[6:0]						
	A2		VRN15[6:0]						
	A3	CGN[1:0]		CGN[1:0]		CGP[1:0]		CGP[1:0]	

5.13.2 OTP programming flow

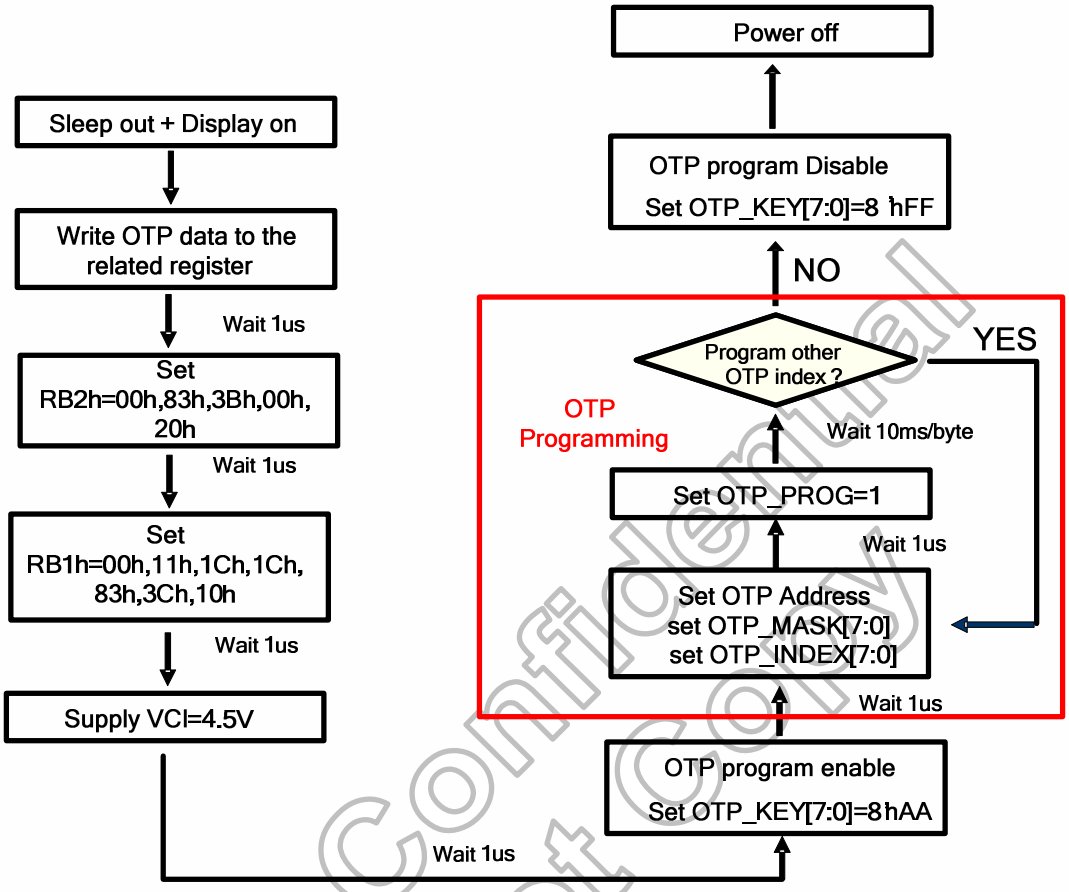


Figure 5.42: OTP programming sequence

6. Command Set

6.1Command set list

6.1.1 Standard command

(Hex)	Operation code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	MESSI_ENB '0'	MESSI_ENB '1'
00	NOP	0	1	↑	0	0	0	0	0	0	0	0	No Operation	-	Yes	
01	SWRESET	0	1	↑	0	0	0	0	0	0	0	1	Software Reset	-	Yes	
04	RDDIDIF	0	1	↑	0	0	0	0	0	1	0	1	Read Display Identification Information	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	ID1[7:0]								ID1	00h		
		1	↑	1	ID2[7:0]								ID2	00h		
		1	↑	1	ID3[7:0]								ID3	00h		
05	RDNUMPE	0	1	↑	0	0	0	0	0	1	0	1	Read Number of the Errors on DSI	-	Yes	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	P[7:0]								-	00h		
06	RDRED	0	1	↑	0	0	0	0	0	1	1	0	Read Red Colour	-	Yes	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	R7	R6	R5	R4	R3	R2	R1	R0	xx	00h		
07	RDGREEN	0	1	↑	0	0	0	0	0	1	1	1	Read Green Colour	-	Yes	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	G7	G6	G5	G4	G3	G2	G1	G0	xx	00h		
08	RDBLUE	0	1	↑	0	0	0	0	1	0	0	0	Read Blue Colour	-	Yes	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	00h		
0A	RDDPM	0	1	↑	0	0	0	0	1	0	1	0	Read display power mode	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	D7	D6	D5	D4	D3	D2	0	0	-	08h		
0B	RDDMADCTL	0	1	↑	0	0	0	0	1	0	1	1	Read display MADCTL	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	D7	D6	D5	D4	D3	D2	0	0	-	00h		
0C	RDDCOLMOD	0	1	↑	0	0	0	0	1	1	0	0	Read display pixel format	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	-	D6	D5	D4	-	D2	D1	D0	-	07h		
0D	RDDIM	0	1	↑	0	0	0	0	1	1	0	1	Read display image mode	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	D7	D6	D5	0	0	D2	D1	D0	-	00h		
0E	RDDSM	0	1	↑	0	0	0	0	1	1	1	0	Read display signal mode	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	D7	D6	0	0	0	0	0	D0	-	00h		
0F	RDDSDR	0	1	↑	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	X	Dummy read	-		
		1	↑	1	D7	D6	0	0	0	0	0	D0	-	00h		
10	SLPIN	0	1	↑	0	0	0	1	0	0	0	0	Sleep In	-	Yes	
11	SLPOUT	0	1	↑	0	0	0	1	0	0	0	1	Sleep Out	-	Yes	

(Hex)	Operation code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	MESSI_ENB '0'	MESSI_ENB '1'
12	PTLON	0	1	↑	0	0	0	1	0	0	1	0	Partial Mode On	-	Yes	
13	NORON	0	1	↑	0	0	0	1	0	0	1	1	Normal display mode on	-	Yes	
20	INVOFF	0	1	↑	0	0	1	0	0	0	0	0	Display inversion off	-	Yes	
21	INVON	0	1	↑	0	0	1	0	0	0	0	1	Display inversion on	-	Yes	
22	ALLPOFF	0	1	↑	0	0	1	0	0	0	1	0	All Pixel Off	-	Yes	
23	ALLPON	0	1	↑	0	0	1	0	0	0	1	1	All Pixel On	-	Yes	
26	GAMSET	0	1	↑	0	0	1	0	0	0	1	1	Gamma Set	-	Yes	
		0	1	↑	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	Gamma Curve	01h		
28	DISPOFF	0	1	↑	0	0	1	0	1	0	0	0	Display off	-	Yes	
29	DISPON	0	1	↑	0	0	1	0	1	0	0	1	Display on	-	Yes	
2A	CASET	0	1	↑	0	0	1	0	1	0	1	0	Column Address Set	-	Yes	
		1	1	↑	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Column address start	00h		
		1	1	↑	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Column address start	00h		
		1	1	↑	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Column address end	01h		
		1	1	↑	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Column address end	67h		
2B	PASET	0	1	↑	0	0	1	0	1	0	1	1	Row address set	-	Yes	
		1	1	↑	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Row address start	00h		
		1	1	↑	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Row address start	00h		
		1	1	↑	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Row address end	02h		
		1	1	↑	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	Row address end	7Fh		
2C	RAMWR	0	1	↑	0	0	1	0	1	1	0	0	Memory Write	-	Yes	
		1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	Write data	-		
		1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Write data	-		
		1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	Write data	-		
2E	RAMRD	0	1	↑	0	0	1	0	1	1	1	0	Memory read	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	D17	D16	D15	D14	D13	D12	D11	D10	Read data	-		
		1	↑	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Read data	-		
		1	↑	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-		
30	PLTAR	0	1	↑	0	0	1	1	0	0	0	0	Partial Area	-	Yes	
		1	1	↑	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	Start row	00h		
		1	1	↑	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	Start row	00h		
		1	1	↑	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	End row	02h		
		1	1	↑	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	End row	7Fh		

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	MESSI_ENB '0'	MESSI_ENB '1'
33	VSCRDEF	0	1	↑	0	0	1	1	0	0	1	1	Vertical scrolling definition	-	Yes	
		1	1	↑	TFA[15:8]								-	00h		
		1	1	↑	TFA[7:0]								-	00h		
		1	1	↑	VSA[15:8]								-	02h		
		1	1	↑	VSA[7:0]								-	80h		
		1	1	↑	BFA[15:8]								-	00h		
		1	1	↑	BFA[7:0]								-	00h		
34	TEOFF	0	1	↑	0	0	1	1	0	1	0	0	Tearing Effect Line OFF	-	Yes	
35	TEON	0	1	↑	0	0	1	1	0	1	0	1	Tearing Effect Line ON	-	Yes	
36	MADCTL	0	1	↑	0	0	1	1	0	1	1	0	Memory Access Control	-	Yes	
		1	1	↑	B7	B6	B5	B4	B3	B2	0	0	-	00h		
37	VSCRSADD	0	1	↑	0	0	1	1	0	1	1	1	Vertical scrolling start address	-	Yes	
		1	1	↑	VSP[15:8]								-	00h		
		1	1	↑	VSP[7:0]								-	00h		
38	IDMOFF	0	1	↑	0	0	1	1	1	0	0	0	Idle mode off	-	Yes	
39	IDMON	0	1	↑	0	0	1	1	1	0	0	1	Idle mode on	-	Yes	
3A	COLMOD	0	1	↑	0	0	1	1	1	0	1	0	-	-	Yes	
		1	1	↑	0	D6	D5	D4	0	D2	D1	D0	-	07h		
3C	RAMWRCON	0	1	↑	0	0	1	1	1	1	0	0	Memory write	-	Yes	
		1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	-	-		
		1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	-	-		
		1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-		
3E	RAMRDCON	0	1	↑	0	0	1	1	1	1	1	0	Memory read	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	D17	D16	D15	D14	D13	D12	D11	D10	-	-		
		1	↑	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	-	-		
		1	↑	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-		
44	TESL	0	1	↑	0	1	0	0	0	1	0	0	TESL	-	No	Yes
		1	1	↑	TELINE[15:8](8'b0)								-	00h		
		1	1	↑	TELINE[7:0](8'b0)								-	00h		
45	GETSCAN	0	1	↑	0	1	0	0	0	1	0	1	Reture the current scanline SLN[15:0]	-	No	Yes
		1	1	↑	SLN[15:8]								-	00h		
		1	1	↑	SLN[7:0]								-	00h		
51	WRDISBV	0	1	↑	0	1	0	1	0	0	0	1	Write Display Brightness	-	Yes	
		1	1	↑	DBV[7:0]								-	00h		
52	RDDISBV	0	1	↑	0	1	0	1	0	0	1	0	Read Display Brightness Value	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	DBV[7:0]								-	00h		
53	WRCTRLD	0	1	↑	0	1	0	1	0	0	1	1	Write CTRL Display	-	Yes	
		1	1	↑	0	0	BCTRL	0	DD	BL	0	0		00h		
54	RDCTRLD	0	1	↑	0	1	0	1	0	0	1	1	Read Control Value Display	-	Yes	
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	0	0	BCTRL	0	DD	BL	0	0	-	00h		
55	WRCABC	0	1	↑	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control	-	Yes	
		1	1	↑	0	0	0	0	0	0	CABC[1:0]		-	00h		

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	MESSI_ENB '0'	MESSI_ENB '1'
56	RDCABC	0	1	↑	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	0	0	0	0	0	0	C1	C0	-	00h		
5E	WRCABCMB	0	1	↑	0	1	0	1	1	1	1	0	Write CABC minimum brightness	-		Yes
		1	1	↑	CMB[7:0]								-	00h		
5F	RDCABCMB	0	1	↑	0	1	0	1	1	1	1	1	Read CABC minimum brightness	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	CMB[7:0]								-	00h		
68	RDABCSDR	0	1	↑	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	-	-		
		1	↑	1	D[7:6]		0	0	0	0	0	0	-	00h		
70	RDBWLB	0	1	↑	0	1	1	1	0	0	0	0	Read Black/White Low Bits	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	-	-		
71	RDBkx	0	1	↑	0	1	1	1	0	0	0	1	Read Bkx	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	-	-		
72	RDBky	0	1	↑	0	1	1	1	0	0	1	0	Read Bky	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	-	-		
73	RDWx	0	1	↑	0	1	1	1	0	0	1	1	Read Wx	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	-	-		
74	RDWy	0	1	↑	0	1	1	1	0	1	0	0	Read Wy	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	-	-		
75	RDRGLB	0	1	↑	0	1	1	1	0	1	0	1	Read Red/Green Low Bits	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Rx1	Rx0	Ry1	Rx0	Gx1	Gx0	Gy1	Gy0	-	-		
76	RDRx	0	1	↑	0	1	1	1	0	1	1	0	Read Rx	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	-	-		
77	RDRy	0	1	↑	0	1	1	1	0	1	1	1	Read Ry	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	-	-		
78	RDGx	0	1	↑	0	1	1	1	1	0	0	0	Read Gx	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	-	-		
79	RDRy	0	1	↑	0	1	1	1	1	0	0	1	Read Gy	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	-	-		
7A	RDBALB	0	1	↑	0	1	1	1	1	0	1	0	Read Biue/AColour Low Bits	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Bx1	Bx0	By1	Bx0	Ax1	Ax0	Ay1	Ay0	-	-		
7B	RDBx	0	1	↑	0	1	1	1	1	0	1	1	Read Bx	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	-	-		
7C	RDBy	0	1	↑	0	1	1	1	1	1	0	0	Read By	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	By9	By8	By7	By6	By5	By4	By3	By2	-	-		

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	MESSI_ENB '0'	MESSI_ENB '1'
7D	RDAx	0	1	↑	0	1	1	1	1	1	0	1	Read Ax	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	-	-		
7E	RDAy	0	1	↑	0	1	1	1	1	1	1	0	Read Ay	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	-	-		
A1	Read_DDB_start	0	1	↑	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-		
		1	↑	1	x	x	x	x	x	x	x	x	-	00h		
		1	↑	1	x	x	x	x	x	x	x	x	-	00h		
		1	↑	1	x	x	x	x	x	x	x	x	-	00h		
		1	↑	1	x	x	x	x	x	x	x	x	-	00h		
		1	↑	1	1	1	1	1	1	1	1	1	0xFF	FFh		
A8	Read_DDB_continue	0	1	↑	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-		Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	00h		
		1	↑	1	x	x	x	x	x	x	x	x	-	00h		
		1	↑	1	x	x	x	x	x	x	x	x	-	00h		
		1	↑	1	x	x	x	x	x	x	x	x	-	00h		
AA	RDFCS	0	1	↑	1	0	1	0	1	1	0	0	Read First Checksum			Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	00h		
		1	↑	1	FCS[7:0]									00h		
AF	RDCCS	0	1	↑	1	0	1	0	1	1	0	0	Read Continue Checksum			Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	00h		
		1	↑	1	CCS[7:0]									00h		
DA	RDID1	0	↑	1	1	1	0	1	1	0	1	0	Read ID1	-		Yes
		1	1	↑	x	x	x	x	x	x	x	x	Dummy read	-		
		1	1	↑	module's manufacturer[7:0]								-	00h		
DB	RDID2	0	↑	1	1	1	0	1	1	0	1	1	Read ID2	-		Yes
		1	1	↑	x	x	x	x	x	x	x	x	Dummy read	-		
		1	1	↑	LCD module/driver version [7:0]								-	80h		
DC	RDID3	0	↑	1	1	1	0	1	1	1	0	0	Read ID3	-		Yes
		1	1	↑	x	x	x	x	x	x	x	x	Dummy read	-		
		1	1	↑	LCD module/driver ID[7:0]								-	00h		

Note: (1) Undefined commands are treated as NOP (00h) command.

6.1.2 User define command list table

(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
B0	SETOSC	0	↑	1	-	1	0	1	1	0	0	0	0	Set Internal Oscillator
		1	↑	1	-	I_UADJ[3:0]				N_UADJ[3:0]				
		1	↑	1	-	-	-	-	-	-	-	-	OSC_EN	
B1	SETPOWER	0	↑	1	-	1	0	1	1	0	0	0	1	Set power control
		1	↑	1	-	-	-	-	-	-	-	-	DP_STB	
		1	↑	1	-	-	-	TRI	XDK	-	BT[2:0]			
		1	↑	1	-	-	-	VRH[5:0]						
		1	↑	1	-	-	-	NVRH[5:0]						
		1	↑	1	-	GAS EN	-	-	-	-	AP[2:0]			
		1	↑	1	-	FS1[3:0]					FS0[3:0]			
		1	↑	1	-	-	VCOMG	1	PON	DK	0	0	STB	
B2	SETDISPLAY	0	↑	1	-	1	0	1	1	0	0	1	0	Set Display control
		1	↑	1	-	-	-	-	-	ISC[3:0]				
		1	↑	1	-	PT[1:0]		-	-	-	-	PTG	REF	
		1	↑	1	-	-	-	NL[5:0]						
		1	↑	1	-	-	SCN[6:0]							
		1	↑	1	-	-	-	GON	DTE	D[1:0]		-	-	
B3	SETRGB	0	↑	1	-	1	0	1	1	0	0	1	1	Set RGB I/F
		1	↑	1	-	SDO_ENB	BYPASS	EPF[1:0]		-	-	RM	DM	
		1	↑	1	-	-	-	-	-	DPL	HSPL	VSPL	EPL	
		1	↑	1	-	RCM	HBP[5:0]							
		1	↑	1	-		VBP[5:0]							
B4	SETCYC	0	↑	1	-	1	0	1	1	0	1	0	0	Set Display cycle
		1	↑	1	-	ZINV	-	I_NW[1:0]		-	-	N_NW[1:0]		
		1	↑	1	-	-	RTN[6:0]							
		1	↑	1	-	-	-	-	-	OSC_DIV2	-	DIV[1:0]		
		1	↑	1	-	N_DUM[7:0]								
		1	↑	1	-	I_DUM[7:0]								
		1	↑	1	-	GDON[7:0]								
		1	↑	1	-	GDOF[7:0]								
B5	SETBGP	0	↑	1	-	1	0	1	1	0	1	0	1	Set BGP Voltage
		1	↑	1	-	-	-	-	-	VREF[3:0]				
		1	↑	1	-	-	-	-	-	NVREF[3:0]				
		1	↑	1	-	VPP[2:0]			-	-	VVDH[2:0]			
B6	SETVCOM	0	↑	1	-	1	0	1	1	0	1	1	0	Set VCOM voltage
		1	↑	1	-	-	VCOM[6:0]							
		1	1	↑	-	-	-	-	-	-	VCOM_OTP_TIMES[2:0]			
B7	SETOTP	0	↑	1	-	1	0	1	1	0	1	1	1	Set OTP
		1	↑	1	-	OTP_KEY[7:0]								
		1	↑	1	-	OTP_MASK[7:0]								
		1	↑	1	-	OTP_INDEX[7:0]								
		1	↑	1	-	LOAD_DIS	VPP_EN	OTP_POR	OTP_PWE	OTP_PTM[1:0]		VPP_SEL	OTP_PROG	
		1	1	↑	-	OTP_DOUT[7:0](8'hFF)								
B9	SETEXTC	0	↑	1	-	1	0	1	1	1	0	0	1	Enter extention command
		1	↑	1	-	1	1	1	1	1	1	1	1	
		1	↑	1	-	1	0	0	0	0	0	1	1	
		1	↑	1	-	0	1	0	1	0	1	1	1	

(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
C1	SETDGC	0	↑	1	-	1	1	0	0	0	0	0	1	Set Digital Gamma Correction
		1	↑	1	-	-	-	-	-	-	-	-	DGC_EN	
		1	↑	1	-	DGC_LUT_R00[7:0]								
		1	↑	1	-	:								
		1	↑	1	-	DGC_LUT_R32[7:0]								
		1	↑	1	-	DGC_LUT_G00[7:0]								
		1	↑	1	-	:								
		1	↑	1	-	DGC_LUT_G32[7:0]								
		1	↑	1	-	DGC_LUT_B00[7:0]								
		1	↑	1	-	:								
		1	↑	1	-	DGC_LUT_B32[7:0]								
C0	SETSTBA	0	↑	1	-	1	1	0	0	0	0	0	0	Set Source option
		1	↑	1	-	N/P_OPON[7:0]								
		1	↑	1	-	I/PI_OPON[7:0]								
		1	↑	1	-	STBA[15:8]								
		1	↑	1	-	STBA[7:0]								
		1	↑	1	-	GENON[7:0]								
C3	SETID	0	↑	1	-	1	1	0	0	0	0	1	1	Set ID
		1	↑	1	-	ID1[7:0]								
		1	↑	1	-	ID2[7:0]								
		1	↑	1	-	ID3[7:0]								
		1	1	↑	-	-	-	-	-	-	ID_OTP_TIMES[2:0]			
C4	SET DDB	0	↑	1	-	1	1	0	0	0	1	0	0	SET DDB
		1	↑	1	-	DDB1[7:0]								
		1	↑	1	-	DDB2[7:0]								
		1	↑	1	-	DDB3[7:0]								
		1	↑	1	-	DDB4[7:0]								
C9	SETCABC	0	↑	1	-	1	1	0	0	1	0	0	1	SET CABC
		1	↑	1	-	BC_CTL	PWMDIV[2:0]			1	1	INVPLUS	1	
		1	↑	1	-	PWM_PERIOD[7:0]								
CC	SETPANEL	0	↑	1	-	1	1	0	0	1	1	0	0	Set Panel characteristics
		1	↑	1	-	-	-	-	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	

(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
E0	SETGAMMA	0	↑	1	-	1	1	1	0	0	0	0	0	Set Gamma
		1	↑	1	-	-	VRP0[6:0]							Set Gamma
		1	↑	1	-	-	VRP1[6:0]							
		1	↑	1	-	-	VRP2[6:0]							
		1	↑	1	-	-	VRP3[6:0]							
		1	↑	1	-	-	VRP4[6:0]							
		1	↑	1	-	-	VRP5[6:0]							
		1	↑	1	-	-	VRP6[6:0]							
		1	↑	1	-	-	VRP7[6:0]							
		1	↑	1	-	-	VRP8[6:0]							
		1	↑	1	-	-	VRP9[6:0]							
		1	↑	1	-	-	VRP10[6:0]							
		1	↑	1	-	-	VRP11[6:0]							
		1	↑	1	-	-	VRP12[6:0]							
		1	↑	1	-	-	VRP13[6:0]							
		1	↑	1	-	-	VRP14[6:0]							
		1	↑	1	-	-	VRP15[6:0]							
		1	↑	1	-	-	VRN0[6:0]							
		1	↑	1	-	-	VRN1[6:0]							
		1	↑	1	-	-	VRN2[6:0]							
		1	↑	1	-	-	VRN3[6:0]							
		1	↑	1	-	-	VRN4[6:0]							
		1	↑	1	-	-	VRN5[6:0]							
		1	↑	1	-	-	VRN6[6:0]							
		1	↑	1	-	-	VRN7[6:0]							
		1	↑	1	-	-	VRN8[6:0]							
		1	↑	1	-	-	VRN9[6:0]							
		1	↑	1	-	-	VRN10[6:0]							
		1	↑	1	-	-	VRN11[6:0]							
		1	↑	1	-	-	VRN12[6:0]							
		1	↑	1	-	-	VRN13[6:0]							
		1	↑	1	-	-	VRN14[6:0]							
		1	↑	1	-	-	VRN15[6:0]							
		1	↑	1	-	CGN1[1:0]		CGN0[1:0]		CGP1[1:0]		CGP0[1:0]		
		1	↑	1	-								GMA_RELOAD	
E9	SETIMAGEI	0	1	↑	-	1	1	1	0	1	0	0	1	Set Image type
		1	1	↑	PWM2_EN	-	-	DITH_EN	YUV_EN	-	-	-	DB_EN	
EA	SETMESSI	0	1	↑	-	1	1	1	0	1	0	1	0	Set command type
		1	1	↑	-	-	-	-	-	-	-	SPI_DCX_SEL	MESSI_ENB	
EB	SETCOLOR	0	1	↑	-	1	1	1	0	1	0	1	1	Set Color
		1	1	↑	-	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	
		1	1	↑	-	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	
		1	1	↑	-	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	
		1	1	↑	-	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	
		1	1	↑	-	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	
		1	1	↑	-	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	
		1	1	↑	-	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	
		1	1	↑	-	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	
		1	1	↑	-	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	
		1	1	↑	-	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	
		1	1	↑	-	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	
		1	1	↑	-	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	
		1	1	↑	-	By9	By8	By7	By6	By5	By4	By3	By2	
		1	1	↑	-	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	
		1	1	↑	-	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	

(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
FE	SETREADINDEX	0	1	↑	-	1	1	1	1	1	1	1	0	SET SPI READ Command Address
		1	1	↑	-	CMD_ADD[7:0]								
FF	GETSPIREAD	0	1	↑	-	1	1	1	1	1	1	1	1	Read SPI Command Data
		1	↑	1	-	CMD_DATA1[7:0]								
		1	↑	1	-	:								
		1	↑	1	-	CMD_DATAn[7:0]								

6.2Command description

6.2.1 NOP

00 H	NOP (No Operation)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write as described in RAMWR (Memory Write) or RAMRD (Memory Read) command.												
Restriction	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Booster Off / Yes												
Default	Status / Default Value Power On Sequence / N/A S/W Reset / N/A H/W Reset / N/A												
Flow Chart	-												

6.2.2 Software reset (01h)

01 H	SWRESET (Software Reset)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately. Note: The GRAM contents are unaffected by this command.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during this 5m sec. If SW Reset is applied during Sleep Out mode, it will be necessary to wait 120m sec before sending Sleep Out command. SW Reset command cannot be sent during Sleep Out sequence.												

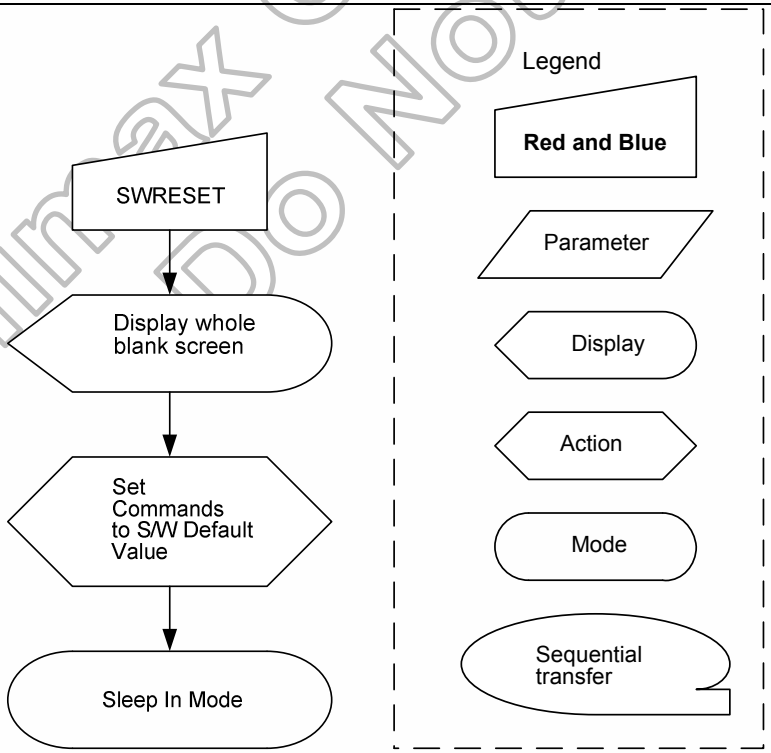
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



6.2.3 Read display identification information (04h)

04 H	RDDIDIF (Read Display Identification Information)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	0	0	04
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-
Description	This read byte returns 24-bit display identification information. The 1st parameter is dummy data. The 2nd parameter: LCD module's manufacturer ID. The 3rd parameter: LCD module/driver version ID. The 4th parameter: LCD module/driver ID. **Note:** Commands RDID1/2/3(DAh, DBh and DCh) read data correspond to the parameters 2, 3, 4 of the command 04h, respectively.												
Restriction													

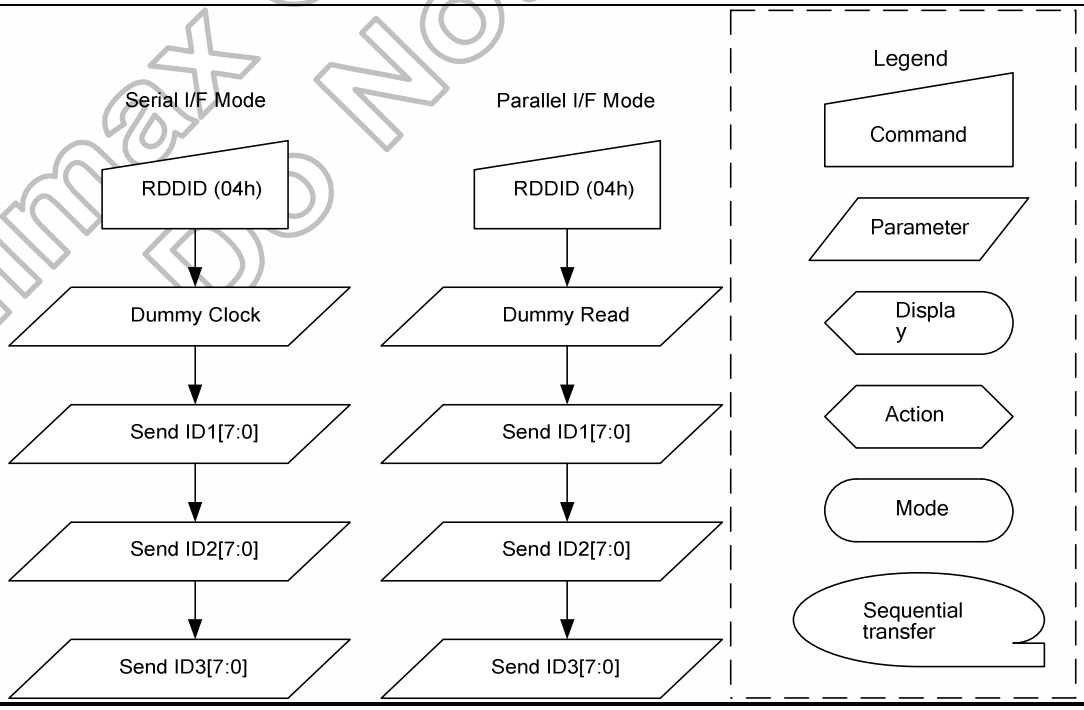
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.4 RDNUMPE: Read Number of the Errors on DSI (05h)

05h	RDNUMPE (Read Number of the Errors on DSI)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	0	1	05
	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
1st parameter	1	↑	1	-	P7	P6	P5	P4	P3	P2	P1	P0	xx
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6..0] bits. P[7..0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (= The read function is completed).												
Restriction	-												

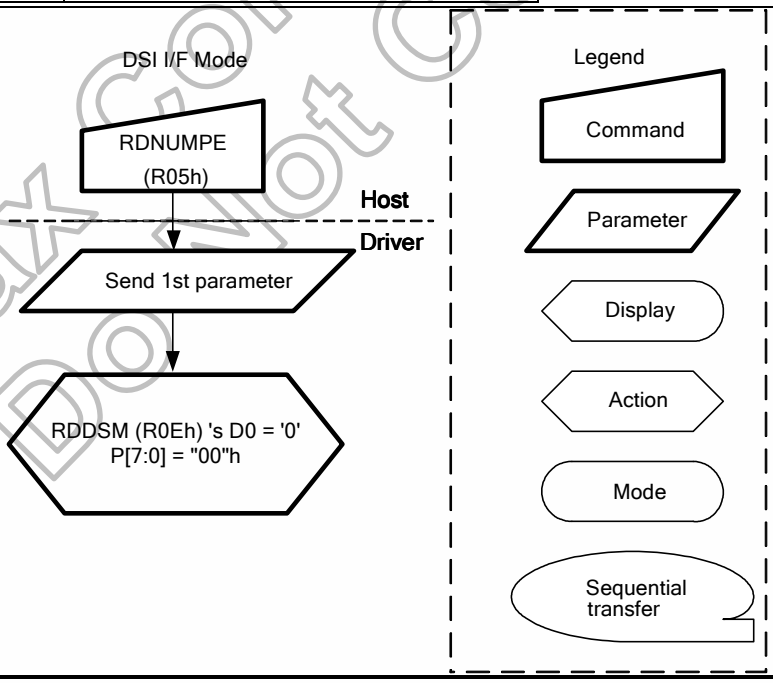
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.5 Read red color (06h)

06 H	RDRED (Read Red Color)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	1	0	06
1st parameter	1	1	↑	-	-	-	R5	R4	R3	R2	R1	R0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16 bit format: R5 is MSB and R1 is LSB. R0 is set to '0'. 18 bit format: R5 is MSB and R0 is LSB.												
Restriction	When BYPASS='0', this command is working as a NOP (00h) command.												

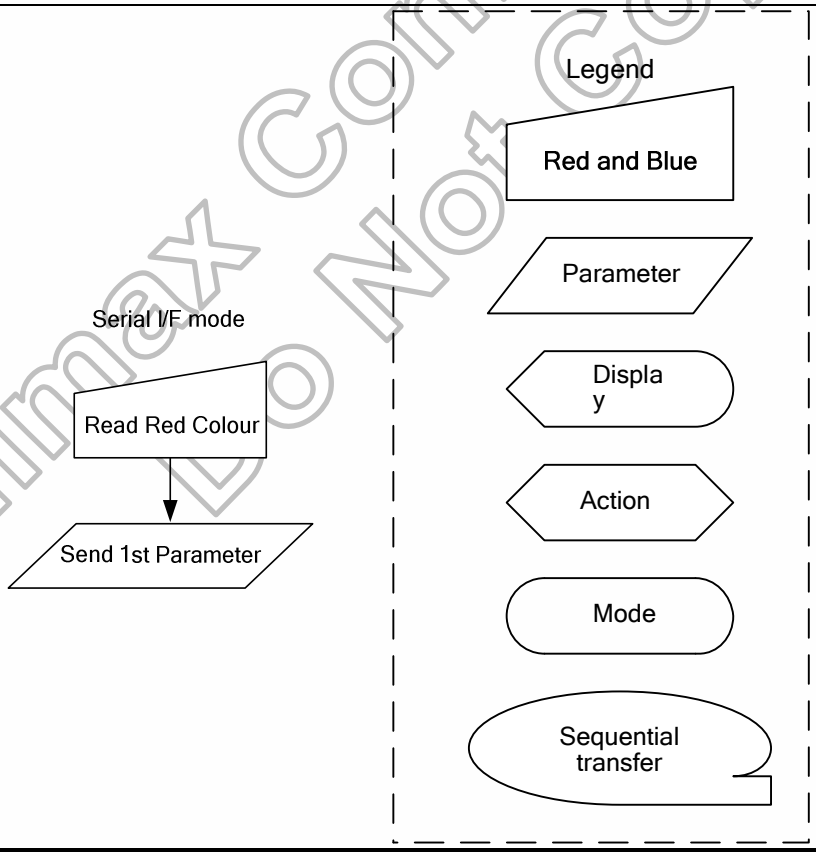
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.6 Read green color (07h)

07 H	RDGREEN (Read Green Color)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	1	1	07
1st parameter	1	1	↑	-	-	-	G5	G4	G3	G2	G1	G0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16, 18 bit formats: G5 is MSB and G0 is LSB.												
Restriction	When BYPASS='0' is disabled, this command is working as a NOP (00h) command.												

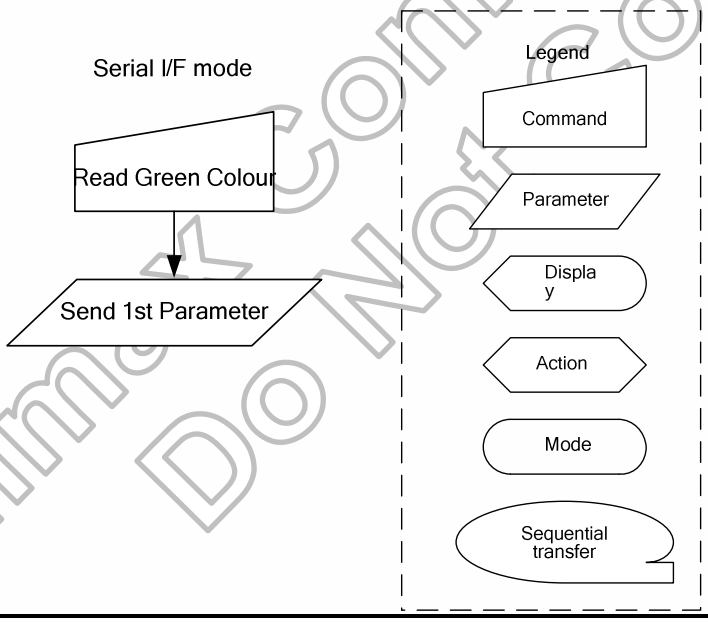
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.7 Read blue color (08h)

08 H	RDBLUE (Read Blue Color)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	0	0	08
1st parameter	1	1	↑	-	-	-	B5	B4	B3	B2	B1	B0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16 bit format: B5 is MSB and B1 is LSB. B0 is set to '0'. 18 bit format: B5 is MSB and B0 is LSB.												
Restriction	When BYPASS='0' is disabled, this command is working as a NOP (00h) command.												

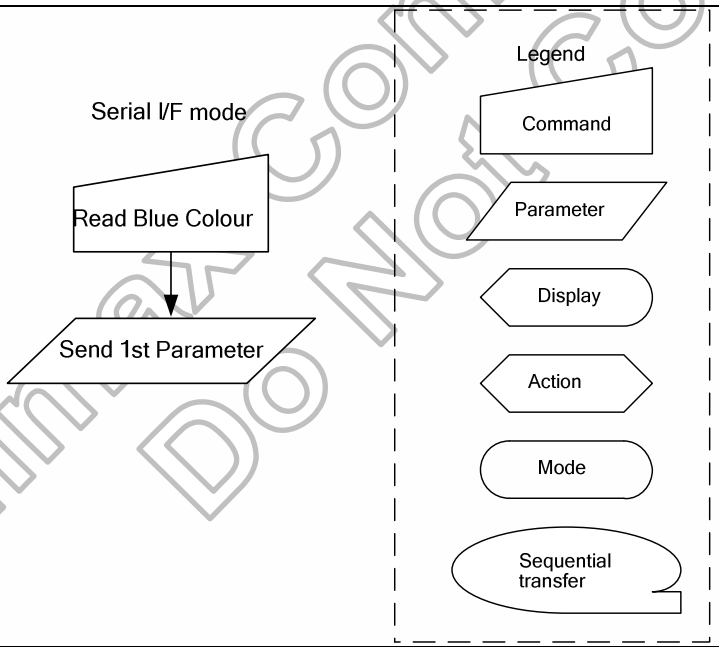
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.8 Read display power mode (0Ah)

0A H	RDDPM (Read Display Power Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	1	0	0A
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Booster Voltage Status	-
D6	Idle Mode On/Off	-
D5	Partial Mode On/Off	-
D4	Sleep In/Out	-
D3	Display Normal Mode On/Off	-
D2	Display On/Off	-
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D7 – Booster Voltage Status
'0' = Booster Off or has a fault.
'1' = Booster On and working OK (Meets display supplier's optical requirements).
Bit D6 – Idle Mode On/Off
'0' = Idle Mode Off.
'1' = Idle Mode On.
Bit D5 – Partial Display Mode On/Off
'0' = Partial Mode Off.
'1' = Partial Mode On.
Bit D4 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit D3 – Normal Display Mode On/Off
'0' = Display Normal Mode Off.
'1' = Display Normal Mode On.
Bit D2 – Display On/Off
'0' = Display is Off.
'1' = Display is On.
Bit D1 – Not Defined
This bit is not applicable for this project, so it is set to '0'.
Bit D0 – Not Defined
This bit is not applicable for this project, so it is set to '0'.

Restrictions

-

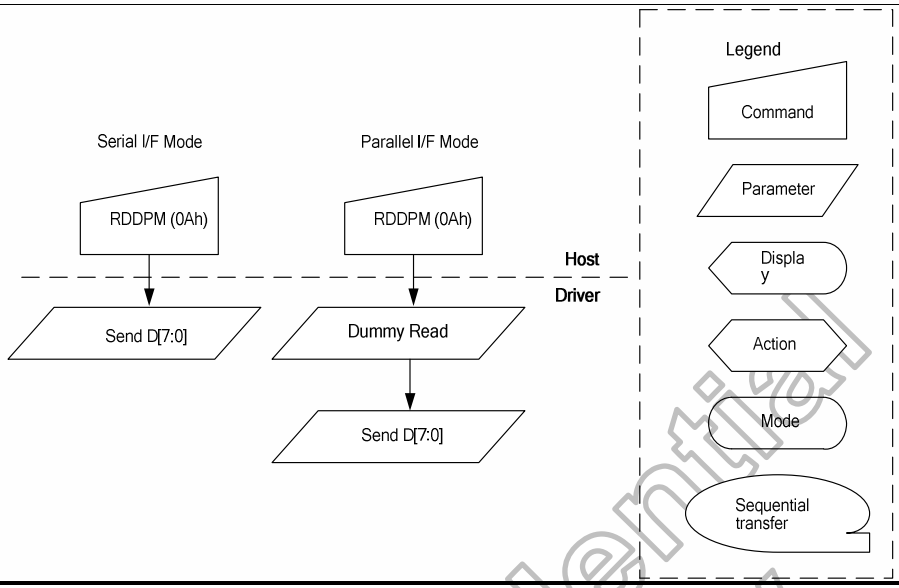
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



6.2.9 Read display MADCTL (0Bh)

0B H	RDDMADCTL (Read Display MADCTL)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	1	1	0B
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	-
D6	Column Address Order	-
D5	Page/Column Order	-
D4	Line Address Order	-
D3	RGB/BGR Order	-
D2	Display Data Latch Order	-
D1	Switching between Segment outputs and RAM	Set to '0'
D0	Switching between Common outputs and RAM	Set to '0'

Bit D7 – Page Address Order
'0' = Top to Bottom (When MADCTL B7(MY) = '0').
'1' = Bottom to Top (When MADCTL B7(MY) ='1').
Bit D6 – Column Address Order
'0' = Left to Right (When MADCTL B6(MX) = '0').
'1' = Right to Left (When MADCTL B6(MX) = '1').
Bit D5 –Page / Column Order
'0' = Normal Mode (When MADCTL B5(MV) = '0').
'1' = Reverse Mode (When MADCTL B5(MV) = '1').
Bit D4 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4(ML) = '0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4(ML) = '1').
Bit D3 – RGB/BGR Order
'0' = RGB (When MADCTL B3 = '0').
'1' = BGR (When MADCTL B3 = '1').
Note: For bits D4, D3 and D2 also refer to 6.2.32 Memory Access Control (R36h)
Bit D2 – Display Data Latch Order
'0' = LCD Refresh Left to Right (When MADCTL B2 = '0').
'1' = LCD Refresh Right to Left (When MADCTL B2 = '1').
Bit D1 – Switching Between Segment Outputs and RAM
This bit is not applicable for this project, so it is set to '0'.
Bit D0 – Switching Between Common Outputs and RAM
This bit is not applicable for this project, so it is set to '0'.

Restrictions

-

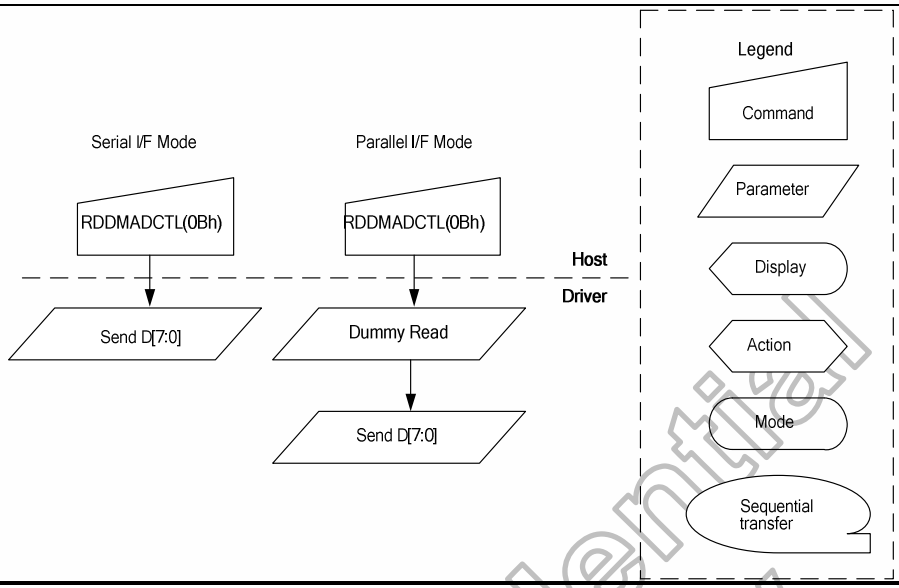
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No Change
H/W Reset	00h

Flow Chart



6.2.10 Read display pixel format (0Ch)

0C H	RDDCOLMOD (Read Display COLMOD)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	0	0C
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Reserved	Set to '0'
D6	DPI Interface Pixel format	-
D5		-
D4		-
D3	Reserved	Set to '0'
D2	DBI Interface Pixel format	-
D1		-
D0		-

Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition
Bits D2, D1, D0 – DSI, DBI Interface Colour Pixel Format Definition.

Interface Colour Format	D6/D2	D5/D1	D4/D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 bit/pixel	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
24 bit/pixel	1	1	1

If a particular interface, either DSI, DBI or DPI, is not used then the corresponding bits in the

Restrictions

-

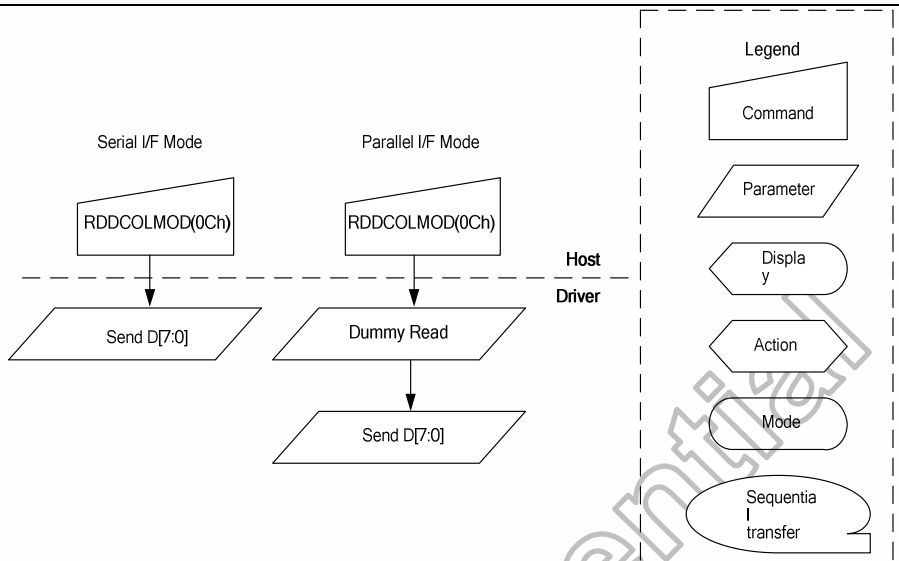
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	18-bit/pixel
S/W Reset	18-bit/pixel
H/W Reset	18-bit/pixel

Flow Chart



6.2.11 Read display image mode (0Dh)

0D H	RDDIM (Read Display Image Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	1	0D
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	0	D5	0	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit D7 – Vertical Scrolling On/Off
'0' = Vertical Scrolling is Off.
'1' = Vertical Scrolling is On.

Bit D6 – Horizontal Scrolling Status
This bit is not applicable for this project, so it is set to '0'

Bit D5 – Inversion On/Off
'0' = Inversion is Off.
'1' = Inversion is On.
This bit is not applicable for this project, so it is set to '0'

Bit D4 – All Pixels On
This bit is not applicable for this project, so it is set to '0'

Bit D3 – All Pixels Off
This bit is not applicable for this project, so it is set to '0'

Bits D2, D1, D0 – Gamma Curve Selection

Gamma Curve Selected	D2	D1	D0	Gamma Set (R26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Restrictions

-

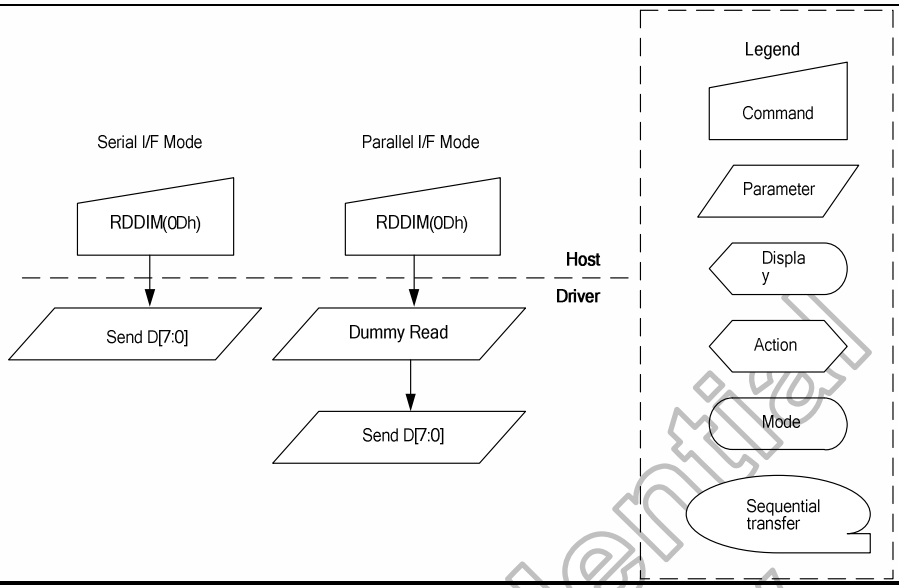
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No change
H/W Reset	00h

Flow Chart



6.2.12 Read display signal mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	0	0E
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	D0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 5.2 for mode definitions. '0' = Mode 1. '1' = Mode 2. Bit [D5:D1] – are for future use and are set to '0'. Bit D0 – Error on DSI, see section **"6.2.4RDNUMPE: Read Number of the Errors on DSI (05h)"** '0' = No Error. '1' = Error.												
Restrictions	-												

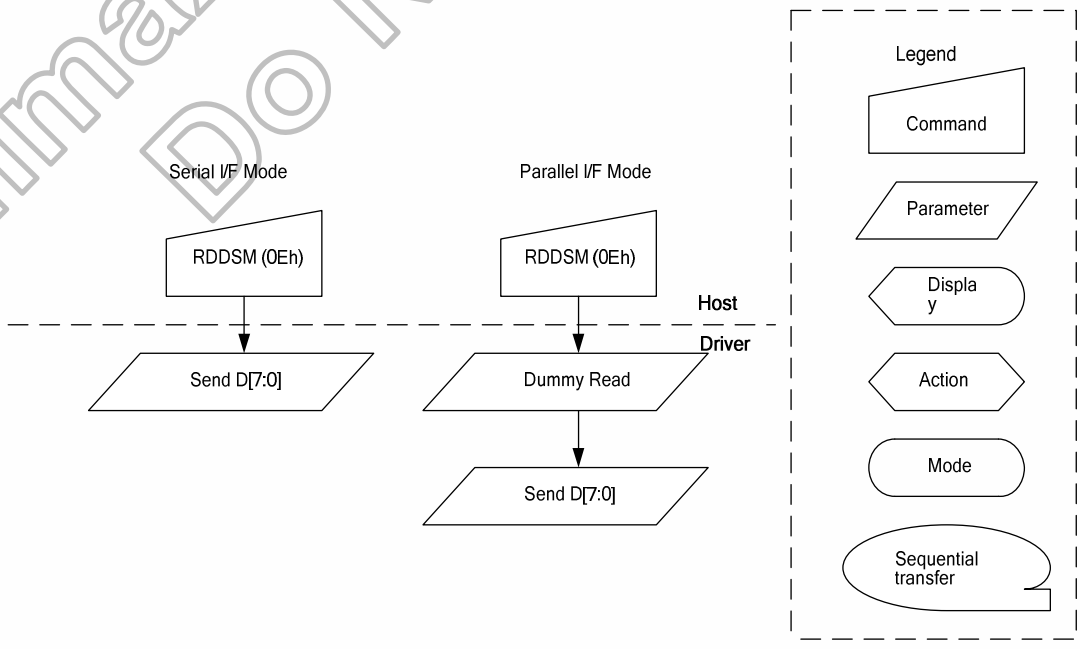
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.13 Read display self-diagnostic result (0Fh)

0F H	RDDSDR (Read Display Self-Diagnostic Result)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	1	0F
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	0	0	0	0	0	D0	-

Description

The display module returns the self-diagnostic results following a Sleep Out command.
Bit D7 – Register Loading Detection
Bit D6 – Functionality Detection
Bits D[5:1] – Reserved, Set to '0'.
Bit D0 – Checksums comparison
'0' = Checksums are same
'1' = Checksums are not same

Restrictions

-

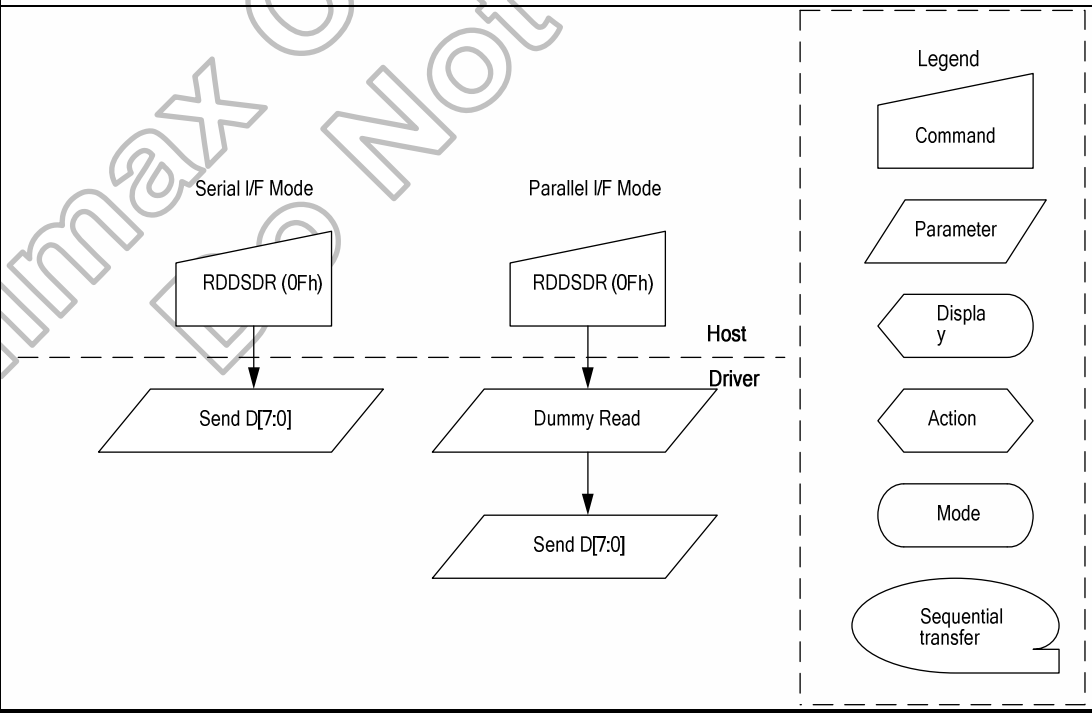
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

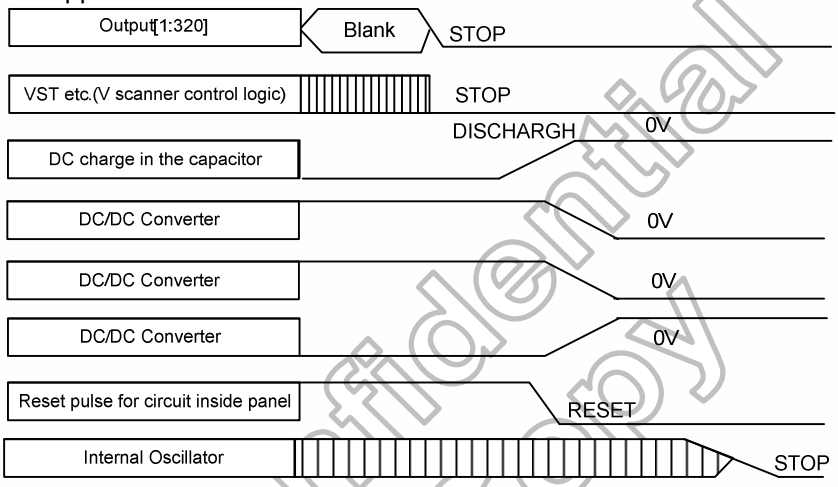
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

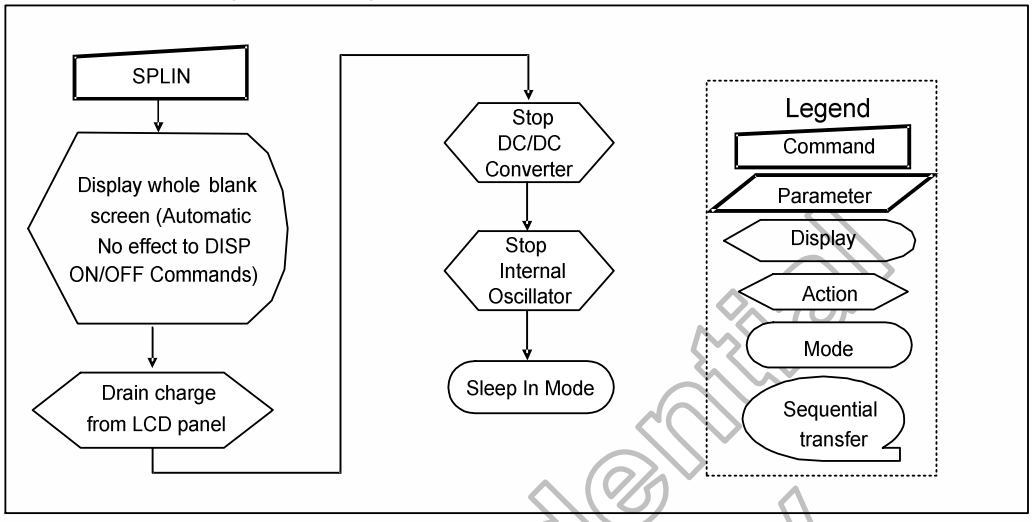


6.2.14 Sleep in (10h)

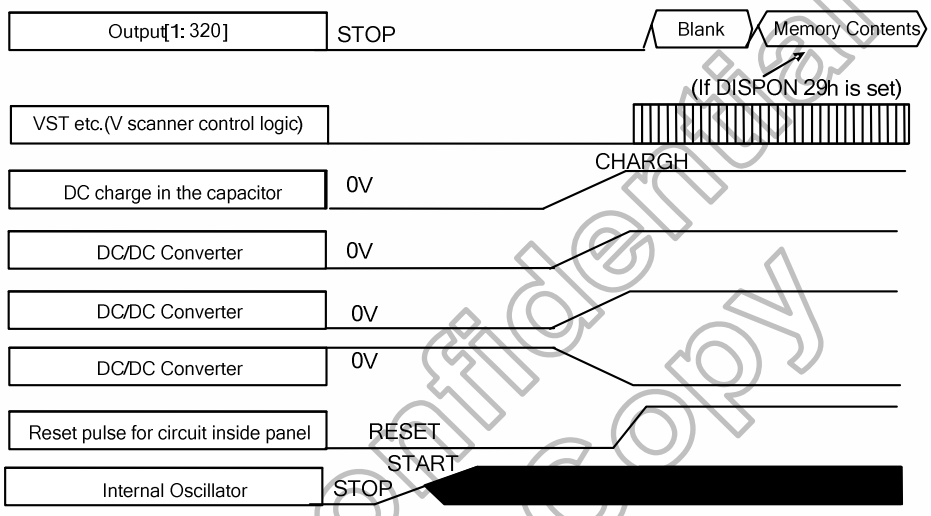
10 H	SLPIN (Sleep In)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents.												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												
Register Availability	Status	Availability											
	Normal Mode On, Idle Mode Off, Sleep Out	Yes											
	Normal Mode On, Idle Mode On, Sleep Out	Yes											
	Partial Mode On, Idle Mode Off, Sleep Out	Yes											
	Partial Mode On, Idle Mode On, Sleep Out	Yes											
	Sleep In or Booster Off	Yes											
Default	Status	Default Value											
	Power On Sequence	Sleep In Mode											
	S/W Reset	Sleep In Mode											
	H/W Reset	Sleep In Mode											

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



6.2.15 Sleep out (11h)

11 H	SLPOUT (Sleep Out)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER												
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. 												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												

Register Availability

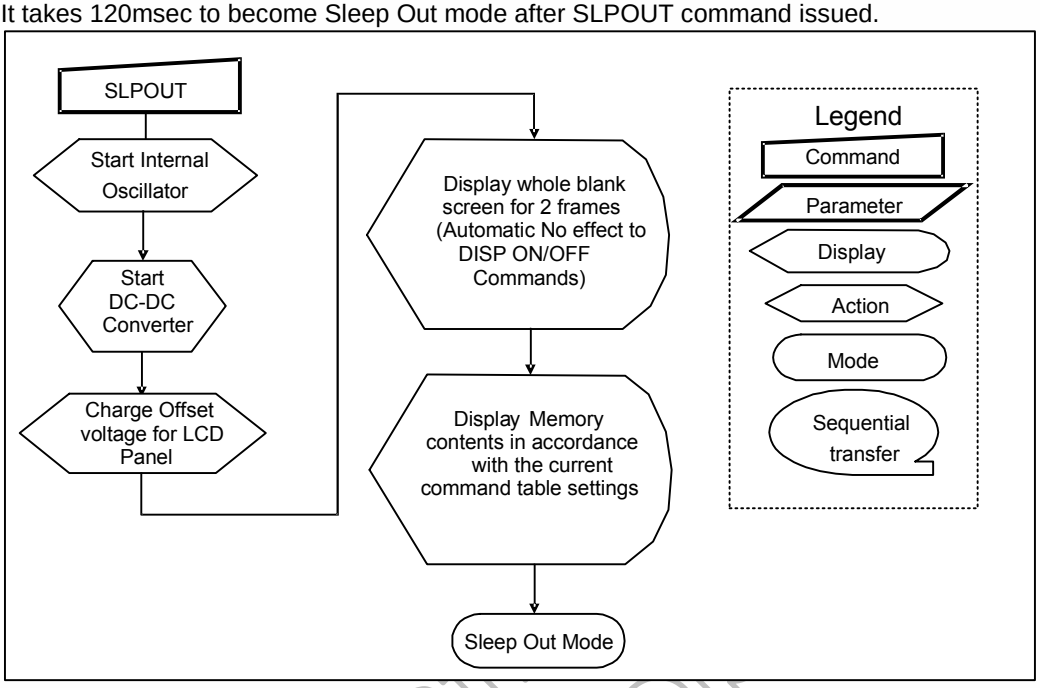
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



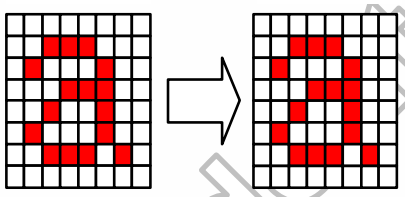
6.2.16 Partial mode on (12h)

12 H	PTLON (Partial Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER												
Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.												
Restrictions	This command has no effect when Partial mode is active.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	Status / Default Value Power On Sequence: Normal Display Mode On S/W Reset: Normal Display Mode On H/W Reset: Normal Display Mode On												
Flow Chart	See Partial Area (30h)												

6.2.17 Normal display mode on (13h)

13 H	NORON (Normal Display Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER												
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off.												
Restriction	This command has no effect when Normal mode is active.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Booster Off / Yes												
Default	Status / Default Value Power On Sequence / Normal Display Mode On S/W Reset / Normal Display Mode On H/W Reset / Normal Display Mode On												
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.												

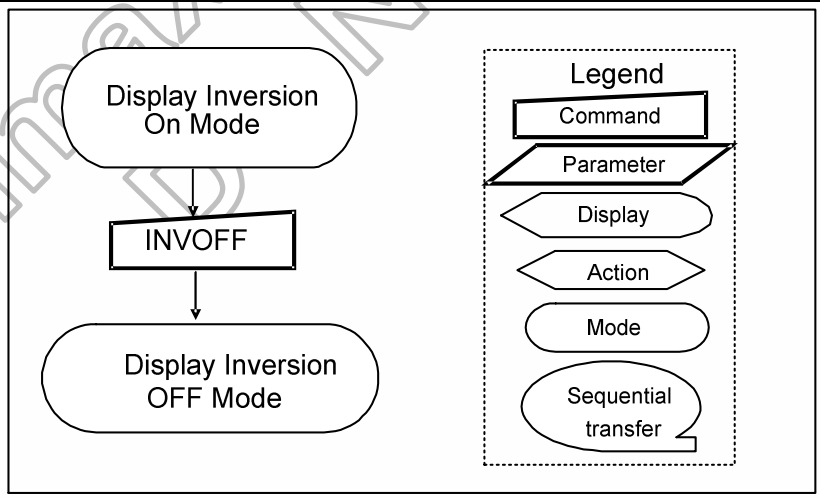
6.2.18 Display inversion off (20h)

20 H	INVOFF (Display Inversion Off)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20
Parameter	NO PARAMETER												
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display 												
Restriction	This command has no effect when module is already in inversion off mode.												

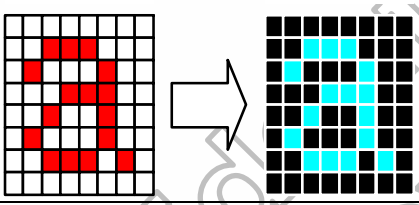
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	Status	Default Value
	Power On Sequence	Display Inversion Off
	S/W Reset	Display Inversion Off
	H/W Reset	Display Inversion Off

Flow Chart



6.2.19 Display inversion on (21h)

21 H	INVON (Display Inversion On)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER												
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display 												
Restriction	This command has no effect when module is already in inversion on mode.												

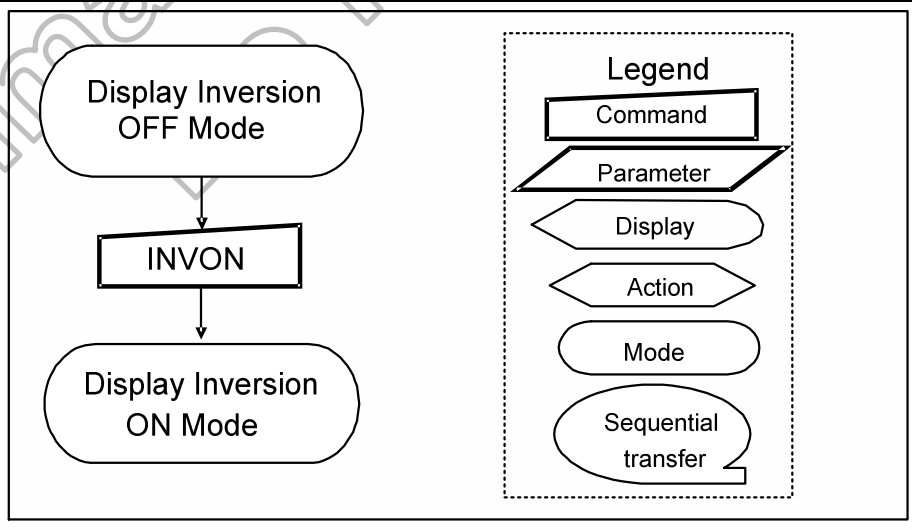
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

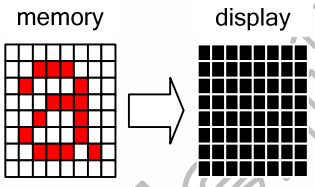
Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



6.2.20 All pixel off (22h)

22h	ALLPOFF (All Pixel Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	1	0	22
Parameter	NO PARAMETER												
Description	This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status (Example)  'All Pixels On', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display panel is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' -commands.												
Restriction	This command has no effect when module is already in all pixels off mode.												

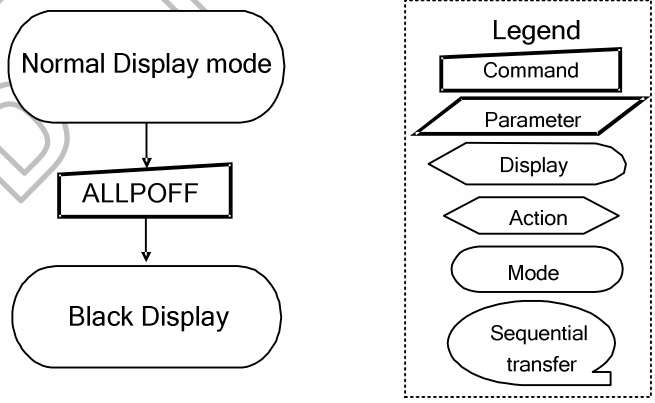
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	off
S/W Reset	off
H/W Reset	off

Flow Chart



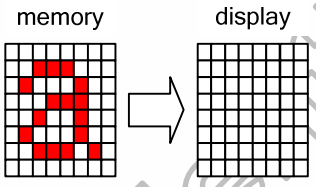
6.2.21 All pixel on (23h)

23h	ALLPON(All Pixel On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	1	1	23
Parameter	NO PARAMETER												

Description

This command turns the display panel white in 'Sleep out ' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



'All Pixels Off', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' –commands.

Restriction

This command has no effect when module is already in all pixels on mode.

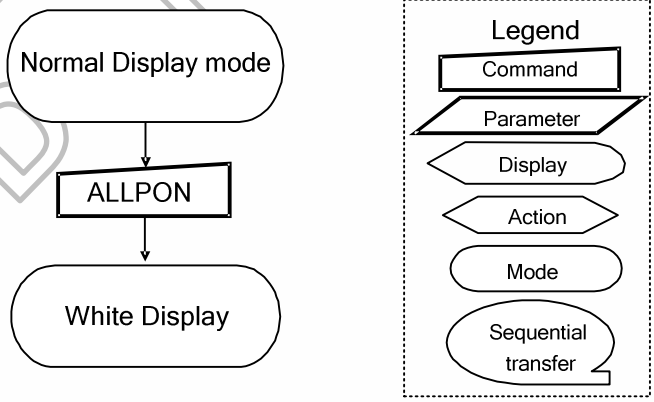
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	off
S/W Reset	off
H/W Reset	off

Flow Chart



6.2.22 Gamma set (26h)

26 H	GAMSET (Gamma Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	0	1	1	0	26
Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the table:

GC[7..0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

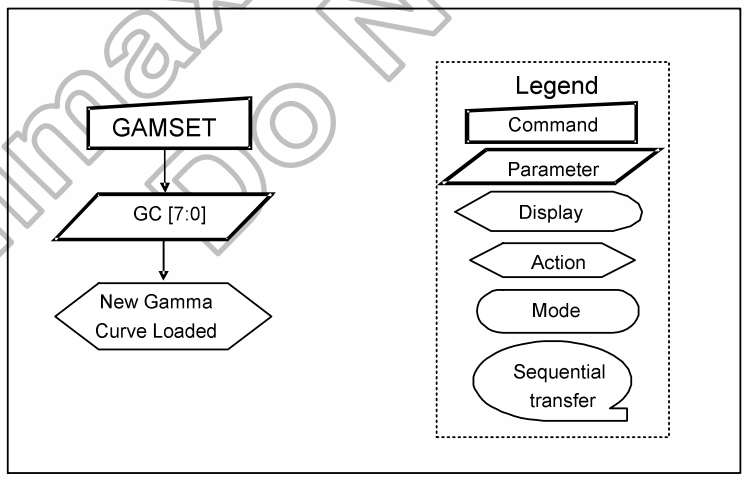
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

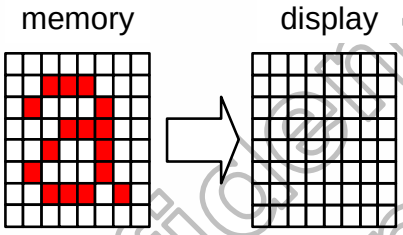
Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



6.2.23 Display off (28h)

28 H	DISPOFF (Display Off)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) 												
Restriction	This command has no effect when module is already in display off mode.												

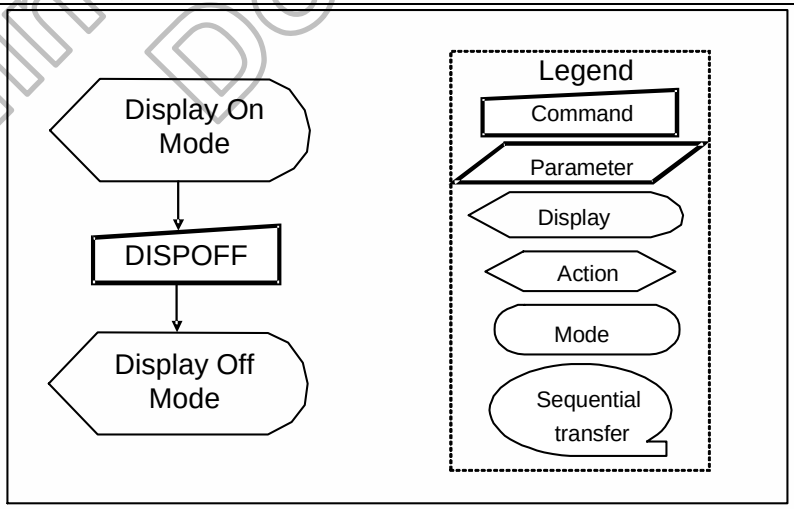
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

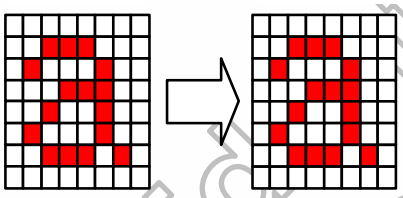
Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



6.2.24 Display on (29h)

29 H	DISPON (Display On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display 												
Restriction	This command has no effect when module is already in display on mode.												

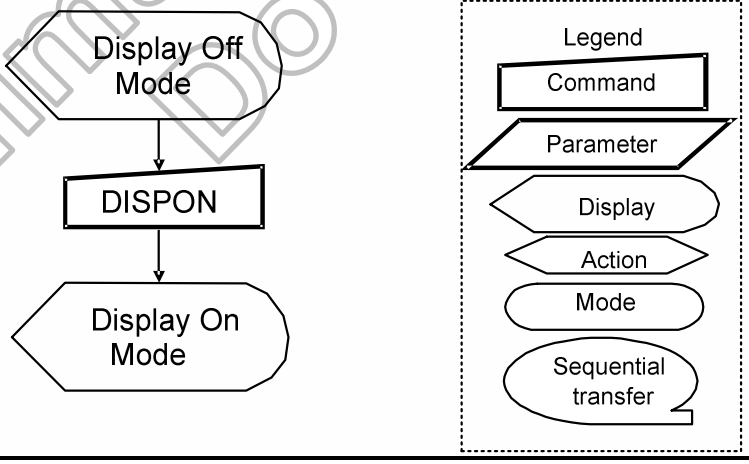
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



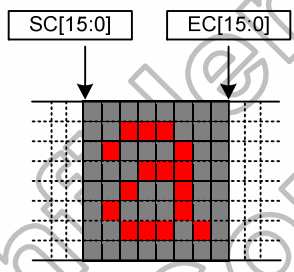
6.2.25 Column address set (2Ah)

2A H	CASET (Column Address Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	1	0	2A
1st parameter	1	↑	1	-	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note 1
2nd parameter	1	↑	1	-	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd parameter	1	↑	1	-	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note 1
4th parameter	1	↑	1	-	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)



Restriction

SC[15:0] always must be equal to or less than EC[15:0]
Note: When SC[15:0] or EC[15:0] is greater than maximum address like below, data out of range will be ignored
0000h<=SC[15:0]<=EC[15:0] <=013Fh ,when MADCTL's B5=0
0000h<=SC[15:0]<=EC[15:0] <=01DFh ,when MADCTL's B5=1

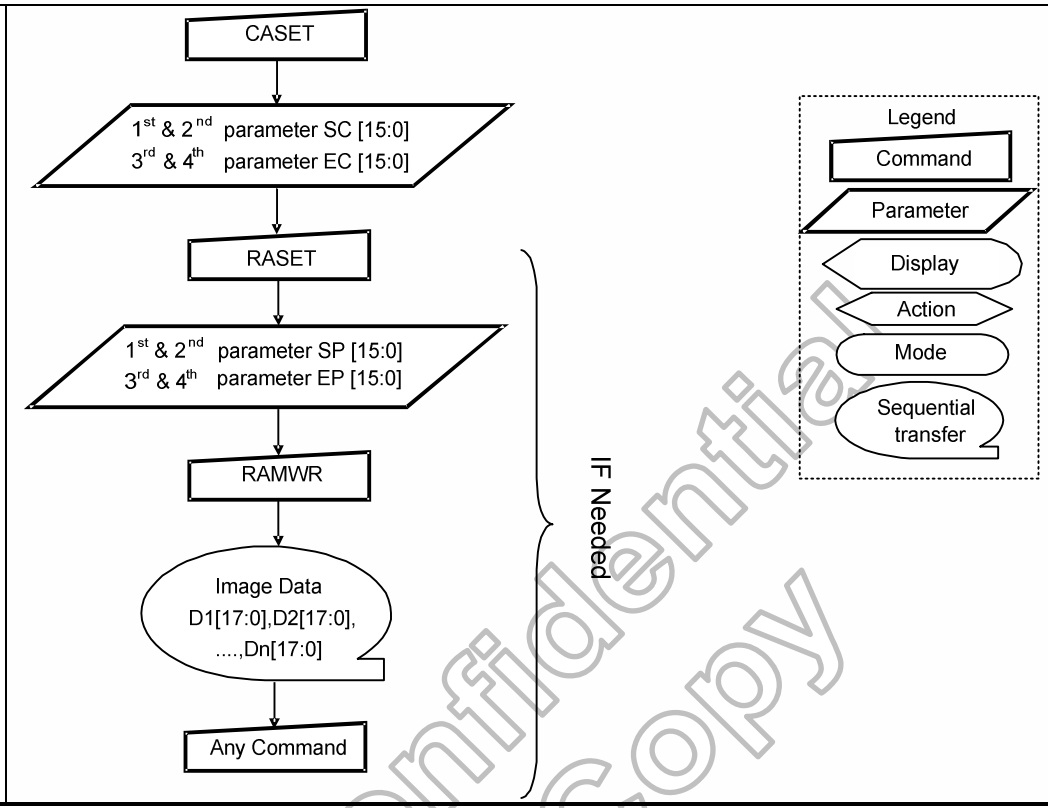
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000h	EC[15:0]=013Fh
SW Reset	SC[15:0]=0000h	EC[15:0]=013Fh
HW Reset	SC[15:0]=0000h	EC[15:0]=013Fh

Flow Chart



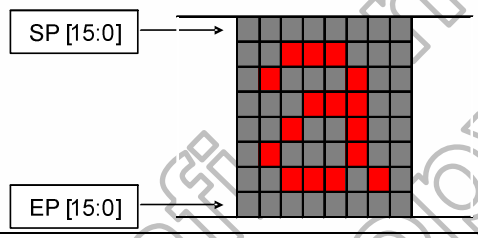
6.2.26 Page address set (2Bh)

2B H	PASET (Page Address Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	1	1	2B
1st parameter	1	↑	1	-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note 1
2nd parameter	1	↑	1	-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd parameter	1	↑	1	-	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note 1
4th parameter	1	↑	1	-	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.

(Example)



Restriction

SP[15:0] always must be equal to or less than EP[15:0]
Note: When SP[15:0] or EP[15:0] is greater than maximum row address like below, data of out of range will be ignored
0000h<=SP[15:0]<=EP[15:0]<=01DFh (When MADCTL's B5=0)
0000h<=SP[15:0]<=EP[15:0]<=013Fh (When MADCTL's B5=1)

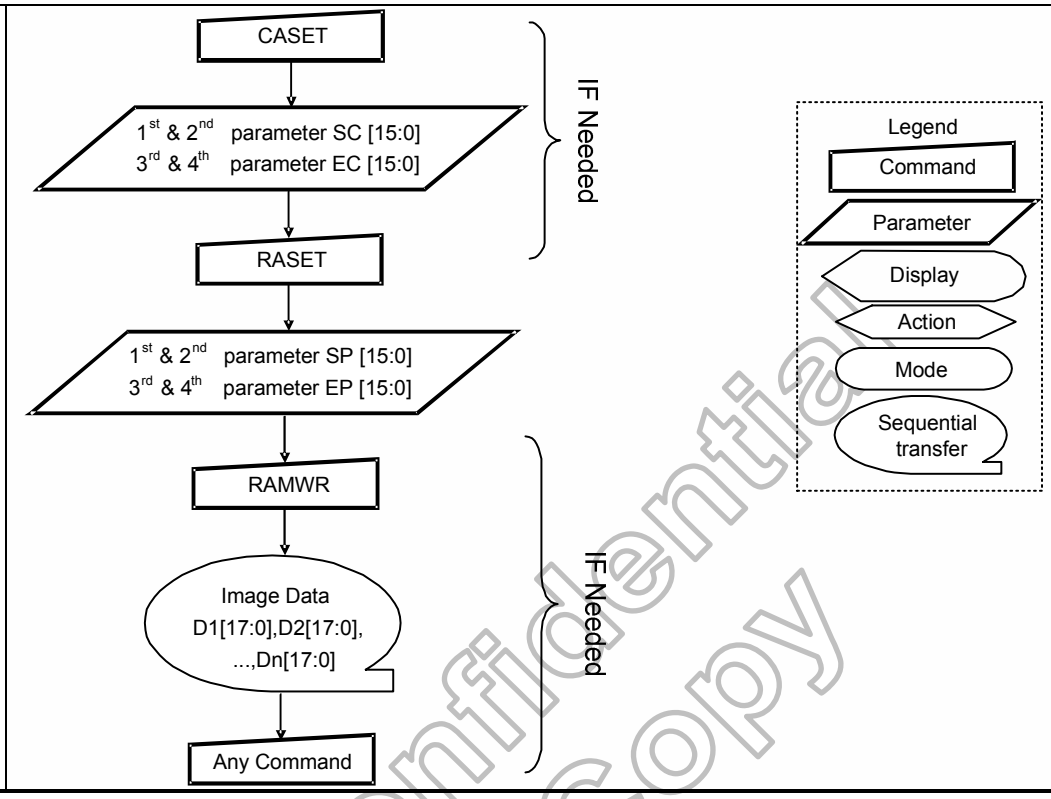
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0]=0000h	EP[15:0]=01DFh
SW Reset	SP[15:0]=0000h	EP[15:0]=01DFh
HW Reset	SP[15:0]=0000h	EP[15:0]=01DFh

Flow Chart



6.2.27 Memory write (2Ch)

2C H	RAMWR (Memory Write)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	0	0	2C
1st parameter	1	↑	1	D1[15:0]									00..FF
:	1	↑	1	Dx[15:0]									00..FF
nth parameter	1	↑	1	Dn[15:0]									00..FF

Description

This command is used to transfer data from MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting.
Then D[7:0] is stored in frame memory and the column register and the page register incremented.
Sending any other command can stop frame Write.

Restriction

In all color modes, there is no restriction on length of parameters.

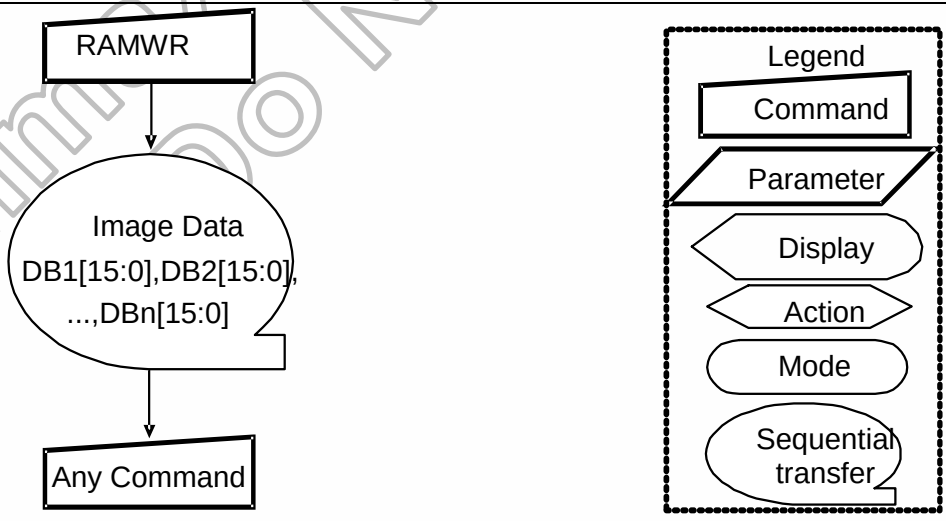
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	No

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



6.2.28 Memory read (2Eh)

2E H	RAMRD (Memory Read)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	↑	1	D1[15:0]									00..FF
:	1	↑	1	Dx[15:0]									00..FF
(n+1)th parameter	1	↑	1	Dn[15:0]									00..FF
Description	This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. Then D[7:0] is read back from the frame memory and the column register and the page register incremented Frame Read can be stopped by sending any other command.												
Restriction													

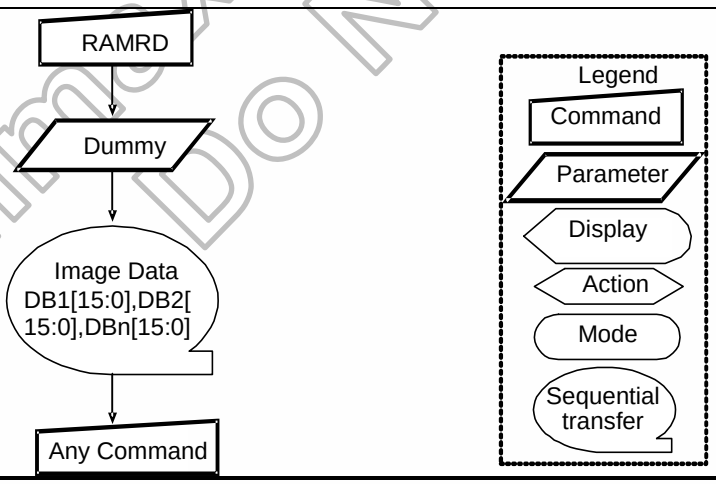
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	No

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



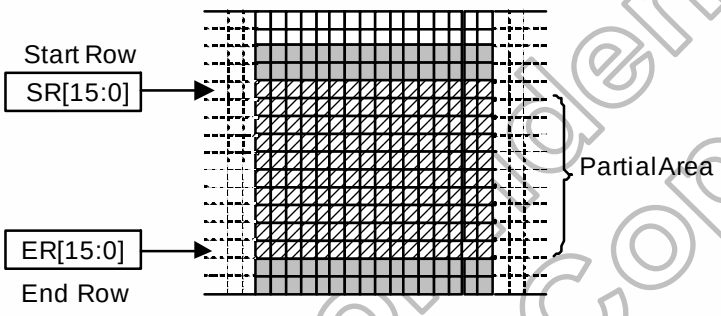
6.2.29 Partial area (30h)

30 H	PLTAR (Partial Area)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	0	0	30
1st parameter	1	↑	1	-	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000:
2nd parameter	1	↑	1	-	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	01DF
3rd parameter	1	↑	1	-	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000:
4th parameter	1	↑	1	-	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	01DF

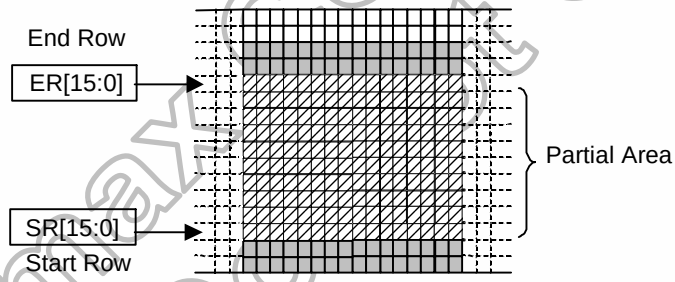
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

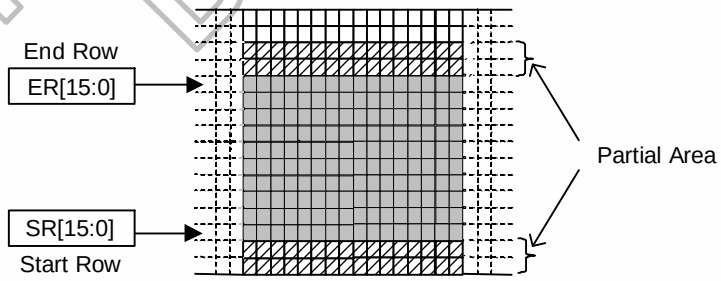
If End Row > Start Row when MADCTL B4(ML) = 0:



If End Row > Start Row when MADCTL B4(ML) = 1:



If End Row<Start Row when MADCTL's B4(ML) = 0:



If End Row = Start Row then the Partial Area will be one row deep.

Restriction

SR[15:0] and ER[15:0] cannot be exceeding than 01DFh.

Register Availability

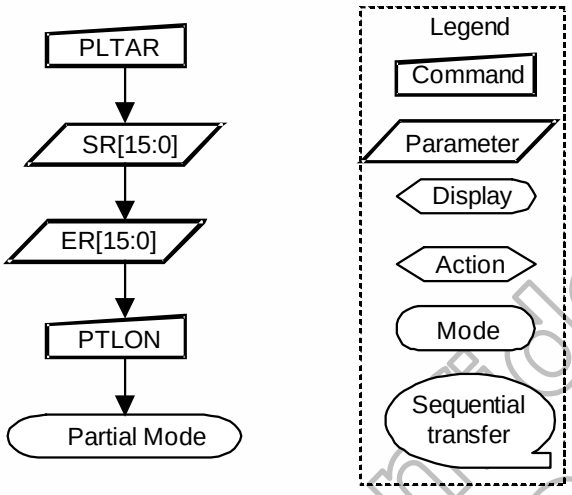
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

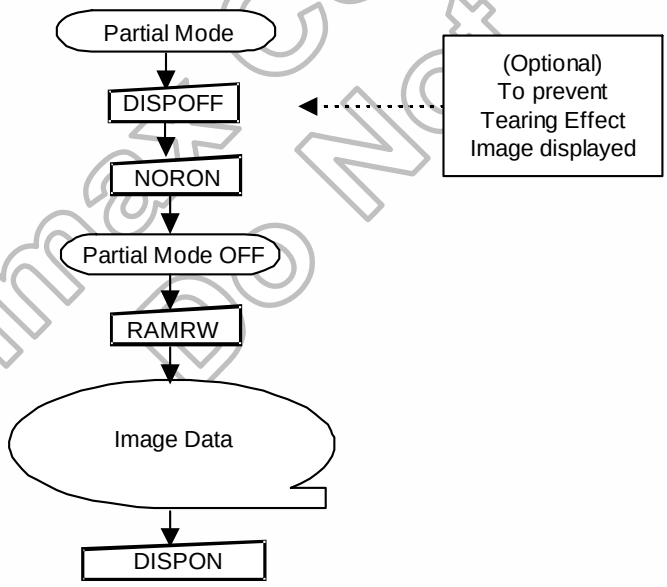
Status	Default Value	
Power On Sequence	SR[15:0]=0000h	ER[15:0]=01DFh
S/W Reset	SR[15:0]=0000h	ER[15:0]=01DFh
H/W Reset	SR[15:0]=0000h	ER[15:0]=01DFh

Flow Chart

1. To Enter Partial Display Mode:



2. To Leave Partial Display Mode

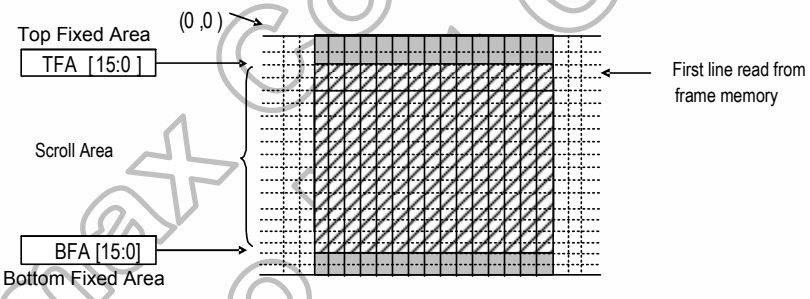


6.2.30 Vertical scrolling definition (33h)

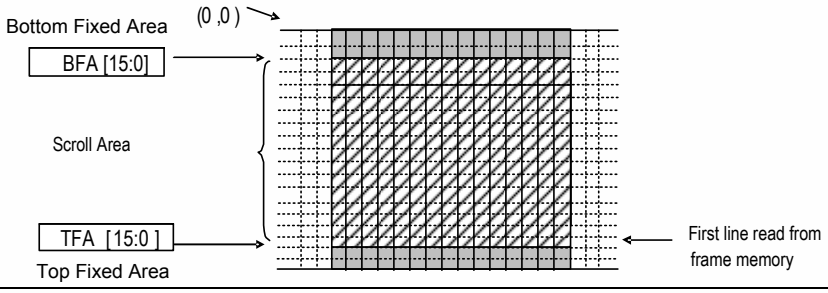
33 H	VSCRDEF (Vertical Scrolling Definition)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	1	1	33
1st parameter	1	↑	1	-	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	0000: 01E0
2nd parameter	1	↑	1	-	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	
3rd parameter	1	↑	1	-	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	0000: 01E0
4th parameter	1	↑	1	-	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	
5th parameter	1	↑	1	-	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	0000: 01E0
6th parameter	1	↑	1	-	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	

Description

This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0, the 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.



When MADCTL B4=1
The 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



Restriction

The condition is (TFA+VSA+BFA)=480, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write.

Register Availability

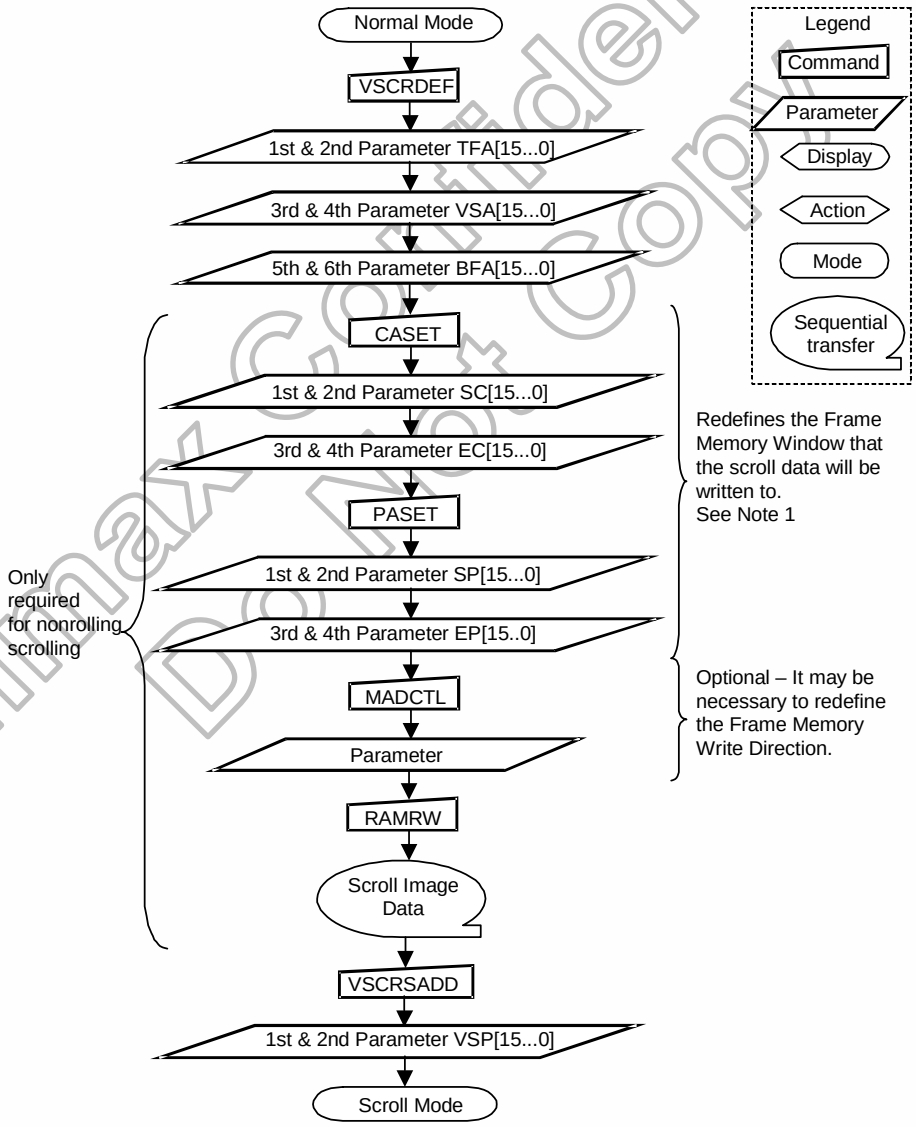
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15:0]=0000	VSA[15:0]=01E0h	BFA[15:0]=0000
S/W Reset	TFA[15:0]=0000	VSA[15:0]=01E0h	BFA[15:0]=0000
H/W Reset	TFA[15:0]=0000	VSA[15:0]=01E0h	BFA[15:0]=0000

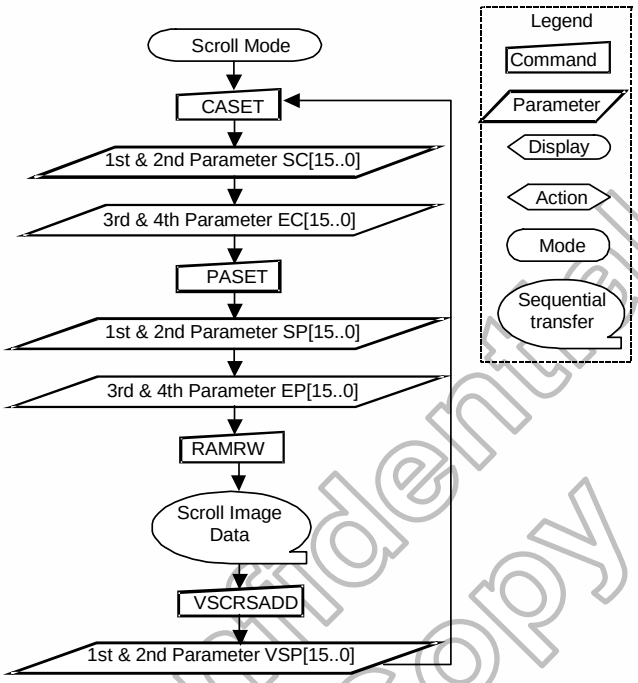
Flow Charts

1. To enter Vertical Scroll Mode:

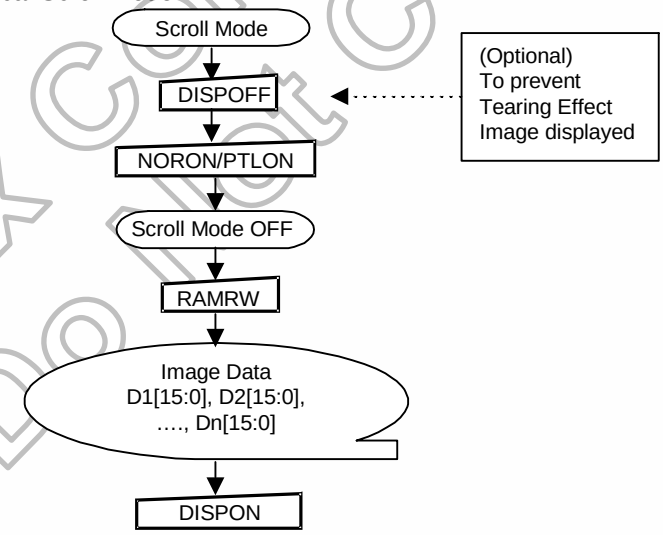


Note: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:



3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

6.2.31 Tearing effect line off (34h)

34 H	TEOFF (Tearing Effect Line OFF)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	0	34
Parameter	No Parameter												
Description	This command is used to turn OFF the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

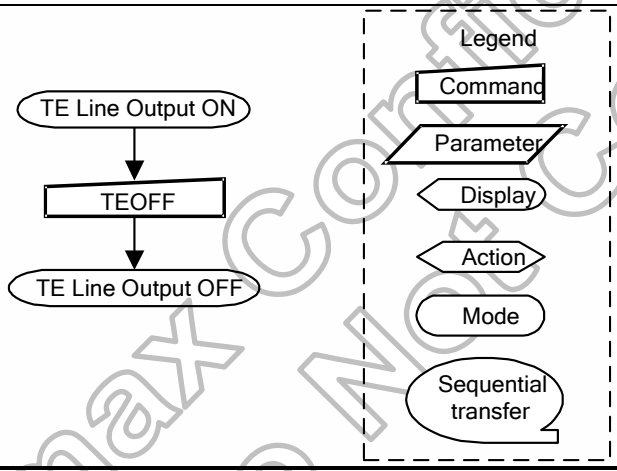
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



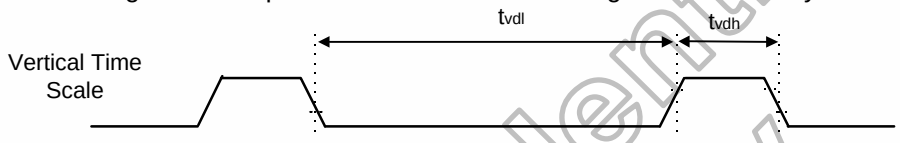
6.2.32 Tearing effect line on (35h)

35 H	TEON (Tearing Effect Line ON)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	1	35
1stparameter	0	↑	1	-	-	-	-	-	-	-	-	TEMODE	-

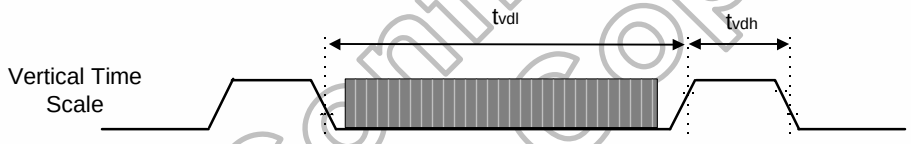
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

When TEMODE=0:
The Tearing Effect Output line consists of V-Blanking information only:



When TEMODE=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

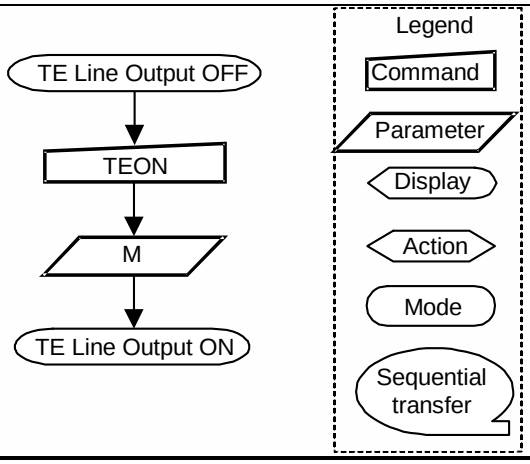
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



6.2.33 Memory access control (36h)

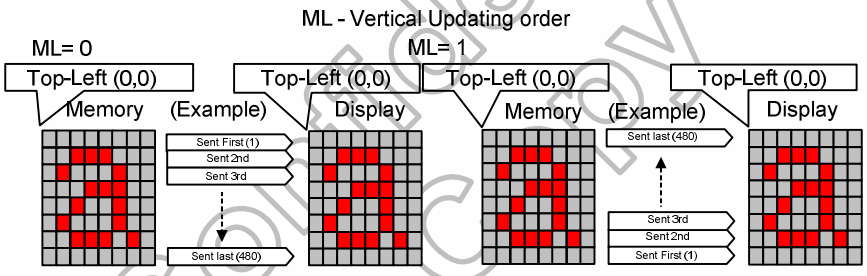
36 H	MADCTL (Memory Access Control)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	1	0	36
1st parameter	1	↑	1	-	MY	MX	MV	ML	BGR	SS	-	-	-

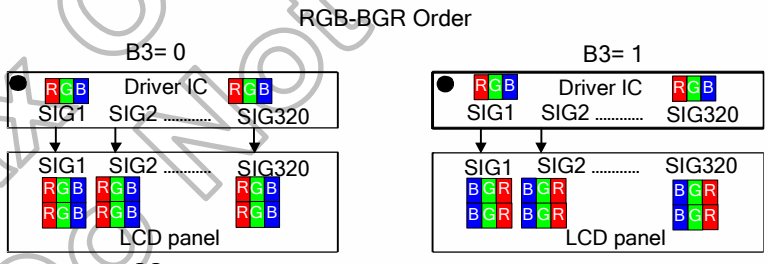
Description

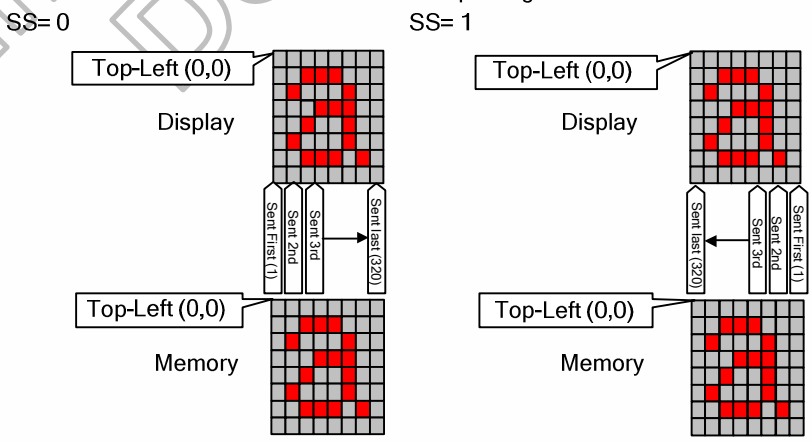
This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit Assignment

BIT	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Vertical ORDER (ML)	LCD vertical refresh direction control
B3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)
B2	Horizontal ORDER (SS)	LCD horizontal refresh direction control







Note: Top-Left (0,0) means a physical memory location.
Bit D1 – Switching Between Segment Output and RAM
This bit is not applicable for this project, so it is set to '0'
Bit D0 – Switching Between Common Output and RAM
This bit is not applicable for this project, so it is set to '0'

Restriction

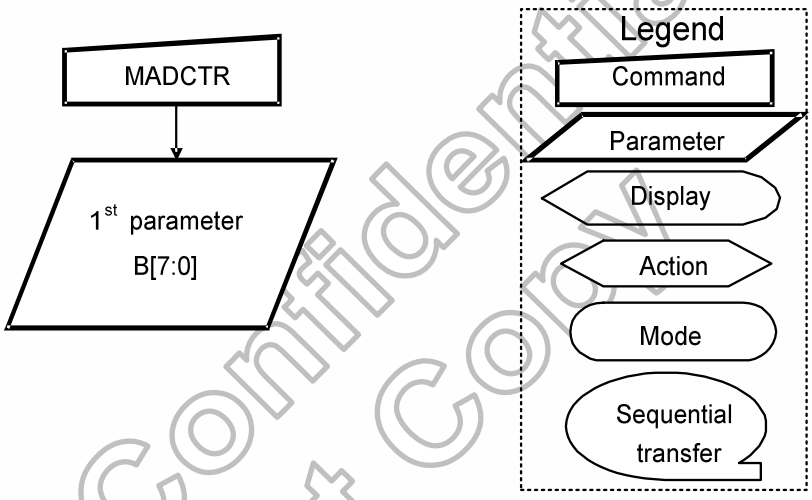
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No change
H/W Reset	00h

Flow Chart

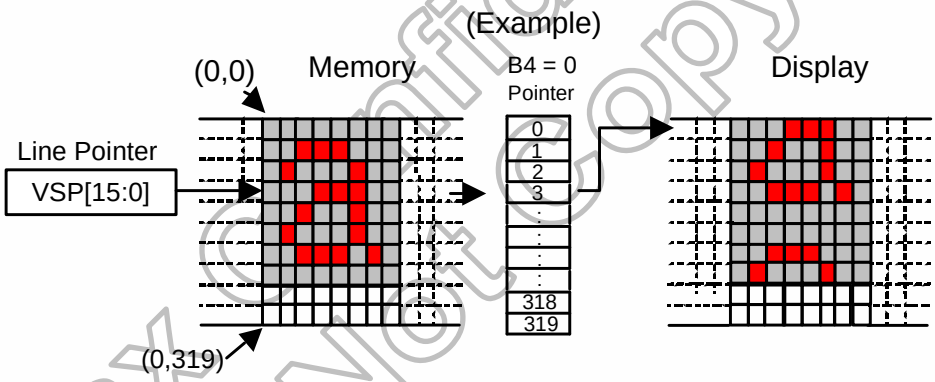


6.2.34 Vertical scrolling start address (37h)

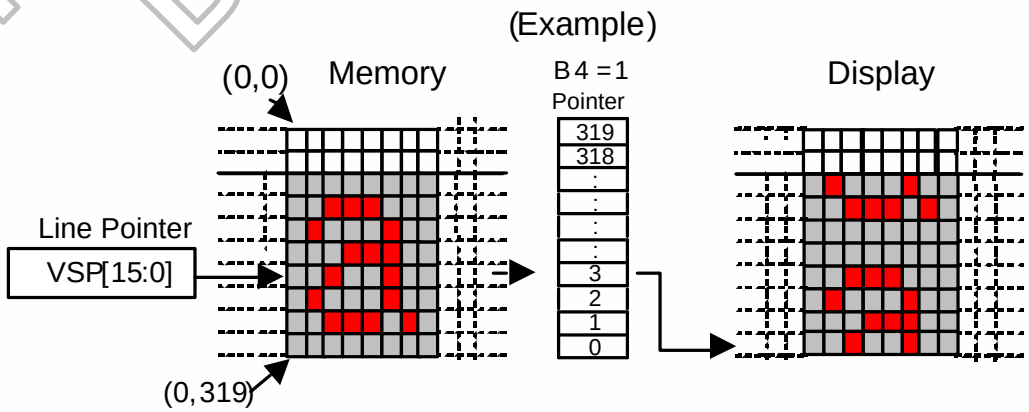
37 H	VSCRSADD (Vertical Scrolling Start Address)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	-	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	01. DF
2nd parameter	1	1	↑	-	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

When MADCTL B4='0'
Example:
When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02'd, Vertical Scrolling Area VSA = '318'd' and VSP = '3d'



When MADCTL B4='1'
Example:
When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02d, Vertical Scrolling Area VSA = '318d' and VSP = '3d'



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.35 Idle mode off (38h)

38 H	IDMOFF (Idle Mode Off)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors.												
Restriction	This command has no effect when module is already in idle off mode.												

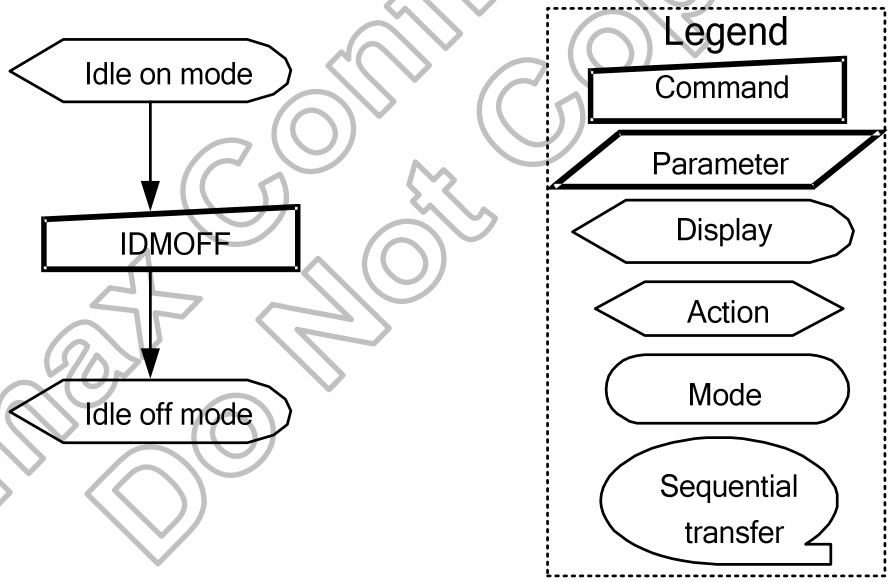
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart

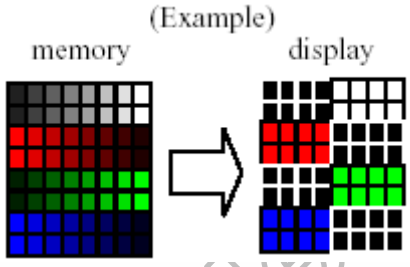


6.2.36 Idle mode on (39h)

39 H	IDMON (Idle Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory contents vs. Display Color			
	$R_5 R_4 R_3 R_2 R_1 R_0$	$G_5 G_4 G_3 G_2 G_1 G_0$	$B_5 B_4 B_3 B_2 B_1 B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

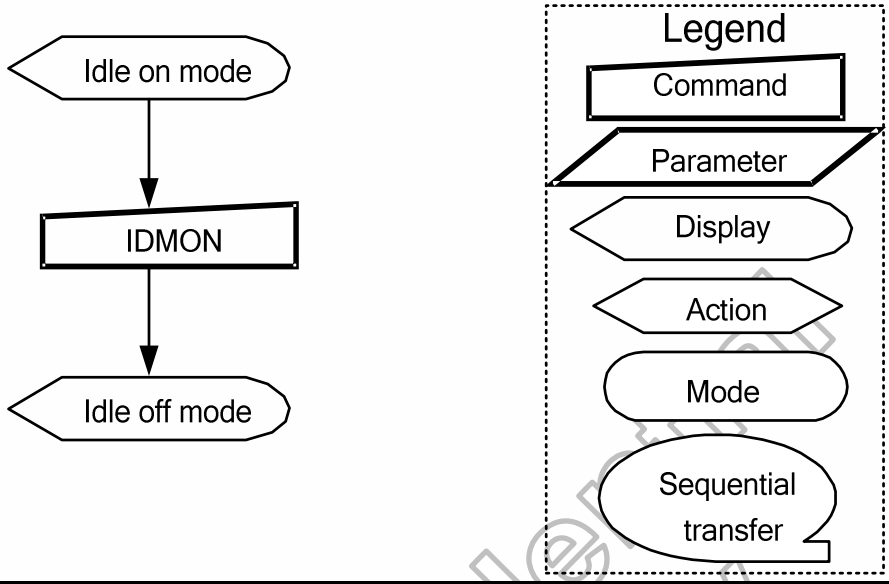
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart	

6.2.37 Interface pixel format (3Ah)

3A H	COLMOD (Interface Pixel Format)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	1	0	3A
1st parameter	1	↑	1	-	-	CS EL2	CS EL1	CS EL0	-	D2	D1	D0	-

Description

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

DBI interface (RM='0')

Interface Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

DPI interface (RM='1')

Interface Format	CSEL2	CSEL1	CSEL0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

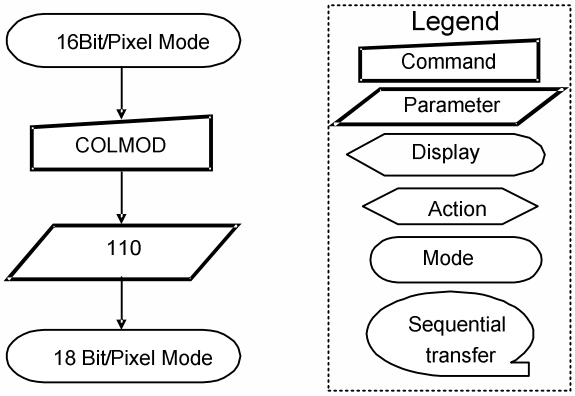
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	18-bit/pixel
S/W Reset	No Change
H/W Reset	18-bit/pixel

Flow Chart

Example:



6.2.38 Write_memory_contiune (3Ch)

3Ch	Write_memory_contiune												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	1	0	0	3C
1st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF

Description

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Sending any other command can stop frame Write.
If set_address_mode B5 = 0:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.
If set_address_mode B5 = 1:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Restriction

In all colour modes, there is no restriction on length of parameters.

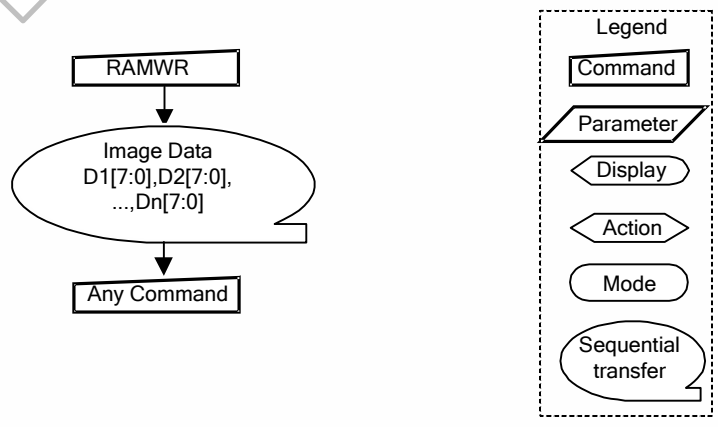
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



6.2.39 Raed_memory_continue (3Eh)

3Eh	Raed_memory_continue												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	1	1	0	3E
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
(n+1)th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF

Description

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command.
If set_address_mode B5=0:
Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.
If set_address_mode B5=1:
Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data.
A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.

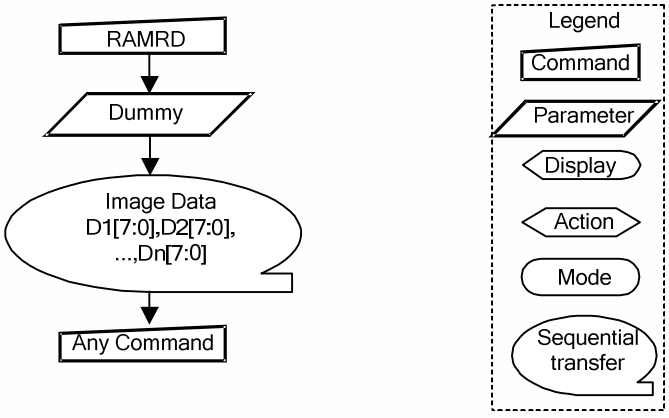
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart

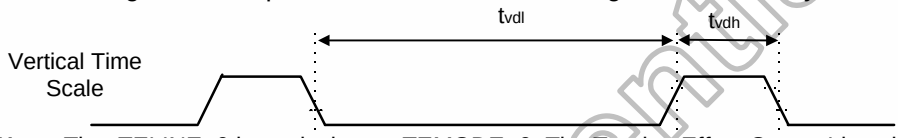


6.2.40 Set tear scan line (44h)

44 H	TESL(Tear Effect Scan Lines)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	0	44
1st parameter	1	1	↑	-	TELINE[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	TELINE[7:0](8'b0)								00..FF

Description

This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reacfes line TELINE. The TE signal is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.
The Tearing Effect Output line consists of V-Blanking information only:



Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.

Restriction

The command has no effect when Tearing Effect output is already ON.

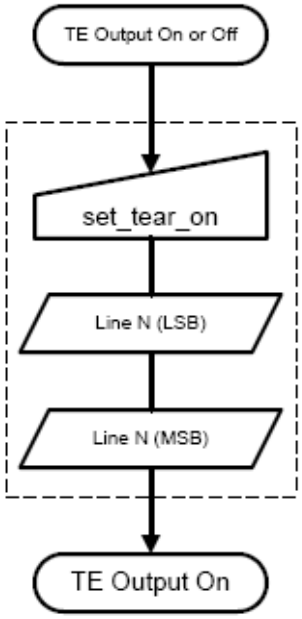
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	TELINE[15:8]=0000h
S/W Reset	TELINE[15:8]=0000h
H/W Reset	TELINE[15:8]=0000h

Flow Chart



6.2.41 Get Scan Lines (45h)

45 H	GETSL(Mipi new Get Scan Lines)												
	D/CX	RDX	WRX	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	1	45
1st parameter	1	↑	1	-	X	X	X	X	X	X	X	X	Dummy read
2nd parameter	1	↑	1	-	SL[15:8]								-
3th parameter	1	↑	1	-	SL[7:0]								-
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.												
Restriction													

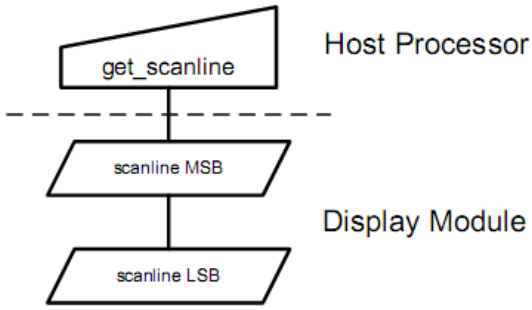
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.42 Write display brightness value (51h)

51 H	WRDISBV (Write Display Brightness Value)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	0	1	51
1st parameter	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00..FF
Description	This command is used to adjust the brightness value of the display. The backlight PWM pulse output duty is equal to DBV[7:0]/255 x CABC_duty.												
Restriction													

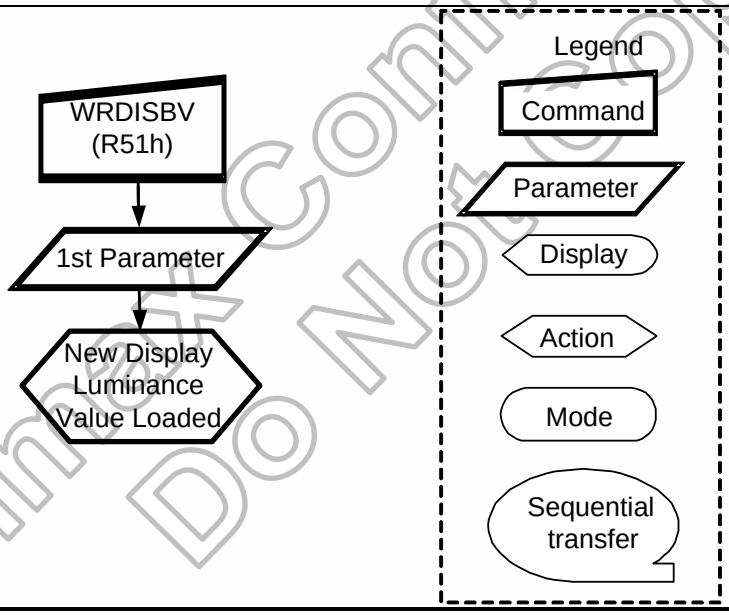
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



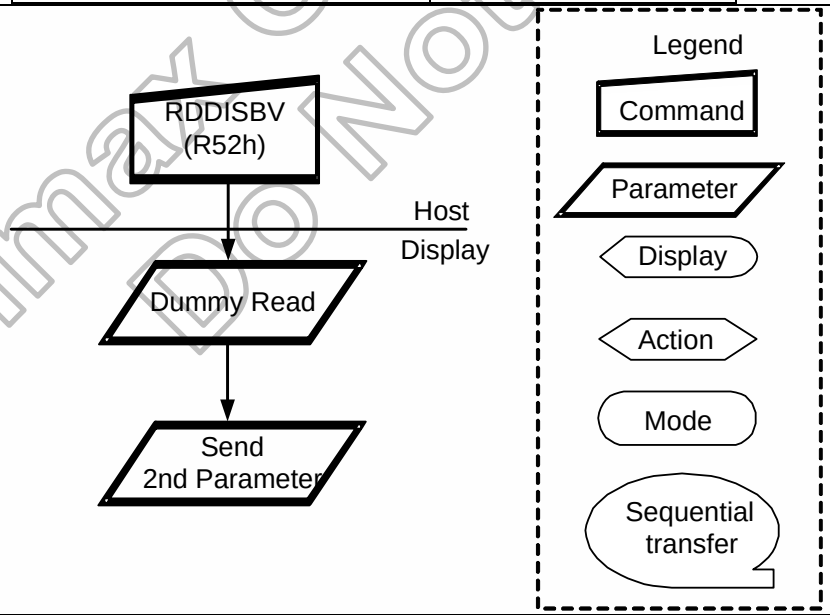
6.2.43 Read display brightness value (52h)

52H	RDDISBV (Read Display Brightness Value)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	1	0	52
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	xx
Description	This command returns the brightness value of the display. DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (R53h)" command is '0'. DBV[7:0] is manual set brightness specified with "Write CTRL Display (R53h)" command when bit BCTRL is '1'. When bit BCTRL of "Write CTRL Display (R53h)" command is '1' and bit C1/C0 of "Write Content Adaptive Brightness Control (R55h)" are '0', DBV[7:0] output is the brightness value specified with " Write Display Brightness (R51h)" command.												
Restriction	-												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

Flow Chart



6.2.44 Write control display (53h)

53H	WRCTRLD (Write Control Display)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	1	1	53
1st parameter	1	↑	1	-	-	-	BCTRL	-	DD	BL	-	-	00..FF

Description

This command is used to control display brightness.

BCTRL: Backlight Control Block On/Off, This bit is always used to switch brightness for display.
0 = Off (Brightness registers are 00h, DBV[7:0] of R52h)
1 = On (Brightness registers are active, according to the other parameters.)

Display Dimming **(DD):** (Only for manual brightness setting)
DD = **0**: Display Dimming is off
DD = 1: Display Dimming is on

BL: Backlight Control On/Off
0 = Off (Completely turn off backlight circuit. Control lines must be low.)
1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (**DD=1**) are selected.

Restriction

-

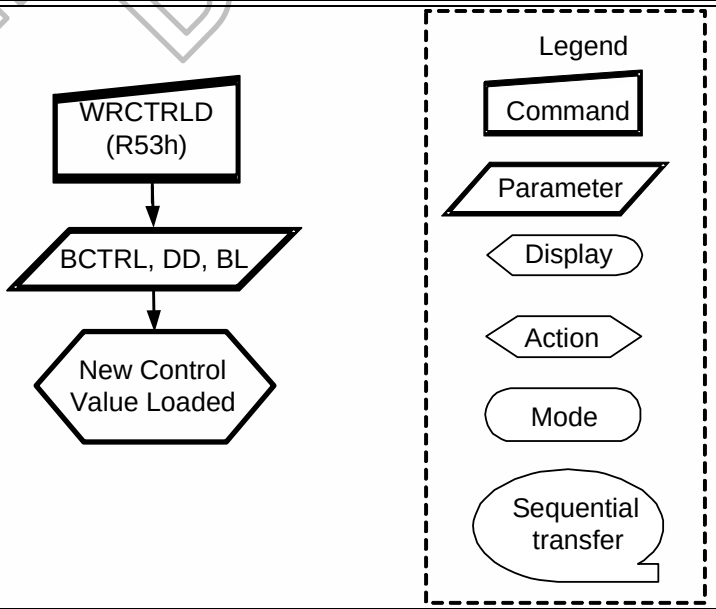
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.45 Read control value display (54h)

54H	RDCTRLD (Read Control Value Display)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	0	0	54
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0	xx

Description

This command returns ambient light and brightness control values, see chapter: "Write CTRL Display (R53h)".

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.
0 = Off
1 = On

Display Dimming (DD):
DD = 0: Display Dimming is off
DD = 1: Display Dimming is on

BL: Backlight Control On/Off
0 = Off
1 = On

Restriction

-

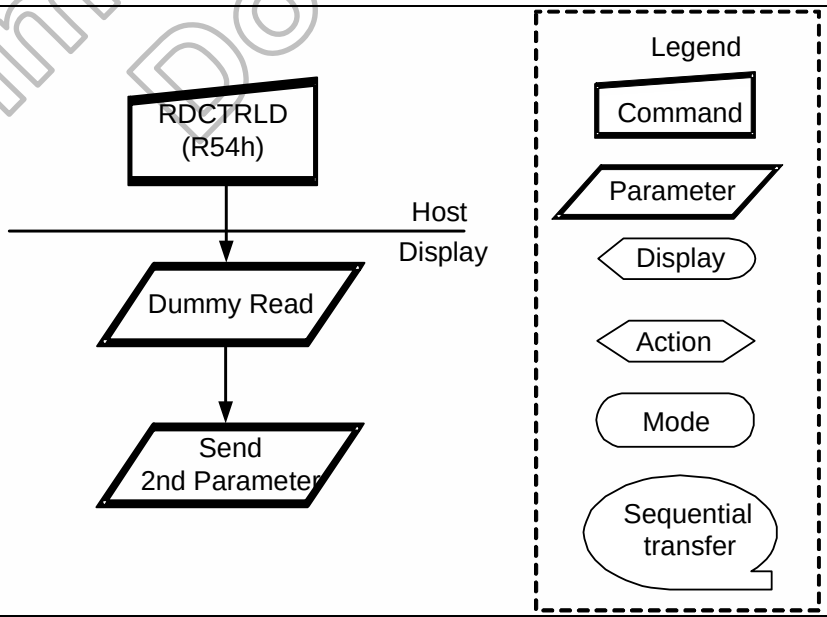
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.46 Write content adaptive brightness control (55h)

55H	WRCABC (Write Content Adaptive Brightness Control)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	0	1	55
1st parameter	1	↑	1	-	-	-	-	-	-	-	C1	C0	00..03

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function	Note
0	0	Off	-
0	1	User Interface Image	-
1	0	Still Picture	-
1	1	Moving Image	-

Restriction

-

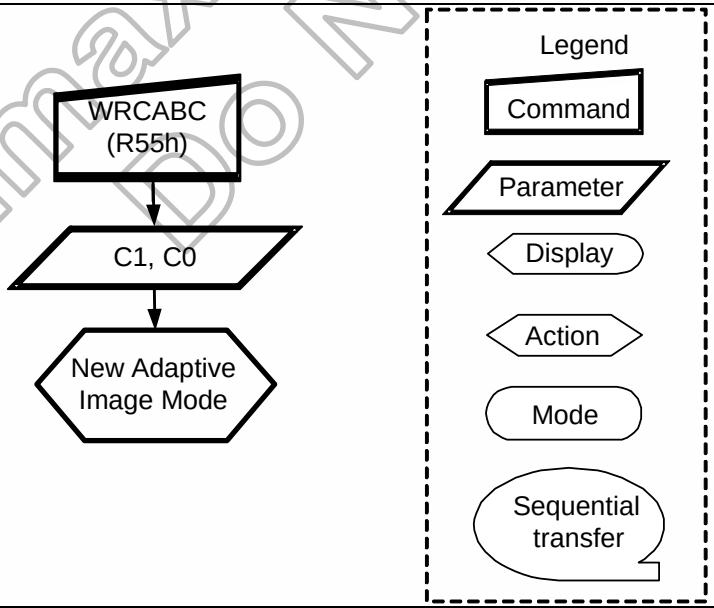
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.47 Read content adaptive brightness control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	1	0	56
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	0	0	0	0	0	0	C1	C0	xx

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function	Note
0	0	Off	-
0	1	User Interface Image	-
1	0	Still Picture	-
1	1	Moving Image	-

Restriction

-

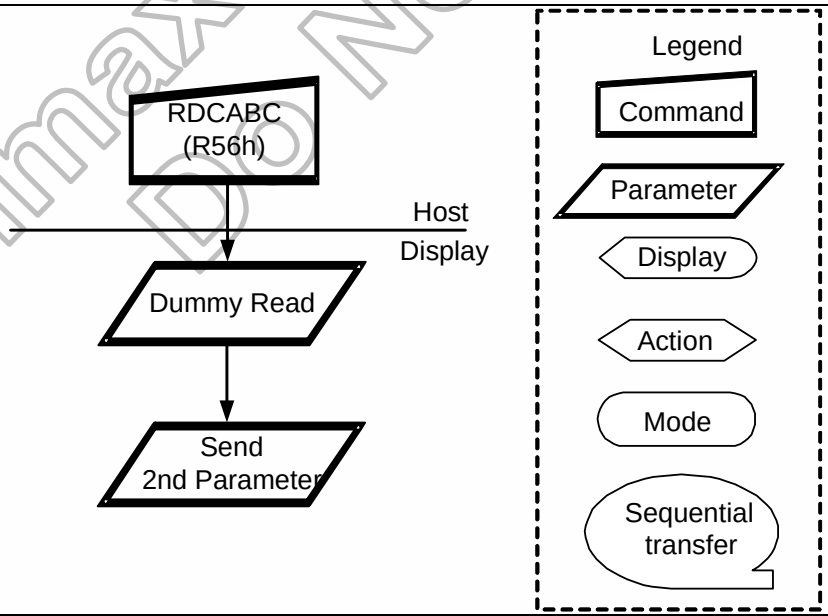
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.48 Write CABC minimum brightness (5Eh)

5EH	WRCABCMB (Write CABC Minimum Brightness)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	1	1	1	0	5E
1st parameter	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00..FF
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.												
Restriction	-												

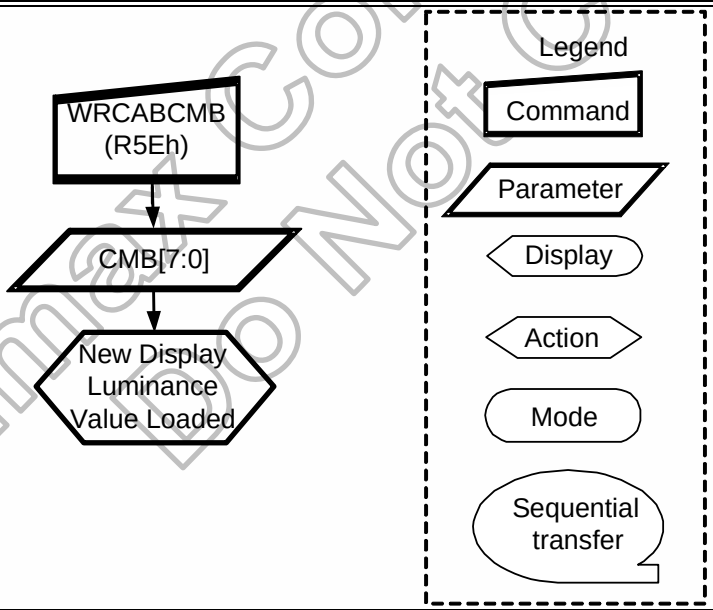
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.49 Read CABC minimum brightness (5Fh)

5FH	RDCABCMB (Read CABC Minimum Brightness)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	1	1	1	1	5F
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	xx
Description	This command is used to return the minimum brightness value of CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. CMB[7:0] is CABC minimum brightness specified with “Write CABC minimum brightness (R5Eh)” command.												
Restriction	-												

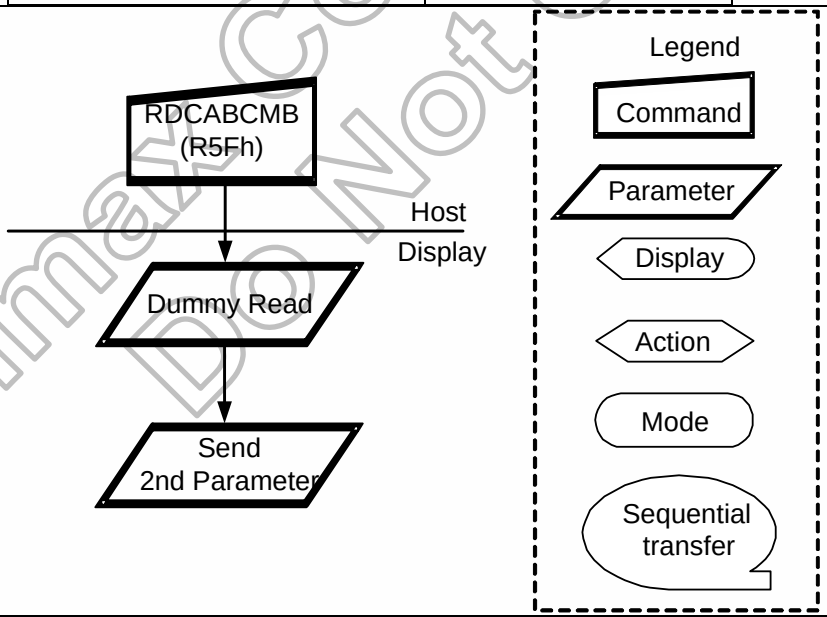
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.50 Read automatic brightness control self-diagnostic result (68h)

68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	1	0	1	0	0	0	68
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	xx
2nd parameter	1	1	↑	-	D7	D6	0	0	0	0	0	0	xx
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out command as described in the table below. **Bit D7:** Register Loading Detection. **Bit D6:** Functionality Detection. Bit D5, D4, D3, D2, D1 and D0 are for future use and are set to '0'.												
Restriction	-												

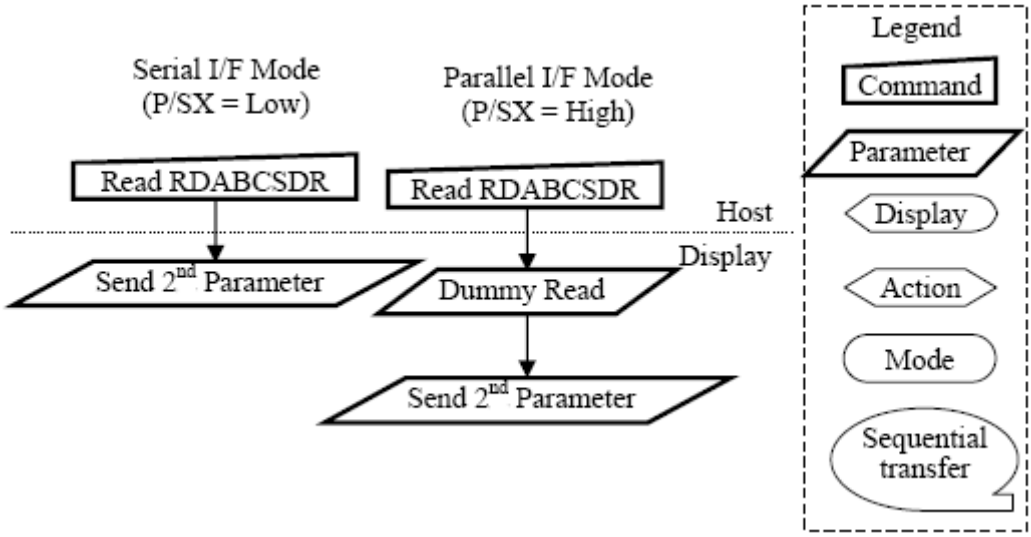
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.51 Read Black/White Low Bits (70h)

70h	RDBWLK (Read Black/White Low Bits)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	0	0	0	70
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	xx
Description	This command returns the lowest bits of black and white color characteristics. Black: Bkx and Bky White: Wx and Wy												
Restriction	-												

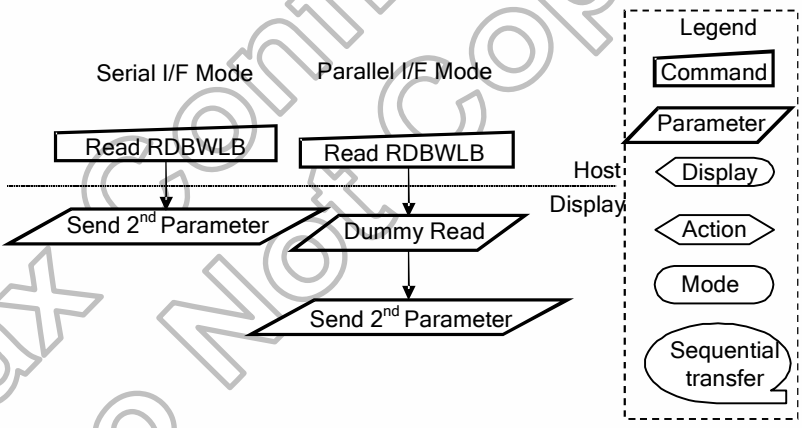
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.52 Read Bkx (71h)

71h	RDBkx (Read Bkx)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	0	0	1	71
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	xx
Description	This command returns the Bkx bits (Bkx[9:2]) of black color characteristics.												
Restriction	-												

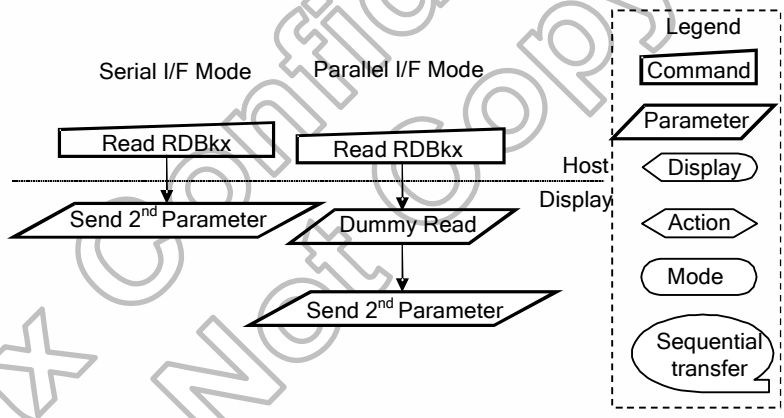
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.53 Read Bky (72h)

72h	RDBky (Read Bky)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	0	1	0	72
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	xx
Description	This command returns the Bky bits (Bky[9:2]) of black color characteristics.												
Restriction	-												

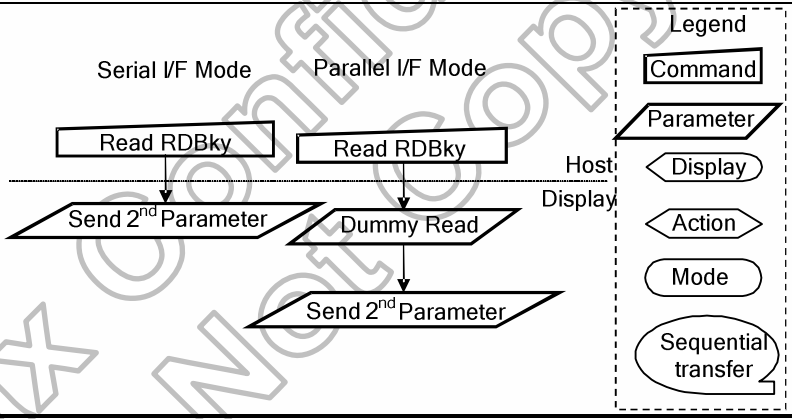
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.54 Read Wx (73h)

73h	RDWx (Read Wx)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	0	1	1	73
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	xx
Description	This command returns the Wx bits (Wx[9:2]) of white color characteristics.												
Restriction	-												

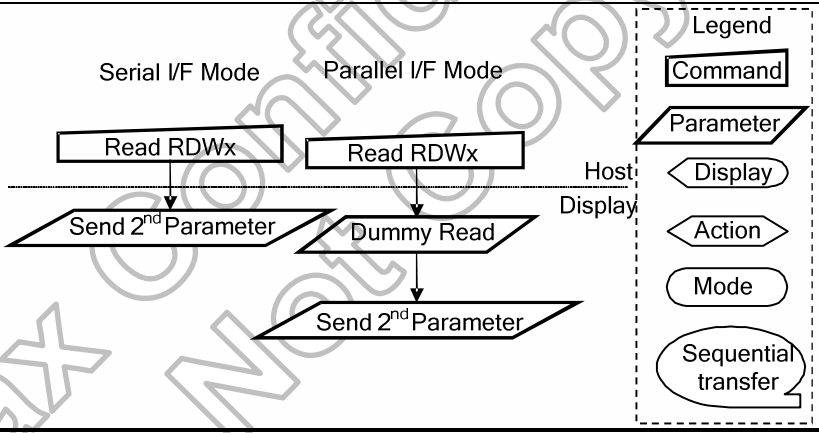
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.55 Read Wy (74h)

74h	RDWy (Read Wy)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	1	0	0	74
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	xx
Description	This command returns the Wy bits (Wy[9:2]) of white color characteristics.												
Restriction	-												

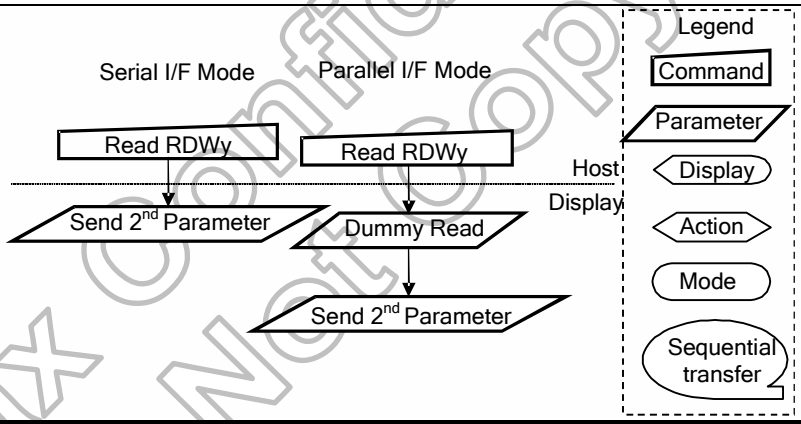
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.56 Read Red/Green Low Bits (75h)

75h	RDRGLB (Read Red/Green Low Bits)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	1	0	1	75
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	xx
Description	This command returns the lowest bits of red and green color characteristics. Red: Rx and Ry Green: Gx and Gy												
Restriction	-												

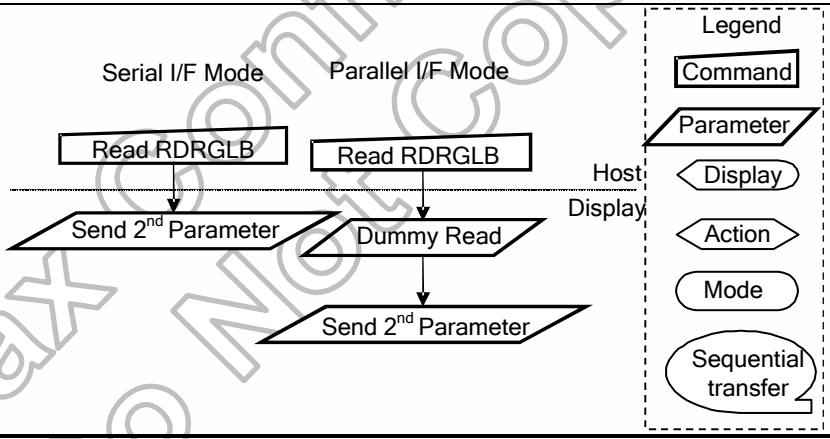
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.57 Read Rx (76h)

76h	RDRx (Read Rx)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	1	1	0	76
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	xx
Description	This command returns the Rx bits (Rx[9:2]) of red color characteristics.												
Restriction	-												

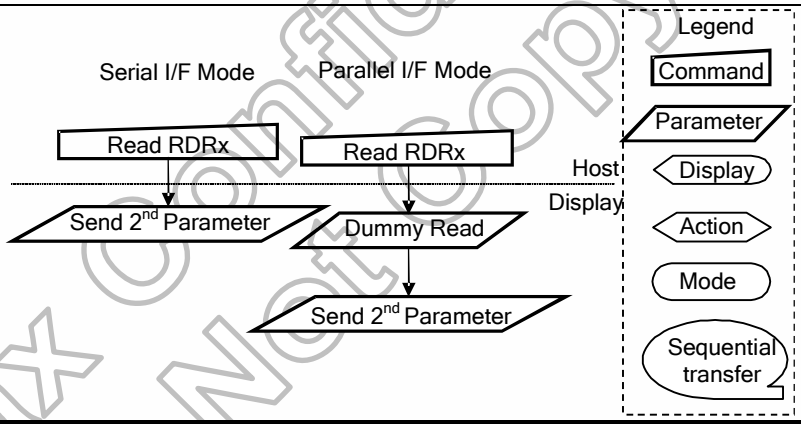
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.58 Read Ry (77h)

77h	RDRy (Read Ry)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	1	1	1	77
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	xx
Description	This command returns the Ry bits (Ry[9:2]) of red color characteristics.												
Restriction	-												

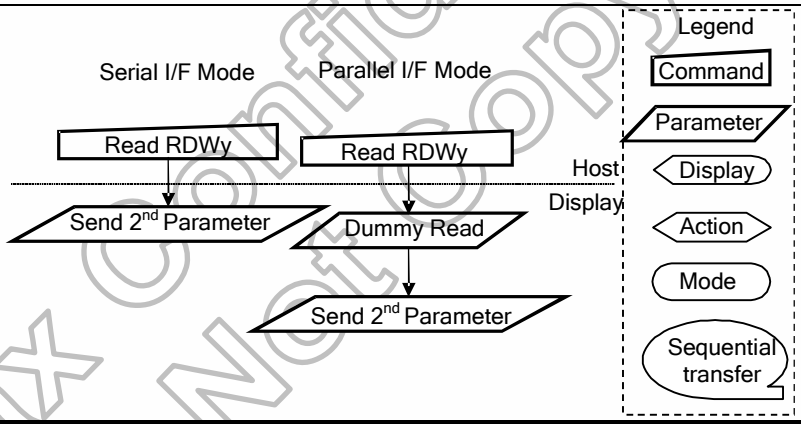
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.59 Read Gx (78h)

78h	RDGx (Read Gx)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	1	0	0	0	78
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	xx
Description	This command returns the Gx bits (Gx[9:2]) of green color characteristics.												
Restriction	-												

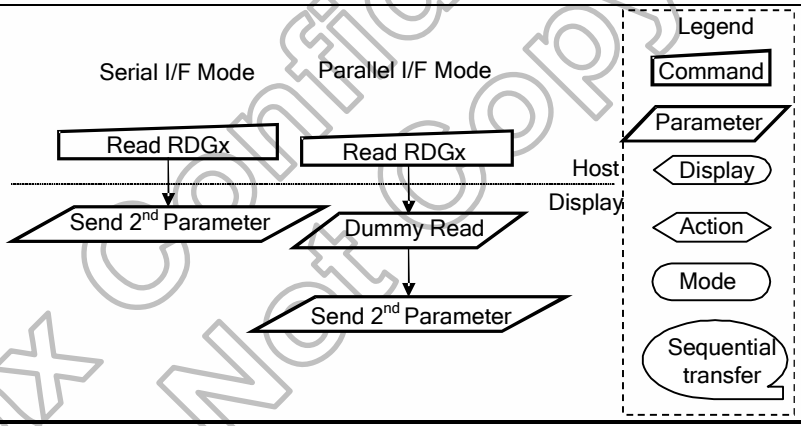
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.60 Read Gy (79h)

79h	RDGy (Read Gy)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	0	1	1	1	79
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	xx
Description	This command returns the Gy bits (Gy[9:2]) of green color characteristics.												
Restriction	-												

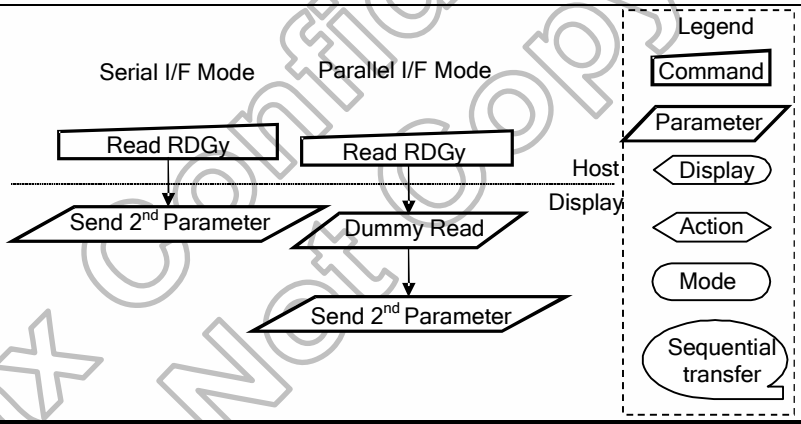
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.61 Read Blue/AColur Low Bits (7Ah)

7Ah	RDBALB (Read Blue/AColour Low Bits)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	1	0	1	0	7A
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	xx
Description	This command returns the lowest bits of blue and A color characteristics. Blue: Bx and By A: Ax and Ay If A is not used Ax[1:0] and Ay[1:0] bits are set to '0's.												
Restriction	-												

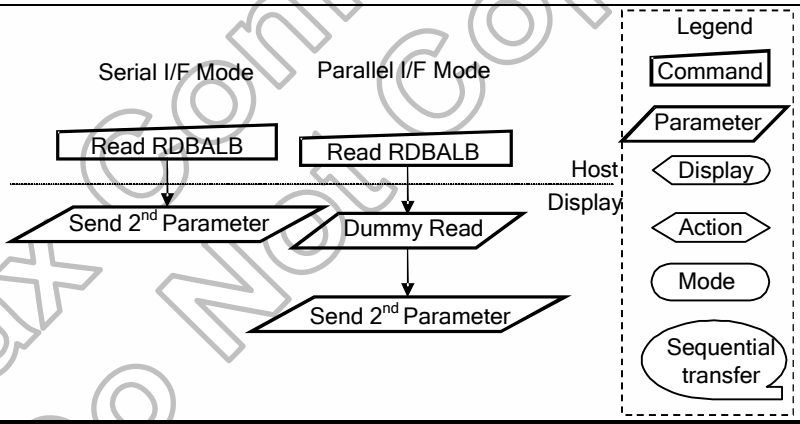
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.62 Read Bx (7Bh)

7Bh	RDBx (Read Bx)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	1	0	1	1	7B
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	xx
Description	This command returns the Bx bits (Bx[9:2]) of blue color characteristics.												
Restriction	-												

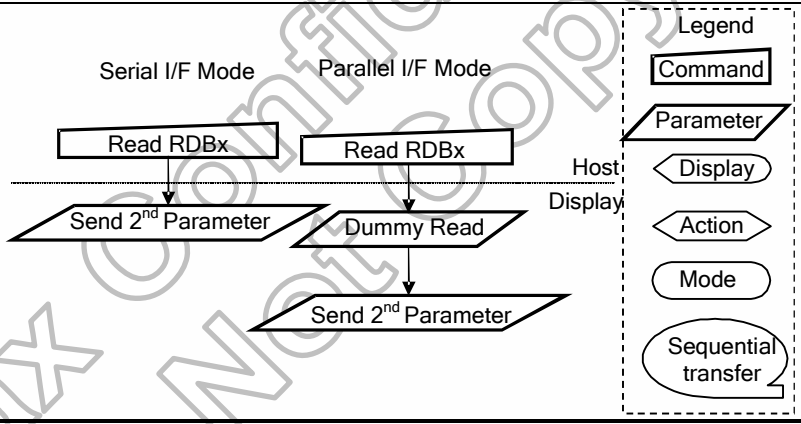
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.63 Read By (7Ch)

7Ch	RDBy (Read By)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	1	1	0	0	7C
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	By9	By8	By7	By6	By5	By4	By3	By2	xx
Description	This command returns the Gy bits (Gy[9:2]) of Blue color characteristics.												
Restriction	-												

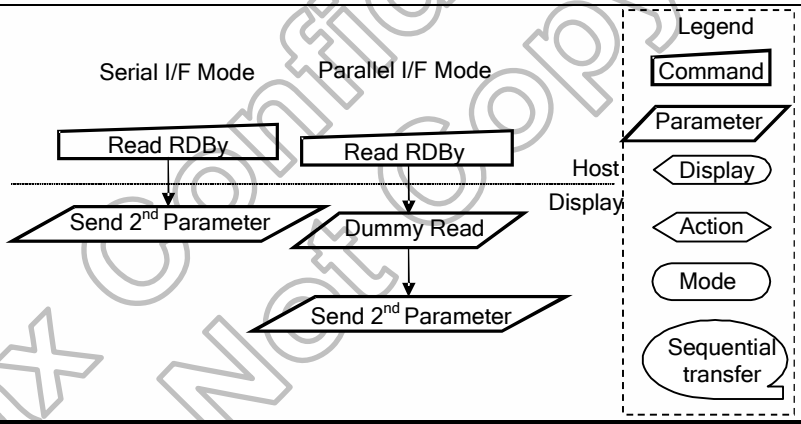
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.64 Read Ax (7Dh)

7Dh	RDAx (Read Ax)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	1	0	0	0	78
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	xx
Description	This command returns the Ax bits (Ax[9:2]) of A color characteristics. Ax[9:2] are set to '0's if they are not used.												
Restriction	-												

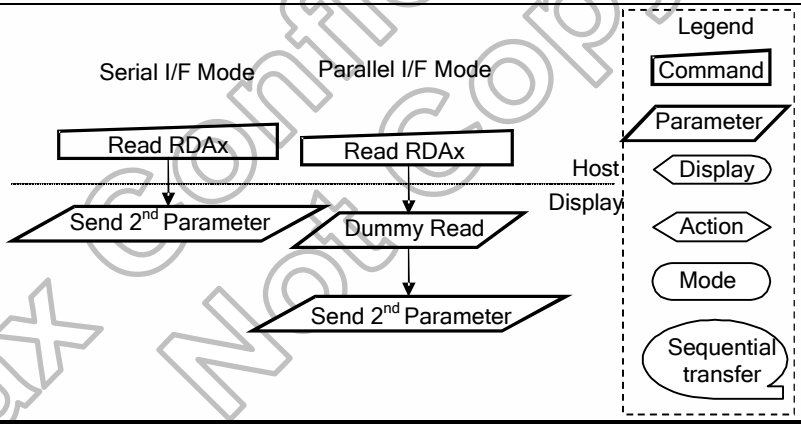
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.65 Read Ay (7Eh)

7Eh	RDAy (Read Ay)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	1	1	1	1	0	7E
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
2nd parameter	1	↑	1	-	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	xx
Description	This command returns the Ay bits (Ay[9:2]) of A color characteristics. Ay[9:2] are set to '0's if they are not used.												
Restriction	-												

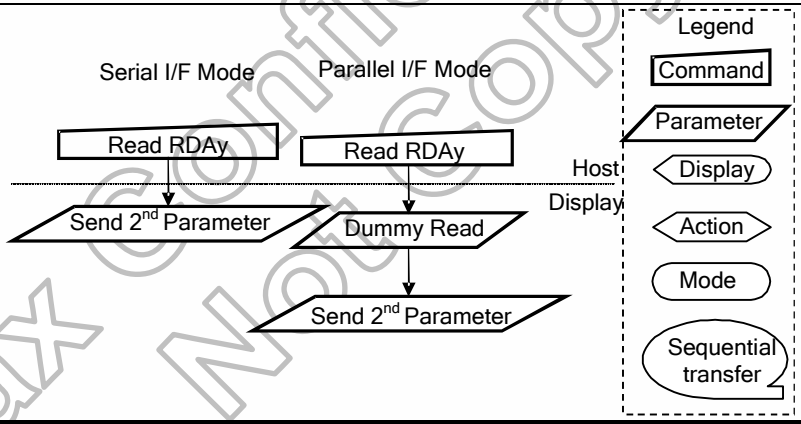
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



6.2.66 Read_DDB_start (A1h)

A1h	Read_DDB_start												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	0	0	0	1	A1
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	X	Dummy read
2nd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
3rd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
4th parameter	1	↑	1		x	x	x	x	x	x	x	x	xx
5th parameter	1	↑	1		x	x	x	x	x	x	x	x	xx
6th parameter	1	↑	1	-	1	1	1	1	1	1	1	1	FF

Description

The format of returned data is as follows:
Parameter 2: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.
Parameter 3: MS (most significant) byte of Supplier ID.
Parameter 4: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.
Parameter 5: MS (most significant) byte of Supplier Elective Data
Parameter 6: single-byte *Escape or Exit Code* (EEC). The code is interpreted as follows:
- FFh - Exit code – there is no more data in the Descriptor Block
- 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard)

Restrictions

-

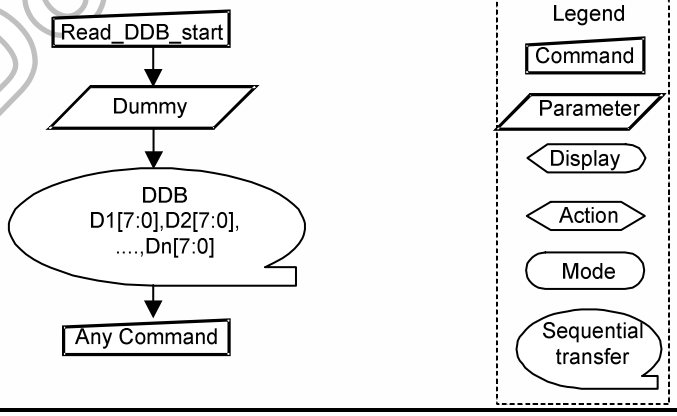
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	PA 2nd~5th =OTP Value, PA 6th =FFh
S/W Reset	PA 2nd~5th =OTP Value, PA 6th =FFh
H/W Reset	PA 2nd~5th =OTP Value, PA 6th =FFh

Flow Chart



6.2.67 Read_DDB_continue (A8h)

A8h	Read_DDB_continue												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	1	0	0	0	A8
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Nth parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx

Description

A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.

Restrictions

-

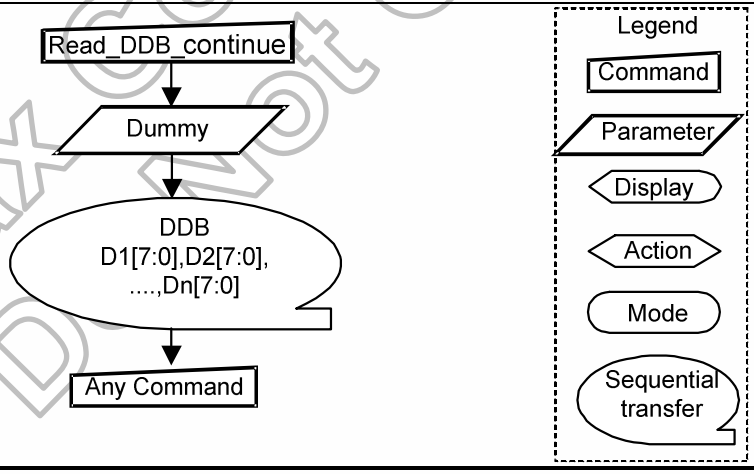
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

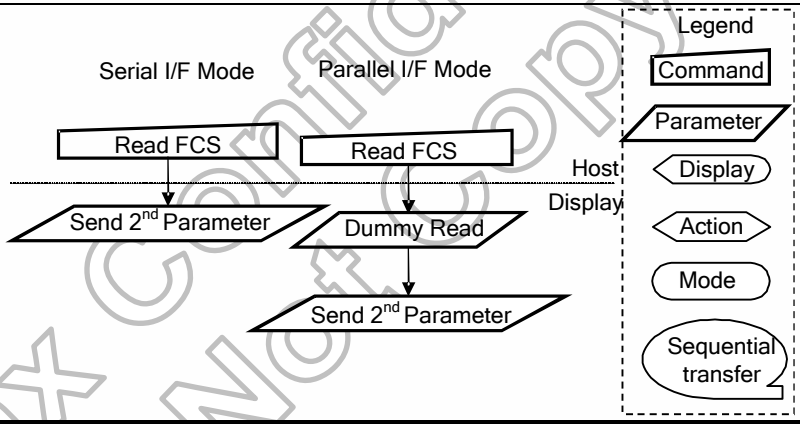
Default

Status	Default value
Power On Sequence	Without reading A1h, read PA 2nd~5th is the same as A1h 2nd~5th OTP value, and the 6th read is FFh.
S/W Reset	Without reading A1h, read PA 2nd~5th is the same as A1h 2nd~5th OTP value, and the 6th read is FFh.
H/W Reset	Without reading A1h, read PA 2nd~5th is the same as A1h 2nd~5th OTP value, and the 6th read is FFh.

Flow Chart



6.2.68 Read first checksum (AAh)

AAH	RDFCS (Read First Checksum)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	1	0	1	0	AA
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read
2nd parameter	1	↑	1	-	FCS[7:0]								xx
Description	This command returns the first checksum what has been calculated from The area registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restrictions	It will be necessary to wait 150ms after there is the last write access on command area registers before there can read this checksum value.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Booster Off / Yes												
Default	FCS[7:0] = 0x00h												
Flow Chart													

6.2.69 Read continue checksum (AFh)

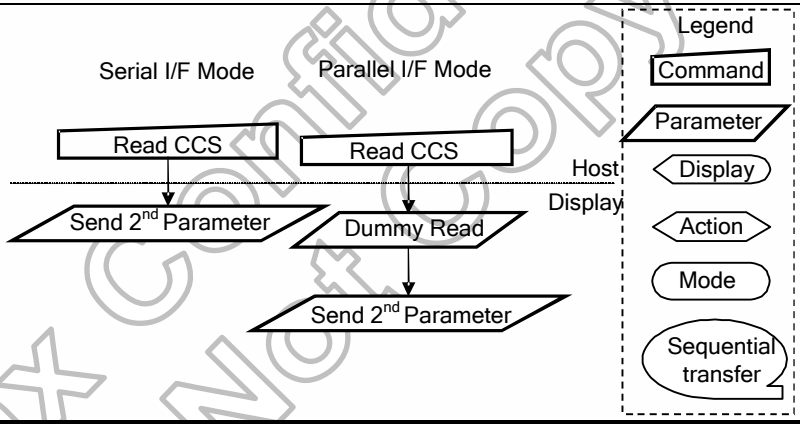
AFH	RDCCS (Read Continue Checksum)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	1	1	1	1	AA
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read
2nd parameter	1	↑	1	-	CCS[7:0]								xx
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from command area registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restrictions	It will be necessary to wait 300ms after there is the last write access on command area registers before there can read this checksum value in the first time.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default: CCS[7:0] = 0x00h

Flow Chart



6.2.70 Read ID1 (DAh)

DA H	RDID1 (Read ID1)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	0	DA
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	module's manufacturer m[7:0]								00
Description	This read byte identifies the LCD module's manufacturer.												
Restriction	-												

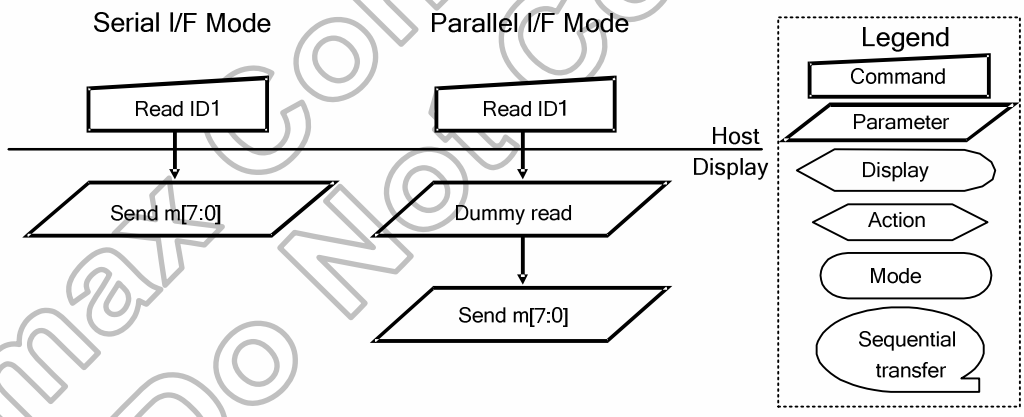
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	xxHEX
S/W Reset	xxHEX
H/W Reset	xxHEX

Flow Chart



6.2.71 Read ID2 (DBh)

DB H	RDID2 (Read ID2)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	1	DB
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	V7	V6	V5	V4	V3	V2	V1	V0	80

Description

This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications.

Restrictions

-

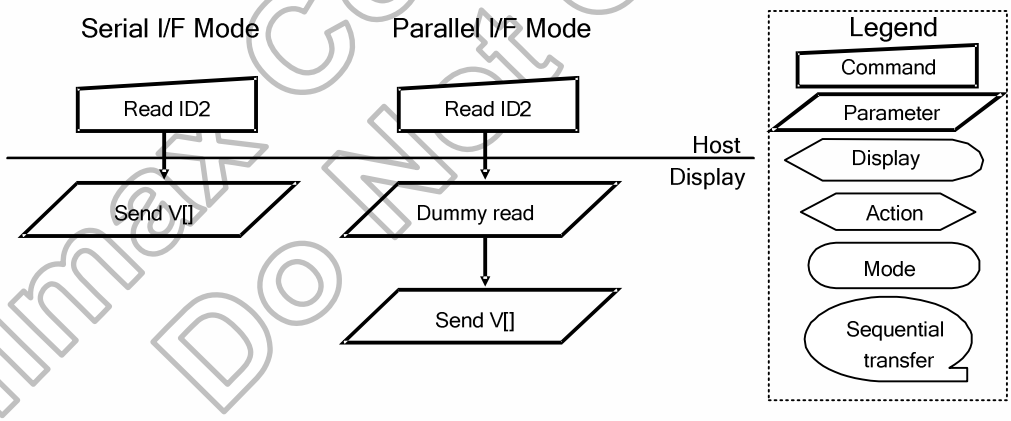
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	xxHEX
S/W Reset	xxHEX
H/W Reset	xxHEX

Flow Chart



6.2.72 Read ID3 (DCh)

DC H	RDID3 (Read ID3)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	1	0	0	DC
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	00
Description	This read byte identifies the LCD module/driver.												
Restrictions	-												

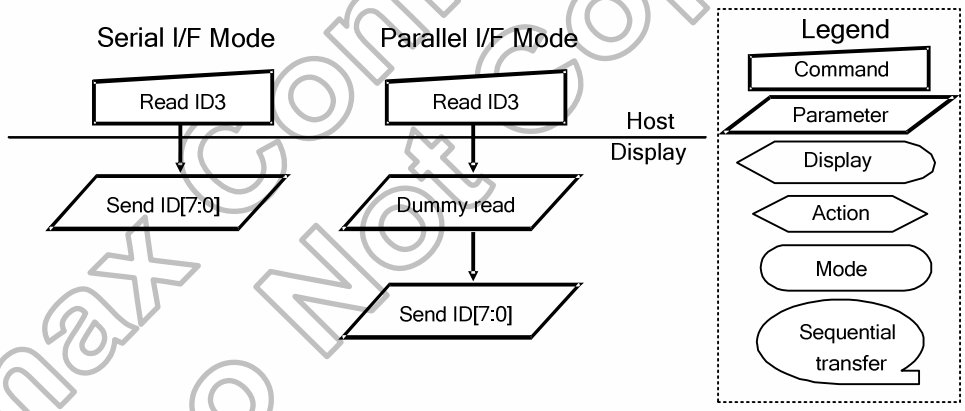
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	xxHEX
S/W Reset	xxHEX
H/W Reset	xxHEX

Flow Chart



6.2.73 SETOSC: set internal oscillator (B0h)

B0 H	SETOSC(Set Internal Oscillator)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	0	0	B0
1st parameter	1	↑	1	-	I_UADJ[3:0]				N_UADJ[3:0]				66
2nd parameter	1	↑	1	-	-	-	-	-	-	-	-	OSC_EN	00

Description

These command is used to set internal oscillator related setting
OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop.

N_UADJ[3:0]: Internal oscillator frequency adjusts in Normal / Partial mode.
I_UADJ[3:0]: Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.

UADJ3	UADJ2	UADJ1	UADJ0	Internal Oscillator Frequency	Display Frame rate
0	0	0	0	50% x 10MHz	30Hz
0	0	0	1	58% x 10MHz	35Hz
0	0	1	0	67% x 10MHz	40Hz
0	0	1	1	75% x 10MHz	45Hz
0	1	0	0	83% x 10MHz	50Hz
0	1	0	1	92% x 10MHz	55Hz
0	1	1	0	100% x 10MHz	60Hz
0	1	1	1	108% x 10MHz	65Hz
1	0	0	0	116% x 10MHz	70Hz
1	0	0	1	125% x 10MHz	75Hz
1	0	1	0	133% x 10MHz	80Hz
1	0	1	1	142% x 10MHz	85Hz
1	1	0	0	150% x 10MHz	90Hz
1	1	0	1	158% x 10MHz	95Hz
1	1	1	0	167% x 10MHz	100Hz
1	1	1	1	175% x 10MHz	105Hz

Restrictions

Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.74 SETPOWER: set power control (B1h)

B1 H	SETPOWER (Set power control)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	0	1	B1
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	DP_STB	00
2nd parameter	1	↑	1	-	-	-	TRI	XDK	-	BT[2:0]			11
3rd parameter	1	↑	1	-	-	-	VRH[5:0]						1C
4th parameter					-	-	NVRH[5:0]						1C
5th parameter	1	↑	1	-	GASEN	-	-	-	-	AP[2:0]			83
6th parameter	1	↑	1	-	FS1[3:0]					FS0[3:0]			5C
7th parameter	1	↑	1	-		VCOMG	1	PON	DK	0	0	STB	29

Description

DP_STB,: These two bits can let the driver into the deep standby mode. And when into deep standby, all display operation stops, including the internal R-C oscillator. In the deep standby mode, the GRAM data and register content are not retained.

XDK, TRI: Specify the ratio of step-up circuit for VSP voltage generation.

TRI	XDK	Step up circuit 1	Capacitor connection pins
0	0	2 x VCI	C11P, C11N
0	1	2 x VCI	C11P, C11N, C12P, C12N
1	0	3 x VCI	C11P, C11N, C12P, C12N
1	1	Setting inhabited	Setting inhabited

VRH[5:0]: Specify the VSPROUT voltage adjusting. VSPROUT voltage is for gamma voltage
NVRH[5:0]: Specify the VSNR voltage adjusting. VSNR voltage is for gamma voltage

TRI=0					
VRH[5:0] NVRH[5:0] (Hex)	VSPROUT VSNROUT (V)	VRH[5:0] NVRH[5:0] (Hex)	VSPROUT VSNROUT (V)	VRH[5:0] NVRH[5:0] (Hex)	VSPROUT VSNROUT (V)
0	3.09/-3.09	B	3.61/-3.61	16	4.13/-4.13
1	3.14/-3.14	C	3.66/-3.66	17	4.17/-4.17
2	3.19/-3.19	D	3.70/-3.70	18	4.22/-4.22
3	3.23/-3.23	E	3.75/-3.75	19	4.27/-4.27
4	3.28/-3.28	F	3.80/-3.80	1A	4.31/-4.31
5	3.33/-3.33	10	3.84/-3.84	1B	4.36/-4.36
6	3.38/-3.38	11	3.89/-3.89	1C	4.41/-4.41
7	3.42/-3.42	12	3.94/-3.94	1D	4.45/-4.45
8	3.47/-3.47	13	3.98/-3.98	1E	4.50/-4.50
9	3.52/-3.52	14	4.03/-4.03	1F	STOP
A	3.56/-3.56	15	4.08/-4.08	20~3F	STOP

TRI=1					
VRH[5:0] NVRH[5:0] (Hex)	VSPROUT VSNROUT (V)	VRH[5:0] NVRH[5:0] (Hex)	VSPROUT VSNROUT (V)	VRH[5:0] NVRH[5:0] (Hex)	VSPROUT VSNROUT (V)
0	3.09/-3.09	12	3.94/-3.94	24	4.78/-4.78
1	3.14/-3.14	13	3.98/-3.98	25	4.83/-4.83
2	3.19/-3.19	14	4.03/-4.03	26	4.88/-4.88
3	3.23/-3.23	15	4.08/-4.08	27	4.92/-4.92
4	3.28/-3.28	16	4.13/-4.13	28	4.97/-4.97
5	3.33/-3.33	17	4.17/-4.17	29	5.02/-5.02
6	3.38/-3.38	18	4.22/-4.22	2A	5.06/-5.06
7	3.42/-3.42	19	4.27/-4.27	2B	5.11/-5.11
8	3.47/-3.47	1A	4.31/-4.31	2C	5.16/-5.16
9	3.52/-3.52	1B	4.36/-4.36	2D	5.20/-5.20
A	3.56/-3.56	1C	4.41/-4.41	2E	5.25/-5.25
B	3.61/-3.61	1D	4.45/-4.45	2F	5.30/-5.30
C	3.66/-3.66	1E	4.50/-4.50	30	5.34/-5.34
D	3.70/-3.70	1F	4.55/-4.55	31	5.39/-5.39
E	3.75/-3.75	20	4.59/-4.59	32	5.44/-5.44
F	3.80/-3.80	21	4.64/-4.64	33~3F	STOP
10	3.84/-3.84	22	4.69/-4.69		
11	3.89/-3.89	23	4.73/-4.73		

Note: Internal VREF can be modified by Custom's special request.
VSPR={Decimal(VRH[5:0])x0.05+3.3 **}*(VREF/4.8) if** TRI=0.
VSNR={Decimal(VRH[5:0])x0.05+3.3 **}*(VREF/5.8) if** TRI=1.
Note: Internal nVREF can be modified by Custom's special request.
VSNR={Decimal(-NVRH[5:0])x0.05-3.3 **}*(nVREF/4.8) if** TRI=0.
VSNR={Decimal(-NVRH[5:0])x0.05-3.3 **}*(nVREF/5.8) if** TRI=1.

BT[2:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation.

BT2	BT1	BT0	VSP	VGH	VGL
0	0	0	5.1V	3VSP	-3 VSP
0	0	1	5.1V	3 VSP	-2 VSP
0	1	0	5.1V	3 VSP	-2 VSP
0	1	1	5.1V	VCI + 2 VSP	-VCI-2 VSP
1	0	0	5.1V	VCI + 2 VSP	-2 VSP
1	0	1	5.1V	VCI + 2 VSP	VCI-2 VSP
1	1	0	5.1V	2 VSP	-2 VSP
1	1	1	5.1V	2 VSP	VCI- VSP

Note: When VCI = 2.8V, TRI=0

FS0[3:0]: Set the operating frequency for VSP and VSN voltage generation.

FS0[3:0] (HEX)	Operation Frequency for VSP and VSN	FS0[3:0] (HEX)	Operation Frequency for VSP and VSN
0	Setting Inhibited	8	Fosc/288
1	Fosc/32	9	Fosc/320
2	Fosc/48	A	Fosc/352
3	Fosc/64	B	Fosc/384
4	Fosc/80	C	Fosc/416
5	Fosc/96	D	Fosc/448
6	Fosc/112	E	Fosc/480
7	Fosc/128	F	Fosc/512

FS1[3:0]: Set the operating frequency for VGH/VGL voltage generation.

FS1[3:0] (HEX)	Operation Frequency for VGH and VGL	FS1[3:0] (HEX)	Operation Frequency for VGH and VGL
0	Setting Inhibited	8	Fosc/288
1	Fosc/32	9	Fosc/320
2	Fosc/48	A	Fosc/352
3	Fosc/64	B	Fosc/384
4	Fosc/80	C	Fosc/416
5	Fosc/96	D	Fosc/448
6	Fosc/112	E	Fosc/480
7	Fosc/128	F	Fosc/512

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Small
0	1	0	Small
0	1	1	Small
1	0	0	Medium
1	0	1	Medium High
1	1	0	Large
1	1	1	Small

STB: When STB = "1", the HX8357-D into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator.
In the standby mode, the GRAM data and register content will be keeping.

GASEN: This stands for abnormal power-off monitor function when the power is off.

DK: Specify on/off control of step-up circuit 1 for VSP voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

PON: Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation.
For detail, see the Power Supply Setting Sequence.

PON	Operation of step-up circuit 2
0	OFF
1	ON

VCOMG: Specify on/off control of step-up circuit 3 for VSN voltage generation. For detail, see the Power Supply Setting Sequence.

VCOMG	Operation of step-up circuit 3
0	OFF
1	ON

Restrictions	Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.75 SETDISPLAY: set display related register (B2h)

B2H	SETDISCTRL (Set display control)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	1	0	B2
1st parameter	1	↑	1	-	-	-	-	-	ISC3	ISC2	ISC1	ISC0	00
2nd parameter	1	↑	1	-	PT1	PT0	-	-	-	-	PTG	REF	83
3rd parameter	1	↑	1	-	-	-	NL[5:0]						3B
3rd parameter	1	↑	1	-	-	SCN[6:0]							00
3rd parameter	1	↑	1	-	-	-	GON	DTE	D1	D0	-	-	20

Description

This command is used to set display related register

D[1:0]: When D1 = '1', display is on; when D1 = '0', display is off. When display is off, the display data is retained in the GRAM and the entire source outputs are set to the VSSD level.
When D[1:0]= '01', the internal display of the HX8357-D is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

D1	D0	Source Output	Internal Display Operations	Gate-Driver Control Signals
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

GON, DTE:

GON	DTE	Gate Output
0	x	Fixed to VGH
1	0	Fixed to VGL
1	1	Normal Operation (VGH/VGL)

PT[1:0] : Specify the Non-display area source output in partial display mode.

		Source Output Level					
REV_Panel	GRAM Data	Display area		Non-display Area			
				PT1-0=(0,*)		PT1-0=(1,0)	PT1-0=(1,1)
		Positive	Negative	Positive	Negative	-	
1 (Normally Black Panel)	18'h00000 . 18'h3FFFF	V63P . V0P	V0N . V63N	V63P	V0N	GND	Hi-z
0 (Normally White Panel)	18'h00000 . 18'h3FFFF	V0P . V63P	V63N . V0N	V63P	V0N		

REF: Refresh display in non-display area in Partial mode enable bit.
REF = '0': Refresh display operation is disabling.
REF = '1': Refresh display operation is enable.

PTG: Specify the scan mode of gate driver in non-display area.

PTG	Gate Outputs in Non-display Area
0	Normal Drive
1	Fixed VGL

ISC[3:0]: Specify the scan cycle of gate driver when **REF** = '1' in non-display area. Then scan cycle is set to Decimal(ISC[3:0])x4+1.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	5 frames	83ms
0	0	1	0	9 frames	150ms
0	0	1	1	13 frames	217ms
0	1	0	0	17 frames	283ms
0	1	0	1	21 frames	350ms
0	1	1	0	25 frames	417ms
0	1	1	1	29 frames	483ms
1	0	0	0	33 frames	550ms
1	0	0	1	37 frames	616ms
1	0	1	0	41 frames	683ms
1	0	1	1	45 frames	750ms
1	1	0	0	49 frames	816ms
1	1	0	1	53 frames	883ms
1	1	1	0	57 frames	950ms
1	1	1	1	Setting inhibited	

NL[5:0]: Set the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL5	NL4	NL3	NL2	NL1	NL0	LCD Drive Lines
0	0	0	0	0	0	8 lines
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
:	:	:	:	:	:	:
1	1	1	0	1	0	472 lines
1	1	1	0	1	1	480 lines
Other Setting						480 lines

SCN[6:0]: Specifies the gate line where the gate driver starts scan.

SCN[6:0]	Scanning Start Position	
	GS=0	GS=1
00h~63h	G(1+SCN[6:0]*4)	G(SCN[6:0]*4+NL[5:0]*8)
Others	Setting inhibited	Setting inhibited

Restrictions	Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.76 SETRGB: set RGB interface (B3h)

B3 H	SETRGBIF(Set RGB interface related register)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	1	1	B3
1st parameter	1	↑	1	-	SDO_EN	BYPASS	EPF[1:0]			-	RM	DM	00
2nd parameter	1	↑	1	-	-	-	-	-	DPL	HSPL	VSPL	EPL	00
3rd parameter	1	↑	1	-	RCM		HBP[5:0]						06
4th parameter	1	↑	1	-			VBP[5:0]						06

Description

This command is used to set RGB interface related register

SDO_EN: SDO Pin Enable.

SDO_EN	Input Pin	Output pin
0	SDA	SDA
1	SDA	SDO

RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting.

RM	Interface for RAM access
0	DBI Interface (MPU)
1	DPI Interface (RGB)

DM bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DPI signal.

DM	Display Mode
0	Internal oscillation clock
1	DPI interface

BYPASS: Select the display data path whether memory or direct to display in RGB interface.

BYPASS	Interface Select
0	Memory
1	Direction to display

Note: When set BYPASS=0, must ensure internal OSC faster than PCLK.

RCM: Select RGB interface mode.

RCM	Interface Select
0	RGB mode 1(VS+HS+DE)
1	RGB mode 2(VS+HS)

BYPASS	RCM	RM	DM	Ram	Display
x	x	0	0	MPU	Internal
x	x	0	1	MPU	V-sync interface
0	0	1	1	RGB1	RGB1
0	1	1	1	RGB2	RGB2
1	0	1	1	RGB1	RGB1
1	1	1	1	RGB2	RGB2

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	Display image	Operation
0	High	Enable	Write data to
0	Low	Disable	Disable
1	High	Disable	Disable
1	Low	Enable	Write data to

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

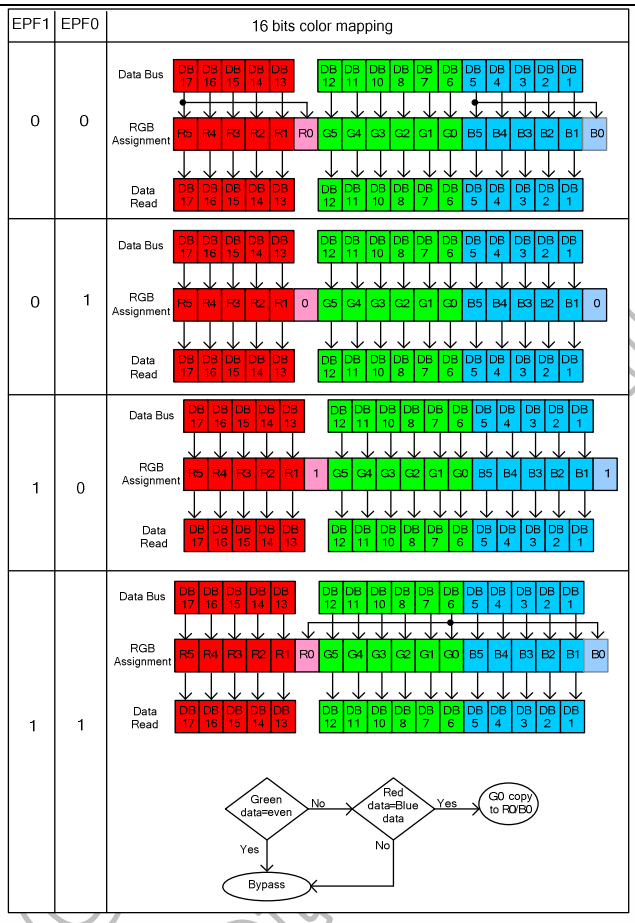
HBP[5:0]: Set the delay period from falling edge of HSYNC signal to first valid data in DPI I/F mode 2

HBP[5:0]	No. of clock cycle of DOTCLK
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
62d	62
63d	Setting Inhibited

VBP[5:0]: Set the delay period from falling edge of VSYNC signal to first valid line in DPI I/F mode 2

VBP[5:0]	No. of clock cycle of HSYNC
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
61d	61
62d	62
63d	Setting Inhibited

EPF[1:0]: 65K color mode data format



Restrictions	Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.77 SETCYC: set display cycle register (B4h)

B4 H	SETCYC(Set display cycle register)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	1	0	0	B4
1st parameter	1	↑	1	-	ZINV	-	I_NW[1:0]		-	-	N_NW[1:0]		02
2nd parameter	1	↑	1	-	-	RTN[6:0]							40
3rd parameter	1	↑	1	-	-	-	-	-	OSC_ DIV2	-	DIV[1:0]		00
4th parameter	1	↑	1	-	N_DUM[7:0]								2A
5th parameter	1	↑	1	-	I_DUM[7:0]								2A
6th parameter	1	↑	1	-	GDON[7:0]								0D
7th parameter	1	↑	1	-	GDOF[7:0]								96

Description

This command is used to set display related register

ZINV: Set Z-inversion mode.

ZINV	Z-inversion
0	Disable
1	Enable

N_ NW[1:0]: Specify LCD driving inversion type in Normal/ Partial mode.
I_ NW[1:0]: Specify LCD driving inversion type in Idle / Partial Idle mode.

NW[1:0]	LCD driving Inversion Type
0d	Column inversion
1d	1-dot inversion
2d	2-dot inversion
3d	4-dot inversion

OSC_DIV2: Set the internal clock divide by 2.

DIV[1:0]: Specify the division ratio of internal clocks mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with these bits.

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Display Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

RTN[6:0]: Specify clock number of one line period for internal operation.
Clock cycles=1/internal operation clock frequency(fosc)

RTN[6:0]	Clock number per Line
00h~7Fh	192+RTN[6:0]*2
Default:40h	320

N_DUM[7:0]: Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.
I_DUM[7:0]: Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

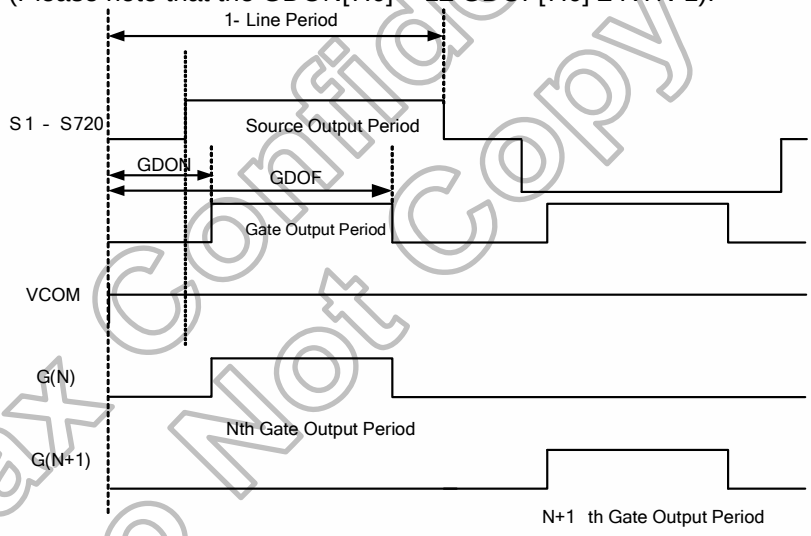
DUM[7:0]	Line number in blanking period
000d	Setting Inhibited
001d	Setting Inhibited
002d	2
003d	3
004d	4

:	:
190d	190
others	Setting Inhibited

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (320+DUM)) [Hz]
fosc: RC oscillation frequency

GDON[7:0]: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting “00h”, “01h”, “02h” is inhibited)**.**

GDOF[7:0]: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the GDON[7:0] + 1≤ GDOF[7:0] ≤ RTN-1).



Restrictions: Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.78 SETBGP (B5h)

B5 H	SETPTBA (Set Power Option)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	1	1	0	1	B5
1st parameter	1	1	↑	-					VREF[3:0]				05
2nd parameter	1	1	↑	-					nVREF[2:0]				05
3rd parameter	1	1	↑	-	VPP[2:0]					VVDHS[2:0]			63

Description

VREF[3:0]: Specify VREF voltage. This command will affect the VSPR voltage.
nVREF[3:0]: Specify nVREF voltage. This command will affect the VSNR voltage.
VSPR={Decimal(VRH[5:0])x0.05+3.3 **}*(VREF/4.8)**
VSNR={Decimal(NVRH[5:0])x0.05+3.3 **}*(nVREF/4.8)**

VREF[3:0]/nVREF				TRI=0 VREF/nVREF	TRI=1 VREF/nVREF
0	0	0	0	4.1V/-4.1V	5.1V/-5.1V
0	0	0	1	4.2V/-4.2V	5.2V/-5.2V
0	0	1	0	4.3V/-4.3V	5.3V/-5.3V
0	0	1	1	4.4V/-4.4V	5.4V/-5.4V
0	1	0	0	4.45V/-4.45V	5.45V/-5.45V
0	1	0	1	4.5V/-4.5V	5.5V/-5.5V
0	1	1	0	4.55V/-4.55V	5.55V/-5.55V
0	1	1	1	4.6V/-4.6V	5.6V/-5.6V
1	0	0	0	4.65V/-4.65V	5.65V/-5.65V
1	0	0	1	4.7V/-4.7V	5.7V/-5.7V
1	0	1	0	4.75V/-4.75V	5.75V/-5.75V
1	0	1	1	4.8V/-4.8V	5.8V/-5.8V
others				Setting disable	Setting disable

VVDHS[2:0]: Specify VSP/VSN voltage.

VVDHS[2:0]			TRI=0 VSP/VSN	TRI=1 VSP/VSN
0	0	0	4.64V/-4.64V	6.08V/-6.08V
0	0	1	4.80V/-4.80V	6.37V/-6.37V
0	1	0	5.07V/-5.07V	6.68V/-6.68V
0	1	1	5.26V/-5.26V	5.59V/-5.59V
1	0	0	5.35V/-5.35V	5.70V/-5.70V
1	0	1	5.47V/-5.47V	5.82V/-5.82V
1	1	0	5.59V/-5.59V	5.95V/-5.95V
1	1	1	5.70V/-5.70V	8.05V/-8.05V

VPP[2:0]: Specify the OTP VPP voltage.

VPP[2:0]			VPP
0	0	0	7.2V
0	0	1	7.3V
0	1	0	7.4V
0	1	1	7.5V
1	0	0	7.6V
1	0	1	7.7V
1	1	0	7.8V
1	1	1	External

Restrictions	SETEXTC turn on to enable this command.

Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Flow Chart	-

6.2.79 SETCOM: set VCOM voltage related register (B6h)

B6 H	SETCOM (Set VCOM Voltage)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	1	1	0	B6
1st parameter	1	↑	1	-	-	VCOM[6:0]							4B
2nd parameter	1	1	↑	-	-	-	-	-	-	VCOM_OTP_TIMES[2:0]			

Description

This command is used to set VCOM Voltage.

VCOM[6:0]: DC VCOM voltage setting.

VCOM [6:0]	VCOM Voltage	VCOM [6:0]	VCOM Voltage	VCOM [6:0]	VCOM Voltage	VCOM [6:0]	VCOM Voltage
00	-2.34	20	-1.74	40	-1.14	60	-0.54
01	-2.33	21	-1.73	41	-1.13	61	-0.53
02	-2.31	22	-1.71	42	-1.11	62	-0.51
03	-2.29	23	-1.69	43	-1.09	63	-0.49
04	-2.27	24	-1.67	44	-1.07	64	-0.47
05	-2.25	25	-1.65	45	-1.05	65	-0.45
06	-2.23	26	-1.63	46	-1.03	66	-0.43
07	-2.21	27	-1.61	47	-1.01	67	-0.41
08	-2.19	28	-1.59	48	-0.99	68	-0.39
09	-2.18	29	-1.58	49	-0.98	69	-0.38
0A	-2.16	2A	-1.56	4A	-0.96	6A	-0.36
0B	-2.14	2B	-1.54	4B	-0.94	6B	-0.34
0C	-2.12	2C	-1.52	4C	-0.92	6C	-0.32
0D	-2.10	2D	-1.50	4D	-0.90	6D	-0.30
0E	-2.08	2E	-1.48	4E	-0.88	6E	-0.28
0F	-2.06	2F	-1.46	4F	-0.86	6F	-0.26
10	-2.04	30	-1.44	50	-0.84	70	-0.24
11	-2.03	31	-1.43	51	-0.83	71	-0.23
12	-2.01	32	-1.41	52	-0.81	72	-0.21
13	-1.99	33	-1.39	53	-0.79	73	-0.19
14	-1.97	34	-1.37	54	-0.77	74	-0.17
15	-1.95	35	-1.35	55	-0.75	75	-0.15
16	-1.93	36	-1.33	56	-0.73	76	-0.13
17	-1.91	37	-1.31	57	-0.71	77	-0.11
18	-1.89	38	-1.29	58	-0.69	78	-0.09
19	-1.88	39	-1.28	59	-0.68	79	-0.08
1A	-1.86	3A	-1.26	5A	-0.66	7A	-0.06
1B	-1.84	3B	-1.24	5B	-0.64	7B	-0.04
1C	-1.82	3C	-1.22	5C	-0.62	7C	-0.02
1D	-1.80	3D	-1.20	5D	-0.60	7D	0.00
1E	-1.78	3E	-1.18	5E	-0.58	7E	0.00
1F	-1.76	3F	-1.16	5F	-0.56	7F	0.00

VCOM_OTP_TIMES[2:0]: Read VCOM OTP programmed times.

VCOM_OTP_TIMES[2:0]	VCOM OTP programmed times
3'b000	Not programmed
3b001	1 time
3'b010	2 times
3'b011	3 times
3'b100	4 times

Restrictions	Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.80 SETOTP: set OTP setting (B7h)

B7 H	SETOTP (Set OTP related setting)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	1	1	1	B7
1st parameter	1	↑	1	-	OTP_KEY[7:0]								FF
2nd parameter	1	↑	1	-	OTP_MASK[7:0]								00
3rd parameter	1	↑	1	-	OTP_INDEX[7:0]								00
4th parameter	1	↑	1	-	LOAD_IDS	VPP_EN	OTP_POR	OTP_PWE	OTP_PTM[1:0]		VPP_SEL	OTP_PROG	00
5th parameter	1	1	↑	-	OTP_DOUT[7:0]								00
Description	This command is used to set the OTP control. **OTP_KEY[7:0]:** "AAh" OTP register access enable and other registers access disable. **OTP_MASK[7:0]:** Bit programming mask. If "1", means don't programming this bit. **OTP_INDEX[7:0]:** Set index of OTP to be programmed. **LOAD_DIS:** When written to "1", OTP load disable. **VPP_EN:** When written to "1", OTP power OP is enable. **OTP_POR:** for OTP read control. When set to from "0" to "1", OTP data can be read the related OTP index at OTP_DOUT[7:0]. **OTP_PROG :** When this bit set to "1", it will programmed to the setting OTP index from related register value. **OTP_PWE :** Internal use, not open. **OTP_PTM[1:0] :** Internal use, not open. **VPP_SEL :** When set to '1', VPP input voltage is fed to OTP. **OTP_DOUT[7:0] :** OTP read data.												
Restrictions	Must enable SETEXTC command												
Register Availability	Status	Availability											
	Normal Mode On, Idle Mode Off, Sleep Out	Yes											
	Normal Mode On, Idle Mode On, Sleep Out	Yes											
	Partial Mode On, Idle Mode Off, Sleep Out	Yes											
	Partial Mode On, Idle Mode On, Sleep Out	Yes											
	Sleep In or Booster Off	Yes											

6.2.81 SETEXTC: enable extension command (B9h)

B9 H	SETEXTC (Set extended command set)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	1	0	0	1	B9
1st parameter	1	↑	1	-	1	1	1	1	1	1	1	1	00
2nd parameter	1	↑	1	-	1	0	0	0	0	0	1	1	00
3rd parameter	1	↑	1	-	0	1	0	0	0	1	1	1	00

Description

This command is used to set extended command set access enable.

Extend cmd	Command description
Enable	After command (B9h), must write 3 parameters (FFh,83h,57h) by order
Disable(default)	After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh,83h,47h)

Restrictions

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.82 SETSTBA (C0h)

C0 H	SETSTBA (Set Source Option)												
	DNC	NRD	NWR	D15~8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	0	0	0	C0
1st parameter	1	1	↑	-	N/P_OPON[7:0]								73
2nd parameter	1	1	↑	-	I/PI_OPON[7:0]								50
3rd parameter	1	1	↑	-	STBA[23:16]								00
4th parameter					STBA[15:8]								3C
5th parameter	1	1	↑	-	STBA[7:0]								C4
6th parameter	1	1	↑	-	GENON[7:0]								-08

Description

This command is used to set source circuit option

N/P_OPON[7:0]: Specify the Normal mode valid source OP period in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode.

I/PI_OPON[7:0]: Specify the IDLE mode valid source OP period in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode.

Clock cycles=1/internal operation clock frequency(fosc)

N/P_OPON[7:0]/ I/PI_OPON[7:0]	Source Period
8'h00	Setting inhabited
8'h01	1 clock cycle
8'h02	2 clock cycles
. . .	. . .
8'hFF	255 clock cycles

STBA[16:10]: Source Bias current fine tune setting.

STBA[9:6]: Source Bias current coarse tune setting.

STBA[4:2]: Gamma Bias current setting.

STBA16	STBA14	STBA13	STBA12	STBA11	STBA10	Fine tune
1	1	1	1	1	1	Very Large
1	0	1	1	1	1	Large
1	0	0	1	1	1	Middle
1	0	0	0	1	1	Small

STBA9	STBA8	STBA7	STBA6	Coarse tune
0	0	1	1	Small
0	0	0	0	Middle
1	1	0	0	Large

STBA4	STBA3	STBA2	Driving Level
1	0	1	Small
1	0	0	Middle Small
1	1	1	Large

GENON[7:0]: Gamma OP on period control The period time value is defined as SYSCLK number in internal clock display mode.

Restrictions	SETEXTC turn on to enable this command.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>N/P_OPON[7:0]=8’h40, I/PI_OPON[7:0]=8’h38, STBA[15:0]=16’h0CC4, GENON[7:0]=8’h10,</td></tr>
<tr><td>S/W Reset</td><td>N/P_OPON[7:0]=8’h40, I/PI_OPON[7:0]=8’h38, STBA[15:0]=16’h0CC4, GENON[7:0]=8’h10</td></tr>
<tr><td>H/W Reset</td><td>N/P_OPON[7:0]=OTP value, I/PI_OPON[7:0]=8’hC0, STBA[11:8]=4’b0000, STBA[7:0]=8’h48, GENON[7:0]=8’h30</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

6.2.83 SETDGC: set DGC related setting (C1h)

C1 H	SETDGC (Set DGC)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	0	0	0	1	C1
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	DGC_EN	00
2nd parameter	1	↑	1	-	DGC_LUT_R00[7:0]								00
3rd parameter	1	↑	1	-	DGC_LUT_R01[7:0]								08
:	1	↑	1	-	:								:
34th parameter	1	↑	1	-	DGC_LUT_R32[7:0]								FC
35th parameter	1	↑	1	-	DGC_LUT_G00[7:0]								00
36th parameter	1	↑	1	-	DGC_LUT_G01[7:0]								08
:	1	↑	1	-	:								:
67th parameter	1	↑	1	-	DGC_LUT_G32[7:0]								FC
68th parameter	1	↑	1	-	DGC_LUT_B00[7:0]								00
69th parameter	1	↑	1	-	DGC_LUT_B01[7:0]								08
:	1	↑	1	-	:								:
100th parameter	1	↑	1	-	DGC_LUT_B32[7:0]								FC
Description	**DGC_EN:** Digital gamma correction enable. '0': Disable '1': Enable For more information about these registers, refer to "5.10.2Gray Voltage Generator for Digital Gamma Correction" section												
Restrictions	Must enable SETEXTC command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.84 SETID: set ID (C3h)

C3 H	SETID (Set ID)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	0	0	1	1	C3
1st parameter	1	↑	1	-	ID1[7:0]								00
2nd parameter	1	↑	1	-	ID2[7:0]								80
3rd parameter	1	↑	1	-	ID3[7:0]								00
4th parameter	1	1	↑	-	-	-	-	-	-	ID_OTP_TIMES[2:0]			00

Description

This command is used to set ID.

ID_OTP_TIMES[2:0]: Read ID OTP programmed times.

ID_OTP_TIMES[2:0]	ID OTP programmed times
3'b000	Not programmed
3'b001	1 time
3'b010	2 times
3'b011	3 times
3'b100	4 times

Restrictions

Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.85 SETDDB: Set DDB (C4h)

C4h	SETDDB (Set DDB)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	1	0	0	C4
1st parameter	1	1	↑	-	DDB1[7:0]								00
2nd parameter	1	1	↑	-	DDB2[7:0]								00
3rd parameter	1	1	↑	-	DDB3[7:0]								00
4th parameter	1	1	↑	-	DDB4[7:0]								00
Description	This command is used to set DDB value.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.2.86 SETCABC: set CABC related setting (C9h)

C9 H	SETCABC(Set CABC Related Setting)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	1	0	0	1	C9
1st parameter	1	↑	1	-	BC_ ON	PWMDIV[2:0]			1	1	INVP LUS	1	0F
2nd parameter	1	↑	1	-	PWM_PERIOD[7:0]								82

Description

This command is used to set CABC parameter

BC_ON: The control reigister for LED driver when IC needs enable signal.
'0': CABC_ON pin='L'
'1': CABC_ON pin='H'

INVPLUS: The backlight PWM output polarity select.
'0', The backlight PWM output is low level active.
'1', The backlight PWM output is high level active.

PWMDIV[2:0]: Internal PWM_CLK divider for CABC clock.

PWMDIV[2:0]			Brightness Control Clock
0	0	0	PWM_CLK / 1
0	0	1	PWM_CLK / 2
0	1	0	PWM_CLK / 4
0	1	1	PWM_CLK / 8
1	0	0	PWM_CLK / 16
1	0	1	PWM_CLK / 32
1	1	0	PWM_CLK / 64
1	1	1	PWM_CLK / 128

PWM_PERIOD[7:0]: The backlight PWM output period setting.
Backlight PWM output period = 1 / (PWM_CLK / clock divider (PWMDIV)) x (256x(PWM_PERIOD[7:0]+1)).

Restrictions

Must enable SETEXTC command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.87 SETPanel: set panel characteristic (CCh)

CCH	SETPANEL(Set Panel characteristic register)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	1	1	0	0	CC
1st parameter	1	↑	1	-	-	-	-	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	00
Description	This command is used to set Panel characteristic related register **REV_PANEL:** The source output data polarity selected. '0': normally white panel. '1': normally black panel. **BGR_PANEL:** The color filter order direction selected. '0': S1:S2:S3='R':'G':'B' '1': S1:S2:S3='B':'G':'R' **GS_PANEL:** The gate driver output shift direction selected. '0': G1→G480 '1': G480→G1 **SS_PANEL:** The source driver output shift direction selected. '0': S1→S960 '1': S960→S1 **SM_PANEL**: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin.												
Restrictions	Must enable SETEXTC command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.88 SETGamma: set gamma curve (E0h)

E0H	SETGAMMA (Set Gamma Curve Related Setting)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	0	0	0	0	E0
1st parameter	1	1	↑	-	-	VRP0[6:0]							0B
2nd parameter	1	1	↑	-	-	VRP1[6:0]							0C
3rd parameter	1	1	↑	-	-	VRP2[6:0]							11
4th parameter	1	1	↑	-	-	VRP3[6:0]							1D
5th parameter	1	1	↑	-	-	VRP4[6:0]							25
6th parameter	1	1	↑	-	-	VRP5[6:0]							37
7th parameter	1	1	↑	-	-	VRP6[6:0]							43
8th parameter	1	1	↑	-	-	VRP7[6:0]							4B
9th parameter	1	1	↑	-	-	VRP8[6:0]							4E
10th parameter	1	1	↑	-	-	VRP9[6:0]							47
11th parameter	1	1	↑	-	-	VRP10[6:0]							41
12th parameter	1	1	↑	-	-	VRP11[6:0]							39
13th parameter	1	1	↑	-	-	VRP12[6:0]							35
14th parameter	1	1	↑	-	-	VRP13[6:0]							31
15th parameter	1	1	↑	-	-	VRP14[6:0]							2E
16th parameter	1	1	↑	-	-	VRP15[6:0]							21
17th parameter	1	1	↑	-	-	VRN0[6:0]							1C
18th parameter	1	1	↑	-	-	VRN1[6:0]							1D
19th parameter	1	1	↑	-	-	VRN2[6:0]							1D
20th parameter	1	1	↑	-	-	VRN3[6:0]							26
21th parameter	1	1	↑	-	-	VRN4[6:0]							31
22th parameter	1	1	↑	-	-	VRN5[6:0]							44
23th parameter	1	1	↑	-	-	VRN6[6:0]							4E
24th parameter	1	1	↑	-	-	VRN7[6:0]							56
25th parameter	1	1	↑	-	-	VRN8[6:0]							44
26th parameter	1	1	↑	-	-	VRN9[6:0]							3F
27th parameter	1	1	↑	-	-	VRN10[6:0]							39
28th parameter	1	1	↑	-	-	VRN11[6:0]							33
29th parameter	1	1	↑	-	-	VRN12[6:0]							31
30th parameter	1	1	↑	-	-	VRN13[6:0]							2E
31th parameter	1	1	↑	-	-	VRN14[6:0]							28
32th parameter	1	1	↑	-	-	VRN15[6:0]							1D
33th parameter	1	1	↑	-	CGN1[1:0]		CGN0[1:0]		E0		CGP0[1:0]		E0
34th parameter	1	1	↑	-			00					GMA_RELOAD	00

Description

GMA_RELOAD: Enable this gamma register function.

Positive/Negative Polarity	Description
VRP0/VRN0	Variable resistor (VR0)for V0 offset adjustment
VRP1/VRN1	Variable resistor (VR1)for V1 offset adjustment
VRP2/VRN2	Variable resistor (VR2)for V2 offset adjustment
VRP3/VRN3	Variable resistor (VR3)for V4 offset adjustment
VRP4/VRN4	Variable resistor (VR4)for V6 offset adjustment
VRP5/VRN5	Variable resistor (VR5)for V13 offset adjustment
VRP6/VRN6	Variable resistor (VR6)for V20 offset adjustment
VRP7/VRN7	Variable resistor (VR7)for V27 offset adjustment
VRP8/VRN8	Variable resistor (VR8)for V36 offset adjustment
VRP9/VRN9	Variable resistor (VR9)for V43 offset adjustment
VRP10/VRN10	Variable resistor (VR10)for V50 offset adjustment
VRP11/VRN11	Variable resistor (VR11)for V57 offset adjustment
VRP12/VRN12	Variable resistor (VR12)for V59 offset adjustment
VRP13/VRN13	Variable resistor (VR13)for V61 offset adjustment

<table>
<tr><td></td><td>
<table>
<tr><td>VRP15/VRN15</td><td>Variable resistor (VR15)for V63 offset adjustment</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td>SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

6.2.89 SETIMAGE: set image function (E9h)

EAh	SETMESSI (Set Command type)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	1	0	0	1	E9
1st parameter	1	1	↑	-	PWM2_EN	-	DITH_EN	YUV_EN	-	-		DB_EN	00
Description	**DB_EN:** Enable 24-bits Data Bus, user can using DB23~DB0 as 24-bits data input. **YUV_EN:** Enable YUV function for 24-bits input transform. **DITH_EN:** Enable DITH function for 24-bits input transform. **PWM2_EN:** Enable CABC_PWM2 as CABC PWM output.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.90 SETMESSI: Set Command type (EAh)

EAh	SETMESSI (Set Command type)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	1	0	1	0	EA
1st parameter	1	1	↑	-	-	-	-	-	-	-	SPI_DCX_SEL	MESSI_ENB	02
Description	**MESSI_ENB:** Command select **SPI_DCX_SEL:** DCX select in 4-wrie SPI Interface. SPI_DCX_SEL: 0 → DCX: 8th SCL; 1 → DCX: 1st SCL												
Restrictions	SETEXTC turn on to enable this command.												
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Partial Mode On, Idle Mode Off, Sleep Out — Yes Partial Mode On, Idle Mode On, Sleep Out — Yes Sleep In or Booster Off — Yes												

6.2.91 SETCOLOR: set color (EBh)

EBh	SETCOLOR (Set Color)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	1	0	1	1	EB
1st parameter	1	1	↑	-	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	-
2nd parameter	1	1	↑	-	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	-
3rd Parameter	1	1	↑	-	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	-
4th Parameter	1	1	↑	-	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	-
5th Parameter	1	1	↑	-	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	-
6th Parameter	1	1	↑	-	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	-
7th Parameter	1	1	↑	-	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	-
8th Parameter	1	1	↑	-	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	-
9th Parameter	1	1	↑	-	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	-
10th Parameter	1	1	↑	-	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	-
11th Parameter	1	1	↑	-	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	-
12th Parameter	1	1	↑	-	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	-
13th Parameter	1	1	↑	-	By9	By8	By7	By6	By5	By4	By3	By2	-
14th Parameter	1	1	↑	-	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	-
15th Parameter	1	1	↑	-	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	-
Description	**Bkx[9:0]:** Set the Bkx bits of black color characteristics. **Bky[9:0]:** Set the Bky bits of black color characteristics. **Wx[9:0]:** Set the Wx bits of white color characteristics. **Wy[9:0]:** Set the Wy bits of white color characteristics. **Rx[9:0]:** Set the Rx bits of red color characteristics. **Ry[9:0]:** Set the Ry bits of red color characteristics. **Gx[9:0]:** Set the Gx bits of green color characteristics. **Gy[9:0]:** Set the Gy bits of green color characteristics. **Bx[9:0]:** Set the Bx bits of blue color characteristics. **By[9:0]:** Set the By bits of blue color characteristics. **Ax[9:0]:** Set the Ax bits of A color characteristics. **Ay[9:0]:** Set the Ay bits of A color characteristics.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.92 SETREADINDEX: set SPI read index (FEh)

FEh	SET SPI READ INDEX (Set SPI READ Command Address)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	1	1	1	1	0	FE
1st parameter	1	1	↑	-	CMD_ADD[7:0]								-
Description	SET SPI READ Command Address for User Define Command.												
Restrictions	SETEXTC turn on to enable this command												
Register Availability													

Status	Availability
Idle Mode Off, Sleep Out	Yes
Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

6.2.93 GETSPIREAD: SPI Read Command Data (FFh)

FFh	GETSPIREAD (Read Command Data)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	1	1	1	1	1	FF
1st parameter	1	↑	1	-	CMD_DATA1[7:0]								-
:	1	↑	1	-	:								-
nth parameter	1	↑	1	-	CMD_DATAn[7:0]								-
Description	Read SPI Command Data for User Define Command.												
Restrictions	SETEXTC turn on to enable this command.												
Register Availability	Status	Availability											
	Idle Mode Off, Sleep Out	Yes											
	Idle Mode On, Sleep Out	Yes											
	Sleep In or Booster Off	Yes											

6.2.94 GETICID: IC ID Read Command Data (D0h)

D0h	GETSPIREAD (Read Command Data)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	0	0	0	0	D0
1st parameter	1	↑	1	-	DUMMY								-
2nd parameter	1	↑	1	-	HIMAX_ID								99
Description	Read HX8357-D ID=99h.												
Restrictions	SETEXTC turn on to enable this command.												
Register Availability	Status	Availability											
	Idle Mode Off, Sleep Out	Yes											
	Idle Mode On, Sleep Out	Yes											
	Sleep In or Booster Off	Yes											

7. Layout Recommendation

TBD

Figure 7.1: Layout recommendation of HX8357-D00/D01

7.1Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	5	Ω
VCI	Power supply	5	Ω
HSI_VCC	Power supply	10	Ω
VSSA	Power supply	5	Ω
HSI_VSS	Power supply	10	Ω
VSSD	Power supply	5	Ω
OSC	Input	100	Ω
IM[2:0]	Input	100	Ω
RDX, WRX_SCL, DCX, CSX, DIN_SDA	Input	100	Ω
RESX	Input	100	Ω
TE, CABC_PWM, CABC_ON,DOUT	Output	100	Ω
DB[23:0]	I/O	100	Ω
HSI_DN,HSI_DP,HSI_CN,HSI_CP	I/O	10	Ω
PCLK, DE, VSYNC, HSYNC	Input	100	Ω
VGH	Output	10	Ω
VGL	Output	10	Ω
HSI_LDO	Capacitor connection	20	Ω
VCOMDC	Output	10	Ω
VSN	Capacitor connection	5	Ω
VSP	Capacitor connection	5	Ω
VDDD	Capacitor connection	5	Ω
VSPROUT,VSNROUT, NVDDDOUT	Output	50	Ω
C13A, C13B, C14A, C14B	Capacitor connection	5	Ω
C11A, C11B ,C12A, C12B	Capacitor connection	5	Ω
TEST[3:1]	Input	100	Ω
DUMMY_VCL	Dummy	100	Ω
VCOM	Panel connection	5	Ω
C22B, C22A	Capacitor connection	5	Ω
DUMMY	Dummy	100	Ω
VTEST, NVTEST	Test Pin	100	Ω

7.2External components connection

Capacitor	Recommended voltage	Capacity
C1 (C13A/B)	10V	1 µF (B characteristics)
C2 (C11A/B)	10V	1 µF (B characteristics)
C3 (VSP)	10V	1 µF ~ 2.2uF (B characteristics)
C4 (C14A/B)	10V	1 µF (B characteristics)
C5 (C12A/B)	10V	1 µF (B characteristics)
C6 (VSN)	10V	1 µF~2.2uF (B characteristics)
C7 (C22A/B)	16V	1 µF (B characteristics)
C8 (VGH)	25V	1 µF (B characteristics)
C9(VDDD)	6V	1 µF (B characteristics)
C10(HSI_LDO)	6V	1 µF (B characteristics)
D1 (VGL-VSSA)	Schottky Diode	VF < 0.4V / 20mA at 25℃, VR ≥30V (Recommended diode: RB521S-30)

Note: If not use High speed interface (DSI), the capacitor of HSI_LDO can be removed.

8. Electrical Characteristic

8.1Absolute maximum ratings

Item	Symbol	Unit	Spec.			Note
			Min.	Typ.	Max.	
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3	-	+4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3	-	+4.6	Note(3)
Power Supply Voltage 3	VSP ~ VSSA	V	-0.3	-	+6.6	Note(4)
Power Supply Voltage 4	VSSA ~ VSN	V	-0.3	-	+6.6	Note(5)
Power Supply Voltage 5	VGH ~ VSSA	V	-0.3	-	+18.5	Note(6)
Power Supply Voltage 6	VSSA ~ VGL	V	-16.5	-	0	Note(7)
Logic Input Voltage	V_{IN}	V	-0.3	-	IOVCC+0.5	-
Logic Output Voltage	Vo	V	-0.3	-	IOVCC+0.5	-
Operating Temperature	Topr	℃	-40	-	+85	Note(8),(9)
Storage Temperature	Tstg	℃	-55	-	+110	Note(8),(9)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure VSP ≥ VSSA.
(5) To make sure VSSA ≥ VSN.
(6) To make sure VGH ≥ VSSA.
(7) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(8) For die and wafer products, specified up to +85℃.
(9) This temperature specifications apply to the TCP package.

Table 8.1: Absolute maximum ratings

8.2DC characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
IO Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Driver Operating voltage	VCI	Operation voltage	2.5	2.8	3.3	
Source Drive Voltage	VSPROUT	Dual Pump				
	VSPROUT	Triple Pump				
	VSNROUT	Dual Pump				
	VSNROUT	Triple Pump				
Gate Drive High Voltage	VGH	VCI=2.8V Dual Pump (Typ:BT=001)				
		IVGH=80uA				
		IVGH=70uA				
		IVGH=60uA				
		IVGH=50uA				
		IVGH=40uA				
Gate Drive Low Voltage	VGL	VCI=2.8V Dual Pump (Typ:BT=001)	-	-	-	
		IVGL=-80uA				
		IVGL=-70uA				
		IVGL=-60uA				
		IVGL=-50uA				
		IVGL=-40uA				
Drive Supply Voltage	|VGH-VGL|	-	-	-	32	
Input / Output						
High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	µA
Oscillator frequency	fOSC	Frame rate at 60hz,default Vs and Hs setting Ta=25℃				MHz
Booster(VCI=2.8V)						
VSP boost voltage	VSP	Dual Pump IVSP=1mA				V
		Triple Pump IVSP=1mA				
VSN boost voltage	VSN	Dual Pump IVSN=-1mA				
		Triple Pump IVSN=-1mA				
VCOM Generator(VCI=2.8V)						
VCOM amplitude	VCOM	No load,	-2.5	-	0	V
Source Driver(Typ:Ta=25℃ VCI=2.8v)						
Output voltage deviation (mean value)	DVOS	VSSD+1.0 ~ VSPROUT-1.0	-	+/- 10	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VSPROUT-1.0 ~ VSPROUT-0.1V	-	+/- 30	+/- 50	mV
Output voltage range	VOS	-	0.1	-	VSP-0.1	V
Output offset voltage	Voff	-		+/-30	+/-50	mV
Current Consumption(Typ: T_A=25℃ IOVCC=VCI=2.8V)						
Sleep in(MPU mode)	Iiovcc	-	-	-	TBD	µA
	Ivci	-	-	-	TBD	µA

8.3 AC characteristics

8.4 DBI Type B interface characteristic

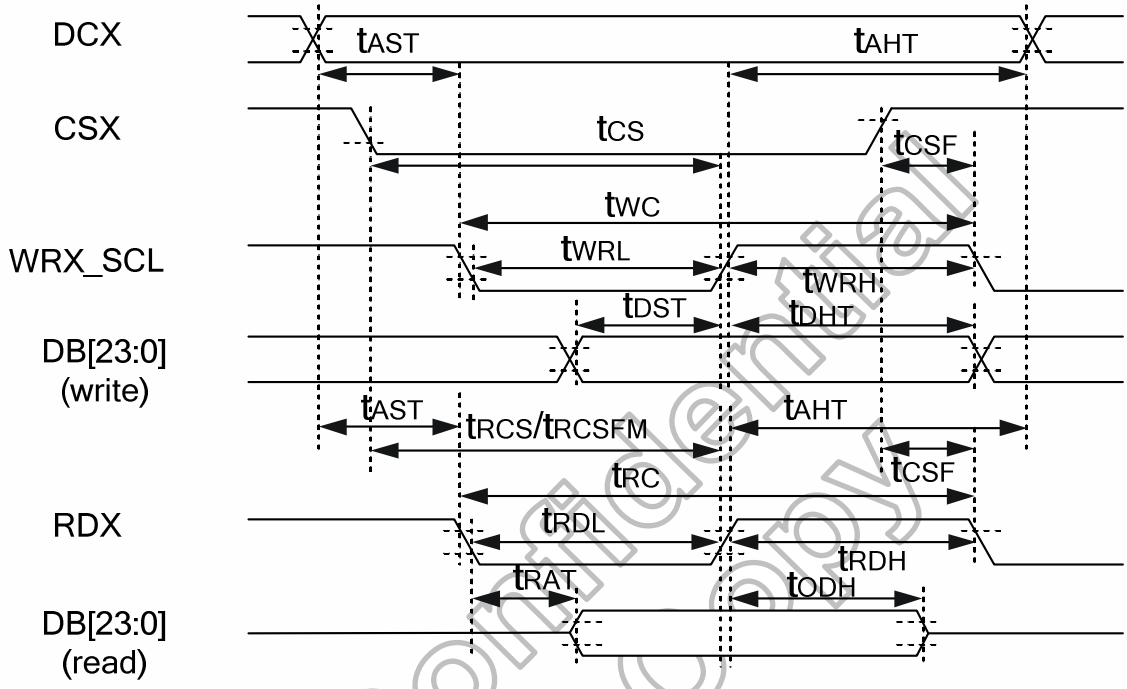


Figure 8.1: DBI Type B interface characteristics

(VSSA=0V, VDD1=1.8V, VDD3=2.8V, T_A=25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
CSX	t_{CS}	Chip select setup time (Write)	10	-	ns	-
	t_{RCS}	Chip select setup time (Read register)	45	-		
	t_{RCSFM}	Chip select setup time (GRAM)	355	-		
	t_{CSF}	Chip select wait time (Write/Read)	10	-		
WRX_SCL	t_{WC}	Write cycle (write register)	50	-	ns	-
	t_{WC}	Write cycle (write GRAM@SLPOUT)	47	-		
	t_{WC}	Write cycle (write GRAM@SLPIN)	100	-		
	t_{WRH}	Control pulse “H” duration	15	-		
	t_{WRL}	Control pulse “L” duration	15	-		
RDX	t_{RC}	Read cycle (read register)	160	-	ns	-
	t_{RC}	Read cycle (GRAM)	450	-		
	t_{RDH}	Control pulse “H” duration	90	-		
	t_{RDL}	Control pulse “L” duration(read register)	35	-		
	t_{RDL}	Control pulse “L” duration(GRAM)	345	-		
DB[23:0]	t_{DST}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	10	-		
	t_{RAT}	Read access time(read register)	-	40		
	t_{RAT}	Read access time(GRAM)	-	340		
	t_{ODH}	Output disable time	20	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.2: DBI Type B interface characteristics

8.4.1 DBI Type C interface characteristics

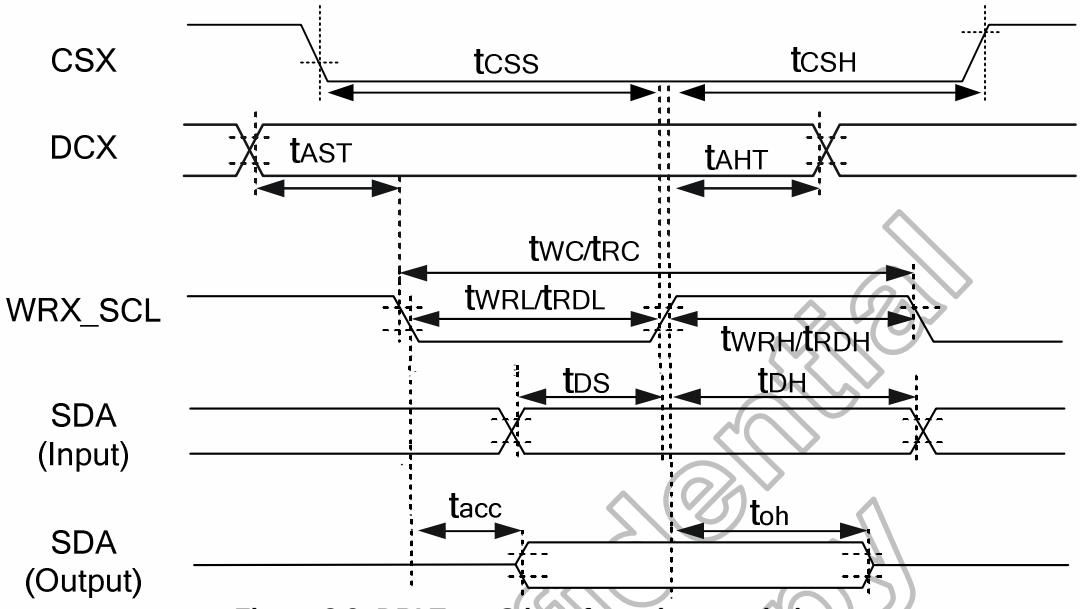


Figure 8.2: DBI Type C interface characteristics

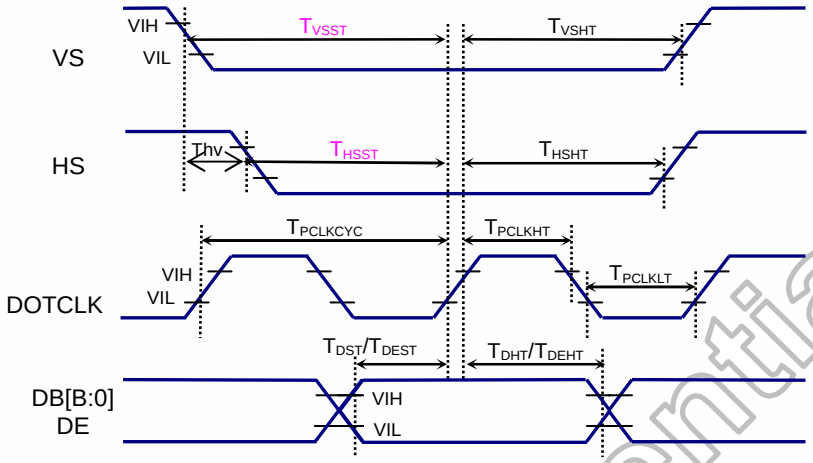
(VSSA=0V, IOVCC=1.8V, VCI=2.8V, T_A = 25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS}	Chip select setup time (Write)	15	-	ns	-
	t_{CSS}	Chip select setup time (Read)	60	-		
	t_{CSH}	Chip select hold time (Write)	15	-		
	t_{CSH}	Chip select hold time (Read)	65	-		
DCX	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
WRX_SCL (Write)	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse “H” duration	15	-		
	t_{WRL}	Control pulse “L” duration	15	-		
WRX_SCL (Read)	t_{RC}	Read cycle	150	-	ns	-
	t_{RDH}	Control pulse “H” duration	60	-		
	t_{RDL}	Control pulse “L” duration	60	-		
SDA (Input)	t_{DS}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DH}	Data hold time	10	-		
SDA (Output)	t_{ACC}	Read access time	10	50	ns	
	t_{OH}	Output disable time	15	50		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 8.3: DBI Type C interface characteristics

8.4.2 DPI interface characteristics



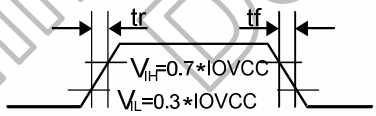
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,T_A = -30 to 70℃)

Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Pixel low pulse width	T_{CLKLT}		15	-	-	ns
Pixel high pulse width	T_{CLKHT}		15	-	-	ns
Vertical Sync. set-up time	T_{VSST}		15	-	-	ns
Vertical Sync. hold time	T_{VSHT}		15	-	-	ns
Horizontal Sync. set-up time	T_{HSST}		15	-	-	ns
Horizontal Sync. hold time	T_{HSHT}		15	-	-	ns
Data Enable set-up time	T_{DEST}		15	-	-	ns
Data Enable hold time	T_{DEHT}		15	-	-	ns
Data set-up time	T_{DST}		15	-	-	ns
Data hold time	T_{DHT}		15	-	-	ns
Phase difference of sync signal falling edge	Thv		0	-	320	Dotclk

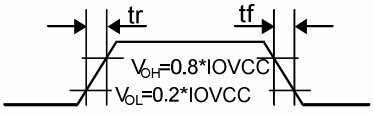
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Table 8.4: DPI interface characteristics-1

Input Signal Slope



Output Signal Slope



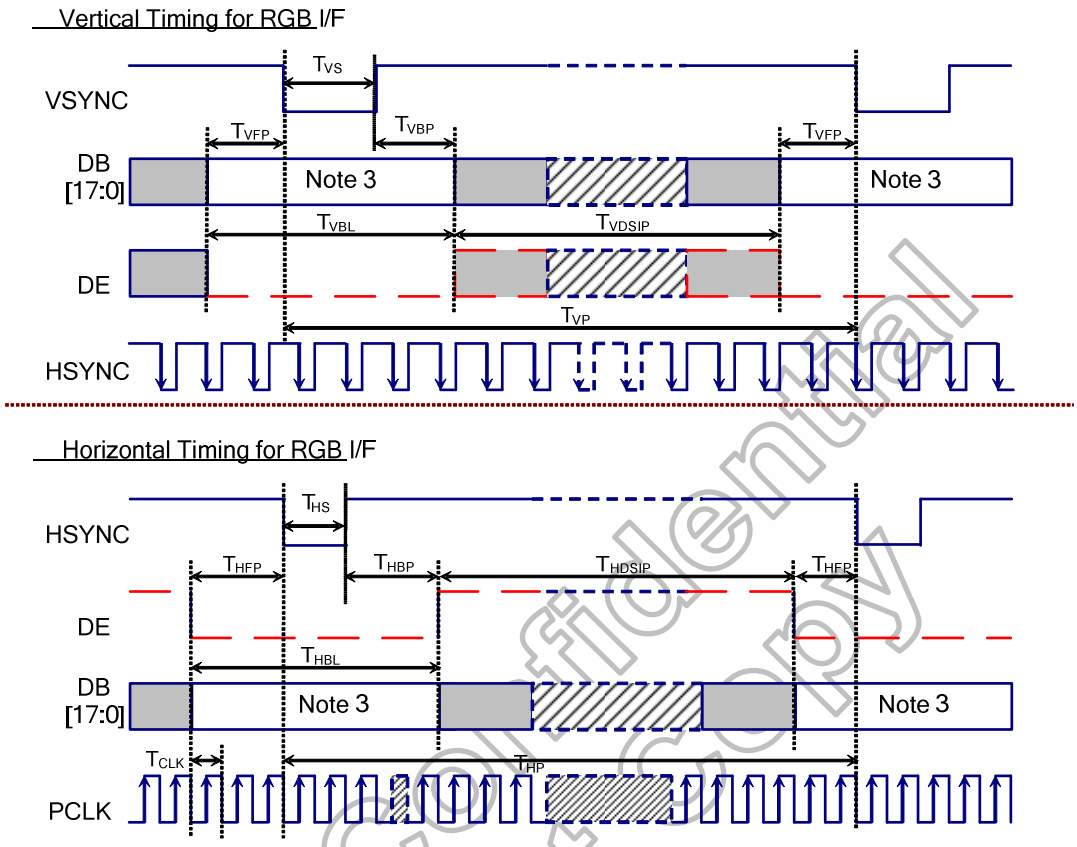


Figure 8.3: General timings for RGB I/F-2

Item	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Vertical Timing						
Vertical cycle period	T_{VP}	-	486	-	-	HS
Vertical low pulse width	T_{VS}	-	2	-	-	HS
Vertical front porch	T_{VFP}	-	2	-	-	HS
Vertical back porch	T_{VBP}	-	2	-	-	HS
Vertical blanking period	T_{VBL}	$T_{VBP} + T_{VFP}$	6	-	-	HS
Vertical active area	T_{VDISP}	-	-	480	-	HS
			-		-	HS
					-	HS
Vertical refresh rate	T_{VRR}	Frame rate	50	60	70	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	326	-	-	DOTCLK
Horizontal low pulse width	T_{HS}	-	2	-	-	DOTCLK
Horizontal front porch	T_{HFP}	-	2	-	-	DOTCLK
Horizontal back porch	T_{HBP}	-	2	-	-	DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP} + T_{HFP}$	6	-	-	DOTCLK
Horizontal active area	T_{HDISP}	-	-	320	-	DOTCLK
Pixel clock cycle TVRR=60Hz	f_{CLKCYC}	-	9	-	-	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(3) HP is multiples of PCLK.

Table 8.5: DPI interface characteristics-2

8.4.3 Reset input timing

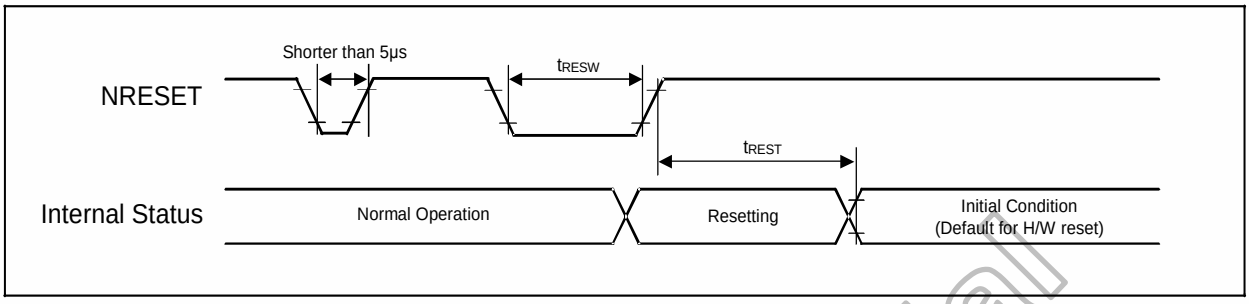


Figure 8.4: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	5	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 8.6: Reset input timing

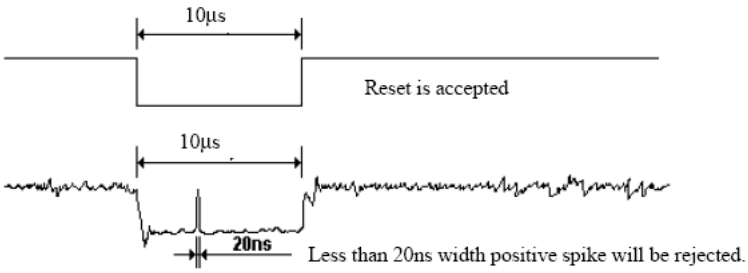
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

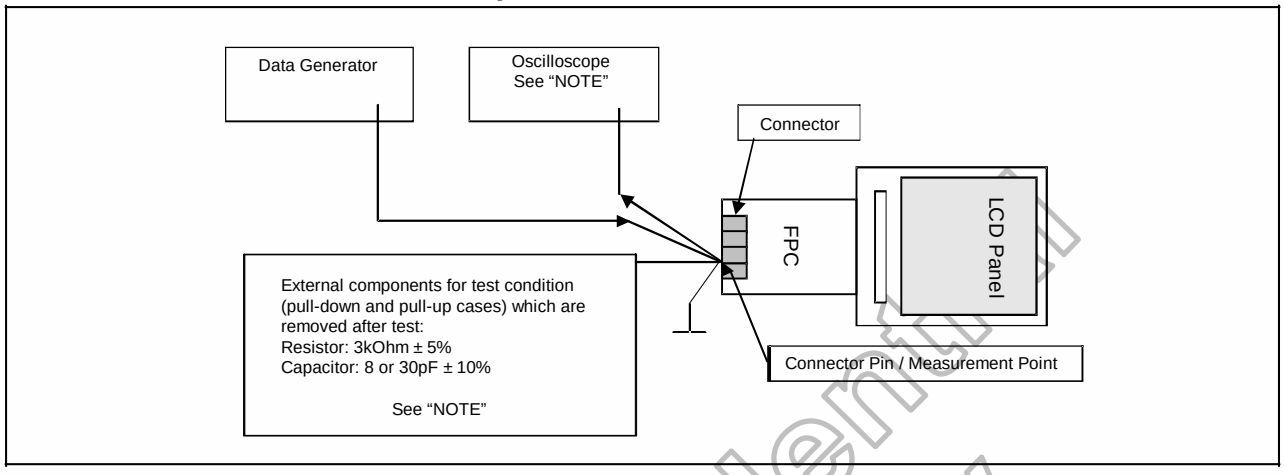
(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

tACC, tOH measurement condition

Measurement condition set-up



Note: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

Figure 8.5: tACC and tOH measurement condition set-up

Minimum value measurement

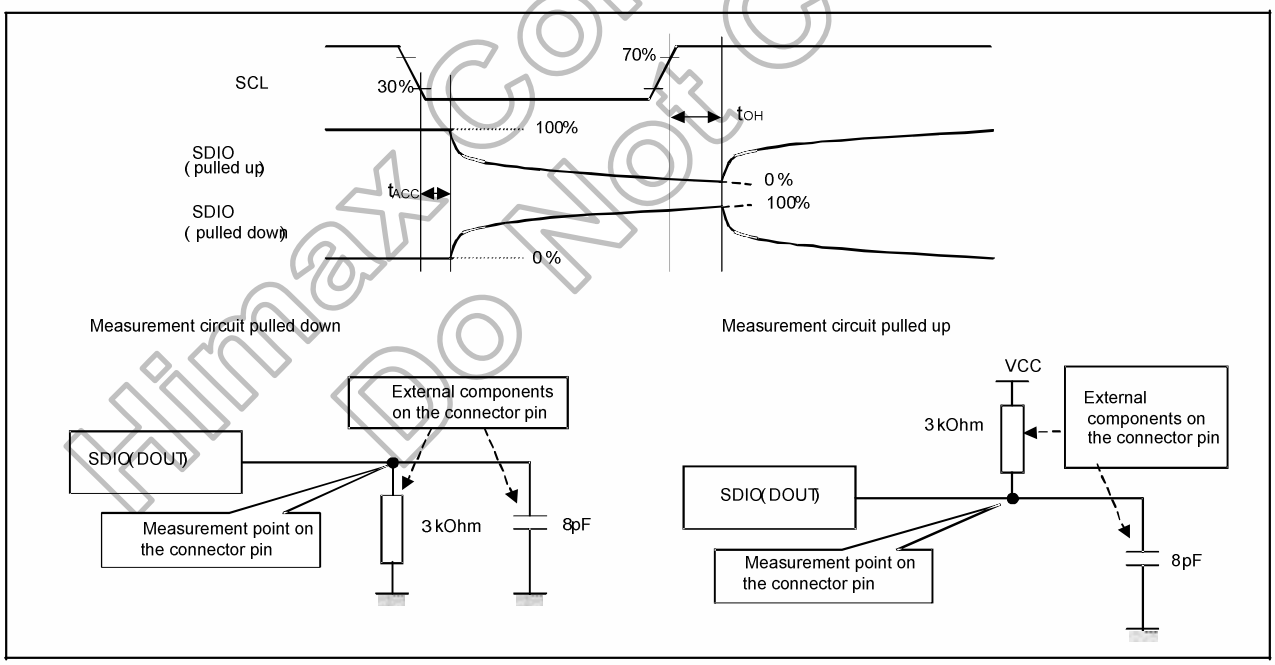


Figure 8.6: tACC and tOH minimum condition set-up

Maximum value measurement

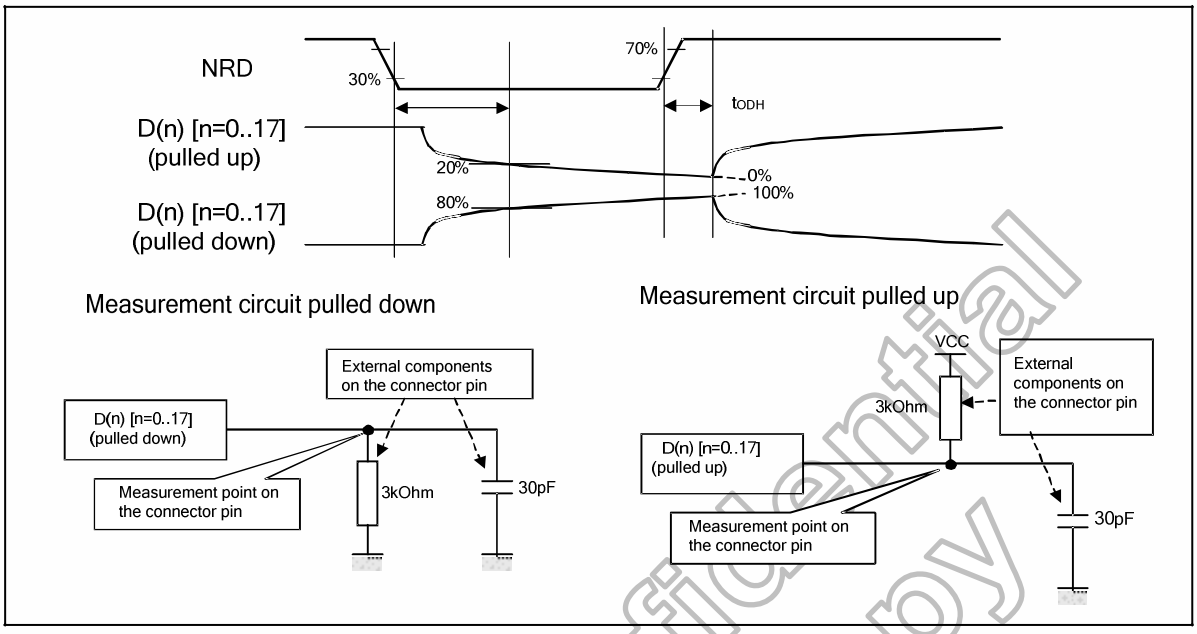


Figure 8.7: tACC and tOH maximum value measurement

8.4.4 DSI D-PHY electrical characteristics

8.4.4.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.6 shows the complete set of electrical functions required for a fully featured PHY transceiver.

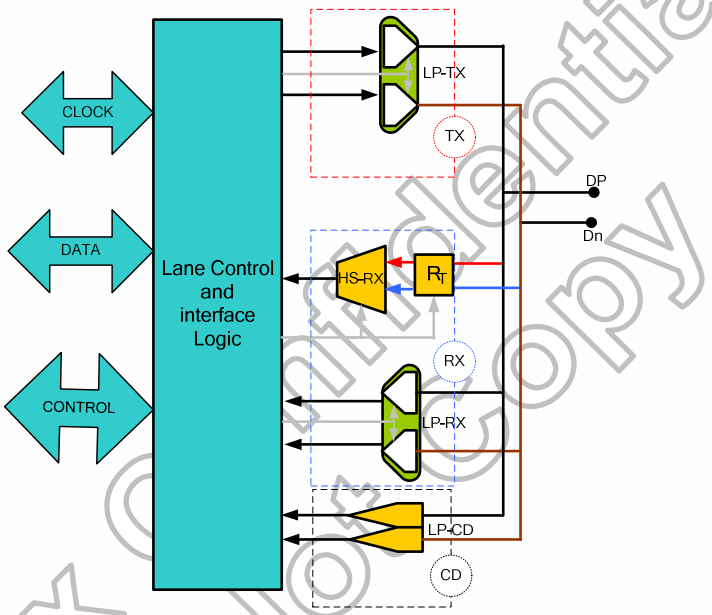


Figure 8.8: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.9 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

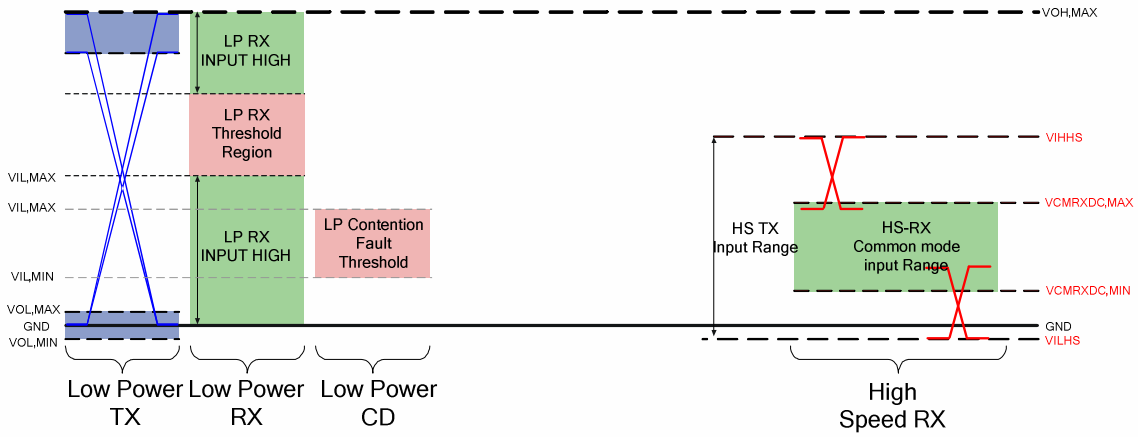


Figure 8.9: Shows both the HS and LP signal levels

8.4.4.2 Electrical characteristics of low-power transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OL}	Thevenin output low level	-50	-	50	mV	-
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	1

Note: Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 8.7: LP transmitter DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	1
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	1, 3, 5, 6
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	1, 3, 5, 6
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	1, 3, 5, 6
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	1, 3, 5, 6
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	1, 2, 3
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	1, 3, 7
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST – 700)	-	-	mV/ns	1, 8, 9
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

Table 8.8: LP transmitter AC specifications

8.4.4.3 Electrical characteristics of receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

8.4.4.4 High-speed receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	1
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	1
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	1, 2
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 8.9: HS receiver DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	1
C_{CM}	Common mode termination	-	-	60	pF	2

Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.10: HS receiver AC specifications

8.4.4.5 Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 8.10 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

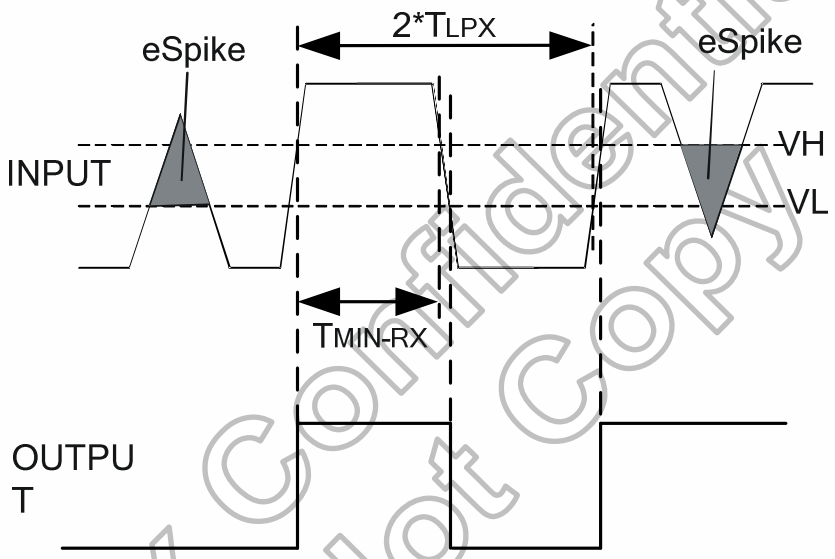


Figure 8.10: Input glitch rejections of low-power receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IL}	Logic 0 input threshold	-	-	550	mV	-
V_{IH}	Logic 1 input threshold	880	-	-	mV	-

Table 8.11: LP receiver DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state.
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 8.12: LP receiver AC specifications

8.4.4.6 Line contention detection

Contention can be inferred from any of the following conditions:

1. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than VIL.

2. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VILF.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 8.13: Contention detector DC specifications

8.4.4.7 High-speed data-clock timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.9.

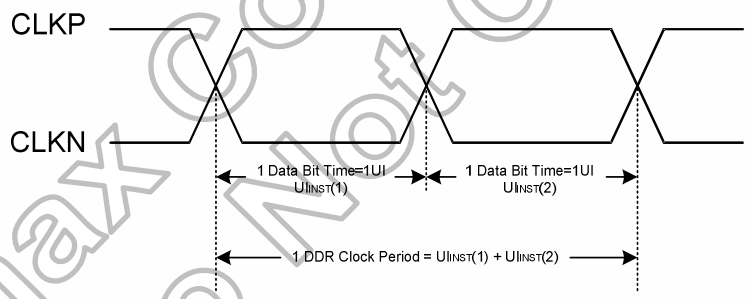


Figure 8.11: DDR clock definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in Table 8.14.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	1, 2

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Table 8.14: Reverse HS data transmission timing parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.12. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

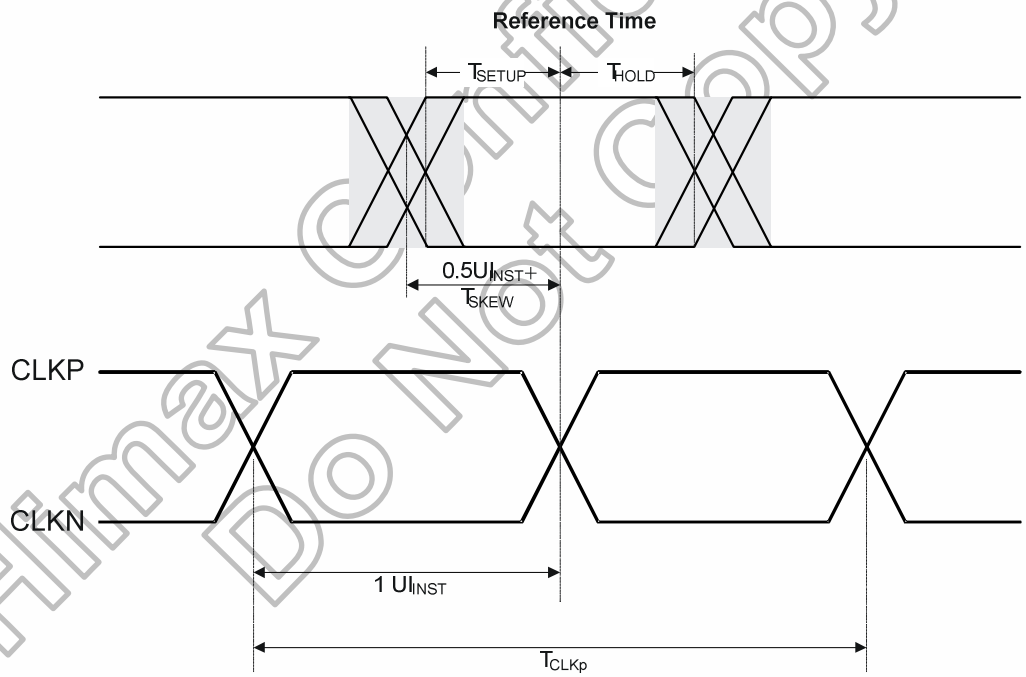


Figure 8.12: Data to clock timing definitions

8.4.4.8 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value UIINST,MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal ½UIINST displaced quadrature clock edge. The setup and hold times, TSETUP[RX] and THOLD[RX], respectively, describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising or falling clock edge and THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4*UIINST, i.e. ±0.2*UIINST for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Table 8.15: Data to clock timing specifications

9. Ordering Information

Part No.	Package
HX8357-D0x0 PDxxx	PD : mean COG xxx : mean chip thickness (µm), (default: 250 µm) D000: Without MIPI DSI interface. D010: With MIPI DSI interface.

10.Revision History

Version	Date	Description of Changes
00	2012/04/20	New setup.