APPLICATION NOTE

(DOC No. HX8238-A -AN)

HX8238-A

960 x 240 TFT LCD Single Chip Digital Driver

Preliminary version 01 December, 2006

Himax Technologies, Inc.
http://www.himax.com.tw

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1. General Description

The HX8238-A application note includes SPI commands, FPC pins, OLB resistance and application circuit. H-Sync (HSYNC), V-Sync (VSYNC), Data enable (DEN), and Clock (DOTCLK) from video decoder or other source.The interface follows digital 8-bit serial/24-bit parallel RGB, CCIR601 and CCIR656 input format.

HX8238-A is a single chip controller and driver LSI that integrated the power circuit. It can drive a maximum 960x240 dot graphics on a-TFT panel displays in 262K colors. HX8238-A has a low-voltage operation, 1.4 min. In addition, HX8238-A is equipped with a DC-DC converter control circuit that generates the supply voltage for source and gate drivers with minimum external components. A common voltage generation circuit is included to drive the TFT-display counter electrode. An integrated gamma control circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

2.SPI commands setting

2.1 Serial Interface

The SPI is available through the chip select line (CSB), serial transfer clock line (SCK), serial data input (SDI), and serial data output (SDO).

The Driver IC recognizes the start of data transfer at the falling edge of CSB input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CSB input. The Driver IC is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the Driver IC are compared and both 6-bit data correspond. The identification code must be 011100. Two different chip addresses must be assigned to the Driver IC because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When the RS = 1, instruction write. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

After receiving the start byte, the Driver IC starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted (9th SCK started). All Driver IC instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (IB15 to 0---9th ~24th SCK).

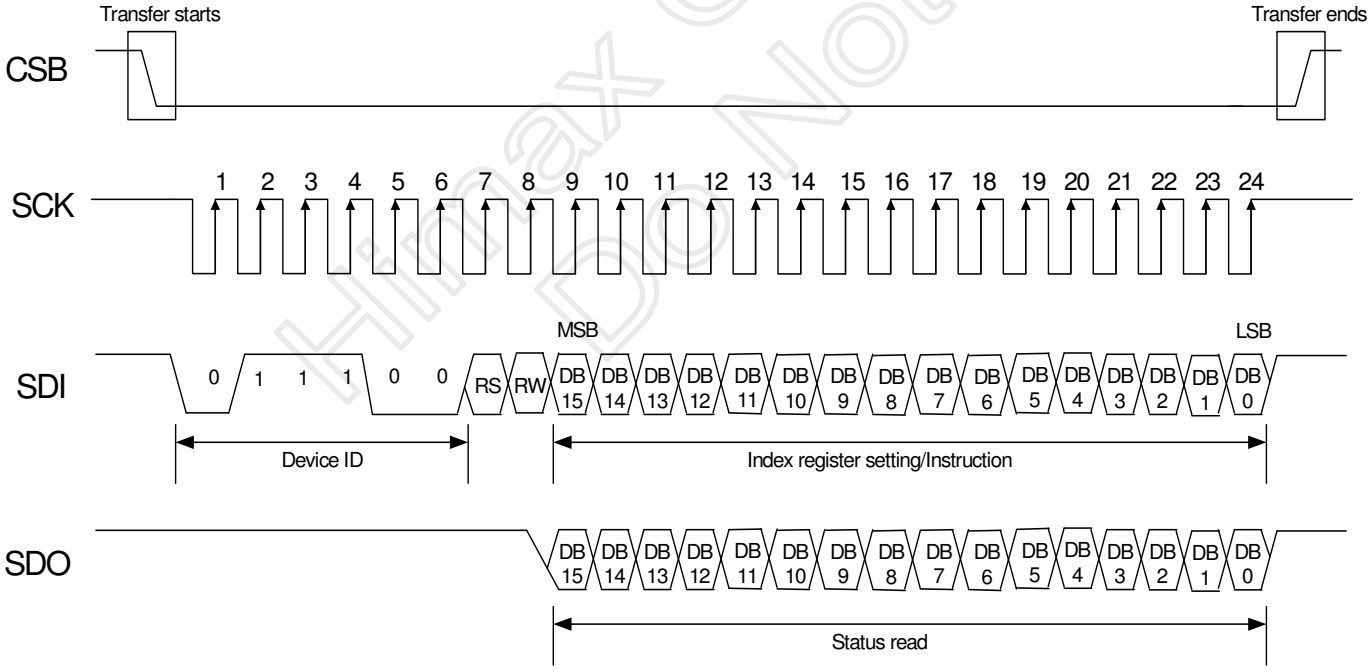


Figure 2.1 SPI Timing

2.2 Command Table

Reg#	Register	R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	PINV	BGR	SM	TB	CPE	0	0	0	0	0	0	0	0
R02h	LCD driver AC control	0	1	0	0	0	0	0	0	B/C	0	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
R04h	Data and color filter control	0	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0
R05h	Function control	0	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0
R06h	Reserved	Reserved																	
R07h	Reserved	Reserved																	
R0Ah	Contrast/ Brightness control	0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0
R0Dh	Power control (3)	0	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R16h	Horizontal Porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0
R17h	Vertical Porch	0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R27h	Reserved	Reserved																	
R28h	Reserved	Reserved																	
R29h	Reserved	Reserved																	
R2Bh	Reserved	Reserved																	
R30h	γ control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	γ control (9)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	γ control (10)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Table 2.1 Command table

2.3 Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	R L	REV	PINV	BGR	S M	T B	CPE	0	0	1	1	1	1	1	1

Figure 2.2 Driver output control

CPE: When CPE=0, internal charge pump circuit is shut down. When CPE=1, internal charge pump circuit is enabled.

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source output level	
		VCOM = "H"	VCOM = "L"
0	00000H : 3FFFFH	V0 : V63	V63 : V0
1	00000H : 3FFFFH	V63 : V0	V0 : V63

Table 2.2 Source output level

PINV: When PINV=0, POL output is same phase with internal VCOM signal. When PINV=1, POL output phase is reversed with VCOM signal.

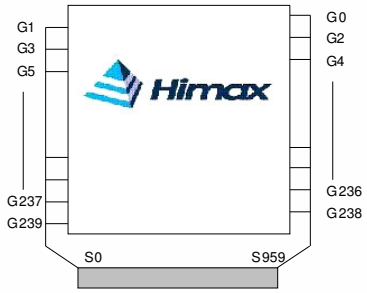
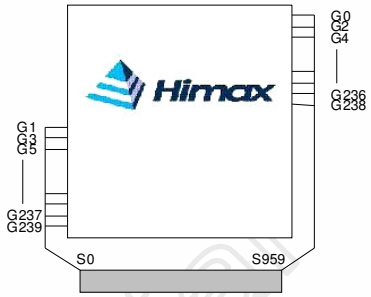
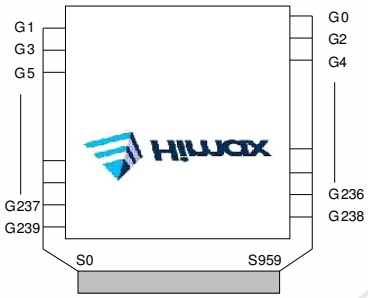
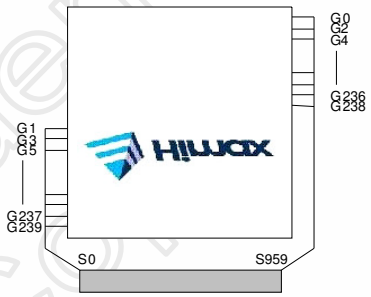
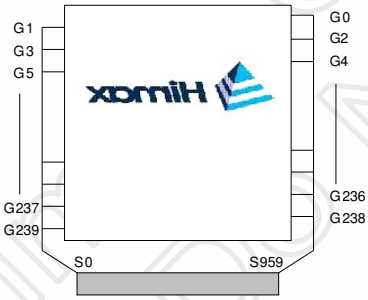
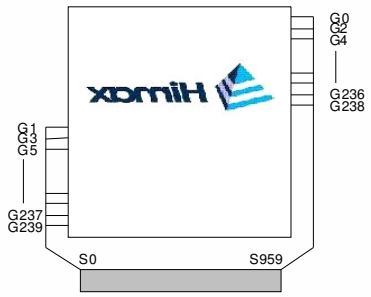
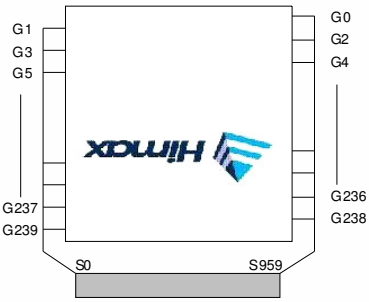
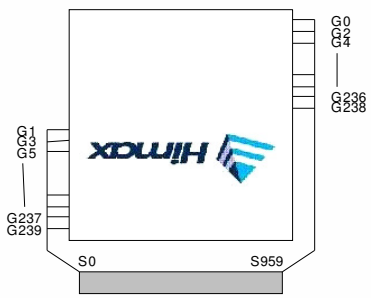
BGR: Selects the <R><G><B> arrangement. When BGR = "0" <R><G><B> color is assigned from S0.When BGR = "1" <B><G><R> color is assigned from S0.

SM: Change the division of gate driver. When SM = "0", odd/even division (interlace mode) is selected. When SM = "1", upper/lower division is selected. Select the division mode according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB = "1", G0 shifts to G239. When TB = "0", G239 shifts to G0.

RL: Selects the output shift direction of the source driver. When RL = "1", S0 shifts to S959 and <R><G><B> color is assigned from S0. When RL = "0", S959 shifts to S0 and <R><G><B> color is assigned from S959. Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits **REV**, **BGR**, **TB** and **RL** are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.

	SM = 0	SM = 1
TB = 1 **RL = 1**		
TB = 0 **RL = 1**		
TB = 1 **RL = 0**		
TB = 0 **RL = 0**		

2.4 LCD-Driving-Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B/C	0	NW7	MW6	NW5	NW4	NW3	NW2	NW1	NW0

Figure 2.3 LCD-driving-waveform control

B/C: When B/C = 0, frame inversion of the LCD driving signal is enabled. When B/C = 1, a N-line inversion waveform is generated and alternates in each N lines specified by bits NW7-0.

NW7-0: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). NW7-0 alternate for every set value + 1 line.

2.5 Power control 1 (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0

Figure 2.4 Power control 1

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM = VDDIO). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

* Fline = horizontal frequency (Fline Typ. 15KHz)

Table2.4 Step-up cycle

BT2-0 & BTF: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power supply voltage to be used.

BTF	BT2	BT1	BT0	VGH output	VGL output
0	0	0	0	V_{CIX2} X 3	- (V_{CIX2} X 3) + V_{CI}
0	0	0	1	V_{CIX2} X 3	- (V_{CIX2} X 2)
0	0	1	0	V_{CIX2} X 3	- (V_{CIX2} X 3)
0	0	1	1	V_{CIX2} X 2 + V_{CI}	- (V_{CIX2} X 2) - V_{CI}
0	1	0	0	V_{CIX2} X 2 + V_{CI}	- (V_{CIX2} X 2)
0	1	0	1	V_{CIX2} X 2 + V_{CI}	- (V_{CIX2} X 2) + V_{CI}
0	1	1	0	V_{CIX2} X 2	- (V_{CIX2} X 2)
1	1	1	1	V_{CIX2} X 2	- (V_{CIX2} X 2) + V_{CI}
1	X	X	X	V_{CIX2} X 3	- V_{CIX2}

Table 2.5 VGH and VGL booster ratio

DC3-0: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = VSS). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

* Fline = horizontal frequency (Fline Typ. 15KHz)

Table 2.6 Step-up cycle

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode, set AP2-0 = “000” to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

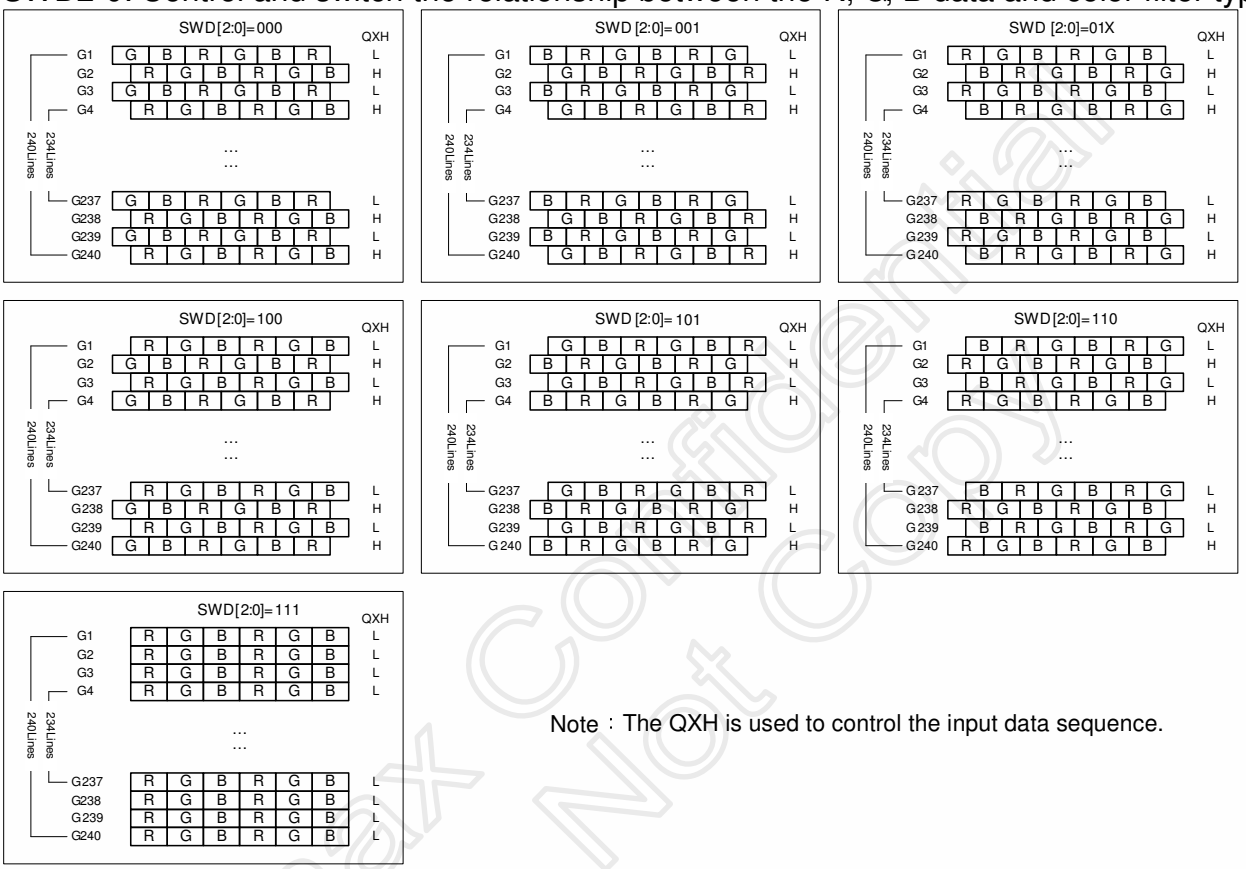
Table 2.7 Op-amp power

2.6 Input Data and Color Filter Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0

Figure2.5 Input data and color filter control

SWD2-0: Control and switch the relationship between the R, G, B data and color filter type.



Note：The QXH is used to control the input data sequence.

Table 2.8 Color filter type.

SEL2-0: Define the input interface mode.

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Table2.9 Interface type.

OEA1-0: Odd/Even filed advanced function.

OEA1	OEA0	
0	0	Display Start @ VBP delay for Odd field and @ ***VBP-1*** for Even field.
0	1	Display Start @ VBP delay for Odd field and @ ***VBP*** for Even field.
1	0	Display Start @ VBP delay for Odd field and @ ***VBP+1*** for Even field.
1	1	No use

Table 2.10 Odd/even filed advanced function.

BLT[1:0]: Set the initial power on black image insertion time.
00: 10 fields
01: 20 fields
10: 40 fields
11: 80 fields

PALM: Set the input data line number in PAL mode
0: 280 lines
1: 288 lines

2.7 Function Control (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0

Figure 2.6 Function control

FB2-0: Set PWM feedback level adjustment.
000: 0.4V
001: 0.45V
010: 0.5V
011: 0.55V
100: 0.6V
101: 0.65V
110: 0.7V
111: 0.75V

PWM: When PWM=0, PWM function is disabled. When PWM=1, PWM function is enabled.

DIT: When DIT=0, dithering function is turned off. When DIT=1, dithering function is enabled.

DEO: When DEO=0, VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP[6:0] and the horizontal first valid data is defined by DE signal. When DEO=1, only DEN signal is needed in DE mode.

HSP: When HSP=0, HSYNC is negative polarity. When HSP=1, HSYNC is positive polarity.

VSP: When VSP=0, VSYNC is negative polarity. When VSP=1, VSYNC is positive polarity.

CKP: When CKP=0, data is latched in CLK falling edge. When CKP=1, data is latched by CLK rising edge.

DEP: When DEP=0, DEN is negative polarity active. When DEP=1, DEN is positive polarity active.

LPF: When LPF=0, the low pass filter function in YUV mode is disabled. When LPF=1, the low pass filter function is YUV mode is enabled.

GDIS: When GDIS=0, VGL has no discharge path to VSS in standby mode. When GDIS=1, VGL will discharge to VSS in standby mode.

XDK: When XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2=3 x VCI) When XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2=2 x VCI)

GHN: When GHN=0, all gate outputs are forced to VGH. When GHN=1, gate driver is normal operation.

2.8 Contrast/Brightness Control (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0

Figure 2.7 Contrast/Brightness control

CON4-0: Display Contrast level adjustment. (0.125/step) Adjust range from 00h(level = 0) to 1Fh(level = 3.875). Default value is 08h(level = 1).

BR6-0: Display Brightness level adjustment. (2/step) Adjust range from 00h(level = -128) to 7Fh(level = +126). Default value is 40h(level = 0).

2.9 Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0

Figure2.8 Frame cycle control

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	1.5 us
0	1	3 us
1	0	4.5 us
1	1	6 us

Table 2.11 Amount of non-overlap

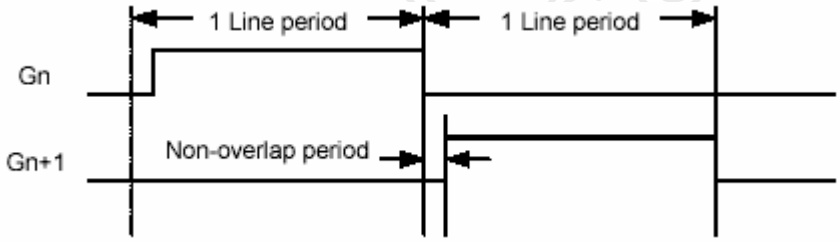


Figure 2.9 **NO timing diagram**

SDT1-0: Set delay amount from the gate output signal falling edge to the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1 us
0	1	3 us
1	0	5 us
1	1	7 us

Table 2.12 Delay amount of the source output

EQ2-0: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	3 us
0	1	0	4 us
0	1	1	5 us
1	0	0	6 us
1	0	1	7 us
1	1	0	8 us
1	1	1	9 us

Table2.13 EQ period

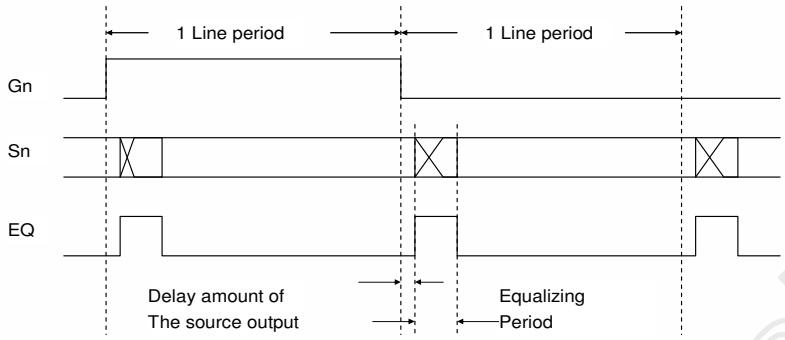


Figure 2.10 EQ timing diagram

2.10 Power Control 2 (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 2.11 Power control 2

VRC[2:0]: set the VCIX2 charge pump voltage clamp.

VRC[2:0]=000, 5.1V
VRC[2:0]=001, 5.3V
VRC[2:0]=010, 5.5V
VRC[2:0]=011, 5.7V
VRC[2:0]=100, 5.9V
VRC[2:0]=101, reserved
VRC[2:0]=110, reserved
VRC[2:0]=111, reserved

VDS[1:0]: set the VDD regulator voltage if pin "REGVDD" is set to VDDIO.

VDS[1:0]=00, 1.8V
VDS[1:0]=01, 2V
VDS[1:0]=10, 2.2V
VDS[1:0]=11, 2.5V

VRH5-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 2.464 to 4.456 times the Vref voltage set by VRH5-0.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63Voltage	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63Voltage
0	0	0	0	0	0	Vref x 2.464	1	0	0	0	0	0	Vref x 3.464
0	0	0	0	0	1	Vref x 2.496	1	0	0	0	0	1	Vref x 3.496
0	0	0	0	1	0	Vref x 2.528	1	0	0	0	1	0	Vref x 3.528
0	0	0	0	1	1	Vref x 2.560	1	0	0	0	1	1	Vref x 3.560
0	0	0	1	0	0	Vref x 2.592	1	0	0	1	0	0	Vref x 3.592
0	0	0	1	0	1	Vref x 2.624	1	0	0	1	0	1	Vref x 3.629
0	0	0	1	1	0	Vref x 2.656	1	0	0	1	1	0	Vref x 3.664
0	0	0	1	1	1	Vref x 2.688	1	0	0	1	1	1	Vref x 3.701
0	0	1	0	0	0	Vref x 2.720	1	0	1	0	0	0	Vref x 3.736
0	0	1	0	0	1	Vref x 2.752	1	0	1	0	0	1	Vref x 3.762
0	0	1	0	1	0	Vref x 2.784	1	0	1	0	1	0	Vref x 3.787
0	0	1	0	1	1	Vref x 2.816	1	0	1	0	1	1	Vref x 3.813
0	0	1	1	0	0	Vref x 2.848	1	0	1	1	0	0	Vref x 3.840
0	0	1	1	0	1	Vref x 2.875	1	0	1	1	0	1	Vref x 3.880
0	0	1	1	1	0	Vref x 2.904	1	0	1	1	1	0	Vref x 3.920
0	0	1	1	1	1	Vref x 2.931	1	0	1	1	1	1	Vref x 3.960
0	1	0	0	0	0	Vref x 2.960	1	1	0	0	0	0	Vref x 4.000
0	1	0	0	0	1	Vref x 2.992	1	1	0	0	0	1	Vref x 4.027

0	1	0	0	1	0	Vref x 3.024	1	1	0	0	1	0	Vref x 4.056
0	1	0	0	1	1	Vref x 3.056	1	1	0	0	1	1	Vref x 4.083
0	1	0	1	0	0	Vref x 3.088	1	1	0	1	0	0	Vref x 4.112
0	1	0	1	0	1	Vref x 3.123	1	1	0	1	0	1	Vref x 4.142
0	1	0	1	1	0	Vref x 3.160	1	1	0	1	1	0	Vref x 4.171
0	1	0	1	1	1	Vref x 3.195	1	1	0	1	1	1	Vref x 4.202
0	1	1	0	0	0	Vref x 3.232	1	1	1	0	0	0	Vref x 4.232
0	1	1	0	0	1	Vref x 3.259	1	1	1	0	0	1	Vref x 4.264
0	1	1	0	1	0	Vref x 3.288	1	1	1	0	1	0	Vref x 4.296
0	1	1	0	1	1	Vref x 3.315	1	1	1	0	1	1	Vref x 4.328
0	1	1	1	0	0	Vref x 3.344	1	1	1	1	0	0	Vref x 4.360
0	1	1	1	0	1	Vref x 3.374	1	1	1	1	0	1	Vref x 4.392
0	1	1	1	1	0	Vref x 3.403	1	1	1	1	1	0	Vref x 4.424
0	1	1	1	1	1	Vref x 3.434	1	1	1	1	1	1	Vref x 4.456

*Vref is the internal reference voltage equals to 1.25V.

Table 2.14 VLCD63 voltage

2.11 Power Control 3 (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0

Figure 2.12 Power control 3

VCOMG: When VCOMG = “1”, it is possible to set output voltage of VCOML to any level, and the instruction (VDV6-0) becomes available. When VCOMG = “0”, VCOML output is fixed to VSS level, VCIM output for VCOML power supply stops, and the instruction (VDV6-0) becomes unavailable. Set VCOMG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV6-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.6 to 1.2525 times the VLCD63 voltage. When VCOMG = “0”, the settings become invalid. External voltage at VCOMR is referenced when VDV = “01111xx”.

VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	0	0	VLCD63 x 0.6000
0	0	0	0	0	0	1	VLCD63 x 0.6075
0	0	0	0	0	1	0	VLCD63 x 0.6150
0	0	0	0	0	1	1	VLCD63 x 0.6225
0	0	0	0	1	0	0	VLCD63 x 0.6300
:	:	:	:	:	:	:	: Step = 0.0075 :
0	1	1	1	0	1	0	VLCD63 x 1.0350
0	1	1	1	0	1	1	VLCD63 x 1.0425
0	1	1	1	1	*	*	Reference from external voltage (VCOMR)
1	0	0	0	0	0	0	VLCD63 x 1.0500
1	0	0	0	0	0	1	VLCD63 x 1.0575
:	:	:	:	:	:	:	: Step = 0.0075 :
1	0	1	1	0	1	0	VLCD63 x 1.2450
1	0	1	1	0	1	1	VLCD63 x 1.2525
1	0	1	1	1	*	*	Reserved
1	1	*	*	*	*	*	Reserved

Table 2.15 VCOM amplitude

2.12 Gate Scan Position (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

Figure2.13 Gate scan position

SCN8-0: Set the scanning starting position of the gate driver.

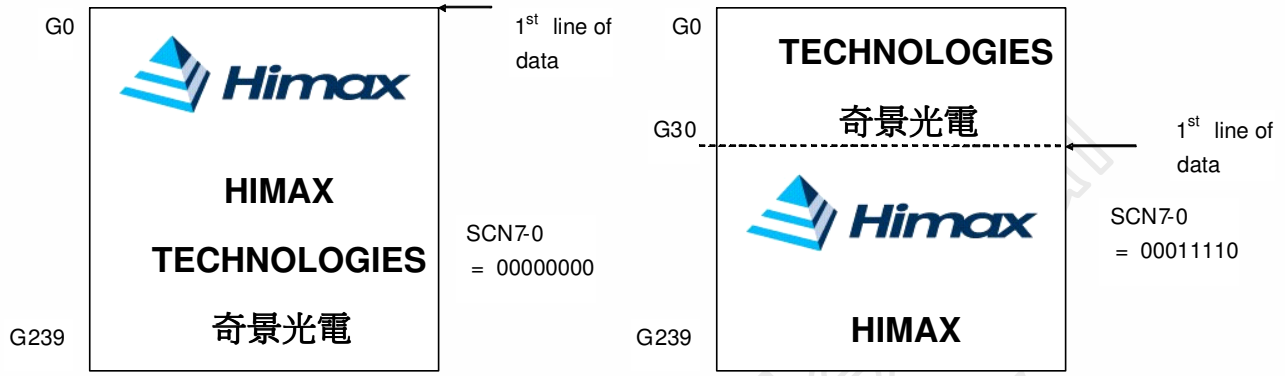


Figure 2.14 Gate scan display position

2.13 Horizontal Porch (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0

Figure 9. 1 Horizontal Porch

XLIM8-0: Set the number of valid pixel per line.

XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					: Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

Table 2.16 No. of pixel per line

2.14 Vertical Porch (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 2.45 Vertical porch

HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XLIM8-0 and before the first valid data will be treated as dummy data. The setting is only effective in SYNC mode timing.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	Can't set
0	0	0	0	0	1	1	Can't set
0	0	0	0	1	0	0	Can't set
0	0	0	0	1	0	1	Can't set
0	0	0	0	1	1	0	Can't set
0	0	0	0	1	1	1	Can't set
0	0	0	1	0	0	0	Can't set
0	0	0	1	0	0	1	9

							: Step = 1 :
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 2.17 No. of clock cycle of clock

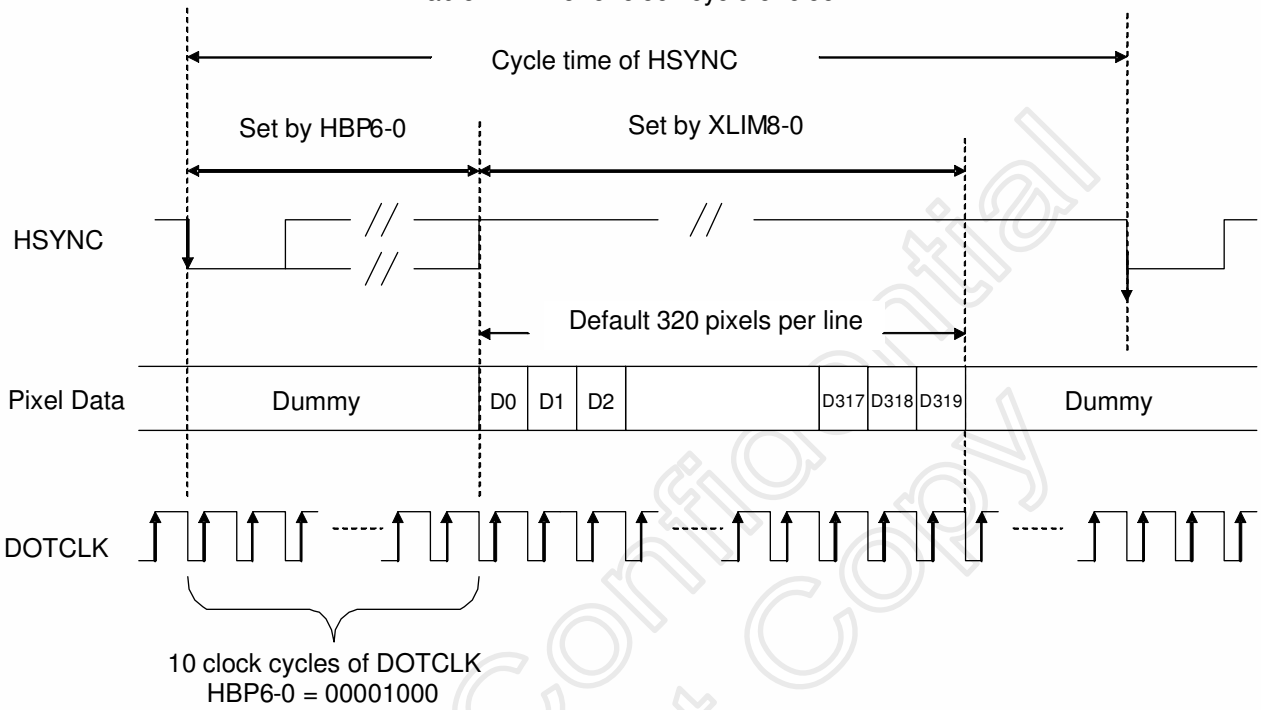


Figure 2.16 **No. of clock cycle of clock**

STH1-0: Adjust the first valid data by dot clock. This setting is not valid in parallel RGB input interface.
STH = 00: +0 dot clock
STH = 01: +1 dot clock
STH = 10: +2 dot clock
STH = 11: +3 dot clock

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line. The setting is only effective in SYNC mode timing.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
							: Step = 1 :
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 2.18 No. of clock cycle of HSYNC

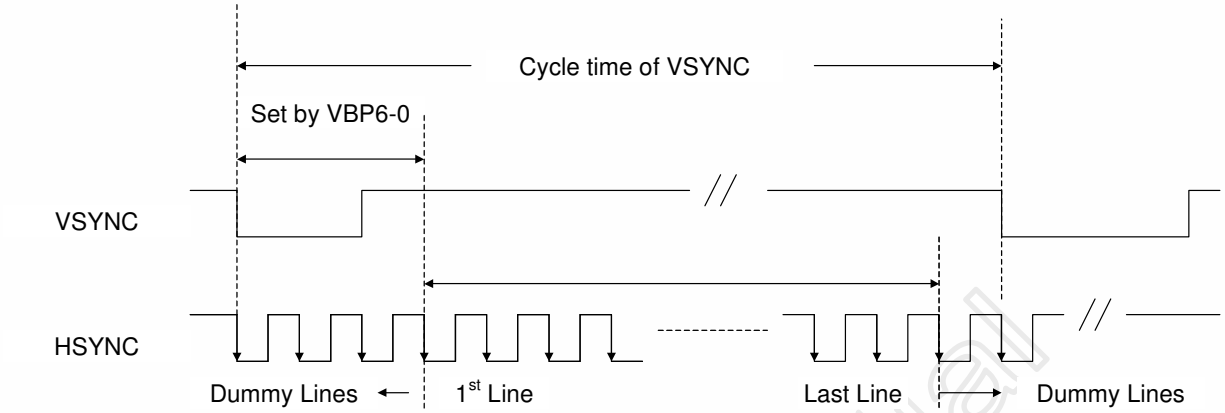


Figure 2.17 No. of clock cycle of HSYNC

2.15 Power Control 4 (R1Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure2.18 Power control 4

nOTP: nOTP equals to “0” after power on reset and VCOMH voltage equals to programmed OTP value. When nOTP set to “1”, setting of VCM6-0 becomes valid and voltage of VCOMH can be adjusted.

VCM6-0: Set the VCOMH voltage if nOTP = “1”. These bits amplify the VCOMH voltage 0.36 to 0.995 times the VLCD63 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VLCD63 x 0.360
0	0	0	0	0	0	1	VLCD63 x 0.365
0	0	0	0	0	1	0	VLCD63 x 0.370
0	0	0	0	0	1	1	VLCD63 x 0.375
0	0	0	0	1	0	0	VLCD63 x 0.380
:	:	:	:	:	:	:	: Step = 0.005 :
1	1	1	1	1	0	0	VLCD63 x 0.980
1	1	1	1	1	0	1	VLCD63 x 0.985
1	1	1	1	1	1	0	VLCD63 x 0.990
1	1	1	1	1	1	1	VLCD63 x 0.995

Note: $2V < V_{COMH} < V_{LCD63}$

Table 2.19 VCOMH

2.16 Gamma Control 1 (R30h to R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1	PKP1	PKP1	0	0	0	0	0	PKP0	PKP0	PKP0
W	1	0	0	0	0	0	PKP3	PKP3	PKP3	0	0	0	0	0	PKP2	PKP2	PKP2
W	1	0	0	0	0	0	PKP5	PKP5	PKP5	0	0	0	0	0	PKP4	PKP4	PKP4
W	1	0	0	0	0	0	PRP1	PRP1	PRP1	0	0	0	0	0	PRP0	PRP0	PRP0
W	1	0	0	0	0	0	PKN1	PKN1	PKN1	0	0	0	0	0	PKN0	PKN0	PKN0
W	1	0	0	0	0	0	PKN3	PKN3	PKN3	0	0	0	0	0	PKN2	PKN2	PKN2
W	1	0	0	0	0	0	PKN5	PKN5	PKN5	0	0	0	0	0	PKN4	PKN4	PKN4
W	1	0	0	0	0	0	PRN1	PRN1	PRN1	0	0	0	0	0	PRN0	PRN0	PRN0

Figure 2.19 Gamma control 1

PKP52–00: Gamma micro adjustment register for the positive polarity output.
PRP12-00: Gradient adjustment register for the positive polarity output.
PKN52-00: Gamma micro adjustment register for the negative polarity output.
PRN12-00: Gradient adjustment register for the negative polarity output.

2.17 Gamma Control 2 (R3Ah to R3Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

Figure 2.20 Gamma control 2

VRP14-00: Adjustment register for amplification adjustment of the positive polarity output.
VRN14-00: Adjustment register for the amplification adjustment of the negative polarity output.
(Refer to Gamma Adjustment Function for details)

3.Application Circuit

3.1 PWM Boost Converter

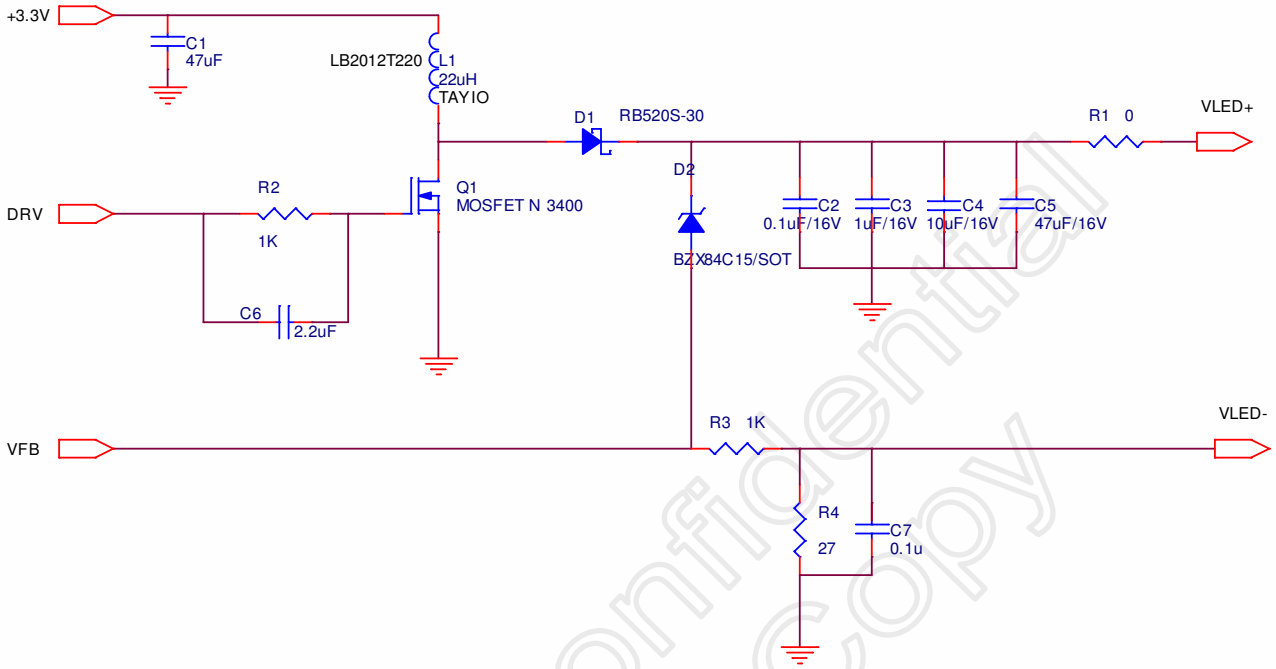


Figure 3.1 PWM Boost Converter

3.2 Booster capacitors

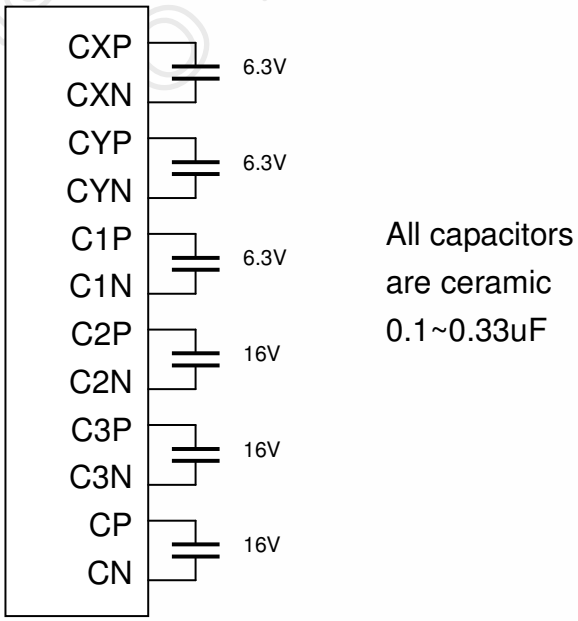


Figure 3.2 Booster capacitors

3.3 Power supply pins connections

System Vdd > 2.5V or
1.8V > System Vdd

REGVDD = VDDIO

2.5V ≧ System Vdd ≧ 1.8V

REGVDD = VSS

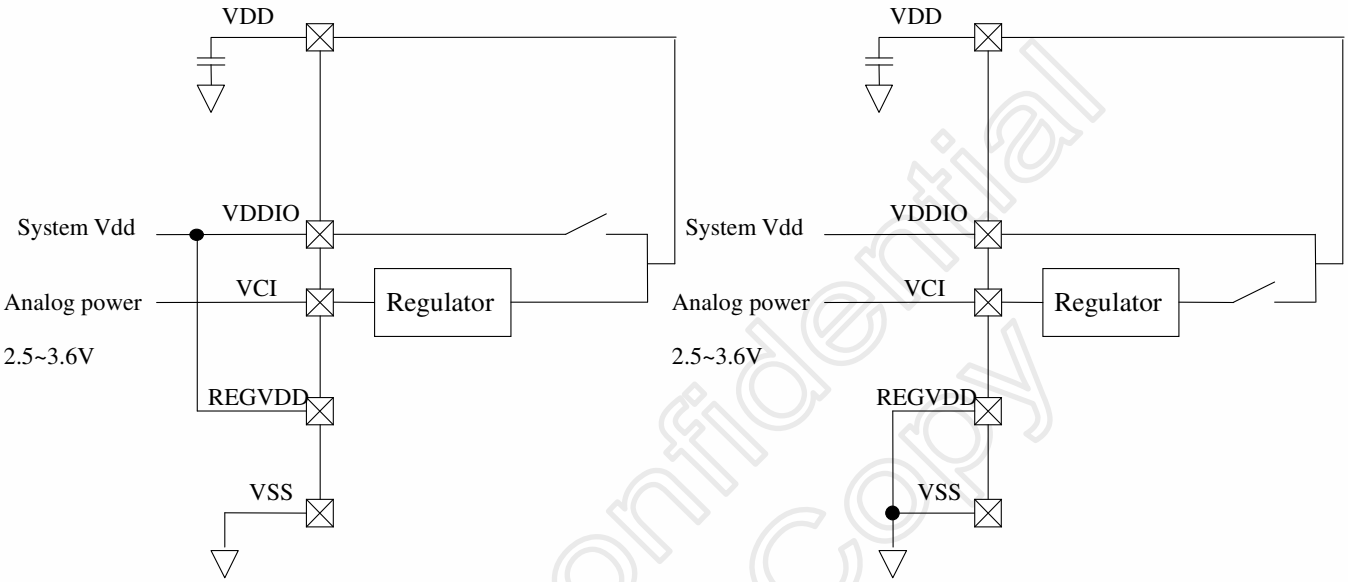


Figure 3.3 Power supply pins connections

3.4 Filtering and charge sharing capacitors

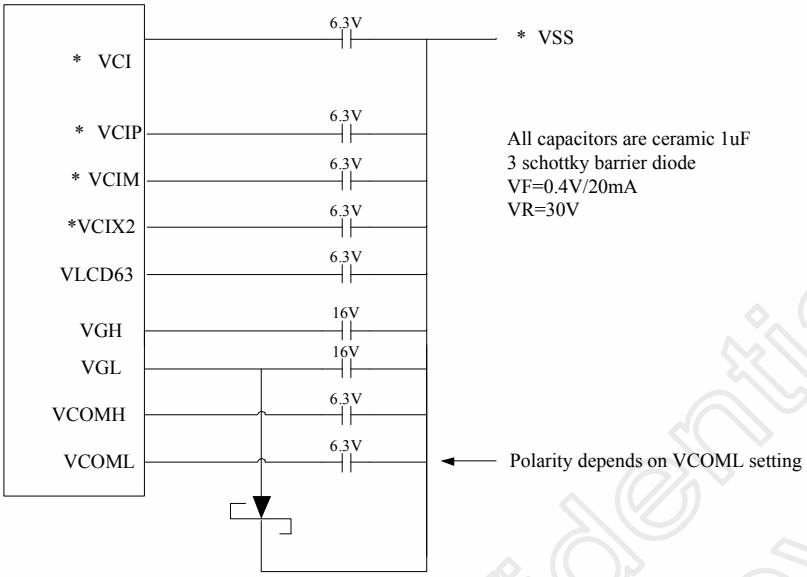


Figure 3.4 Filtering and charge sharing capacitors

1.Capacitors on VCI should be 4.7uF.
2.Capactiors on VCIP should be 1uF
3.Capacitor on VCIX2 should be 3.3uF
4.Capacitors on VGH, VGL, VCIM should be 2.2uF
5.Other capacitors should be 1uF
* VCIX2 should be separate with VCIX2J at ITO layout to provide noise free path
* VCI should be separate with VCIP at ITO layout to provide noise free path
* VSS should be separate with VCHS, AVSS and VSSRC at ITO layout to provide noise free path

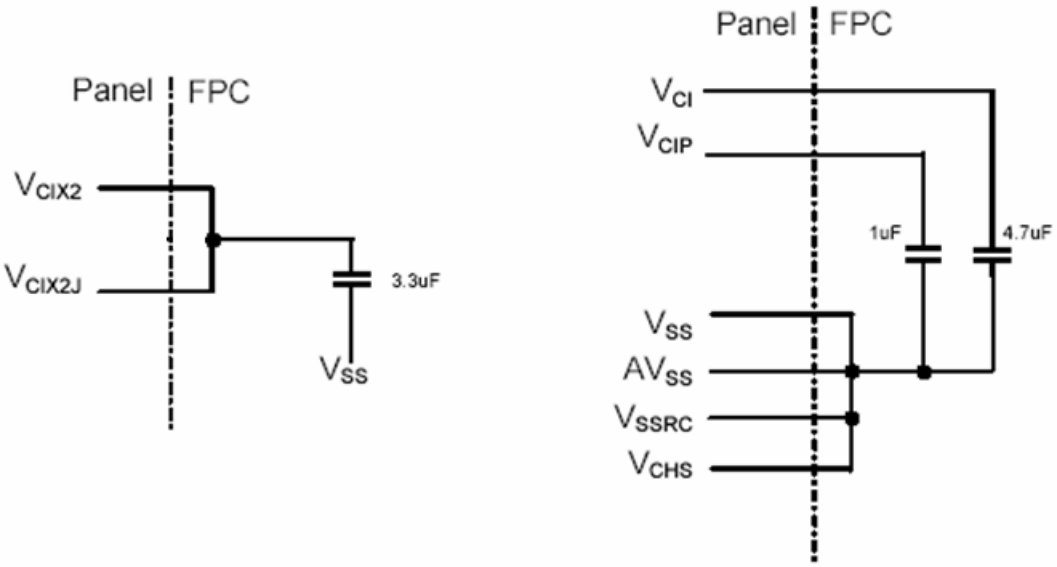


Figure 3.5 Panel and FPC connection

3.5 Panel connection example

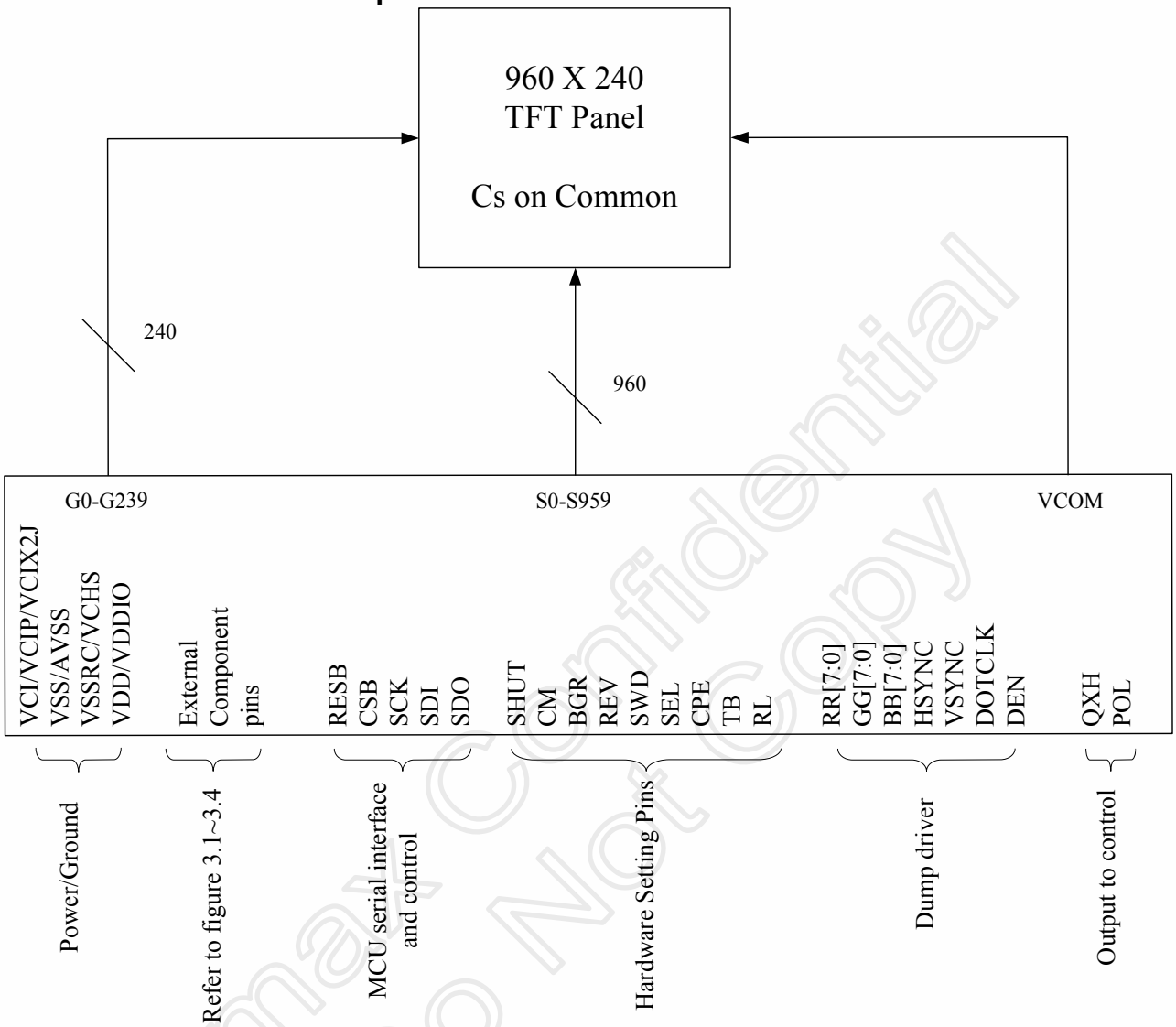


Figure 3.6 Panel connection example.

3.6 FPC and Glass layout with internal charge pumb

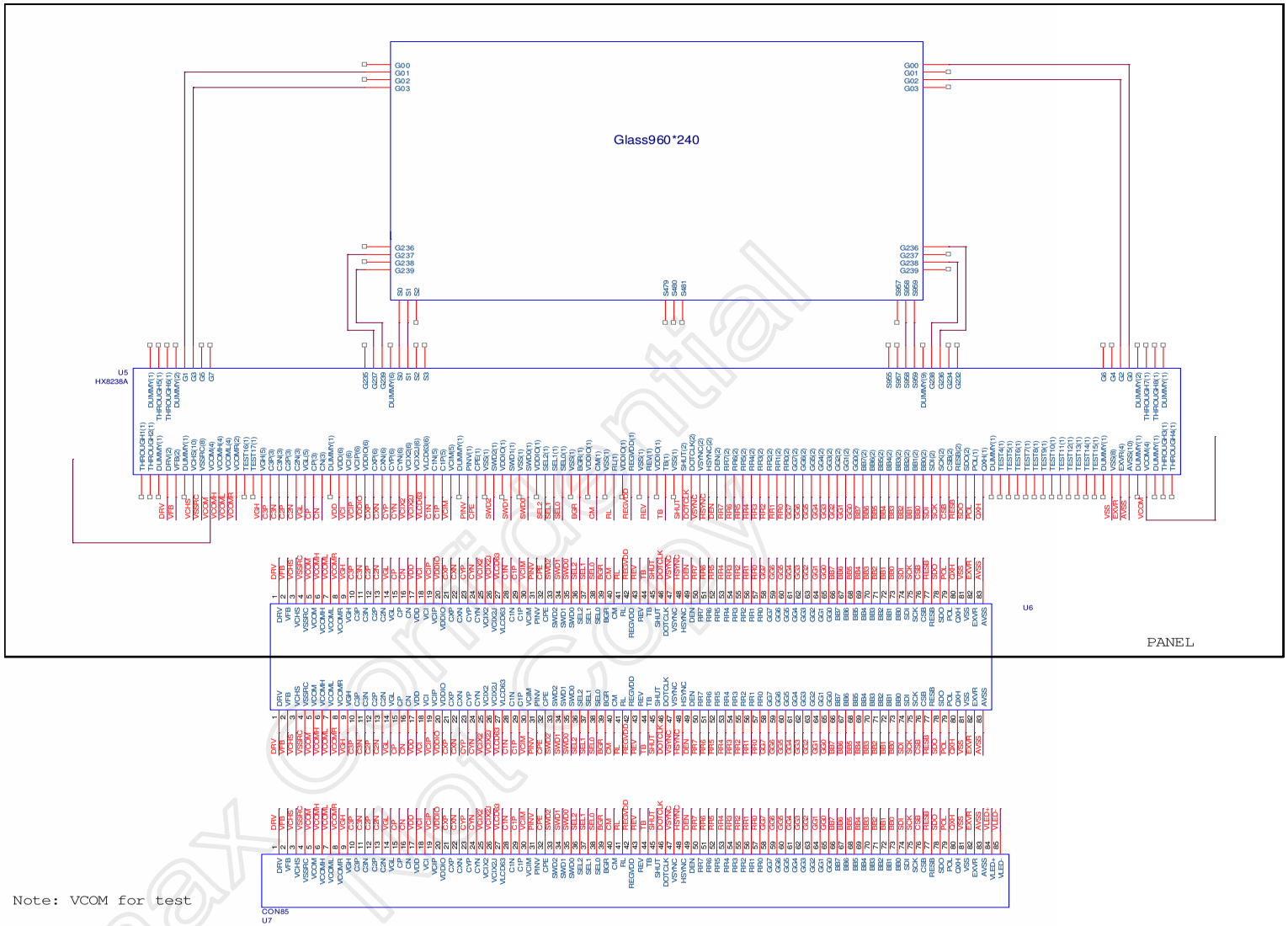


Figure 3.7 FPC and Glass layout with internal charge pumb

3.7 FPC, Power connection and LED Backlight Driving Circuit with internal charge pumb

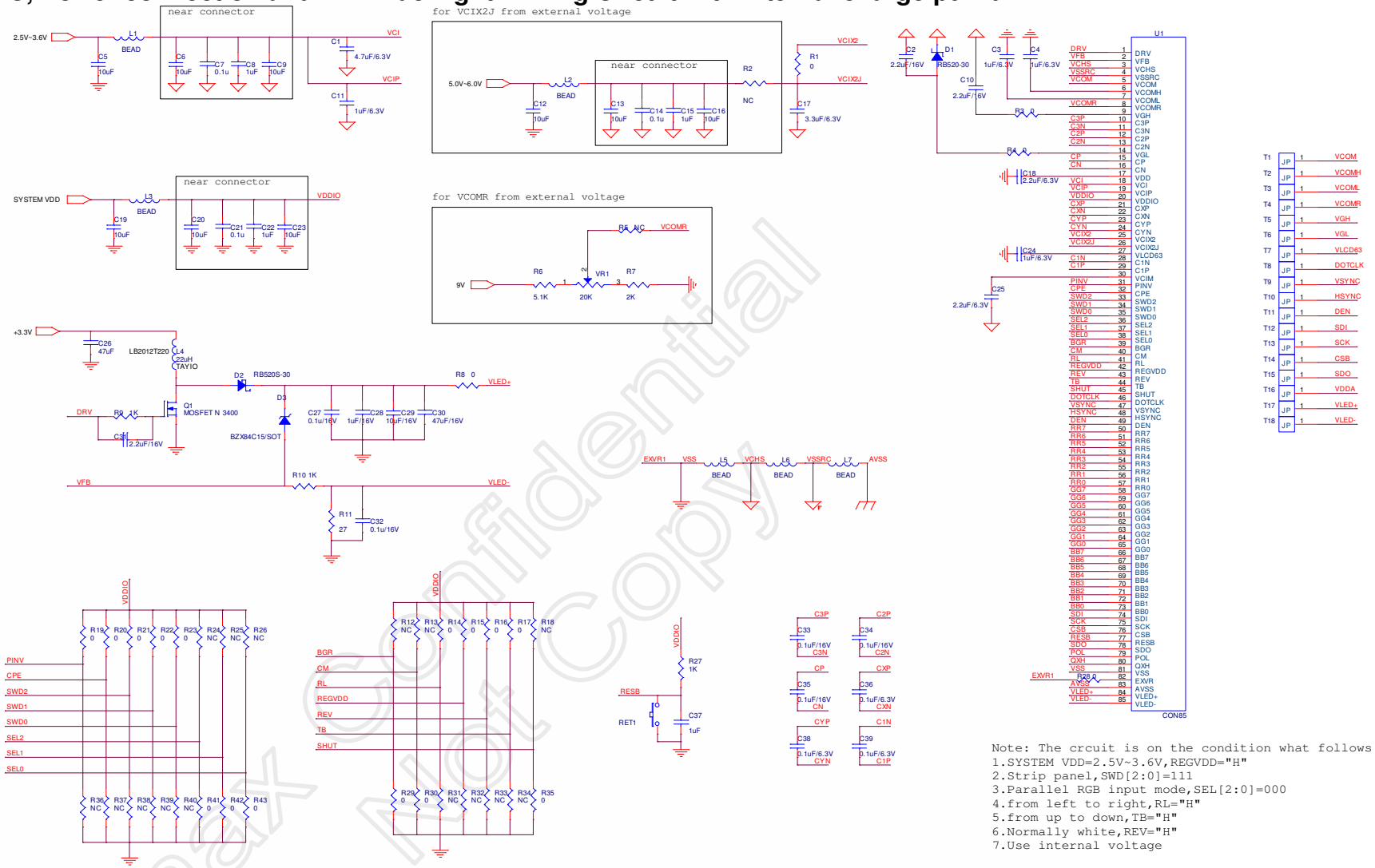
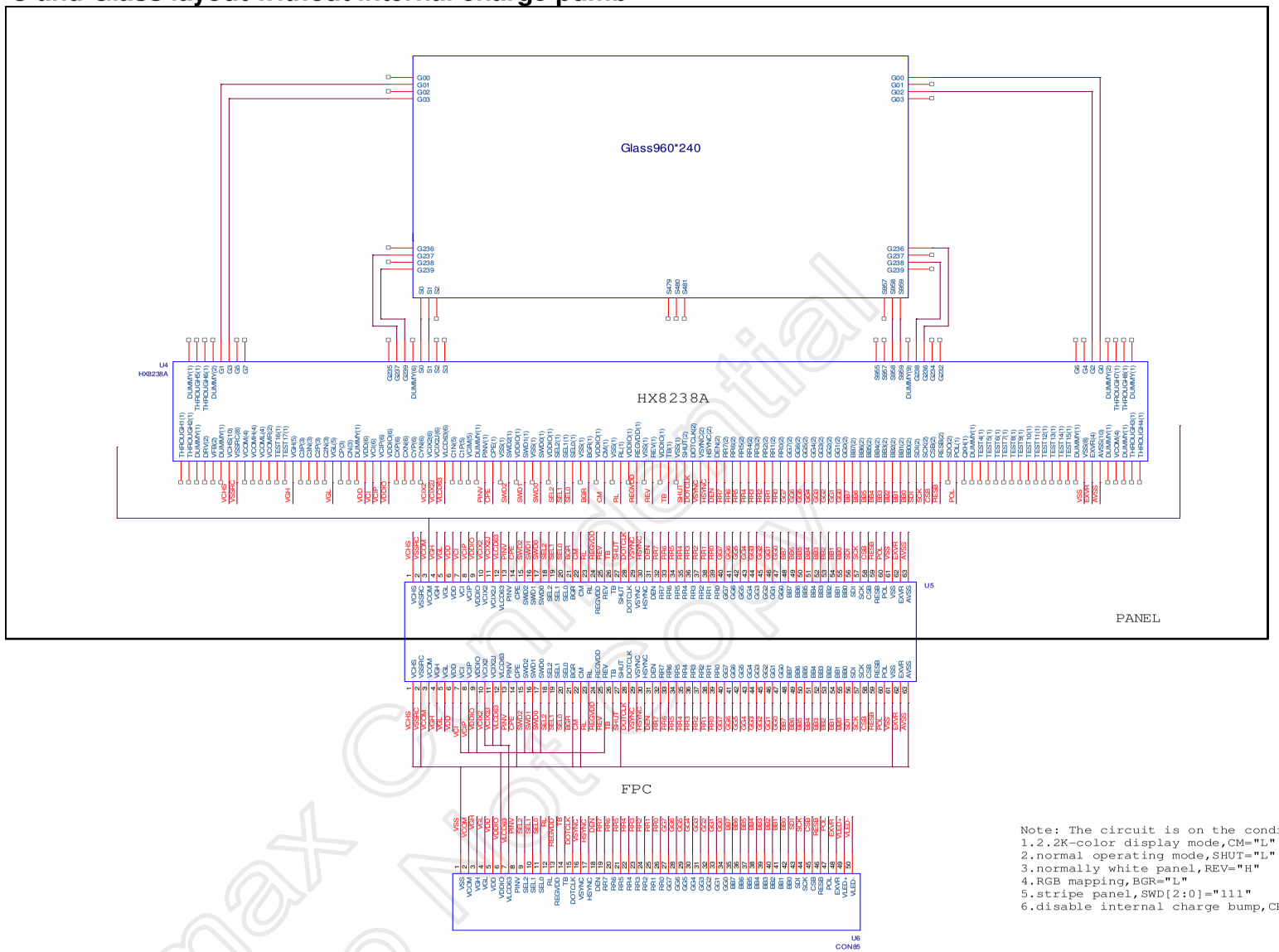


Figure 3.8 FPC, Power connection and LED Backlight Driving Circuit with internal charge pumb

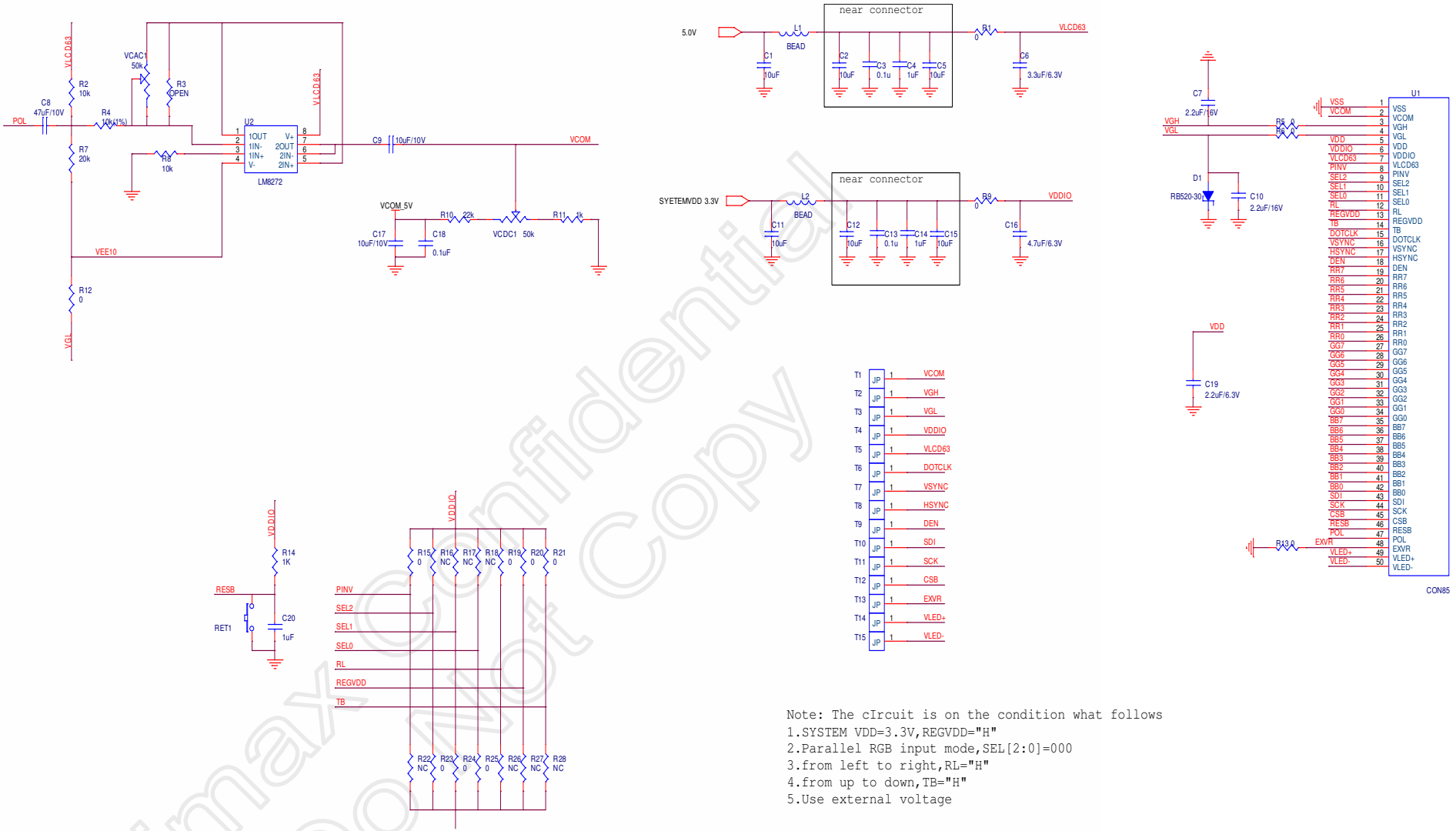
3.8 FPC and Glass layout without internal charge pumb



Note: The circuit is on the condition what follows
1.2.2K-color display mode,CM="L"
2.normal operating mode,SHUT="L"
3.normally white panel,REV="H"
4.RGB mapping,BGR="L"
5.stripe panel,SWD[2:0]="111"
6.disable internal charge bump,CPE="L"

Figure 3.9 FPC and Glass layout without internal charge pumb

3.9 FPC, Power connection without internal charge pumb



3.10 FPC, Power connection without internal charge pumb

4. OLB resistance value

PAD NO.	PAD NAME	max. wiring resistance(Ohm)
1	THROUGH4	
2	THROUGH3	
3	DUMMY	
4	VCOM	7.5
5	VCOM	
6	VCOM	
7	VCOM	
8	DUMMY	
9	AVSS	5
10	AVSS	
11	AVSS	
12	AVSS	
13	AVSS	
14	AVSS	
15	AVSS	
16	AVSS	
17	AVSS	
18	AVSS	
19	EXVR	7.5
20	EXVR	
21	EXVR	
22	EXVR	
23	VSS	5
24	VSS	
25	VSS	
26	VSS	
27	VSS	
28	VSS	
29	VSS	
30	VSS	
31	DUMMY	
32	TEST15	
33	TEST14	
34	TEST13	
35	TEST12	
36	TEST11	
37	TEST10	
38	TEST9	
39	TEST8	
40	TEST7	
41	TEST6	
42	TEST5	
43	TEST4	
44	DUMMY	
45	QXH	100
46	POL	100

PAD NO.	PAD NAME	max. wiring resistance(Ohm)
47	SDO	100
48	SDO	100
49	RESB	100
50	RESB	
51	CSB	100
52	CSB	
53	SCK	100
54	SCK	
55	SDI	100
56	SDI	
57	BB0	100
58	BB0	
59	BB1	100
60	BB1	
61	BB2	100
62	BB2	
63	BB3	100
64	BB3	
65	BB4	100
66	BB4	
67	BB5	100
68	BB5	
69	BB6	100
70	BB6	
71	BB7	100
72	BB7	
73	GG0	100
74	GG0	
75	GG1	100
76	GG1	
77	GG2	100
78	GG2	
79	GG3	100
80	GG3	
81	GG4	100
82	GG4	
83	GG5	100
84	GG5	
85	GG6	100
86	GG6	
87	GG7	100
88	GG7	
89	RR0	100
90	RR0	
91	RR1	100
92	RR1	

PAD NO.	PAD NAME	max. wiring resistance(Ohm)
93	RR2	100
94	RR2	
95	RR3	100
96	RR3	
97	RR4	100
98	RR4	
99	RR5	100
100	RR5	
101	RR6	100
102	RR6	
103	RR7	100
104	RR7	
105	DEN	100
106	DEN	
107	HSYNC	100
108	HSYNC	
109	VSYNC	100
110	VSYNC	
111	DOTCLK	100
112	DOTCLK	
113	SHUT	100
114	SHUT	
115	VSS	
116	TB	100
117	VDDIO	
118	REV	100
119	VSS	
120	REGVDD	100
121	VDDIO	
122	RL	100
123	VSS	
124	CM	100
125	VDDIO	
126	BGR	100
127	VSS	
128	SEL0	100
129	SEL1	100
130	SEL2	100
131	VDDIO	
132	SWD0	100
133	VSS	
134	SWD1	100
135	VDDIO	
136	SWD2	100
137	VSS	
138	CPE	100
139	PINV	100

PAD NO.	PAD NAME	max. wiring resistance(Ohm)
140	DUMMY	
141	VCIM	10
142	VCIM	
143	VCIM	
144	VCIM	
145	VCIM	
146	C1P	10
147	C1P	
148	C1P	
149	C1P	
150	C1P	
151	C1N	10
152	C1N	
153	C1N	
154	C1N	
155	C1N	
156	VLCD63	10
157	VLCD63	
158	VLCD63	
159	VLCD63	
160	VLCD63	
161	VLCD63	
162	VCIX2J	5
163	VCIX2J	
164	VCIX2J	
165	VCIX2J	
166	VCIX2J	
167	VCIX2J	
168	VCIX2	5
169	VCIX2	
170	VCIX2	
171	VCIX2	
172	VCIX2	
173	VCIX2	
174	CYN	5
175	CYN	
176	CYN	
177	CYN	
178	CYN	
179	CYN	
180	CYP	5
181	CYP	
182	CYP	
183	CYP	
184	CYP	
185	CYP	

PAD NO.	PAD NAME	max. wiring resistance(Ohm)
186	CXN	5
187	CXN	
188	CXN	
189	CXN	
190	CXN	
191	CXN	
192	CXP	5
193	CXP	
194	CXP	
195	CXP	
196	CXP	
197	CXP	
198	VDDIO	10
199	VDDIO	
200	VDDIO	
201	VDDIO	
202	VDDIO	
203	VDDIO	
204	VCIP	10
205	VCIP	
206	VCIP	
207	VCIP	
208	VCI	5
209	VCI	
210	VCI	
211	VCI	
212	VCI	
213	VCI	
214	VCI	
215	VCI	
216	VCI	
217	VCI	
218	VDD	7.5
219	VDD	
220	VDD	
221	VDD	
222	VDD	
223	VDD	
224	DUMMY	
225	CN	10
226	CN	
227	CN	
228	CP	10
229	CP	
230	CP	

PAD NO.	PAD NAME	max. wiring resistance(Ohm)
231	VGL	10
232	VGL	
233	VGL	
234	VGL	
235	VGL	
236	C2N	10
237	C2N	
238	C2N	
239	C2P	10
240	C2P	
241	C2P	
242	C3N	10
243	C3N	
244	C3N	
245	C3P	10
246	C3P	
247	C3P	
248	VGH	10
249	VGH	
250	VGH	
251	VGH	
252	VGH	
253	TEST17	
254	TEST16	
255	VCOMR	100
256	VCOMR	
257	VCOML	7.5
258	VCOML	
259	VCOML	
260	VCOML	
261	VCOMH	7.5
262	VCOMH	
263	VCOMH	
264	VCOMH	
265	VCOM	7.5
266	VCOM	
267	VCOM	
268	VCOM	
269	VSSRC	7.5
270	VSSRC	
271	VSSRC	
272	VSSRC	
273	VSSRC	
274	VSSRC	
275	VSSRC	
276	VSSRC	

PAD NO.	PAD NAME	max. wiring resistance(Ohm)
277	VCHS	5
278	VCHS	
279	VCHS	
280	VCHS	
281	VCHS	
282	VCHS	
283	VCHS	
284	VCHS	
285	VCHS	
286	VCHS	
287	DUMMY	
288	VFB	100
289	VFB	
290	DRV	100
291	DRV	
292	DUMMY	
293	THROUGH2	
294	THROUGH1	

5.Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2006/12/08	New setup
	2006/12/15	1.Add FPC and Glass layout with internal charge pumb 2. Add FPC, Power connection and LED Backlight Driving Circuit with internal charge pumb 3.Add FPC and Glass layout without internal charge pumb 4.Add FPC, Power connection without internal charge pumb 5. Modify Figure 3.4、3.6
	2007/01/03	1. Modify Figure 3.4 2. Modify Figure 3.8