AIP31107

64CH COMMON DRIVER FOR DOT MATRIX LCD

1、GENERAL DESCRIPTION

The AIP31107 is an LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 output drivers. It generates the timing signal to control the AIP31108 (64 channel segment driver).

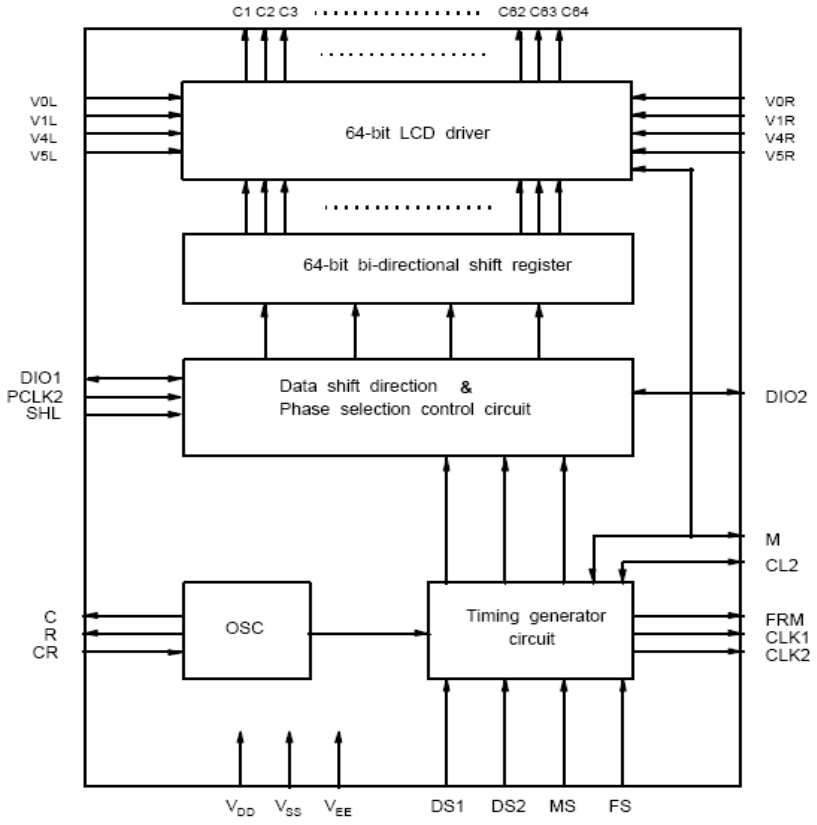
The AIP31107 is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the AIP31108 (64 channel segment driver).

Features

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage: + 5V ±10%
- LCD driving voltage: 8V~17V （V_{DD}-V_{EE}）
- High voltage CMOS process
- Chip size: 3180×3840 (μm×μm).
- The IC substrate should be connected to V_{DD} or float in the PCB layout artwork.
- 100QFP and bare chip available

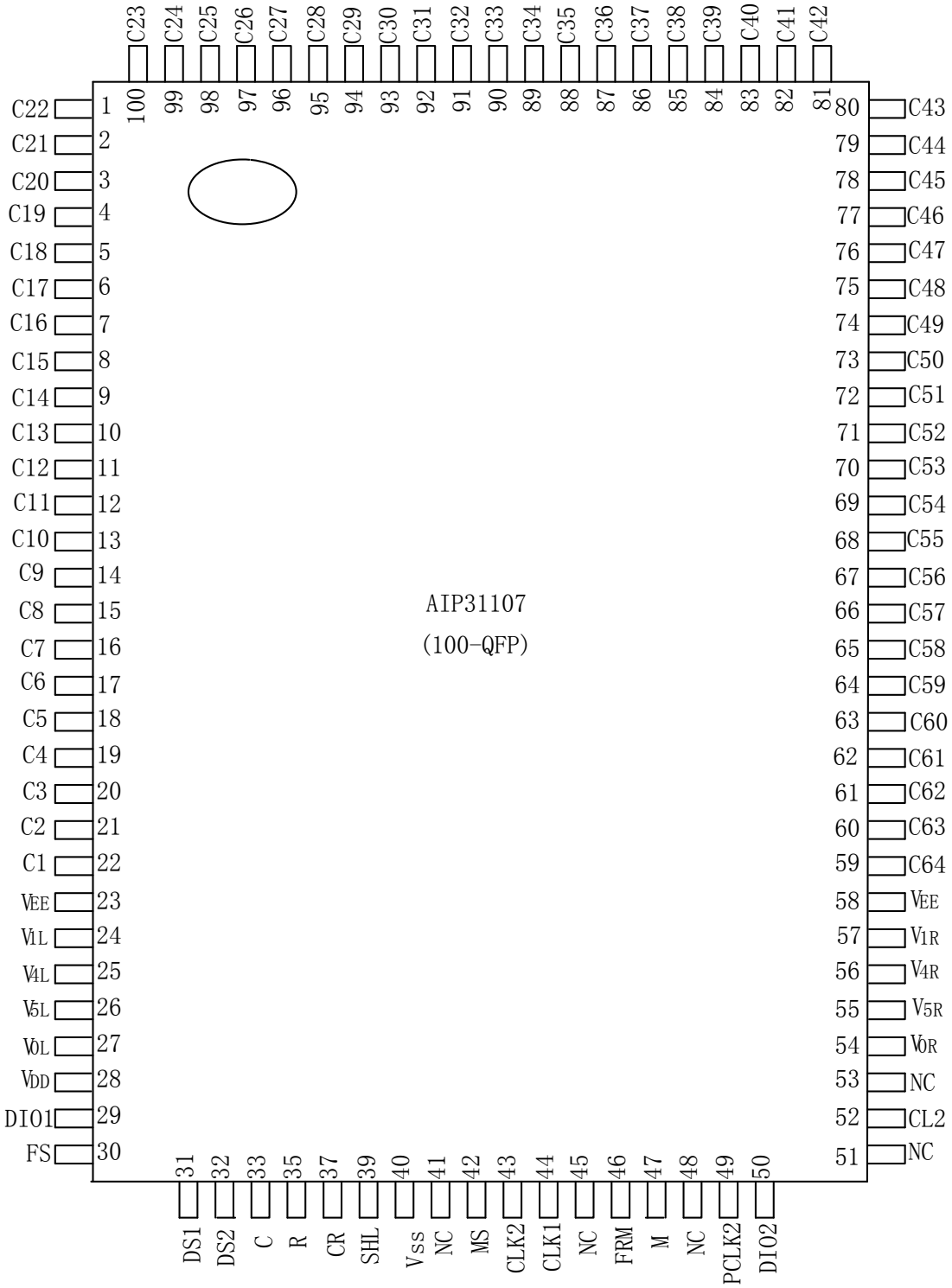
2、BLOCK DIAGRAM AND PIN DESCRIPTION

2.1、BLOCK DIAGRAM



2.2、PIN CONFIGURATIONS

100-QFP



2.3、PIN DESCRIPTION

<table>
<tr><th>Pin No.(QFP)</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>28
40
23,58</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Power</td><td>For internal logic circuit(+5V±10%)
GND (0 V)
For LCD driver circuit</td></tr>
<tr><td>27,54
24,57
25,56
26,55</td><td>V_{0L}, V_{0R}
V_{1L}, V_{1R}
V_{4L}, V_{4R}
V_{5L}, V_{5R}</td><td>Power</td><td>Bias supply voltage terminals to drive LCD.
<table><tr><td>Select Level Non</td><td>Select Level</td></tr><tr><td>$V_{0L(R)}$,$V_{5L(R)}$</td><td>$V_{1L(R)}$, $V_{4L(R)}$</td></tr></table>$V_{0L}$and V_{0R}（V_{1L}&V_{1R}，V_{4L}&V_{4R}, V_{5L}&V_{5R}）should be connected by the same voltage.</td></tr>
<tr><td>42</td><td>MS</td><td>I</td><td>Selection of master/slave mode
- Master mode（MS=1）
DIO1, DIO2, CL2 and M is output state.
- Slave mode（MS=0）
SHL=1→DIO1is input state(DIO2 is output state)
SHL=0→DIO2is input state(DIO1is output state)
CL2 and M are input state.</td></tr>
<tr><td>39</td><td>SHL</td><td>I</td><td>Selection of data shift direction.
<table><tr><td>SHL</td><td>Data shift direction</td></tr><tr><td>H</td><td>DIO1→C1…C64→DIO2</td></tr><tr><td>L</td><td>DIO2→C64…C1→DIO1</td></tr></table></td></tr>
<tr><td>49</td><td>PCLK2</td><td>I</td><td>Selection of shift clock (CL2) phase.
<table><tr><td>PCLK2</td><td>Shift clock (CL2) phase</td></tr><tr><td>H</td><td>data shift at the rising edge of CL2</td></tr><tr><td>L</td><td>data shift at the falling edge of CL2</td></tr></table></td></tr>
<tr><td>30</td><td>FS</td><td>I</td><td>Selection of oscillation frequency.
- Master mode
When the frame frequency is 70 Hz, the oscillation frequency should be
FS=1—fosc=430KHz
FS=0—fosc=215KHz
- Slave mode
Connect to V_{DD}</td></tr>
<tr><td>31
32</td><td>DS1
DS2</td><td>I</td><td>Selection of display duty.
- Master mode
<table><tr><td>DS1</td><td>DS2</td><td>Duty</td></tr><tr><td>L</td><td>L</td><td>1/48</td></tr><tr><td>L</td><td>H</td><td>1/64</td></tr><tr><td>H</td><td>L</td><td>1/96</td></tr><tr><td>H</td><td>H</td><td>1/128</td></tr></table>-Slave mode
Connect to V_{DD}</td></tr>
</table>

3、ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

(Tamb=25°C, All voltage referenced to Vss, unless otherwise specified)

Characteristic	Symbol	Value	Unit	Note
Operating Voltage	V_{DD}	-0.3～+7.0	V	（1）
Supply Voltage	V_{EE}	V_{DD}-19.0～V_{DD}+0.3	V	（4）
Driver Supply Voltage	V_B	-0.3～V_{DD}+0.3	V	（1），（2）
	V_{LCD}	V_{EE}-0.3～V_{DD}+0.3	V	（3），（4）
Operating Temperature	T_{OPR}	-30～+85	℃	—
Storage Temperature	T_{STG}	-55～+125	℃	—
Soldering Temperature	T_L	245(10s)	℃	

Note : *1. Based on V_{SS}=0 V

*2. Applies to input terminals and I/O terminals at high impedance.

(Except $V_{0L(R)}$, $V_{1L(R)}$, $V_{4L(R)}$ and $V_{5L(R)}$)

*3. Applies to $V_{0L(R)}$, $V_{1L(R)}$, $V_{4L(R)}$ and $V_{5L(R)}$.

*4. Voltage level: $V_{DD} \geq V_{0L} = V_{0R} \geq V_{1L} = V_{1R} \geq V_{4L} = V_{4R} \geq V_{5L} = V_{5R} \geq V_{EE}$.

3.2、ELECTRICAL CHARACTERISTICS

3.2.1 DC Characteristics（V_{DD}=+5V±10%,V_{SS}=0V,|V_{DD}-V_{EE}|=8～17V,Ta=-30～+85℃）

Characteristic		Symbol	condition	Min	Typ	Max	Unit	Note
Input Voltage	H	V_{IH}	—	0.7V_{DD}	—	V_{DD}	V	(1)
	L	V_{IL}		V_{SS}	—	0.3V_{DD}		
Output Voltage	H	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	—	—	V	(2)
	L	V_{OL}	I_{OL}=0.4mA	—	—	0.4		
Input Leakage Current		I_{LKG}	V_{IN}=V_{DD}-V_{SS}	-1.5	—	1.5	uA	(1)
OSC Frequency		f_{OSC}	Rf=47KΩ±2% Cf=20pf±5%	315	450	585	KHz	
On Resistance		R_{ON}	V_{DD}-V_{EE}=17V Load current=±150uA	—	—	1.5	KΩ	
Operating Current		I_{DD1}	1/128（Master mode）	—	—	1.2	mA	(3)
		I_{DD2}	1/128（Slave mode）	—	—	200	uA	(4)
Supply Current		I_{EE}	1/128（Master mode）	—	—	100	uA	(5)

Operating Frequency	f_{OP1}	Master mode External clock	50	—	600	KHz	
	f_{OP2}	Slave mode	0.5	—	1500		

*1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.

*2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the output state.

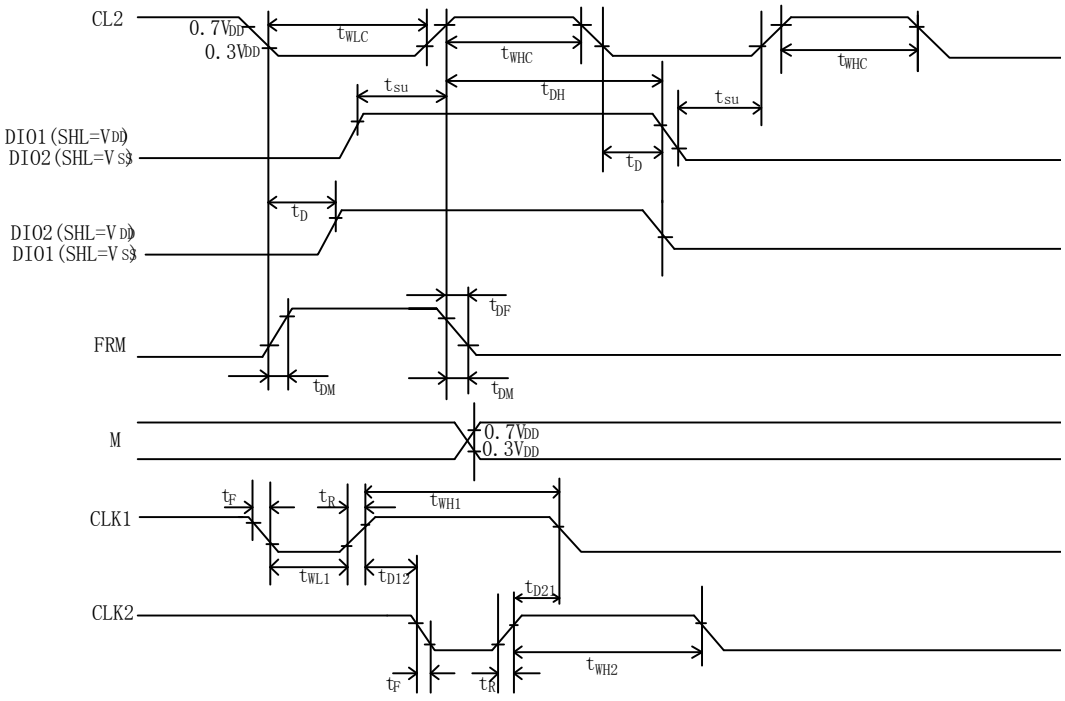
*3. This value is specified at about the current flowing through V_{SS}.
Internal oscillation circuit: Rf=47 kΩ, Cf=20 pf, Each terminal of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.

*4. This value is specified at about the current flowing through V_{SS}.
Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD}, and MS is connected to V_{SS}. CL2, M, DIO1 is external clock.

*5. This value is specified at about the current flowing through V_{EE}.
Don' t connect to V_{LCD} (V1~V5).

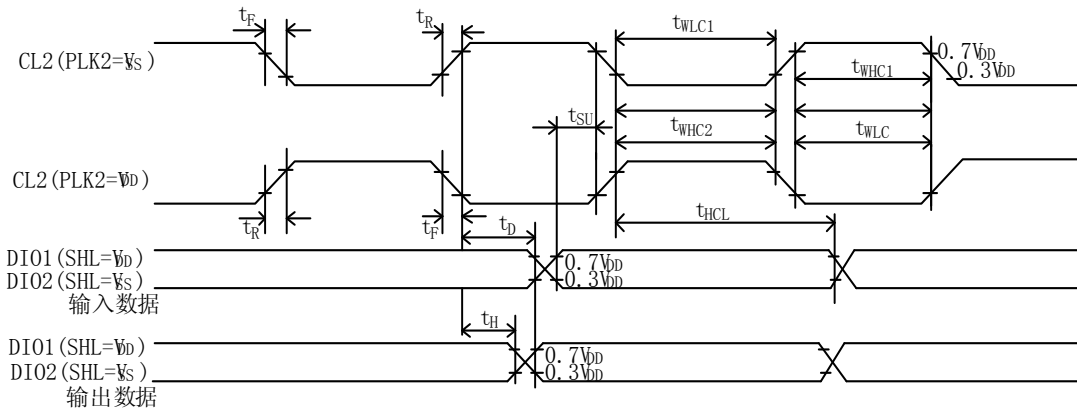
3.2.2、AC Characteristics（V_{DD}=5V±10%，TA=-30℃～+85℃）

Master mode（MS=V_{DD}，PCLK2=V_{DD}，Cf=20pF，Rf=47KΩ）



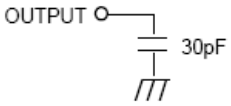
Characteristic	Symbol	Min	Typ	Max	Unit
Data Setup Time	t_{SU}	20	—	—	uS
Data Hold Time	t_{DH}	40	—	—	
Data Delay Time	t_D	5	—	—	
FRM Delay Time	t_{DF}	-2	—	2	
M Delay Time	t_{DM}	-2	—	2	
CL2 Low Level Widt	t_{WLC}	35	—	—	
CL2 High Level Width	t_{WHC}	35	—	—	nS
CLK1 Low Level Width	t_{WL1}	700	—	—	
CLK2 Low Level Width	t_{WL2}	700	—	—	
CLK1 High Level Width	t_{WH1}	2100	—	—	
CLK2 High Level Width	t_{WH2}	2100	—	—	
CLK1-CLK2 Phase Difference	t_{D12}	700	—	—	
CLK2-CLK1 Phase Difference	T_{D21}	700	—	—	
CLK1，CLK2 Rise/Fall Time	t_R/t_F	—	—	150	

Slave mode ($MS=V_{SS}$)



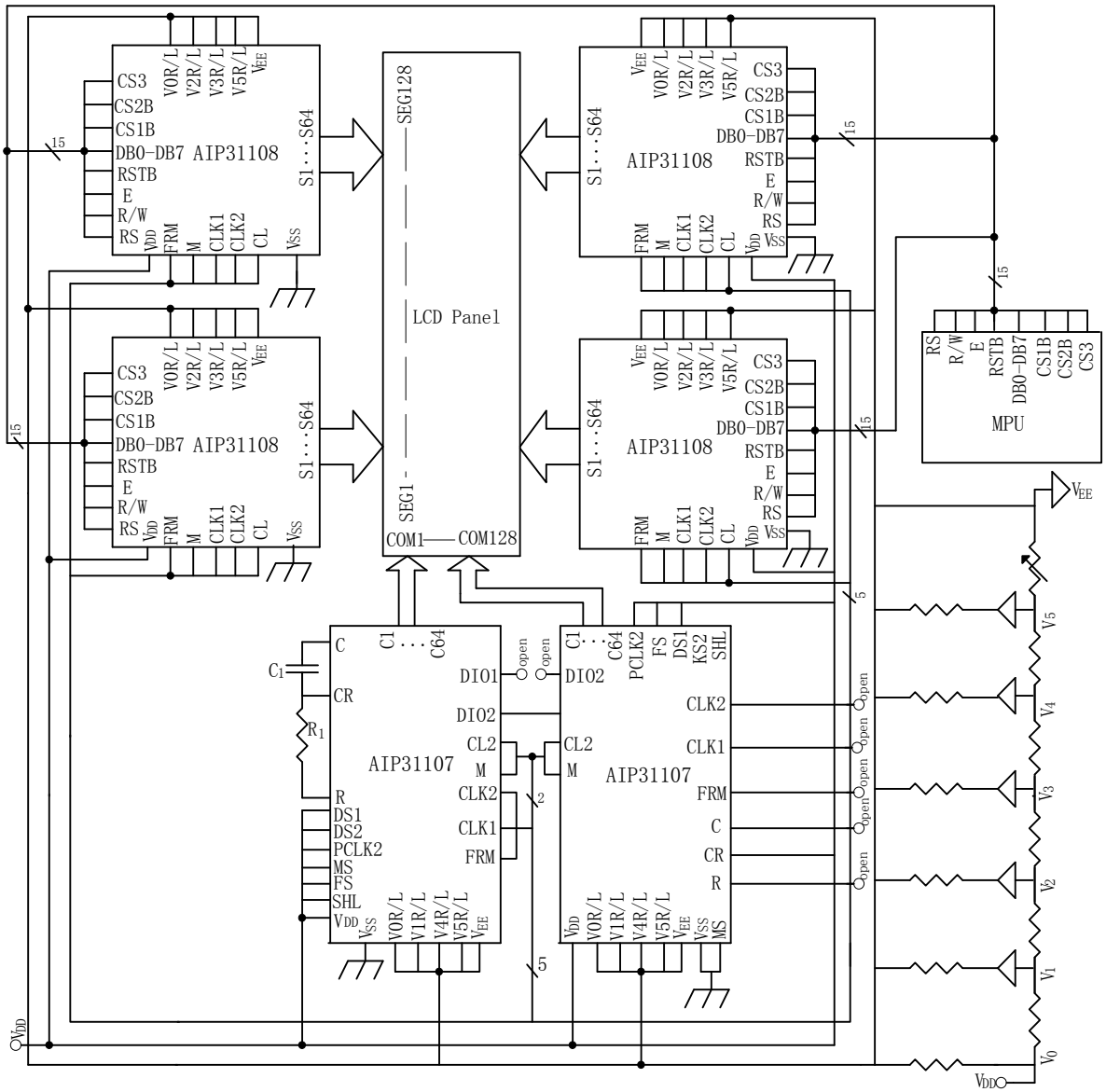
Characteristics	Symbol	Min	Typ	Max	Unit	Note
CL2 Low Level Width	t_{WLC1}	450	—	—	ns	PCLK2=V_{SS}
CL2 High Level Width	t_{WHC1}	150	—	—	ns	PCLK2=V_{SS}
CL2 Low Level Width	t_{WLC2}	150	—	—	ns	PCLK2=V_{DD}
CL2 High Level Width	t_{WHL}	450	—	—	ns	PCLK2=V_{DD}
Data Setup Time	t_{SU}	100	—	—	ns	
Data Hold Time	t_{DH}	100	—	—	ns	
Data Delay Time	t_D	—	—	200	ns	*1
Output Data Hold Time	t_H	10	—	—	ns	
CL2 Rise/Fall Time	t_R/t_F	—	—	30	ns	

*1; Connect load CL=30 pF



4、TYPICAL APPLICATION CIRCUIT AND FUNCTION DESCRIPTION

4. 1、APPLICATION CIRCUIT



4. 2、APPLICATION NOTE

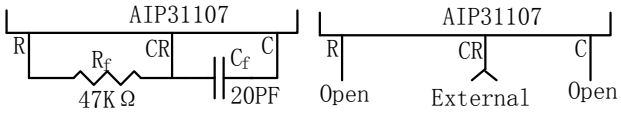
Functional Description

RC Oscillator

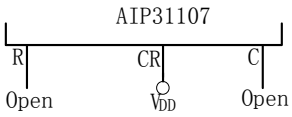
The RC Oscillator generates CL2, M, FRM of the AIP31107, and CLK1 and CLK2 of the AIP31108 by the oscillation resister R and capacitor C.

When selecting the master/slave mode, the oscillation circuit is as following:

1) Master Mode: in the master mode, use these terminals as shown below.



2) Slave Mode: in the slave mode, stop the oscillator as shown below.



Timing Generation Circuit

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

1) Selection of Master/Slave (M/S) Mode

When M/S is “H”, it generates CL2, M, FRM, CLK1 and CLK2 internally.

When M/S is “L”, it operates by receiving M and CL2 from the master device.

2) Frequency Selection (FS)

To adjust FRM frequency by 70 Hz, the oscillation frequency should be as follows:

FS	**Oscillation Frequency**
H	fosc=430KHz
L	fosc=215KHz

In the slave mode, it is connected to V_{DD}

3) Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

DS1	DS2	Duty
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

Data Shift & Phase Select Control

1) Phase Selection

It is a circuit to shift data on synchronization or rising edge, or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

2) Data Shift Direction Selection

When M/S is connected to V_{DD}, DIO1 and DIO2 terminal is only output.

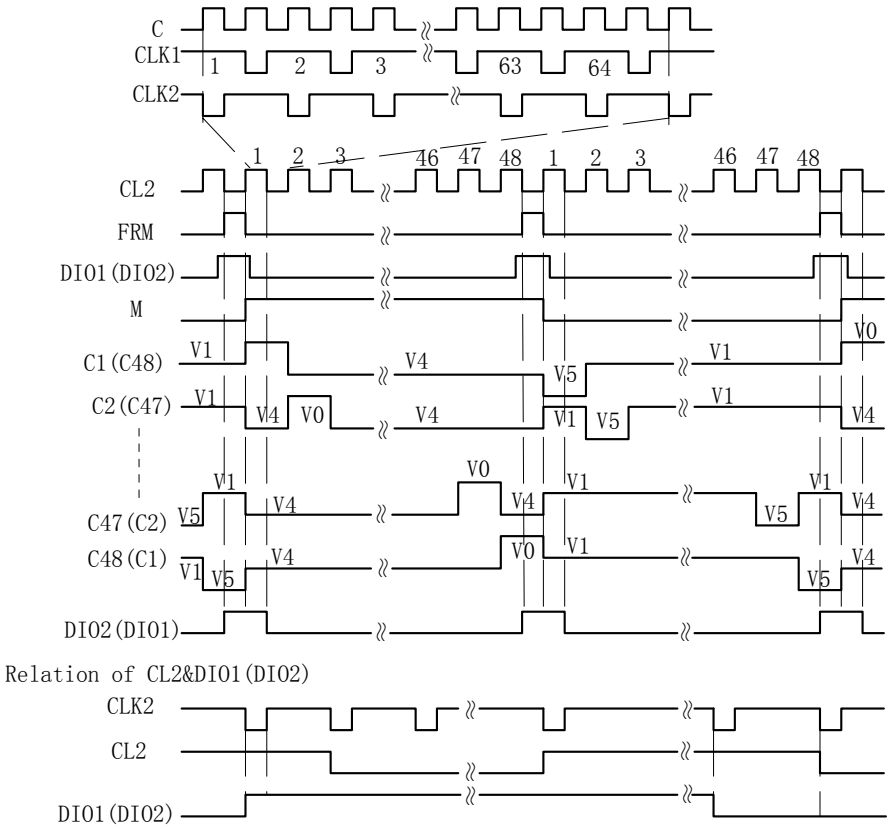
When M/S is connected to V_{SS}, it depends on the SHL.

MS	SHL	DIO1	DIO2	Direction of Data
H	H	O	O	C1→C64
	L	O	O	C64→C1
L	H	I	O	DIO1→C1→C64→DIO2
	L	O	I	DIO2→C64→C1→DIO1

Timing Diagram

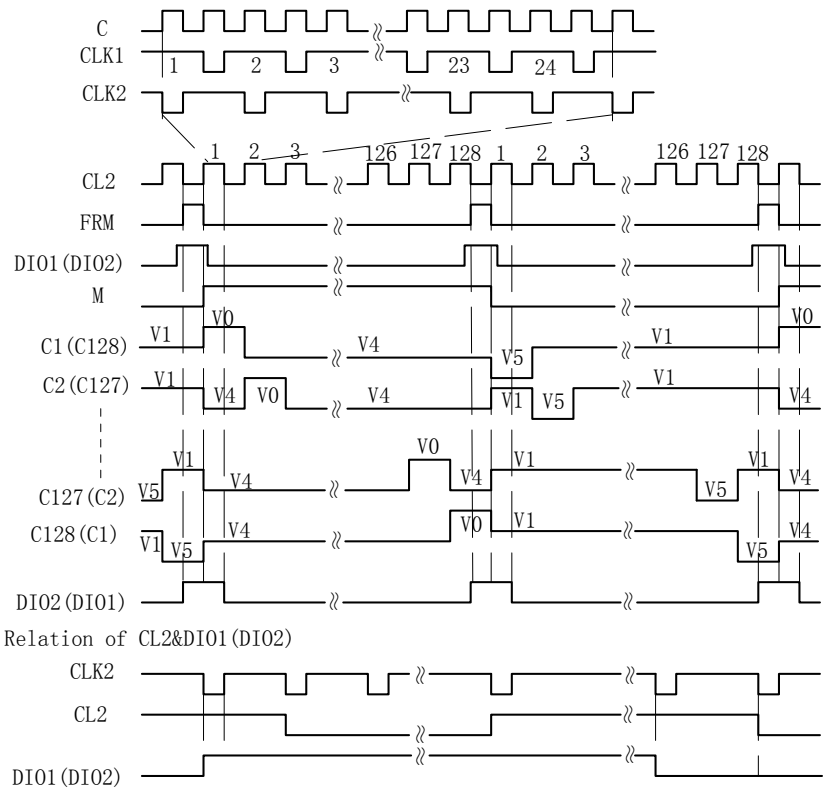
1/48 Duty Timing (Master Mode)

Condition: DS1=L, DS2=L, SHL=H(L), PCLK2=H



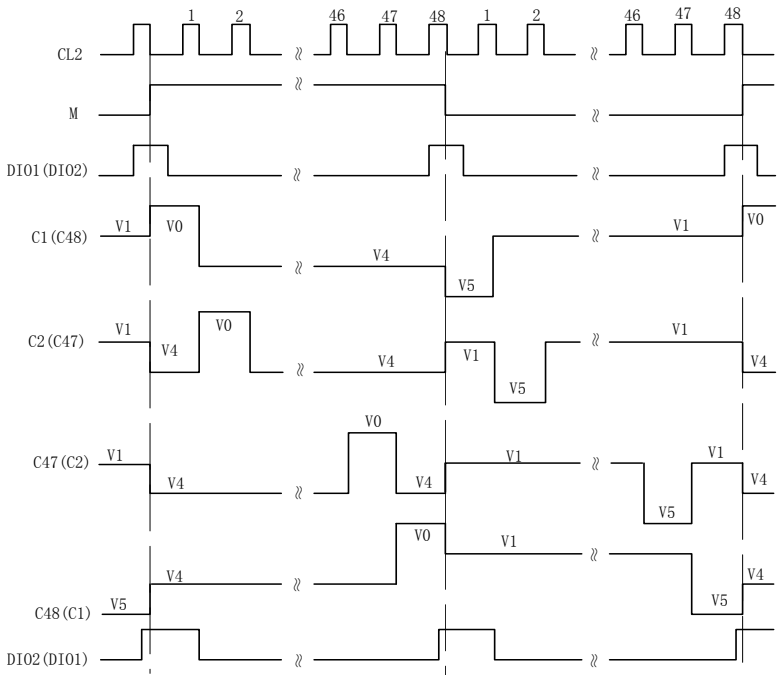
1/128 duty timing (Master mode)

Condition: DS1=H, DS2=H, SHL=H(L), PCLK2=H

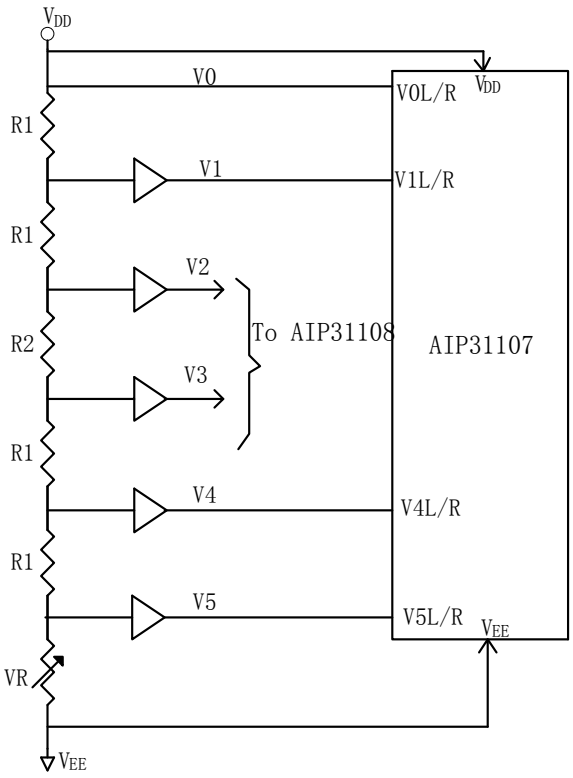


1/48 Duty Timing (Slave Mode)

Condition: PCLK2=L, SHL=H(L)



Power Driver Circuit



Relation of duty & bias

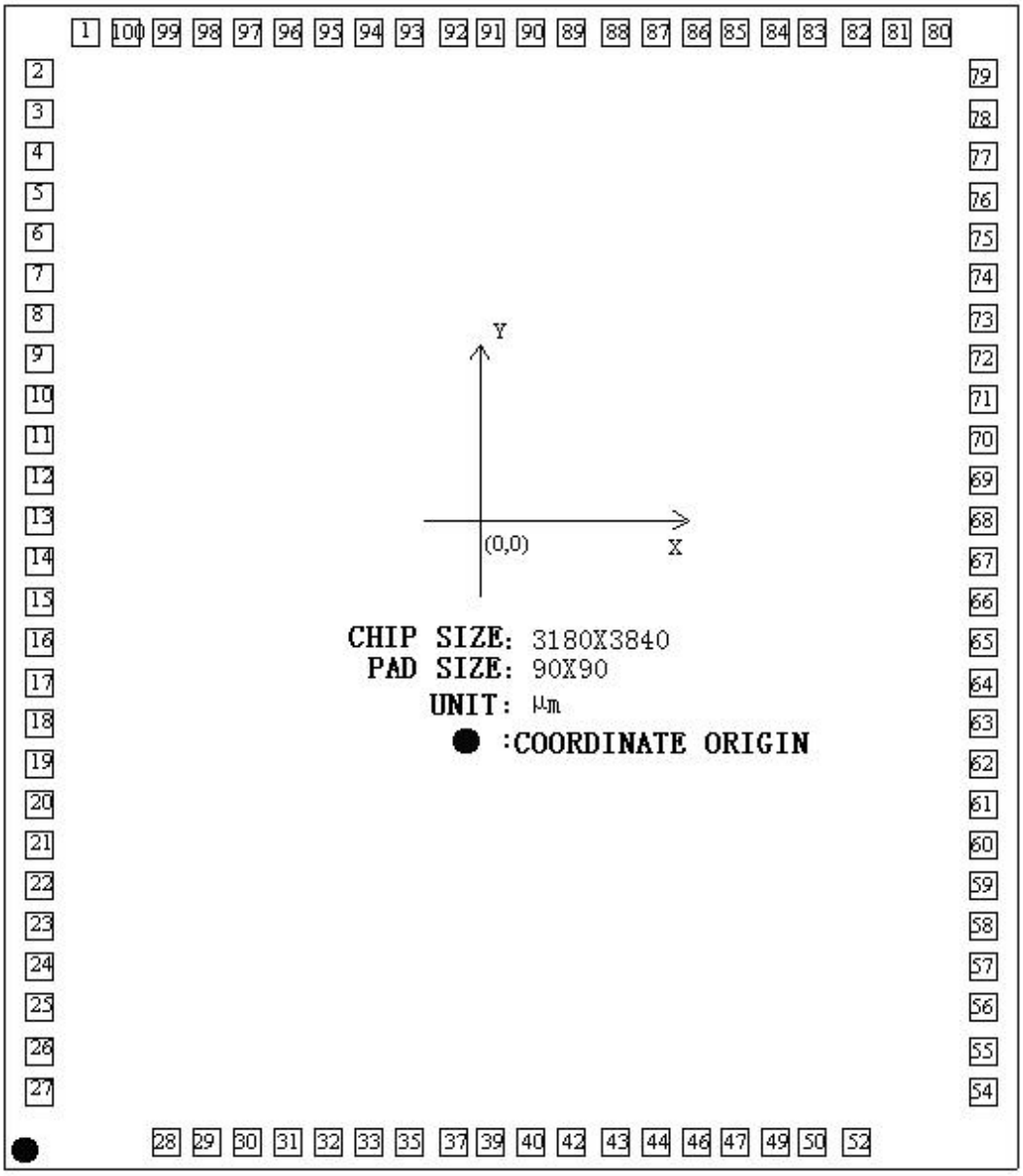
Duty	Bias	RDIV
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

*When duty factor is 1/48, the value of R1 & R2 should satisfy.

R1/(4R1+R2)=1/8,R1=3 KΩ, R2=12 KΩ

5、PAD DIAGRAM AND PAD LOCATION

5.1、PAD DIAGRAM



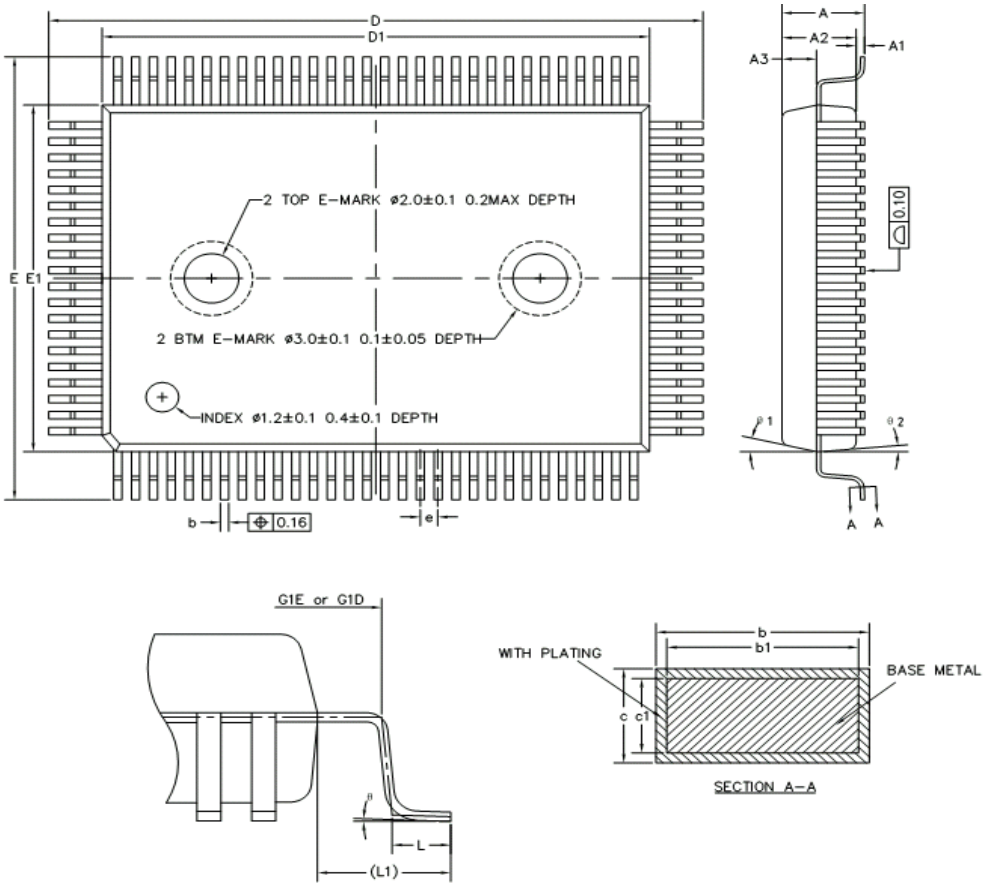
5.2、PAD Location （UNIT:μm）

序号	PAD 名	X	Y	序号	PAD 名	X	Y
1	C22	278.50	3542.10	51	NC		
2	C21	145.00	3347.70	52	CL2	2555.40	145.00
3	C20	145.00	3227.70	53	NC		
4	C19	145.00	3107.70	54	V_{0R}	2932.00	347.70
5	C18	145.00	2987.70	55	V_{5R}	2932.00	467.70
6	C17	145.00	2867.70	56	V_{4R}	2932.00	587.70
7	C16	145.00	2747.70	57	V_{1R}	2932.00	707.70
8	C15	145.00	2627.70	58	V_{EE}	2932.00	827.70
9	C14	145.00	2507.70	59	C64	2932.00	947.70
10	C13	145.00	2387.70	60	C63	2932.00	1067.70
11	C12	145.00	2267.70	61	C62	2932.00	1187.70
12	C11	145.00	2147.70	62	C61	2932.00	1307.70
13	C10	145.00	2027.70	63	C60	2932.00	1427.70
14	C9	145.00	1907.70	64	C59	2932.00	1547.70
15	C8	145.00	1787.70	65	C58	2932.00	1667.70
16	C7	145.00	1667.70	66	C57	2932.00	1787.70
17	C6	145.00	1547.70	67	C56	2932.00	1907.70
18	C5	145.00	1427.70	68	C55	2932.00	2027.70
19	C4	145.00	1307.70	69	C54	2932.00	2147.70
20	C3	145.00	1187.70	70	C53	2932.00	2267.70
21	C2	145.00	1067.70	71	C52	2932.00	2387.70
22	C1	145.00	947.70	72	C51	2932.00	2507.70
23	V_{EE}	145.00	827.70	73	C50	2932.00	2627.70
24	V_{1L}	145.00	707.70	74	C49	2932.00	2747.70
25	V_{4L}	145.00	587.70	75	C48	2932.00	2867.70
26	V_{5L}	145.00	467.70	76	C47	2932.00	2987.70
27	V_{0L}	145.00	347.70	77	C46	2932.00	3107.70
28	V_{DD}	515.40	145.00	78	C45	2932.00	3227.70
29	DIO1	635.40	145.00	79	C44	2932.00	3347.70
30	FS	755.40	145.00	80	C43	2798.50	3542.10

31	DS1	875.40	145.00	81	C42	2678.50	3542.10
32	DS2	995.40	145.00	82	C41	2558.50	3542.10
33	C	1115.40	145.00	83	C40	2438.50	3542.10
34	NC			84	C39	2318.50	3542.10
35	R	1235.40	145.00	85	C38	2198.50	3542.10
36	NC			86	C37	2078.50	3542.10
37	CR	1355.40	145.00	87	C36	1958.50	3542.10
38	NC			88	C35	1838.50	3542.10
39	SHL	1475.40	145.00	89	C34	1718.50	3542.10
40	Vss	1595.40	145.00	90	C33	1598.50	3542.10
41	NC			91	C32	1478.50	3542.10
42	MS	1715.40	145.00	92	C31	1358.50	3542.10
43	CLK2	1835.40	145.00	93	C30	1238.50	3542.10
44	CLK1	1955.40	145.00	94	C29	1118.50	3542.10
45	NC			95	C28	998.50	3542.10
46	FRM	2075.40	145.00	96	C27	878.50	3542.10
47	M	2195.40	145.00	97	C26	758.50	3542.10
48	NC			98	C25	638.50	3542.10
49	PCLK2	2315.40	145.00	99	C24	518.50	3542.10
50	DIO2	2435.40	145.00	100	C23	398.50	3542.10

6、PACKAGE INFORMATION

6. 1、QFP100-14×20-0.65



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.30
A1	0.10	–	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.27	–	0.37
b1	0.27	0.30	0.33
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.55	0.65	0.75
G1D	22.00REF		
G1E	16.00REF		
L	0.60	0.80	1.00
L1	1.95REF		
θ	0°	2°	8°
θ 1	11°	13°	15°
θ 2	3°	5°	7°

7、STATEMENTS AND NOTES：

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

7.2 NOTION:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

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8、CONTACT：

Wuxi I-CORE Electronics Co., Ltd.

Addr：2F Building9，100Di cui Road, LiYuan Development Zone, Wuxi, jiangsu, China

P.C: 214072 Tel：0510-81888895 Fax：0510-85572700

Marketing Department：2F Building9，100Di cui Road, LiYuan Development Zone, Wuxi, jiangsu, China

P.C: 214072 Tel：0510-85572708 Fax：0510-85887721

Shenzhen office：26F Building12, xiangli garden hongli west Road, Shenzhen, Guangdong ,China

P.C: 518000 Tel：0755-88370509 Fax：0755-88370507

Guangzhou office：901room-57,ledeGarden, leming fiest street,Guanghua Road, baiyun District,Guangzhou,China

Tel：020-36743257 Fax：020-36743257

Applied Technical Services：

Application Department：

2F Building9，100Di cui Road, LiYuan Development Zone, Wuxi, jiangsu, China

P.C：214072 Tel：0510-85572715 Fax：0510-85572700

26F Building12, xiangli garden hongli west Road, Shenzhen, Guangdong ,China

P.C：518000 Tel：0755-88370509 Fax：0755-88370507