MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI1602M

Revision	
Engineering	
Date	
Our Reference	

CONTENTS

3. PRECAUTIONS FOR LCM

3.1 Precautions in handling LCD Modules (hereinafter LCMs)

Multi-Inno's LCMs have been assembled and accurately calibrated before delivery.

Please observe the following criteria when handling.

A. Do not subject the module to excessive shock.

B. Do not modify the tab on the metal holder.

C. Do not tamper with the printed circuit board.

D. Limit the soldering of the printed circuit board to I/O terminals only.

E. Do not touch the zebra strip nor modify its location.

3.2 Static electricity warning

Multi-Inno's LCM uses CMOS LSI technology. Therefore, strict measures to avoid static electricity discharge are followed through all processes from manufacturing to shipping. When handling a LCM, take sufficient care to prevent static electricity discharge as you would any CMOS IC.

A. Do not take the LCM from its anti-static bag until it's to be assembled.

LCM's are individually packaged in bags specially treated to resist static electricity. When storing, keep the LCM packed in the original bags, or store them in a container processed to be resistant to static electricity, or in an electric conductive container.

B. Always use a ground strap when handling a LCM.

Always use a ground strap while working with the module, from the time it is taken out of the anti-static bag until it is assembled. If it is necessary to transfer the LCM, once it has been taken out of the bag, always place it in an electric conductive container. Avoid wearing clothes made of chemical fibers, the use of cotton or conductive treated fiber clothing is recommended.

C. Use a no-leak iron for soldering the LCM.

The soldering iron to be used for soldering the I/O terminals to the LCM are to be insulated or grounded at the iron tip.

D. Always ground electrical apparatuses required for assembly.

Electrical apparatuses required to assemble the LCM into a product, i.e. electrical screw drivers, are to be first grounded to avoid transmitting spike noises from the motor.

E.Assure that the work bench is properly grounded.

F. Peel off the LCM protective film slowly.

The module is attached with a film to protect the display surface from contamination, damage, adhesion of flux, etc. Peeling off this film abruptly could cause static electricity to be generated, so peel the tape slowly.

G. Pay attention to the humidity in the work area.

50~60% RH is recommended.

3.3 Precautions for the soldering of a LCM

The following procedures should be followed when soldering the LCM:

A. Solder only to the I/O terminal.

B. Use a no leakage soldering iron and pay particular attention to the following:

(1) Conditions for soldering I/O terminals

Temperature at iron tip: 280℃ + 10℃

Soldering time: 3~4 sec/terminal

Type of solder: Eutectic solder (rosin flux filled)

Note: (Avoid using flux, because it could penetrate the module and the module may get contaminated during cleaning.) Peel off protective film after soldering the I/O terminals. By following this procedure, the surface contamination caused by the dispersion of flux while soldering can be avoided.

(2) Removing the wiring

(When a lead wire, or a connector to the I/O terminal of the module is to be removed, remove it only after the solder at the connection has sufficiently melted since the I/O terminal is a through hole.) If it is forcefully removed, it could cause the terminal to break or peel. The recommended procedure is to use a suction-type solder remover. Caution: do not reheat the I/O terminal more than 3 times.

3.4 Long-term storage

If the correct method of storage is not followed, deterioration of the display material (polarizer) and oxidation of the I/O terminal plating may make the process of soldering difficult. Please comply with the following procedure.

A. Store in the shipping container.

B. If the shipping container is not available, place in anti-static bags and seal the opening.

C. Store the modules where they are not subjected to direct sunlight or a fluorescent lamp.

D.Store in a tempeature range of 0℃ – 35℃ with low relative humidity.

3.5 Precautions in use of LCD modules

A. Do not give any external shock.

B. Do not wipe the surface with hard materials.

C. Do not apply excessive force on the surface.

D. Do not expose to direct sunlight or fluorescent light for a long time.

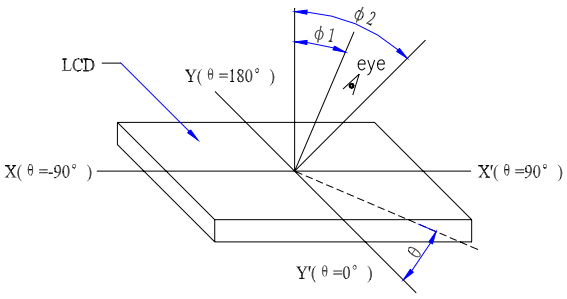
E. Avoid storage in high temperature and high humidity.

F. When storage for a long time at 40℃ or higher is required, R/H should be less than 60%.

G. Liquid in LCD is hazardous substance. Do not lick, swallow when the liquid is attached to your hands, skin, clothes etc. Wash it out thoroughly.

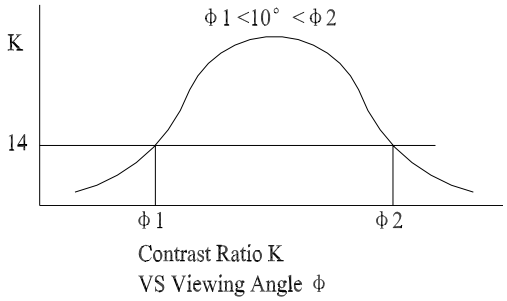
4. OPTICAL DEFINITIONS

4.1 Definition of angle θ and ϕ



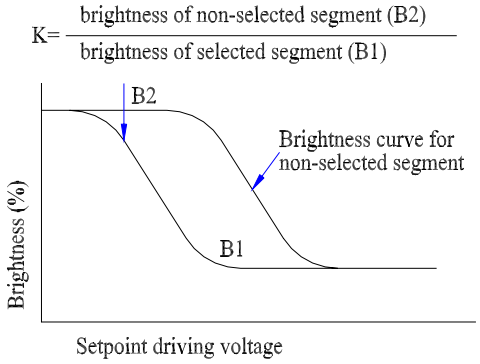
POSITIVE TYPE

4.2 Definition of viewing angle ϕ1 and ϕ2



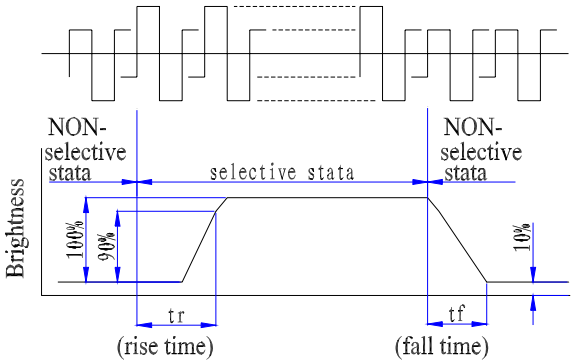
POSITIVE TYPE

4.3 Definition of contrast "K"



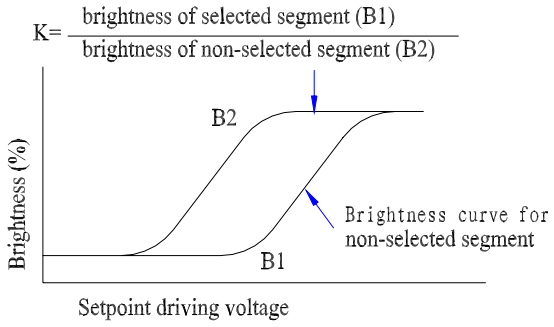
NEGATIVE TYPE

4.4 Definition of optical response

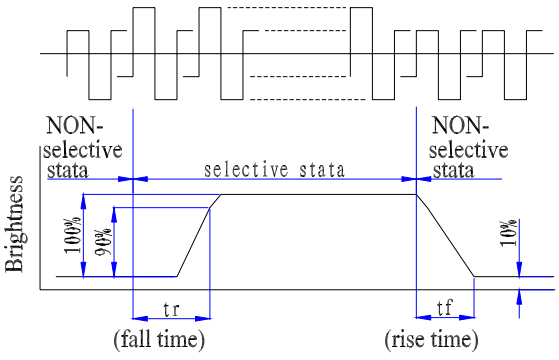


NEGATIVE TYPE

4.5 Definition of contrast "K"



4.6 Definition of optical response



5. Timing Characteristics and Electrical Characteristics

5.1 Timing Characteristics

(VDD=4.5V to 5.5V, Ta=-30 to +85℃)

Mode	Item	Symbol	Min	Type	Max	Unit
Write Mode (Refer to Figure 1)	E Cycle Time	ts	500	—	—	ns
	E Rise / Fall Time	tr, tf	—	—	20	ns
	E Pulse Width (High, Low)	tw	230	—	—	ns
	R/W and RS Setup Time	tsu1	40	—	—	ns
	R/W and RS Hold Time	th1	10	—	—	ns
	Data Setup Time	tsu2	80	—	—	ns
	Data Hold Time	th2	10	—	—	ns
Read mode (refer to figure 2)	E Cycle Time	tc	500	—	—	ns
	E Rise / Fall Time	tr,tf	—	—	20	ns
	E Pulse Width (High, Low)	tw	230	—	—	ns
	R/W and RS Setup Time	tsu	40	—	—	ns
	R/W and RS Hold Time	th	10	—	—	ns
	Data Output Time	t_D	—	—	120	ns
	Data Hold Time	t_{DH}	5	—	—	ns

(VDD=2.7V to 4.5V, Ta=-30 to +85℃)

Mode	Item	Symbol	Min	Type	Max	Unit
Write Mode (Refer to Figure 1)	E Cycle Time	tc	1000	—	—	ns
	E Rise / Fall Time	tr, tf	—	—	25	ns
	E Pulse Width (High, Low)	tw	450	—	—	ns
	R/W and RS Setup Time	tsu1	60	—	—	ns
	R/W and RS Hold Time	th1	20	—	—	ns
	Data Setup Time	tsu2	195	—	—	ns
	Data Hold Time	th2	10	—	—	ns
Read mode (refer to figure 2)	E Cycle Time	tc	1000	—	—	ns
	E Rise / Fall Time	tr,tf	—	—	25	ns
	E Pulse Width (High, Low)	tw	450	—	—	ns
	R/W and RS Setup Time	tsu	60	—	—	ns
	R/W and RS Hold Time	th	20	—	—	ns
	Data Output Time	t_D	—	—	360	ns
	Data Hold Time	t_{DH}	5	—	—	ns

Mode	Item	Symbol	Min	Type	*Max*	Unit
Interface Mode with Extension Driver (refer to figure 3)	Clock Pulse Width (High, Low)	tw	800	—	—	ns
	Clock Rise/Fall Time	tr, tf	—	—	25	ns
	Clock Setup Time	tsu1	500	—	—	ns
	Data Setup Time	tsu2	300	—	—	ns
	Data Hold Time	t_D	300	—	—	ns
	M Delay Time	t_{DH}	-1000	—	1000	ns

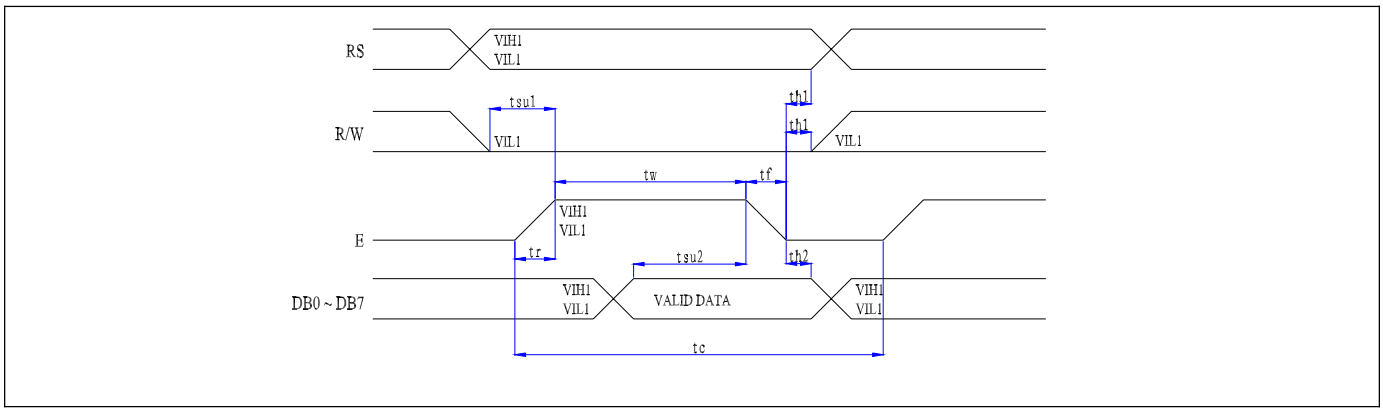


Figure 1. Write Mode Timing Diagram

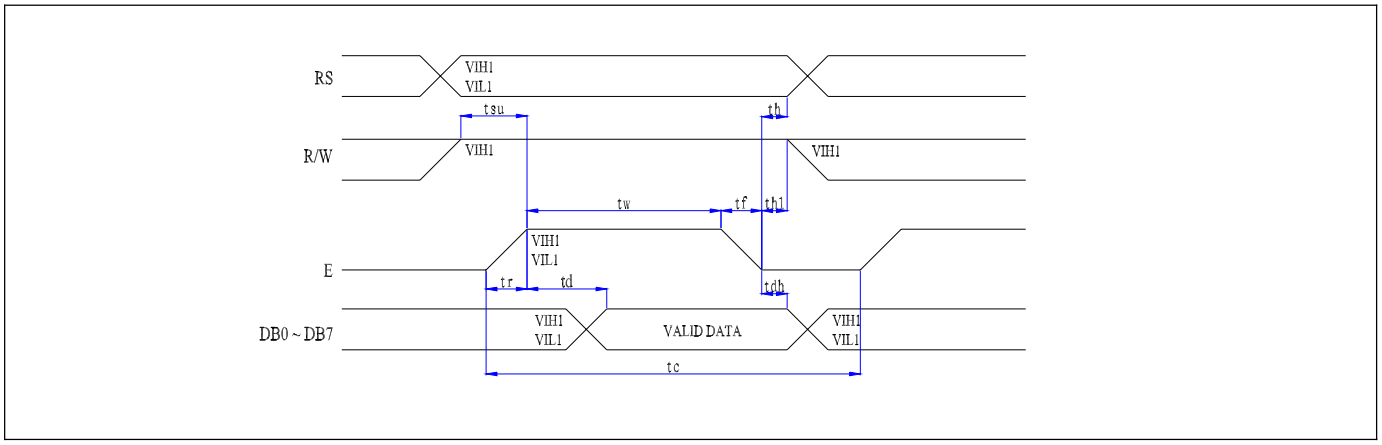


Figure 2. Read Mode Timing Diagram

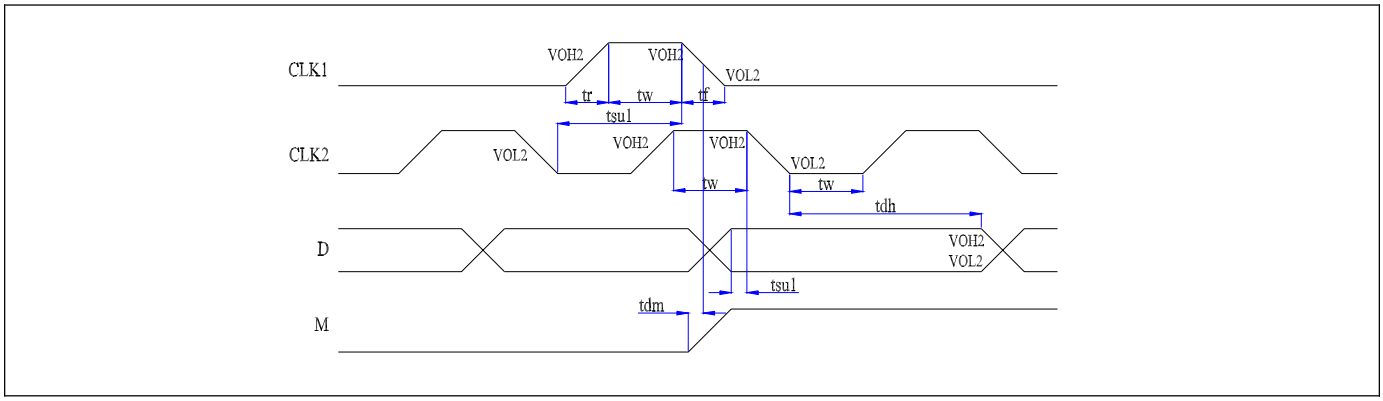


Figure 3. Interface Mode with Extension Driver Timing Diagram

5.2 Electrical Characteristics

DC Characteristics(VDD=4.5V to 5.5V, Ta=-30 to +85℃)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP	MAX.	UNIT
H LEVEL INPUT VOLTAGE	VIH	——	2.2	____	___	V
L LEVEL INPUT VOLTAGE	VIL	——	___	____	0.6	V
H LEVEL OUTPUT VOLTAGE	VOH	-IOH=0.205mA	2.4	____	___	V
L LEVEL OUTPUT VOLTAGE	VOL	IOL=1.2mA	___	____	0.4	V
POWER SUPPLY CURRENT (LOGIC)	IDD	VDD=5.0V	___	1.0	4	mA
RECOMMENDED LCD DRIVING VOLTAGE	VDD-V0 DUTY=1/16 Φ = 25 ^{0}	Ta=0℃	___	4.6	___	V
		Ta=25℃	___	4.2	___	V
		Ta=50℃	___	3.8	___	V
CLOCKOSCILLATION FREQUENCY	FOSC	Ta=25℃	___	270	___	KHz

6 FUNCTION DESCRIPTION

6.1 System Interface

This chip has all two kinds of interface type with MPU: 4-bit bus and 8-bit bus is selected by DL bit in the instruction register. During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.The instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use RS input pin in 4-bit /8-bit bus mode.

Table 1. Various Kinds of Operations according to RS and R/W Bits

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes instruction code into IR)
L	H	Read Busy flag (DB7) and address counter (DB0~DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

6.2 Busy Flag (BF)

When BF=High, it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS=Low and R/W=High (Read instruction Operation), through DB7 port. Befroe executing the next instruction, be sure that BF is not High..

6.3 Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS=Low and R/W=High, AC can be read through DB0 – DB6 ports.

6.4 Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Fig-4)

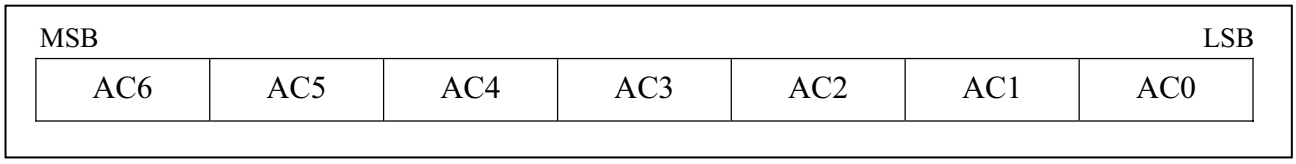
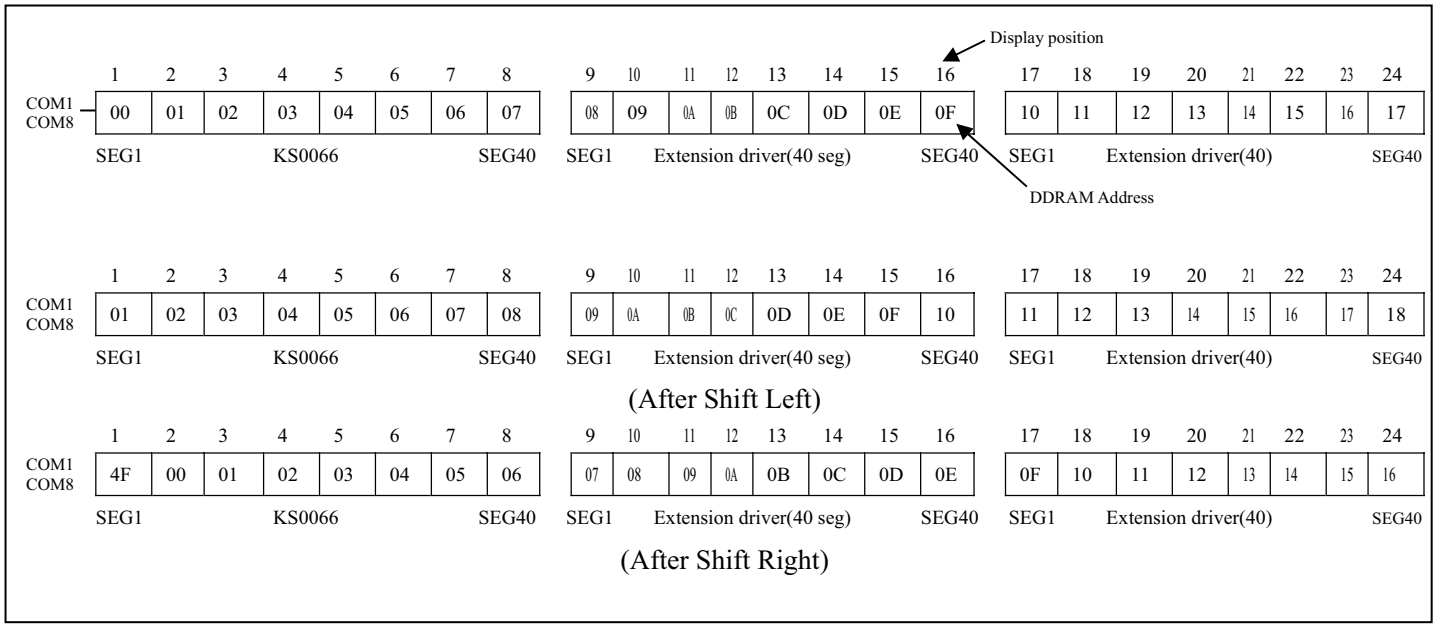


Figure 4. DDRAM Address

1) 1-line Display

In the case of a 1-line display, the address range of DDRAM is 00H-04H. An Extension driver will be used. Figure 5 shows the example when a 40-segment extension driver is added.

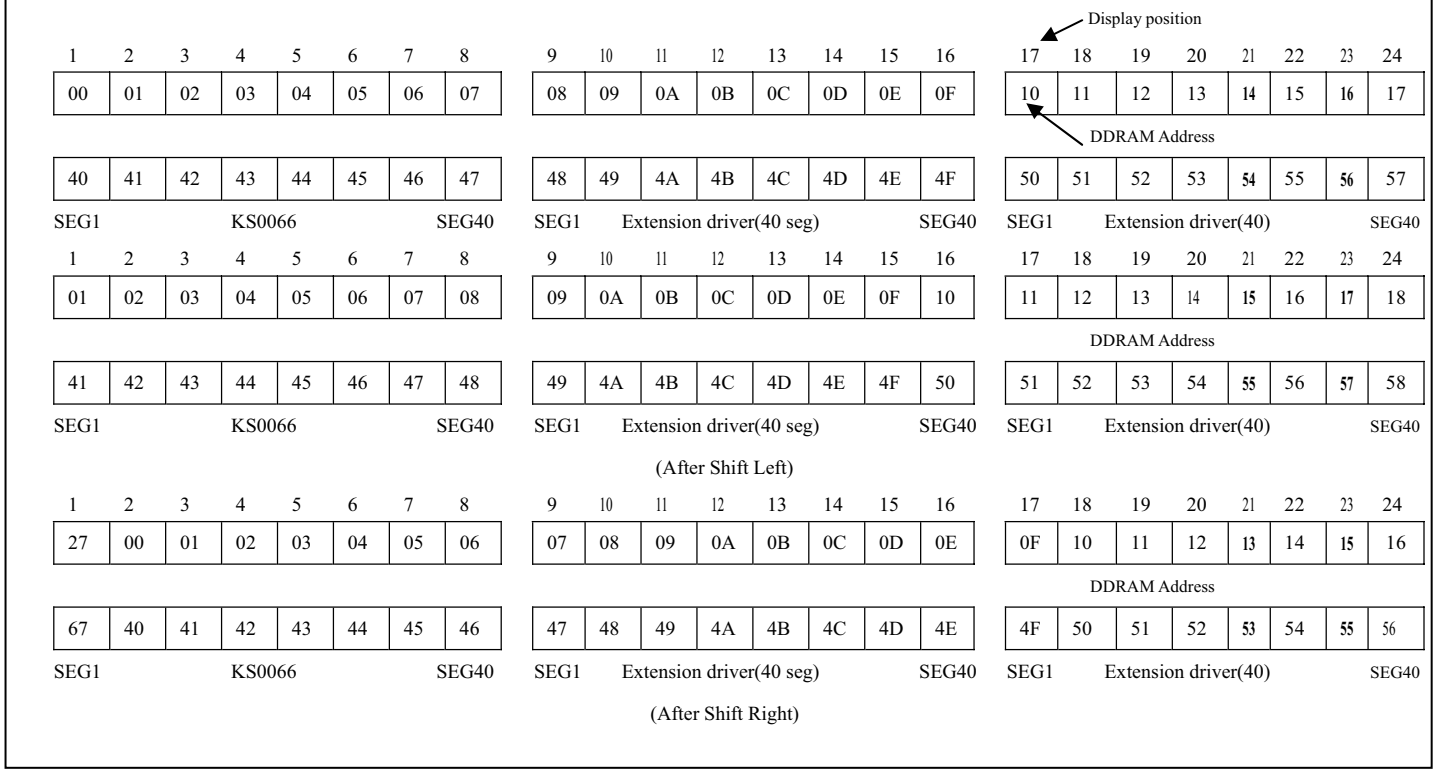
Figure 5. 1-line x 24ch. Display with 40 SEG. Extension Driver



2) 2-line Display

In the case of a 2-line display, the address range of DDRAM is 00H-27H and 40H-67H.An Extension driver will be used. Figure 6 shows the example a 40-segment extension Driver is added.

Figure 6. 2-line x 24ch. Display with 40 SEG. Extension Driver



6.5 Character generator ROM (CG ROM)

The relationship between character codes and Character Patterns

	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)														
LLLH	(2)														
LLHL	(3)														
LLHH	(4)														
LHLL	(5)														
LHLH	(6)														
LHHL	(7)														
LHHH	(8)														
HLLL	(1)														
HLLH	(2)														
HLHL	(3)														
HLHH	(4)														
HHLL	(5)														
HHLH	(6)														
HHHL	(7)														
HHHH	(8)														

6.6 CGROM (Character Generator ROM)

CGROM has a 5 x 8 dots 204 characters pattern and a 5 x 10 dots 32 characters pattern. CGROM has 204 character patterns of 5 x 8 dots, and 32 character patterns of 5 x 11 dots.

6.7 CGRAM (Character Generator RAM)

CGRAM has up to 5 x 8 dot, 8 characters. By writing font data to CGRAM, user defined characters can be used (Refer to table 1).

Table 1. Relationship Between Character Code (DDRAM) and Character Pattern (CGROM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0	1	1	1	0	
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
				.						.								.				.
				.						.								.				.
				.						.								.				.
0	0	0	0	x	1	1	1	0	0	0	0	0	0	x	x	x	1	0	0	0	1	
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
									.		0	1	1		.		1	1	1	1	1	
									.		1	0	0		.		1	0	0	0	1	
									.		1	0	1		.		1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

" x " Don't care

6.8 Timing Generation Circuit

Timing generation circuit generates clock signals for the insternal operations.

6.9 LCD Driver Circuit

LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40 bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch, In case of 1-line display mnode, COM1-COM8 have 1/8

duty or COM1-COM11 have 1/11 duty, and in 2-line mode, COM1 – COM16 have 1/16 duty ratio.

6.10 Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF at cursor position.

7 INSTRUCTION DESCRIPTION

7.1 Outline

To overcome the speed difference between internal clock of KS0066 and MPU clock, KS0066 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 3) Instruction can be divided largely four kinds.

1) KS0066 function set instructions (set display methods, set data length, etc.)

2) Address set instructions to internal RAM.

3) Data transfer instructions with internal RAM.

4) Others.

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) is read “High”. Busy Flag check must precede the next instruction. When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the ‘E’ signal after the Busy Flag (DB7) goes to “Low”.

Contents

1) **Clear Display**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = “1”).

2) **Return Home**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	—

eturn Home is cursor return home instruction. Set DDRAM address to “00H” in the address cousor. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change

3) **Entry Mode Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)

When I/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when reading from or write to CGRAM.

SH: Shift of Entire Display

When DDRAM read (CGRAM read/write) operation or SH = “Low”, shirt of entire display is not performed. If SH= “High” and DDRAM write operation, shift of entire display is performed according to I/D value (I/D= “1”: shift left, I/D=“0”: shift right)

4) **Display ON/OFF Control**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF Control Bit

When D= “High”, entire display is turned on.

When D= “Low”, display is turned off, but display data is remained in DDRAM.

C: Cursor ON/OFF Control Bit

When C= “High”, cursor is turned on.

When C= “Low”, cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF Control Bit

When B= “High”, cursor blink is on, that performs alternate between all the high data and display character at the cursor position. When B= “Low”, blink is off.

5) **Display ON/OFF Control**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	—	—

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data (Refer to table 2). During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously in all the lines. When displayed data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.

Table 2. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	--	--

DL: Interface Data Length Control Bit

When DL= “High”, it means 8-bit bus mode with MPU.

When DL= “Low”, it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit

When N= “Low”, it means 1-line display mode.
When N= “High”, 2-line display mode is set.

F: Display Font Type Control Bit

When F= “Low”, 5 x 7 dots format display mode.
When F= “High”, 5 x 10 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU. When 1-line display mode (N=0), DDRAM address is from “00H” to “4FH”. In 2-line display mode (N=1), DDRAM address in the 1st line is from “00H” to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

10) Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read Data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to

transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction; it also transfer RAM data to output data register. After read operation, address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

Table 3. Instruction Table

Instruction	Instruction Code										Description instruction code	Execution time (fosc=270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM, and set DDRAM address to “00H” from AC.	1.53ms
Return home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted	1.53ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display	39us
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor(C), and blinking of cursor (B) on/off control bit.	39us
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	39us
Function set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL: 4-bit/8-bit), numbers of display line (N: 1-line/2-line), display font type (F:5x8dots/5x11dots)	39us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39us
Read busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

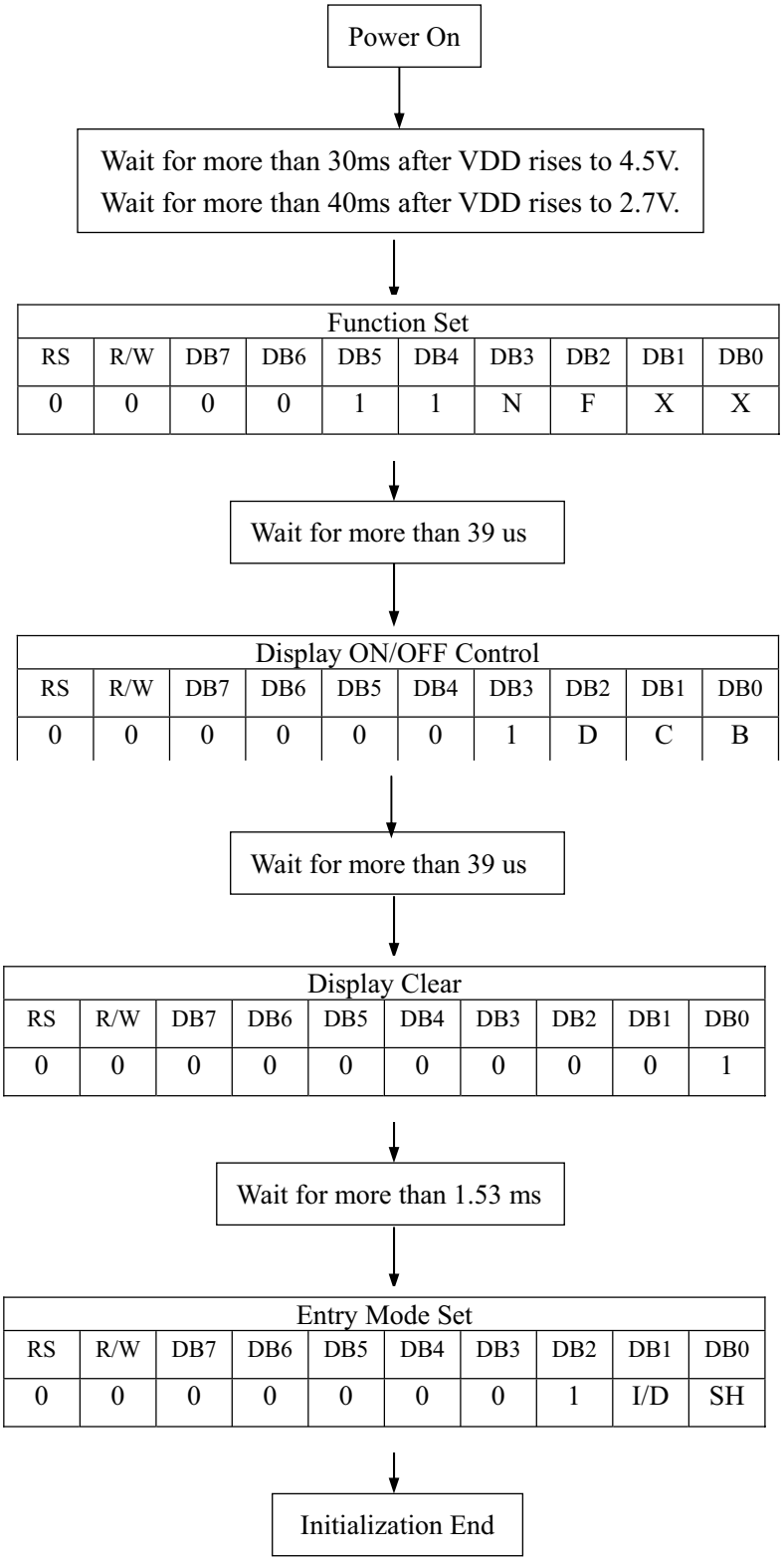
NOTE: When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc is necessary for executing the next instruction by the falling edge of the ‘E’ signal after the Busy Flag (DB7) goes to “Low”.

7.2 INITIALIZING BY INSTRUCTION

If the internal reset circuit doesn't operate correctly, initialization by instruction is required.

Use the following procedure for initialization.

1) **8-bit Interface Mode(Condition: fosc=270kHz)**



Condition: fosc=270kHz

N	0	1-line mode
	1	2-line mode

F	0	5X7 dots
	1	5X10 dots

D	0	Display off
	1	Display on

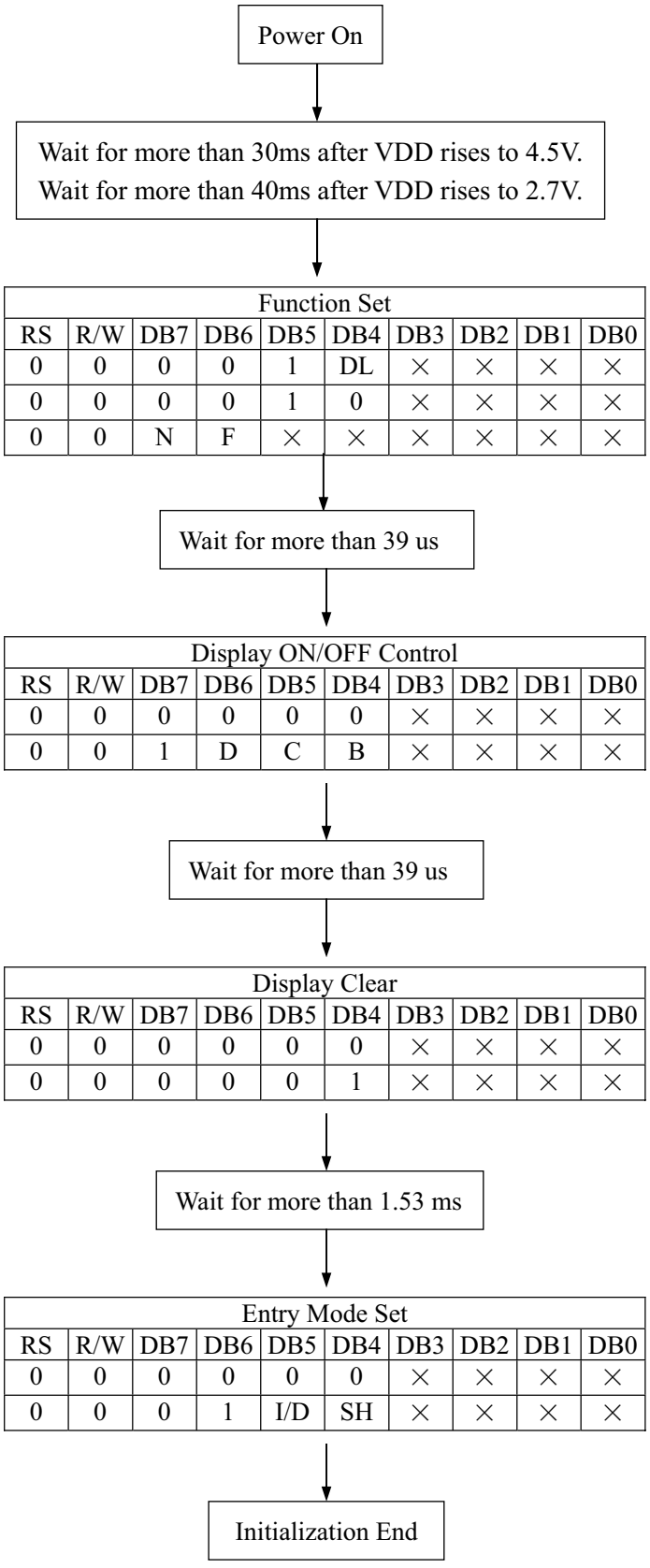
C	0	Cursor off
	1	Cursor on

B	0	Blink off
	1	Blink on

I/D	0	Decrement mode
	1	Increment mode

SH	0	Entire shift off
	1	Entire shift on

2) 4-bit Interface Mode(Condition: fosc=270kHz)



Condition: fosc=270kHz

DL	0	4-bit mode
	1	8-bit mode
N	0	1-line mode
	1	2-line mode
F	0	5X7 dots
	1	5X10 dots
D	0	Display off
	1	Display on
C	0	Cursor off
	1	Cursor on
B	0	Blink off
	1	Blink on
I/D	0	Decrement mode
	1	Increment mode
SH	0	Entire shift off
	1	Entire shift on

8 QUALITY AND RELIABILITY

8.1 Test condition

Test should be conducted under the following conditions:

Ambient temperature: 25 ± 5 ℃

Humidity : 60 ± 20% RH

8.2 Sampling plan

Sampling method shall be in accordance with DW1602M, inspection level Ⅱ, normal inspection, and single sampling plan tables for normal tightened, and reduced inspection.

8.3 Acceptable quality level

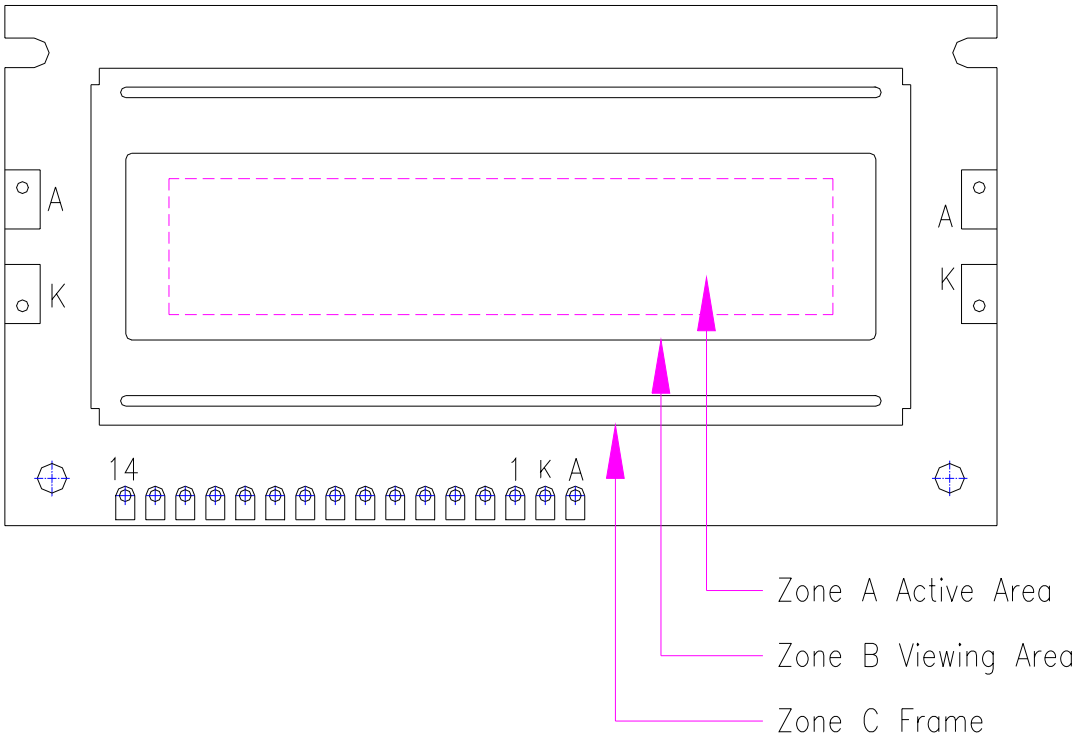
A major defect is a defect that could result in failure or materially reduce that the usability of the unit of product for its intended purpose.

A minor defect is one that does not materially reduce the usability of the unit of product for its intended purpose or is a departure from established standards having no significant bearing on the effective use or operation of the unit.

8.4 Appearance

Appearance test is to be conducted by human eyes at approximately 30cm distance from LCD module under the single fluorescent light.

The inspection area of LCD panel shall be within the range. Of following limits.



8.5 Inspection quality criteria

ITME	DESCRIPTION OF DEFECTS			Class of defects	Acceptable level (%)
FUNCTION	Short circuit or Pattern cut			Major	0.65
DIMENSION	Refer to individual acceptance specification			Major	2.5
BLACK SPOTS	Ave. Dia. D	area A	area B	Minor	2.5
	D≤0.2	Disregard			
	0.2<D≤0.3	2	3		
	0.3<D≤0.4	0	1		
	0.4<D	0	0		
BLACK LINES	Width W, Length L	A	B	Minor	2.5
	W≤0.03	disregard			
	0.03<W≤0.05	3	4		
	0.05<W≤0.07, L≤3.0	1	1		
BUBBLES IN POLARIZER	Average diameter D 0.2 < D < 0.5mm for N = 4 0.5 < D < 0.7mm for N=1			Minor	2.5
COLOR UNIFORMITY	Rainbow color or Newton ring.			Minor	2.5
GLASS SCRATCHES	Obvious visible damage.			Minor	2.5
VIEWING ANGLE	Refer to individual acceptance specification			Minor	2.5
CONTRAST RATIO	Refer to individual acceptance specification			Minor	2.5
RESPONSE TIME	Refer to individual acceptance specification			Minor	2.5

8.6 Reliability

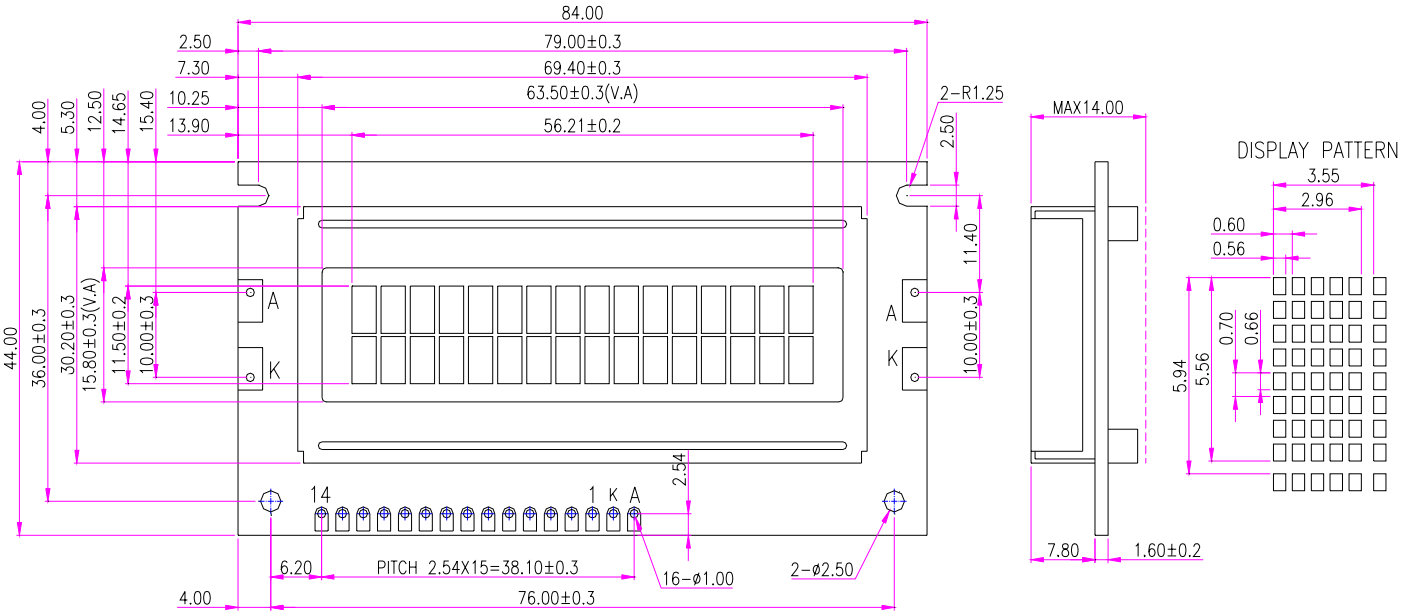
The LCD module should have no failure in the following reliability test.

TEST ITEM	TEST CONDITIONS	NOTE
HIGH TEMPERATURE STORAGE	80℃, 200hr.	Note
LOW TEMPERATURE STORAGE	-30℃, 200hr	Note
HUMIDITY STORAGE	60℃, 90%RH, 96hr.	Note
HIGH TEMPERATURE OPERATION	70℃, typical operating conditions, 200hr.	Note
LOW TEMPERATURE OPERATION	-20℃, typical operating conditions, 200hr.	Note
TEMPERATURE CYCLING	-30 ℃ ~80 ℃ 10min, between each step temp. 50min, at each step temp. 5 cycles.	Note
MECHANICAL VIBRATION	10 ~ 100 Hz sweep, 4G, amp1 = 10mm(max) XYZ for 60min, each.	Note
MECHANICAL SHOCK	10 ~ 55Hz, 50G. XYZ for 1 time, each.	Note

NOTE 1: The module should not have condensation of water on the module.

NOTE 2: The module shelled be inspected after 1 hour storage in normal conditions (15~35℃, 45~65%RH).

9 OUTLINE DIMENSION



Unmarked Tolerance: ±0.5mm

Display Data Address

Character	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF

NOTES:

1. DISPLAY TYPE: STN/Y-G MODE, TRANSFLECTIVE/POSITIVE.
2. DRIVE: KS0066U
3. VIEWING DIRECTION: 6 O'CLOCK.
4. PIN CONNECTION:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	A	K
VSS	VDD	VO	RS	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	VLED	VLSS

5. OPERATING TEMP: -20~70℃.
6. STORAGE TEMP： -30℃~80℃.

10. OPERATING OPTION

10.1 Input signal Function

No.	Symbol	Function	Note
1	VSS	Ground (0V)	
2	VDD	Power Suply for Logic Circuit	
3	VO	Power Supply for Driving the LCD	
4	RS	Data/Instruction select	
5	R/W	Read/Write select	
6	E	Enable signal	
7~14	DB0~DB7	Data Bus Line	
A	VLED	Led Backlight(+)	4.1V
K	VLSS	Led Backlight(-)	0V

10.2 Block diagram