FORMIKE ELECTRONIC CO.,LTD

PRODUCT SPECIFICATION

TFT LCD MODULE

MODEL : KWH032ST03-F02 Version: 1.0

【 ◆ 】 Preliminary Specification
【　　】 Finally Specification

CUSTOMER'S APPROVAL	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWD	PD REVIEWD	PREPARED BY
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Prepared By :

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Http:// www.wandisplay.com

● This specification is subject to change without notice.Please contact FORMIKE or it's
representative before designing your product based on this specification.

Issued Date:Jan-31-2011

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1. Record of Revision

Version	Issued Date	Page	Content	Created or Modified by
1.0	2011.01.31	All	New Creation	Stephen

2. GENERAL DESCRIPTION

2.1 Description

KWH032ST03-F02 is a Transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver ICs, FPC, backlight unit and touch screen . The following table described the features of FORMIKE KWH032ST03-F02

2.2 Application

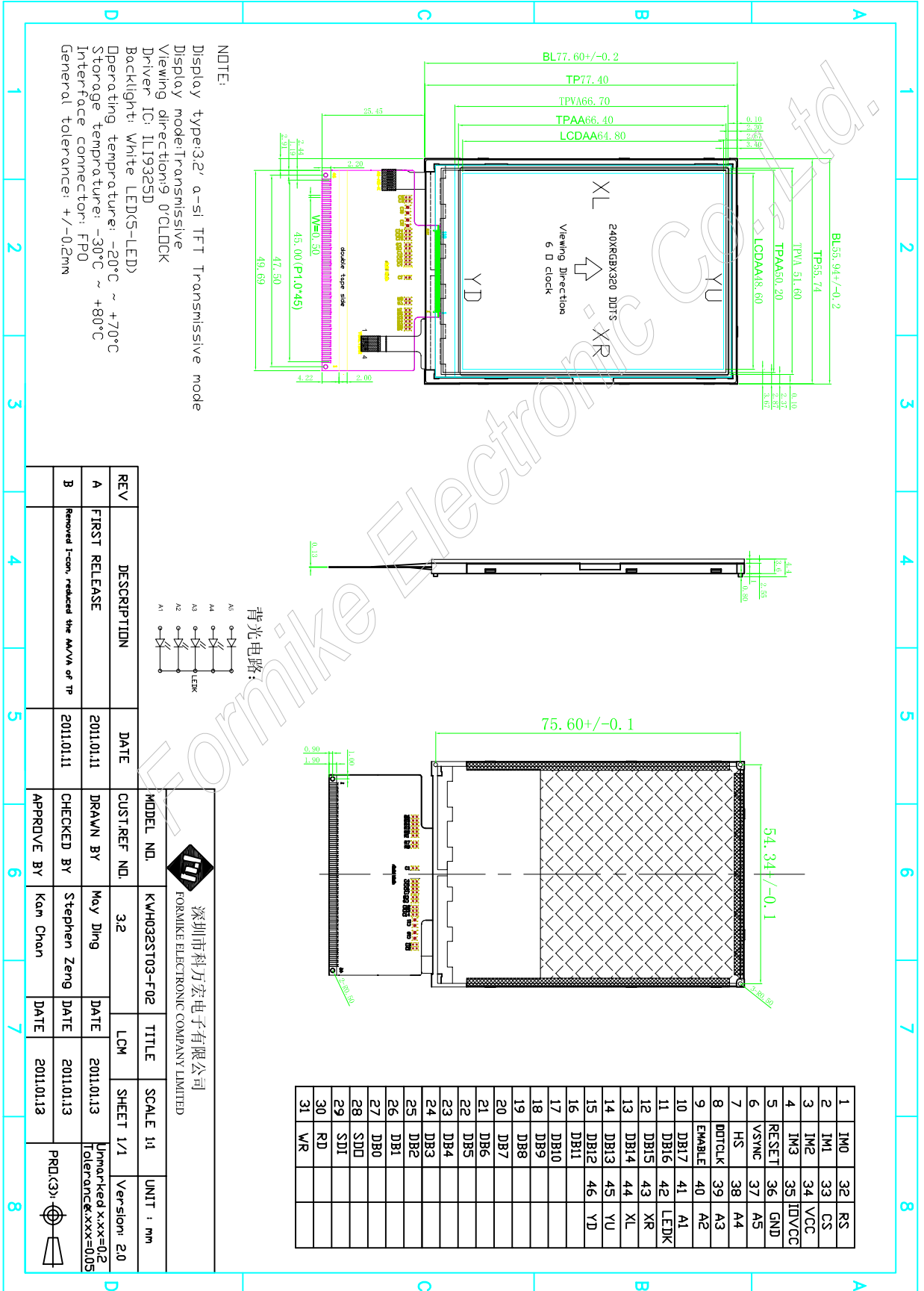Mobile phone, Multimedia products, instrument Device.
and other electronic Products
Etc.

2.3 Features

Feature	Description
Size	3.2 inchs (Diagonal)
Display Mode	Normally White, Transmissive
Resolution	240 (RGB) x 320
Display Format	R.G.B. vertical stripe
Color Depth	262K color
Inteface	MPU I/F(8/9/16/18 bit), RGB I/F (18bit)
Viewing Direction	9 O' clock
Technology Type	a-Si
Outline Dimension (W x H x D) (mm)	55.94 x77.6 x 3.6
Active Area(W x H mm)	48.6 x 64.8
Pixel pitch(mm)	0.2025 x 0.2025
With/Without TSP	With TSP
Weight (g)	TBD

3. Mechanical Drawing

NOTE:
Display type:3.2' a-si TFT Transmissive mode
Display mode:Transmissive
Viewing direction:9 0'CLOCK
Driver IC: ILI9325D
Backlight: White LEDS(5-LED)
Operating temprature: -20°C ~ +70°C
Storage temprature: -30°C ~ +80°C
Interface connector: FP0
General tolerance: +/-0.2mm

REV	DESCRIPTION	DATE
A	FIRST RELEASE	2011.01.11
B	Removed I-con, reduced the AA/VA of TP	2011.01.11

MODEL NO.	KWH032ST03-F02	TITLE	LCM	
CUST.REF NO.	3.2	SCALE 1:1	UNIT : mm	
DRAWN BY	May Ding	DATE	2011.01.13	
CHECKED BY	Stephen Zeng	DATE	2011.01.13	
APPROVE BY	Kam Chan	DATE	2011.01.13	

深圳市科力万宏电子有限公司
FORMIKE ELECTRONIC COMPANY LIMITED

Version: 2.0
Unmarked x.xx=0.2 Tolerance x.xxx=0.05
PRO(3):

1	IM0	32	RS
2	IM1	33	CS
3	IM2	34	VCC
4	IM3	35	IOVCC
5	RESET	36	GND
6	VSYNC	37	A5
7	HS	38	A4
8	DOTCLK	39	A3
9	ENABLE	40	A2
10	DB17	41	A1
11	DB16	42	LEDK
12	DB15	43	XR
13	DB14	44	XL
14	DB13	45	YU
15	DB12	46	YD
16	DB11		
17	DB10		
18	DB9		
19	DB8		
20	DB7		
21	DB6		
22	DB5		
23	DB4		
24	DB3		
25	DB2		
26	DB1		
27	DB0		
28	SDO		
29	SDI		
30	RD		
31	WR		

4. Pin Assignment

Pin NO.	Symbol	Description
1	IM0	Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code. Please refer to **Note 1** for detail information
2	IM1	
3	IM2	
4	IM3	
5	RESET	RESET pin. This is an active low signal.
6	VSYNC	In external interface mode, served as a vertical synchronize signal input. **Must connect to the GND level when not in use.**
7	HSYSC	In external interface mode, served as a horizontal synchronized signal input. **Must connect to the GND level when not used.**
8	DOTCLK	In external interface mode, served as a dot clock signal. When DPL = "0": Input data on the rising edge of DOTCLK When DPL = "1": Input data on the falling edge of DOTCLK **It is fixed to the GND level when not in use.**
9	ENABLE	In external interface mode, polarity of ENABLE signal is synchronized with valid graphic data input. Low: Valid data on DB17-DB0 High: Invalid data on DB17-DB0 Moreover, setting EPL bit can change the polarity of the ENABLE signal. **Must connect to the GND or IOVCC level when not in use.**
10	DB17	Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
11	DB16	
12	DB15	
13	DB14	
14	DB13	

15	DB12	**Mode**	**Pin Assignment**
16	DB11	8-bit system interface	DB17-DB10
17	DB10	9-bit system interface	DB17-DB9
18	DB9	16-bit system interface	DB17-DB10, DB8-DB1
19	DB8	18-bit system interface	DB17-DB0
20	DB7	6-bit External (RGB) interface	DB17-DB12
21	DB6	16-bit External (RGB) interface	DB17-13, DB11-DB1
22	DB5	18-bit External (RGB) interface	DB17-DB0
23	DB4	**Must connect to the GND level when not in use.** Please refer to **Note2** for detail information.	
24	DB3		
25	DB2		
26	DB1		
27	DB0		
28	SDO	Series Data is the output on the rising edge of the SCL signal in SPI mode.	
29	SDI	Series Data is the input on the rising edge of the SCL signal in SPI mode. **Must connect to the GND or level when not in use.**	
30	RD	In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low. **Must connect to the GND or IOVCC level when not in use.**	
31	WR	(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low. (B) In SPI mode, served as a synchronizing clock signal.	

32	RS	Register select signal. Low: Index register or internal status is selected. High: Control register is selected. Must connect to the GND or IOVCC level when not used. This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
33	CS	Chip select signal. Low: the LCD module is accessible High: the LCD module is not accessible Must connect to the GND or level when not used. This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
34	VCC	Internal logic power: VCC = 2.5V ~3.3V. **VCC ≥ IOVCC**.
35	IOVCC	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0,VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. **VCC ≥IOVCC**.
36	GND	Power Ground
37	LED A5	Anode of backlight diode
38	LED A4	Anode of backlight diode
39	LED A3	Anode of backlight diode
40	LED A2	Anode of backlight diode
41	LED A1	Anode of backlight diode
42	LED K	Cathode of backlight diode
43	X1	Touch screen interface (Right)
44	X2	Touch screen interface (Left)
45	Y1	Touch screen interface (Top)
46	Y2	Touch screen interface (Bottom)

Select the MPU system interface mode

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO
0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDA, SCL, nCS
0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDA, SCL, nCS, RS (D/CX)
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	0	1	0	i80-system 18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.
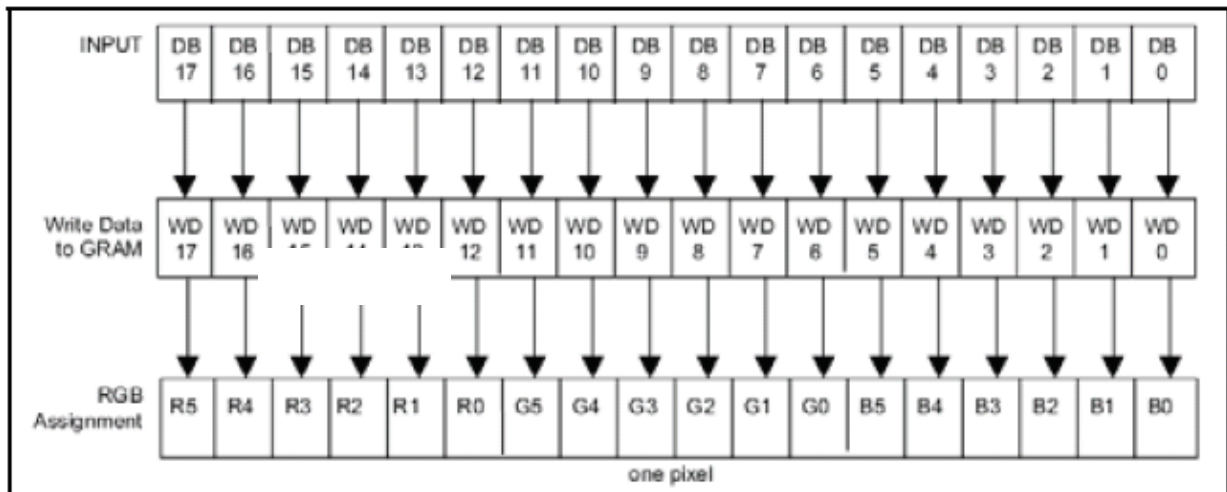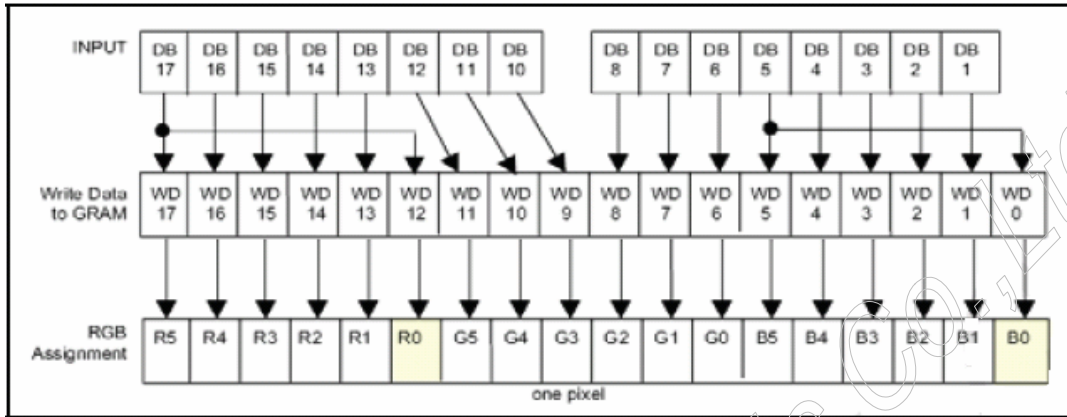

Figure 6-8 18-bit interface (262,144 colors)

Figure 6-9 16-bit interface (65,536 colors) TRIREG= 0
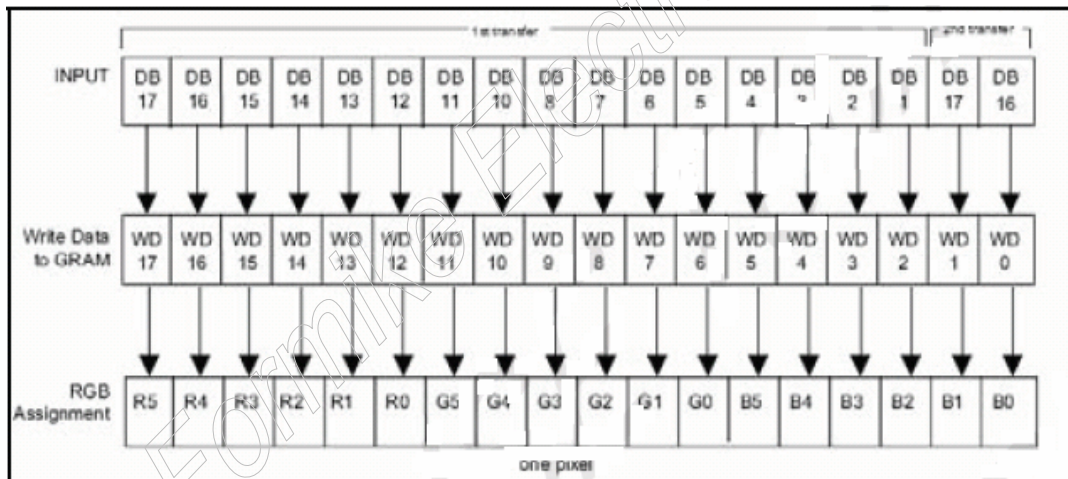

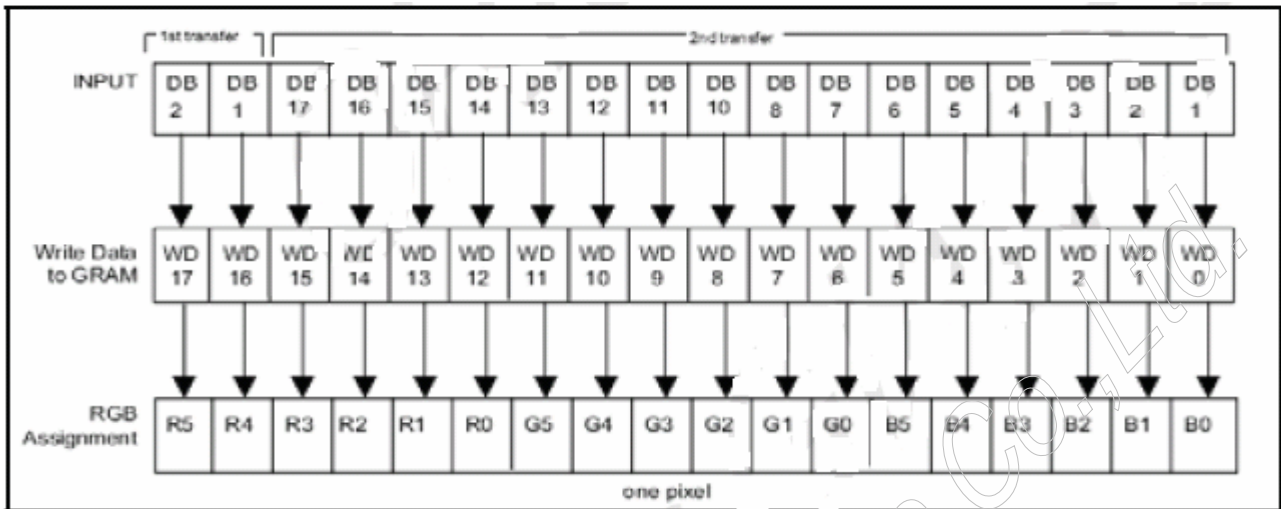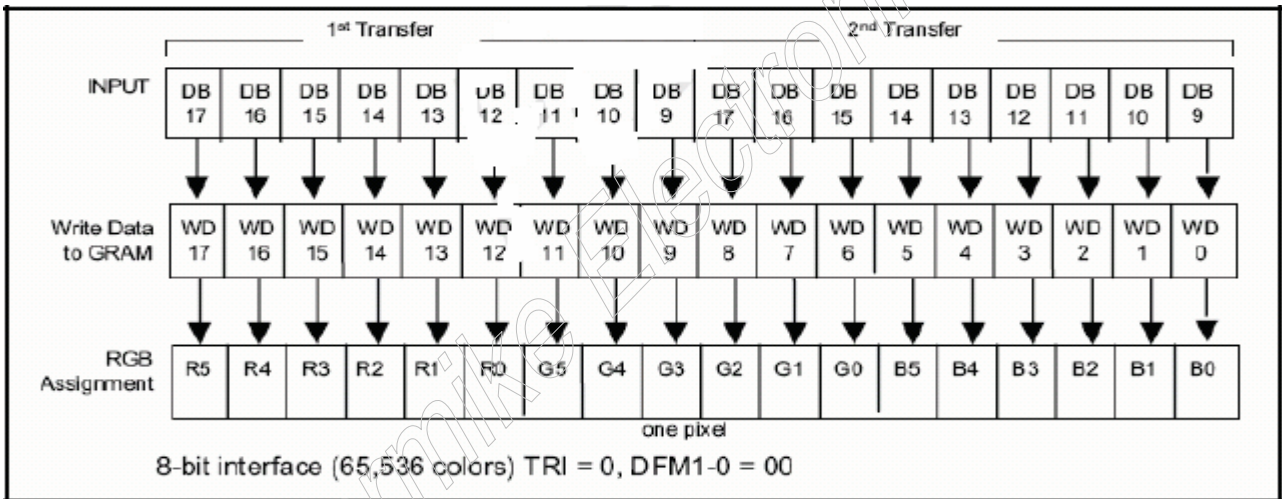**Figure 6-10** 16-bit interface (262,144 colors) TRIREG = 1, DFM = 0

Figure 6-11 16-bit interface (262,144 colors) TRIREG = 1, DFM = 1

8-bit interface (65,536 colors) TRI = 0, DFM1-0 = 00
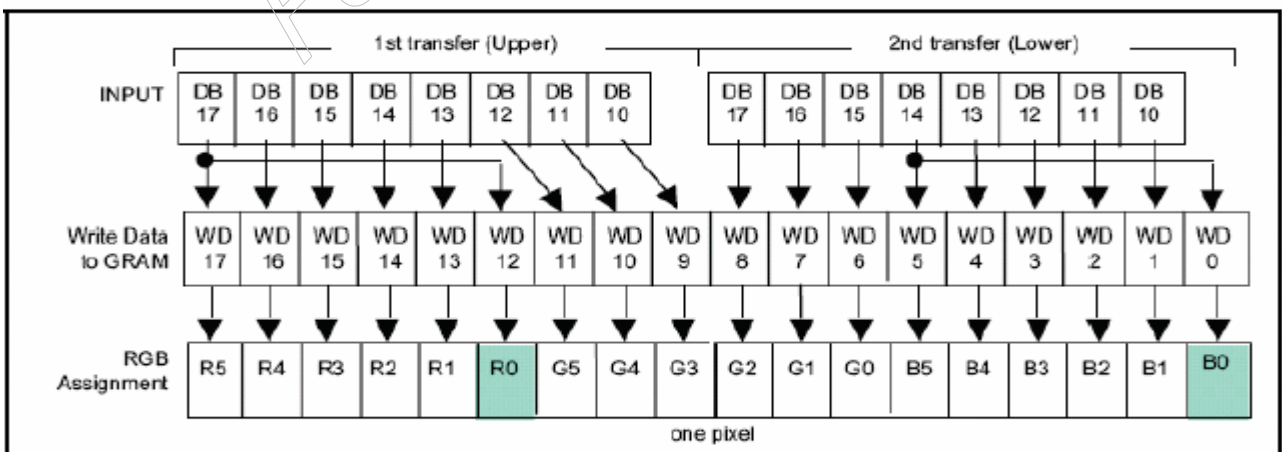
Figure 6-12 9-bit interface (262,144 colors)

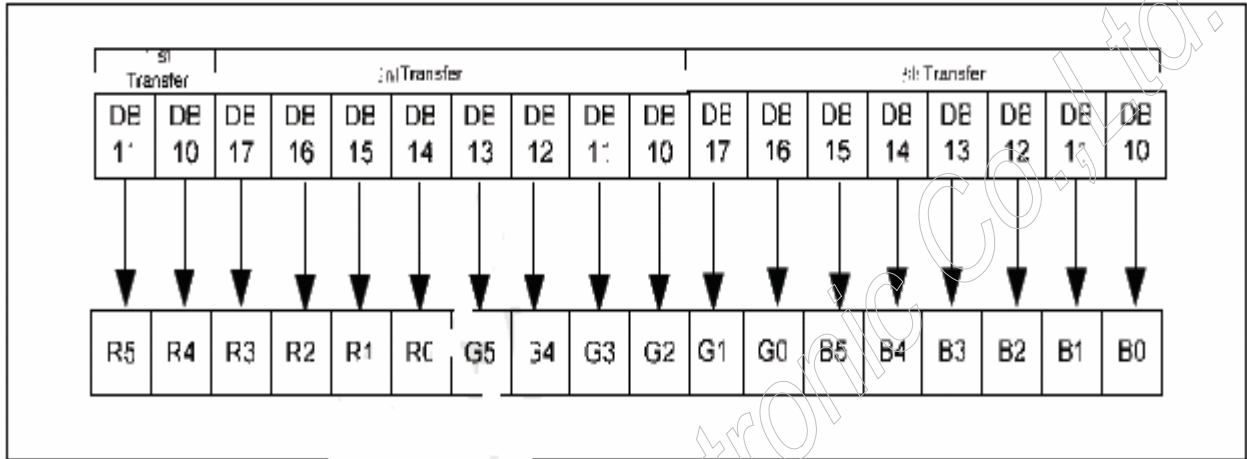**Figure 6-13** 8-bit interface (65,536 colors) TRIREG = 0

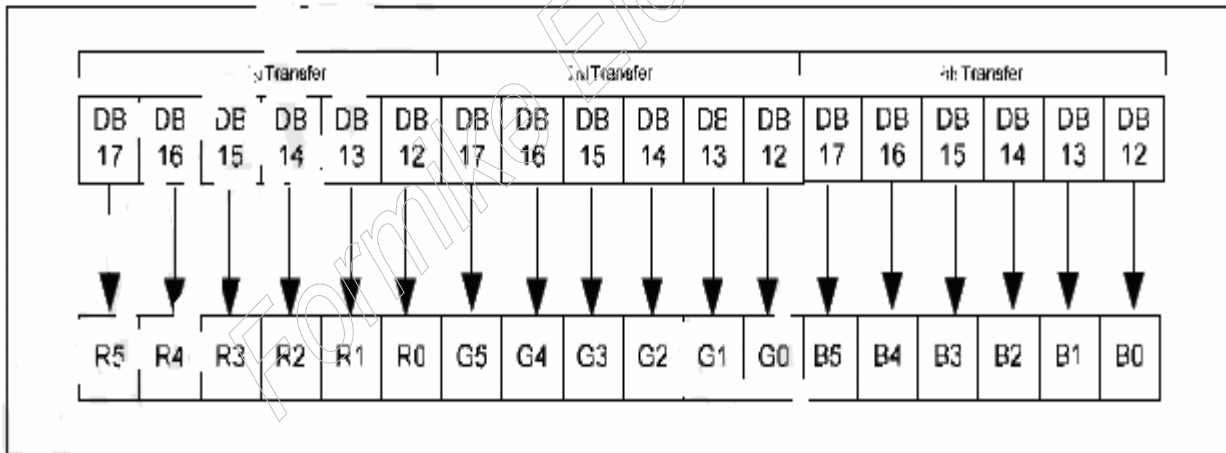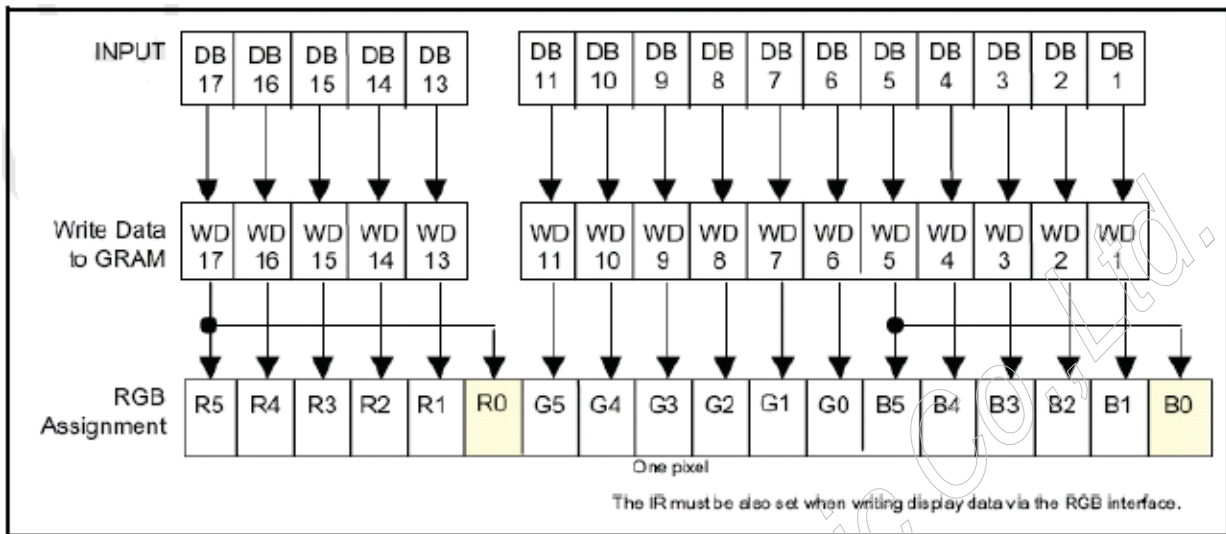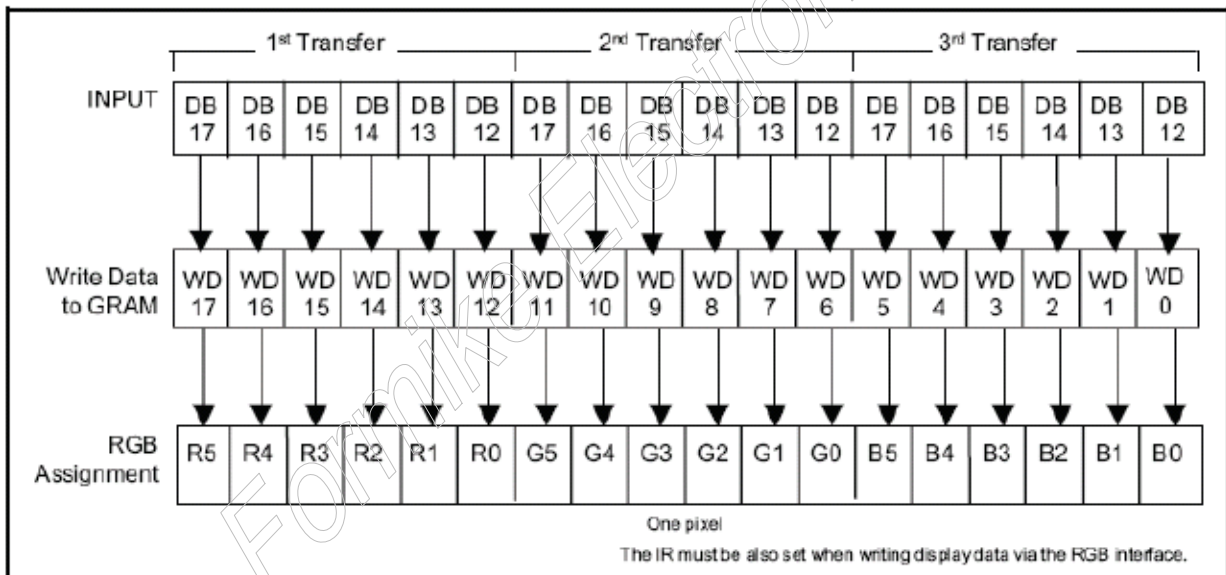**Figure 6-14** 8-bit interface 262 colors) TRIREG = 1, DFM=0.

Figure 6-15 8-bit interface (262K colors) TRIREG = 1, DFM=1

16-bit RGB interface (65,563 colors)

6-bit RGB interface (262,144 colors)

5. ELECTRICAL CHARACTERISTICS

5.1.LCM DC CHARACETRISTIC

Typical operating conditions   (GND=AVSS=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Power supply		VCC	2.5	-	3.3	V	
		IOVCC	1.65	-	3.3		
Driver Input signal voltage	H	V_{IH}	0.8*IOVCC	-	IOVCC	V	
	L	V_{IL}	GND	-	0.2*IOVCC	V	
Driver output signal voltage	H	V_{OH}	0.8*IOVCC	-	-	V	
	L	V_{OL}	-	-	0.2*IOVCC	V	
Power consumption		P_{LCD}	-	30	-	mW	*1

Note:

*1: Not include backlight.

5.2.BACKLIGHT CHARACETRISTIC

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power Consumption	P	288	330	450	mW	Backlight unit
LED Current	I_{LED}	18	20	25	mA	Single LED
LED Voltage	V_{LED}	3.2	3.3	3.6	V	Single LED
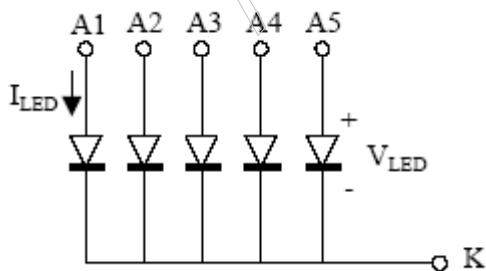
5.3.AC CHARACETRISTIC

A.80-system (18-bit / 16-bits) bus interface

Normal Write Mode (IOVCC = 1.65~3.3V)

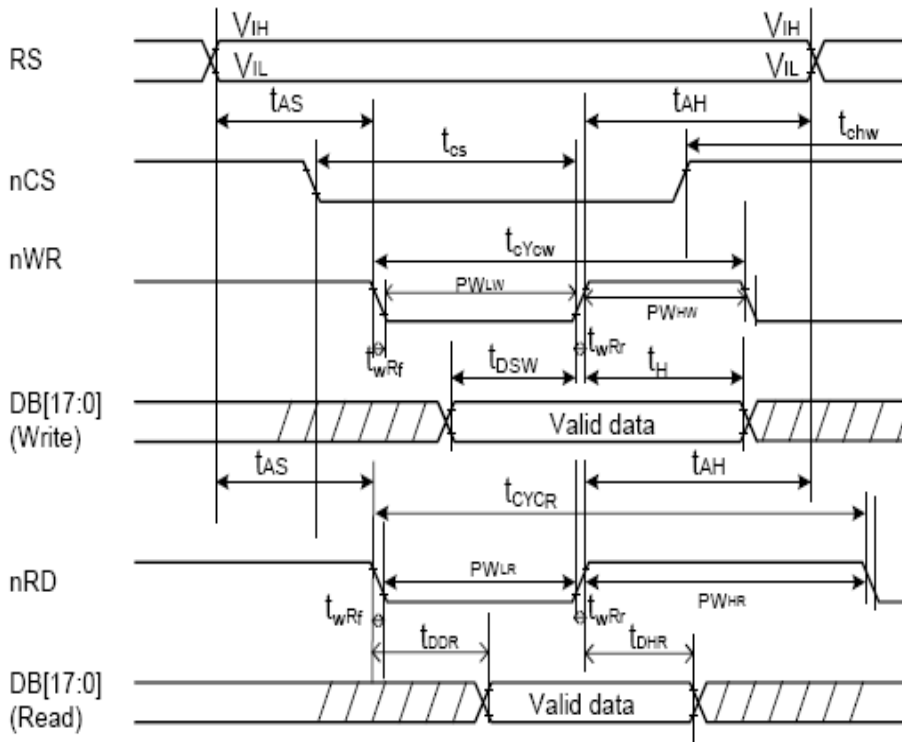| Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	TBD	-		-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	TBD	-	500	-
Write high-level pulse width		PW_{HW}	ns	TBD	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_H	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	

Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.65 ~ 3.3V)

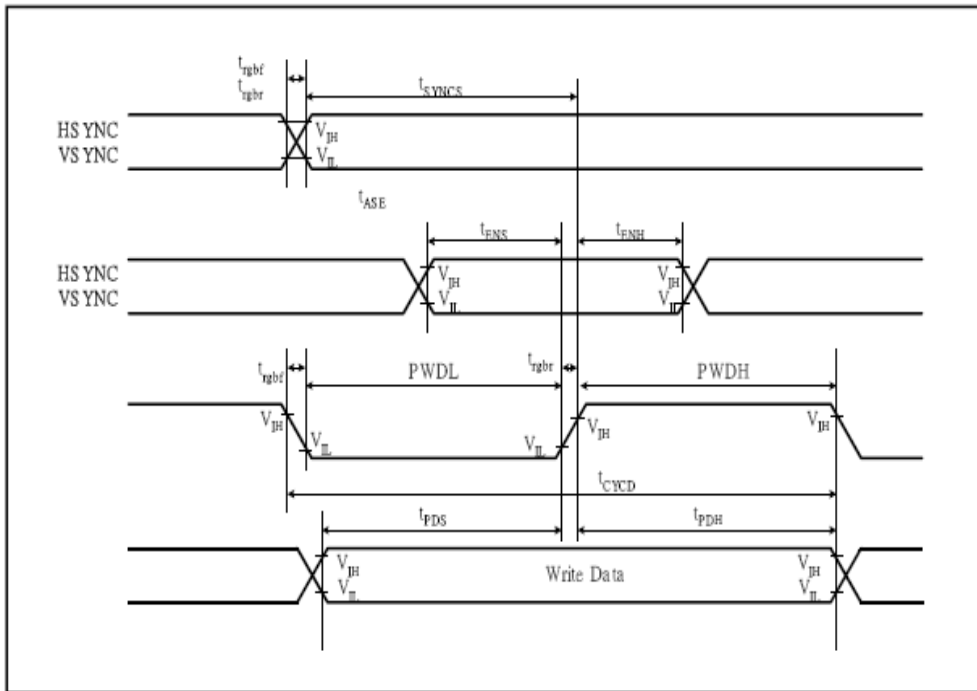| Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	μs	TBD	-	-	
	Read (transmitted)	t_{SCYC}	μs	200	-	-	
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	
	Read (transmitted)	t_{SCH}	ns	100	-	-	
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	
	Read (transmitted)	t_{SCL}	ns	100	-	-	
Serial clock rise / fall time		t_{SCr}, t_{SCf}	ns	-	-	5	
Chip select set up time		t_{CSU}	ns	10	-	-	
Chip select hold time		t_{CH}	ns	50	-	-	
Serial input data set up time		t_{SISU}	ns	20	-	-	
Serial input data hold time		t_{SIH}	ns	20	-	-	
Serial output data set up time		t_{SOD}	ns	-	-	100	
Serial output data hold time		t_{SOH}	ns	5	-	-	
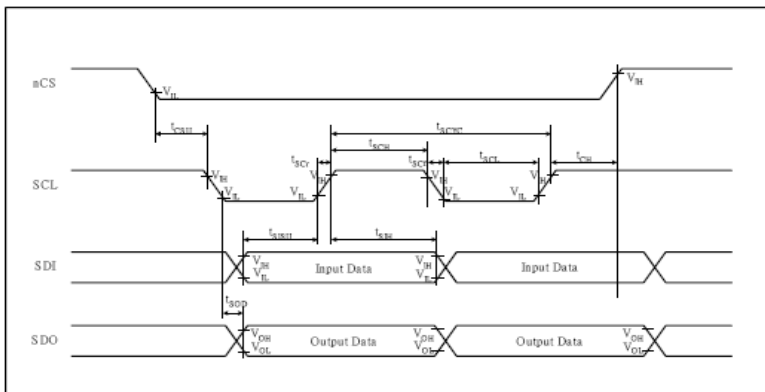
RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	TBD	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rgfr}, t_{rgff}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rgfr}, t_{rgff}	ns	-	-	25	-

6. ELECTRO-OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
Brightness		L	White pattern	160	200	-	cd/m^2	
Response time		T_R+T_F	$\Theta=\phi=0$	-	25	-	ms	Note 2
Contrast ratio		CR	At the center point of A.A.	300	350	-		
Color Chromaticity	White	W_x	$\Theta=\phi=0$	0.273	0.313	0.353		Note 2
		W_y		0.289	0.329	0.369		
Viewing Angle	Horizontal		CR 10	-	110	-	Degree	
	Vertical			-	120	-		

Note.1 These items are measured by C light.

Note.2 Definition of Viewing Angle(θ, ϕ),refer to Fig.1 as below：

Upper(+)

θ

ϕ

Left(-)

Right(+)

Lower(-)
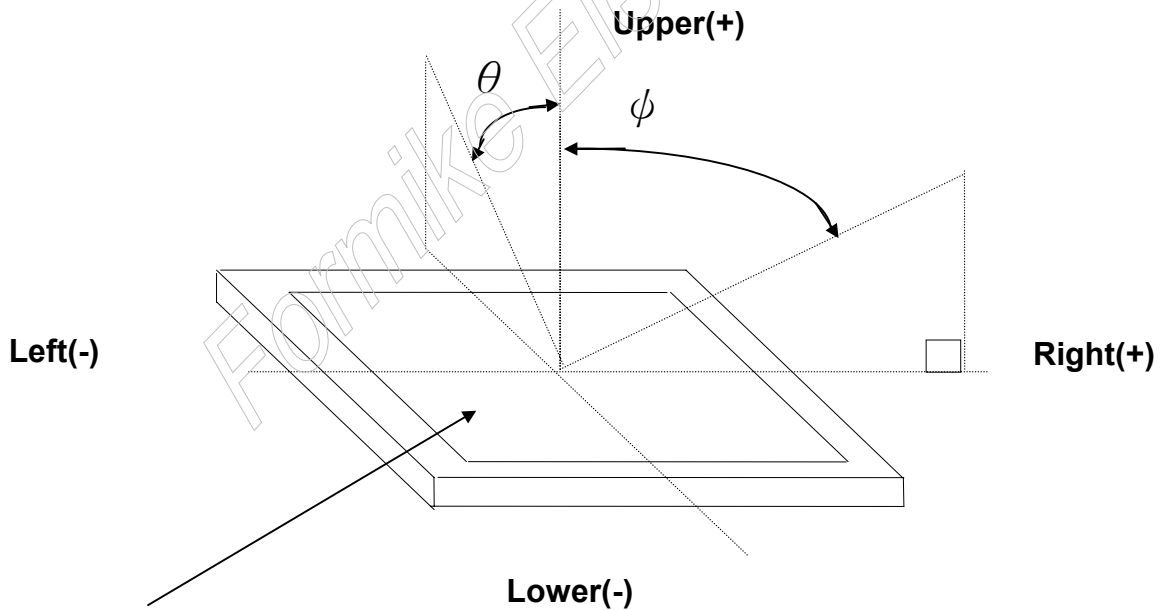
Ⅰ. **CF substrate**

Fig.1 Definition of Viewing Angle

7. MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Operation Temperature	T_{OP}	-20	70		
Storage Temperature	T_{ST}	-30	80		
Power supply voltage1	VCC, IOVCC	-0.3	+4.6	V	

8. RELIABILITY

8.1.MTTF

The LCD module shall be designed to meet a minimum MTTF value of 50,000 hours with normal condition. (25°C in the room without sunlight; not include life time of backlight).

8.2.Tests

NO.	ITEM	CONDITION	CRITERION
1	High Temperature Operating	70℃　　　　　240 hrs	◦No defect of Operational function in room temperature are allowable. ◦Leakage current should be below double of initial value.
2	Low Temperature Operating	-20℃　　　　　240 hrs	
3	High Temperature Non-Operating	80℃　　　　　240 hrs	
4	Low Temperature Non-Operating	-30℃　　　　　240 hrs	
5	High Temperature/ Humidity Non-Operating	50℃,90%RH　　240 hrs	
6	Temperature Shock Non-Operating	-30℃ ⟷ 80℃ (30min)　(5min)　(30min) 10 CYCLES	
7	Electro-static Discharge	HBM:　±2KV	

Note 1: Test after 24 hours in room temperature.
Note 2: The sampling above is individually for each reliability testing condition.
Note 3: The color fading of polarizing filter should not care.
Note 4: All of the reliability testing chamber above, is using D.I. water.(Min value:1.0 MΩ-cm)
Note 5: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

8.3.Color performance

No.	ITEM	Criterion (initial)
1	Luminance	>50%
2	NTSC	>70%
3	Contrast Ratio	>50%

9.PRECAUTIONS   FOR USE

9.1.Safety

(1) Do not swallow any liquid crystal,   even   if   there is no proof   that liquid   crystal is poisonous.

(2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.

(3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

9.2.Storage   Conditions

(1) Store the panel or module in a dark place where the temperature is 23±5℃   and the humidity is below 50±20%RH.

(2) Store in anti-static electricity container.

(3) Store in clean environment, free from dust, active gas, and solvent.

(4) Do not place the module near organics solvents or corrosive gases.

(5) Do not crush, shake, or jolt the module.

(6) Do not exposed to direct sun light of fluorescent lamps.

9.3.Installing LCD Module

Attend to the following items when installing the LCD Module.

(1) Cover the surface with a transparent protective plate or touch panel to protect the polarizer and LC cell.

(2) When assembling the LCD Module into other equipment, the spacer to the bit between the LCD Module and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm.

9.4.Precautions For Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (Vo). Adjust Vo to show the best contrast.

(2) Driving the LCD in the voltage above the limit will shorten its lifetime.

(3) Response time is greatly delayed at temperature below the   operating

temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) When turning the power on, input each signal after the positive/negative voltage becomes stable.

(5) Do not apply water or any liquid on product which composed of T/P.

9.5.Handling Precautions

(1) Avoid static electricity which can damage the CMOS LSI; please wear the wrist strap when handling.

(2) The polarizing plate of the display is very fragile. so, please handle it very carefully.

(3) Do not give external shock.

(4) Do not apply excessive force on the surface; it may cause display abnormal .

(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.

(7) Do not operate it above the absolute maximum rating.

(8) Do not remove the panel or frame from the module.

(9) Do not apply water or any liquid on product, which composed of T/P.

9.6.Warranty

(1) The period is within 12 months since the date of shipping out under normal using and storage conditions.

(2) The warranty will be avoided in case of defect induced by customer.