



FORMIKE ELECTRONIC CO.,LTD

PRODUCT SPECIFICATION

TFT LCD MODULE

MODEL : KWH028Q24-F02 Version: 1.0

- 【 ◆ 】 Preliminary Specification
【 】 Finally Specification

CUSTOMER'S APPROVAL	
SIGNATURE:	DATA:

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Revision record

VEV NO.	REV DATE	CONTENTS	Note
V1.0	2012-07-19	NEW ISSUE	

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1. General Description

1.1 Description

KWH028Q24-F02 is a Transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver IC, FPC, TP and backlight unit . The following table described the features of FORMIKE KWH028Q24-F02.

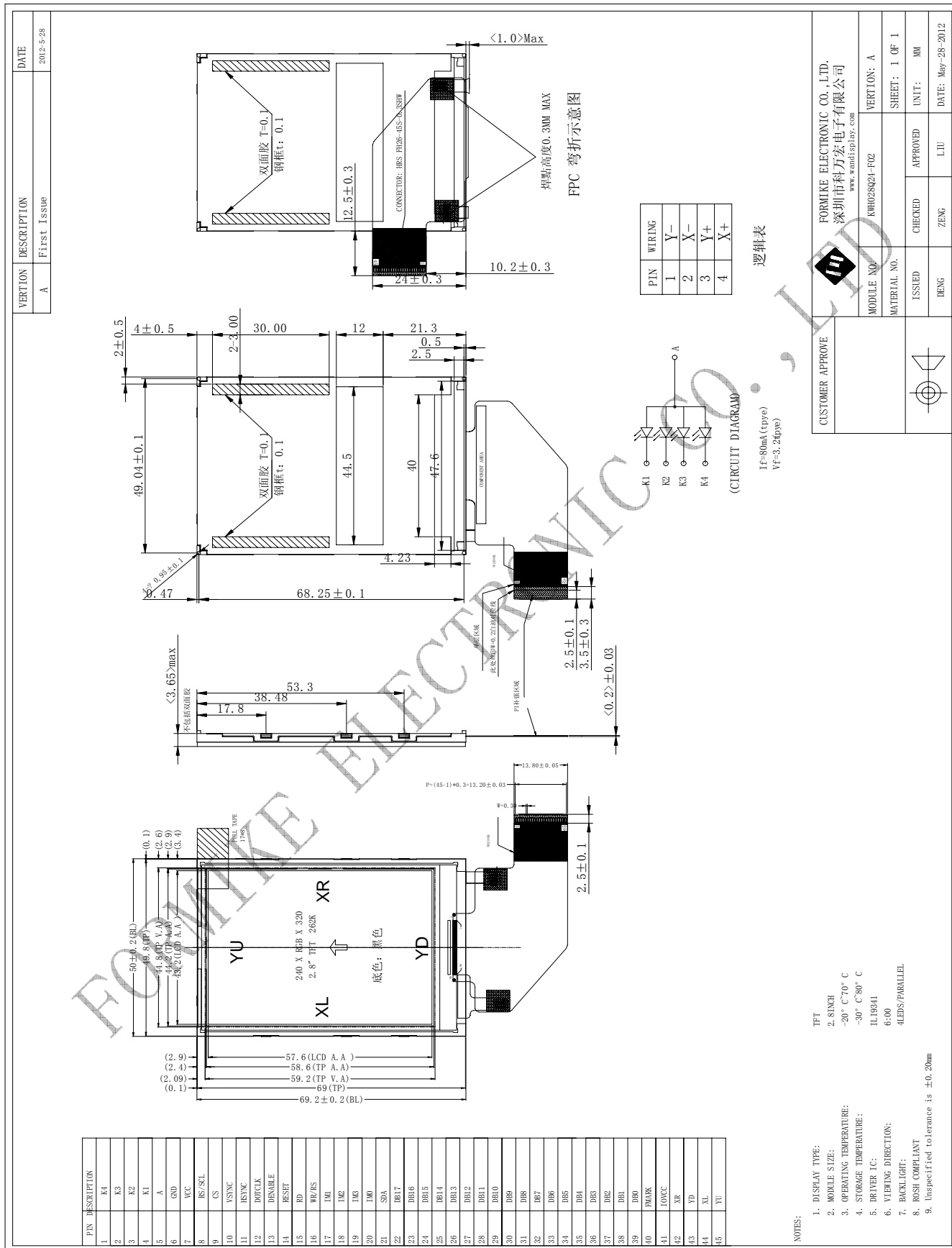
1.2 Application

Mobile phone, Multimedia products
 and other electronic Products
 Etc.

1.3 Features:

Features	Description	UNITS
LCD type	2.8" TFT	--
Dot arrangement	240 (RGB) × 320	dots
Driver IC	ILI9341	--
Color Depth	262K	--
Interface	RGB ,MCU,Serial Interface	--
View Direction	6 O'clock	--
Module size	50.0(W) × 69.2 (H) × 3.65(T)	mm
Active area	43.2(W) × 57.6(H)	mm
Dot pitch	0.18 (W) × 0.18 (H)	mm
Back Light	4 White LED In parallel	--
With/Without TSP	With TSP	--
Weight(g)	TBD	--

2. External Dimensions



3. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1-4	K4-K1	Power supply for LED backlight Cathode input
5	A	Power supply for LED backlight Anode input
6	GND	Ground.
7	VCC	Power supply (+2.3V~+3.3V).
8	RS/SCL	This pin is used to select "data or command" in the parallel interface or 4-wire 8-bit serial data interface. When RS="1", data is selected. When RS="0", command is selected. This pin is used serial interface clock in 3-wire 9-bit/4-wire 8-bit serial data interface. Fix to IOVCC or GND level when not in use.
9	CS	Chip select input pin(" low" enable).
10	VSYNC	Frame synchronizing signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
11	HSYNC	Line synchronizing signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
12	DOTCLK	Dot clock signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
13	ENABLE	Data enable signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
14	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
15	RD	8080-I/8080-II system(RD):Serves as a read signal and MCU read data at the rising edge. Fix to IOVCC level when not in use.
16	WR/RS	8080-I/8080-II system(WR):Serves as a write signal and writes data at the rising edge. 4-Line system(RS):Serves as command or parameter select. Fix to IOVCC level when not in use.
17	IM1	The selection of the given interfaces are done by external IM[3:0] Pins and shown as below Note 1.
18	IM2	
19	IM3	
20	IM0	
21	SDA	The data is applied on the rising edge of the SCL signal. Fix to IOVCC or GND level when not in use.
22-39	DB17-DB0	18-Bit parallel data bus for MCU system and RGB interface mode. Fix to GND level when not in use.
40	FMARK	Frame Synchronous Signal. If not used, please open this pin.
41	IOVCC	Power supply Voltage for I/O Interface (1.65V/3.3V).
42	XR	Touch Panel Right Side Wire.
43	YD	Touch Panel Down Side Wire.
44	XL	Touch Panel Left Side Wire.
45	YU	Touch Panel Up Side Wire.

NOTE 1:

ILI9341 provides four kinds of MCU system interface with 8080- I /8080- II series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,D/CX,SDO, CSX	

4. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9341 is used out of the absolute maximum ratings, ILI9341 may be permanently damaged. To use ILI9341 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9341 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.0
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	°C	-40 ~ +85
Storage temperature	Tstg	°C	-55 ~ +110

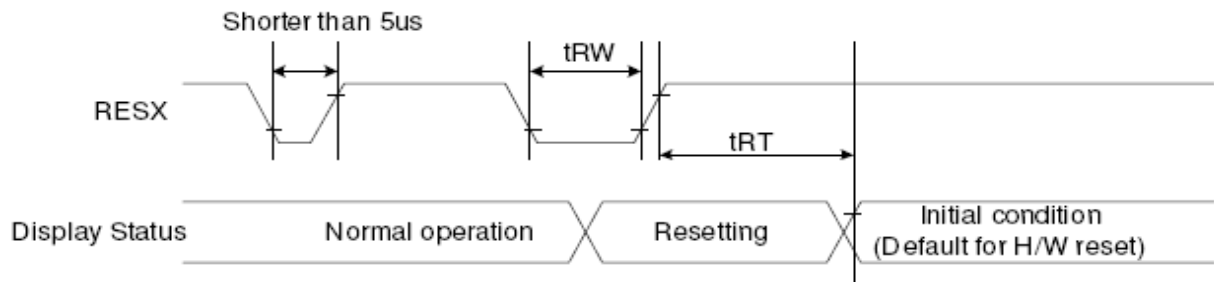
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5. Electrical Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-10.0	-	-5.0	Note3
Driver Supply Voltage	-	V	VGH-VGL	15	-	28	Note3
Current consumption during standby mode	I _{ST}	μA	VCI=2.8V , Ta=25 °C	-	-	100	-
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	μA	-	-	-	1	Note1,2,3
Logic Low Level input Current	IIL	μA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	μA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	VCOMH-VCOML	4.0	-	5.5	Note3
Source Driver							
Source Output Range	V _{sout}	V	-	0.1	-	DDVDH-0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3
Output Deviation Voltage (Source Output channel)	V _{dev}	mV	Sout>=4.2V Sout<=0.8V	-	-	20	Note4
Output Offset Voltage	VOFSET	mV	4.2V>Sout>0.8V	-	-	15	-
				-	-	35	Note7
Booster Operation							
1 st Booster (VCIx2) Voltage	DDVDH	V	-	4.95 (Note 5)	-	5.8 (Note 6)	Note3
1 st Booster (VCIx2) Drop Voltage	VCIx2 drop	%	loading=1mA	-	-	5	Note3
Liner Range	V _{liner}	V	-	0.2	-	DDVDH-0.2	

6. Timing Characteristics.

6.1 Reset Timing Characteristics.



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

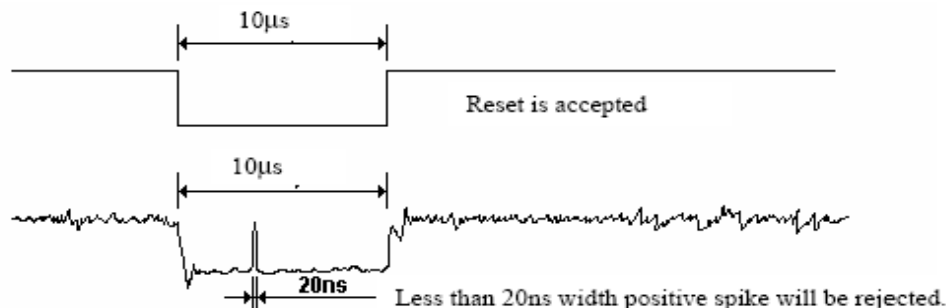
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



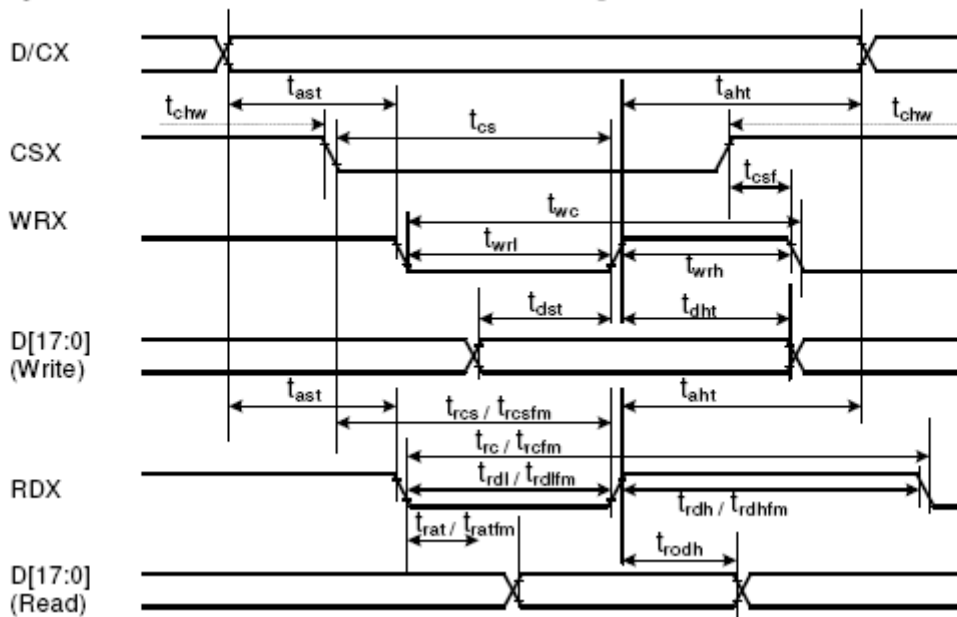
Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

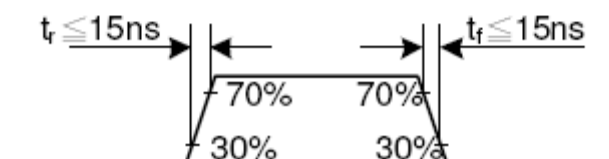
6.2. i80-System Interface Timing Characteristics.

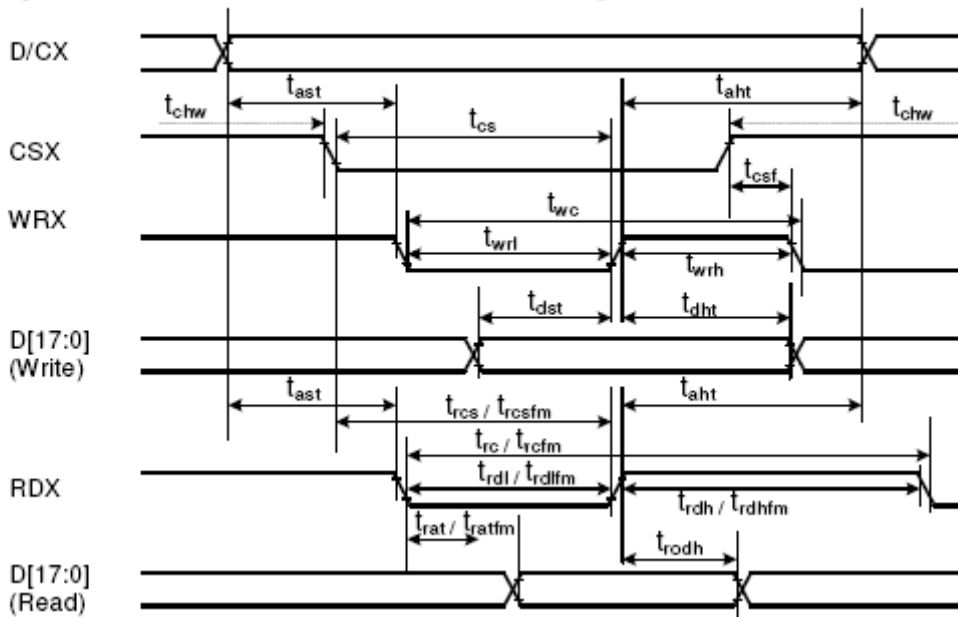
Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ah}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{rcfm}	Read Cycle (FM)	450	-	ns	
	t _{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rod}	Read output disable time	20	80	ns	

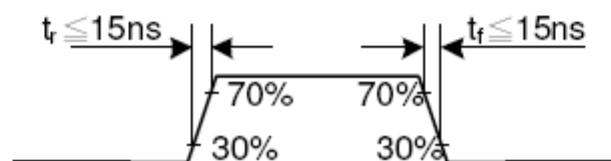
Note: $T_a = -30$ to 70 °C, $V_{DD1} = 1.65V$ to $3.3V$, $V_{CI} = 2.5V$ to $3.3V$, $V_{SS} = 0V$



Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080- II system)


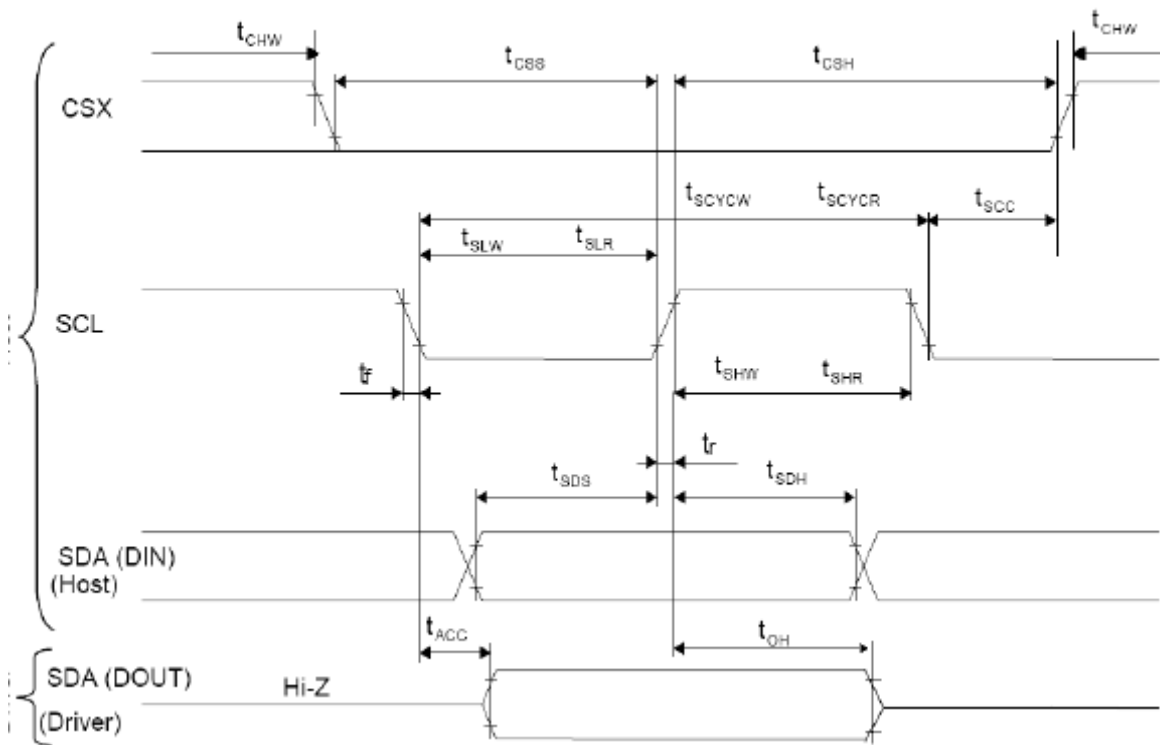
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ah}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{rcfm}	Read Cycle (FM)	450	-	ns	
	t _{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rod}	Read output disable time	20	80	ns	

Note: T_a = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.



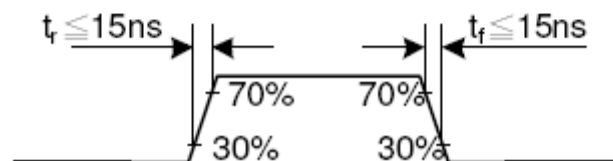
6.3. SPI Interface Timing Characteristics.

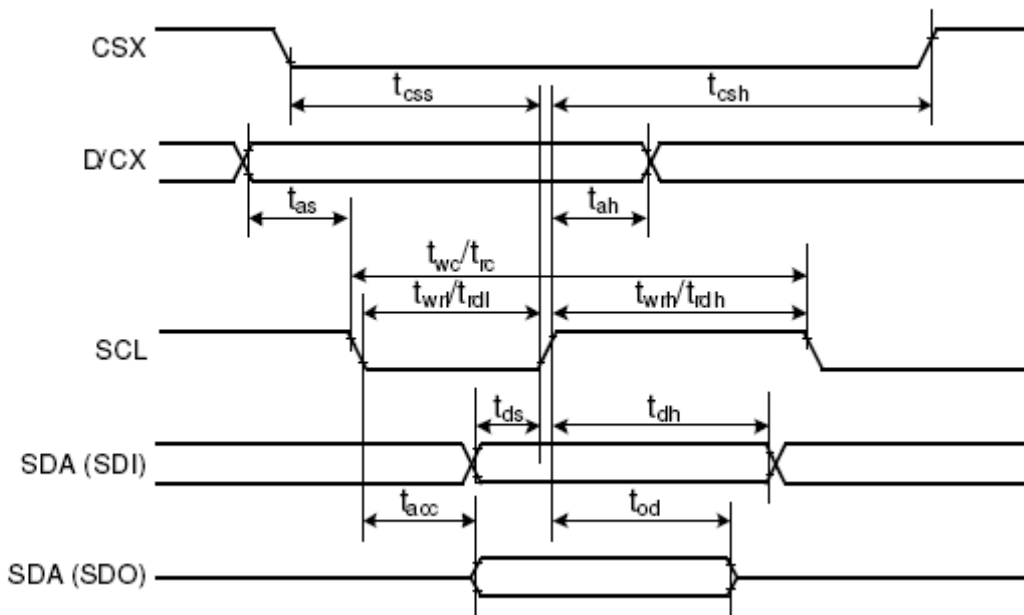
Display Serial Interface Timing Characteristics (3-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tchsh		65	-	ns	

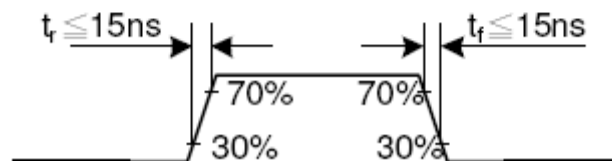
Note: $T_a = 25\text{ }^\circ\text{C}$, $V_{DDI} = 1.65\text{V to } 3.3\text{V}$, $V_{CI} = 2.5\text{V to } 3.3\text{V}$, $AGND = VSS = 0\text{V}$



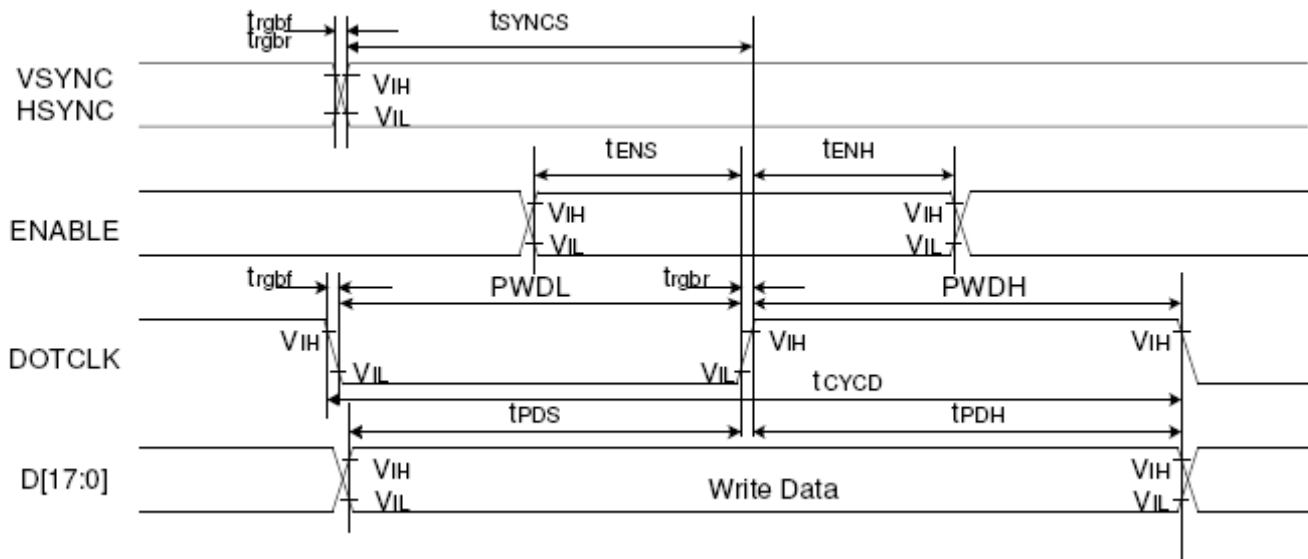
Display Serial Interface Timing Characteristics (4-line SPI system)


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	40	-	ns	
	t_{csh}	Chip select hold time (Read)	40	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	-	ns	
	t_{wrh}	SCL "H" pulse width (Write)	40	-	ns	
	t_{wrl}	SCL "L" pulse width (Write)	40	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL "H" pulse width (Read)	60	-	ns	
	t_{rdl}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-		
	t_{ah}	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	t_{ds}	Data setup time (Write)	30	-	ns	
	t_{dh}	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t_{acc}	Access time (Read)	10	-	ns	For maximum $C_L=30pF$
	t_{od}	Output disable time (Read)	10	50	ns	For minimum $C_L=8pF$

Note: $T_a = 25\text{ }^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$

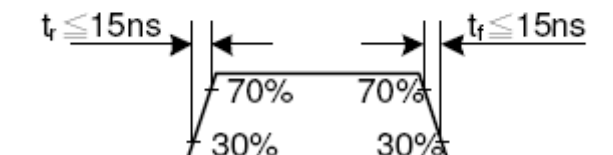


6.4. RGB Interface Timing Characteristics.

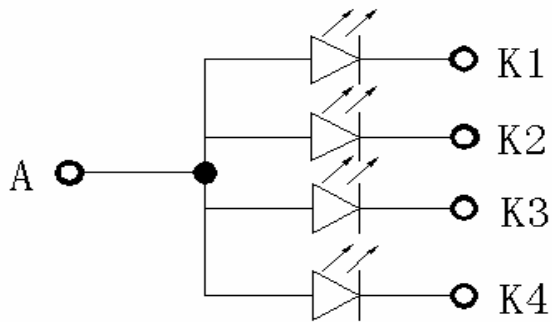


Signal	Symbol	Parameter	min	max	Unit	Description	
VSYNC / HSYNC	t_{SYNCs}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode	
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns		
DE	t_{ENS}	DE setup time	15	-	ns		
	t_{ENH}	DE hold time	15	-	ns		
D[17:0]	t_{POS}	Data setup time	15	-	ns		
	t_{PDH}	Data hold time	15	-	ns		
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns		
	PWDL	DOTCLK low-level period	15	-	ns		
	t_{CYCD}	DOTCLK cycle time	100	-	ns		
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns		
VSYNC / HSYNC	t_{SYNCs}	VSYNC/HSYNC setup time	15	-	ns		6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns		
DE	t_{ENS}	DE setup time	15	-	ns		
	t_{ENH}	DE hold time	15	-	ns		
D[17:0]	t_{POS}	Data setup time	15	-	ns		
	t_{PDH}	Data hold time	15	-	ns		
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns		
	PWDL	DOTCLK low-level pulse period	15	-	ns		
	t_{CYCD}	DOTCLK cycle time	100	-	ns		
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns		

Note: $T_a = -30$ to 70 °C, $V_{DDI} = 1.65V$ to $3.3V$, $V_{CI} = 2.5V$ to $3.3V$, $AGND = VSS = 0V$



7. Backlight Characteristics.



Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	V_f	3.0	3.2	3.4	V	I_f=60 mA	-
Supply Current	I_f	-	60	-	mA	-	-
Reverse Voltage	V_r	-	-	5	V	10uA	
Power dissipation	P_d	-	192	-	mW	-	
Luminous Intensity for LCM		-	280	-	Cd/m²	I_f=60 mA	
Uniformity for LCM	-	80	-	-	%	I_f=60 mA	
Life Time	-	50000	-	-	Hr	I_f=60 mA	-
Backlight Color	White						

8.Optical Characteristics

Item	Symbol	Conditions	Specifications	Unit	Note	
Transmittance	T%	Viewing normal angle $\theta_x = \theta_y = 0^\circ$	6.0	%	All left side data are based on CMO's following condition – 1.CG : NTSC 60% 2.LC : TN 3.Light Source : CMI LED BLU 4.Film : Nitto Linear Polarizer 5.Machine : DMS	
Contrast Ratio	CR		300	--		
Response Time (by Quick)	Ton+ Toff		30	ms		
Viewing Angle	Hor.	θ_{x+}	45	deg.		
		θ_{x-}	45			
	Ver.	θ_{y+}	45			
		θ_{y-}	20			
CF only Chromaticity	Red	X_R	0.635	--		Under C light Simulation
		Y_R	0.317	--		
	Green	X_G	0.298	--		
		Y_G	0.564	--		
	Blue	X_B	0.136	--		
		Y_B	0.116	--		
	White	X_W	0.298	--		
		Y_W	0.328	--		

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L63 / L0$$

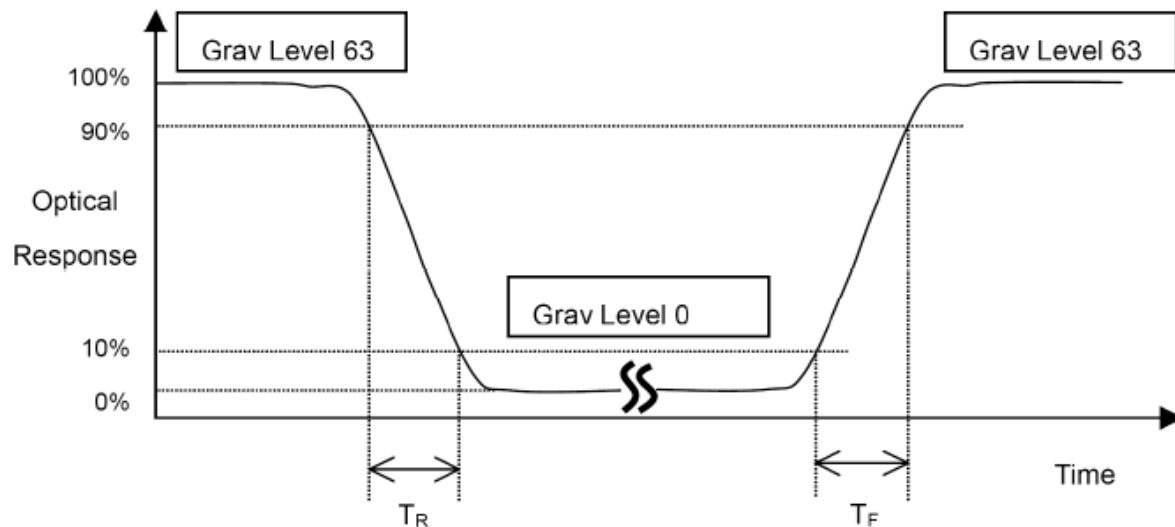
L63: Luminance of gray level 63

L0: Luminance of gray level 0

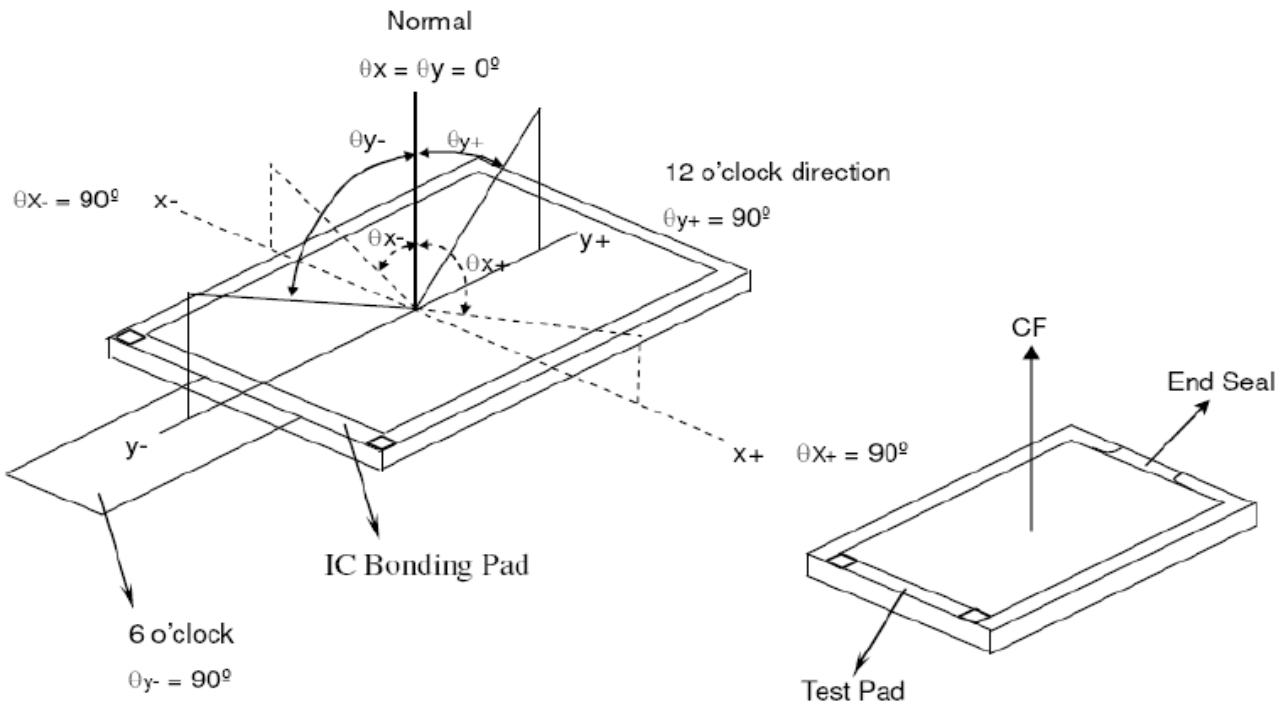
$$CR = CR (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

*Note (2) Definition of Response Time (TR, TF):



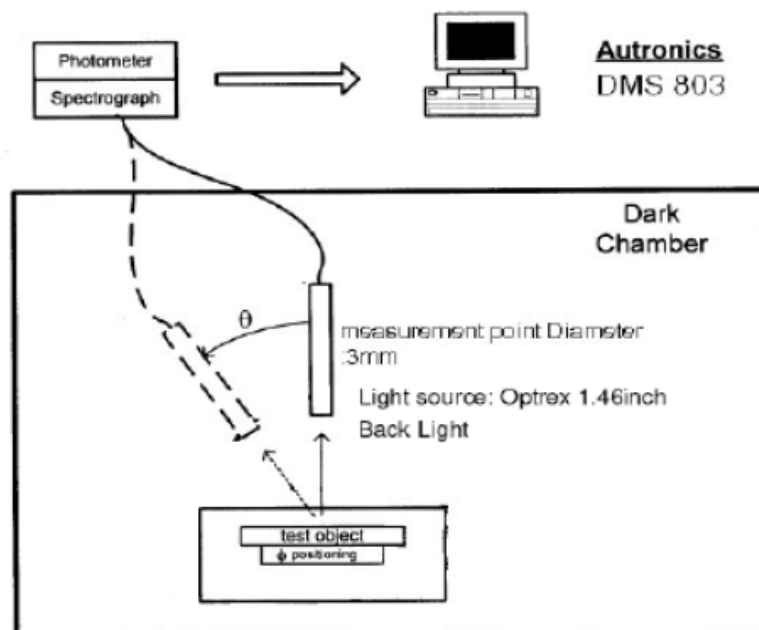
*Note(3) Definition of Viewing Angle



*** The above "Viewing Angle" is the measuring position with Largest Contrast Ratio; not for good image quality. View Direction for good image quality is 6 O'clock. Module maker can increase the "Viewing Angle" by applying Wide View Film.

*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



9. Reliability Test Conditions And Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
①	High Temperature Storage	80°C ± 2°C × 200Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1,Air bubble in the LCD. 2,Sealleak. 3,Non-display. 4,Missing segments. 5,Glass crack. 6,Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric Characteristics requirements shall be satisfied.
②	Low Temperature Storage	- 30°C ± 2°C × 200Hours	
③	High Temperature Operating	70°C ± 2°C × 120Hours	
④	Low Temperature Operating	- 20°C ± 2°C/120Hours	
⑤	Temperature Cycle(Storage)	- 30°C ± 2°C ↔ 25°C 80°C ± 2°C (30min) (5min) (30min) ←————→ 1cycle Total 10cycle	
⑥	Damp Proof Test	50°C ± 5°C × 90%RH × 120Hours	
⑦	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (Packing Condition)	
⑧	Drooping Test	Drop to the ground from 1M height one time every side of carton. (Packing Condition)	
⑨	ESD Test	Voltage: ± 8KV, R:330 Ω, C:150PF, Air Mode, 10times	

REMARK:

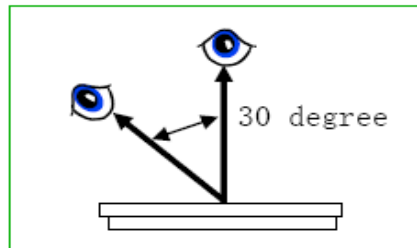
- 1,The Test samples should be applied to only one test item.
- 2,Sample side for each test item is 5~10pcs.
- 3,For Damp Proof Test,Pure water(Resistance>10MΩ) should be used.
- 4, In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
- 5,EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
- 6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Inspection Standard

This standard apply to TFT module specification.

1. Inspection condition:

Under daylight lamp 20~40W, product distance inspector'eye 30cm, incline degree 30° .



2. Inspection standard

NO.	Item	Inspection standard	Rate												
2.1	Dot	Case of Dot defect is below ① Bright Dot (whit spot) : "0" ② Dark Dot (black spot) : "0" (In case of Dark Dot on Main TFT LCD) - NG if there's full Dot defect. - Damaged less than the size of sub-pixel is not counted as defect - Dots darker than the size of sub-pixel are not defined as bright dot defect	minor												
		<table border="1"> <thead> <tr> <th>area size (mm)</th> <th>Acceptable number</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td>ignore</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.15$</td> <td>3</td> </tr> <tr> <td>$0.15 < \Phi \leq 0.20$</td> <td>2</td> </tr> <tr> <td>$0.25 < \Phi \leq 0.25$</td> <td>1</td> </tr> <tr> <td>$0.25 < \Phi$</td> <td>0</td> </tr> </tbody> </table>		area size (mm)	Acceptable number	$\Phi \leq 0.10$	ignore	$0.10 < \Phi \leq 0.15$	3	$0.15 < \Phi \leq 0.20$	2	$0.25 < \Phi \leq 0.25$	1	$0.25 < \Phi$	0
		area size (mm)		Acceptable number											
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<table border="1"> <thead> <tr> <th colspan="2">Size (mm)</th> <th>Acceptable number</th> </tr> </thead> <tbody> <tr> <td>ignore</td> <td>$W \leq 0.03$</td> <td>ignore</td> </tr> <tr> <td>$L \leq 4.0$</td> <td>$0.03 < W \leq 0.04$</td> <td>2</td> </tr> <tr> <td>$L \leq 4.0$</td> <td>$0.04 < W \leq 0.05$</td> <td>1</td> </tr> <tr> <td></td> <td>$0.05 < W$</td> <td>Treat with dot non-conformance</td> </tr> </tbody> </table>	Size (mm)		Acceptable number	ignore	$W \leq 0.03$	ignore	$L \leq 4.0$	$0.03 < W \leq 0.04$	2	$L \leq 4.0$	$0.04 < W \leq 0.05$	1		$0.05 < W$	Treat with dot non-conformance
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	$0.05 < W$	Treat with dot non-conformance													
2.2	line														

11. Handling Precautions

11.1 Mounting method

The LCD panel of FORMIKE ELECTRONIC CO.,LTD. module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

11.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

11.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to V_{dd} or V_{ss} , do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

11.4 packing

- Module employ LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

11.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit. Usage under the maximum operating temperature, 50%Rh or less is required.

11.6 storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
It is recommended to store them as they have been contained in the inner container at the time of delivery from us

11.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

12. Precaution For Use

12.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

12.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to FORMIKE ELECTRONIC CO.,LTD,and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.