FORMIKE ELECTRONIC CO.,LTD

PRODUCT SPECIFICATION

TFT LCD MODULE

MODEL : KWH028Q12-F02 Version: 1.0

【 ◆ 】 Preliminary Specification

【 】 Finally Specification

CUSTOMER'S APPROVAL	
SIGNATURE:	DATA:

Designed by	R&D Checked by	Quality Department by	Approved by
DENG			

Prepared By :

FORMIKE ELECTRONIC CO.,LTD

Address :Room 14H, HanKing Building, 23# DengLiang Road, NanShan District, ShenZhen, 518054, China.

TEL:(86) 755 88306921,88306931 FAX:(86) 755 88304615

Http:// www.wandisplay.com

● This specification is subject to change without notice. Please contact FORMIKE or it's representative before designing your product based on this specification.

Revision record

VEV NO.	REV DATE	CONTENTS	Note
V1.0	**2012-07-19**	**NEW ISSUE**	

Table Of Contents

1. General Description

1.1 Description

KWH028Q12-F02 is a Transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver IC, FPC, TP and backlight unit . The following table described the features of FORMIKE KWH028Q12-F02.

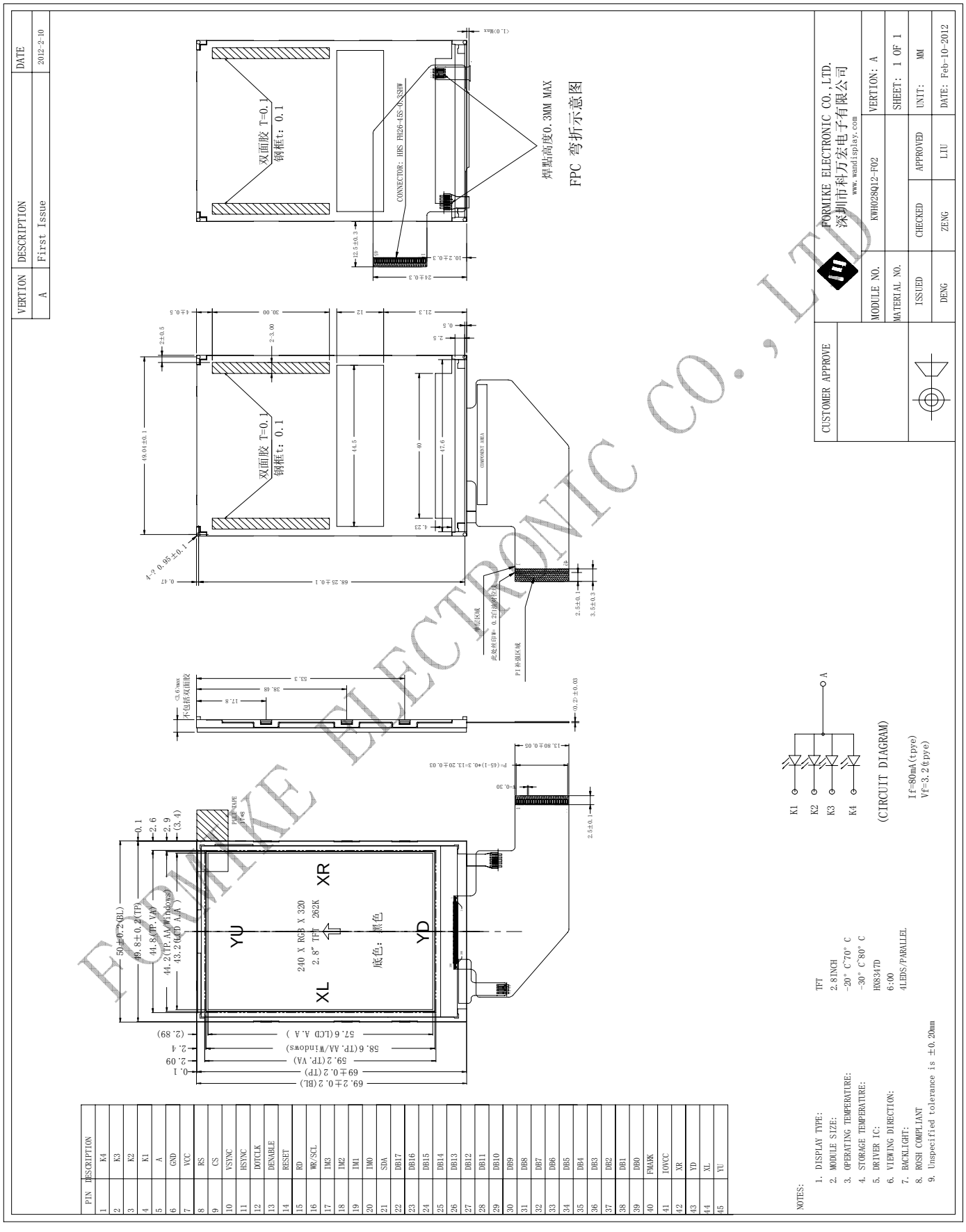
1.2 Application

Mobile phone, Multimedia products
and other electronic Products
Etc.

1.3 Features:

Features	Description	UNITS
LCD type	2.8"TFT	--
Dot arrangement	240（RGB）×320	dots
Driver IC	HX8347D	--
Color Depth	262K	
Interface	RGB ,MCU,Serial Interface	--
View Direction	6 O'clock	--
Module size	50.0(W) ×69.2 (H)×3.6(T)	mm
Active area	43.2(W) ×57.6(H)	mm
Dot pitch	0.18 (W) ×0.18 (H)	mm
Back Light	4 White LED In parallel	--
With/Without TSP	With TSP	
Weight(g)	TBD	

2. External Dimensions



3. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1-4	K4-K1	Power supply for LED backlight Cathode input
5	A	Power supply for LED backlight Anode input
6	GND	Ground.
7	VCC	Power supply (+2.3V~+3.3V).
8	RS	This pin is used to select ”data or command” in the parallel interface. When RS=”1”, data is selected. When RS=”0”, command is selected. Fix to IOVCC or GND level when not in use.
9	CS	Chip select input pin(“ low” enable).
10	VSYNC	Frame synchronizing signal for RGB interface operation. Fix to GND level when not in use.
11	HSYNC	Line synchronizing signal for RGB interface operation. Fix to GND level when not in use.
12	DOTCLK	Dot clock signal for RGB interface operation. Fix to GND level when not in use.
13	ENABLE	Data enable signal for RGB interface operation. Fix to GND level when not in use.
14	RESET	Reset input pin, When reset is “L”, Initialization is executed.
15	RD	Read enable pin I80 parallel bus system interface. Fix to IOVCC or GND level when not in use.
16	WR/SCL	Write enable pin I80 parallel bus system interface. (SCL)server as serial data clock in serial bus system interface. Fix to IOVCC or GND level when not in use.
17	IM3	System interface select: NOTE 1
18	IM2	
19	IM1	
20	IM0	
21	SDA	Serial data input pin and output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. The unused pins let to open or connected to GND.
22-39	DB17-DB0	18-Bit parallel data bus for MCU system and RGB interface mode. The unused pins let to open or connected to GND.
40	FMARK	Frame Synchronous Signal. If not used, please open this pin.
41	IOVCC	Power supply Voltage for I/O Interface (1.65V/3.3V).
42	XR	Touch Panel Right Side Wire.
43	YD	Touch Panel Down Side Wire.
44	XL	Touch Panel Left Side Wire.
45	YU	Touch Panel Up Side Wire.

NOTE 1:

The system interface circuit in HX8347-D supports, 18-/16-/9-/8-bit bus width parallel bus system interface for I80 series CPU, and 4-/3-wire serial bus system interface for serial data input. When NCS = "L", the parallel and serial bus system interface of the HX8347-D become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the display data RAM. The input bus format of system interface circuit is selected by external pins setting. For selecting the input bus format, please refer to Table 5.1.

IM3	IM2	IM1	IM0	Interface	DNC SCL	NWR SCL	Data Bus use	
							Register/Content	GRAM
0	0	0	0	8080 MCU 16-bit parallel type I	DNC	NWR	D7-D0	D15-D0: 16-bit data
0	0	0	1	8080 MCU 8-bit parallel type I	DNC	NWR	D7-D0	D7-D0: 8-bit data
0	0	1	0	8080 MCU 16-bit parallel type II	DNC	NWR	D8-D1	D17-10, D8-D1: 16-bit data
0	0	1	1	8080 MCU 8-bit parallel type II	DNC	NWR	D17-D10	D17-D10: 8-bit data
0	1	0	ID	3-wire serial interface	-	SCL	SDA	
0	1	1	-	4-wire serial interface	DNC	SCL	SDA	
1	0	0	0	8080 MCU 18-bit parallel type I	DNC	NWR	D7-D0	D17-D0: 18-bit data
1	0	0	1	8080 MCU 9-bit parallel type I	DNC	NWR	D7-D0	D8-D0: 9-bit data
1	0	1	0	8080 MCU 18-bit parallel type II	DNC	NWR	D8-D1	D17-D0: 18-bit data
1	0	1	1	8080 MCU 9-bit parallel type II	DNC	NWR	D17-D10	D17-D9: 9-bit data
Other Setting				Setting Invalid				

Table 5.1 Input bus format selection of system interface circuit

It has an Index Register (IR) in HX8347-D to store index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

4. Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3 to +4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +4.6	Note(3)
Power Supply Voltage 3	DDVDH ~ VSSA	V	-0.3 to +6.6	Note(4)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3 to +4.6	Note(5)
Power Supply Voltage 5	DDVDH ~ VCL	V	-0.3 to +9	Note(6)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3 to +18.5	Note(7)
Power Supply Voltage 7	VSSA ~ VGL	V	0 to -16.5	Note(8)
Logic Input Voltage	V_{IN}	V	-0.3 to IOVCC+0.5	-
Logic Output Voltage	Vo	V	-0.3 to IOVCC+0.5	-
Operating Temperature	Topr	℃	-40 to +85	Note(9),(10)
Storage Temperature	Tstg	℃	-55 to +110	Note(9),(10)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure DDVDH ≥ VSSA.
(5) To make sure VSSA ≥ VCL.
(6) To make sure DDVDH ≥ VCL.
(7) To make sure VGH ≥ VSSA.
(8) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(9) For die and wafer products, specified up to +85℃.
(10) This temperature specifications apply to the TCP package.

5. Electrical Characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
IO Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Driver Operating voltage	VCI	Operation voltage	2.3	2.8	3.3	
Source Drive Voltage	VREG1	Triple Pump	3.3	4.65	4.8	
	VREG1	Dual Pump	3.3	4.65	5.8	
Gate Drive High Voltage	VGH	IVGH=100μA (Typ:BT=001) VCI=2.8 Dual Pump	9.5	14.25	-	
		IVGH=100uA (Typ:BT=001) VCI=2.8 Triple Pump	11.6	17.39	-	
Gate Drive Low Voltage	VGL	IVGL=100μA (Typ:BT=001) VCI=2.8 Dual Pump	-6.85	-9.5	-	
		IVGL=100μA (Typ:BT=001) VCI=2.8 Triple Pump	-8.46	-11.59	-	
Drive Supply Voltage	|VGH-VGL|	-	-	-	30	
Input / Output						
High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
High level output voltage	VOH	IOH=-1.0mA	0.8IOVCC	-	IOVCC	
Low level output voltage	VOL	IOL=+1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	μA
Oscillator frequency	fOSC	Frame rate at 65hz,default Vs and Hs setting T_A=25℃	2.76	2.85	2.94	MHz
Booster(VCI=2.8V)						
DDVDH boost voltage1	DDVDH	Dual Pump IDDVDH=1mA	4.8	5.0	5.2	V
		Triple Pump IDDVDH=1mA	5.9	6.1	6.3	
VCL boost voltage	VCL	ICL=-300μA	-2.5	-2.65	2.75	
VCOM Generator(VCI=2.8V)						
VCOM amplitude	VCOM	No load, Dual Pump	2.5	4.4	7.3	V
		No load Triple Pump	2.5	4.4	8.3	V
VCOM high level	VCOMH	No load Dual Pump	2.5	3.205	4.8	V
		No load Triple Pump	2.5	3.205	5.8	V
VCOM low level	VCOML	No load	-2.5	-1.195	VSSD	V
Source Driver(Typ:T_A=25℃ VCI=2.8v)						
Output voltage deviation (mean value)	DVOS	VSSD+1.0 ~ VREG1-1.0	-	+/-10	+/-20	mV
		VSSD+0.1V ~ VSSD+1.0 VREG1-1.0 ~ VREG1-0.1V	-	+/-30	+/-50	mV
Output voltage range	VOS	-	0.1	-	DDVDH-0.1	V
Output offset voltage	Voff	-		+/-30	+/-50	mV

6.Timing Characteristics.

6.1 Reset Timing Characteristics.

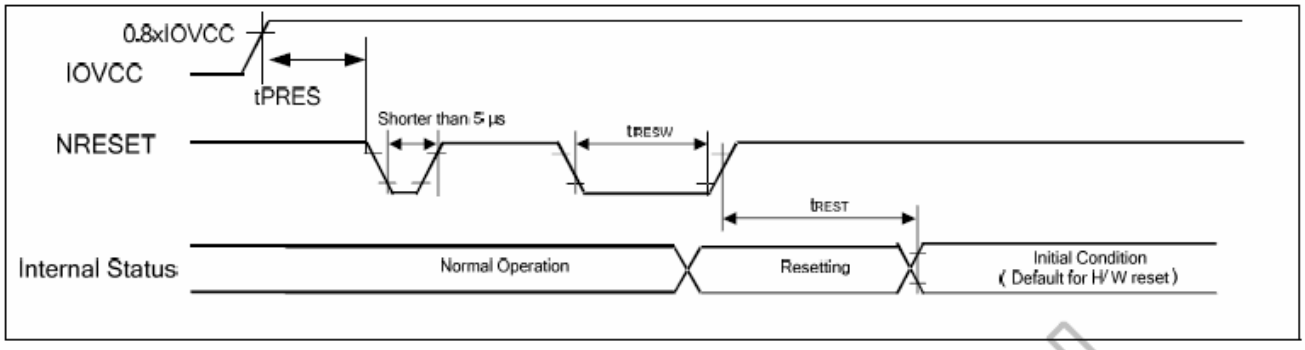


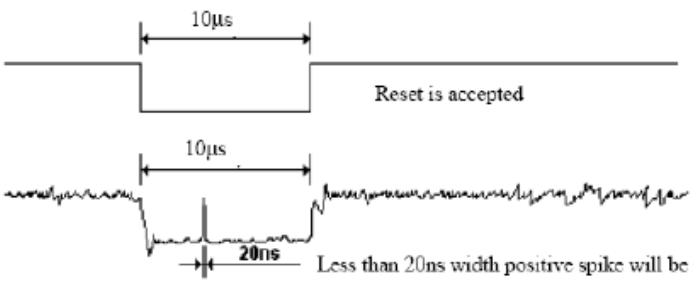
Figure 11.5 Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	-	-	5	When reset applied during STB OUT mode	ms
		-		-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, VMF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



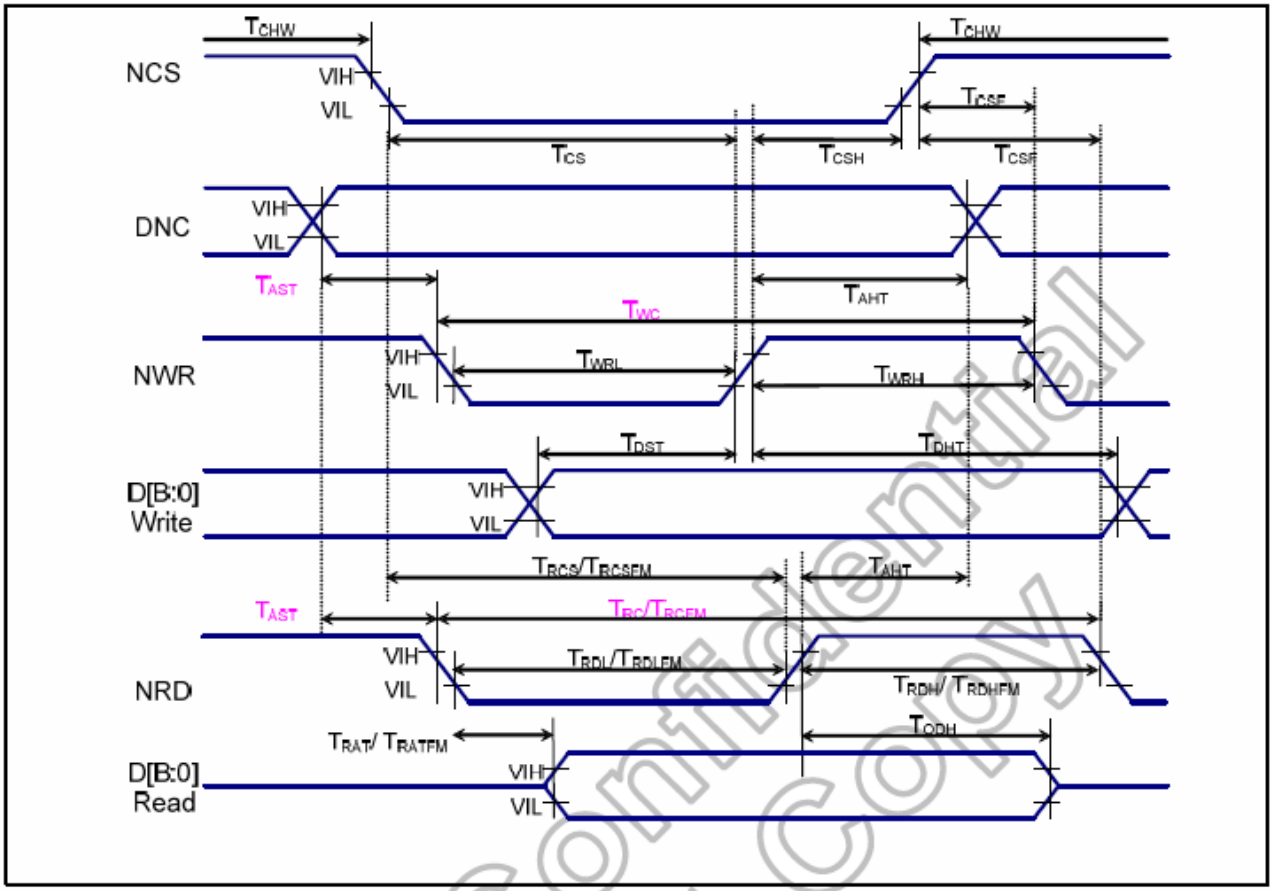
(5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out

6.2. i80-System Interface Timing Characteristics.

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70° C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	tAST	Address setup time	0	-	ns	-
	tAHT	Address hold time (Write/Read)	10	-		
NCS	tCHW	Chip select "H" pulse width	0	-	ns	-
	tCS	Chip select setup time (Write)	15	-		
	tRCS	Chip select setup time (Read ID)	45	-		
	tRCSFM	Chip select setup time (Read FM)	355	-		
	tCSF	Chip select wait time (Write/Read)	10	-		
	tCSH	Chip select hold time	10	-		
NWR_SCL	tWC	Write cycle	66	-	ns	-
	tWRH	Control pulse "H" duration	15	-		
	tWRL	Control pulse "L" duration	15	-		
NRD(ID)	tRC	Read cycle (ID)	160	-	ns	When read ID data
	tRDH	Control pulse "H" duration (ID)	90	-		
	tRDL	Control pulse "L" duration (ID)	45	-		
NRD(FM)	tRCFM	Read cycle (FM)	450	-	ns	When read from frame memory
	tRDHFM	Control pulse "H" duration (FM)	90	-		
	tRDLFM	Control pulse "L" duration (FM)	355	-		
DB17 to DB0	tDST	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tDHT	Data hold time	10	-		
	tRAT	Read access time (ID)	-	40		
	tRATFM	Read access time (FM)	-	340		
	tODH	Output disable time	20	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



6.3. Serial Interface Timing Characteristics.

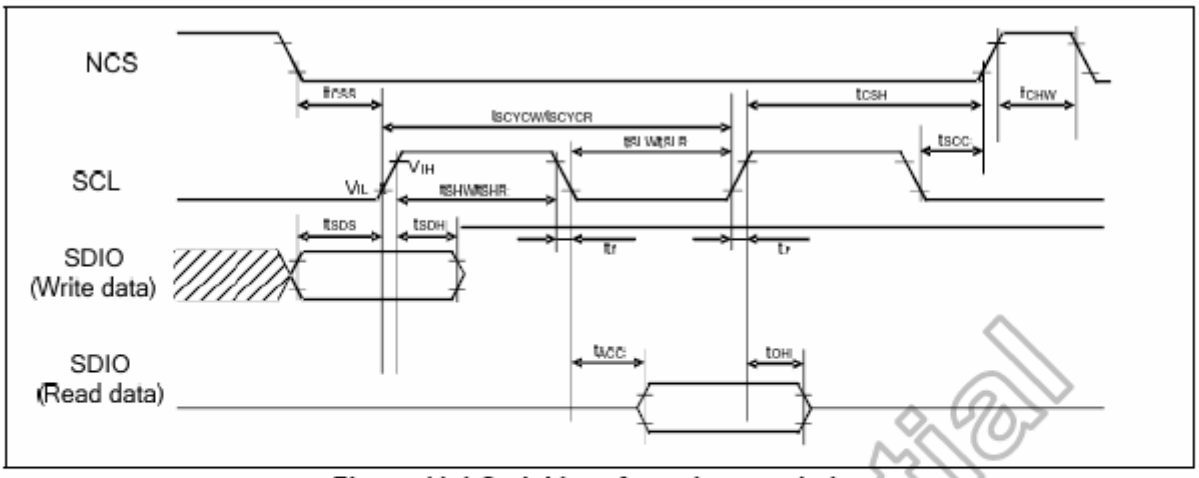


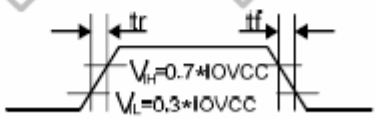
Figure 11.4 Serial interface characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A=-30 to 70° C)

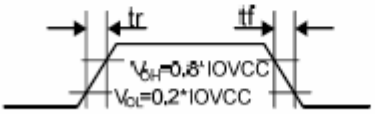
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	tSCYCW tSHW tSLW	SCL	20 8 8	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	tSDS tSDH	SDIO	10 10	- -	- -	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	tSCYCR tSHR tSLR	SCL	150 60 60	- - -	- - -	ns
Access Time	tACC	SDI for maximum CL=30pF For minimum CL=8pF	10	-	50	ns
Output disable time	tOH	SDO For maximum CL=30pF For minimum CL=8pF	15	-	50	ns
SCL to Chip select	tSCC	SCL, NCS	20	-	-	ns
NCS "H" pulse width	tCHW	NCS	40	-	-	ns
Chip select setup time Chip select hold time	tCSS tCSH	NCS	15 15	- -	- -	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

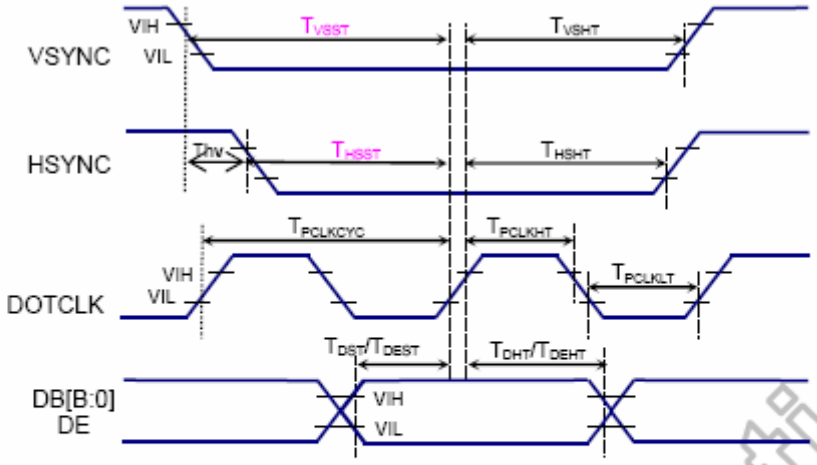
Input Signal Slope



Output Signal Slope



6.4. RGB Interface Timing Characteristics.

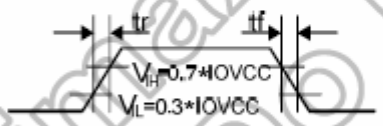


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,Ta = -30 to 70° C)

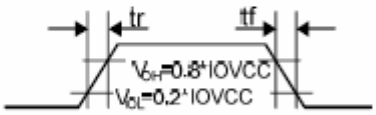
Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Pixel low pulse width	T_{CLKLT}	-	15	-	-	ns
Pixel high pulse width	T_{CLKHT}	-	15	-	-	ns
Vertical Sync. set-up time	T_{VSST}	-	15	-	-	ns
Vertical Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Horizontal Sync. set-up time	T_{HSST}	-	15	-	-	ns
Horizontal Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Data Enable set-up time	T_{DEST}	-	15	-	-	ns
Data Enable hold time	T_{DEHT}	-	15	-	-	ns
Data set-up time	T_{DST}	-	15	-	-	ns
Data hold time	T_{DHT}	-	15	-	-	ns
Phase difference of sync signal falling edge	Thv	-	0	-	240	Dotclk

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

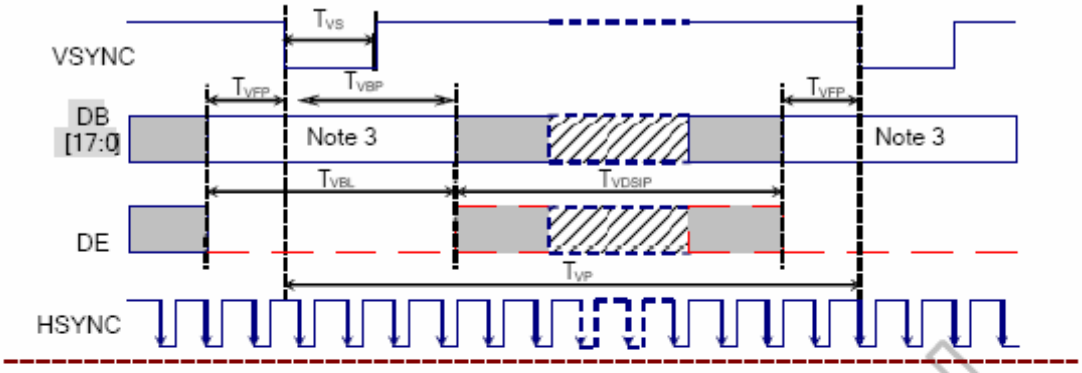
Input Signal Slope



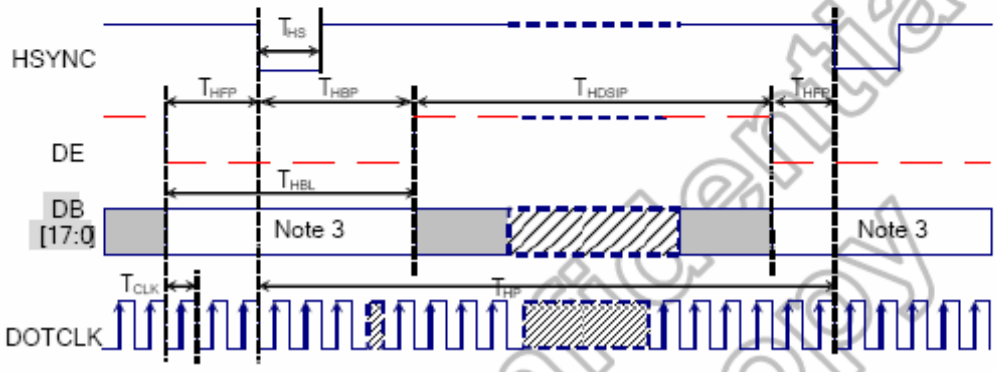
Output Signal Slope



Vertical Timing for RGB I/F



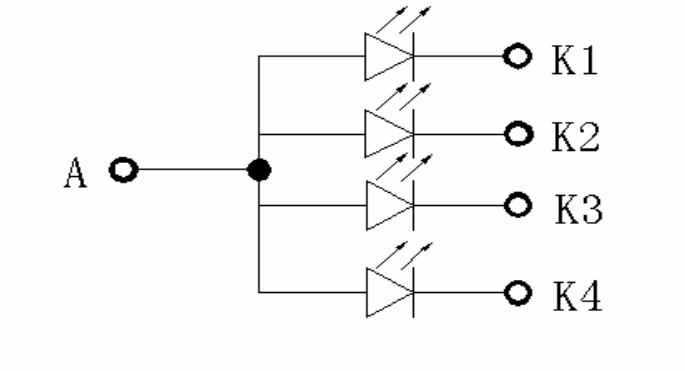
Horizontal Timing for RGB I/F



Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical Timing						
Vertical cycle period	T_{VP}	-	324	326	452	HS
Vertical low pulse width	T_{VS}	-	2	2	-	HS
Vertical front porch	T_{VFP}	-	2	2	6	HS
Vertical back porch	T_{VBP}	-	2	4	126	HS
Vertical blanking period	T_{VBL}	$T_{VBP}+T_{VFP}$	4	6	132	HS
Vertical active area	T_{VDISP}	-	-	320	-	HS
			-		-	HS
			-		-	HS
Vertical refresh rate	TVRR	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	244	252	1008	DOTCLK
Horizontal low pulse width	T_{HS}	-	2	2	256	DOTCLK
Horizontal front porch	T_{HFP}	-	2	4	256	DOTCLK
Horizontal back porch	T_{HBP}	-	2	8	256	DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP}+T_{HFP}$	4	12	256	DOTCLK
Horizontal active area	T_{HDISP}	-	-	240	-	DOTCLK
Pixel clock cycle TVRR=60Hz	f_{CLKCYC}	-	3.9	-	16.6	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V, T_A=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(3) HP is multiples of DOTCLK.

7. Backlight Characteristics.



Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	**Vf**	**3.0**	**3.2**	**3.4**	**V**	**If=60 mA**	**-**
Supply Current	**If**	**-**	**60**	**-**	**mA**	**-**	**-**
Reverse Voltage	**Vr**	**-**	**-**	**5**	**V**	**10uA**	
Power dissipation	**Pd**	**-**	**192**	**-**	**mW**	**-**	
Luminous Intensity for LCM		-	**280**	-	**Cd/m^2**	**If=60 mA**	
Uniformity for LCM	**-**	**80**	**-**	**-**	%	**If=60 mA**	
Life Time	**-**	**50000**	**-**	**-**	**Hr**	**If=60 mA**	**-**
Backlight Color	**White**						

8.Optical Characteristics

Item		Symbol	Conditions	Specifications Min.	Typ.	Max.	Unit	Note
Transmittance		T%	Viewing normal angle $\theta_X = \theta_Y$ =0°	-	5.8	-	%	All left side data are based on CMO's following condition – 1. LC Type: TN 2. Light Source : CMO LED BLU 3. Film : Nitto Linear Polarizer (NPF-TEG1465DU) 4. Machine : DMS
Contrast Ratio		CR		150	250	-		
Response Time		T_R		-	10	20	ms	
		T_F		-	20	30	ms	
Viewing Angle	Hor.	θ_{X+}	Center CR>10	-	45	-	deg.	
		θ_{X-}		-	45	-		
	Ver.	θ_{Y+}		-	35	-		
		θ_{Y-}		-	15	-		
CF only Chromaticity	Red	X_R	Viewing normal angle $\theta_X = \theta_Y$ =0°	0.602	0.632	0.662		Under C light Simulation CG : NTSC 61%
		Y_R		0.298	0.328	0.358		
	Green	X_G		0.266	0.296	0.326		
		Y_G		0.546	0.576	0.606		
	Blue	X_B		0.103	0.133	0.163		
		Y_B		0.092	0.122	0.152		
	White	X_W		0.274	0.304	0.334		
		Y_W		0.304	0.334	0.364		

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

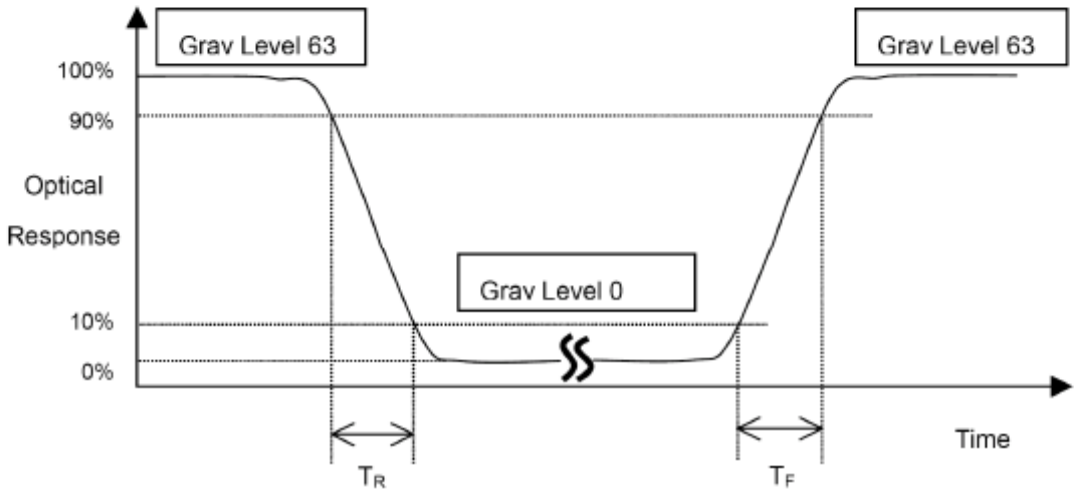
L63: Luminance of gray level 63

L0: Luminance of gray level 0

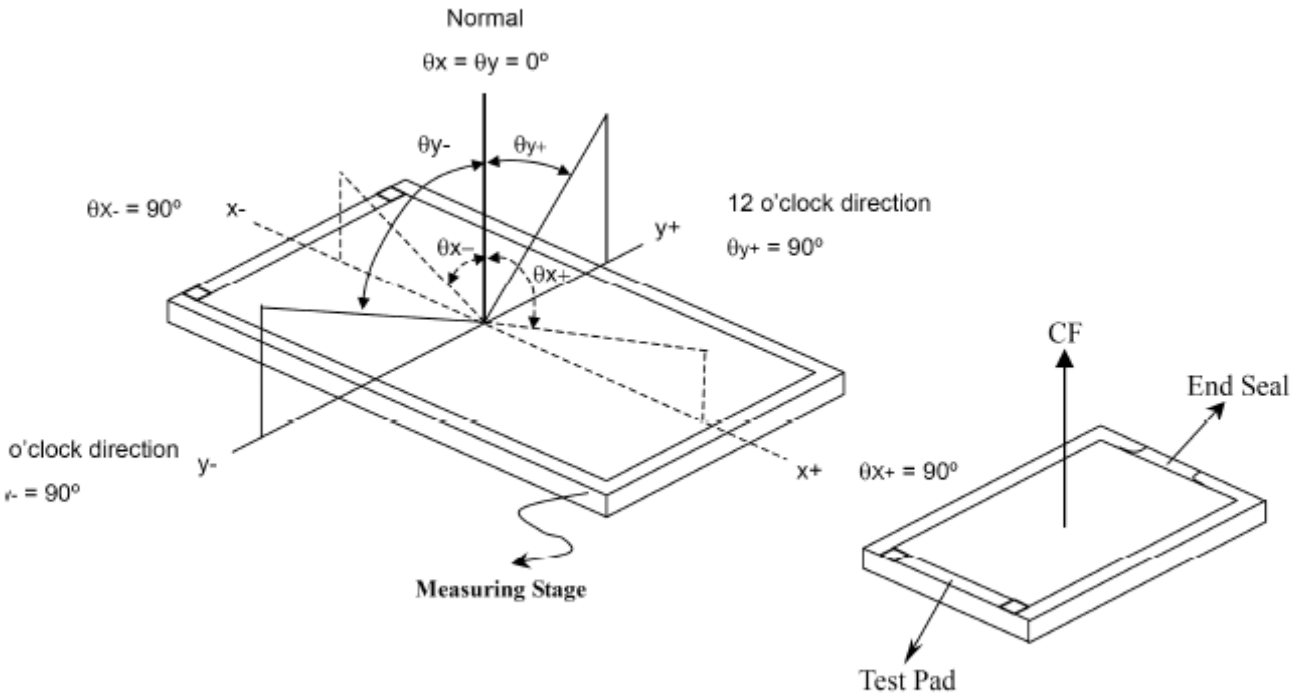
CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

*Note (2) Definition of Response Time (TR, TF):



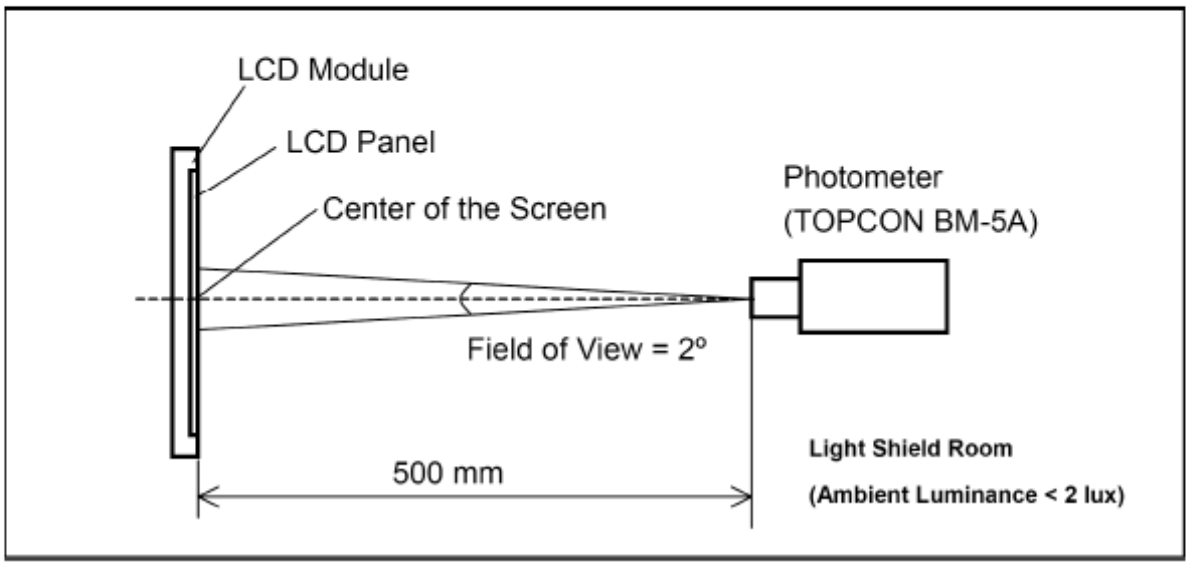
*Note(3) Definition of Viewing Angle



*** The above "Viewing Angle" is the measuring position with Largest Contrast Ratio; not for good image quality. View Direction for good image quality is 6 O'clock. Module maker can increase the "Viewing Angle" by applying Wide View Film.

*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



9. Reliability Test Conditions And Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
①	High Temperature Storage	80℃±2℃×200Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1,Air bublle in the LCD. 2,Sealleak. 3,Non-display. 4,Missing segments. 5,Glass crack. 6,Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric Characteristics requirements shall be satisfied.
②	Low Temperature Storage	-30℃±2℃×200Hours	
③	High Temperature Operating	70℃±2℃×120Hours	
④	Low Temperature Operating	-20℃±2℃/120Hours	
⑤	Temperature Cycle(Storage)	-30℃±2℃ ⟺ 25℃ 80℃±2℃ (30min) (5min) (30min) 1cycle Total 10cycle	
⑥	Damp Proof Test	50℃±5℃×90%RH×120Hours	
⑦	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (Packing Condition)	
⑧	Drooping Test	Drop to the ground from 1M height one time every side of carton. (Packing Condition)	
⑨	ESD Test	Voltage: ± 8KV,R:330Ω,C:150PF,Air Mode,10times	

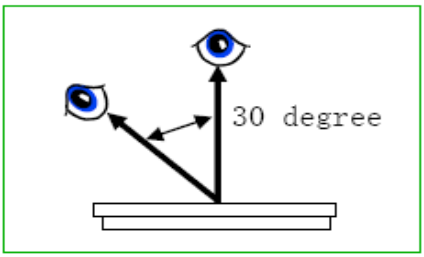
REMARK:
1,The Test samples should be applied to only one test item.
2,Sample side for each test item is 5~10pcs.
3,For Damp Proof Test,Pure water(Resistance＞10MΩ)should be used.
4,In case of malfunction defect caused by ESD damage,if it would be recovered to normal state after resetting,it would be judge as a good part.
5,EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10.Inspection Standard

This standard apply to TFT module specification.

1. Inspection condition:

Under daylight lamp 20~40W, product distance inspector'eye 30cm,incline degree 30° 。



2. Inspection standard

<table>
<tr><th>NO.</th><th>Item</th><th>Inspection standard</th><th>Rate</th></tr>
<tr><td>2.1</td><td>Dot</td><td>Case of Dot defect is below
① Bright Dot (whit spot) : “0”
② Dark Dot (black spot) : “0” (In case of Dark Dot on Main TFT LCD)
- NG if there's full Dot defect.
- Damaged less than the size of sub-pixel is not counted as defect
- Dots darker than the size of sub-pixel are not defined as bright dot defect

<table>
<tr><th>area
size （mm）</th><th>Acceptable number</th></tr>
<tr><td>Φ≤0.10</td><td>ignore</td></tr>
<tr><td>0.10＜Φ≤0.15</td><td>3</td></tr>
<tr><td>0.15＜Φ≤0.20</td><td>2</td></tr>
<tr><td>0.25＜Φ≤0.25</td><td>1</td></tr>
<tr><td>0.25＜Φ</td><td>0</td></tr>
</table></td><td rowspan="2">minor</td></tr>
<tr><td>2.2</td><td>line</td><td>
<table>
<tr><th colspan="2">Size （mm）</th><th>Acceptable number</th></tr>
<tr><td>ignore</td><td>W≤0.03</td><td>ignore</td></tr>
<tr><td>L≤4.0</td><td>0.03＜W≤0.04</td><td>2</td></tr>
<tr><td>L≤4.0</td><td>0.04＜W≤0.05</td><td>1</td></tr>
<tr><td></td><td>0.05＜W</td><td>Treat with dot non-conformance</td></tr>
</table></td></tr>
</table>

11. Handling Precautions

11.1 Mounting method

The LCD panel of FORMIKE ELECTRONIC CO,.LTD. module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

11.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent [recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Salfur (S)

If goods were sent without being sili8con coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (CI), Salfur (S) from customer, Responsibility is on customer.

11.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

11.4 packing

- Module employ LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

11.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit. Usage under the maximum operating temperature, 50%Rh or less is required.

11.6 storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
  It is recommended to store them as they have been contained in the inner container at the time of delivery from us

11.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

12. Precaution For Use

12.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

12.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to FORMIKE ELECTRONIC CO,.LTD,and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.