



Display Future Ltd

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LCD MODULE SPECIFICATION

Model: DF-AMC0548FB-M1

This module uses ROHS materials

For customer acceptance

| | | |
|----------|--|------|
| Customer | | date |
| Approved | | |
| Comments | | |

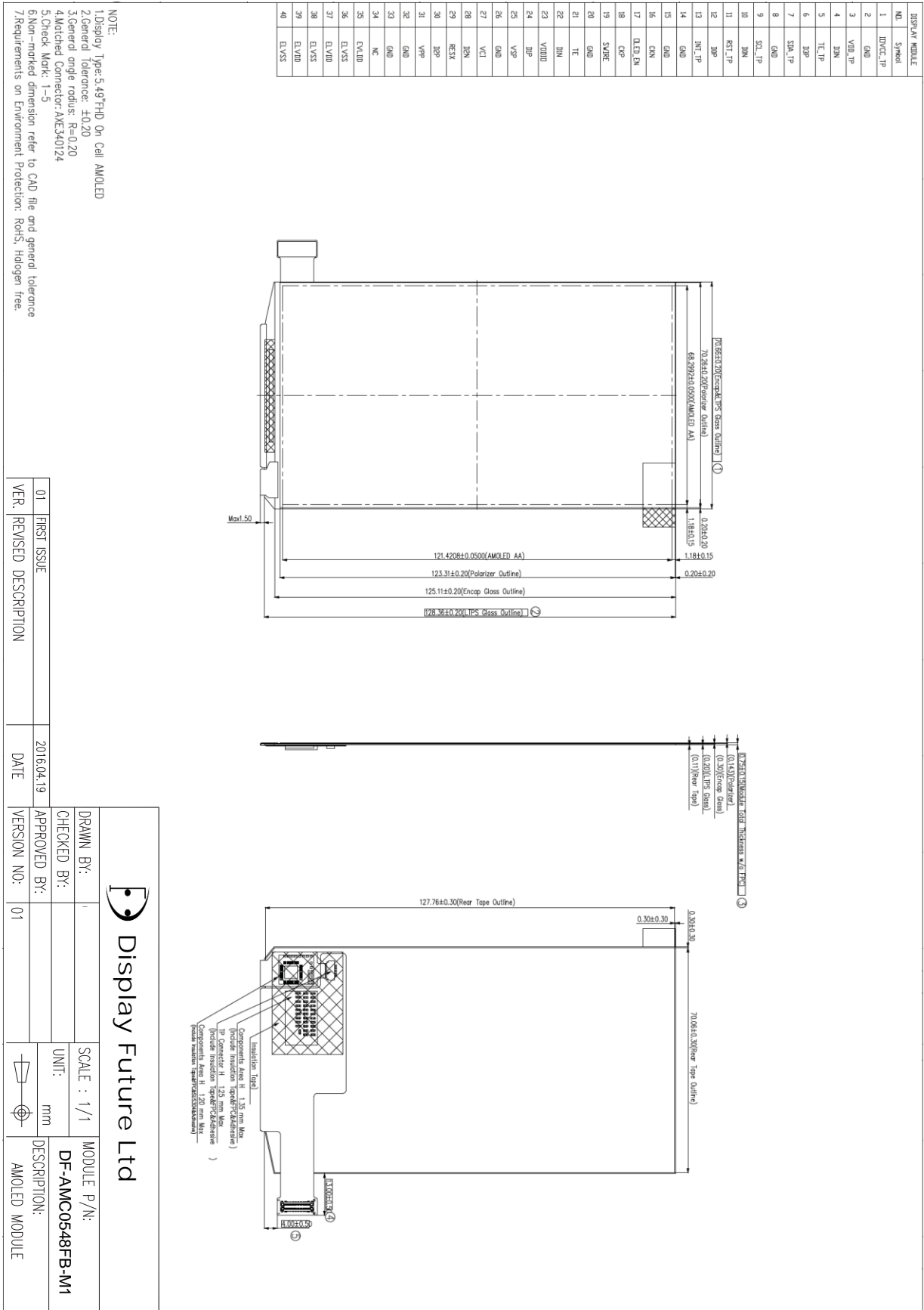
The standard product specification may change without prior notice in order to improve performance or quality. Please contact Display Future Ltd for updated specification and product status before design for the standard product or release of the order.

| | |
|---------------|-----------|
| Revision | 1.0 |
| Engineering | |
| Date | 2018/01/8 |
| Our Reference | |

■ PHYSICAL DATA

| No. | Items | Specification | Unit |
|-----|-------------------|-----------------------------------|-----------------|
| 1 | Display Mode | AMOLED | - |
| 2 | Display Color | 16.7M(RGB x 8bits) | - |
| 3 | Diagonal Size | 5.49 | Inch |
| 4 | Resolution | 1080 RGB x 1920(Rendering) | Dots |
| 5 | Active Area | 68.299(W) x 121.421(H) | mm ² |
| 6 | Outline Dimension | 70.66 (W) x 128.36 (H) x 0.75 (D) | mm ³ |
| 7 | Pixel Pitch | 0.3162 (W) x 0.6324 (H) | mm ² |
| 8 | Driver IC | RM67191 W/RAM(Raydium) | - |
| 9 | Touch IC | S3508 or GT1151 | - |
| 10 | Interface | MIPI 4 lanes | - |
| 11 | Touch screen | On-cell | - |
| 12 | Polarizer | Hard coating polarizer | - |
| 13 | Weight | TBD | g |

EXTERNAL DIMENSIONS



■ ABSOLUTE MAXIMUM RATINGS

| Items | Symbol | Min | Max | Unit | Notes |
|----------------------------|---------------|------------|------------|-------------|--------------|
| Analog/boost power voltage | VCI | -0.3 | 5.28 | V | - |
| VCI I/O voltage | VCI_IF | -0.3 | 5.28 | V | - |
| I/O voltage | VDDIO | -0.3 | 3.96 | V | - |
| VSP voltage | VSP | - | 6.5 | V | - |
| VPP (OTP power) | VPP | - | 8.64 | V | - |
| TP power voltage | VDD3 | -0.3 | 3.6 | V | - |
| TP I/O digital voltage | IOVCC | 1.8 | 3.6 | V | - |
| Operating temperature | TOP | -20 | 60 | °C | - |
| Storage temperature | TST | -30 | 70 | °C | - |

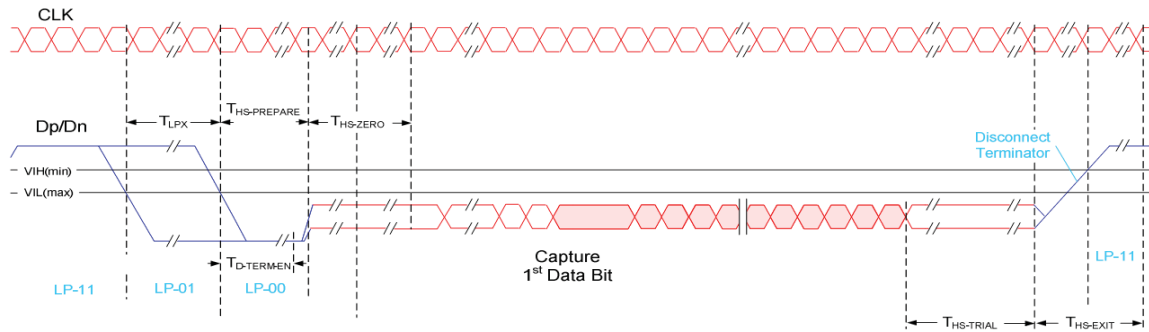
■ ELECTRICAL CHARACTERISTICS

◆ DC Characteristics

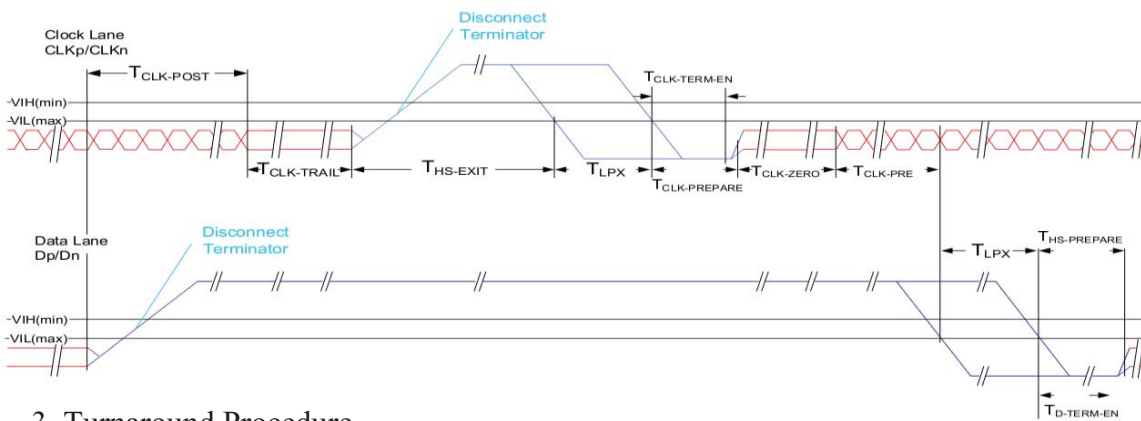
| Items | Symbol | Min | Typ. | Max | Unit | Remark |
|-------------------------|--------------------------|------|------|------|------|-------------------------|
| AMOLED power positive | ELVDD | - | 4.6 | - | V | |
| AMOLED power negative | ELVSS | - | -2.5 | - | V | Ref |
| Gamma voltage | VSP | 6.1 | 6.4 | 6.5 | V | Ref |
| Digital power supply | VDDI | 1.65 | 1.8 | 3.6 | V | Ref |
| Analog power supply | VCI | 2.5 | 3.3 | 4.8 | V | Ref |
| TP power supply voltage | VDD_TP | 2.8 | - | 3.6 | V | |
| TP logic input voltage | VIH | 1.26 | - | 1.8 | V | |
| | VIL | -0.3 | - | 0.54 | V | |
| TP logic output voltage | VOH | 1.26 | - | - | V | |
| | VOL | - | - | 0.54 | V | |
| 350 ANSI@Gray 255 | I _{ELVDD/ELVSS} | - | 210 | 275 | mA | VELVDD=4.6V |
| | IVCI | - | 2 | 3 | mA | VELVSS=-2.5V |
| | IVDDIO | - | 50 | 60 | mA | VCI=3.3V |
| | IVSP | - | 15 | 17 | mA | VDDIO=1.8V VSP=6.1V |
| Normal operation | Iopr | - | 13.2 | - | mA | |
| Monitor | Imon | - | 0.43 | - | mA | VDD_TP=3V MCLK=24MHz |
| Sleep | Islp | - | 42 | - | uA | |

◆ AC Characteristics

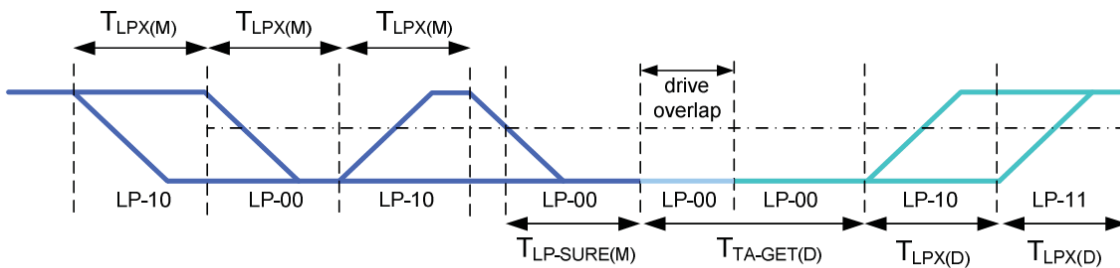
1. HS Data Transmission Burst



2. HS Clock Transmission



3. Turnaround Procedure



4. Timing Parameters

| Symbol | Description | Min | Typ | Max | Unit |
|-------------------------|--|------------------------|-----|-----|------|
| T _{TREOT} | 30%-85% rise time and fall time | - | - | 35 | ns |
| T _{CLK-MISS} | Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX. | - | - | 60 | ns |
| T _{CLK-POST*1} | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T _{HS-TRAIL} to the beginning of T _{CLK-TRAIL} . | 60ns + 52*UI (For DCS) | - | - | ns |

| | | | | | |
|------------------------|--|-------------------------------|--------|----------------|----|
| TCLK-PRE | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | - | - | ns |
| TCLK-SETTLE | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE. | 95 | - | 300 | ns |
| TCLK-TERM-EN | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX. | Time for Dn to reach VTERM-EN | | 38 | ns |
| THS-SETTLE | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THSPREPARE. | 85 ns + 6*UI | | 145 ns + 10*UI | ns |
| TEOT | Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state | - | - | 105ns+48*UI | ns |
| THS-EXIT(1) | time to drive LP-11 after HS burst | 100 | - | - | ns |
| THS-PREPARE | Time to drive LP-00 to prepare for HS transmission | 40ns + 4*UI | - | 85ns+6*UI | ns |
| THS-PREPARE + THS-ZERO | THS-PREPARE + Time to drive HS-0 before the Sync sequence | 145ns + 10*UI | - | - | ns |
| THS-SKIP | Time-out at RX to ignore transition period of EoT | 40 | - | 55ns+4*UI | ns |
| THS-TRAIL | Time to drive flipped differential state after last payload data bit of a HS transmission burst | 60 + 4*UI | - | - | ns |
| TLPX | Length of any Low-Power state period | 50 | - | - | ns |
| Ratio TLPX | Ratio of TLPX(MASTER)/TLPS(SLAVE) between Master and Slave side | 2/3 | - | 3/2 | ns |
| TTA-GET | Time to drive LP-00 by new TX | 5*TLPX | 5*TLPX | 5*TLPX | ns |

| | | | | | |
|----------------------|--|--------|--------|--------|----|
| T _{TA-GO} | Time to drive LP-00 after Turnaround Request | 4*TLPX | 4*TLPX | 4*TLPX | ns |
| T _{TA-SURE} | Time-out before new TX side starts driving | TLPX | - | 2*TLPX | ns |

5. Timing Requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset.

When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.6V, VSS=0V, T_A=-20°C~+85°C)

| Parameter | Symbol | Conditions | Spec | | | Unit |
|-----------------------|--------|------------|------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Reset low pulse width | Trst | - | 20 | - | - | μs |

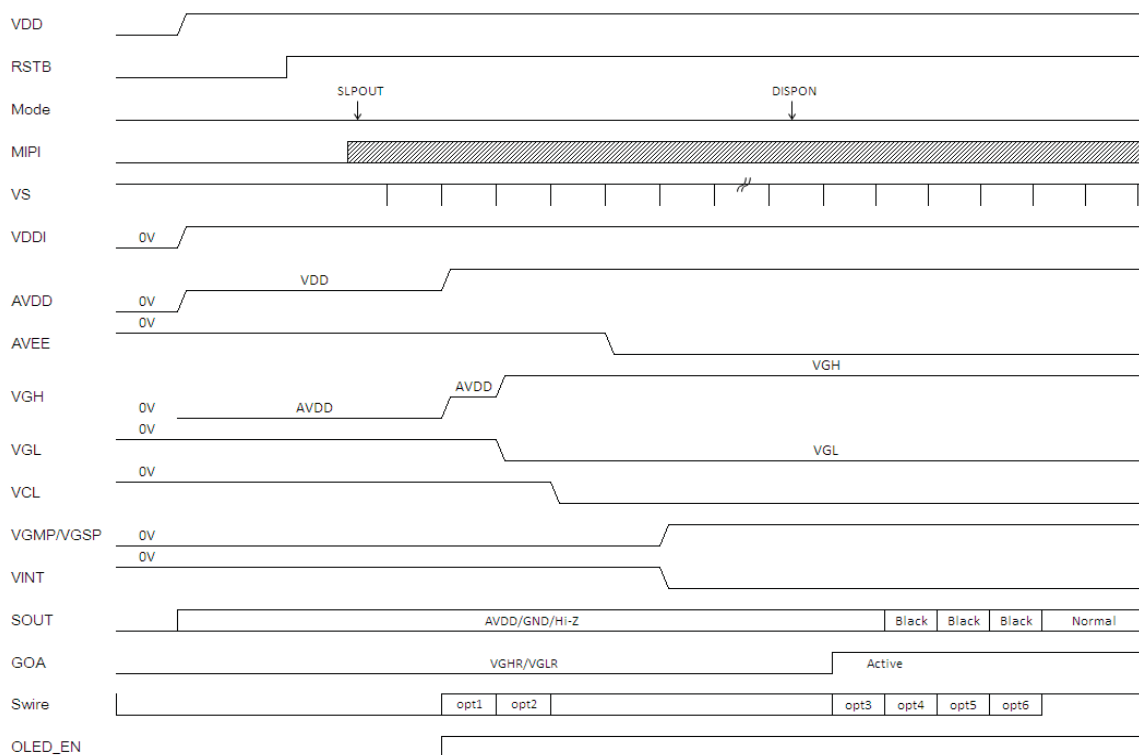
Table: Reset timing



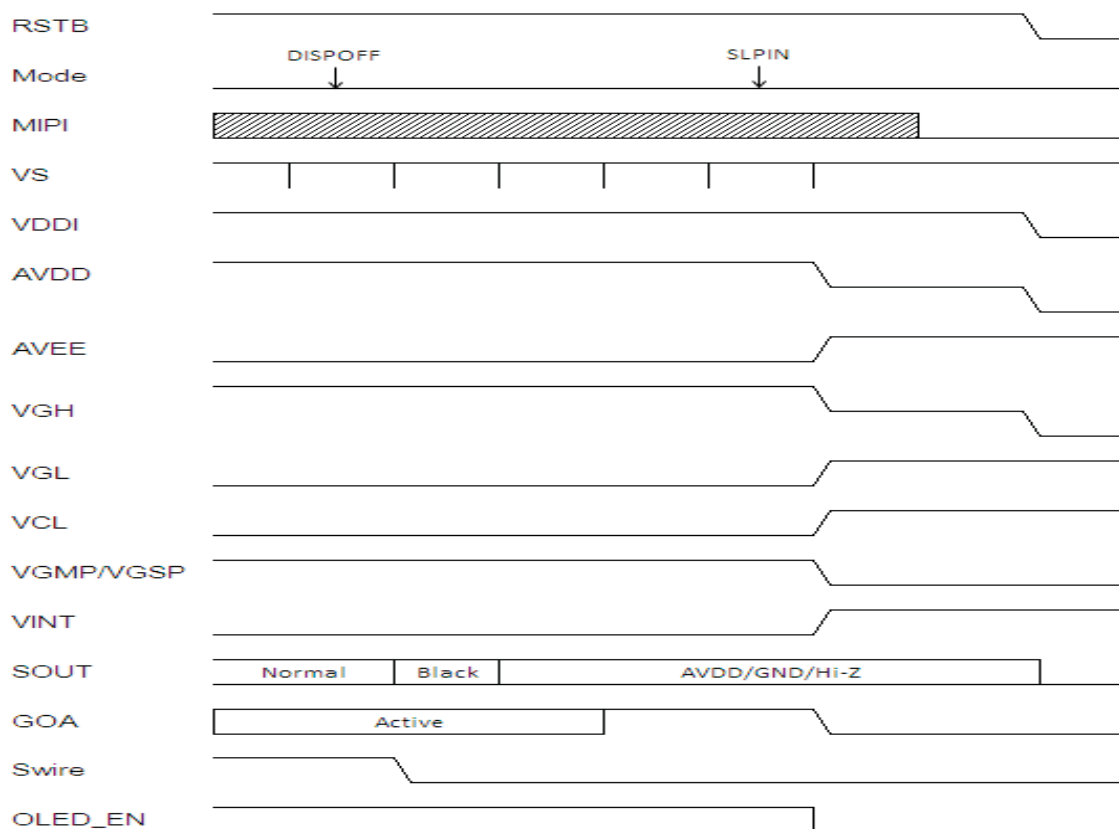
Figure: Reset timing

6. Recommended Operating Sequence

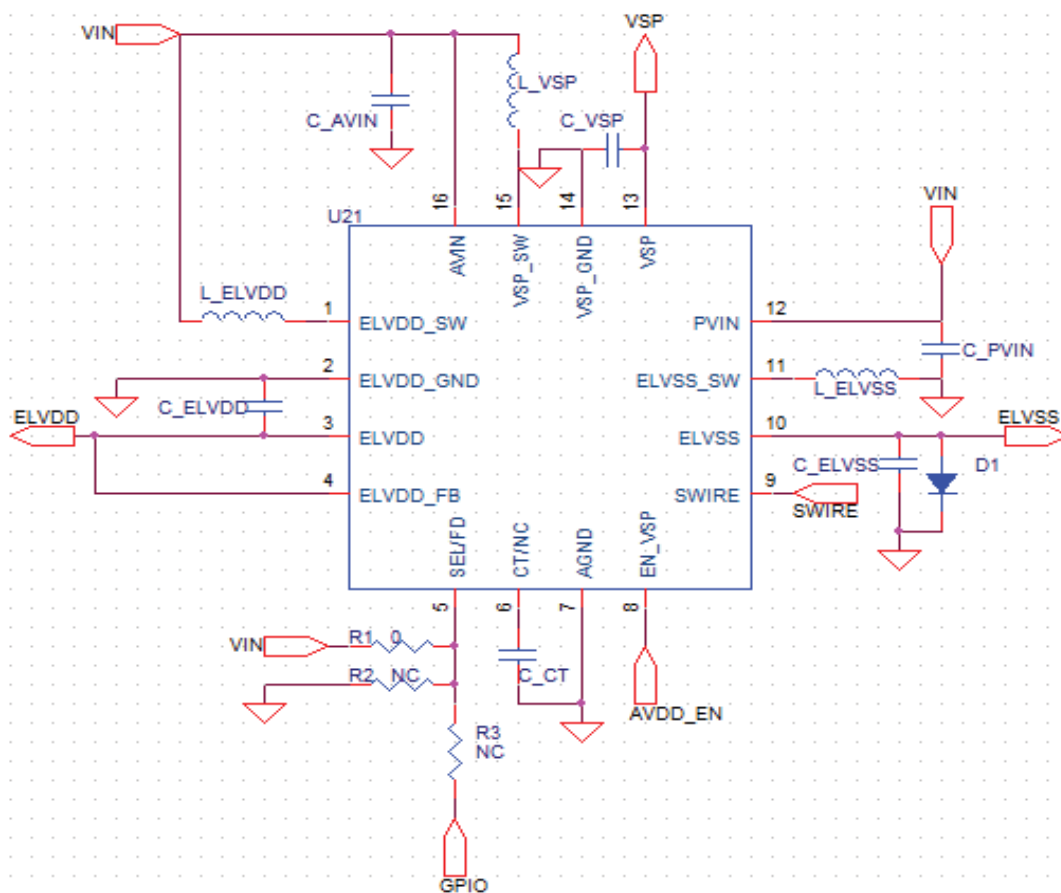
6.1 Power ON Sequence



6.2 Power OFF Sequence



◆ APPLICATION CIRCUIT



■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

| Item | Symbol | Condition | Min | Typ | Max | Unit | Remark | |
|-------------------------|--------|---|-------------------|-------|------|-------------------|--------|------|
| Brightness | Lv | Full white | 300 | 350 | - | cd/m ² | Note 2 | |
| Brightness uniformity | - | Full white | 70 | 85 | - | % | | |
| Contrast ratio | Cr | Normal to surface | 8000 | 10000 | - | - | | |
| CIE (x, y) chromaticity | Red | x | Normal to surface | 0.63 | 0.66 | 0.69 | - | Ref. |
| | | y | | 0.31 | 0.34 | 0.37 | | |
| | Green | x | | 0.16 | 0.21 | 0.26 | | |
| | | y | | 0.67 | 0.72 | 0.77 | | |
| | Blue | x | | 0.09 | 0.13 | 0.17 | | |
| | | y | | 0.02 | 0.06 | 0.10 | | |
| | White | x | | 0.28 | 0.30 | 0.32 | | |
| | | y | | 0.30 | 0.32 | 0.34 | | |
| Color gamut | - | vs.NTSC | 80 | 100 | - | % | - | |
| Viewing angle | - | U/D/L/R CR≥1000 | 80 | 85 | - | - | - | |
| Cross-talk | - | 4% black or white window,117 gray scale | - | - | 5 | % | Note 3 | |
| Gamma | - | V(gray)=48,72,104,132,164,192,224,255 | 1.9 | 2.2 | 2.5 | - | - | |
| Color shift | - | @30 degree | - | 4 | 5 | JNCD | Note 4 | |
| Response time | - | | - | - | 2 | ms | Note 5 | |

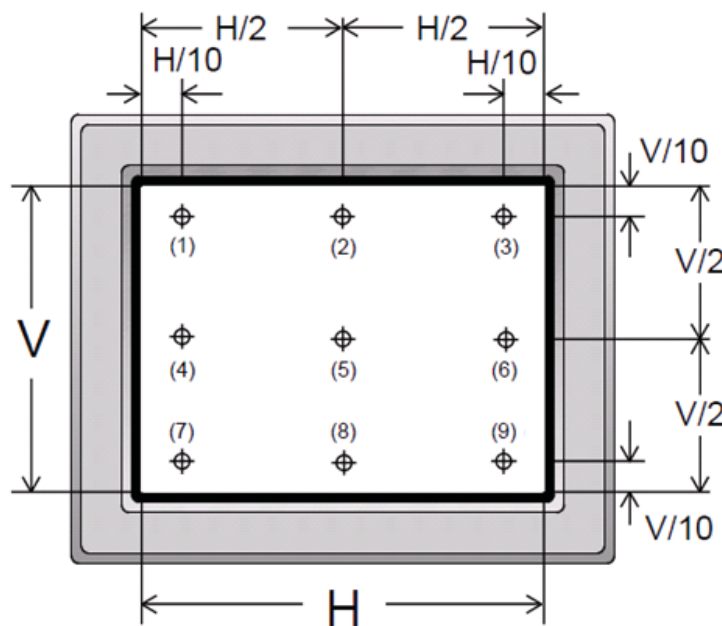
Note1: Temp.25 °C, (Angle, distance)

Environmental conditions: Temp.25°C±3°C, 65± 20%RH, Dark Room.
Distance of OLED display center to measuring machine is 50cm

Note2: Brightness Uniformity definition

Measure 9 points of Display Brightness,

$$\text{Brightness Uniformity} = L_{\min} / L_{\max} \times 100\%$$



⊕ Denote 9-point locations.
(1), (2), (3), ..., (9)

Contrast Ratio:

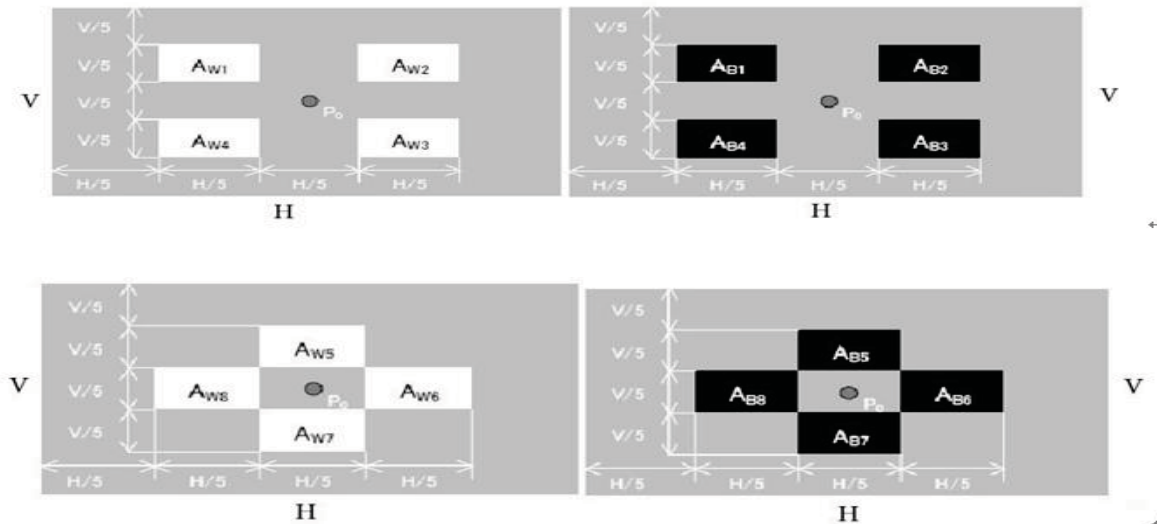
Dark Room C.R=LW/LB

LW: full white brightness of display center P0

LB : full black brightness of display center P0

Note3: Cross-talk

4% black or white window ,117 gray background.



$$L_{W_OFF} = \frac{L_{w1} + L_{w2} + L_{w3} + L_{w4}}{4}$$

$$L_{B_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$CT = \frac{|L_{Wi_ON} - L_{W_OFF}|}{L_{W_OFF}} \times 100\% (i = 5 \text{ to } 8)$$

For white windows A_{wi} (i = 5 to 8), and

$$CT = \frac{|L_{Bi_ON} - L_{B_OFF}|}{L_{B_OFF}} \times 100\% (i = 5 \text{ to } 8)$$

For black windows A_{Bi} (i = 5 to 8).

The maximum cross-talk value shall be noted in the measurement report.

Note4: Color Shift JNCD

For JNCD measure:

Fix on one pattern like white pattern,

On the condition $\theta=0$ $F=0^\circ$, we can get the color coordinate $(u1', v1')$ and on $\theta F=30^\circ$ we can get another color coordinate $(u2', v2')$

$$\Delta = \text{Square Root}(u2'-u1')^2 + (v2'-v1')^2$$

JNCD stands for "Just Noticeable Color Difference"

For the (u', v') color space JNCD=0.0040

2JNCD means $\Delta u'v' < 0.0080$

For color shift we need to measure white/red/green/blue pattern.

This requirement is from our customer and we have test some of our phone display and the result is OK.

Note5: Response Time

Response time=Pixel turn on and turn off time (White \rightleftharpoons Black).

It is measuring transition time from 10% to 90% of luminance.

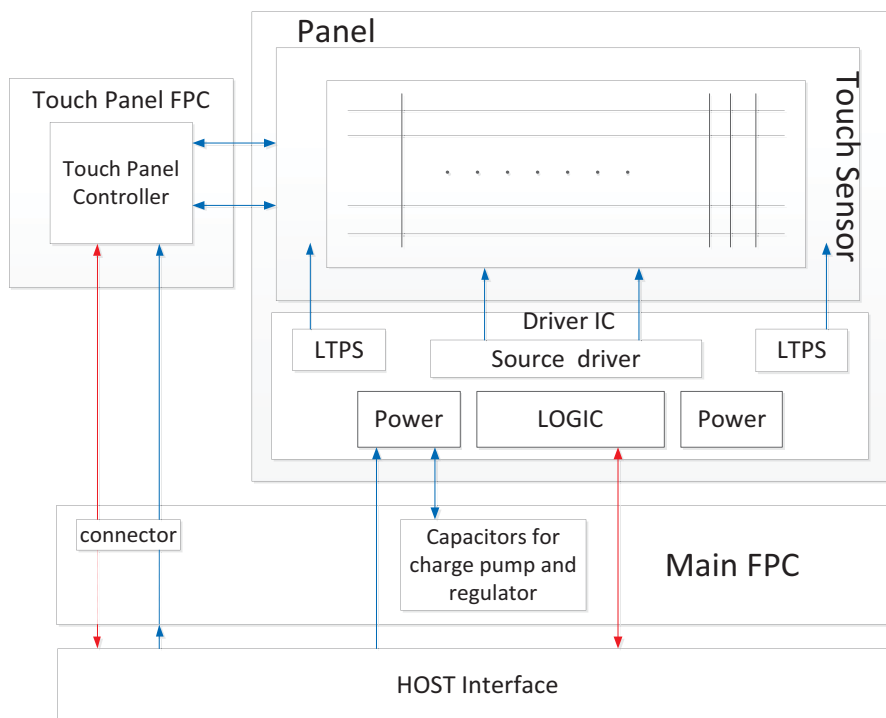
■ INTERFACE PIN CONNECTIONS

1. I/O Connection

| P/N | Pin_name | I/O | Description |
|-----|----------|-------|--|
| 1 | IOVCC_TP | Power | I/O Power Supply |
| 2 | GND | Power | The power ground |
| 3 | VDD_TP | Power | Digital power supply |
| 4 | D3N | I | MIPI DSI data3- |
| 5 | TE_TP | I | LCD Sync |
| 6 | D3P | I | MIPI DSI data3+ |
| 7 | SDA_TP | I/O | I2C Data Input & Output |
| 8 | GND | Power | The power ground |
| 9 | SCL_TP | I/O | I2C Clock Input |
| 10 | D0N | I/O | MIPI DSI data0- |
| 11 | RST_TP | I | External Reset,Low is Active |
| 12 | D0P | I/O | MIPI DSI data0+ |
| 13 | INT_TP | I | Interrupt request to the host, or Wakeup request from the host. |
| 14 | GND | Power | The power ground |
| 15 | GND | Power | The power ground |
| 16 | CKN | I | MIPI DSI clock- |
| 17 | OLED_EN | O | Power IC enable |
| 18 | CKP | I | MIPI DSI clock+ |
| 19 | SWIRE | O | Power IC control pin |
| 20 | GND | Power | The power ground |
| 21 | TE | O | Tear effect output |
| 22 | D1N | I | MIPI DSI data1- |
| 23 | VDDIO | Power | Driver IC digital I/O supply |
| 24 | D1P | I | MIPI DSI data1+ |
| 25 | VSP | Power | PFM's Voltage |
| 26 | GND | Power | The power ground |
| 27 | VCI | Power | Driver IC analog supply |
| 28 | D2N | I | MIPI DSI data2- |
| 29 | RESX | I | This signal will reset the device and must be applied to properly initialize the chip. Active low. |
| 30 | D2P | I | MIPI DSI data2+ |

| | | | |
|----|-------|-------|---|
| 31 | VPP | Power | Power supply for OTP. Leave the pin to open when not in use. |
| 32 | GND | Power | The power ground |
| 33 | GND | Power | The power ground |
| 34 | NC | - | No connection |
| 35 | ELVDD | Power | AMOLED power Positive |
| 36 | ELVSS | Power | AMOLED power Negative |
| 37 | ELVDD | Power | AMOLED power Positive |
| 38 | ELVSS | Power | AMOLED power Negative |
| 39 | ELVDD | Power | AMOLED power Positive |
| 40 | ELVSS | Power | AMOLED power Negative |

2. Display Module Block Diagram



■ RELIABILITY TESTS

1. Environmental Test

| No | Item | Conditions | Note |
|----|-------------------------------------|---|------|
| 1 | High Temperature Operation | 70°C / 128hours | |
| 2 | Low Temperature Operation | -20°C / 128hours | |
| 3 | High Temperature Storage | 85°C 128hrs | |
| 4 | Low Temperature Storage | -40°C 128hrs | |
| 5 | High Temperature Humidity Operation | 60°C/93% RH96hrs | |
| 6 | High Temperature Humidity Storage | 60°C/93% RH96hrs | |
| 7 | Thermal Shock | -20°C ~ 70°C 30min,change time <5min, 10 cycles | |

2. Electrical Test

| No | Item | Conditions |
|----|-------------------|-------------------------------------|
| 1 | Air discharge | ±8KV,150PF/330 Ω (Module level) |
| 2 | Contact discharge | ±4KV, 150PF/330 Ω (Module level) |

3. Mechanical Test

| No | Item | Conditions | Note |
|----|---------------------|--|----------------|
| 1 | Glass Strength Test | 4PB, B10 >100MPa | |
| 2 | Ball Drop Test | Min 0.2J @ center (Φ20mm,32.5g,62.5cm) | Module with CL |
| 3 | Shock Test | Half Sine, 60G, duration time 6 ms , 3 times for each direction , total 6 shocks | Module |

| | | | |
|---|---------------------------|---|---------|
| 4 | Drop Test | GB/T4857.18-19 Test Description For Packages(1 corner, 3 edges, 6 surfaces) | Package |
| 5 | Sinusoidal Vibration Test | Frequency range:10~55Hz,Stroke:1.5mm,Sweep:10Hz~55Hz~10Hz,2hours for each direction of X.Y.Z.(6 hours for total, Package condition) | Package |

■ CAUTIONS IN USING OLED MODULE**◆ Precautions For Handling OLED Module:**

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
 - i. Avoid drop from high, avoid excessive impact and pressure.
 - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
 - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
 - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
 - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
 - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
 - i. Be sure to ground the body when handling the OLED Modules.
 - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
 - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
 - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
 - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
 - vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrode the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{PP}$, and power off sequence: $V_{PP} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module' s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆ **Precautions For Soldering OLED Module:**

1. Soldering temperature : $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ **Precautions For Storing OLED Module:**

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ **Limited Warranty**

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) Display Future will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with Display Future OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to Display Future within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of Display Future is limited to repair and/or replacement on the terms above. Display Future will not be responsible for any subsequent or consequential events.

◆ **Return OLED Module Under Warranty:**

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.